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LMS6002D –Wide Band Multi Standard Radio Chip

Improving Transceiver Performance Using Digital Techniques

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Revision History

Version 1.0r0
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Initial version.

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Made more general.

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Released: Jun 21, 2012
Made more general.

1

Introduction

This document describes frequently asked questions and answers regarding the DC Offset cancelation using third party baseband utilizing the LMS6002D transceiver. The document includes Repeater test which is done on two Lime Evaluation Kits.

2

Lime Setup for Repeater Tests

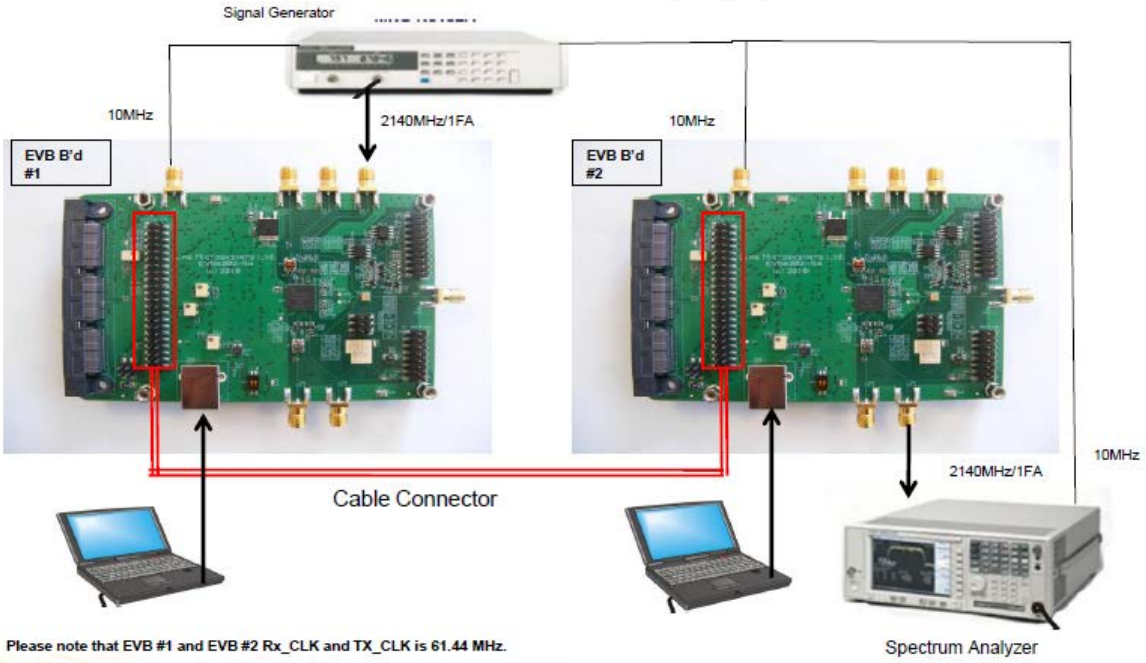


Figure 2.1: Repeater test bench block diagram

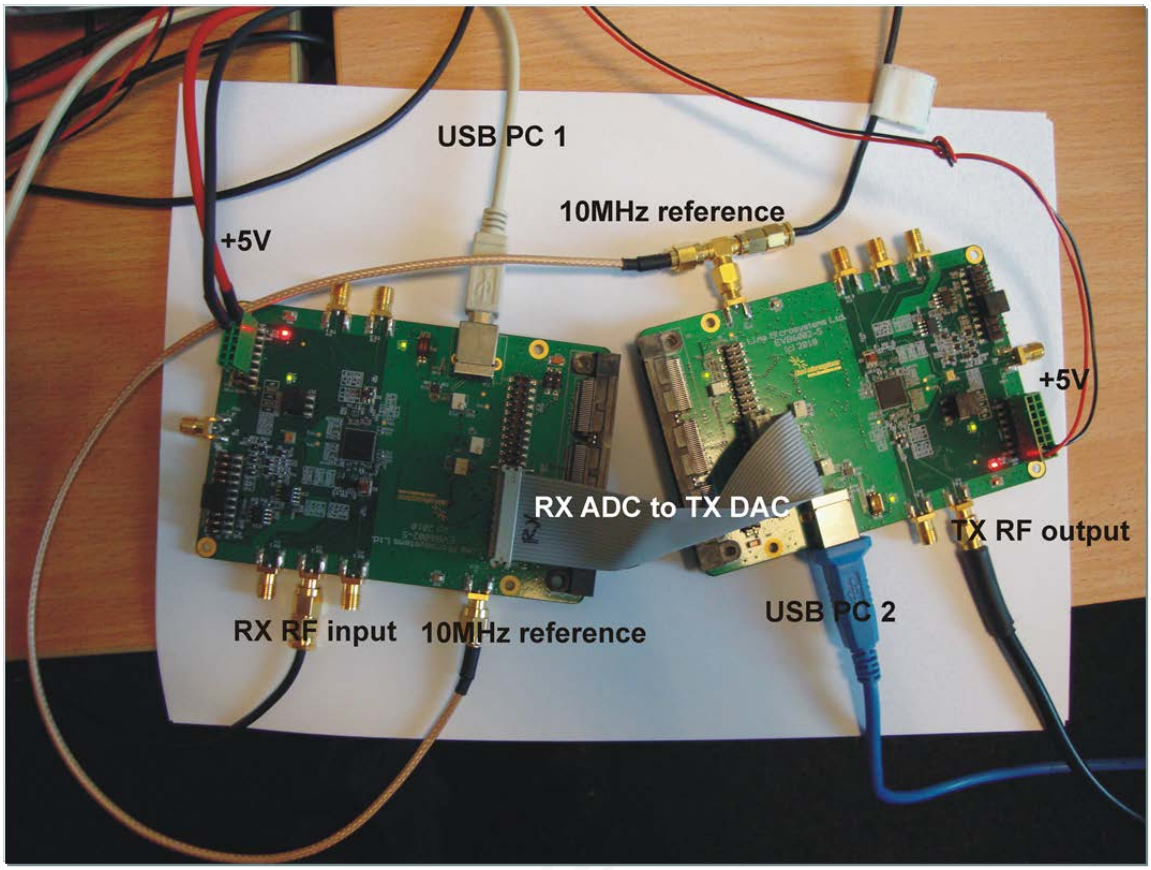


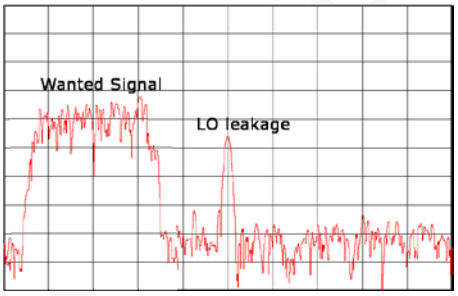
Figure 2.2: Repeater test bench photo

The Lime test bench used in the repeater tests presented in this document is shown in Figures 2.1 and 2.2. Lime is a RF IC chip company so there is no repeater base band in the tests. However, the absence of a base band in the tests will make the performance worse rather than making it better. Hence the Lime results presented in the following text will be even better when a base band is involved (IQ imbalance correction, for example).

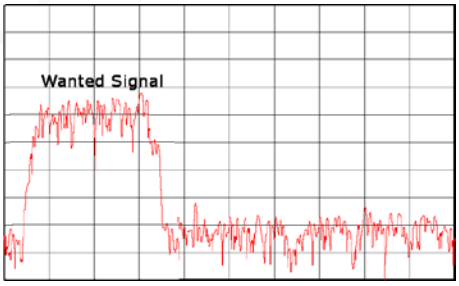
3

RX DC and TX LO Leakage Issue

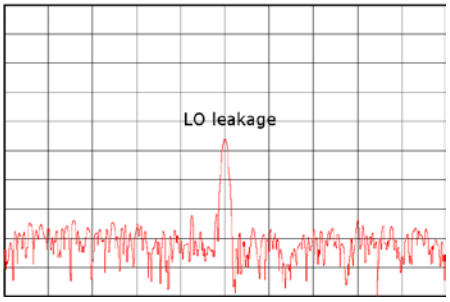
3.1 Problem Description



(a)



(b)



(c)

Figure 4,1: RX DC and TX LO leakage issue

Customers performed the following experiment:

- RX DC, TX DC and TX LO leakage calibrated with no RF signal applied at RX input.
- When the RF signal is applied to the RX input, LO leakage appears at the TX output as shown in Figure 3.1.a.
- TX LO leakage is recalibrated with RF signal present at RX input and LO leakage at TX output is cancelled as in Figure 3.1.b.
- When the RF input is switched off LO leakage at TX output appears again as in Figure 3.1.c.

3.2 Problem Explanation

This result is due to IP2. Figure 3.2. shows the spectrum of the RX output when RF input is driven by a continuous wave (CW). Second order harmonic distortion generates two components, one at *fsignal+fsignal* and one at *fsignal-fsignal* i.e. two IP2 components appear, one at 2**fsignal* and more importantly another one at DC. The DC IP2 component at the RX output is up-converted by the TX chain and appears as LO leakage at the TX output. The IP2 component at 2**fsignal* is either in-band, modulated and does not appear as a spur or will be filtered by the RXLPF.

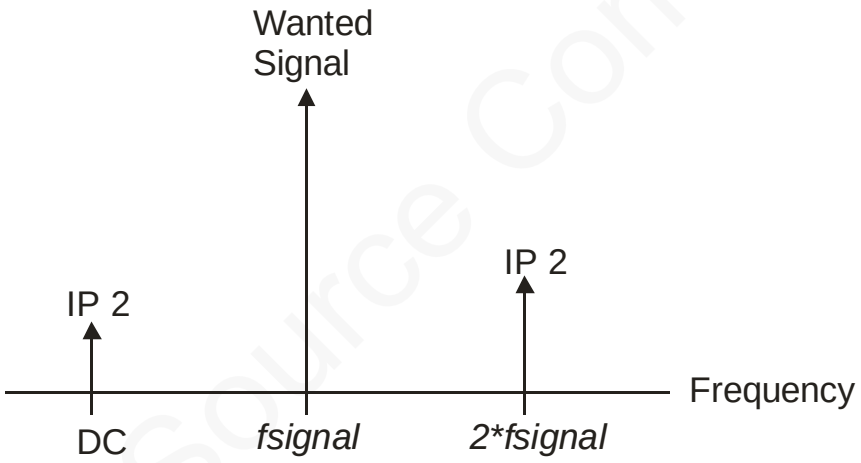


Figure 3.2: IP2 effect

The amplitude of both IP2 components in Figure 3.2. depends on the signal level applied at RX RF input, hence the difference between LO leakages in Figures 3.1.b and 3.1.c. When the LO leakage is cancelled while the signal is present (Figure 3.1.b) and switching the input signal off (Figure 3.1.c) the DC IP2 component at the RX output changes hence the LO leakage calibration parameters are no longer valid and the LO leakage reappears.

Note that apart from IP2, DC at the RX output has two additional sources: RX LO leakage and DC offset of the IF blocks (RXVGA1, RXLPF, RXVGA2) however these are compensated by on-chip DC cancellation loops.

3.3 IP2 Compensation in the RX Chain

Since the DC IP2 component changes with the RX input level, a compensation loop running real time is needed to track and correct the DC at the RX output. A simple digital implementation of such loop is given in Figure 3.3. This circuit should be implemented in the BB/FPGA.

Iin and Qin are in fact the RX ADCs outputs i.e. RX digital outputs. Outputs from the corrector circuit (Iout, Qout) are provided for further processing. The averaging filter calculates the DC of the receiver output and that DC is subtracted to cancel it. The loop is running all the time so any change of the RX DC due to the signal level change, RX gain change or temperature will be tracked and cancelled automatically hence RX DC calibration is required only once at power up. The averaging filter enables the repeater to run in Zero IF mode as well.

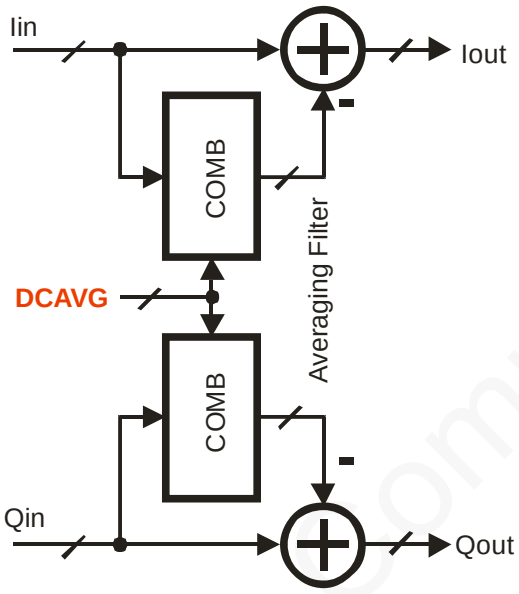


Figure 3.3: Digital implementation of IP2 compensation circuit

Implementation of averaging filter is given in Appendix 1.

3.4 Improving TX LO Leakage Cancellation

LMS6002D has on-chip DACs for TX LO leakage calibration. Those DACs have been designed to provide around -50/-60dBc LO leakage cancellation. If finer LO leakage cancellation is required there are two options that can be applied.

3.4.1 Option A

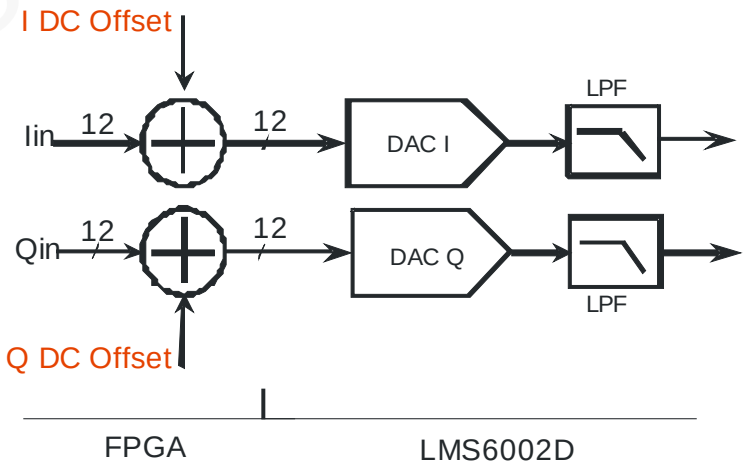


Figure 3.4: Improving TX LO leakage calibration using on-chip data DACs

This option uses the 12-bit IQ data DACs as shown in Figure 3.4. The data DAC's LSB is programmable via the full scale current and load resistance and can be made smaller than the LSB of the dedicated on-chip LO leakage cancellation DACs, hence enabling one to improve the LO leakage.

Please note that the MUX on the FPGA side and DEMUX on the LMS6002D side are not shown in Figure 3.4 for clarity.

3.4.2 Option B

This option uses two additional external auxiliary DACs as shown in 3.5.

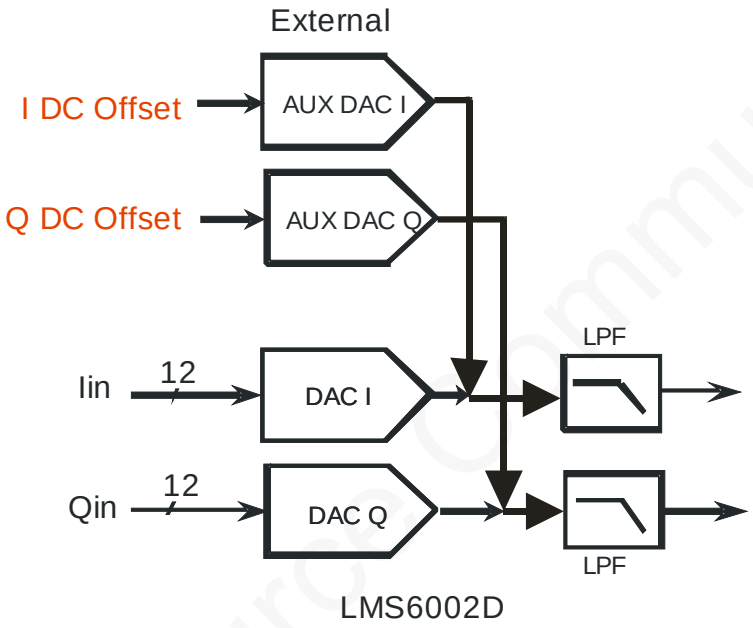


Figure 3.5: Improving TX LO leakage calibration using external auxiliary DACs

Option A relies on the fact that improvement in the LO leakage is more than the loss of gain of the data converters. For example, if we reduce the full scale current by 6dB, the DAC's gain is also reduced by 6dB. If we improve the LO leakage by 12dB then the total improvement is 12-6=6dB. Option B is more robust in this respect. The auxiliary DAC's LSB can be reduced to get better LO leakage but the data DAC's gain is not affected.

Option A requires a simple digital circuit in BB/FPGA, while option B requires two additional external DACs. Option B is still valuable as the specifications of the auxiliary DACs are very relaxed. Neither high speed nor high linearity auxiliary DACs are needed; monotonicity is the only requirement. Also, auxiliary DACs with serial digital interfaces can be used, which simplifies the PCB design.

4

Improved Transceiver Architecture

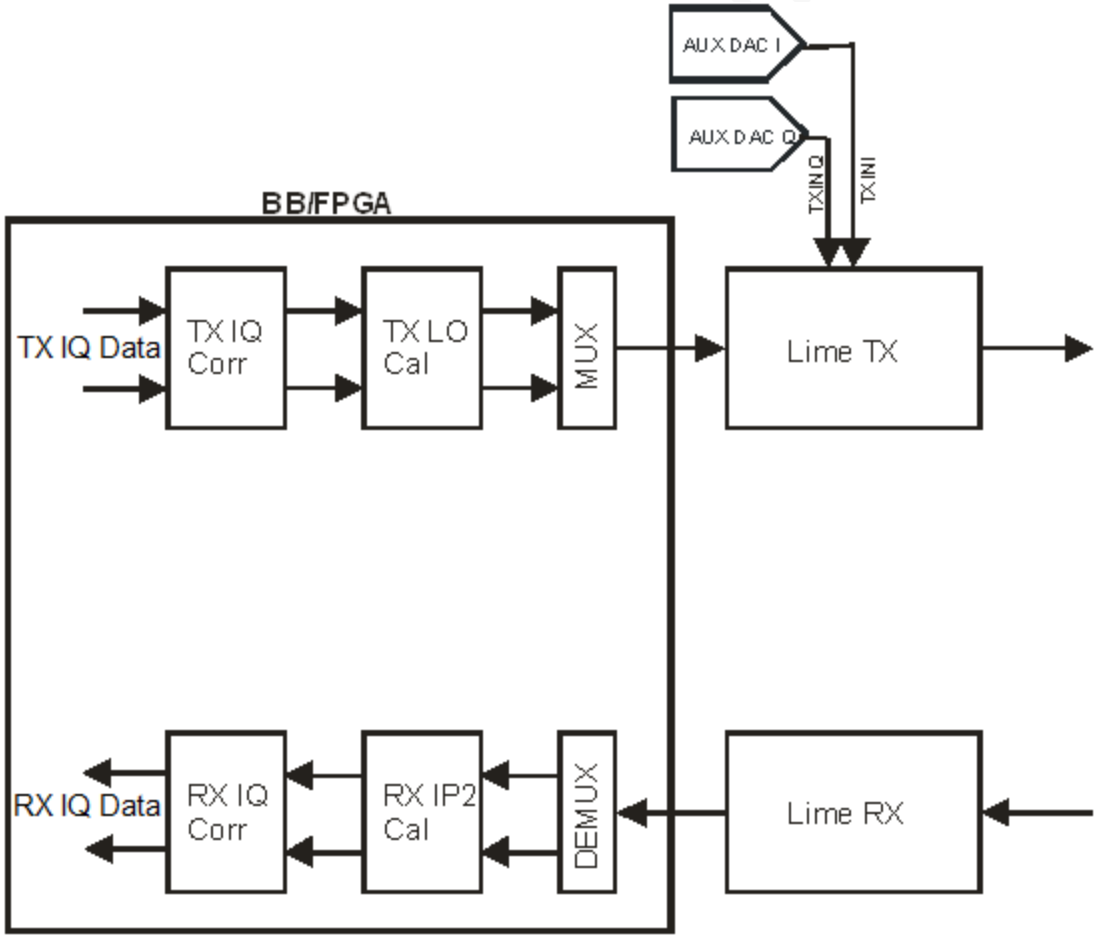


Figure 4.1: Implementation architecture

Figure 4.1 shows architecture which implements all of the improvements proposed in previous chapters. The “RX IP2 Cal” block implements the circuit of Figure 3.3. The “RX IQ Corr” corrects the RX IQ phase error. The circuit is implemented as explained in Appendix 2. Similarly, the “TX IQ Corr” corrects the TX IQ phase error. The block is implemented in the same way as the “RX IQ Corr”. The “TX LO Cal” block implements the circuit of Figure 3.4 while auxiliary DACs implement option B of Figure 3.5. Whether “TX LO Cal”, auxiliary DACs or none of these is needed is based on the customers’ measurements or requirements. If the TX LO leakage is at the acceptable level without these enhancement options, they may be removed from the design.

Key features are as follows:

- “RX IP2 Cal”: tracks and corrects any changes in DC at the receiver output.
- “RX IQ Corr”: improves the SNR of the received signal enabling the ICS algorithm to function better.
- “TX IQ Corr”: improves the SNR at the transmitter output, improving EVM.
- TX LO leakage can be fine-tuned enabling undesired LO leakage to be pushed to the measurement noise floor.

Appendix 1

Averaging (COMB) Filter Implementation

$$H(z) = \frac{1}{L} \cdot \frac{1 - z^{-L}}{1 - z^{-1}}$$

$$y(n) = \frac{1}{L}[x(n) - x(n-L) + y(n-1)]$$

L programmable, 2<= L <= 4096

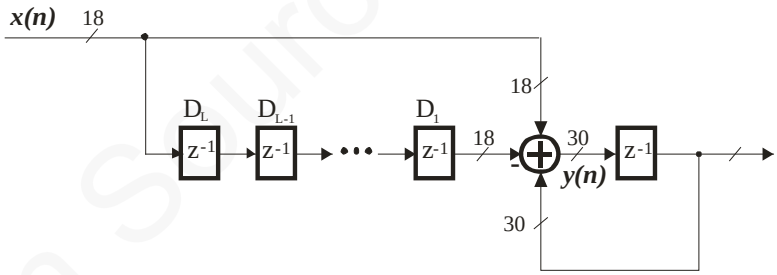


Figure A1.1: Averaging filter implementation using registers

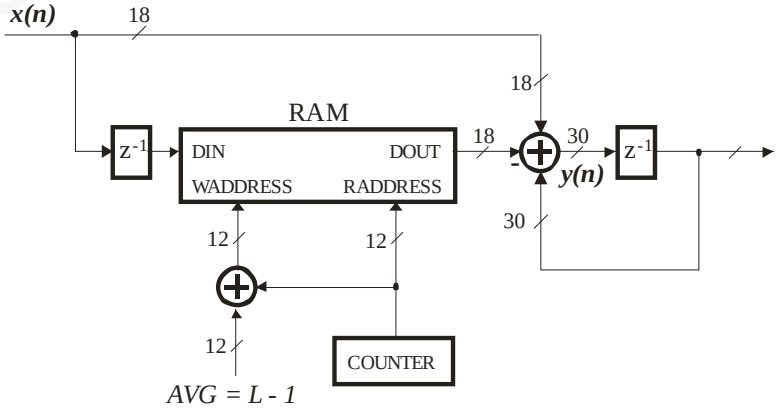


Figure A1.2: Averaging filter implementation using dual port RAM

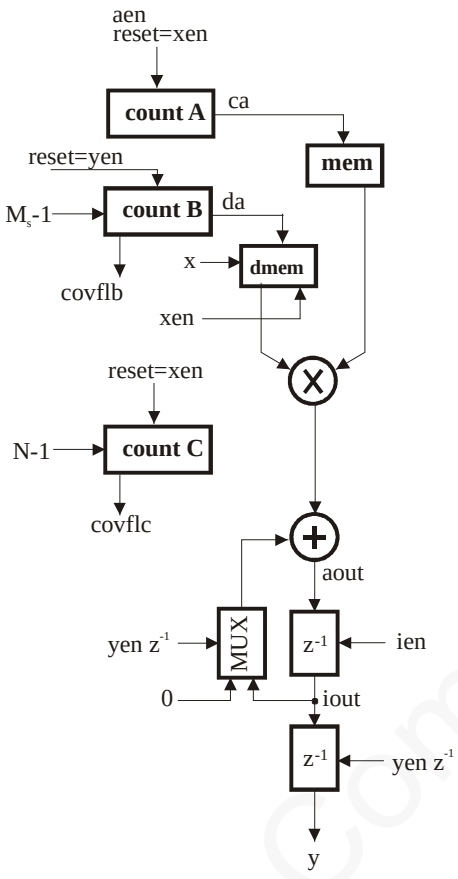


Figure A1.3: Averaging filter implemented as multiply-and-accumulate (MAC) architecture

Appendix 2

IQ Phase Error Correction

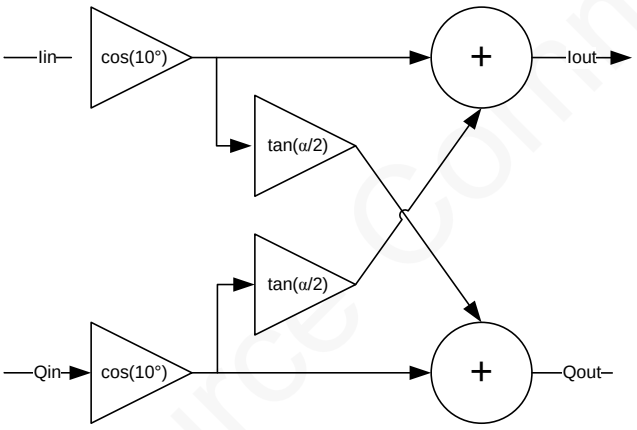


Figure A2.1:

Digital implementation of IQ phase correction is shown in Figure A2.1. It consists of 4 multipliers and 2 adders. Here, α is IQ phase error we want to correct. Inputs Iin and Qin are first scaled with fixed factor ($\cos(10^o)$ in the example shown above) in order to keep the gain of the Fcorrector at <= 1 i.e. to prevent arithmetic overflow.