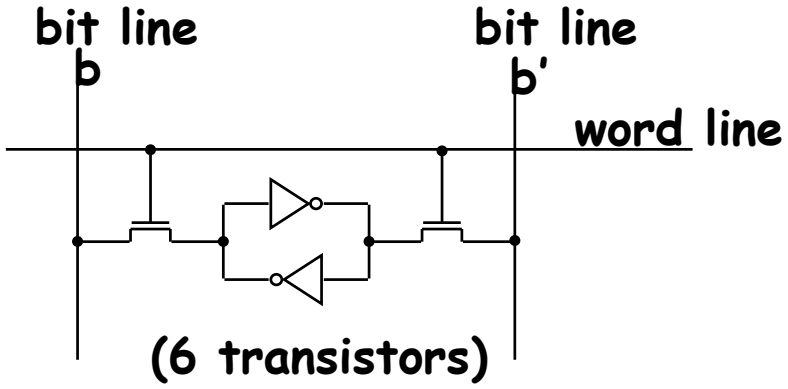
L4: Phase Change Memory

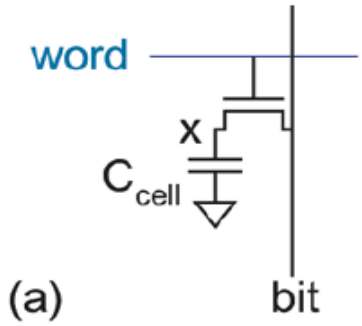
Term Paper and Team Project

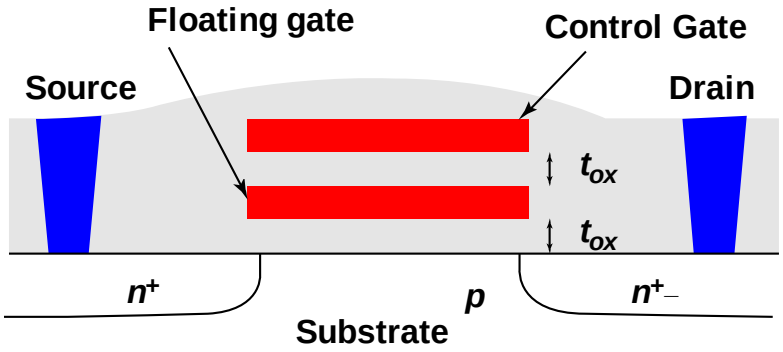
- Finalize your topic by **1159 pm, Feb 5th**
  - You will lose 5% of your grade daily for each day after the deadline
- Link: https://goo.gl/BkgftK
- Written report (4-page IEEE-style paper) due on **Feb 26th**
- Team project: 6 people per team (29 enrolled)
- Finalize your team and topic by **Mar 4th**
  - You can still submit a partial list of your team to me, where I will try my best to pair up
  - If we have to break up one or more partial team(s), the priority will be given first to partial teams with the most team members; and then to teams that contacted me earliest
- Presentation and report due on **Apr 15th**

Recap

- SRAM
- DRAM
- Flash







Outline

- Optical Data Storage
  - CDs, DVDs, blu-rays
- Phase Change Material
  - History
  - Phase change
- Phase Change Memory Device
  - Device structure
  - Threshold switching
- Scaling of PCM
  - Crystallization and melting temperature
  - Programming current
- Reliability
  - Endurance
  - Variability

Optical Data Storage

- Cave painting

- Drawing

- Photography

Compact Disk Read Only Memory (CDROM)

- Invented by James Russell in 1970
- Mass production since 1985 by Philips and Sony

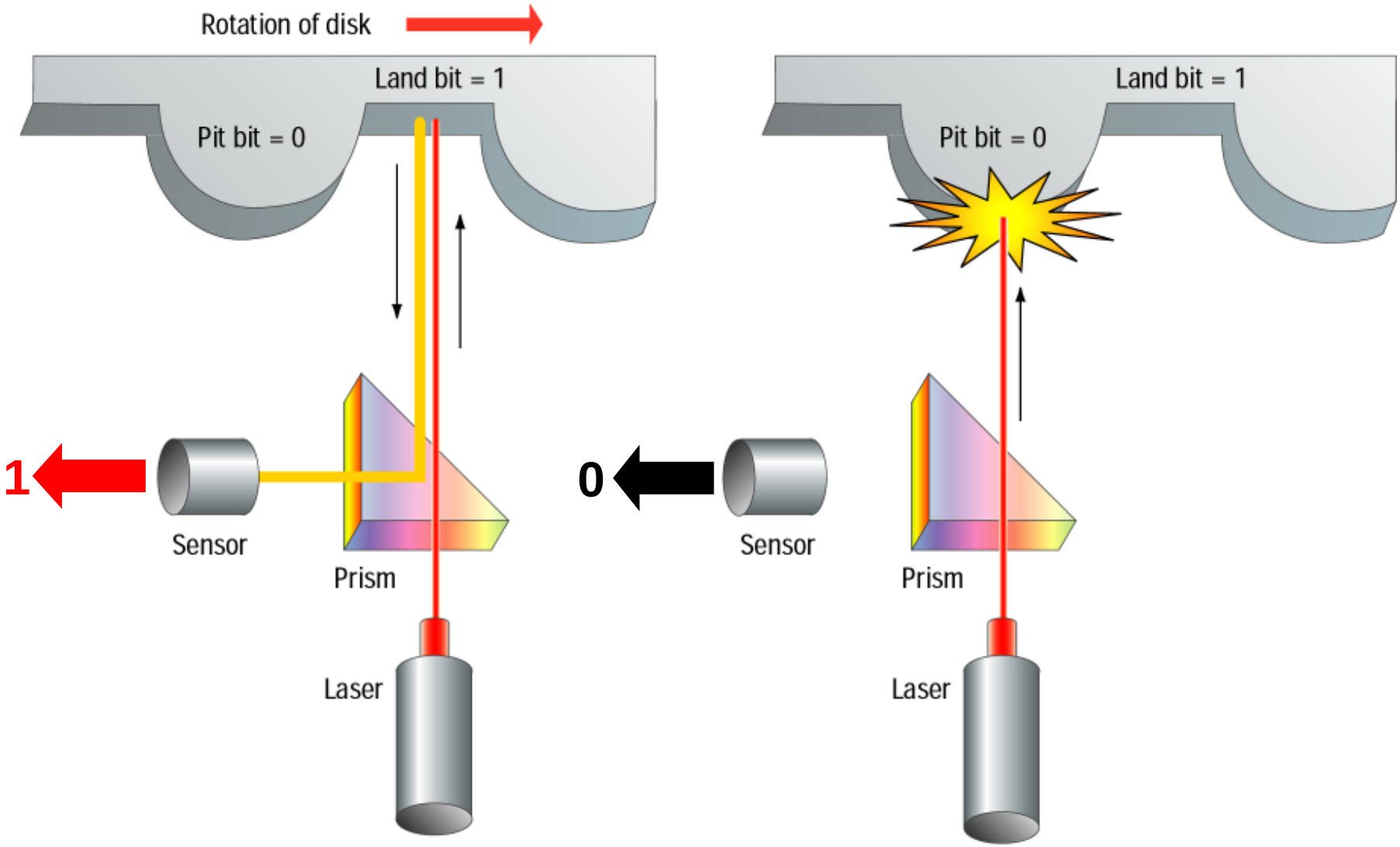
- Basis
  - Optical recording technology developed for audio CDs
    - 74 minutes playing time

- Bit Rate
  - 150 KB / second

- Capacity
  - 74 Minutes * 150 KB / second * 60 seconds / minute = 650 MB

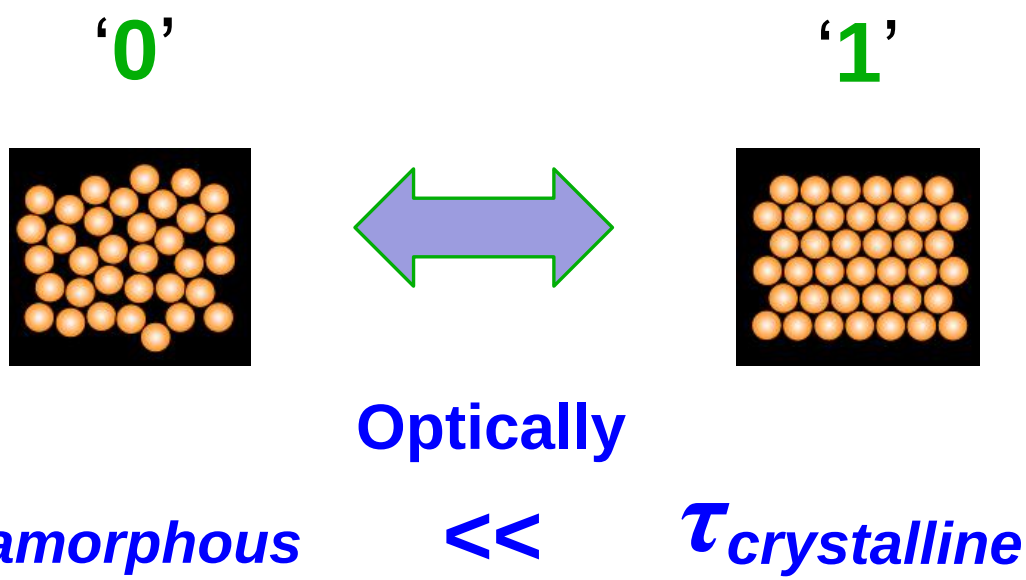
- Read only, cannot be overwritten

CDROM Working Principle



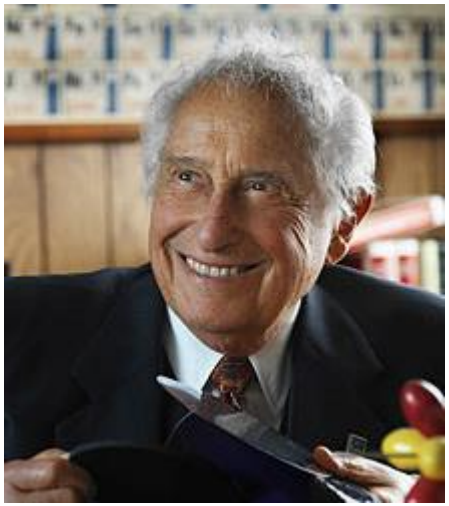
CD-Rewritable (CD-RW)

- Allows writing new data over recorded data
- Endurance: 100-1000 times
- Based on phase change materials (PCMs)



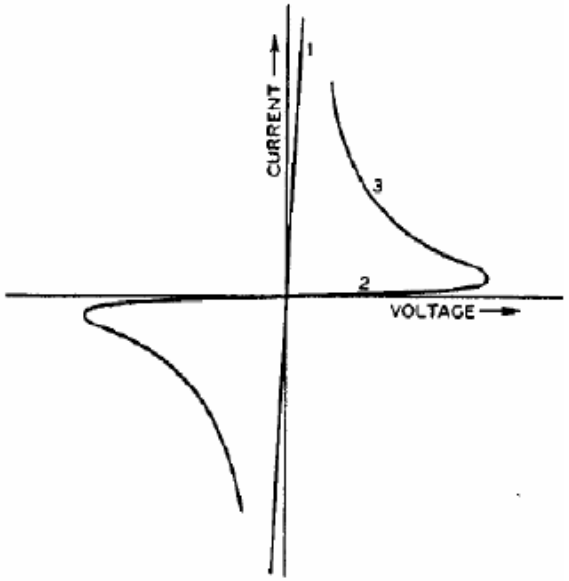
History of Phase Change Material

- Discovered by Stanford Ovshinsky in 1969



- Stanford Ovshinsky (inventor and scientist)
  - >400 patents
  - Nickel-metal hydride battery
  - Phase change memory

- First reversible switching material
  - 48% Te, 30% As, 12% Si, 10% Ge
  - Continuous switching over a period of months
  - However, switching is slow ~10 μs

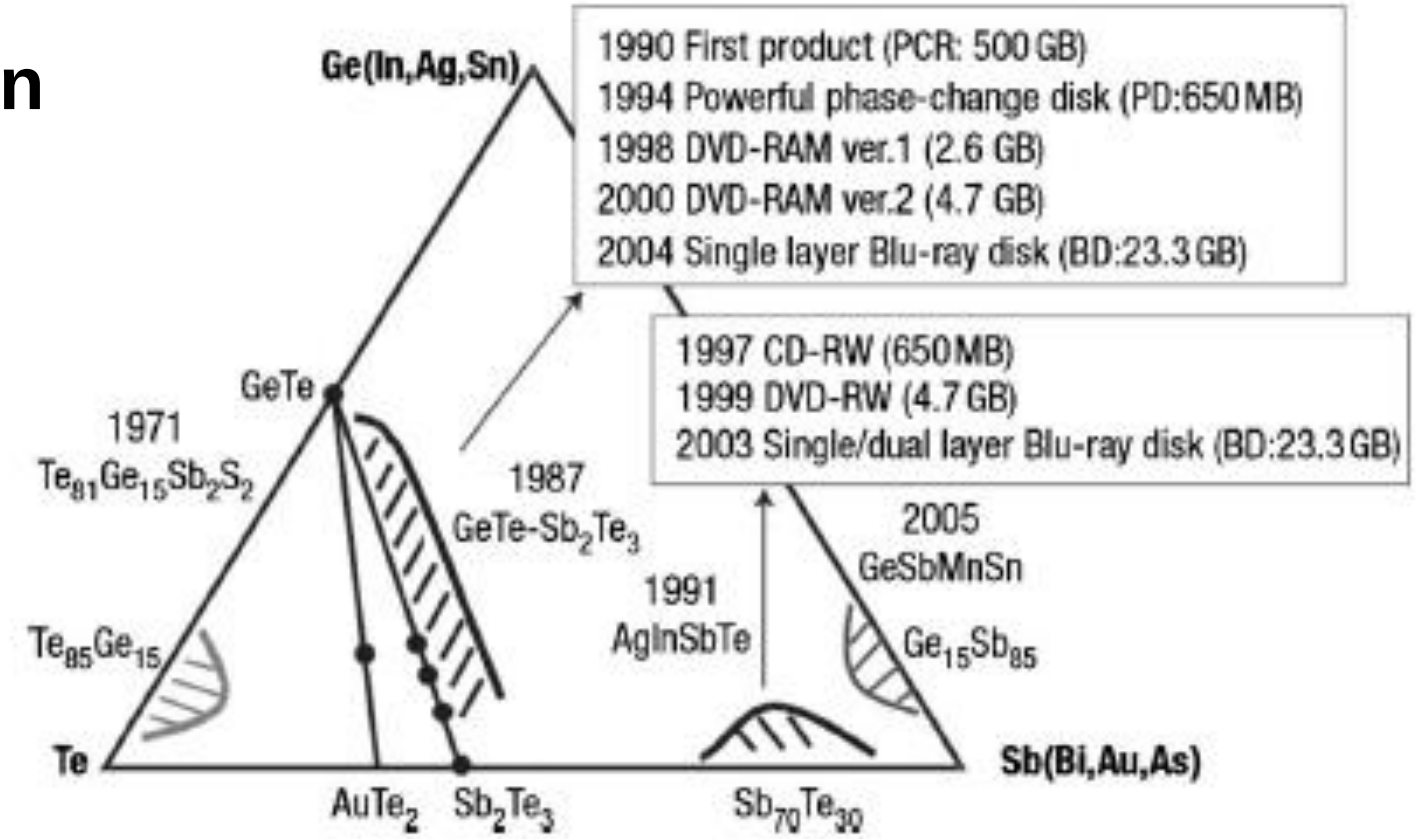


Rebirth of Phase Change Material

Crystallization Rate

@ 25 ºC, ~10 years (3×10^9 s)

@ 150 ºC, ~10 ns (10^{-8} s)

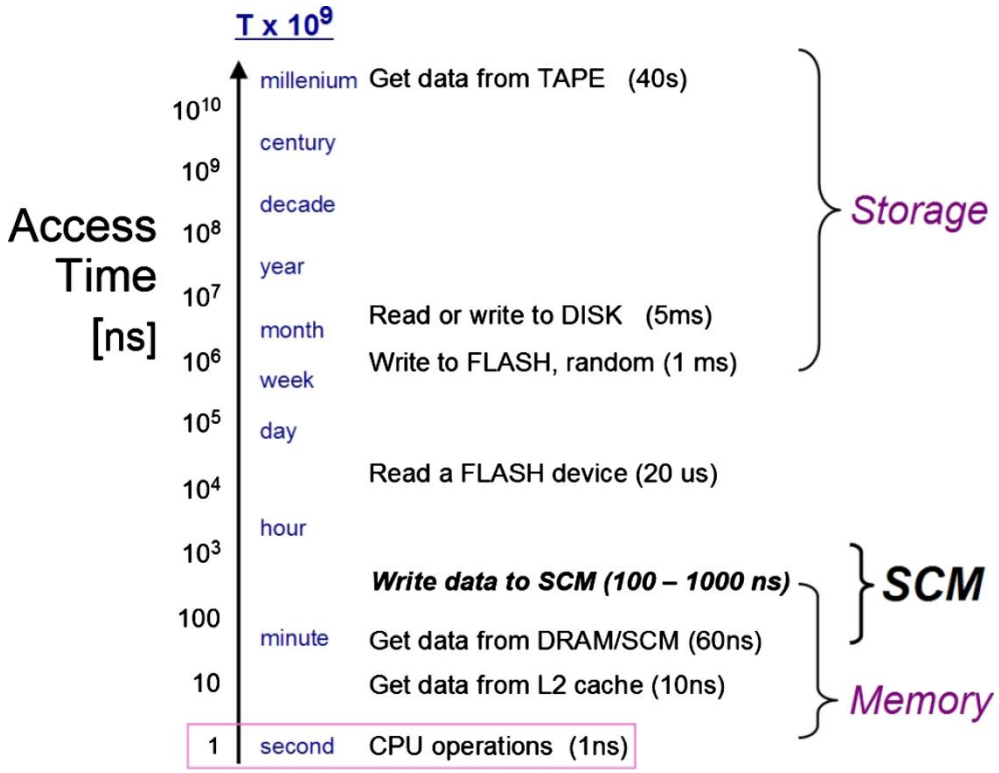


Best known: $Ge_2Sb_2Te_5$ (GST)

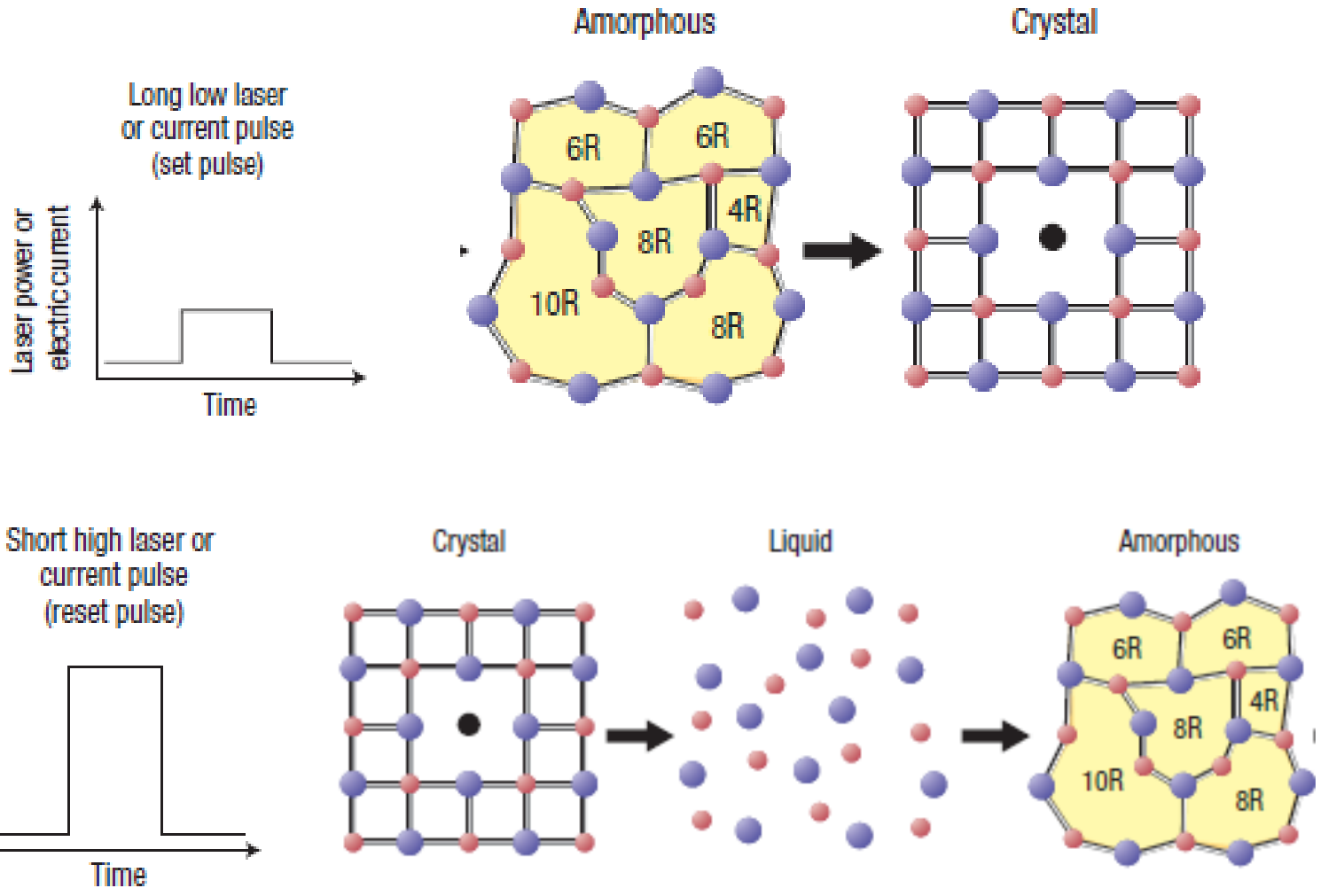
fast crystallization, good stability and large contrast

Phase Change Memory

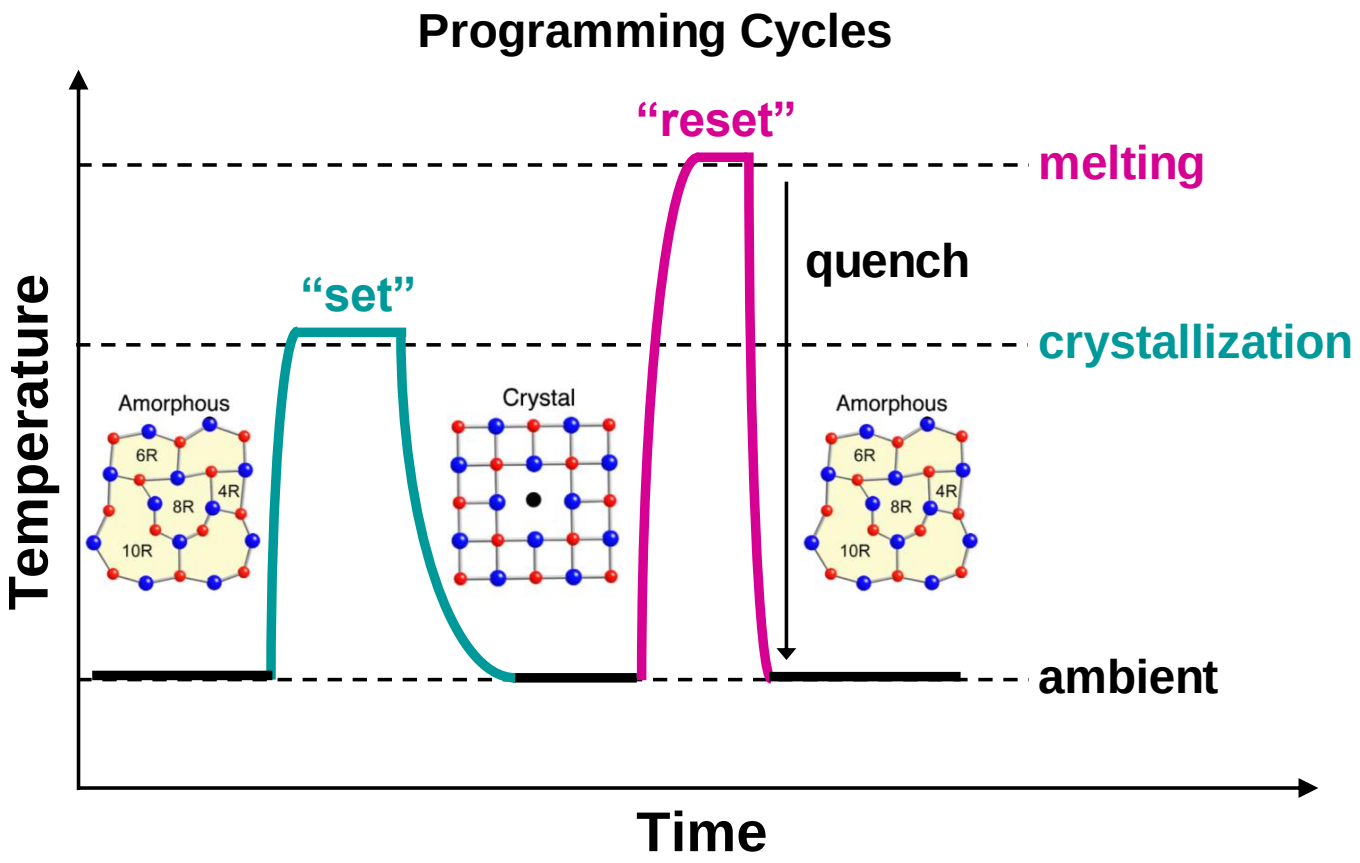
- Non-volatile
- Fast access time ~50 ns
- Large dynamic range
- High endurance
- High packing density
- Highly scalable
- Radiation resistant



Phase Transformation



Programming

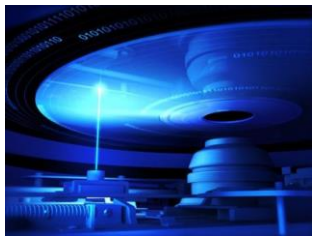


- "set": crystallization → data rate limiting (~10 ns)
- "reset": melt-quench → power limiting (~600 C)

DVD

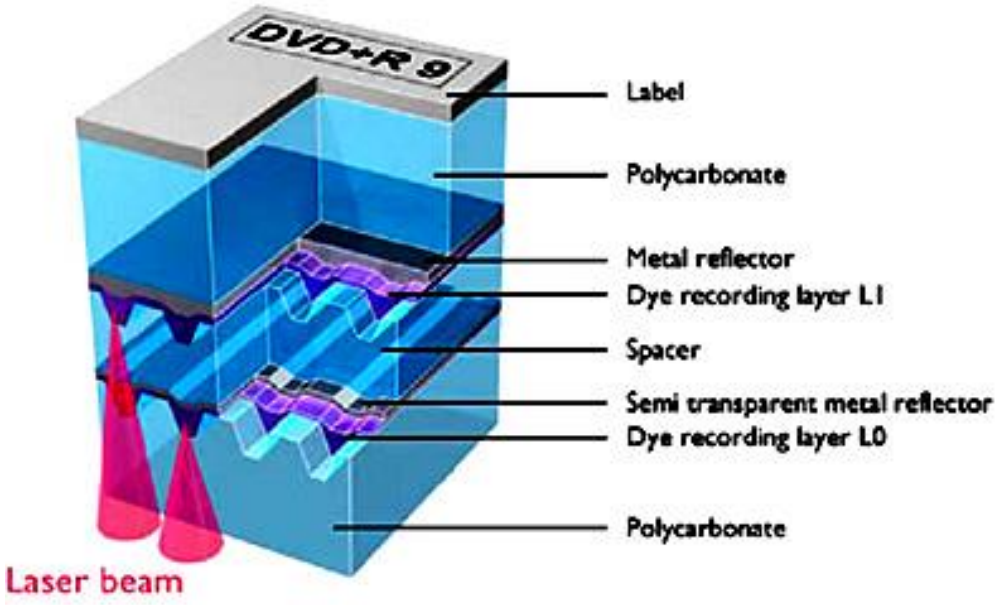
- Improved technology upon CD-RW
- Smaller wavelength → higher density
- Better mechanical control
- Improved error correction

- Larger capacity
  - Standard – Up to 4.7 GB, 7 times more than CD-ROM
  - Double layers – 8.5 GB
  - Double-sided – 17 GB
  - Blu-ray (BD) disk – 25 GB
  - Dual layer BD – 50 GB



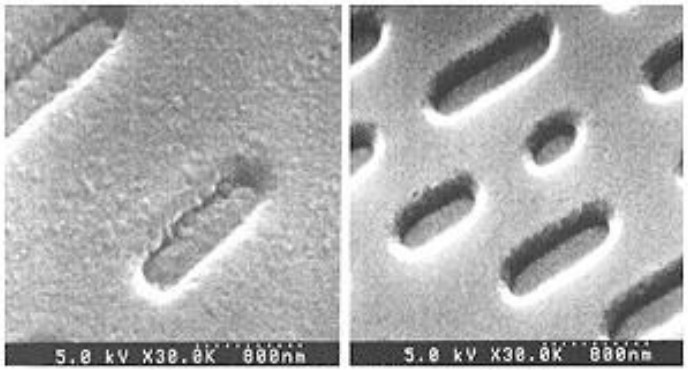
Dual Layer Technology

- Benefits
  - Increased durability
  - Increased capacity
- Detriments
  - Decreased S/N
  - Decreased data density



Numerical Aperture

- NA = n sin(θ/2)
- Spot size = λ/NA
- CD-RW λ ~ 780 nm IR
- DVD λ ~ 650 nm red
- Blu-ray λ ~ 405 nm blue



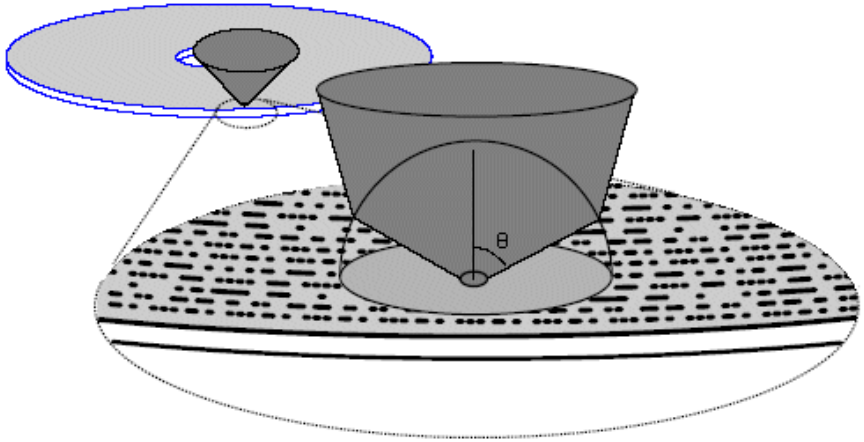
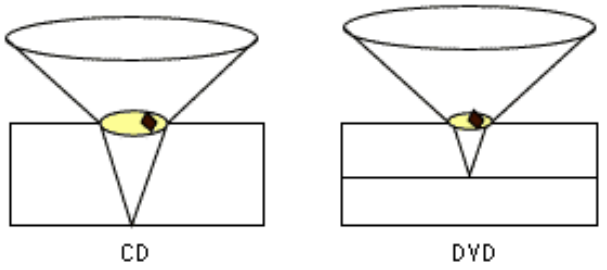
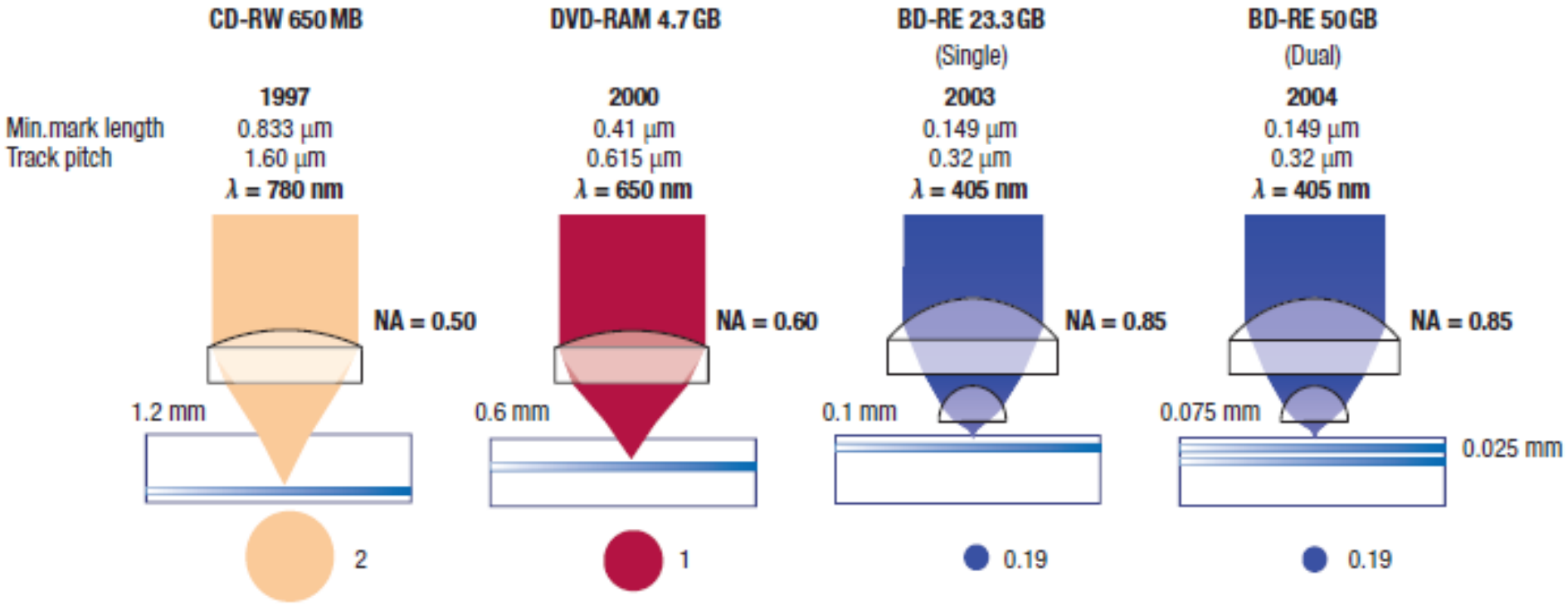


Figure 2: A solid–immersion lens (SIL) can increase the effective NA beyond 1.0, further increasing density but requiring evanescent coupling between the SIL and disk.



Comparison of Optical Storage



Depth of Focus (DoF)

- DoF = λ/NA^2
- Determines spacing of layers
- Decreasing depth of focus → more layer → higher density
- Affects S/N; places an upper limit on NA.

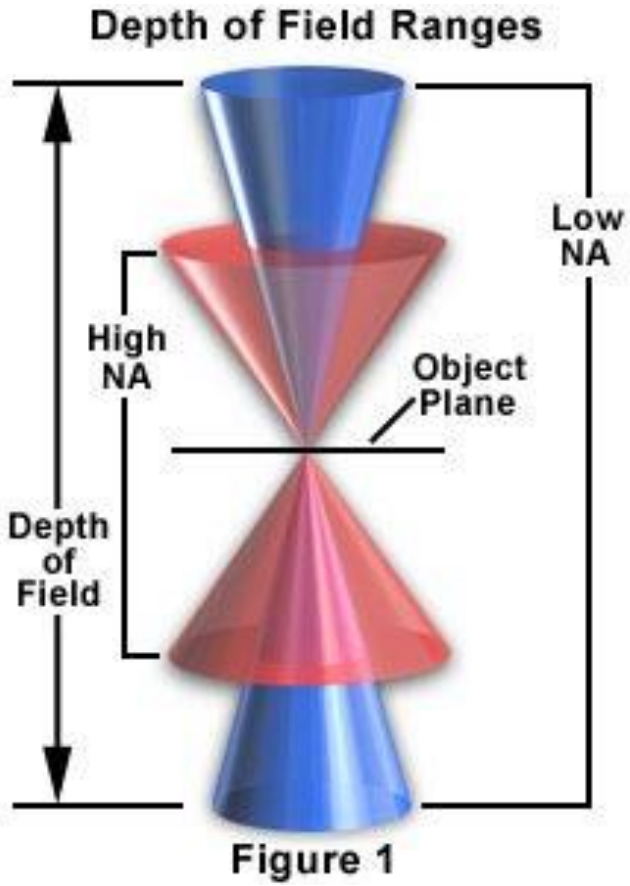
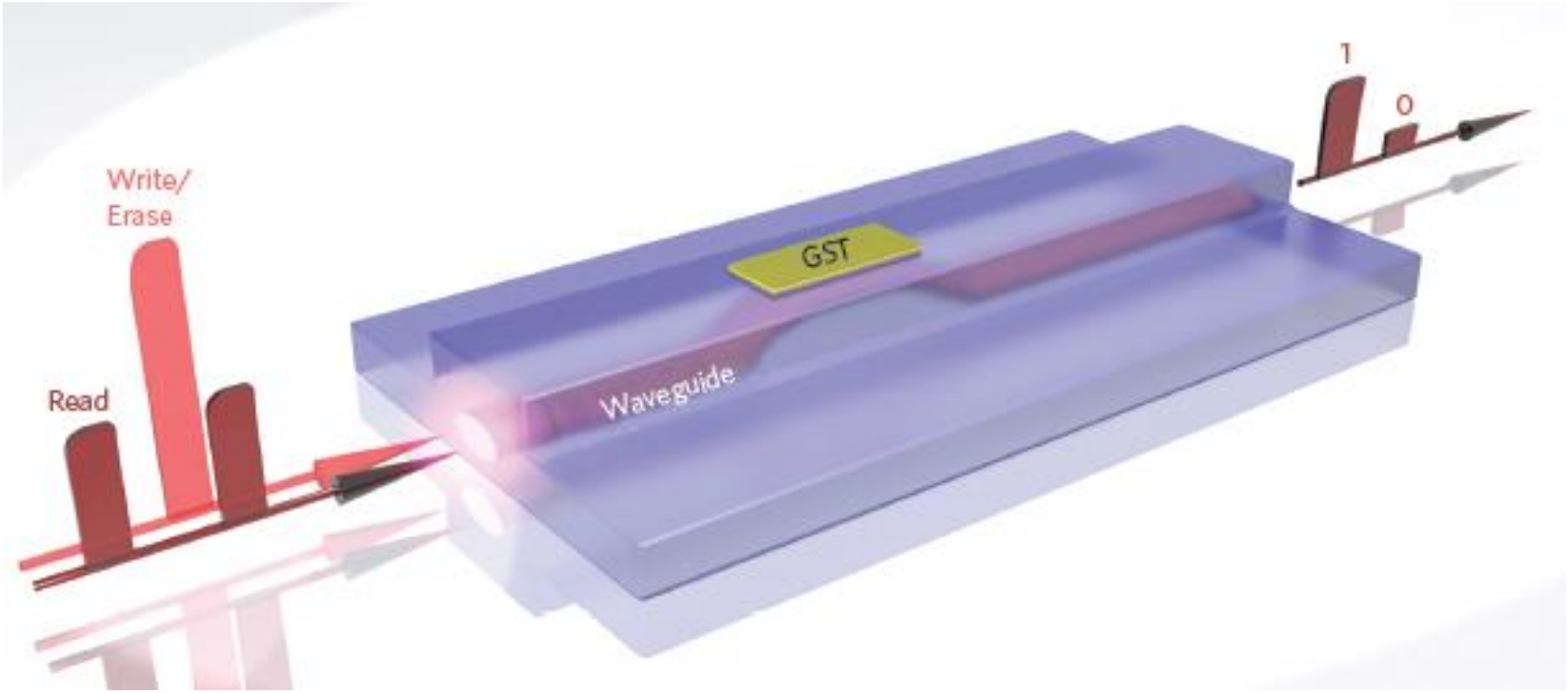


Figure 1

Photonic Memory

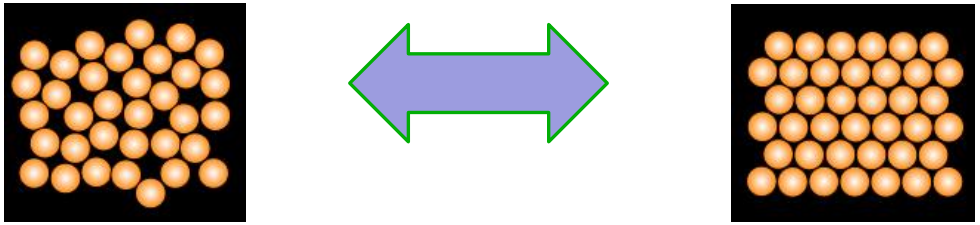


- Change in Absorption in photonic waveguide
- Optical memory and all photonic circuit

Phase Change Material

‘0’ ‘1’

Amorphous **Crystalline**



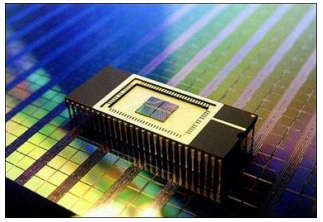
Optically

$\tau_{amorphous} << \tau_{crystalline}$

Optical Drive

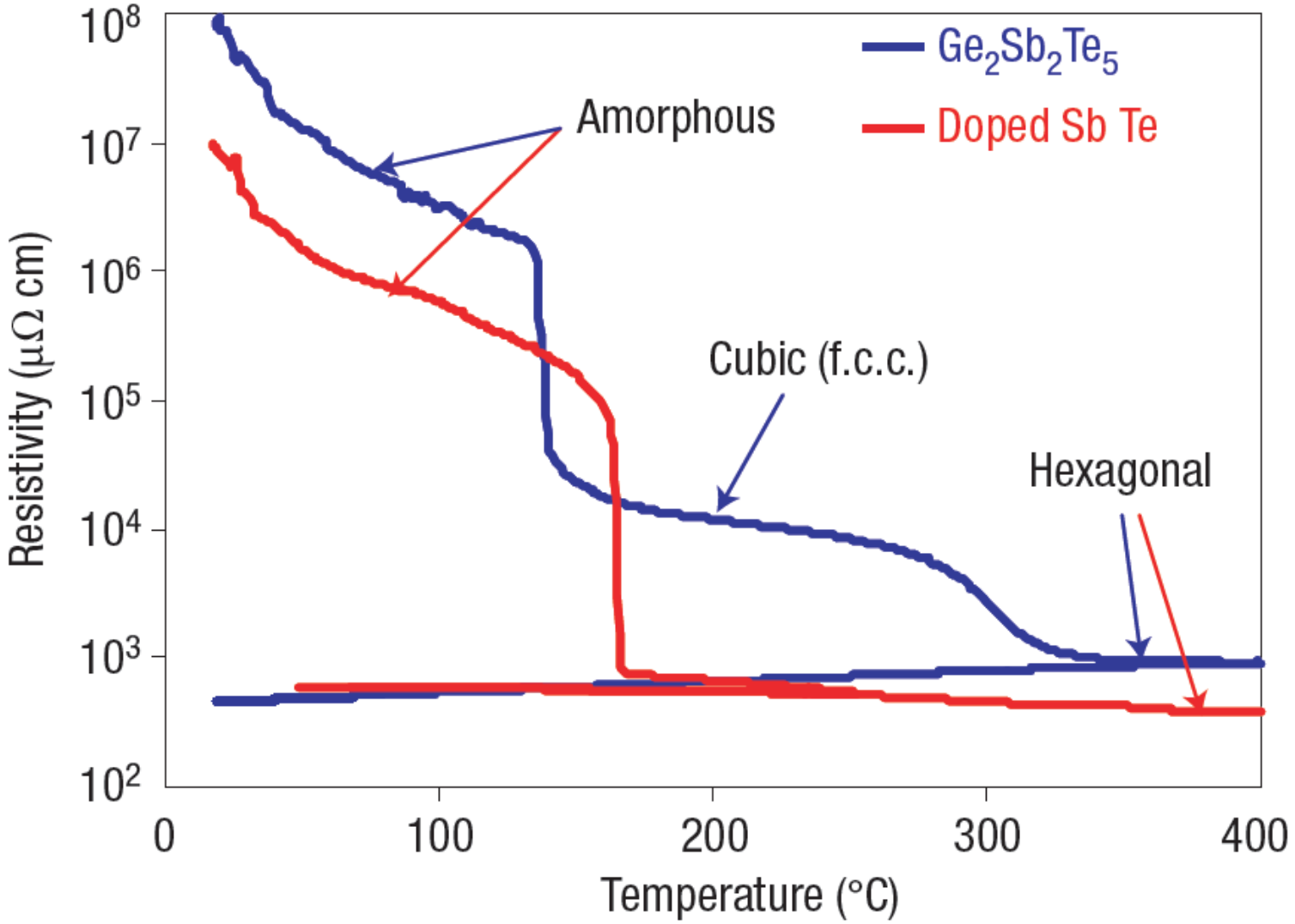
Electrically

$\rho_{amorphous} >> \rho_{crystalline}$



PCRAM

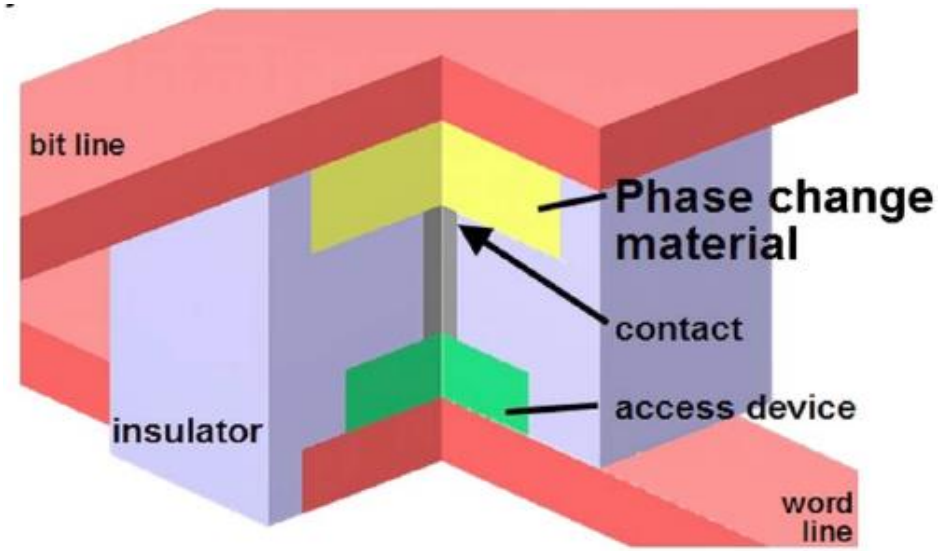
Temperature Dependent Resistivity

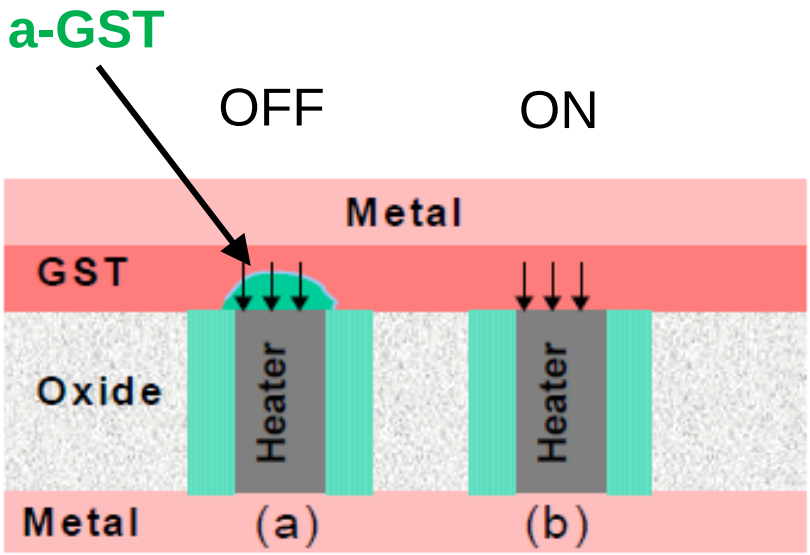


M. Lankhorst *et al*, *Nat. Mater.* (2015)

Phase Change Memory Device

PCM “Mushroom” Cell

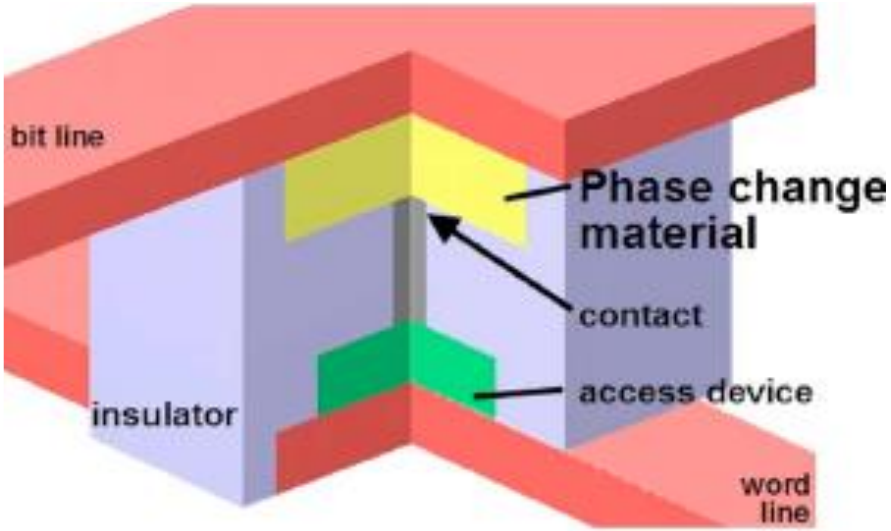




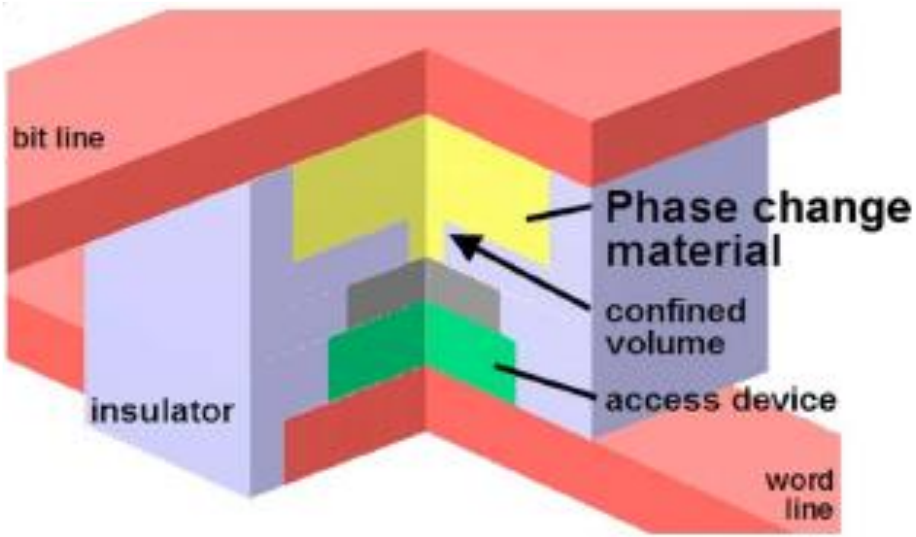
- Mushroom cell with PCM cap
- Electrode/heater
- Threshold switching

PCM Cell Structure

Contact-minimized

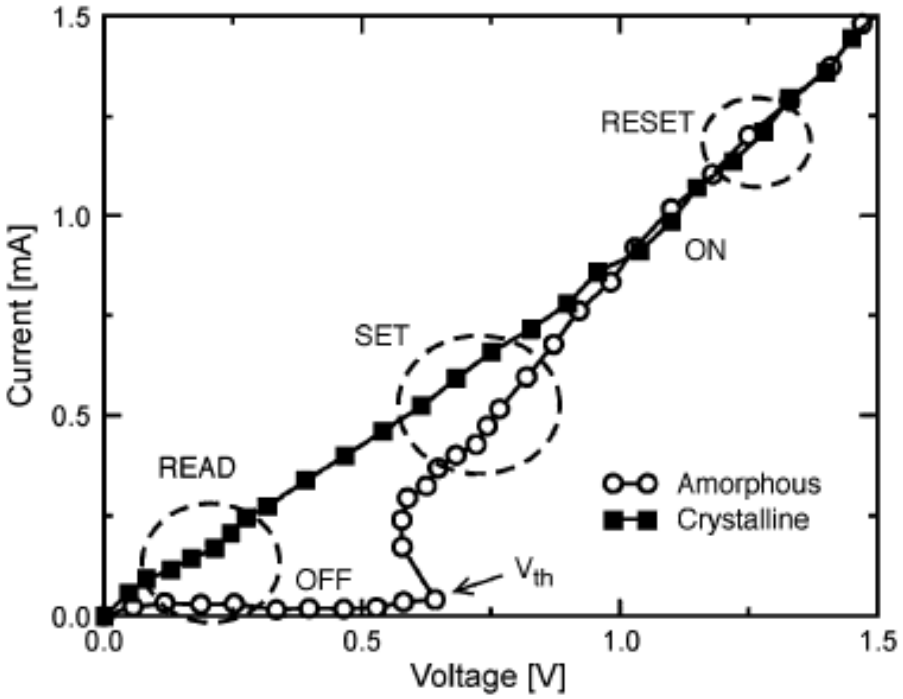


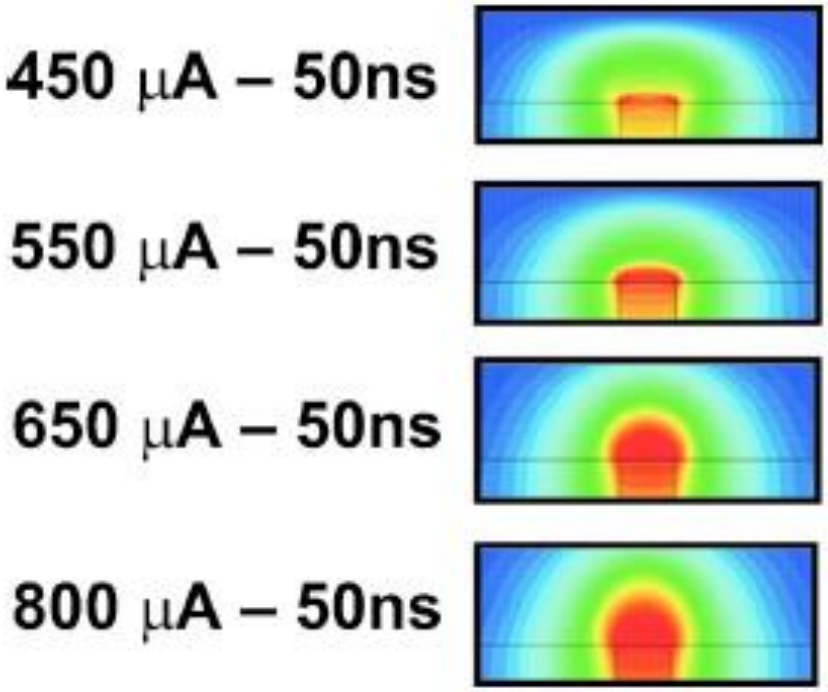
Volume-minimized



- Contact-minimized cell
  - easier to fabricate, most common, halo effect
- volume-minimized cell
  - good scaling behavior, difficult to fabricate

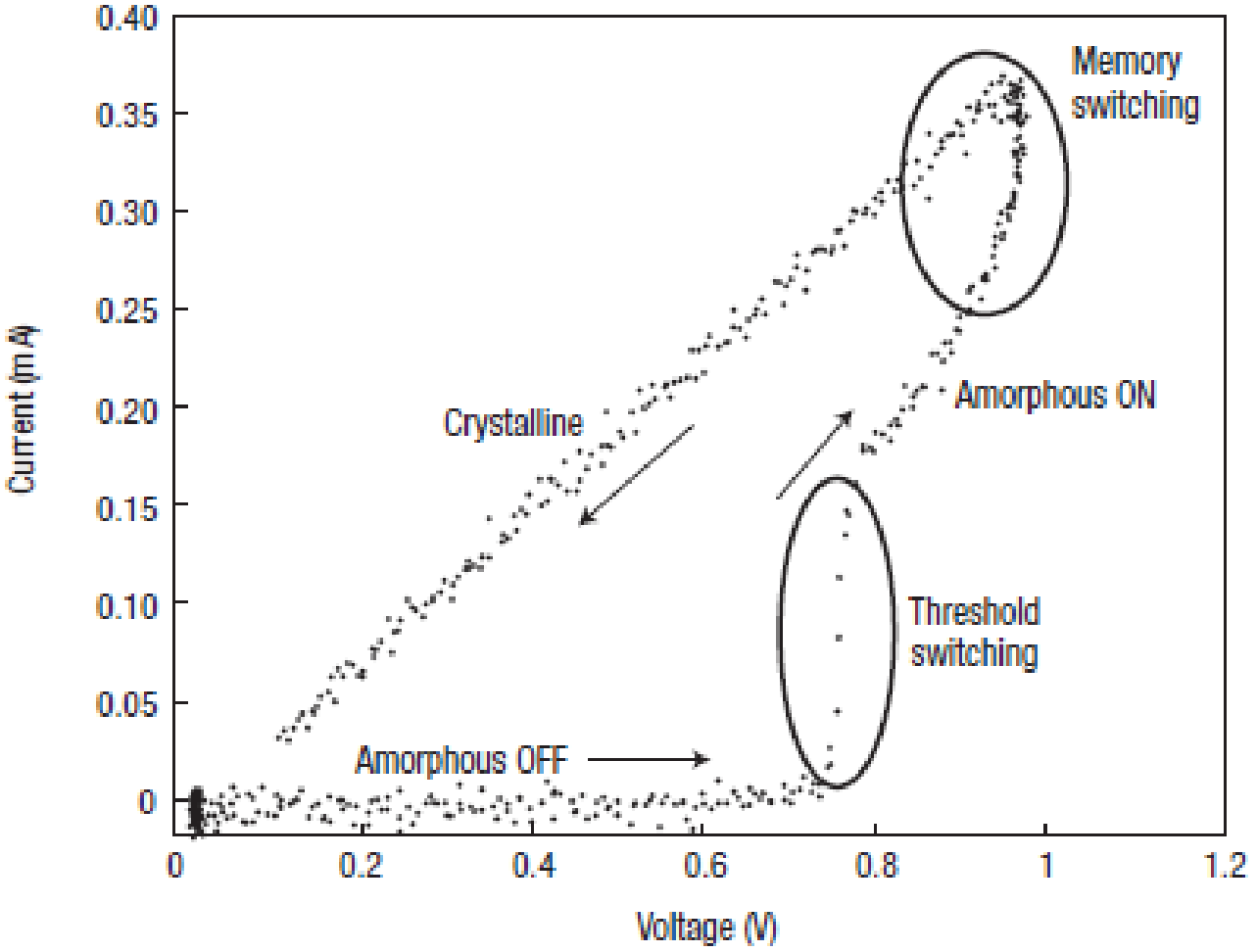
Temperature Profile





- Temperature profile for set and reset
- Crystallization ~ 150 C
- Melting ~ 600 C

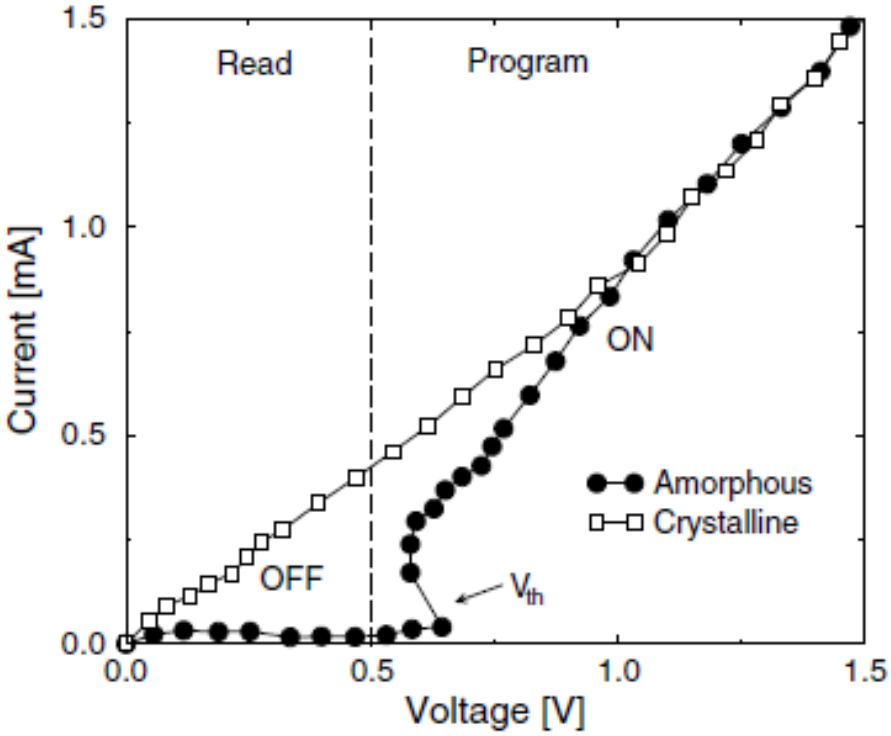
Threshold Switching



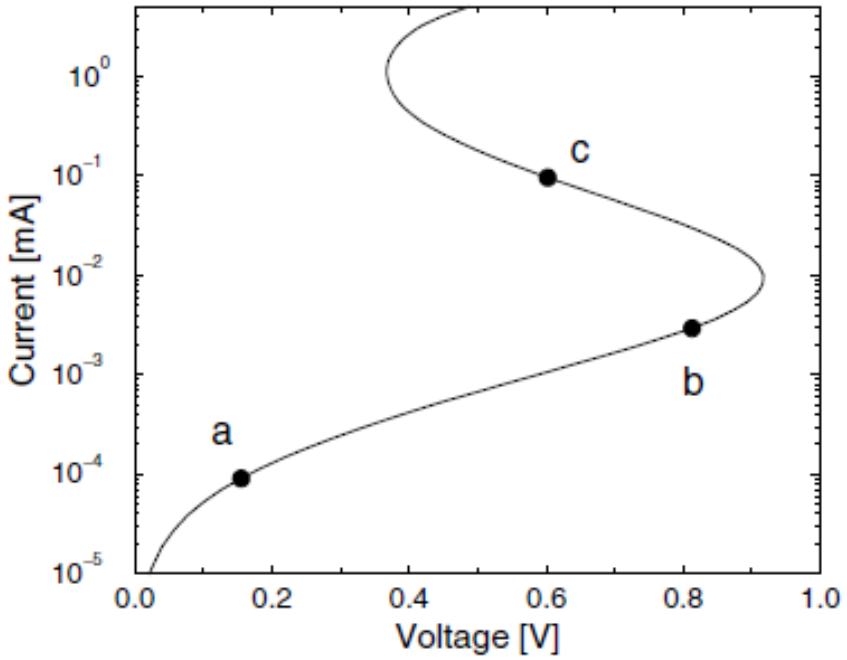
- Threshold switching – E-field dependent
- Threshold switching → I↑ → Joule heating → Crystallization

Threshold Switching

Experimental IV

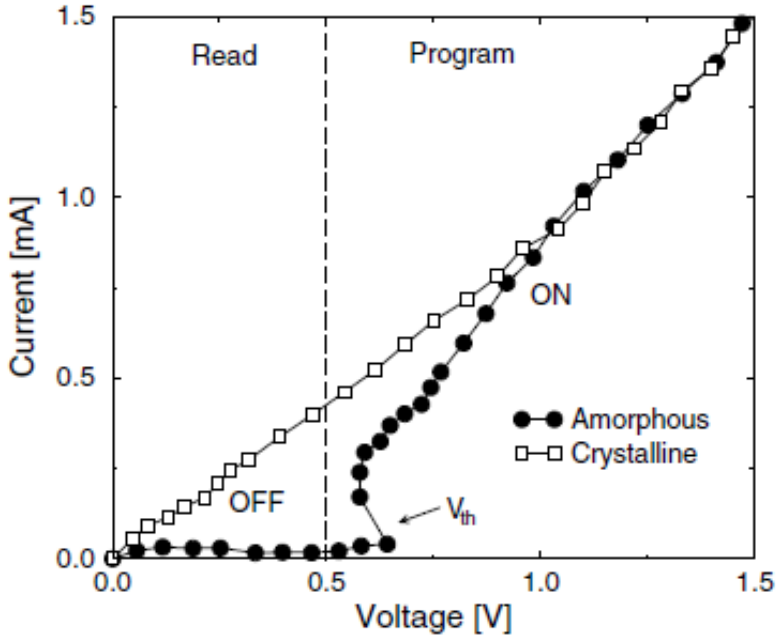


Simulated IV



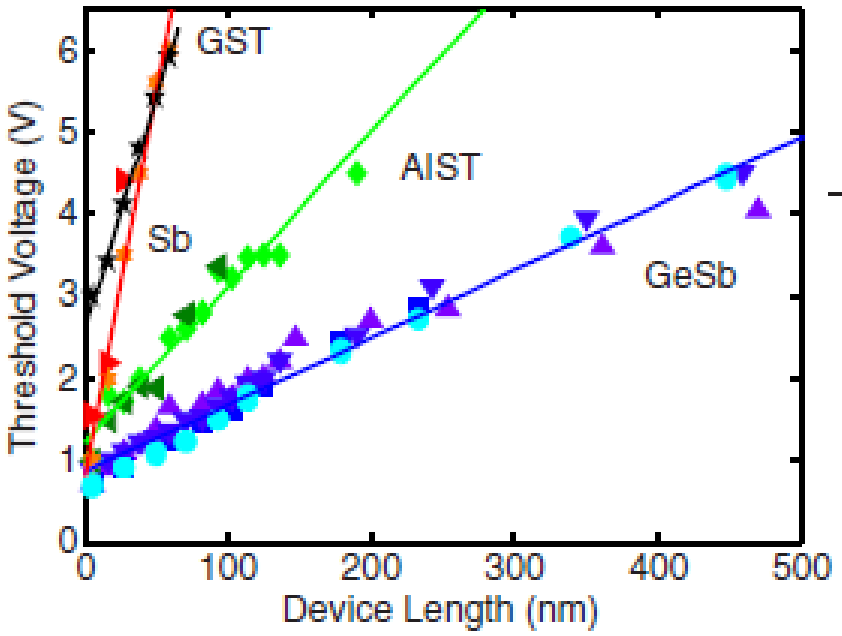
- Amorphous: Poole-Frankel conduction
- Avalanche effect upon critical field→ threshold switching
- Crystalline: drift-diffusion (ohmic + Joule heating)

Threshold Switching



- Threshold switching = resistive to pseudo-conductive
- Joule heating → amorphous to crystalline
- Threshold switching is reversible
- No memory switching if voltage is removed quickly
- Dissolution of premature crystalline embryos upon removal of E-field

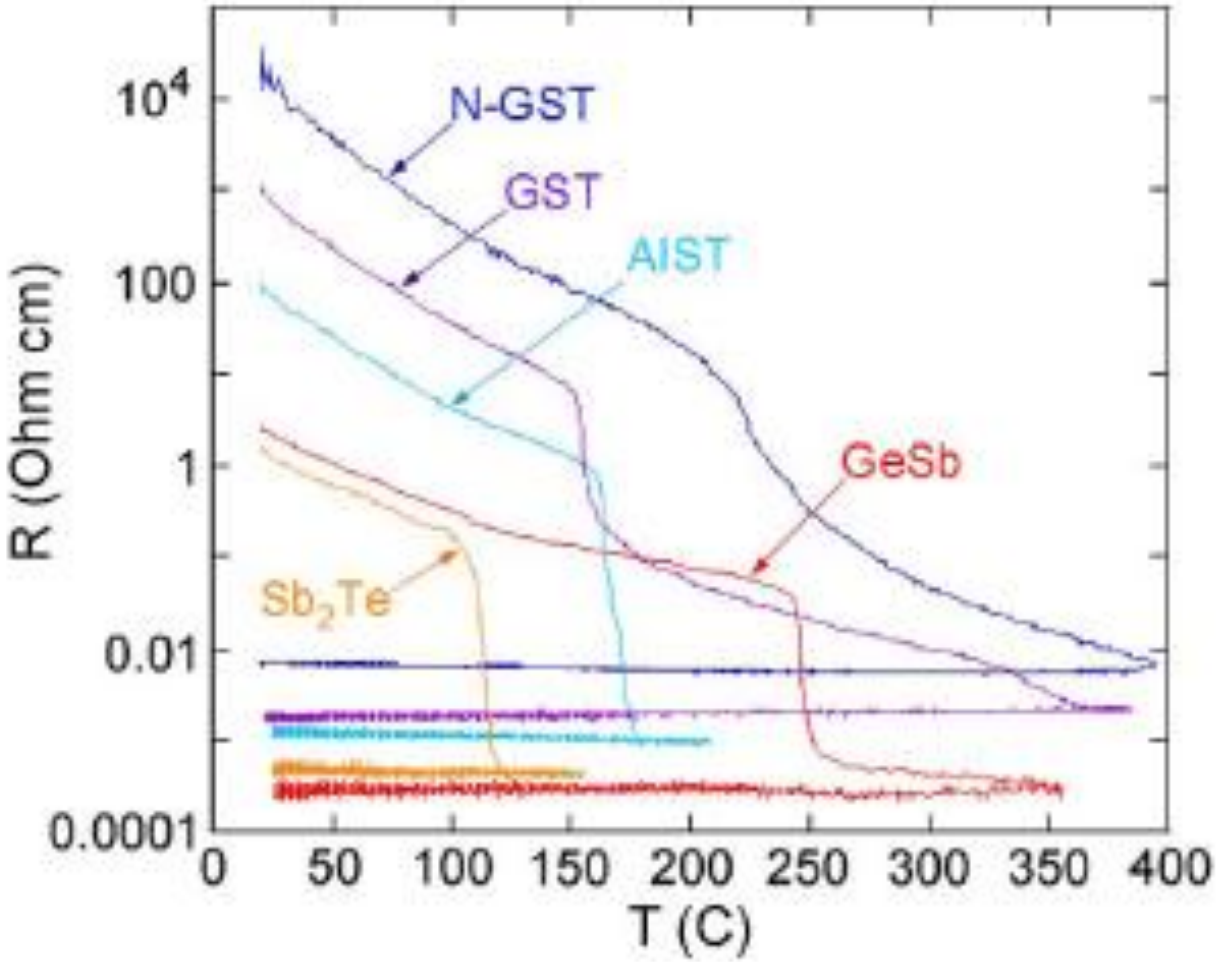
E-Field Dependent



Material	Threshold field (V/μm)
$Ge_{15}Sb_{85}$	8.1 ± 0.2
AIST	19 ± 1
$Ge_2Sb_2Te_5$	56 ± 2
4 nm thick Sb	94 ± 9

- Threshold field: 10 to 100 V/μm
- No significant difference between as-deposited and melt-quenched
- Needs to consider under factor like crystallization T, rate, melting T, endurance etc

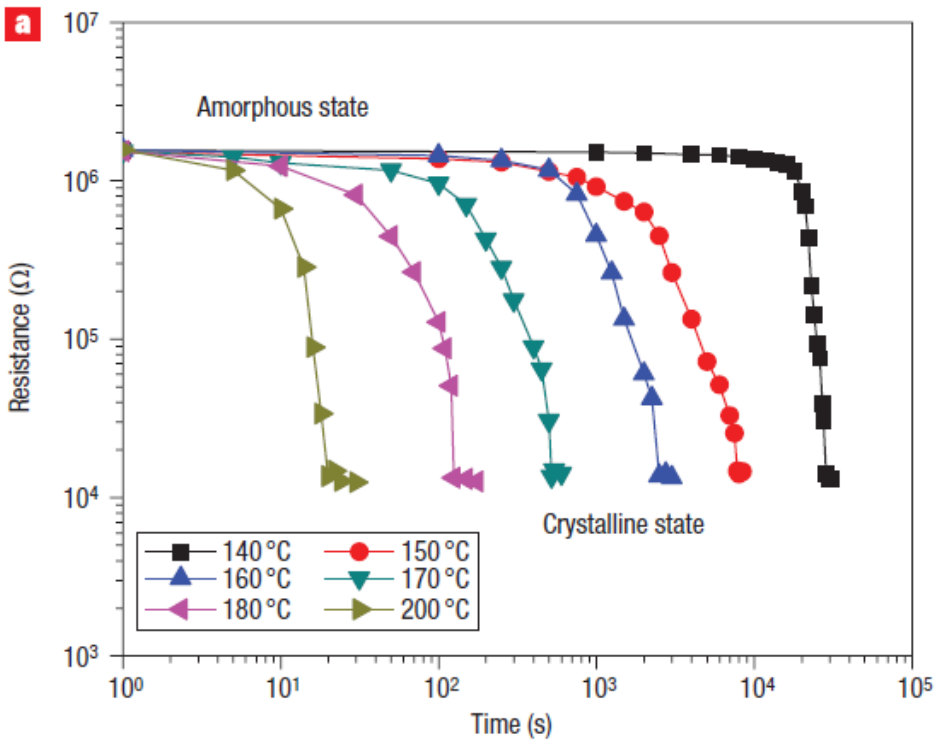
Doping Effect on Crystallization Temperature

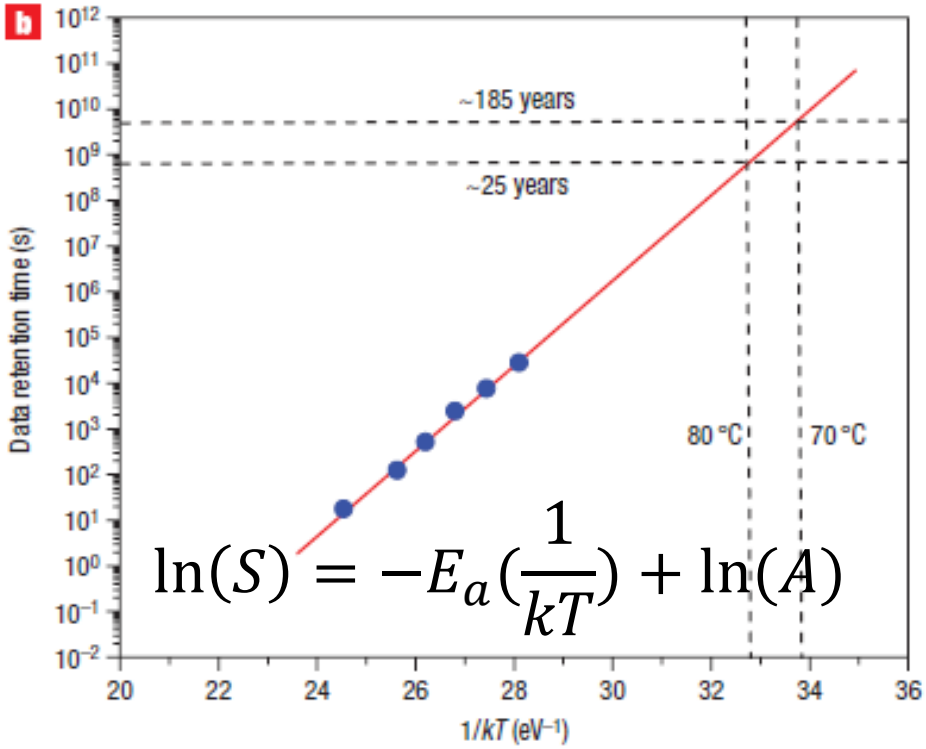


- Doping – co-sputtering or ion-implantation
- Trade-off: energy consumption vs thermal stability

Thermal Stability

$$S = Ae^{-\frac{E_a}{kT}}$$





- Recrystallization occurs naturally – thermodynamically favorable → data retention?
- Arrhenius plot → activation energy and retention time

Scaling of PCM Properties

PCM Parameter	Scaling Behavior	Influence on Performance
Crystallization Temperature	↑	Better Data Rentention
Melting Temperature	↓	Lower RESET Power
Threshold Voltage	↓	Lower Power
Crystallization Speed	↑	Faster Data Rate
Melt-quench Speed	↑	Lower RESET Energy
Thermal Conductivity	↓	Lower Switching Energy
Switching Current	↓	Lower Switching Power
Thermal Cross-Talk	↑	More Failure
Variability	↑	Reliability Issue

Scaling: Crystallization Temperature

- T_{crys} ↑ as film thickness ↓

- Ultimate limit? What is the thinnest film that still showed a phase transition?
- 1.3 nm of GeSb with T_{crys} of 300 C vs. ~235 C for bulk

- GST: T_{crys} starts to increase for films thinner than 20 nm
- No more fcc phase below 3.6 nm
- No crystallization below 2 nm

- T_{crys} ↑ → higher activation energy → better data retention

Scaling: Melting Temperature

- T_{melt} ↑ as film thickness ↓

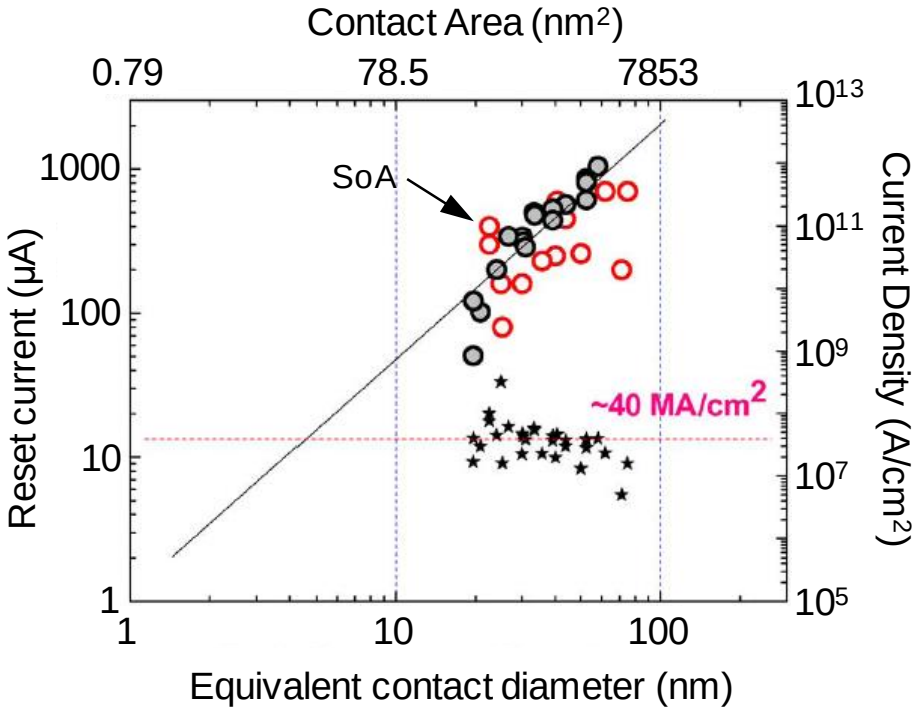
- GeTe nanowire (60 nm) ~390 C vs. 725 C in bulk
- In2Se3 nanowire (40 nm) ~680 C vs 890 C in bulk
- GST nanowire (25 nm) ~450 C vs 650 C in bulk

- T_{melt} ↓ → lower power consumption → reset/melting is power limiting

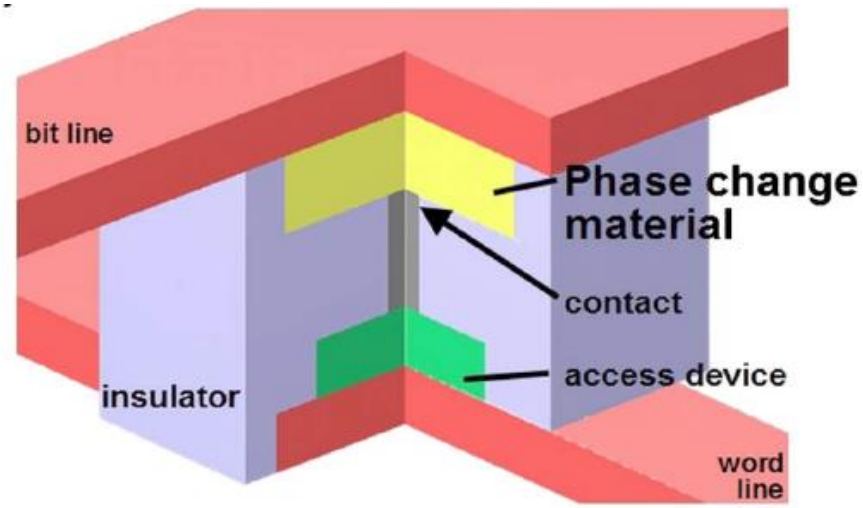
- Possible reasons: better thermal insulation/localization; interfacial effect

Scaling: Programming Current

HSP Wong *et al*, *Proc. IEEE* 98, 2201 (2010)



PCM "Mushroom" Cell

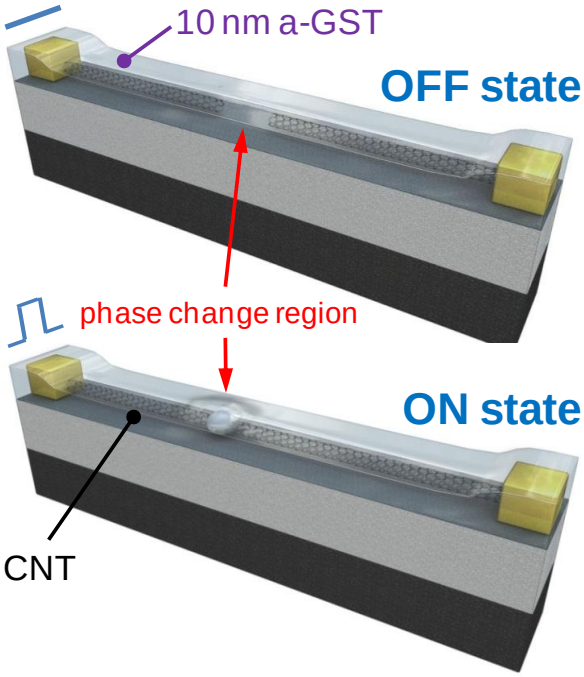


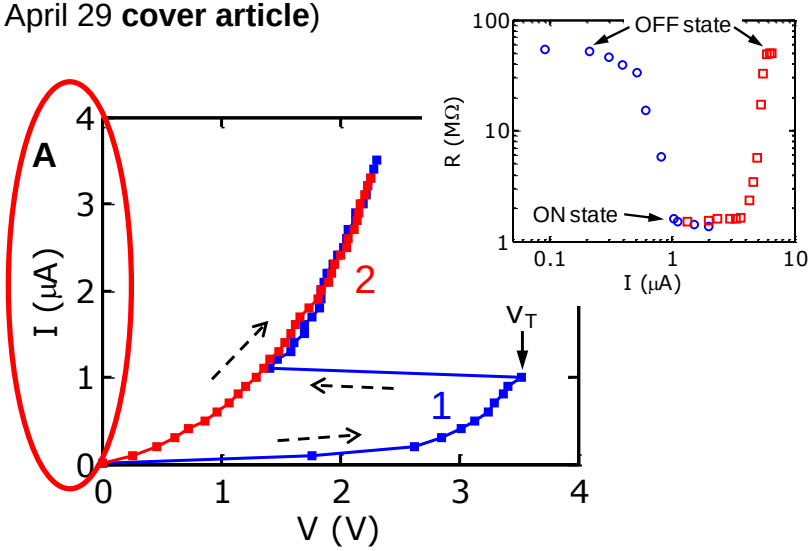
S. Raoux, *et al*, *IBM J.R.Dev.* 52, 468 (2008)

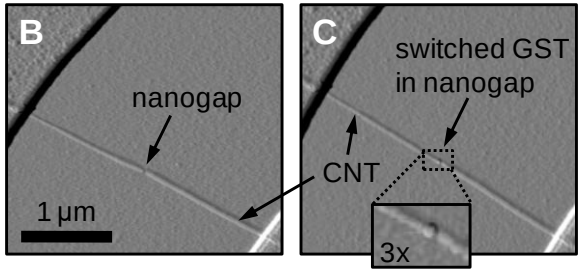
- Phase change memory is highly scalable with electrode size
- Nanowire vs Nanoscale Electrode

Nanotube – PCM Device

F. Xiong, A. Liao, D. Estrada, E. Pop, *Science* **332**, 568 (2011, April 29 **cover article**)





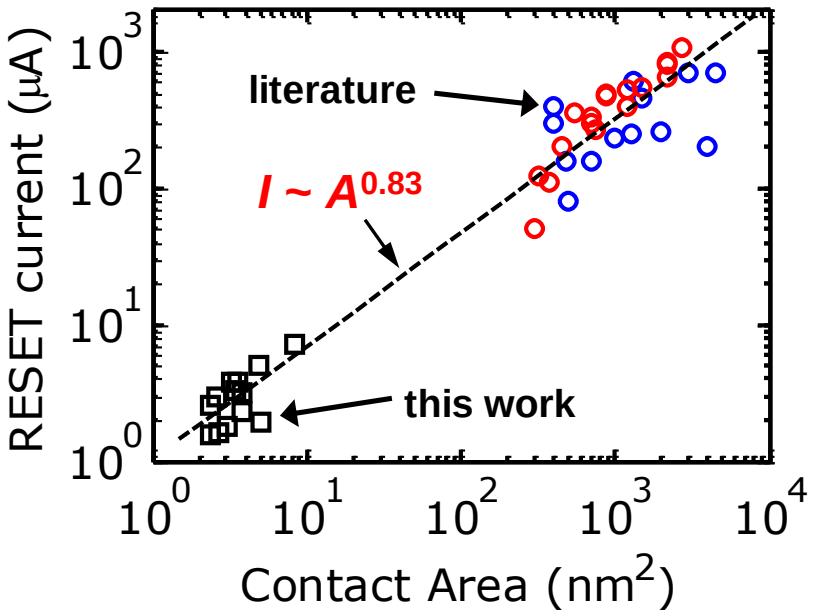


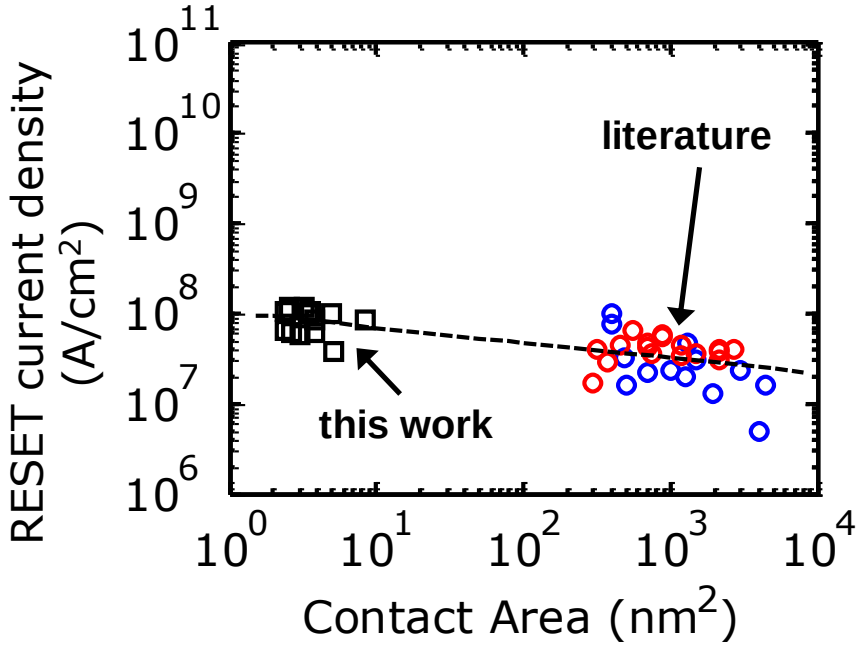
Patent TF11023 Filed

- Make CNT nanogaps by AFM or electrical "cutting"
- CNT nanogap filled with PCMs (here GST)
- I_{set} ~ 1 μA, I_{reset} ~ 5 μA **(~100x < conventional PCM)**

RESET Current Scaling

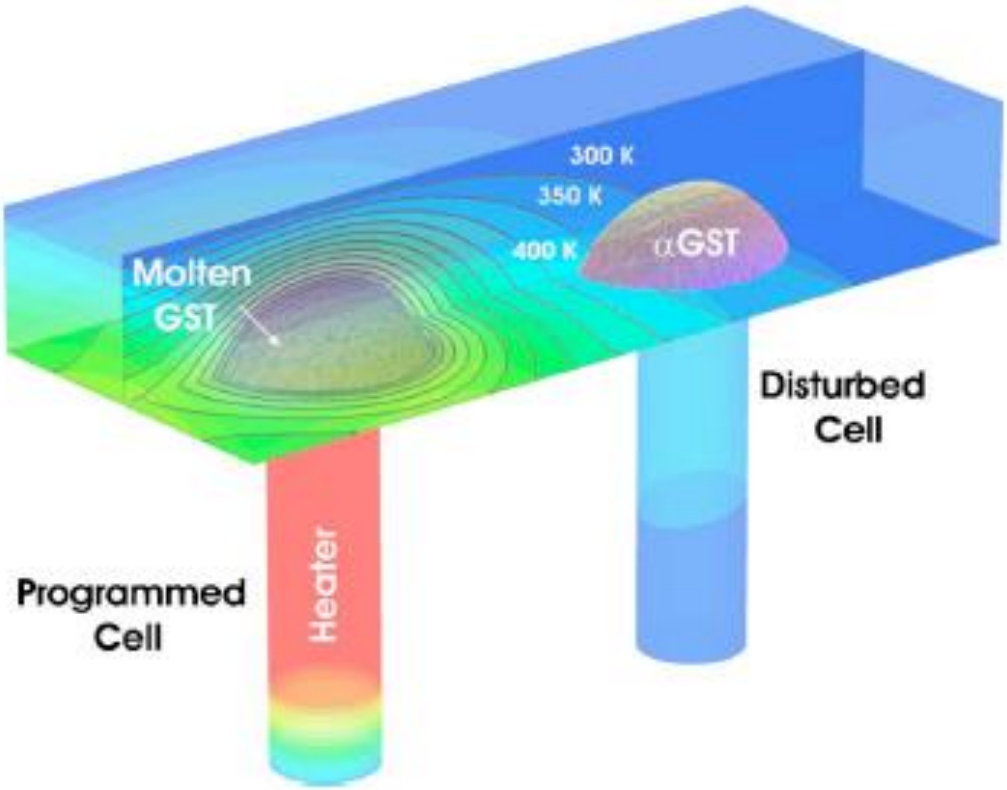
F. Xiong, M.-H. Bae, Y. Dai, A. Liao, A. Behnam, E. Carrion, S. Hong, D. Ielmini, E. Pop, *Nano Lett.* **13**, 464 (2013)





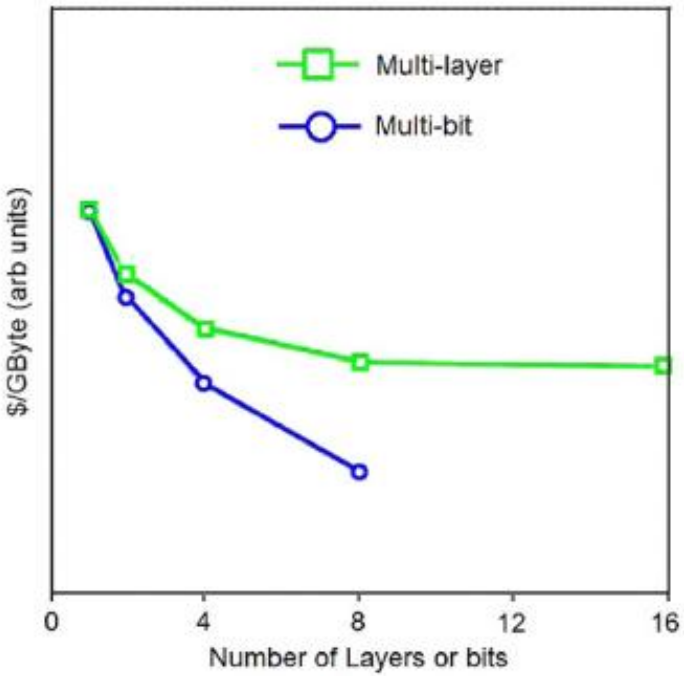
- $I_{reset} \sim A^{0.83}$
- CNT electrode → 100x reduction in I_{reset}
- Isotropic scaling (equal scaling of all three dimensions) → $I_{reset} \sim A^{1}$
- non-isotropic scaling → exponent of 0.83
- $I_{reset}/A \sim A^{-0.17}$ → higher current density as device scales

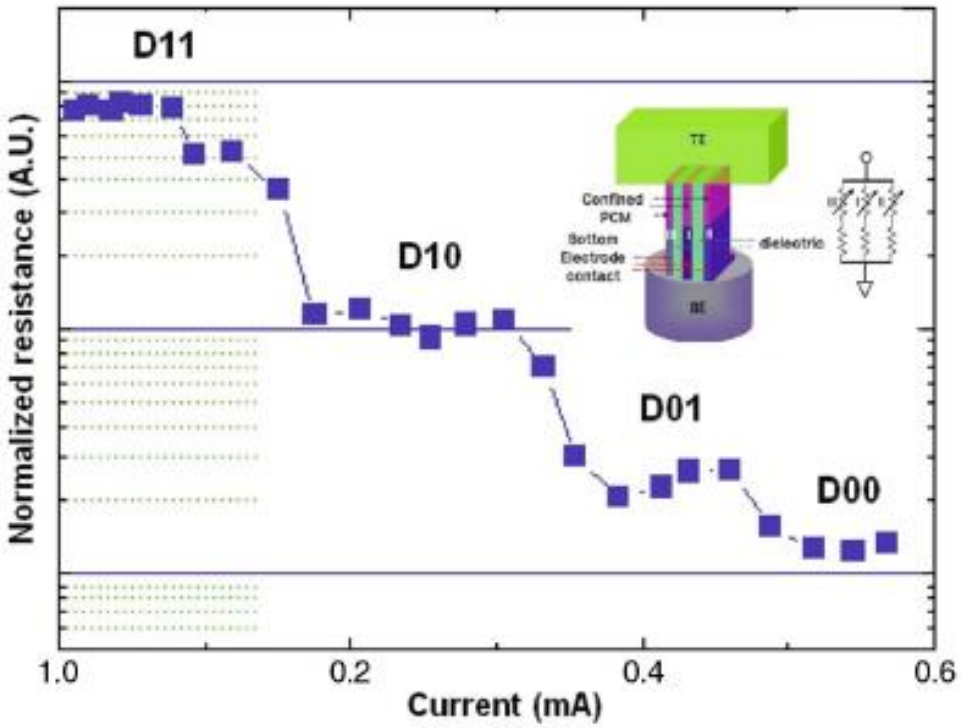
Thermal Cross-Talk



- Thermal cross-talk: inadvertent programming of adjacent cell
- Thermal cross-talk affected by scaling of cell distance

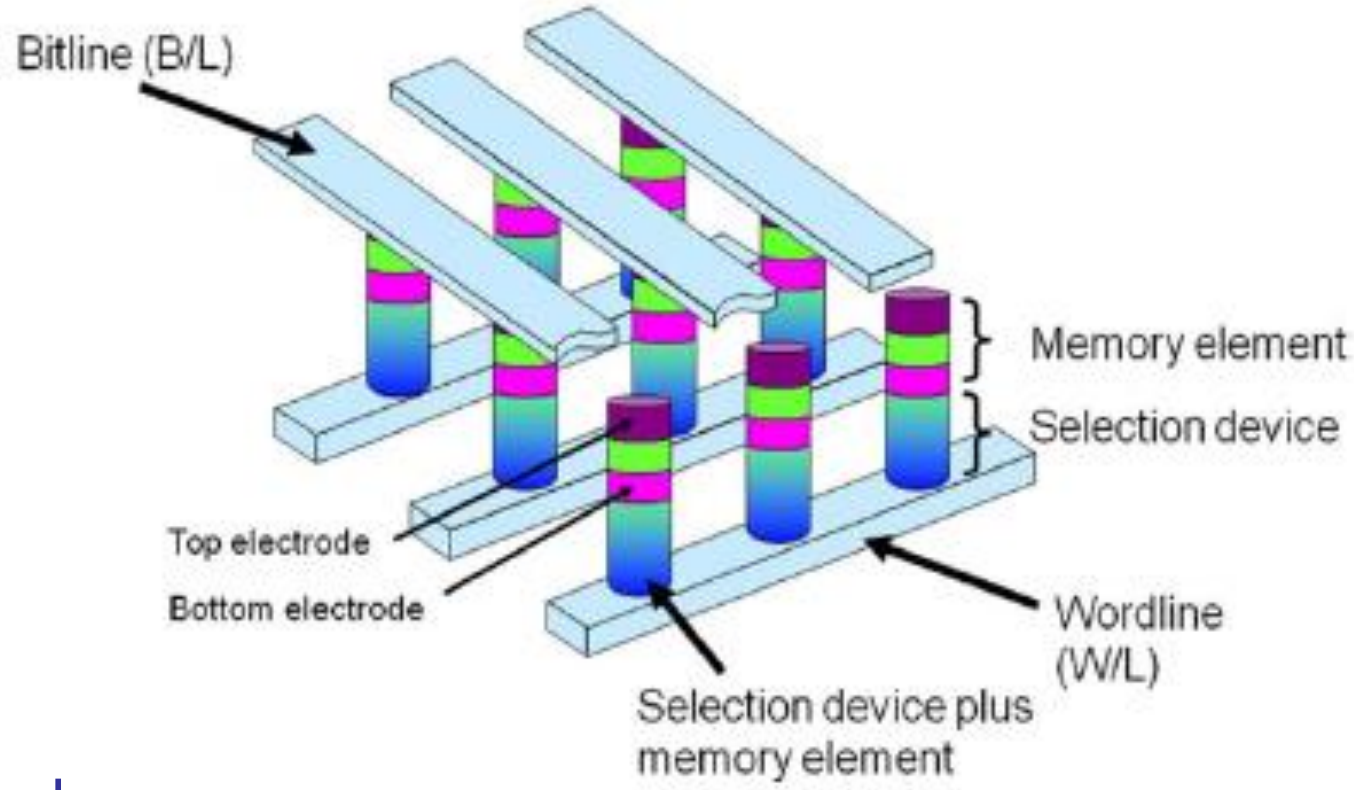
Multi-Level Cell





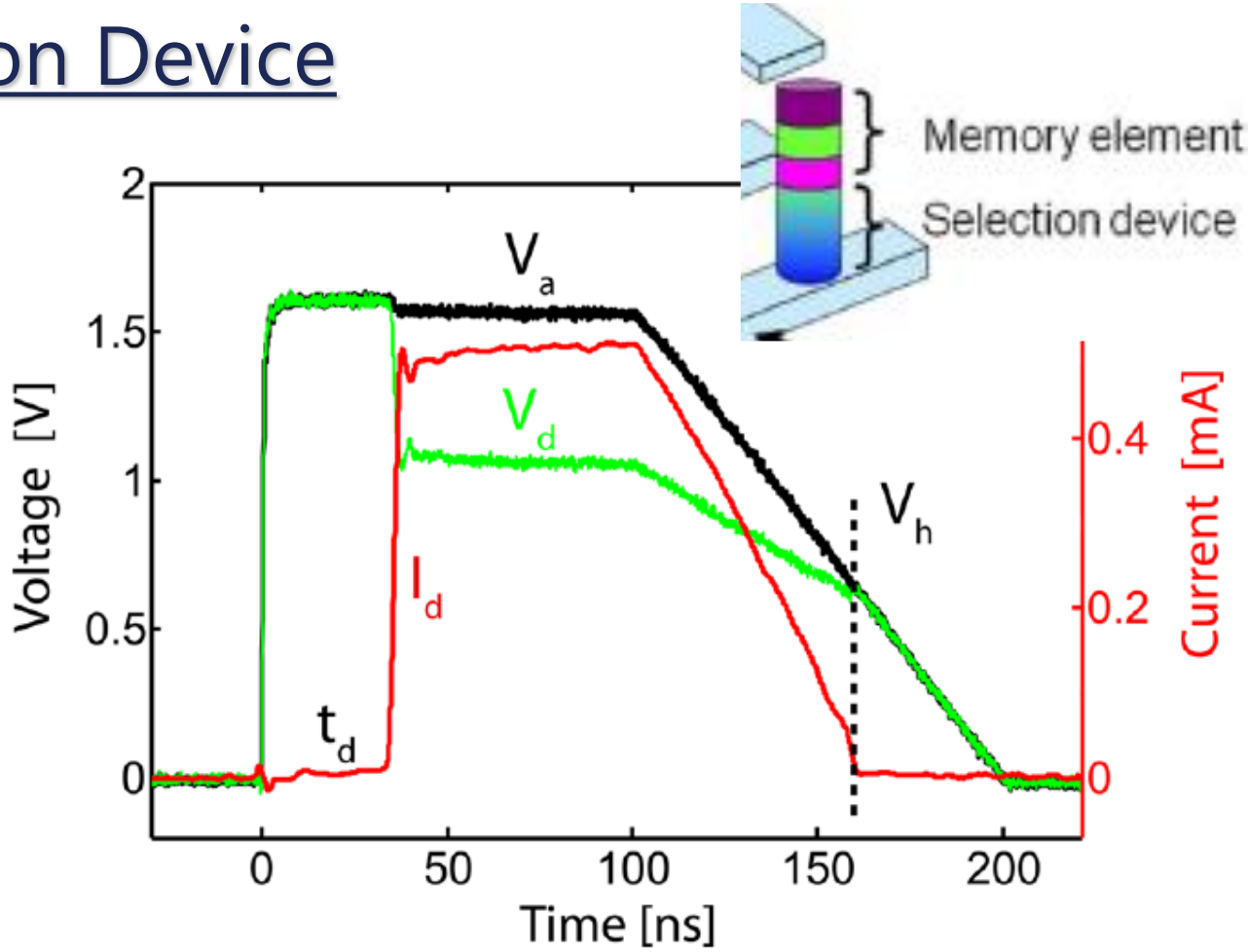
- Multi-level of resistance level to increase density
- Iterative programming: reset first then set

Crossbar Memory Array



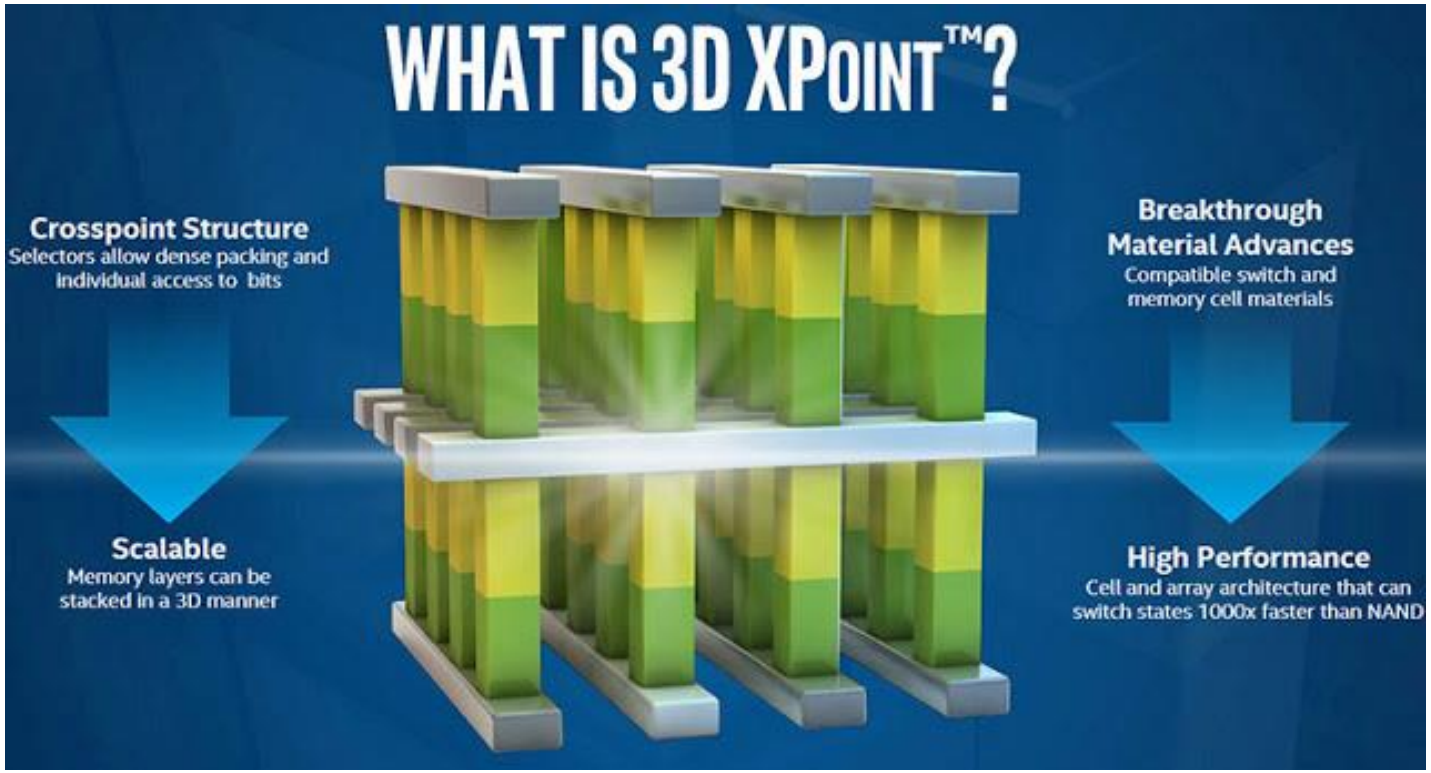
- Crossbar array
  - random access, CMOS compatible
  - high density, small cross-sectional area (low power)
  - selection device needed

Selection Device



- CMOS transistor could provide enough current density
- BJT consumes large power with big foot print
- Chalcogenide selector – shows OTS switching but NO crystallization (high T_{crys} or disordered)

3D Xpoint from Intel

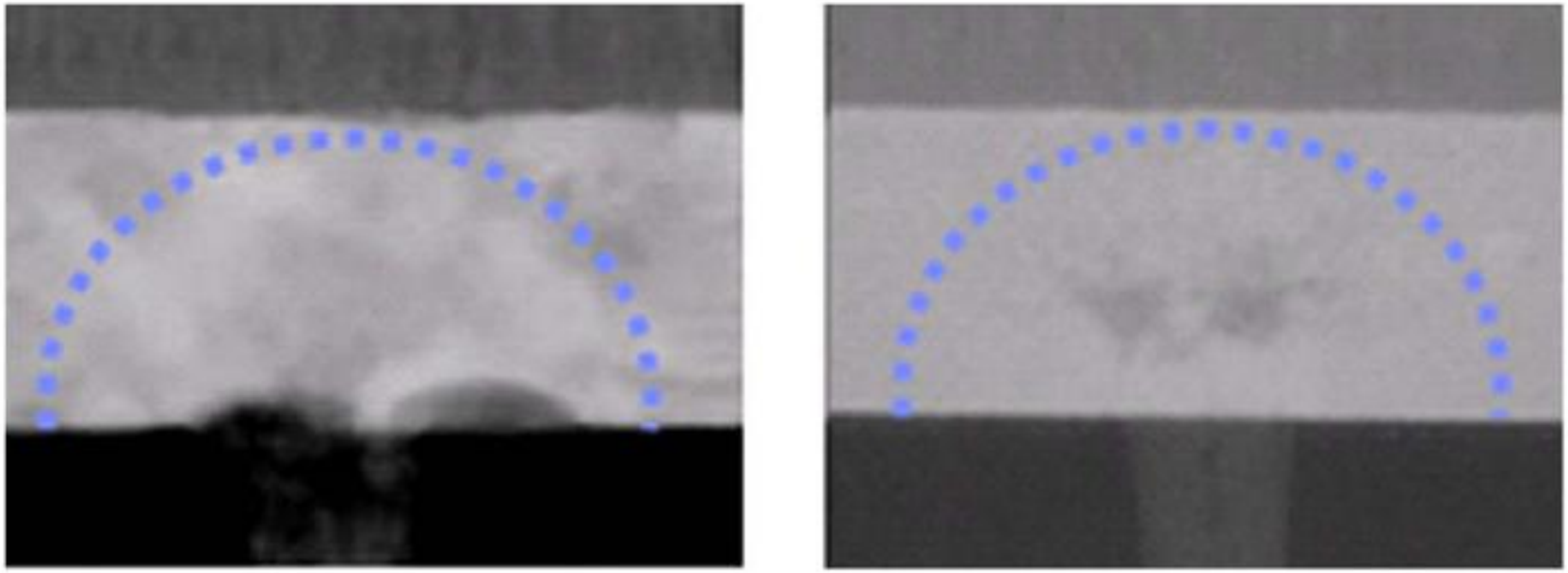


- stackable cross-point structure
- bridging storage and memory

PCM Endurance Issue

- The best reported endurance in PCM is 10^{12} cycles for GST
- Average ~10^6 to 10^9 cycles
- Compare to flash (~10^3-10^4) and DRAM (~10^{16} to 10^{18})
- Intrinsically a more "damaging" process: melting and quenching
- Two major failure mechanisms in PCM
  - Void formation due to volume expansion
  - Phase segregation due to melting

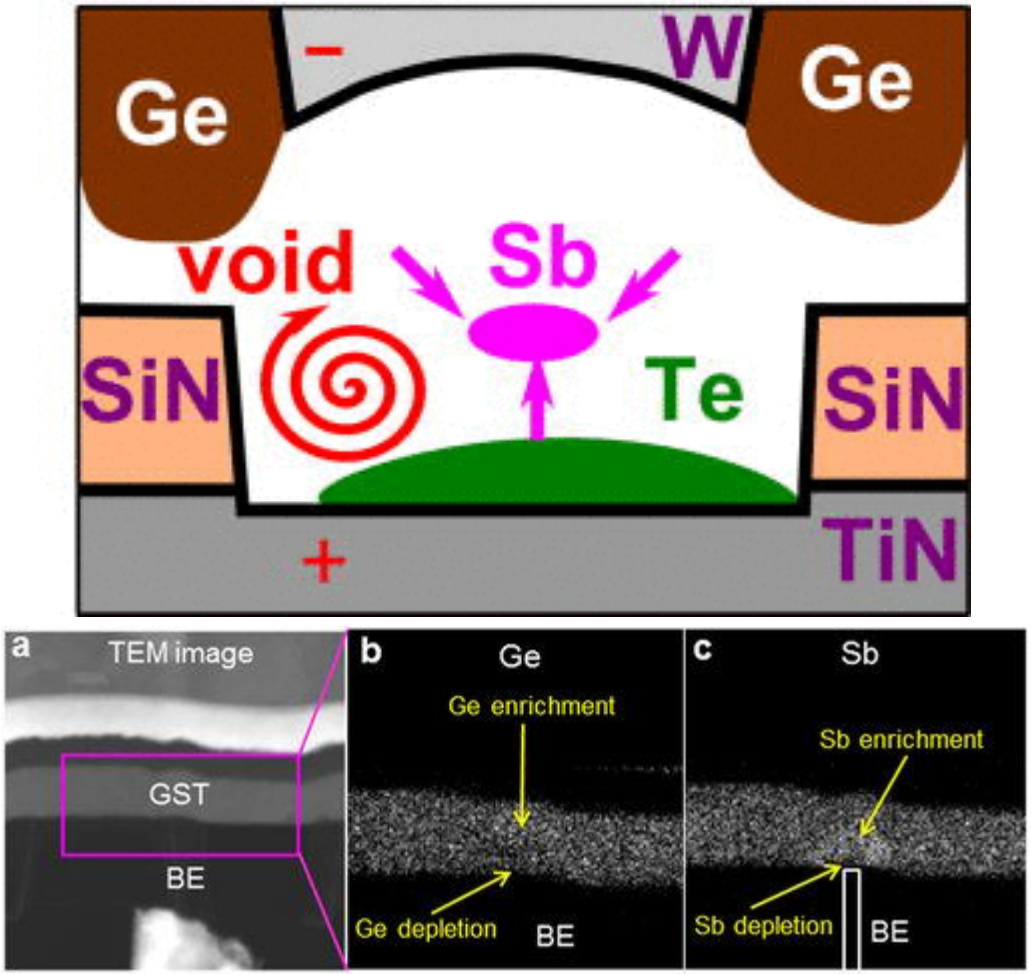
Void Formation



C.-F. Chen et al., Proc. IEEE Int. Memory Workshop, 2009

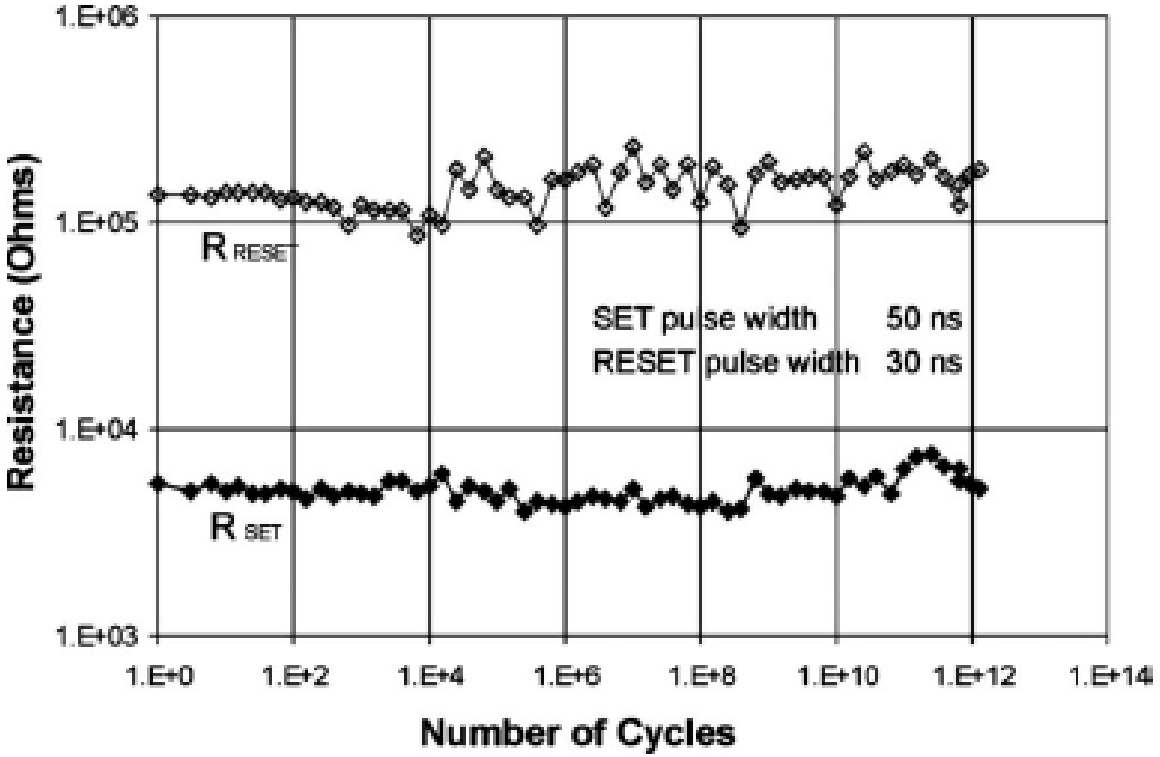
- 7% volume change upon phase change in GST
- Voids will form in the phase change film
- Solution: materials with smaller volume change

Phase Segregation



- Phase segregation and void formation due to E-field
- Affects endurance; Solution: bipolar switching

Variability



- Intra-device variability
- Melt-quench reset is inherently stochastic
- Large variability → narrows the operating window esp for MLC