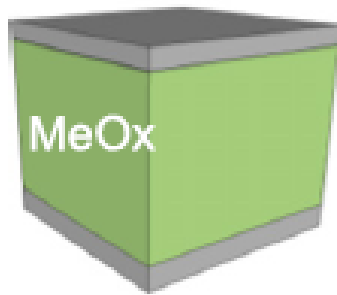


# **L6: Resistive RAM II**

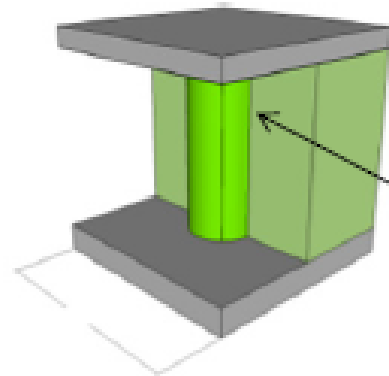
# Recap

Top electrode (TE)



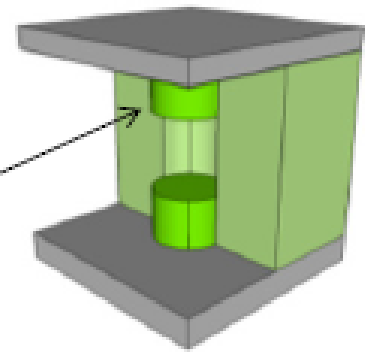
Bottom electrode (TE)

(a) Initial state



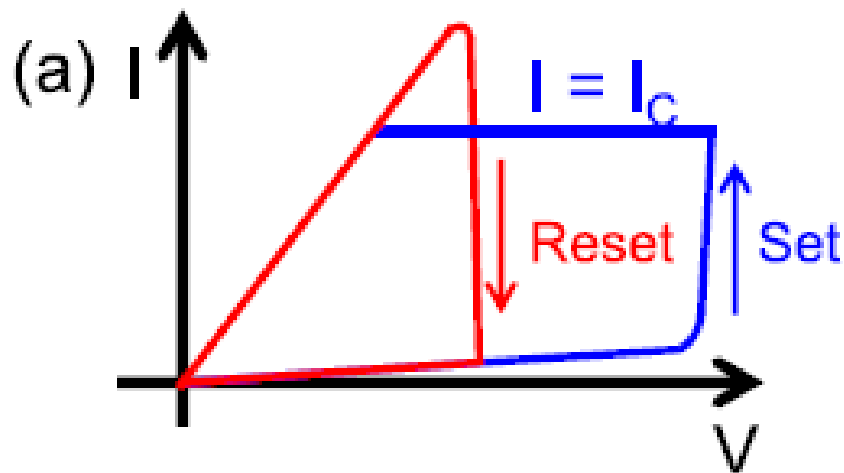
Conductive filament

(b) Set state

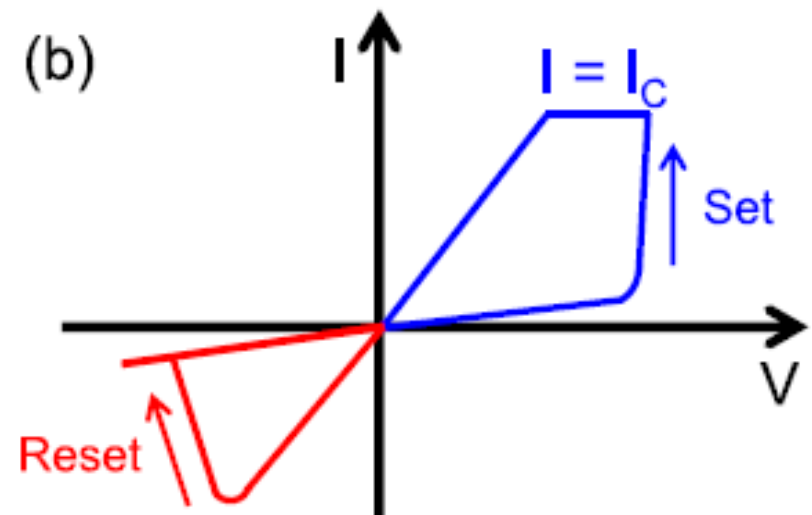


(c) Reset state

## Unipolar

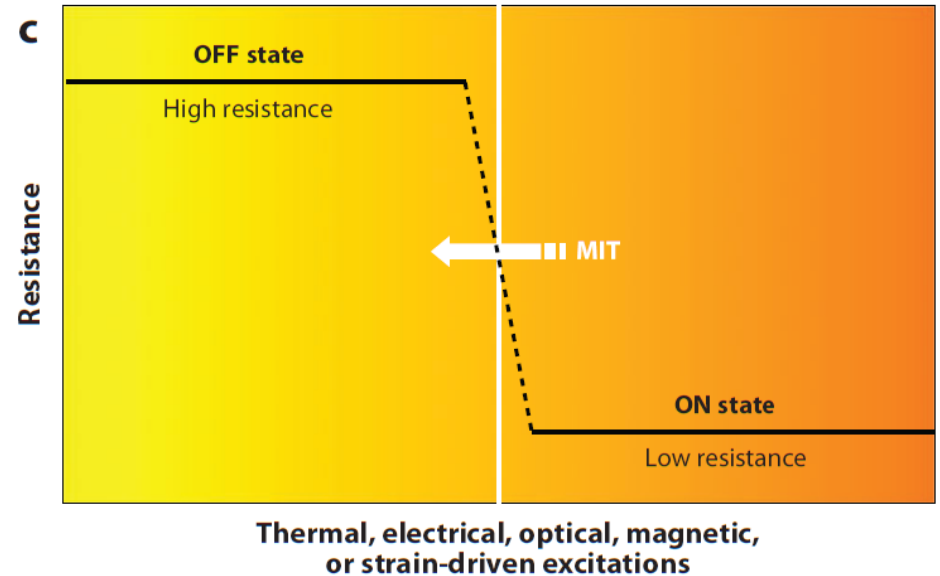
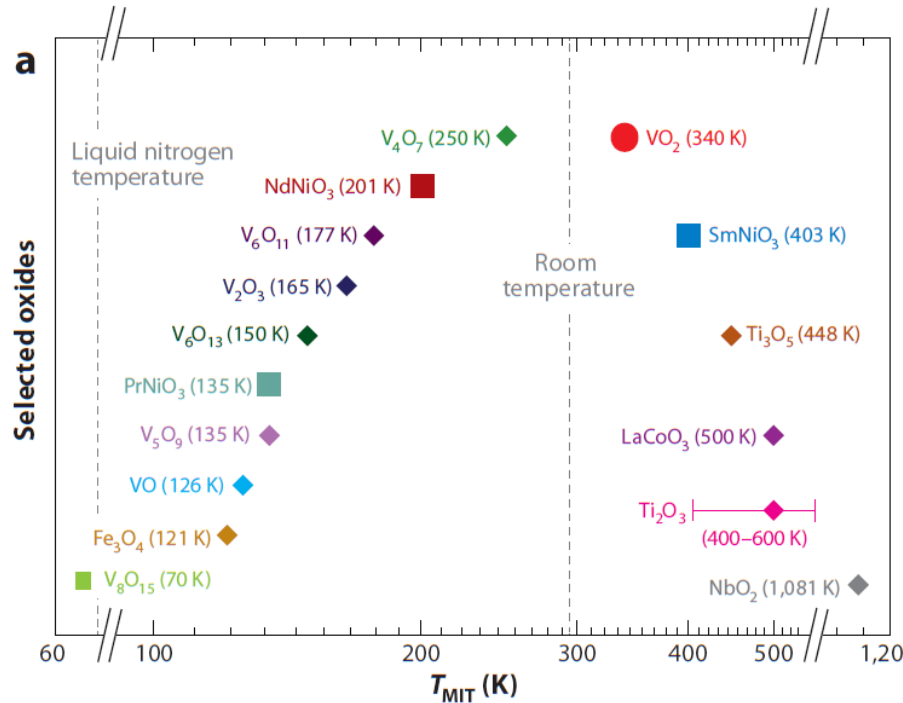


## Bipolar



# Metal-Insulator Transition (MIT)

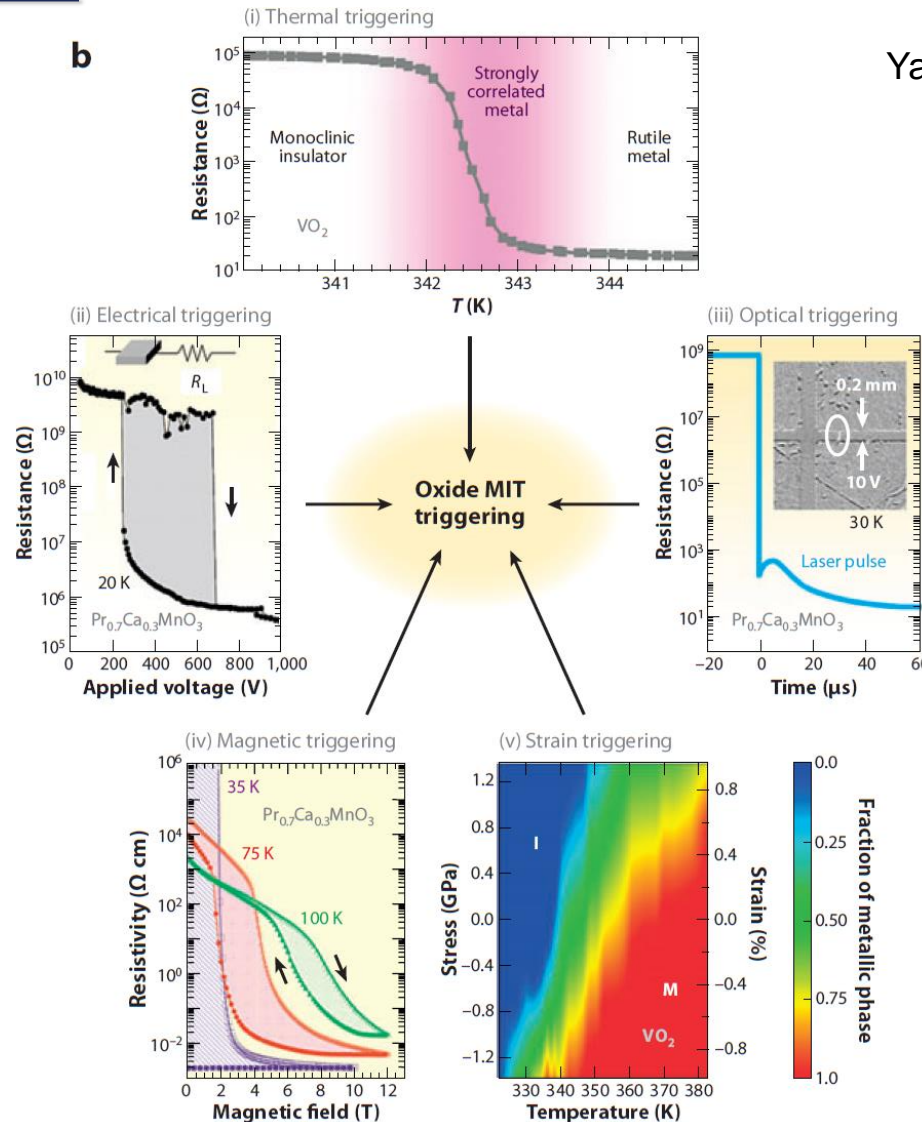
Yang et al., Annual Rev., 2011



- Metal-insulator transition
- Happens in metal oxides:  $VO_2$ ,  $V_2O_3$ ,  $VO$  and  $Ti_2O_3$
- Transition temperature  $T_{MIT}$

# MIT Triggers

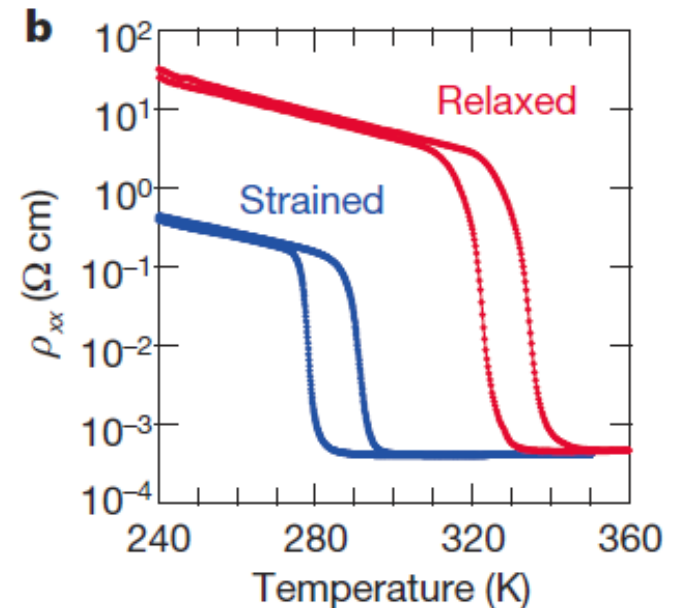
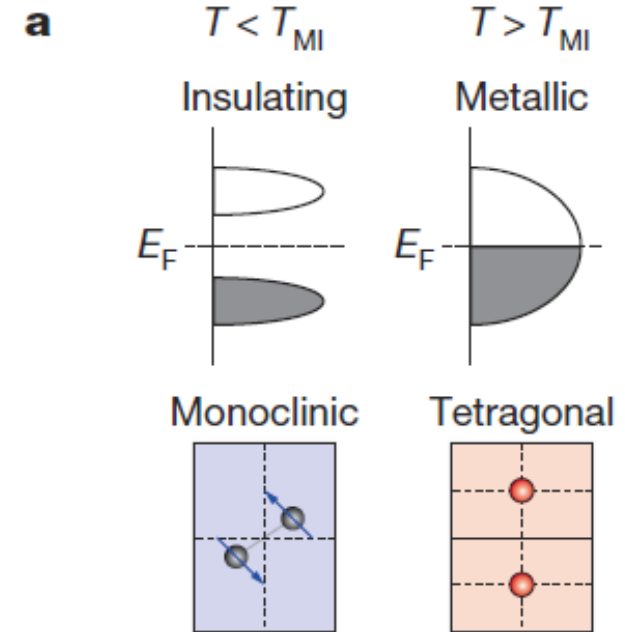
Yang et al., Annual Rev., 2011



- Triggered thermally, electrically, optically and magnetically

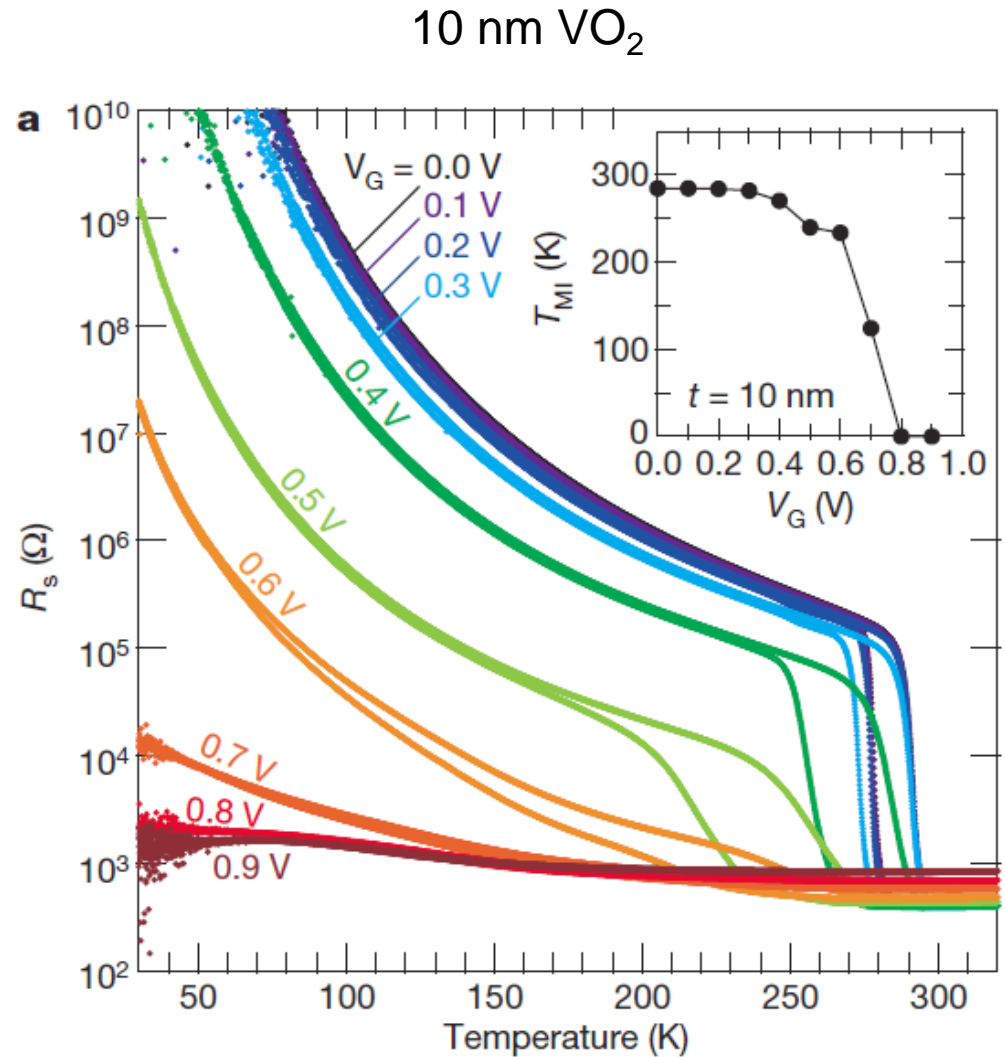
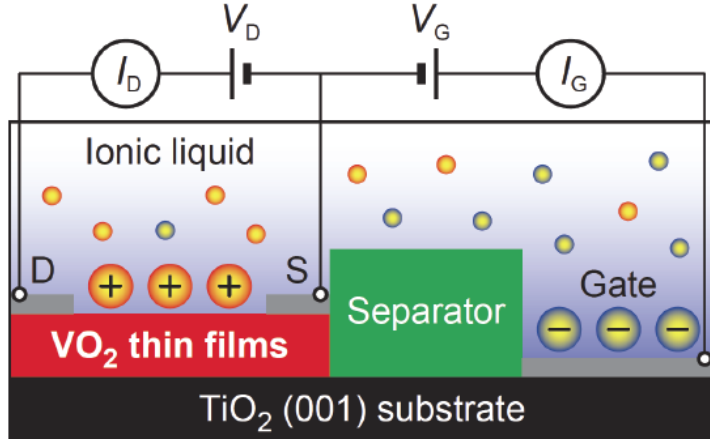
# MIT Induced by Temperature

- Vanadium dioxide  $\text{VO}_2$
- Metal-Insulator transition  $T_{\text{MIT}} \sim 340 \text{ K}$  or  $67 \text{ C}$
- Tunable  $T_{\text{MIT}}$  via strain
- Low-Temp Monoclinic phase (3d electrons localized on V site)
- High-Temp tetragonal phase (mobile 3d electrons)



# Inducing MIT with E-field

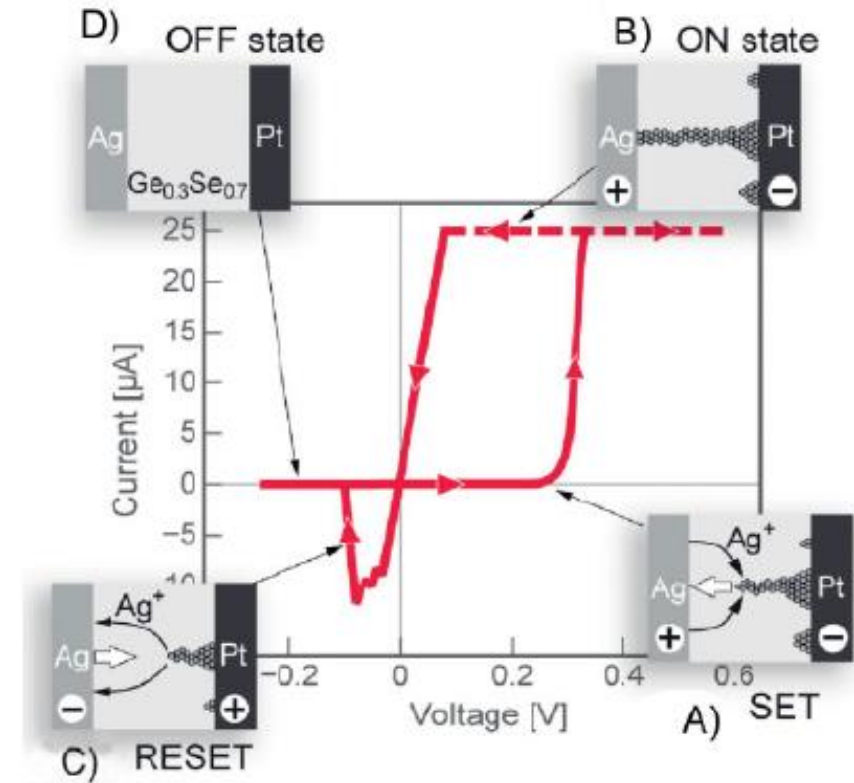
- No MIT has been achieved in  $\text{VO}_2$  by pure electrostatic
  - requiring too high of an E-field
- $T_{\text{MIT}}$  can be tuned by electron doping
  - ionic liquid gating  $\rightarrow$  surface charge density  $10^{15} \text{ cm}^{-2}$



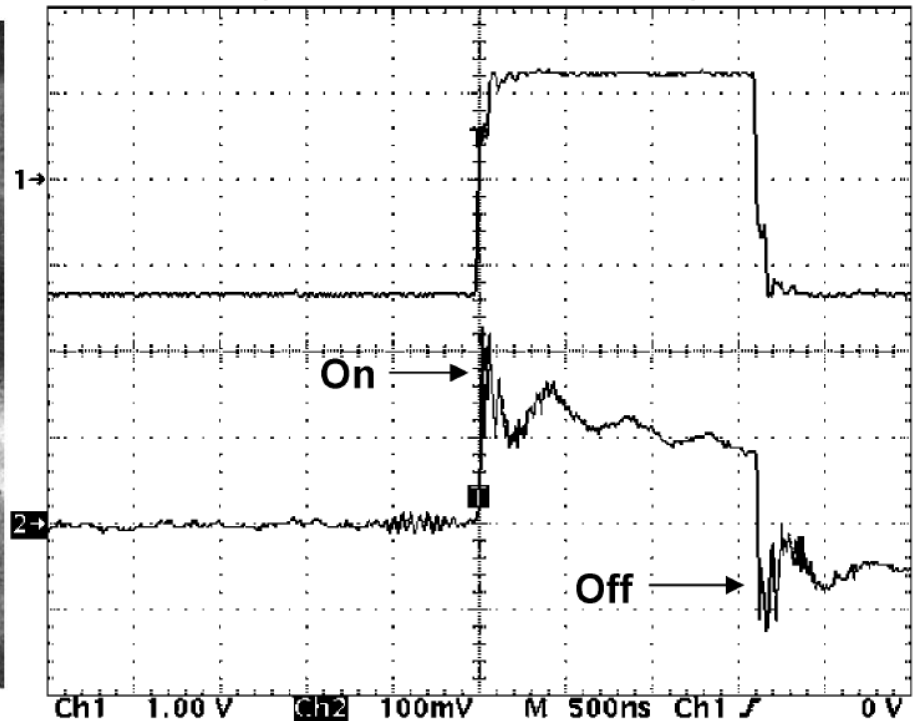
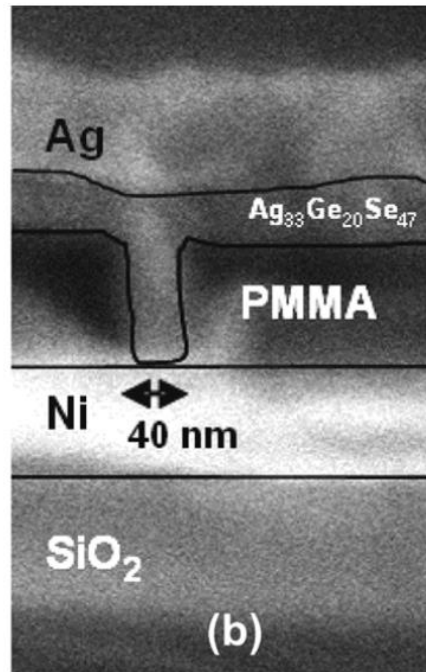
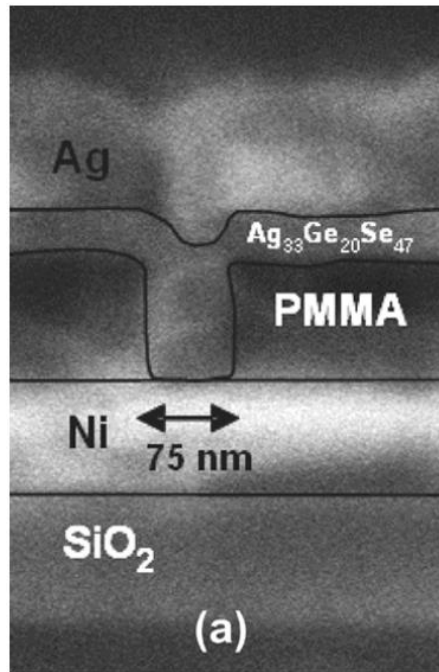
Nakano et al., Nature, 2012

# Electrochemical Metallization (ECM) Device

- Switching type: bipolar
- Switching material: chalcogenides (GeS,  $\text{Ag}_2\text{S}$ , etc), amorphous film (a-Si, a-C, etc)
- E-field driven redox reactions
- Metal filament formation
- Electrode plays an active role (e.g. Ag or Cu)



# High Speed AgGeSe Device



- AgGeSe compound with Ag electrode
- sub-70 ns switching speed

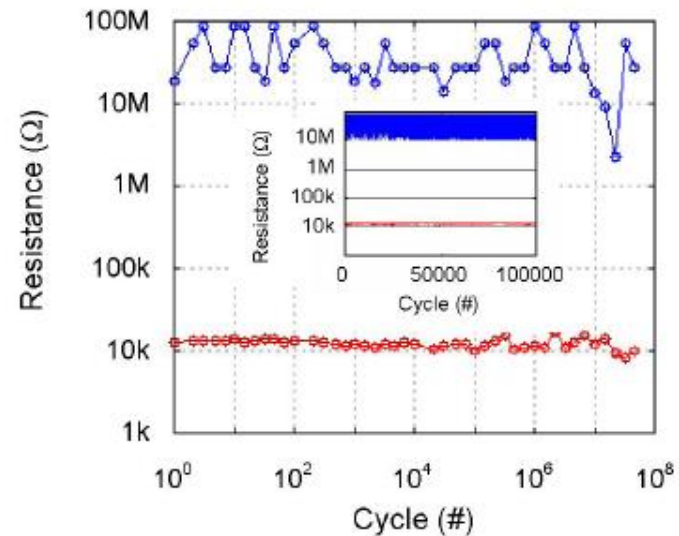
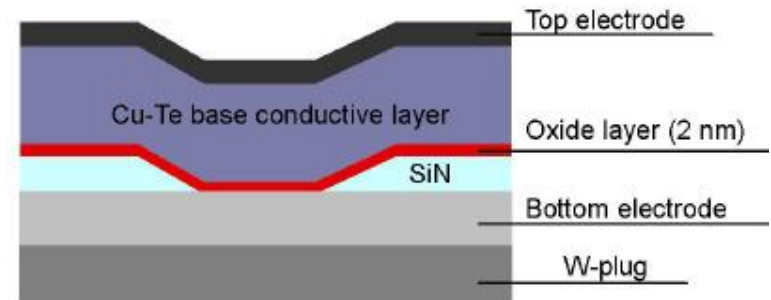
Kozicki et al., IEEE T-NANO, 2005



# Cu-Te ECM Device

**Table 1.** Typical parameters and key features.

FEOL	180-nm CMOS
Active cell area	40 nm $\phi$
Set pulse width	5 ns
Set current	110 $\mu$ A
Set voltage	+3 V
Reset pulse width	1 ns
Reset current	125 $\mu$ A
Reset voltage	-1.7 V
Resistance read voltage	+0.1 V
Endurance	10 <sup>7</sup> cycles

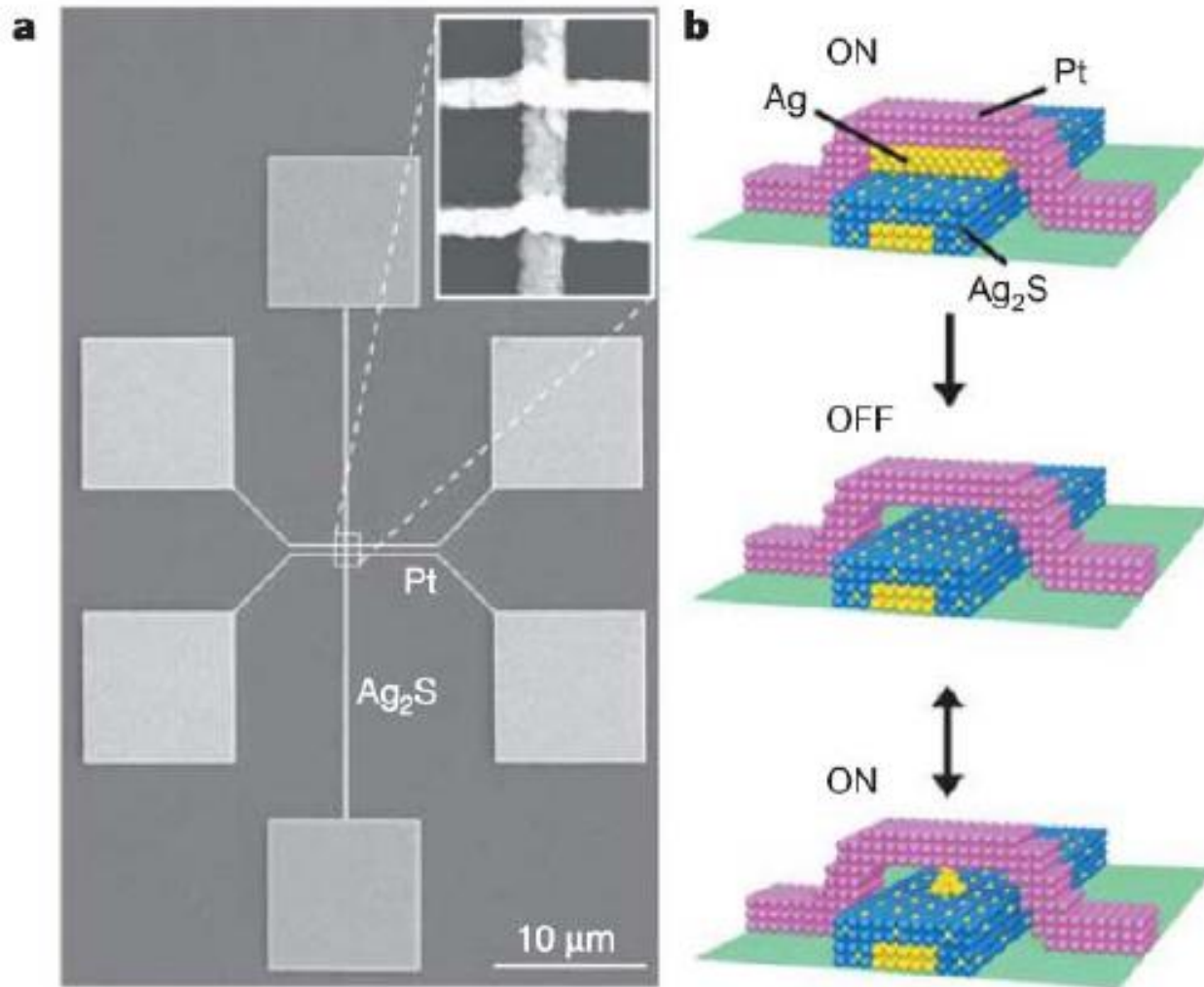


- High speed with good endurance

Aratani et al., IEDM, 2007

# Au Atomic Switch

Terabe et al., Nature, 2005

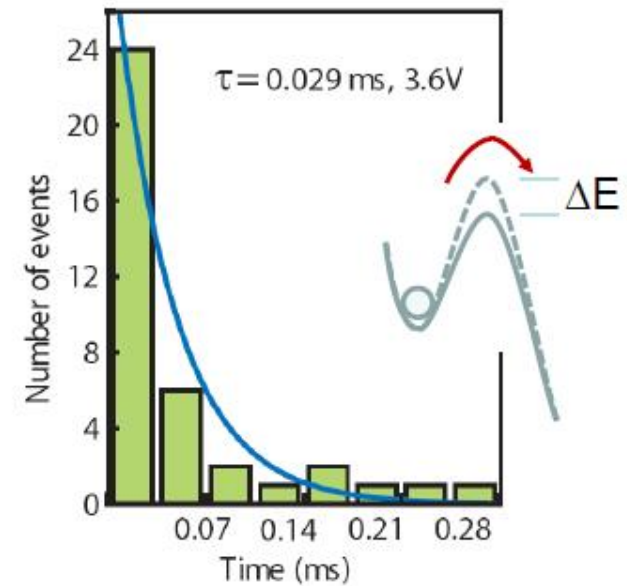
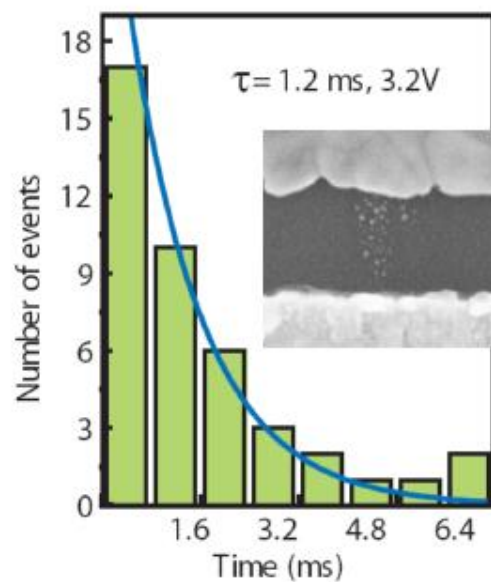
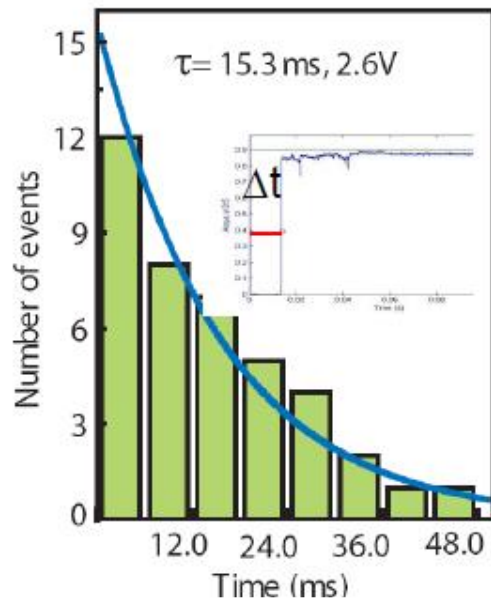


- Single Au atom bridge between TE and BE in  $\text{Ag}_2\text{S}$

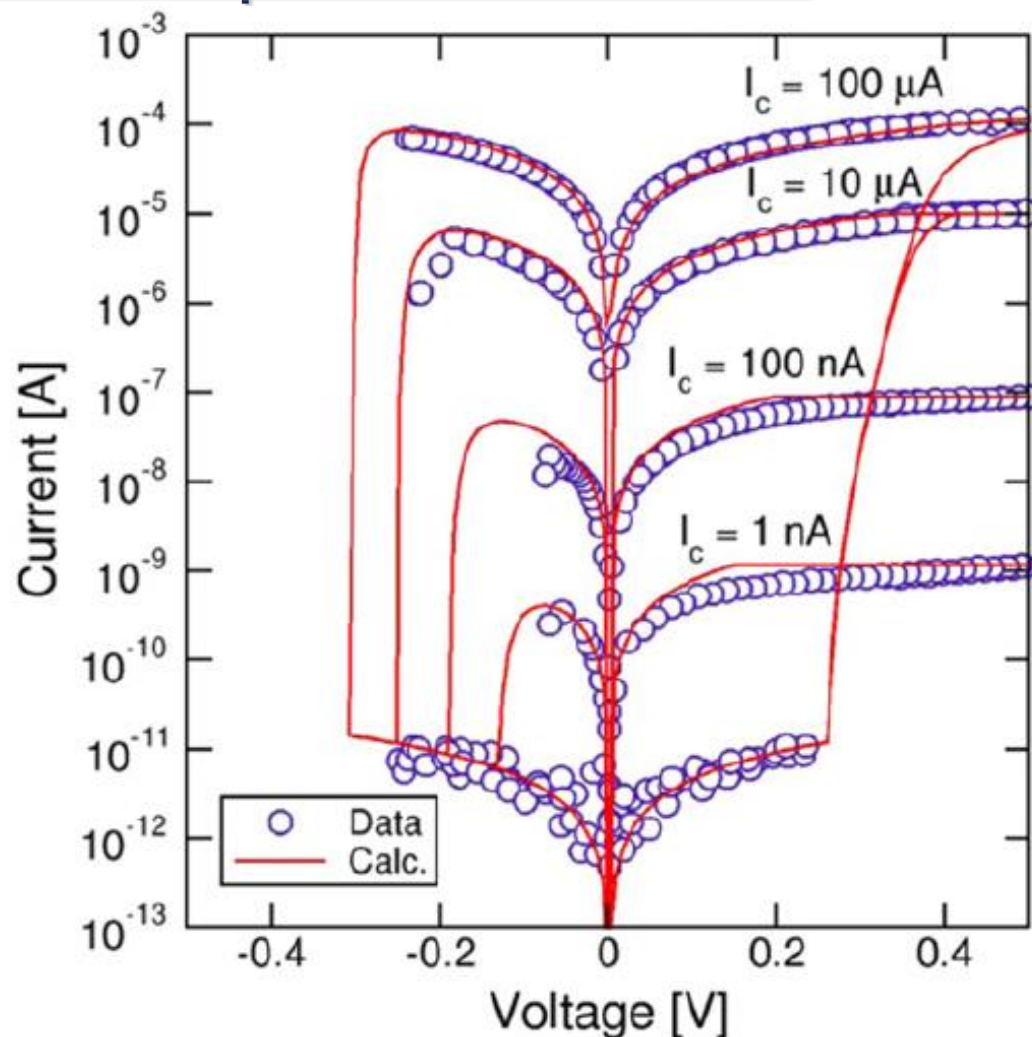
# Stochastic Device

- Stochastic vs deterministic
- True random number generator
  - physical event: thermal noise, radioactive decay
  - too slow
- Filamentary formation is a stochastic process → following a Poisson distribution at a given condition

Gaba et al., Nanoscale, 2013



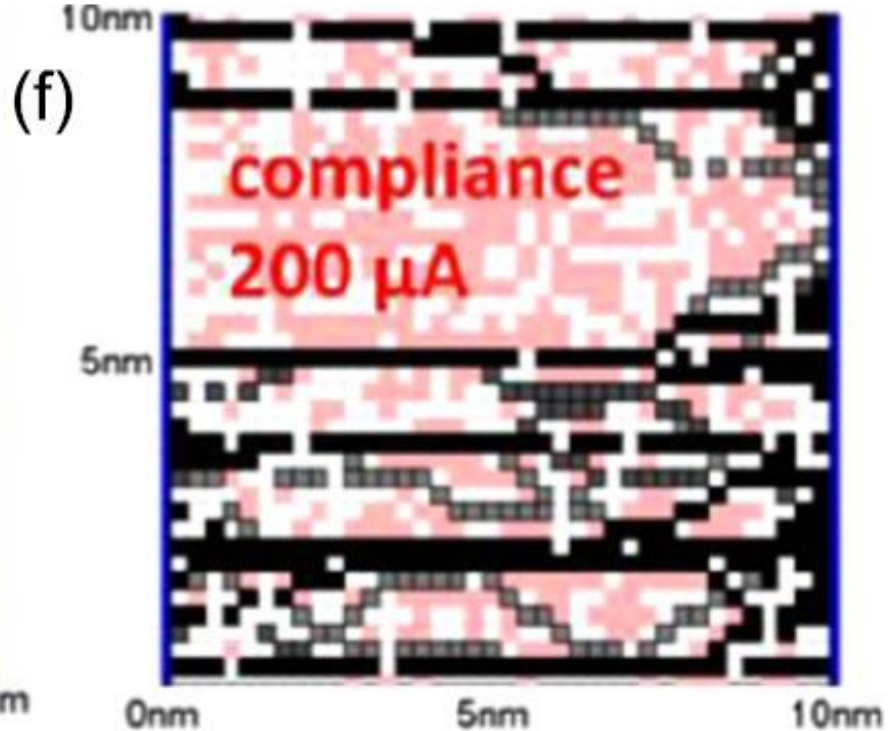
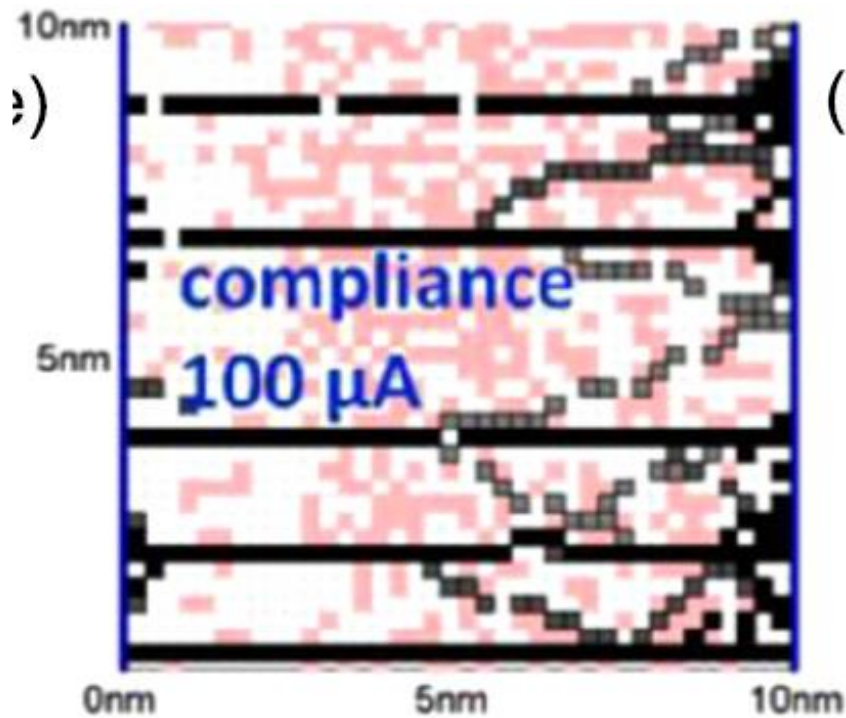
# Effect of Compliance Current



Ielmini et al., SST., 2016

- Compliance determines filament size, thus on/off ratio and voltage

# Modeling of Device



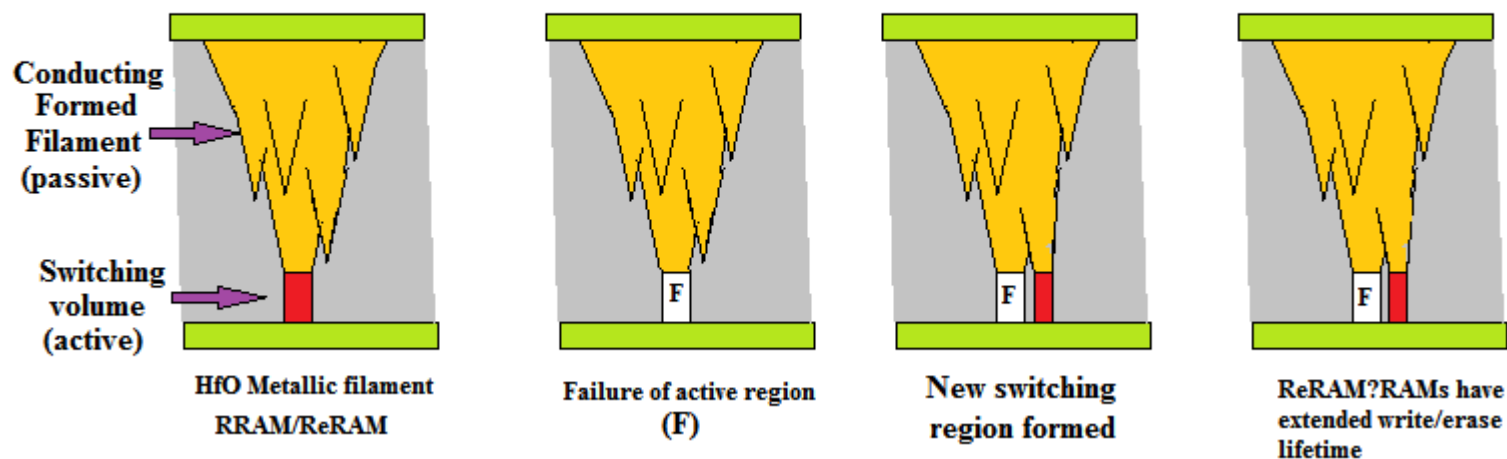
Ielmini et al., SST., 2016

- Modeling of resistive switching with different compliance current
- Affects number of filaments and the size of the filament

# Scalability

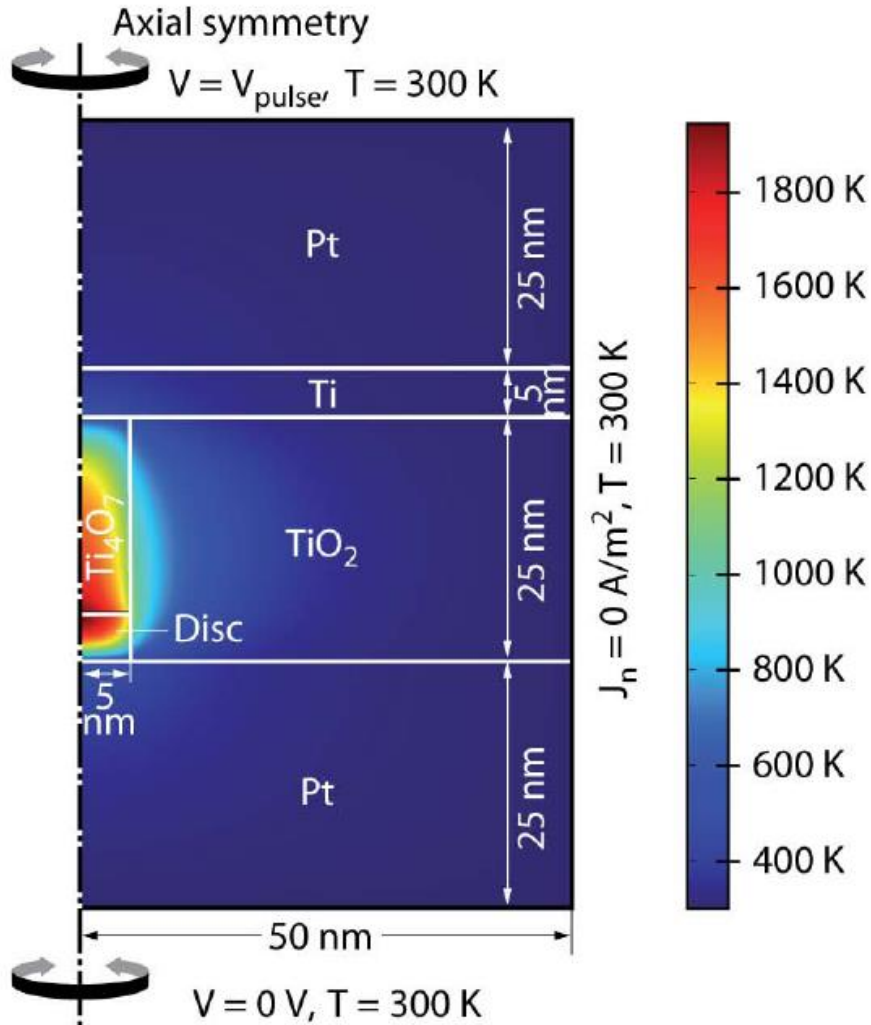
- Conductive filament critical size
  - Switching mechanism
  - Endurance
- Better on/off ratio
- Reduced variability in operations

**Scaling implications: Write/Erase endurance requires the existence of a large filament**

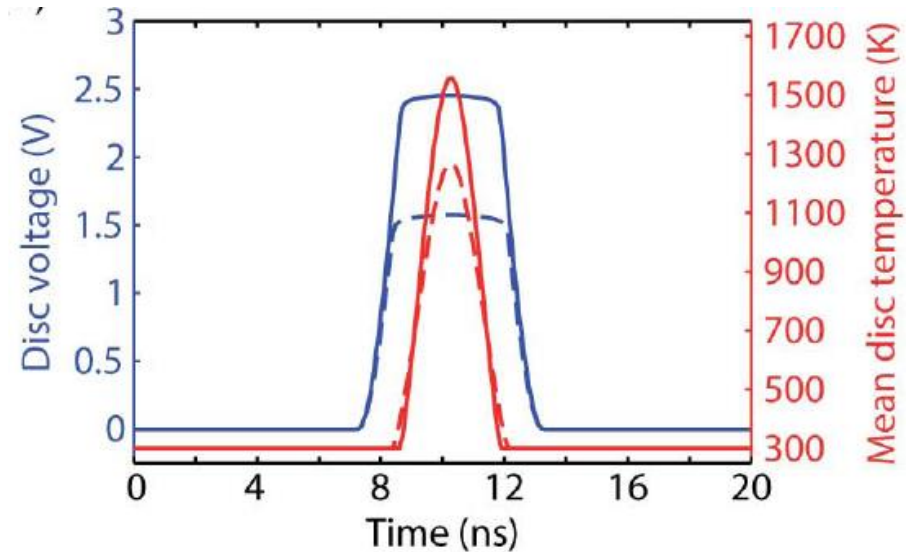




# Switching Speed

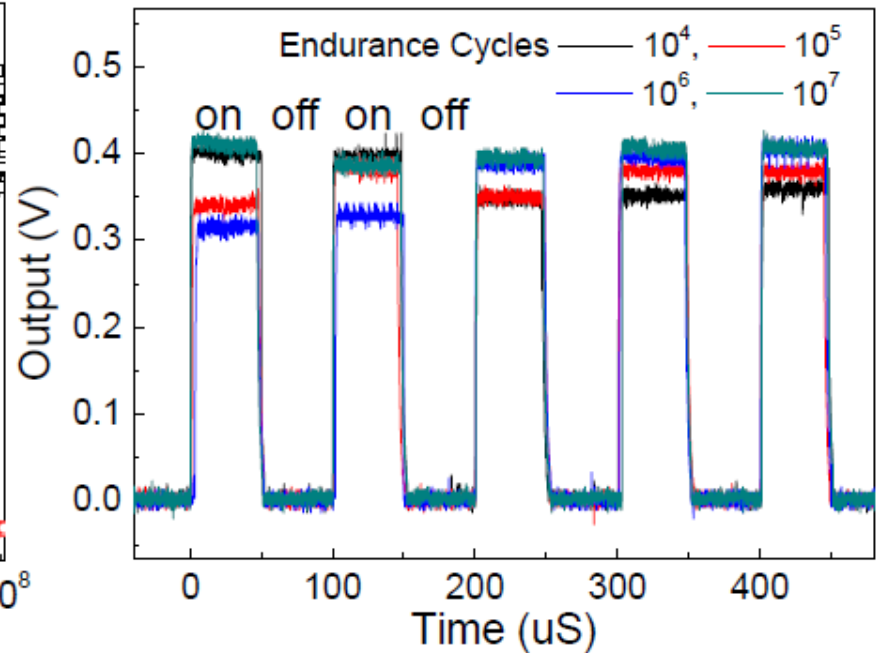
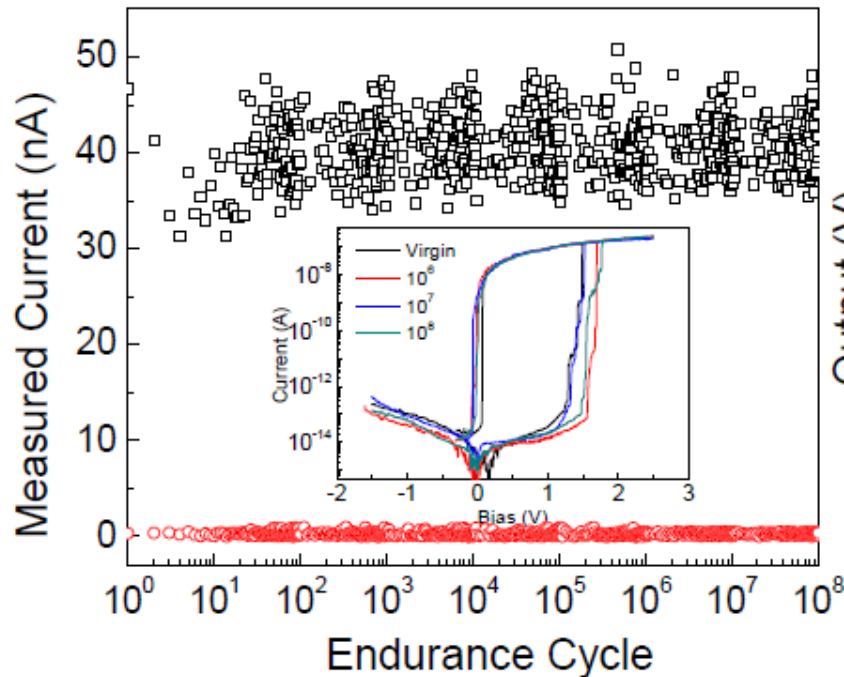


- Benchmark: DRAM write/erase time  $< 10/10 \text{ ns}$
- Pt/Ti/TiO<sub>2</sub>/Pt cross-point
  - 1 ns rise/fall and 3 ns plateau



Hermes et al., IEEE EDL, 2011

# Endurance



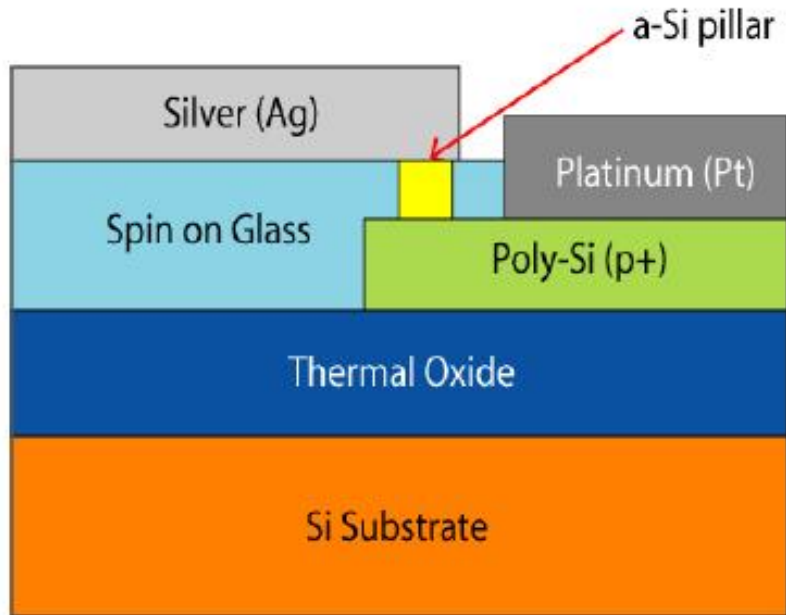
Jo et al., Nano Lett., 2008

- $10^8$  write/erase cycles
- $10^6$  on/off ratio
- Endurance depends on device dimensions

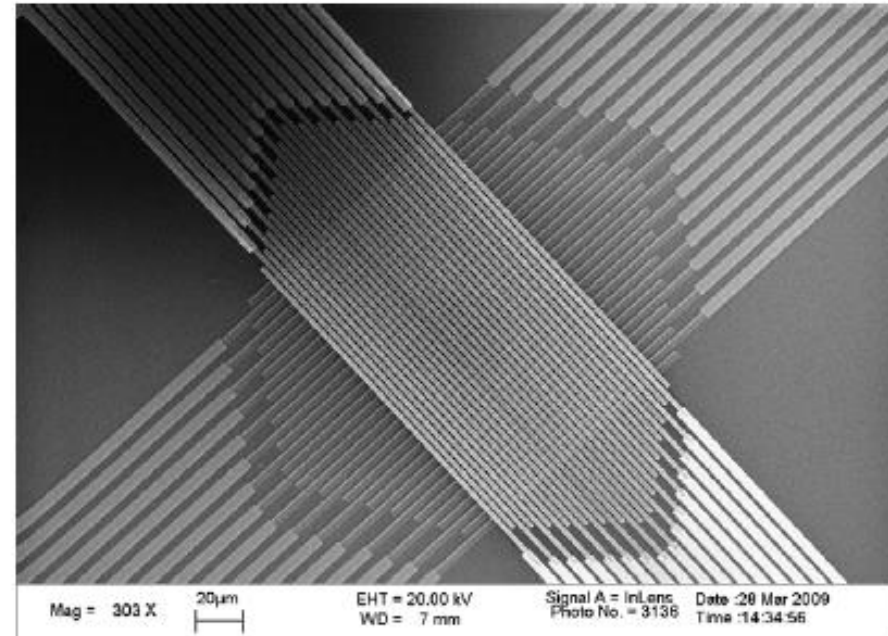


# RRAM Device Structure Pillar vs. Crossbar

Pillar structure



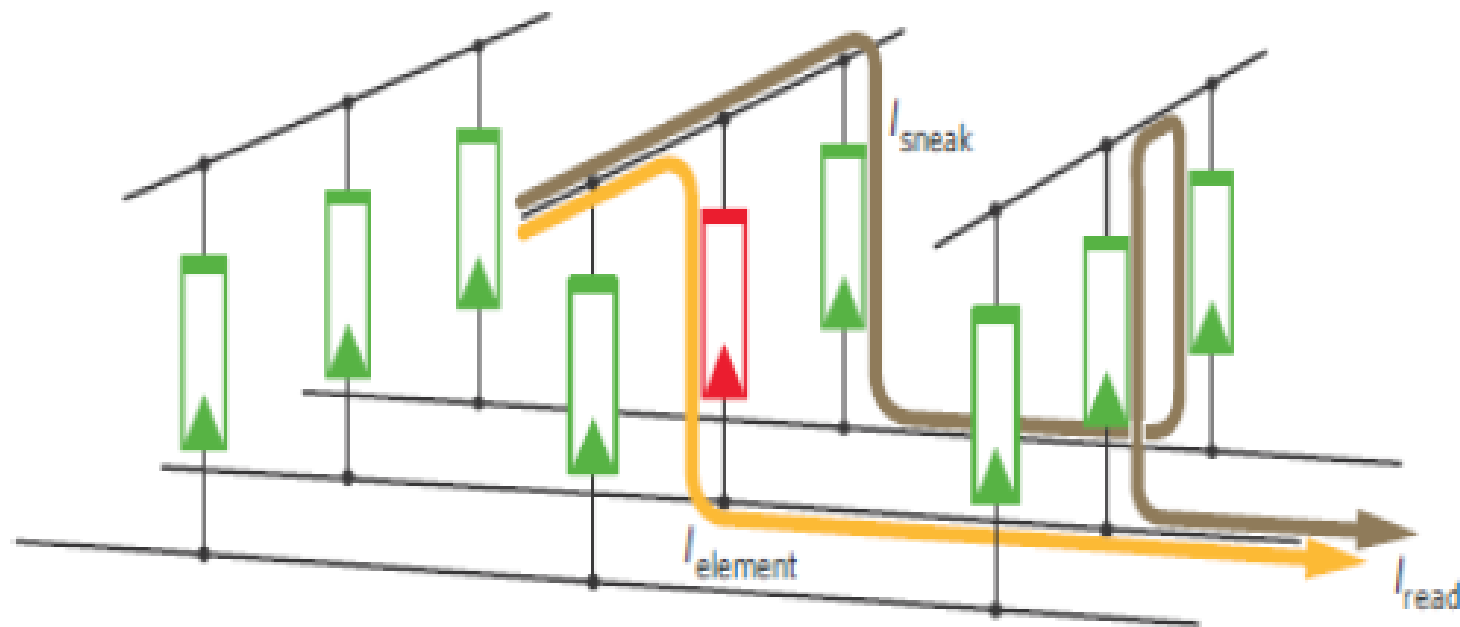
Crossbar array



Jo et al., Nano Lett., 2008

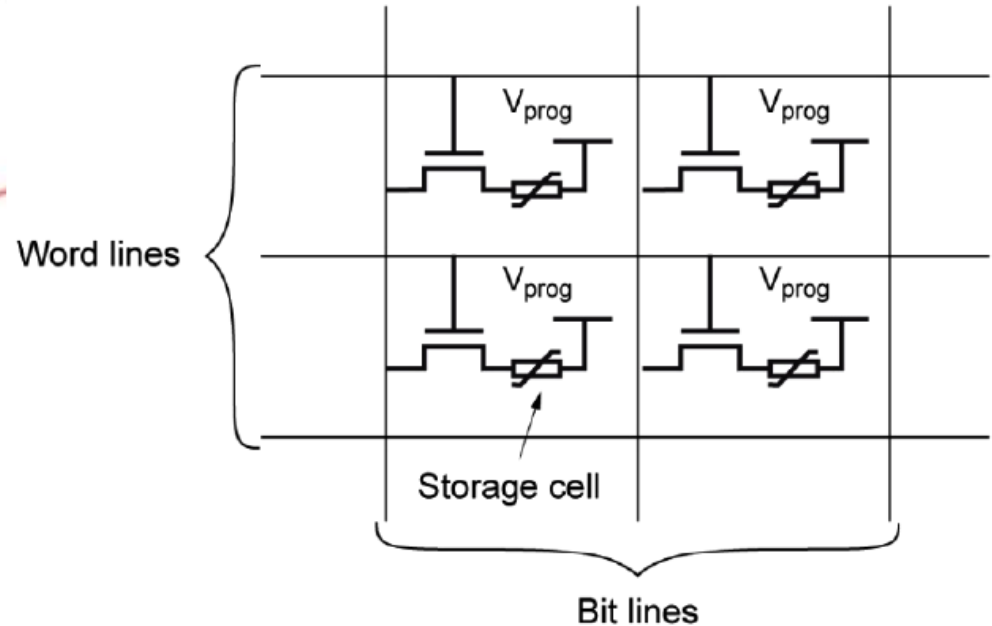
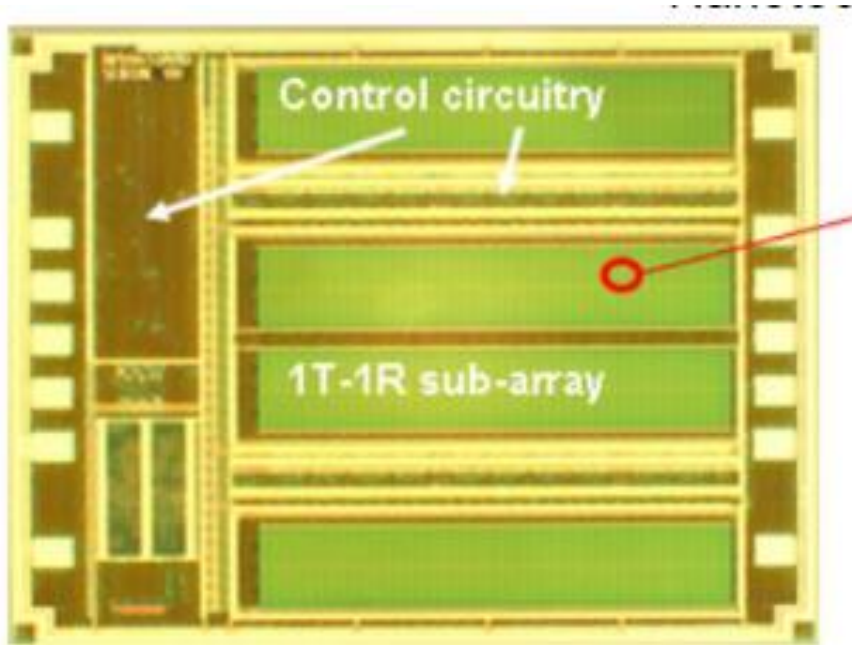
- Pillar vs crossbar
- Pillar is easier to fabricate;
- crossbar has better density and offers random access

# Sneak Path and Selection Device



- Sneak path in crossbar arrays
- Selection device is required
- 1 transistor 1 resistor (1T1R)
- 1 diode 1 resistor (1D1R), more compact

# 1T1R Array Demonstration

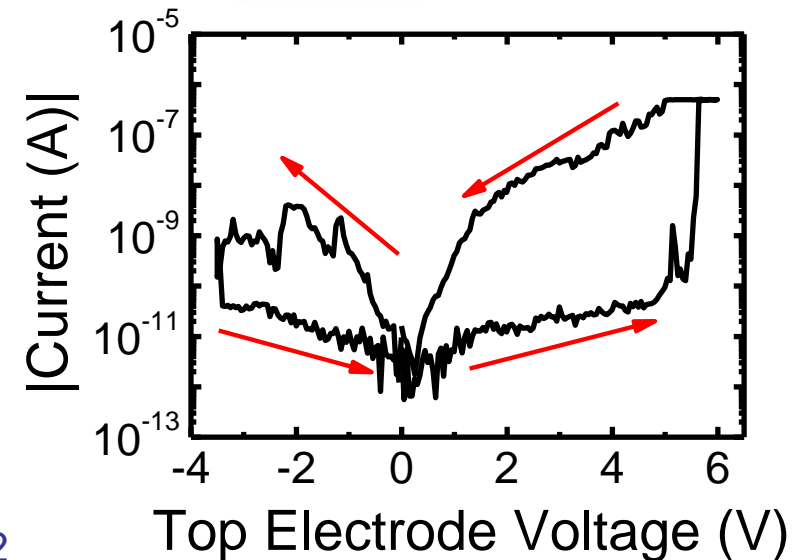
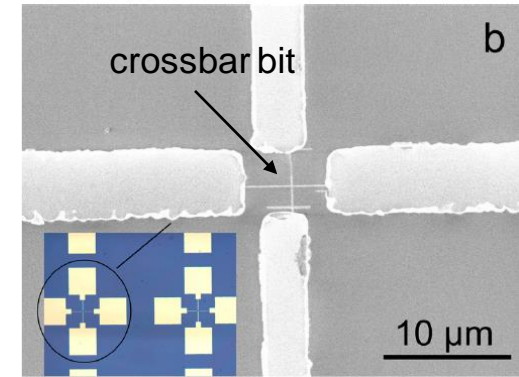
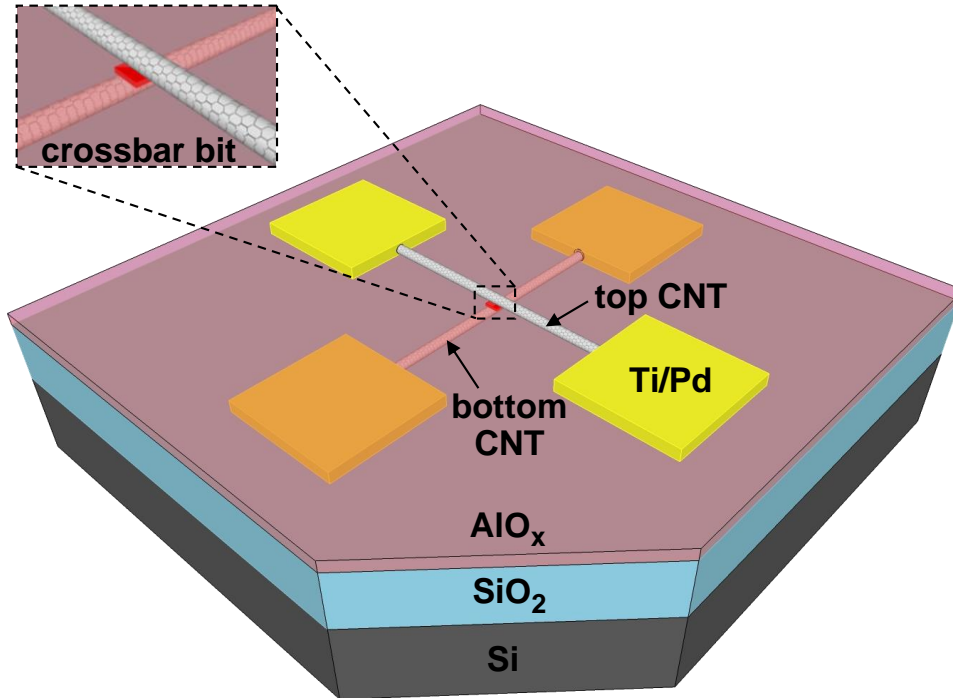


- 1T1R – 1 transistor and 1 RRAM cell
- Prevents sneak path
- Good density

Valov et al., Nanotechnology, 2011

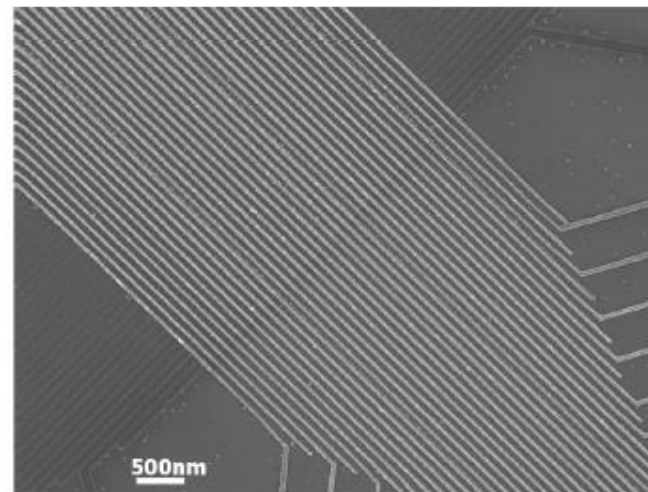
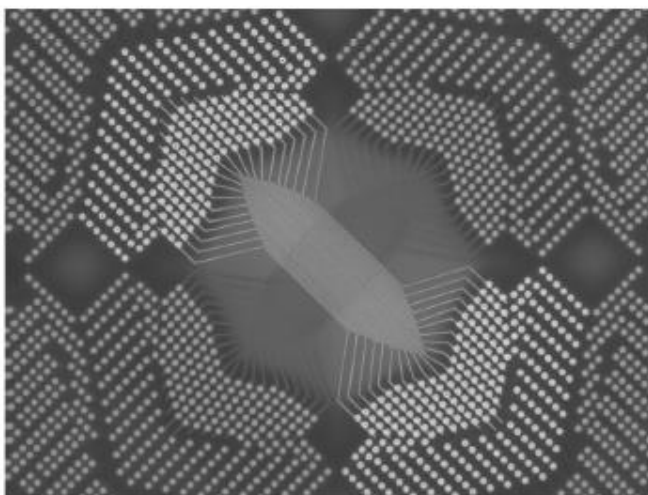
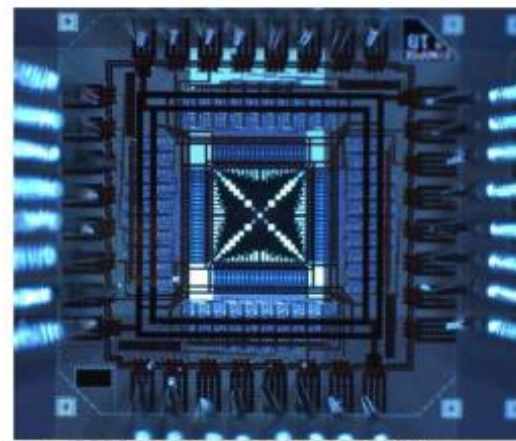
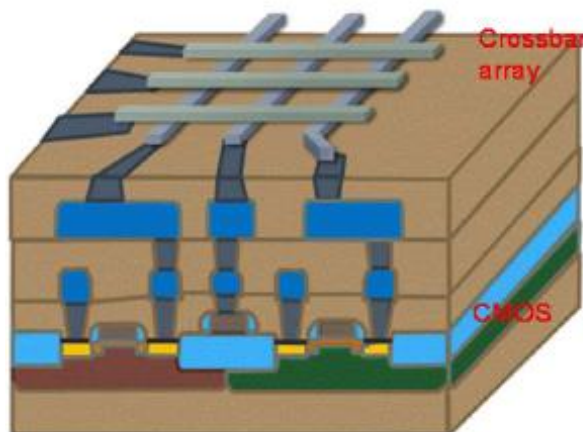
# CNT Crossbar Devices

C.-L. Tsai, F. Xiong, E. Pop, M. Shim, *ACS Nano* **7**, 5360-5366 (2013)



- CNT crossbar electrodes  $\sim 2 \text{ nm}^2$
- High performance and low power

# Crossbar Array from Crossbar Inc.



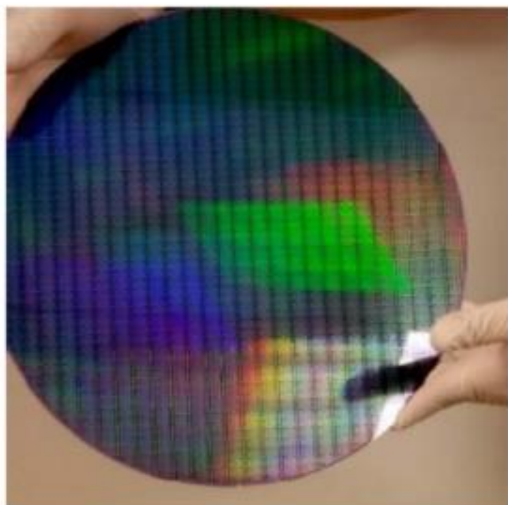
- RRAM crossbar array: 100 nm pitch
- 10 Gbits/cm<sup>2</sup>

Kim et al., Nano Lett., 2012

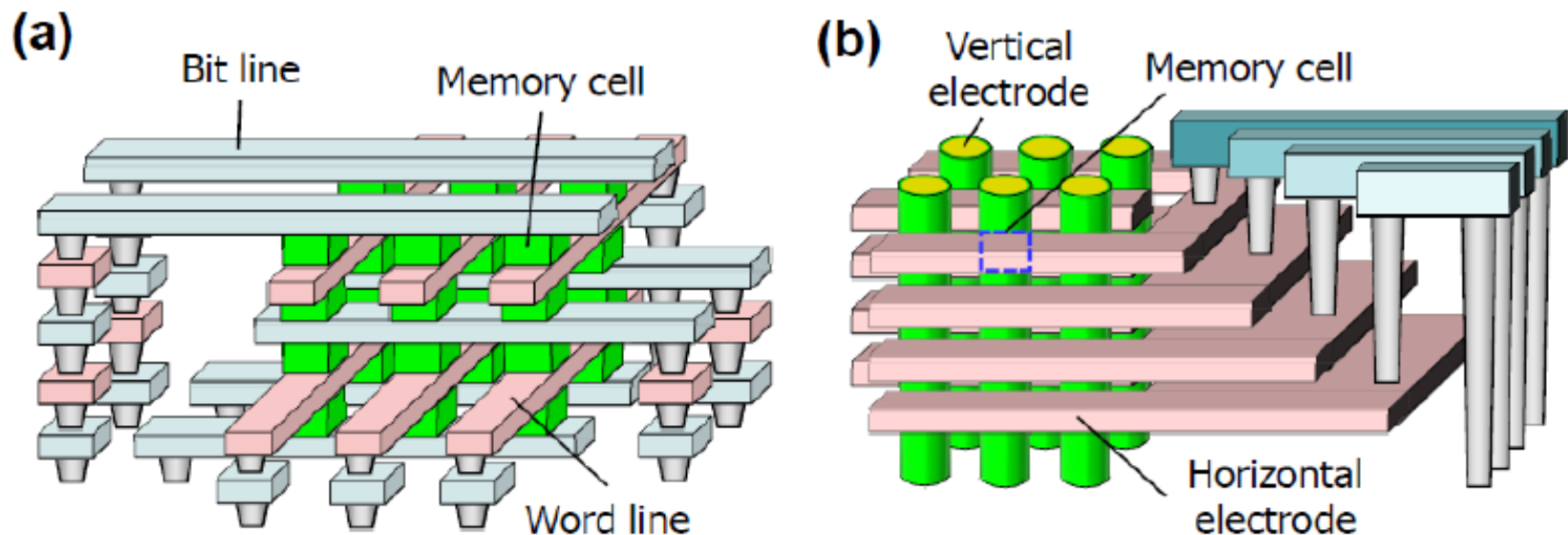


# Towards Commercialization

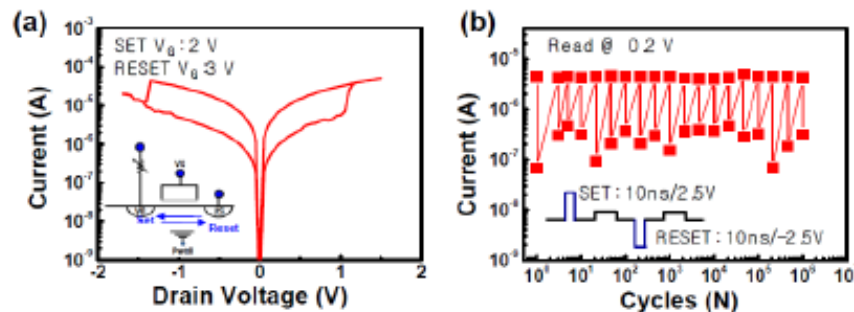
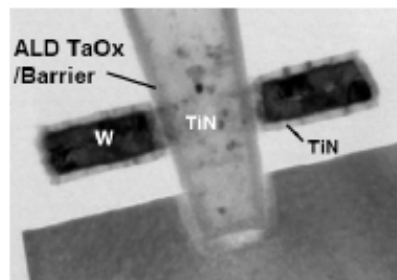
- Crossbar Inc. founded in 2010 with \$85 M funding so far
- Commercial products offered in 2016 with 40 nm CMOS
- CMOS compatible
- 3D stackable with low thermal budget process



# Samsung Vertical 3D



**Fig. 1** Schematic drawings of (a) 3D X-point ReRAM, (b) Vertical ReRAM

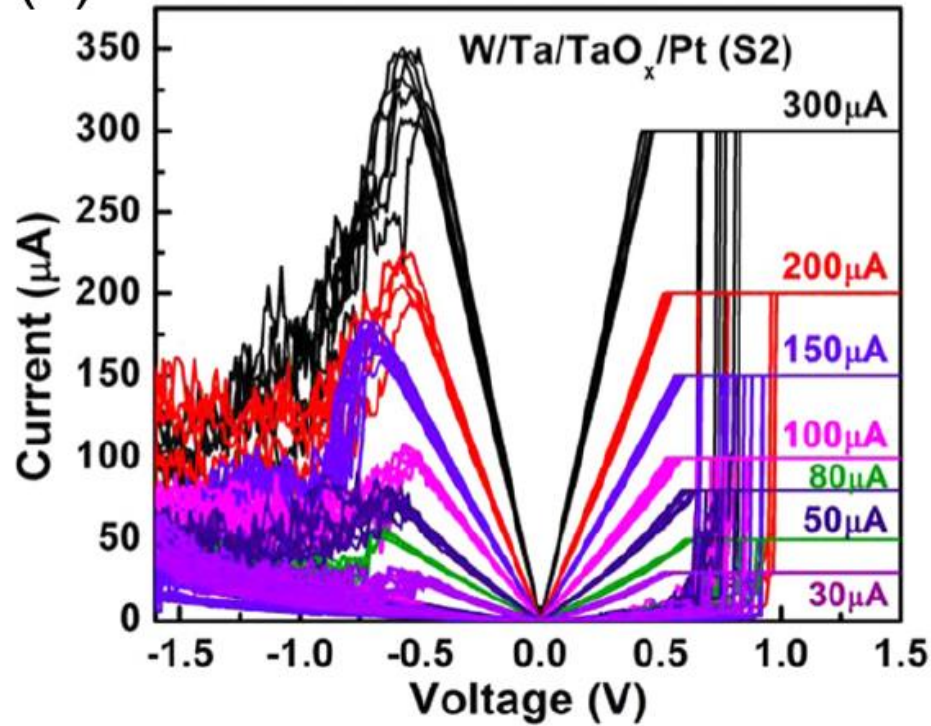


- Samsung claims vertical RRAM is more cost effective
- Prototype cell works with a vertical structure (TaOx-based)

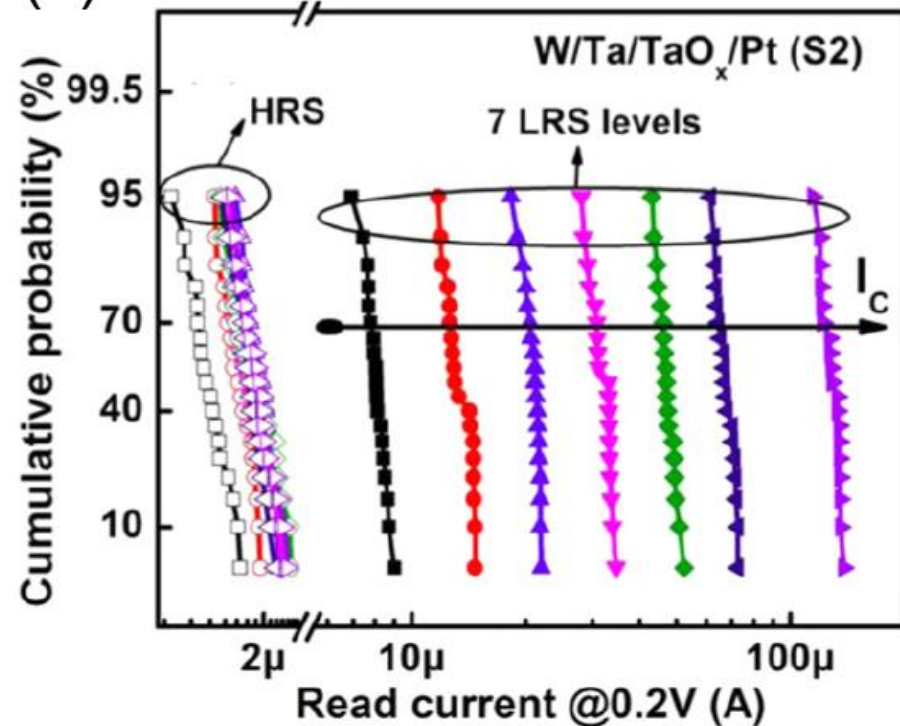
Baek, IEDM 2011, 31.8

# Multi-Level Cell

(a)



(b)

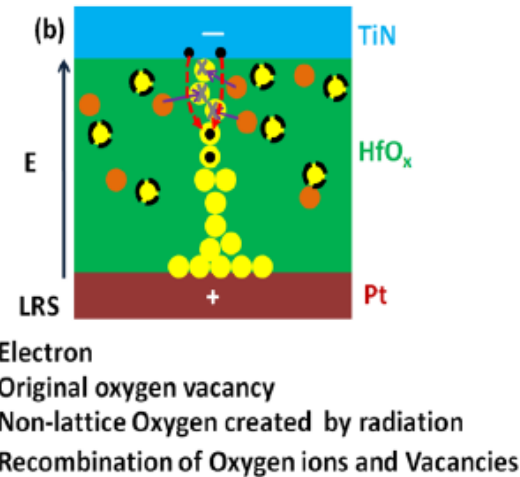
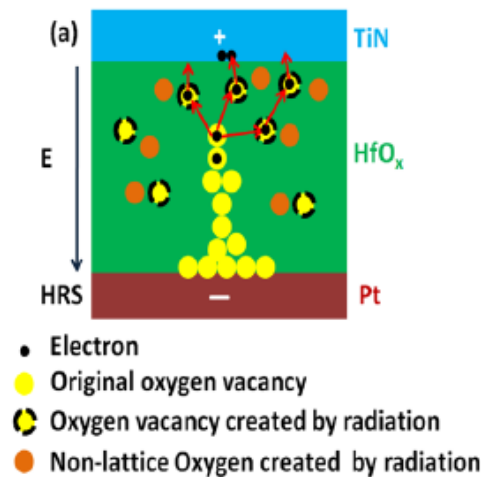
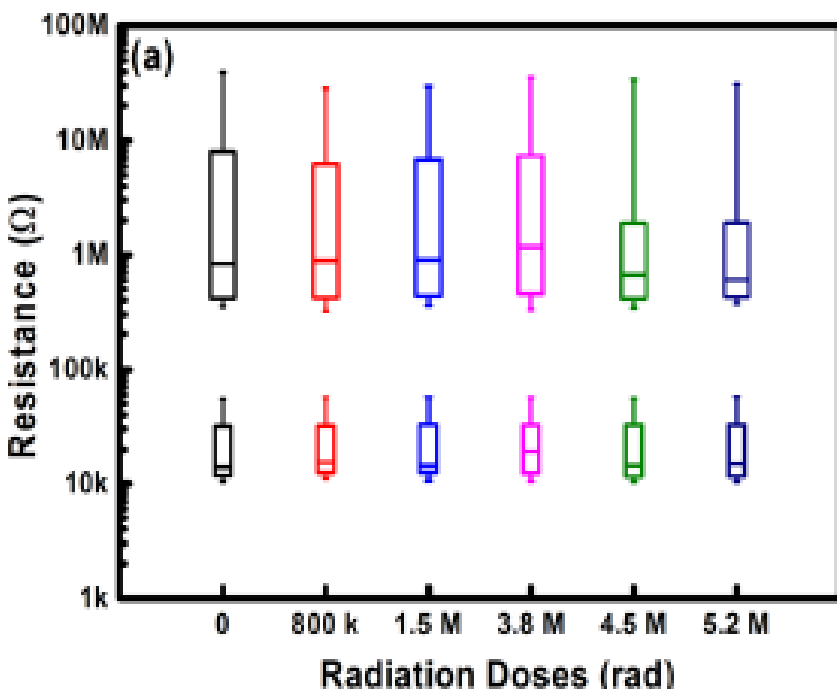


- Multi-level cell (MLC) → higher density
- 8 levels → 3 bit per cell
- Stochastic process makes uniformity more challenging



# Radiation Resistant

- RRAM is not charge-based (DRAM and flash)
- Radiation resistant → good for military and space applications
- HRS ( $\text{HfO}_x$ ) may decrease slightly upon radiation



Fang et al., APL, 2014