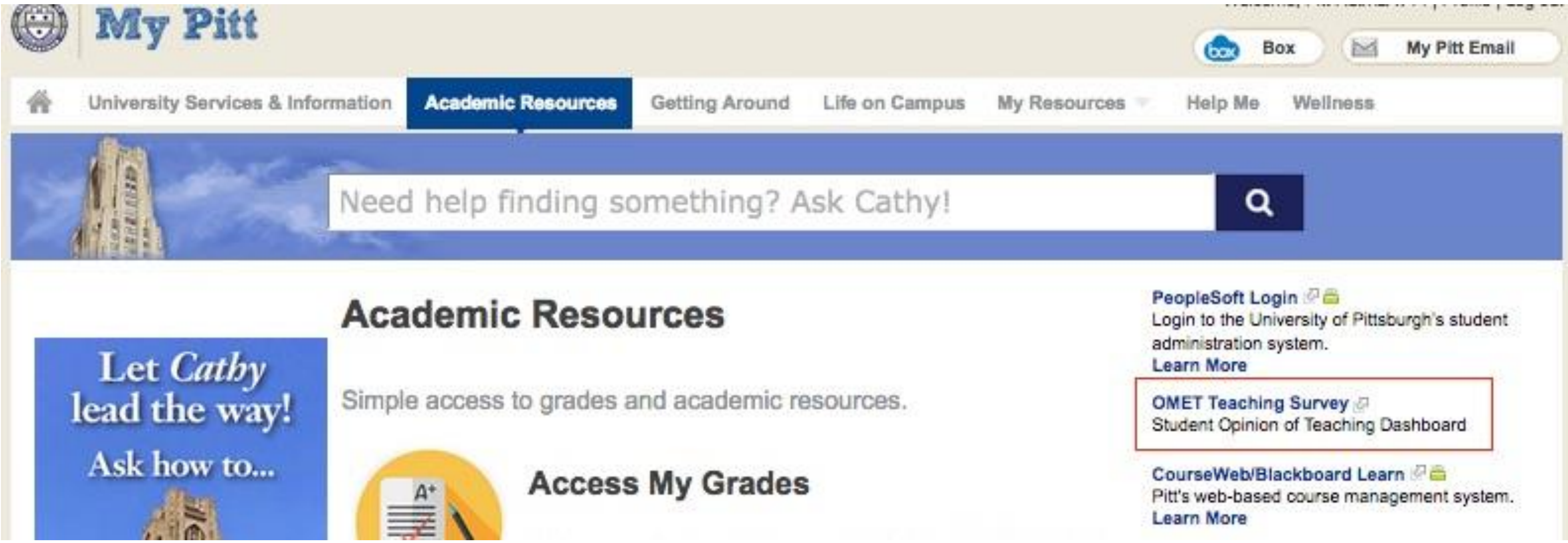
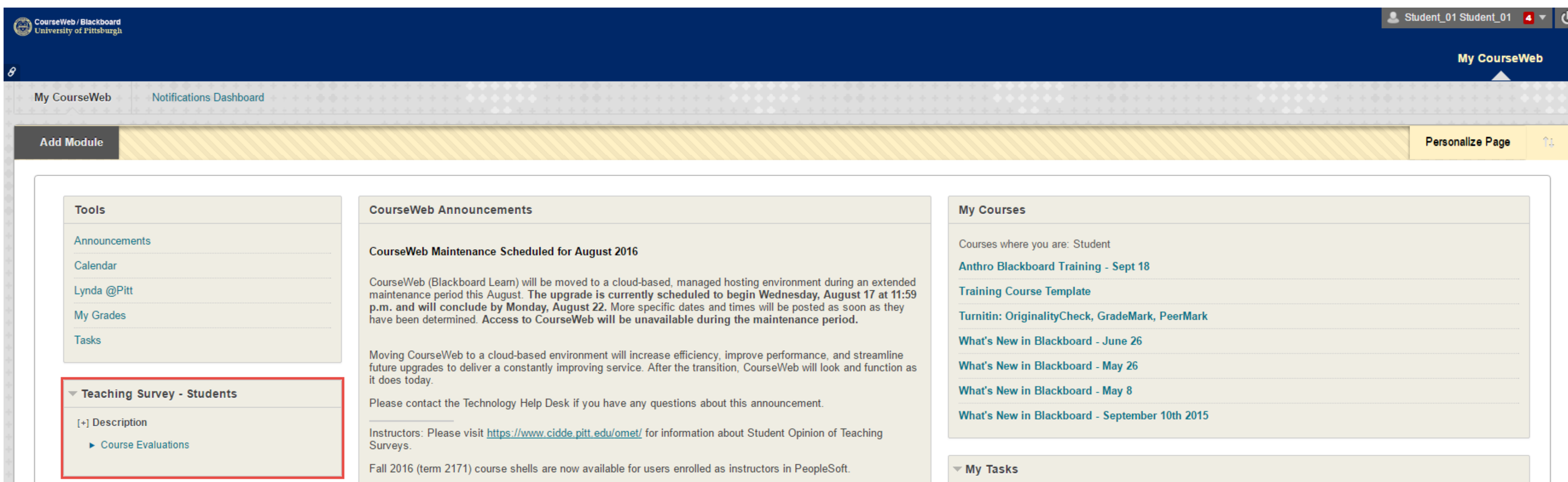
L9: Synaptic Electronics

Instructor: Prof. Feng Xiong

Teaching Survey





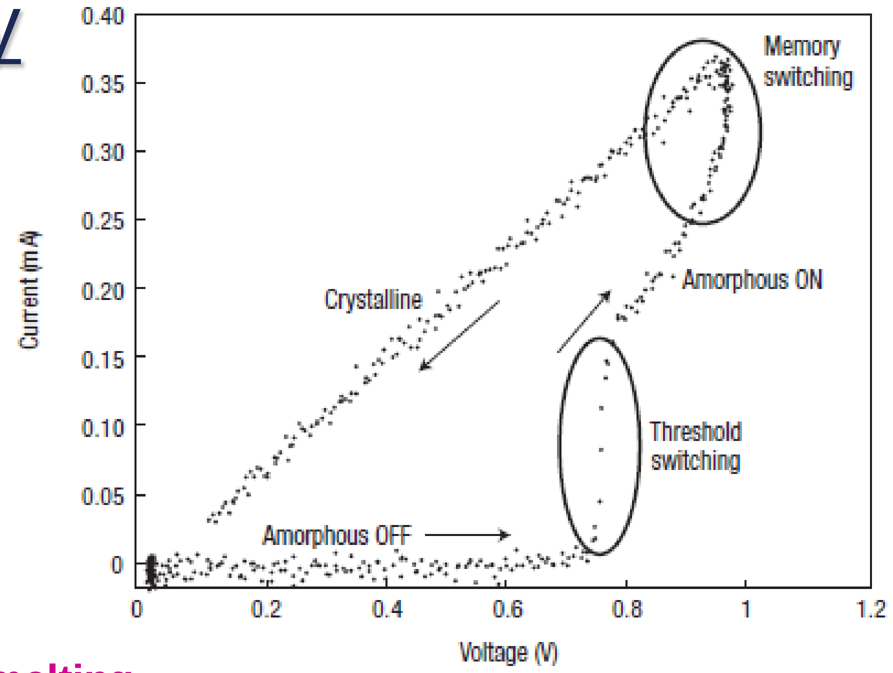
Outline

- PCM synapses
  - PCM for synaptic electronics
  - Pulse programming schemes
- RRAM synapses
  - Non-filamentary switching
  - Pros and cons
- Electrochemical synapses
  - Proton intercalation
  - Li intercalation

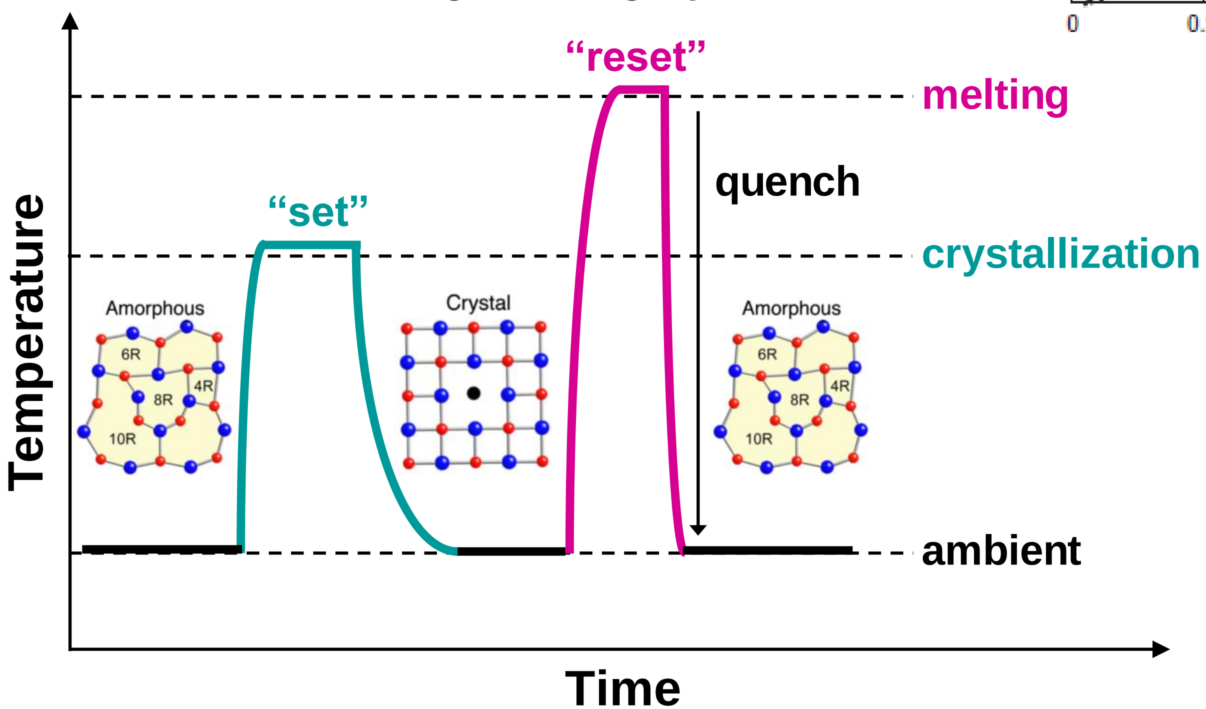
Synaptic Device Requirements

- Synaptic device = Memory?
- Similarities
  - data retention
  - Energy and speed
  - Reliability: variations, endurance, stability
  - scalability
- Differences
  - High-precision
  - High linearity and symmetry for DNNs
  - Temporal dynamics (both short-term and long-term) for SNNs

Phase Change Memory

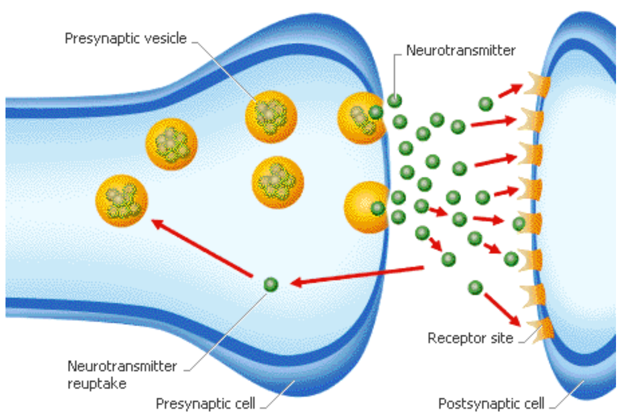


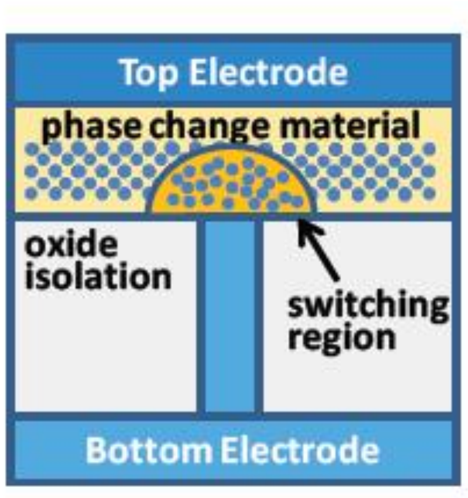
Programming Cycles



Why is PCM Suitable for Synaptic Electronics?

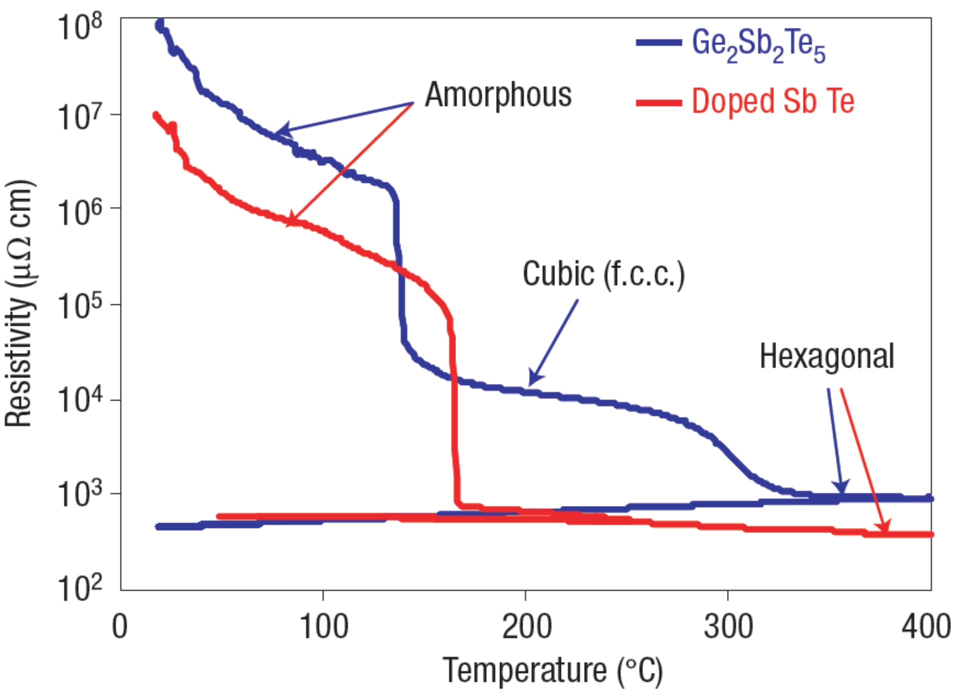
- Biological synapse
  - non-volatile
  - continuous
  - endurance ~ 10^{10}
  - energy < 50 fJ
  - speed ~1-100 ms
- PCM
  - non-volatile
  - analog
  - endurance ~ 10^{12}
  - energy < 1 pJ
  - speed ~1 ns

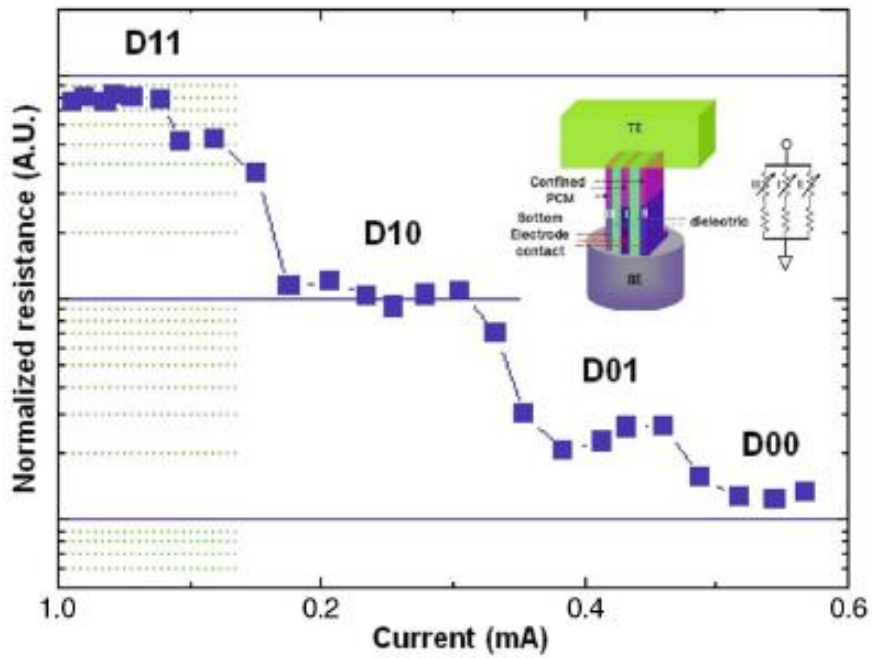




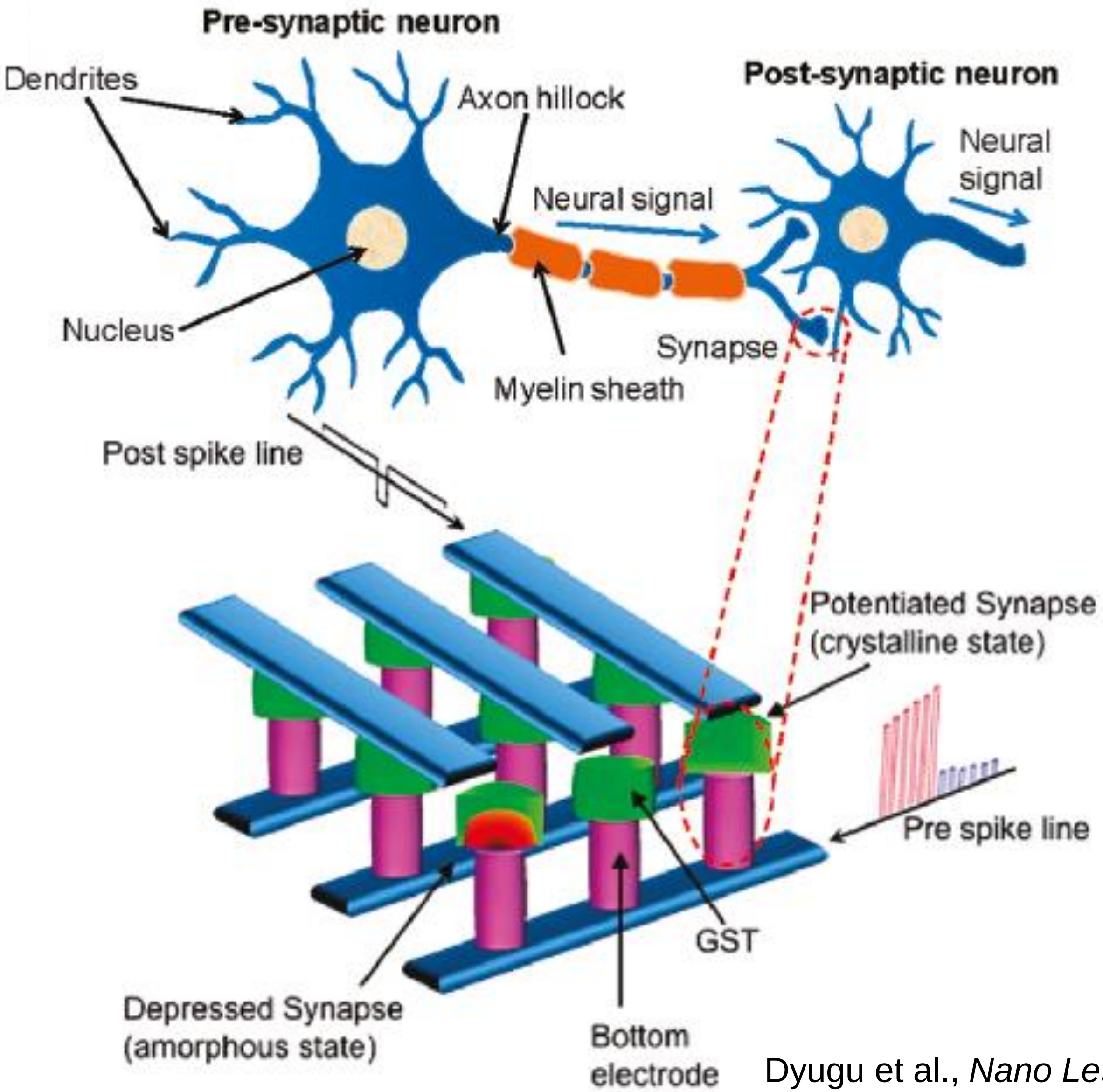
Analog Conductance

- Targeted synaptic electronics: 1% change per switching
- PCM: multi-level of resistances possible





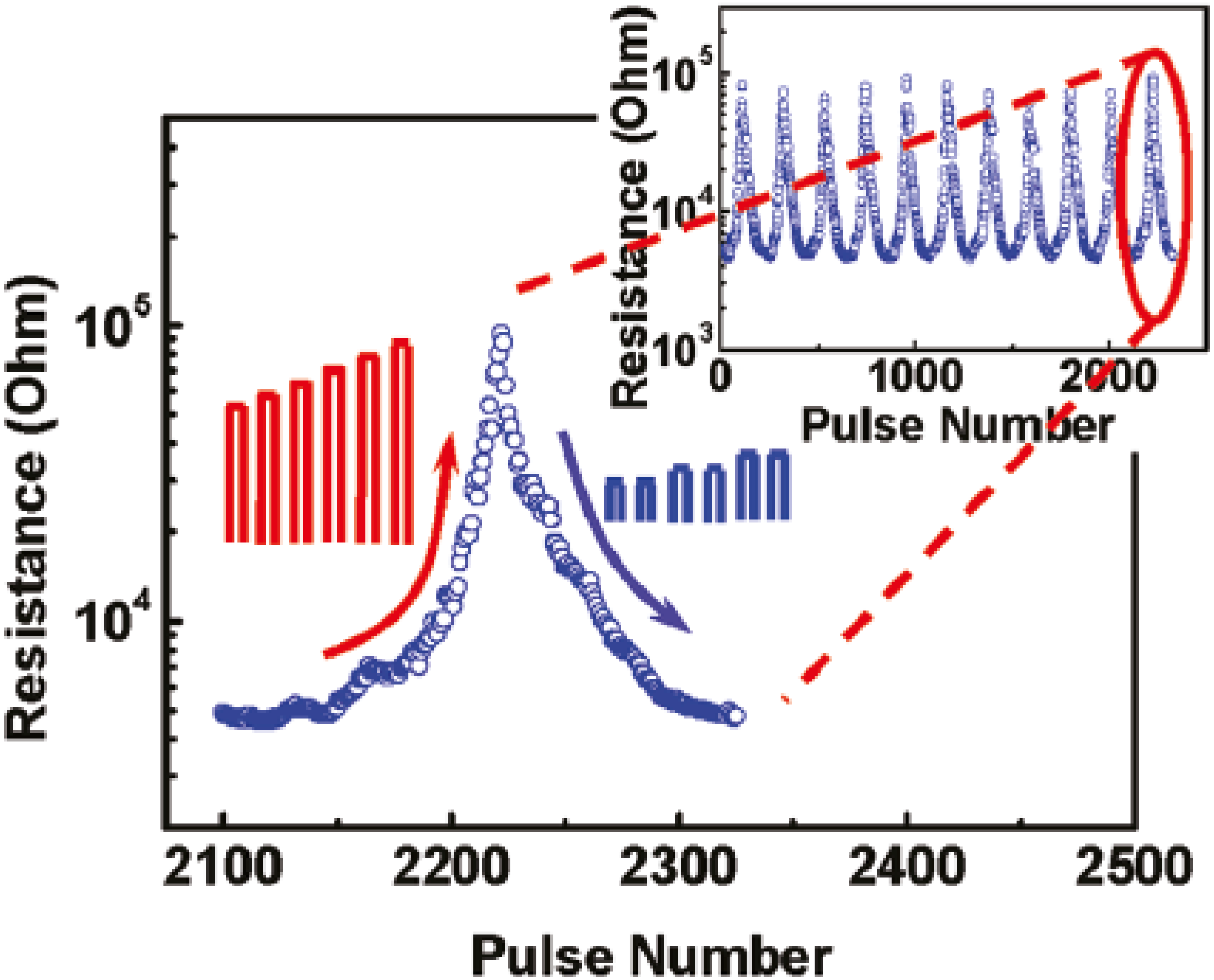
PCM as a Synapse



Dyugu et al., *Nano Lett.*, 2012

- PCM = Synapse
- Potentiation = Crystallization = SET
- Depression = Amorphization = RESET

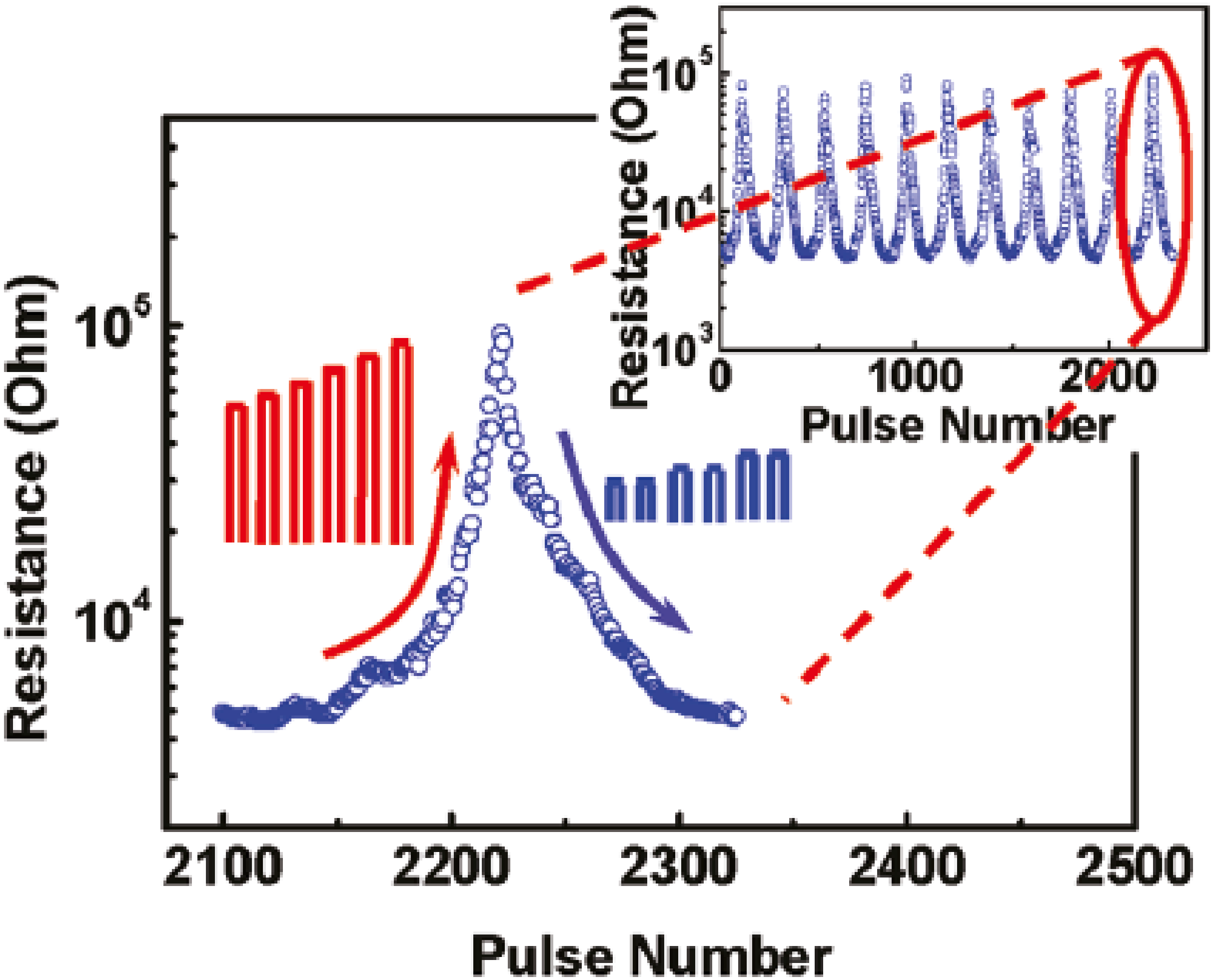
Potentiation/Crystallization (SET)



- SET = 100 total pulses → 20 pulses × 5 different amplitudes (0.5 to 1 V with 0.1 V step)
- Pulse width = 1 μs width and 500 ns rise/fall edge
- Gradual SET is possible with constant amplitude

Dyugu et al., *Nano Lett.*, 2012

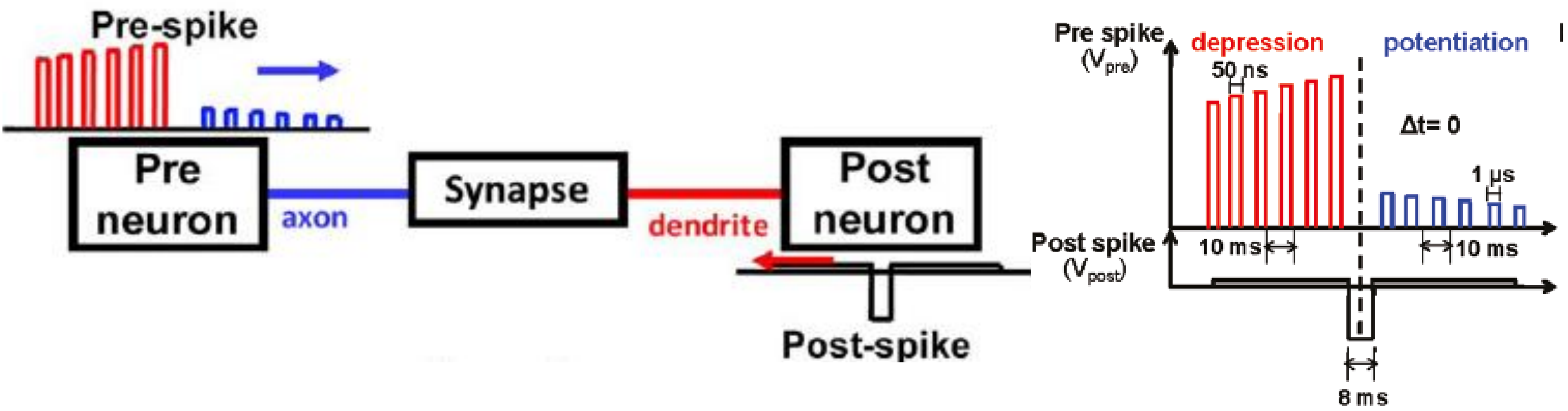
Depression/Amorphization (RESET)



- RESET = 100 total pulses → 2 to 4 V with 20 mV step
- Pulse width = 50 ns width and 25 ns rise/fall edge
- Intentionally slow fall edge for gradual R change
- Gradual RESET has to be with increasing amplitude

Dyugu et al., *Nano Lett.*, 2012

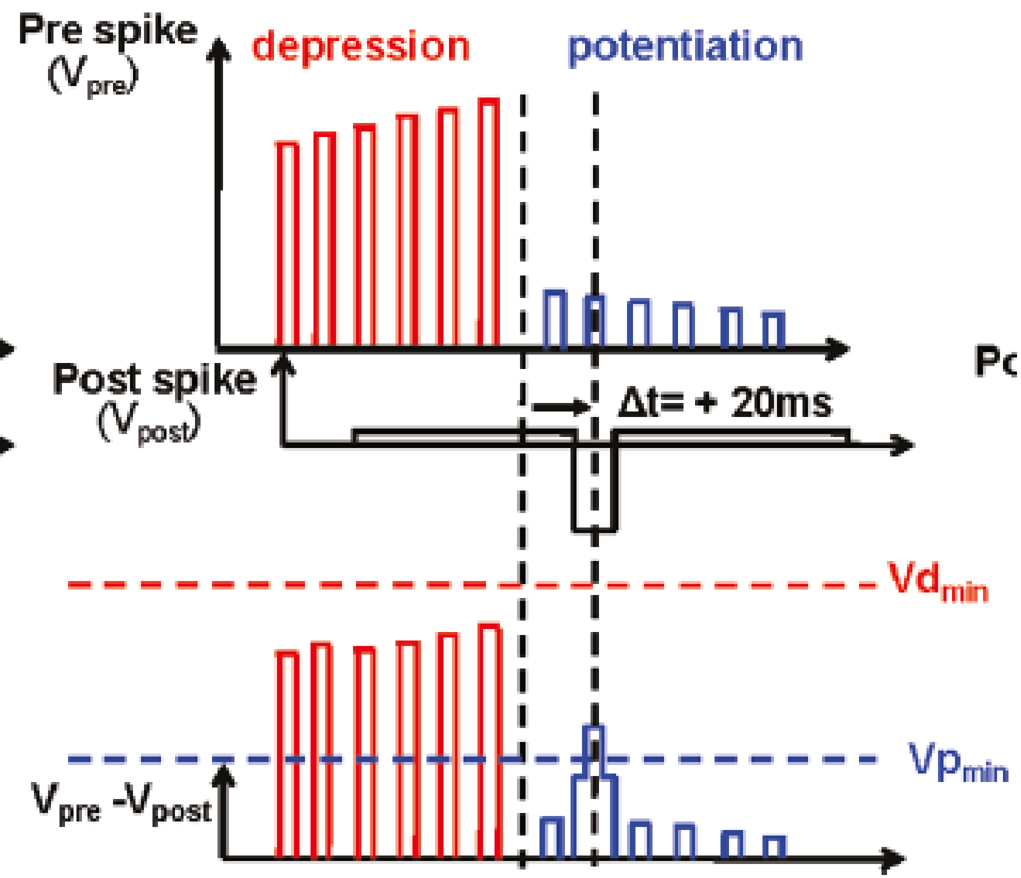
Pre-Spike and Post-Spike Pulses

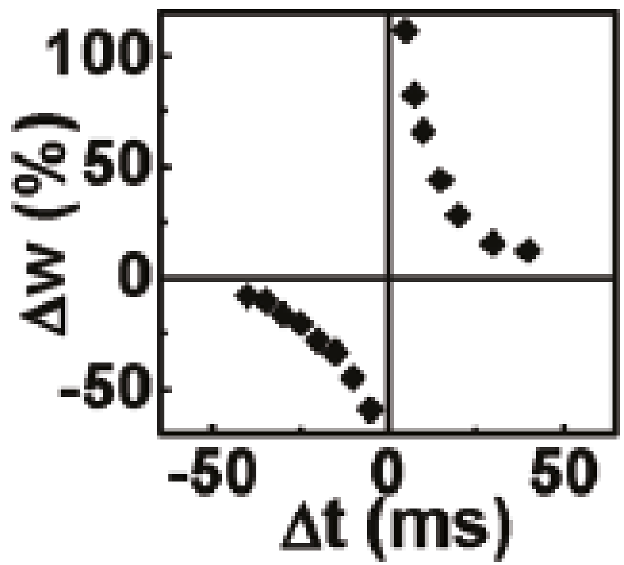


- Pre-spike signals = pulse trains with 10 ms interval
- Post-spike signal = single negative pulse for gating
- Post-spike pulse is 8 ms; could only overlap with one pulse

Dyugu et al., *Nano Lett.*, 2012

Asymmetric STDP

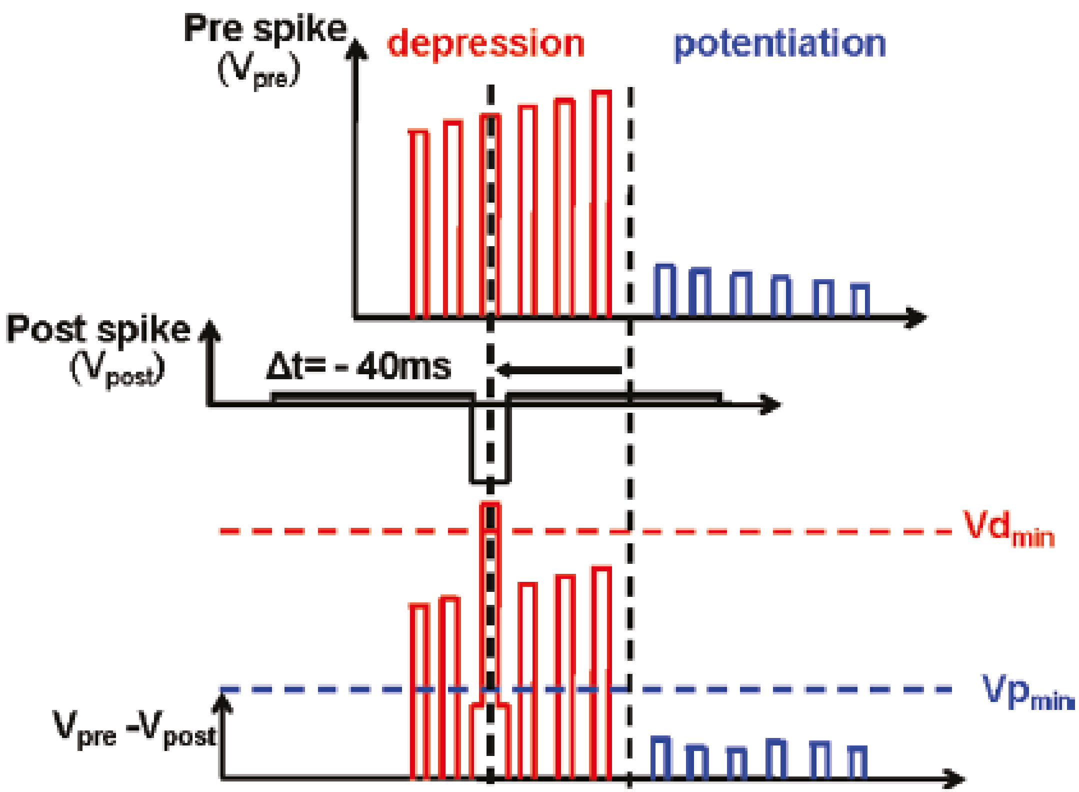


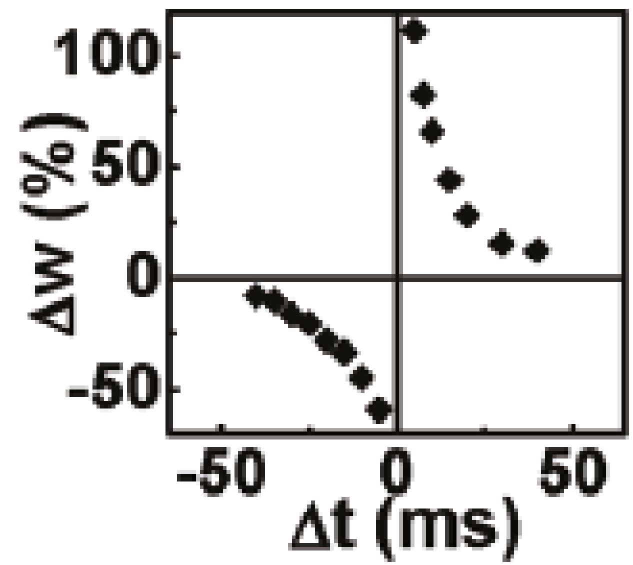


- Programming only happens when two overlaps
- Δw depends on timing → asymmetric STDP

Dyugu et al., *Nano Lett.*, 2012

Asymmetric STDP





- Programming only happens when two overlaps
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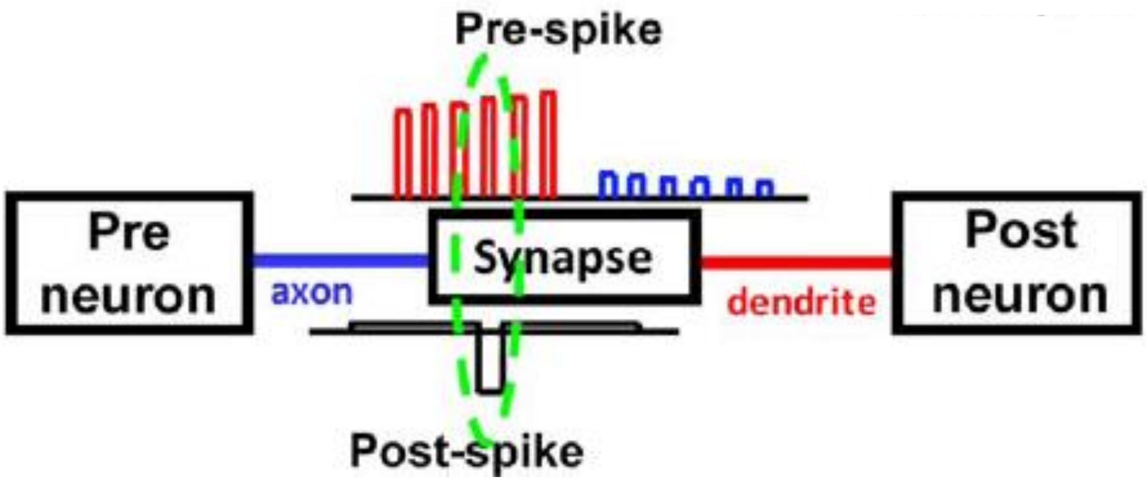
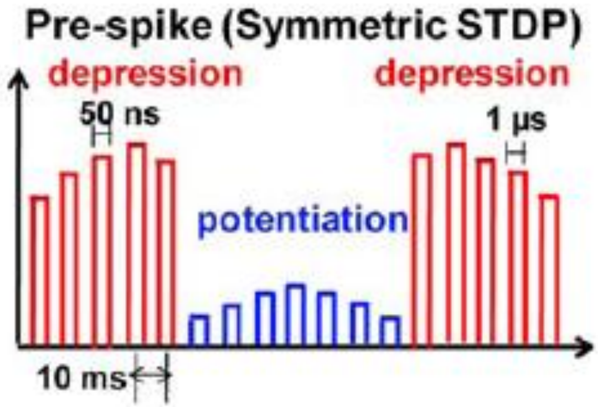
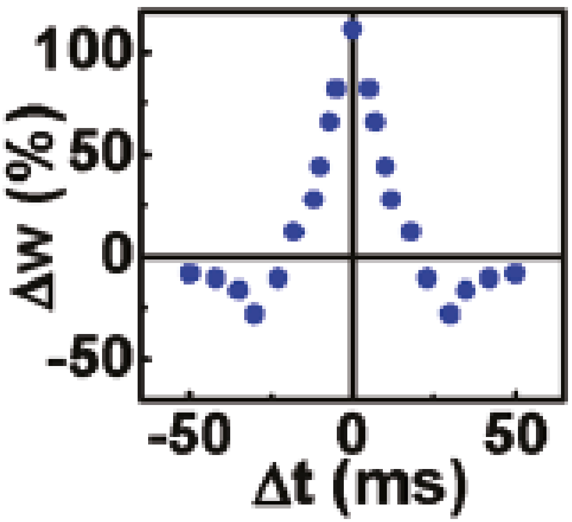
Dyugu et al., *Nano Lett.*, 2012

Symmetric STDP



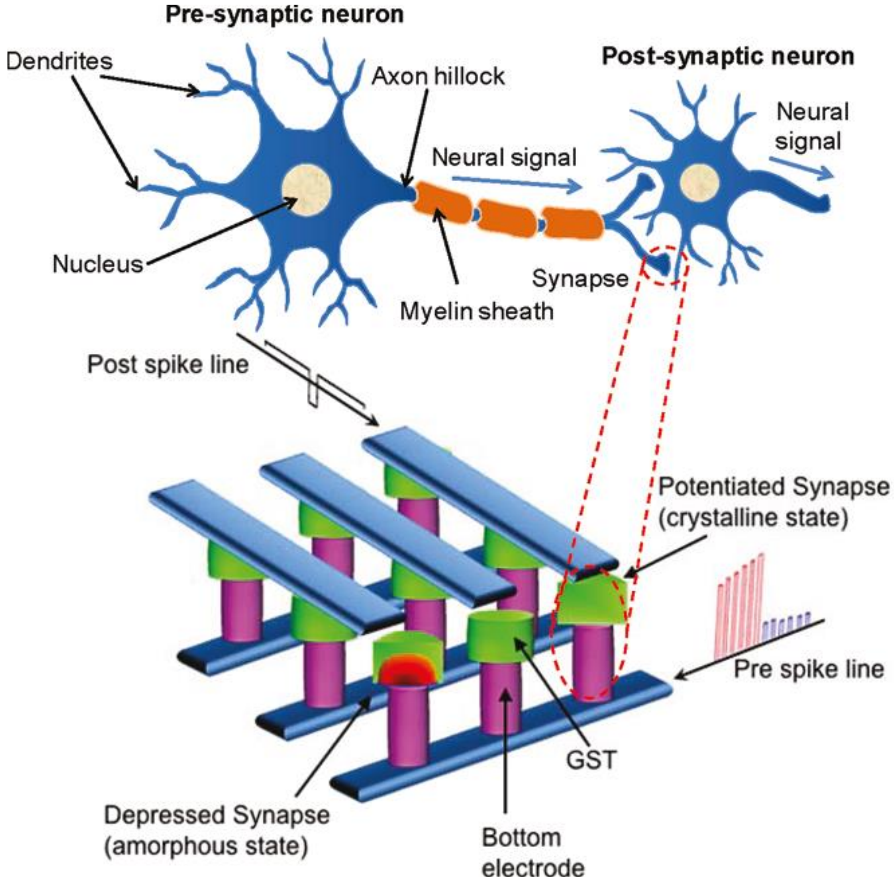


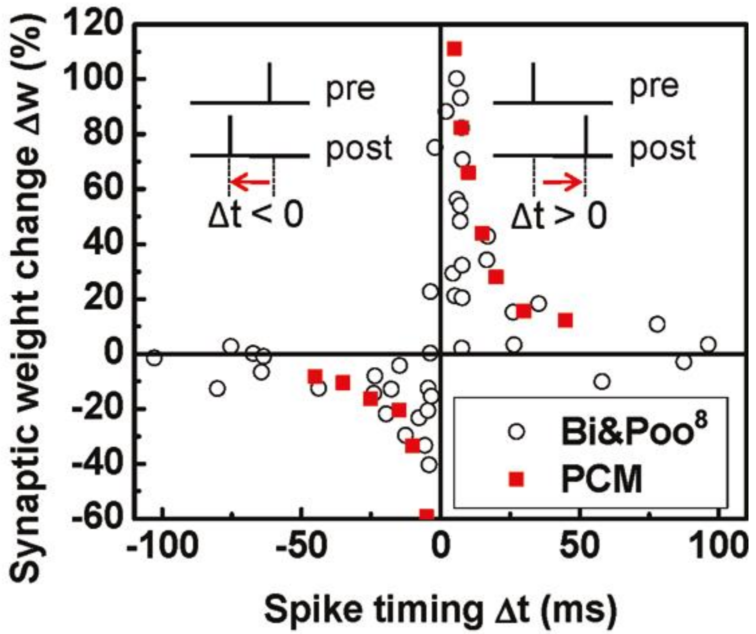


- Adjusting STDP with different schemes of pre-spike pulses
- Symmetric STDP

Dyugu et al., *Nano Lett.*, 2012

Drawbacks





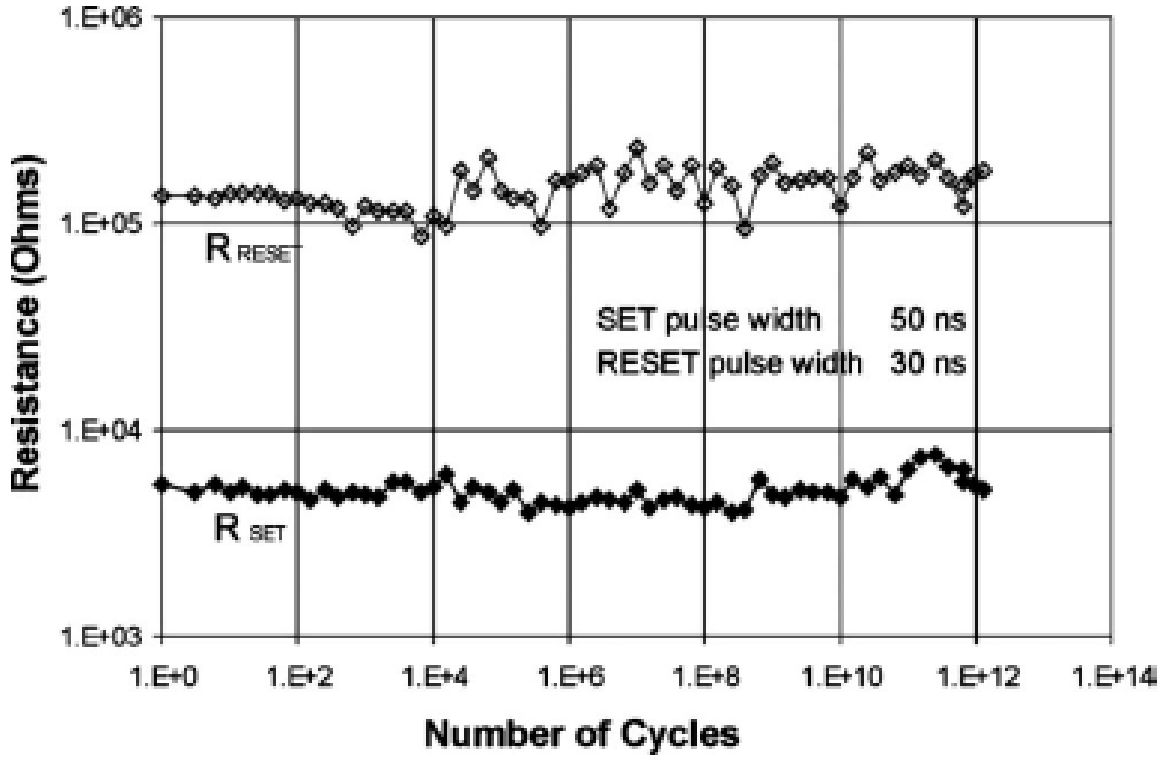
Dyugu et al., *Nano Lett.*, 2012

- Undesired programming and disturbance due to additional pulses
- Excess energy consumption

PCM Pulse Scheme

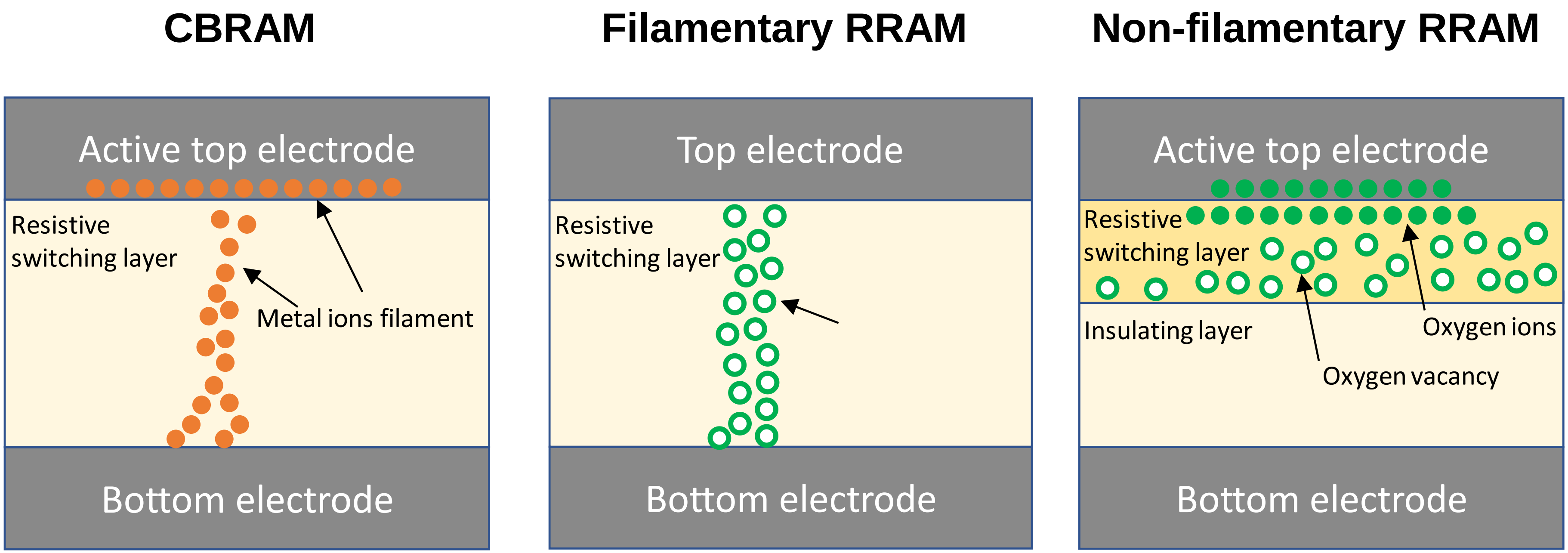
- Gating and response spike alone are not enough for programming
- Gating is used to ensure that only the intended synapse is programmed
- Possible to implement both
  - Asymmetric STDP: pre-neuron is reset and post-neuron is set
  - Symmetric STDP: quick response signal is set, slow is reset
- Disadvantage
  - computer-controlled pulse generator needs to be implemented

Challenges: Variability



- Intra-device and inter-device variability
- Implication: less accurate, longer training time, consumes more energy

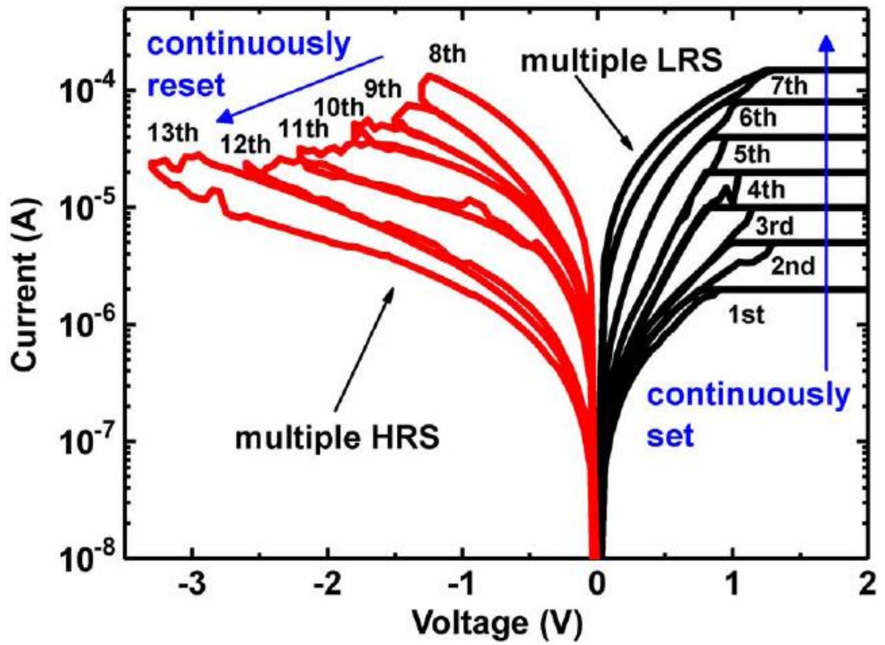
RRAM Synapses



- Synaptic devices prefers analog switching behaviors
- Non-filamentary devices show more analog switching

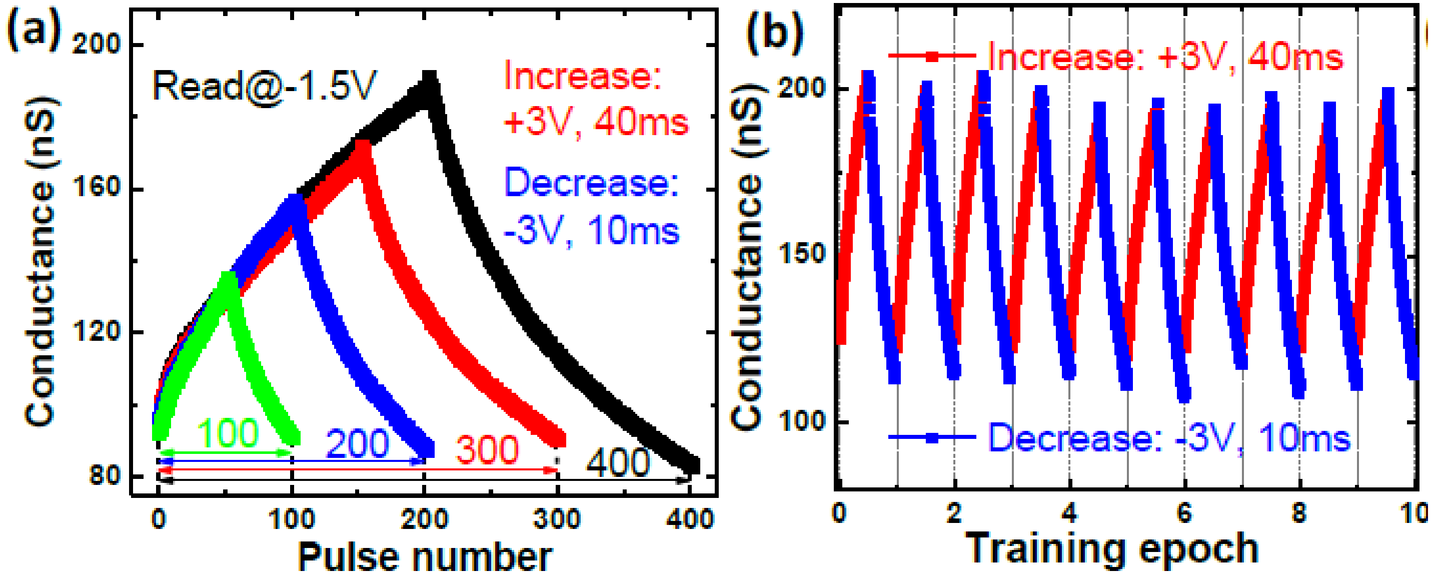
RRAM for Synaptic Electronics

- Advantages
  - non-volatile
  - analog with large on/off ratio
  - endurance ~ 10^8
  - energy < 1 fJ
  - speed ~1 ns
  - two-terminal



- Disadvantages
  - Large device variations
  - non-linear IV, especially abrupt tuning
  - limited precision
  - the need for a forming step
  - No built-in temporal component

Non-Filamentary Switching



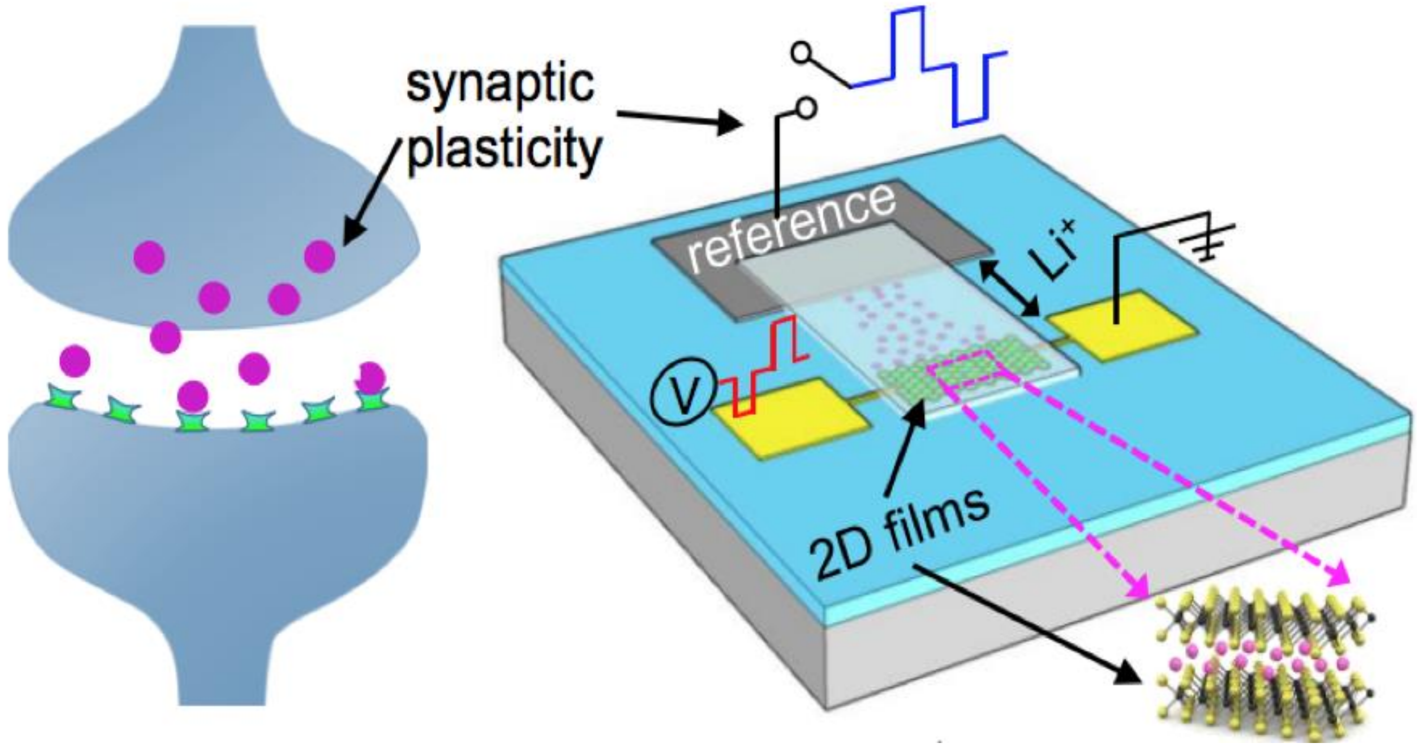
- Higher precision → high density
- More linear and symmetrical → better for online training

2D Electrochemical Graphene Synapse

Bio-Synapse

2D Gr-Synapse

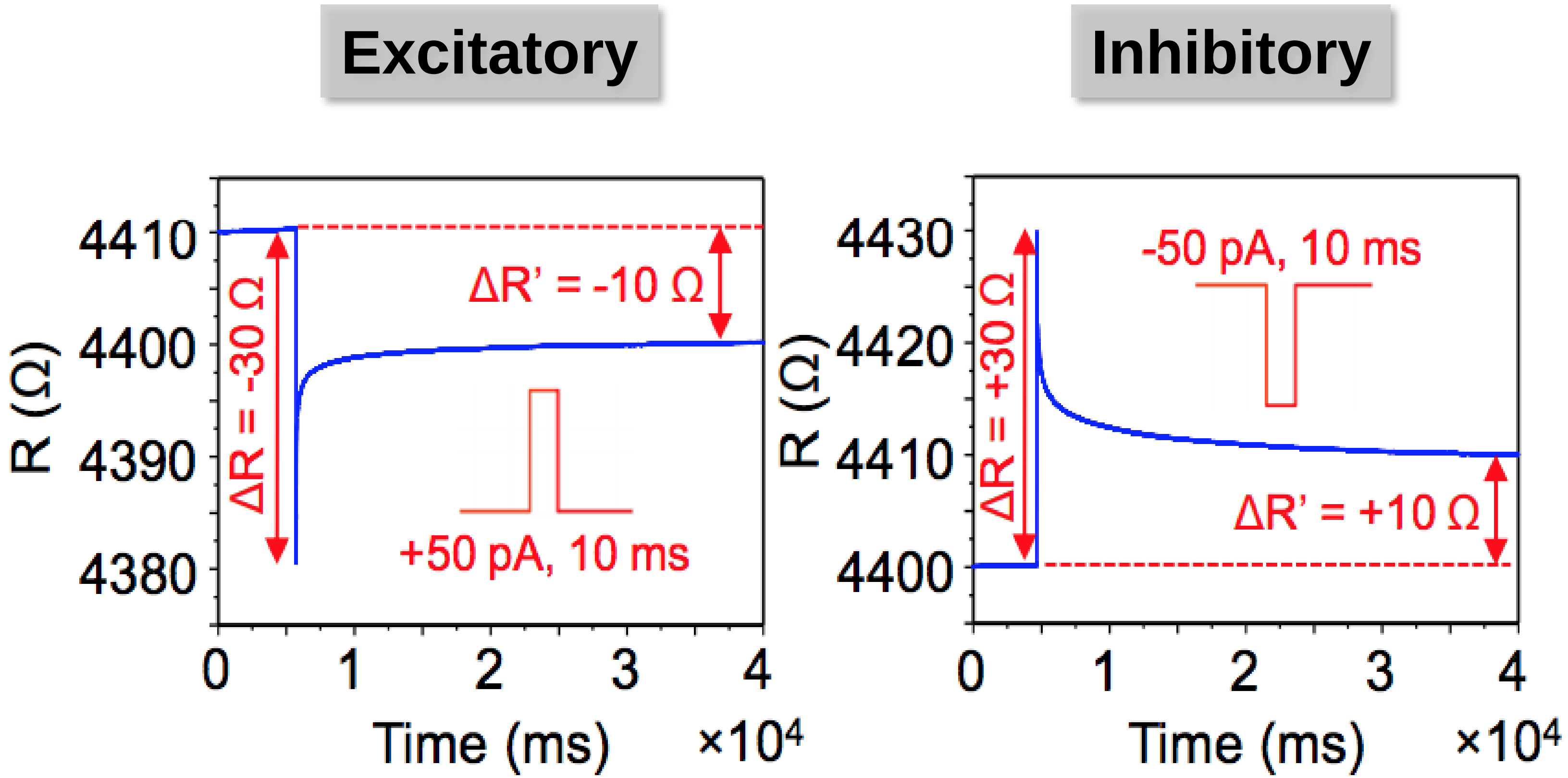
M. Sharbati, ..., F. Xiong, *Adv. Mater.*, 2018



- Synaptic weight = graphene conductance
- Synaptic plasticity = electrochemical intercalation

Excitatory and Inhibitory Synapses

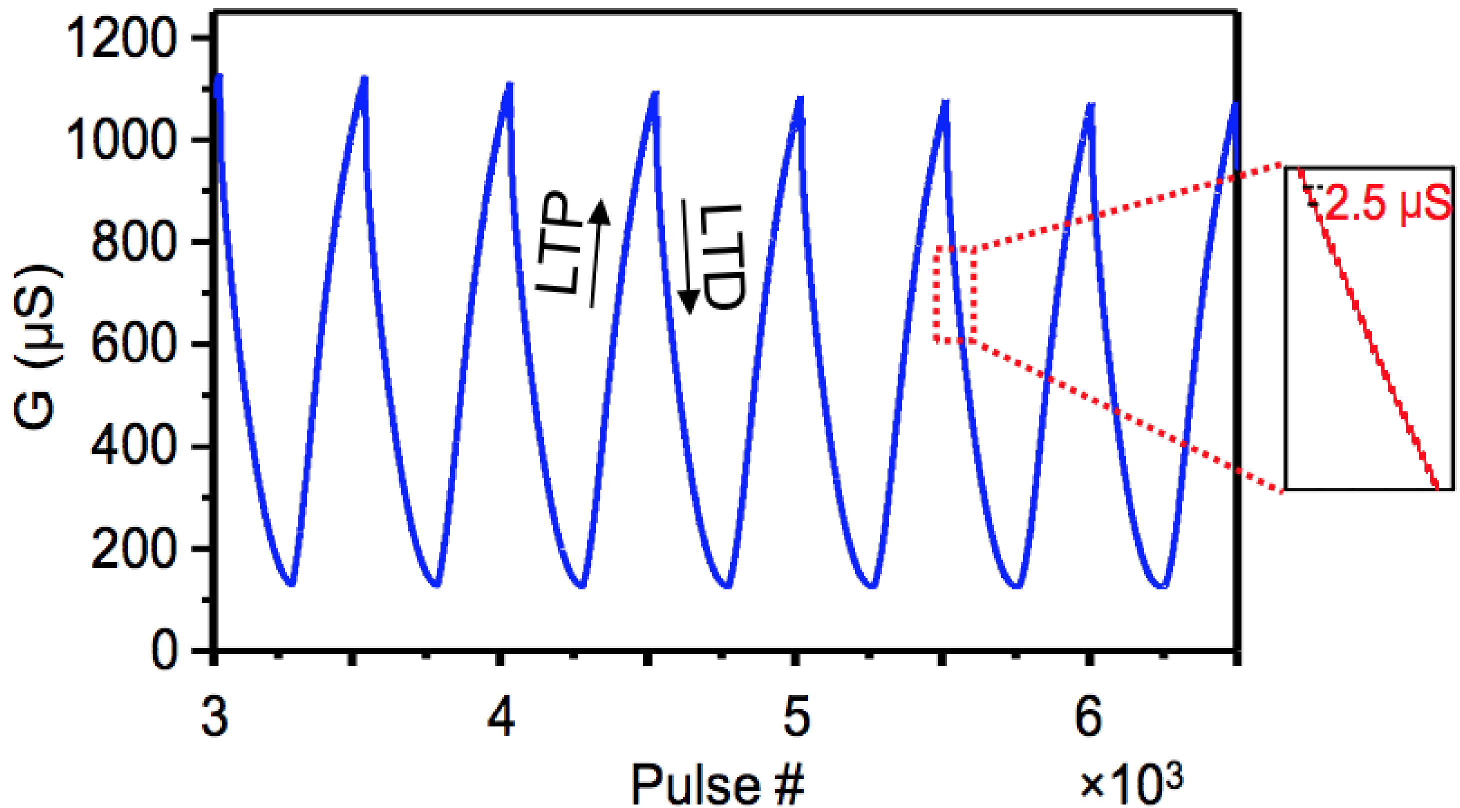
M. Sharbati, ..., F. Xiong, *Adv. Mater.*, 2018



- Li doping: non-volatile effect
- Electric double layer (EDL) gating effect: transient change

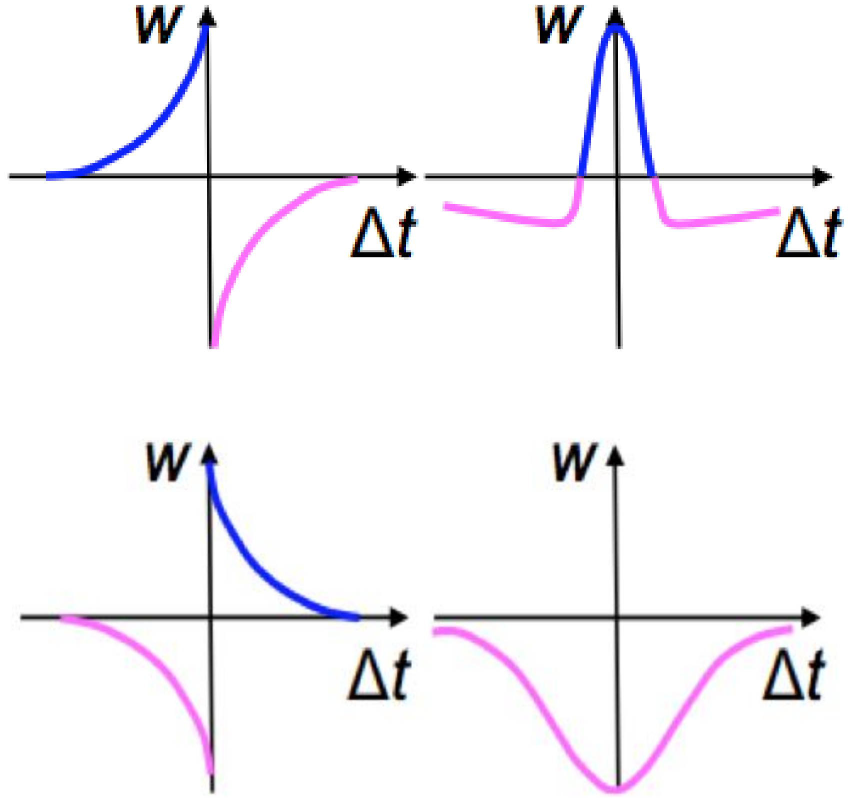
Linear and Symmetric Response

M. Sharbati, ..., F. Xiong, *Adv. Mater.*, 2018



- Long term potentiation (LTP) and depression (LTD)
- Highly linear, symmetric, and reproducible
- > 400 states, i.e. $\Delta G/G < 0.25\%$

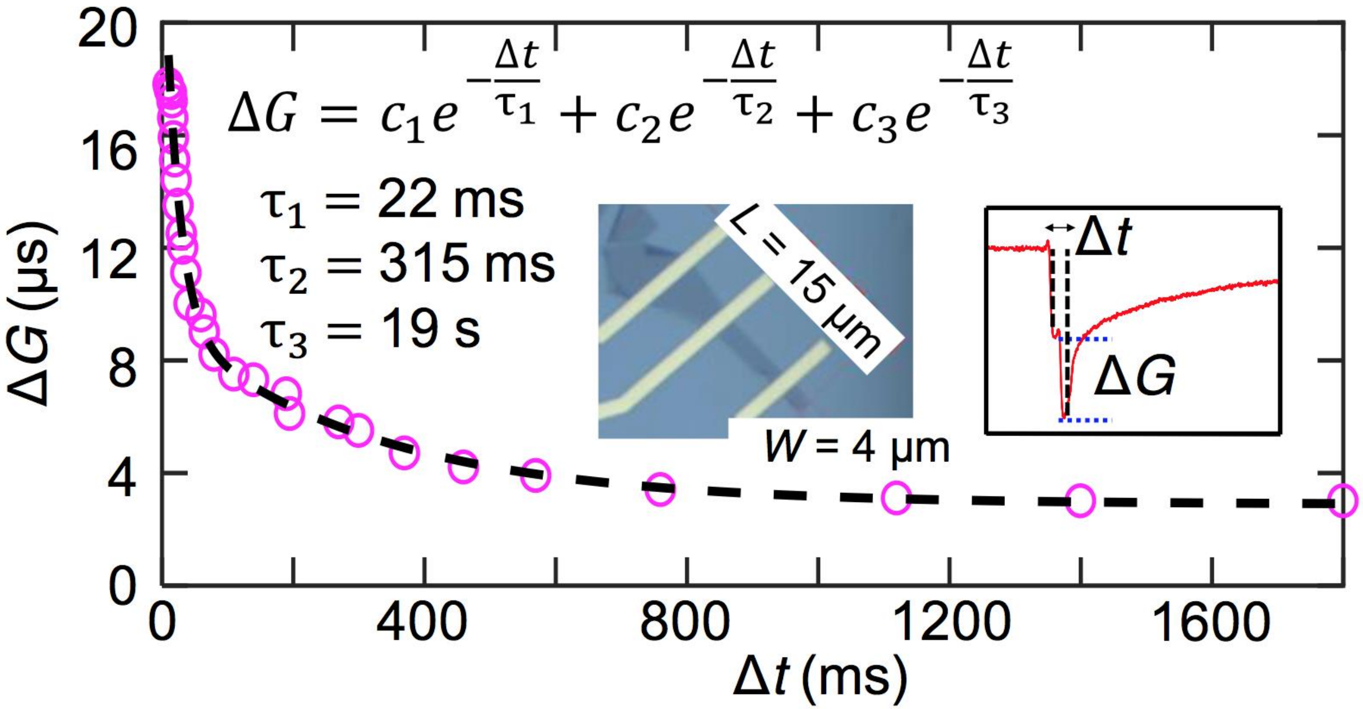
Spike Timing Dependent Plasticity (STDP)



Different forms of STDP in biological synapses

Programmable STDP

M. Sharbati, ..., F. Xiong, *Adv. Mater.*, 2018



$$\tau_D \approx L^2/_{2D}$$

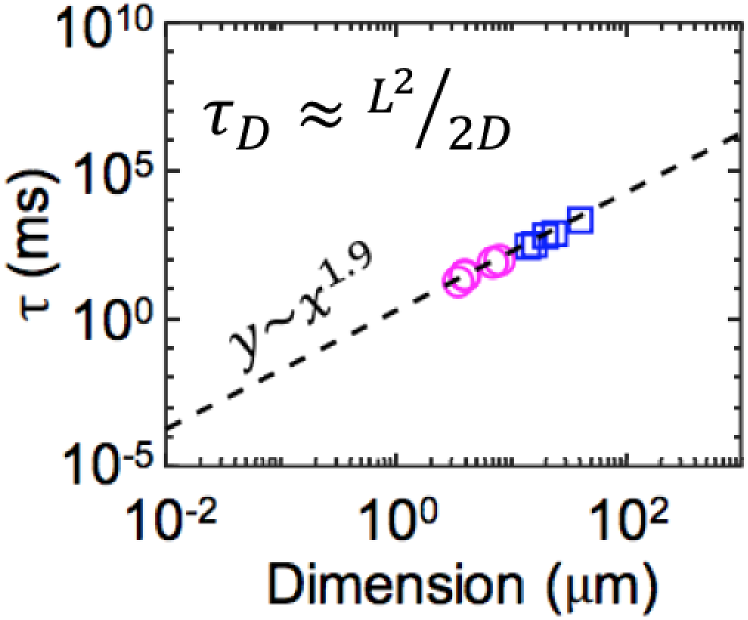
$$\frac{\tau_2}{\tau_1} = 14.5$$

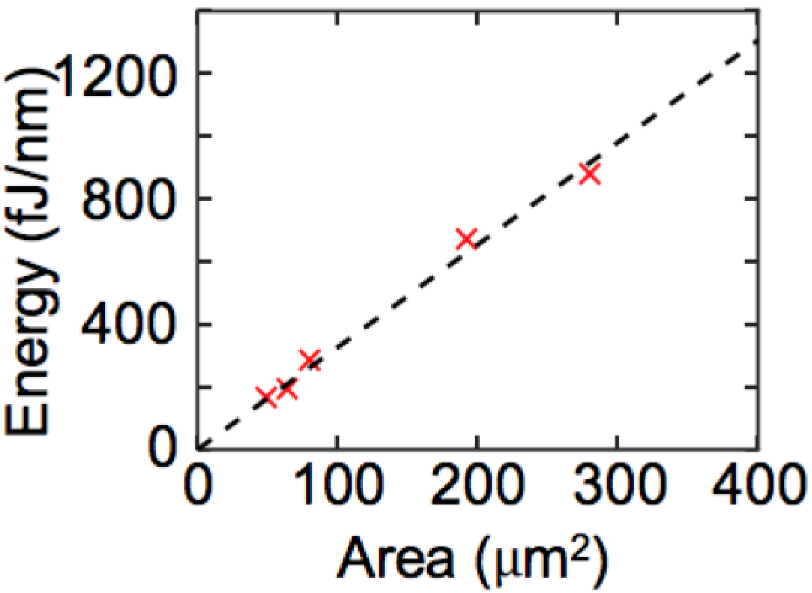
$$(\frac{L}{W})^2 = 14.1$$

- Assume D_{coeff} ~ 4×10^{-6} cm^2/s
  $\rightarrow \tau_1\sim$ 20 ms, $\tau_2\sim$ 280 ms in W and L direction
- τ_3 may rise from diffusion between LFP to Gr
- engineering time constants

Scaling Analysis

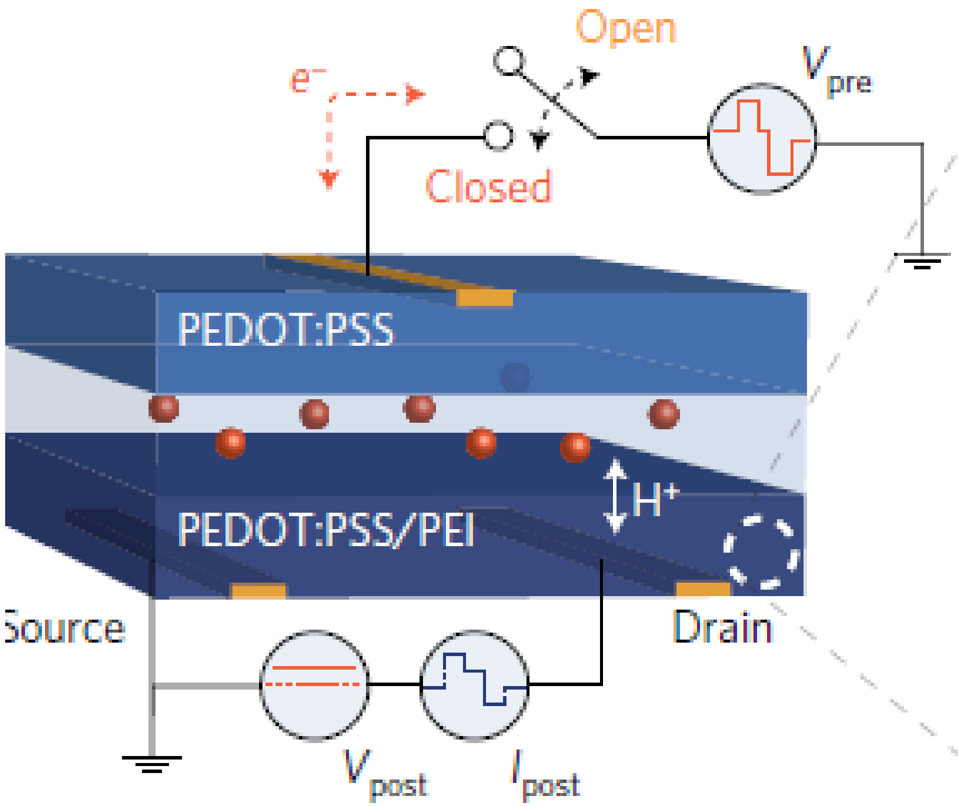
M. Sharbati, ..., F. Xiong, *Adv. Mater.*, 2018





- Scalable in terms of energy and time
- For 30 nm x 30 nm: 100 ns and 5 aJ switching

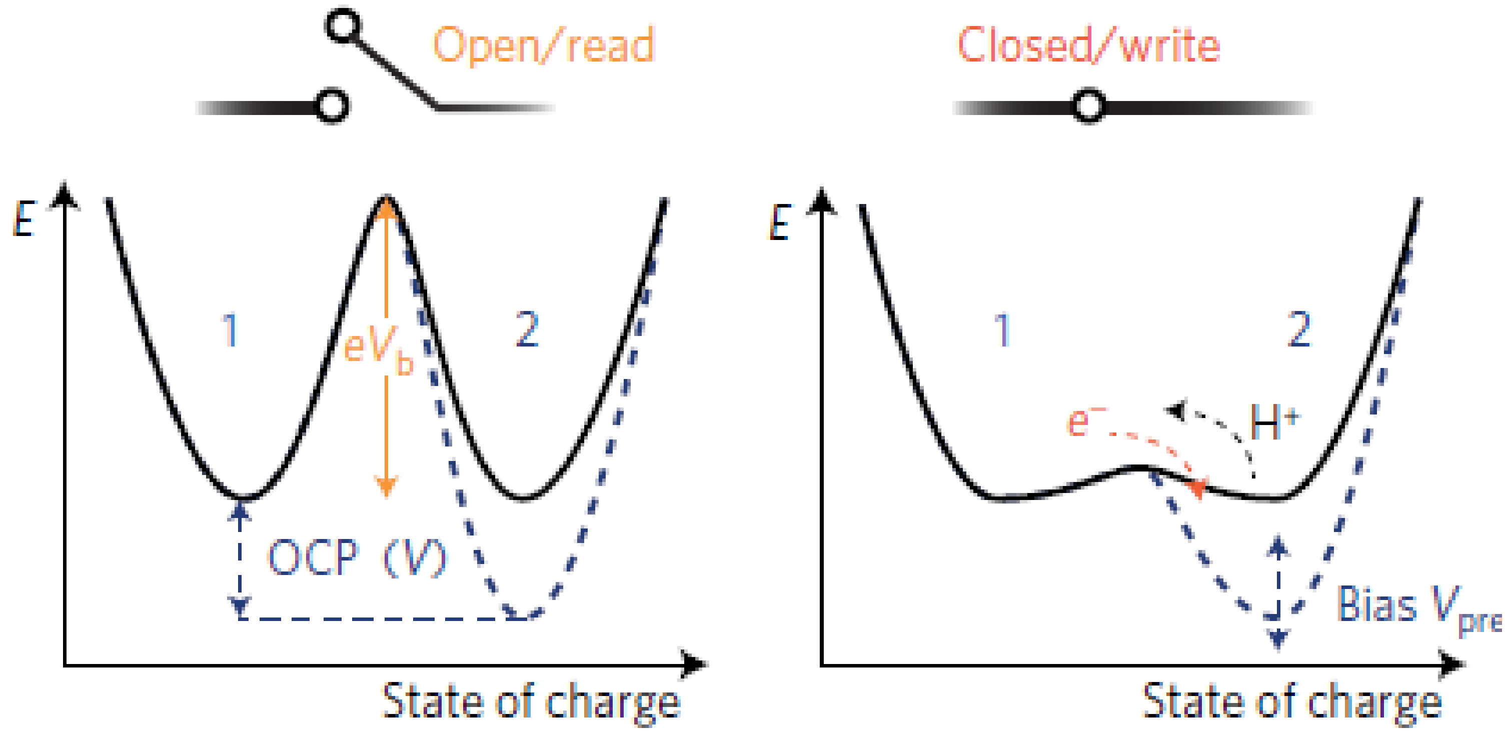
Redox Synapse



- Synapse weight is channel conductance
- Programming through electrochemical reaction – adding H+ ions into the conduction channel

Burgt *et al.*, *Nat. Mater*, 2017

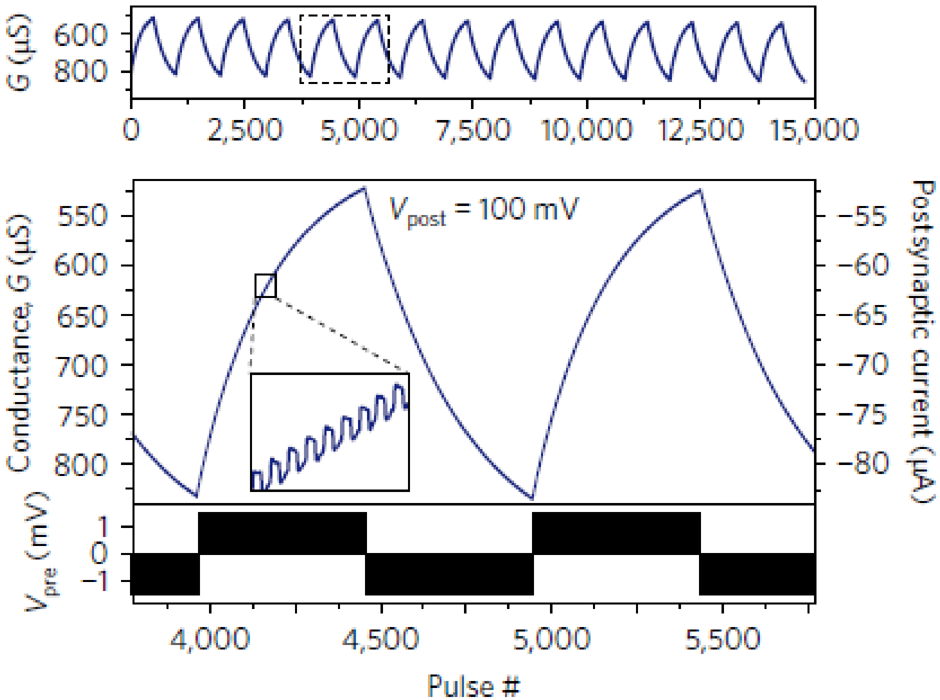
Retention and Power Consumption

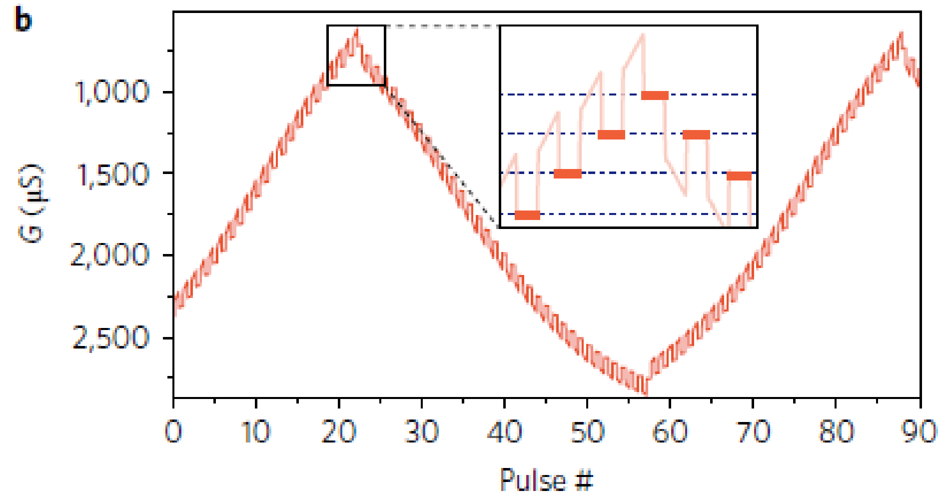


- Typically, retention and power consumption are coupled
- Better retention → large barrier → high power
- Here: retention (electrochemical reaction) and programming (conduction) are de-coupled
- Good retention AND low power

Burgt *et al.*, *Nat. Mater*, 2017

LTP and LTD

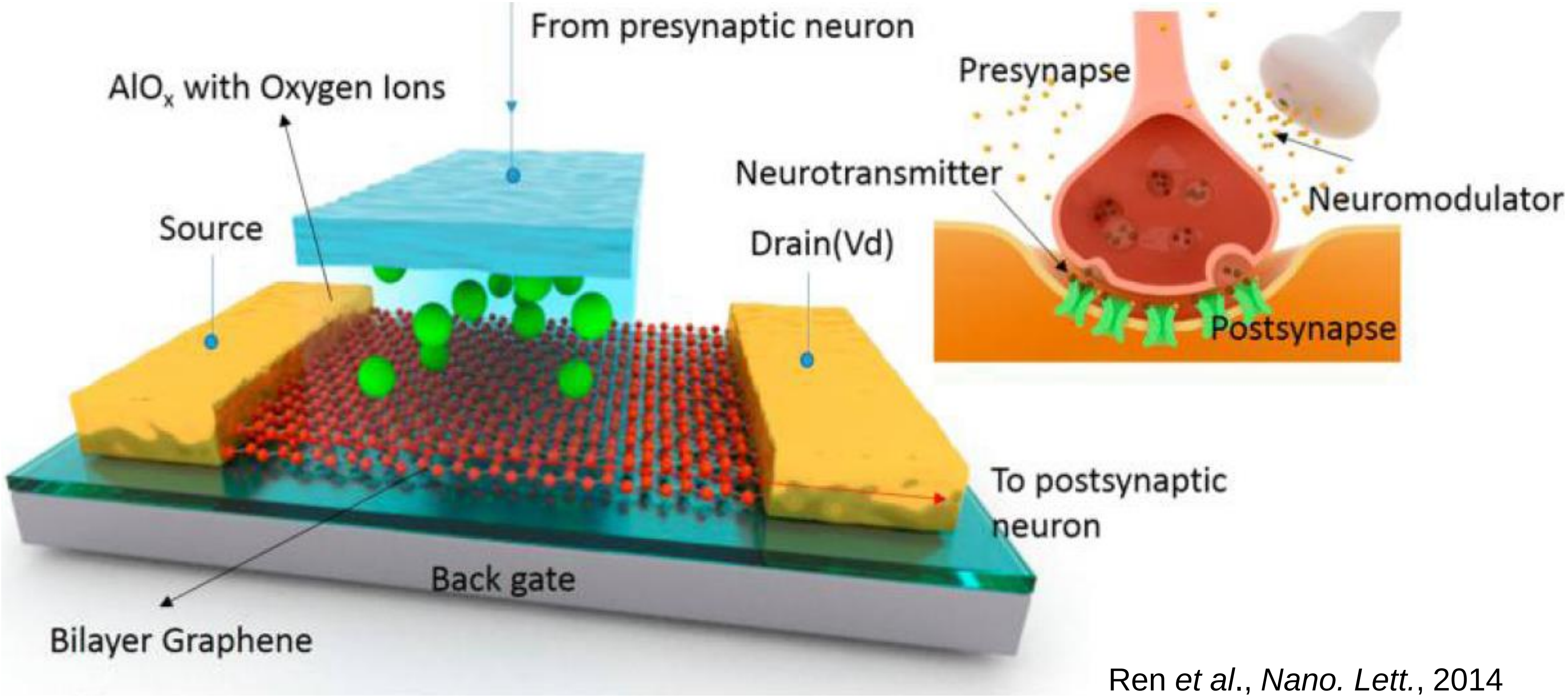




- Fine control over conductance
- Stable operation with good endurance

Burgt *et al.*, *Nat. Mater*, 2017

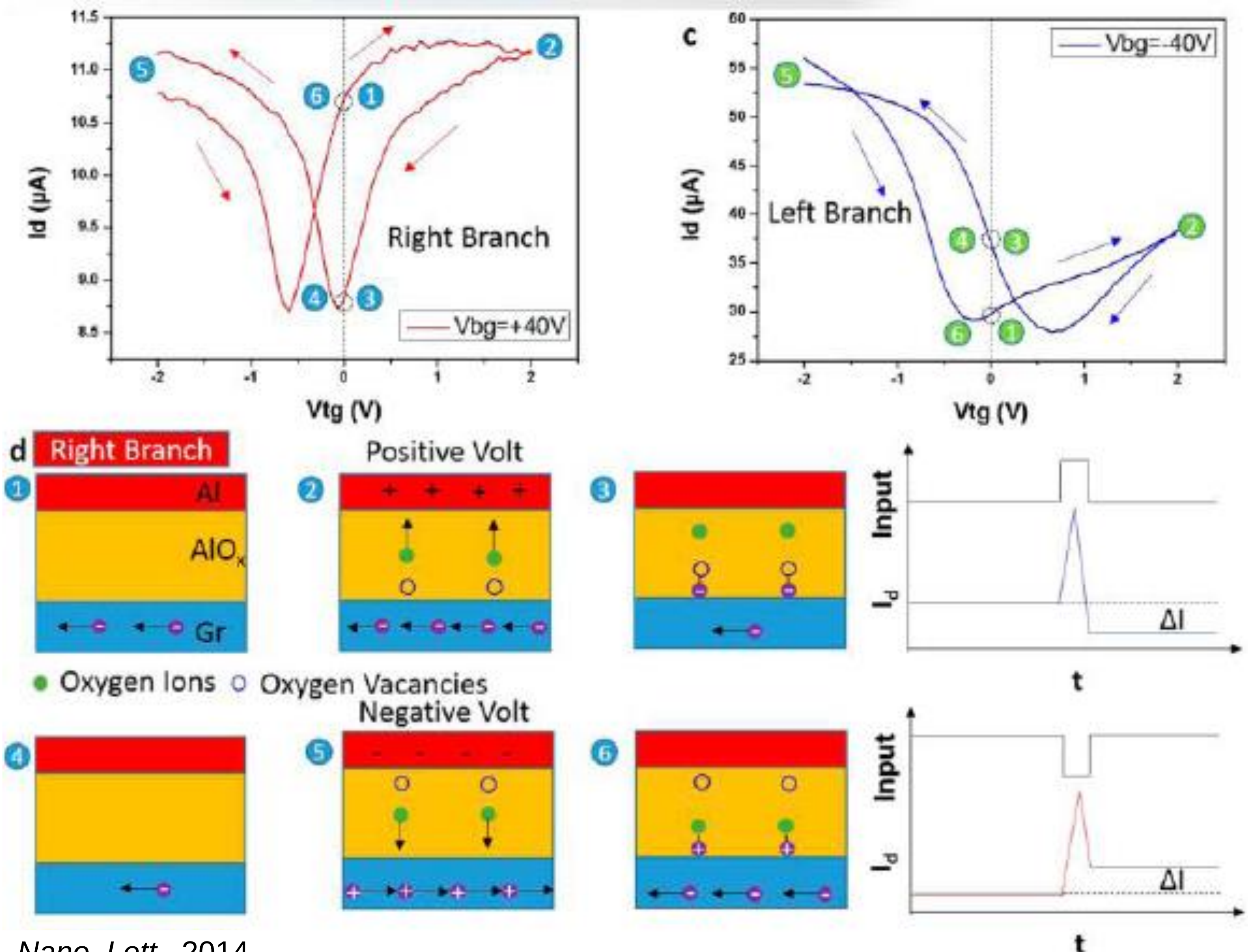
Graphene FET with Top AlOx Gate



Ren *et al.*, *Nano. Lett.*, 2014

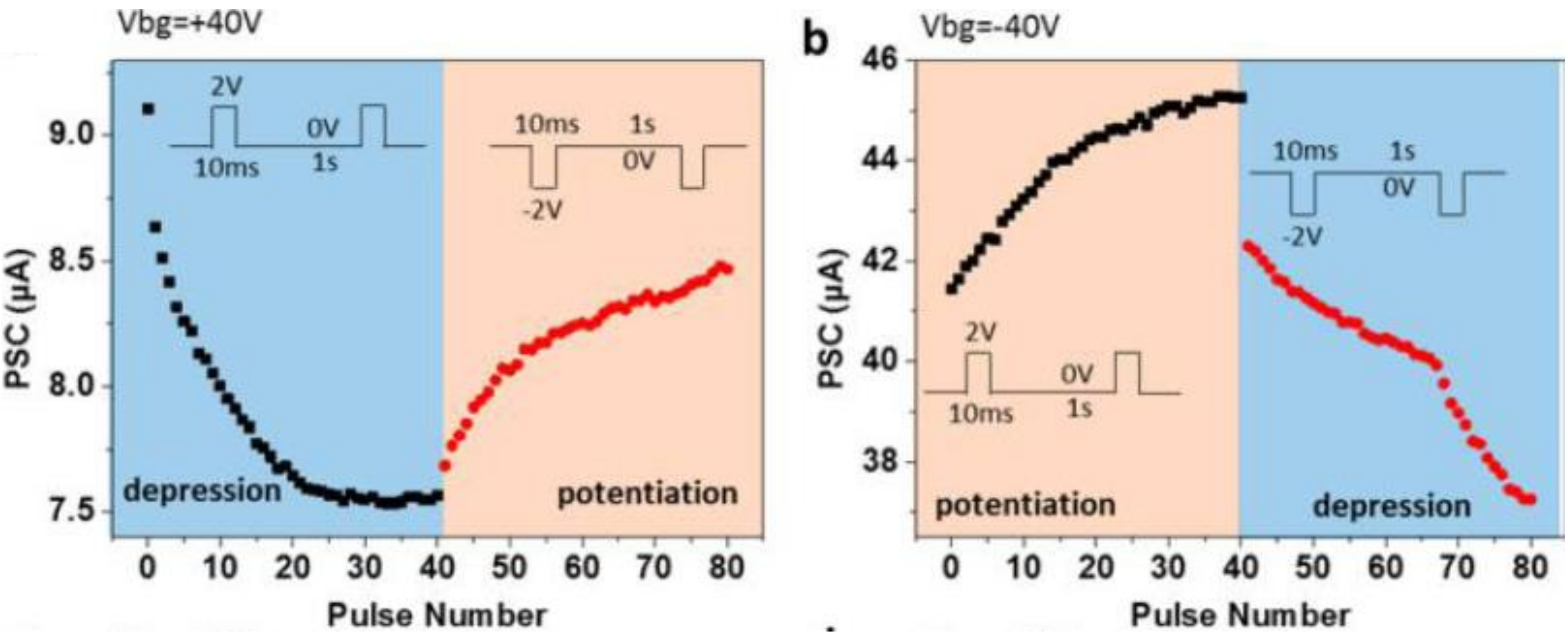
- Graphene field effect transistor
- Back-gate: electron or hole
- Top-gate: AlO$_x$

Charge Trapping in AlO_x



Ren *et al.*, *Nano. Lett.*, 2014

Long Term Potentiation and Depression



Ren *et al.*, *Nano. Lett.*, 2014

- Continuous change via pulse trains