Lab 4: OpenCL Channels on FPGA and Compilation Reports

Due Date: See the course syllabus or piazza page.

rev:11/26/17

Objectives

- Learn the advanced features in OpenCL programming
- Learn the basics of compiling a kernel binary for an FPGA board.
- Understand how OpenCL channels are used
- Understand the compilation reports generated by Intel FPGA OpenCL compiler.

Description

In this lab, you will be given an OpenCL project called "channelizer" including host program and kernels. The source code is on our github repository [1].
(It can also be found on Intel FPGA resource page at
https://www.altera.com/support/support-resources/design-examples/design-software/opencl/channelizer.html)

"The channelizer combines a polyphase filter bank (PFB) with a fast Fourier transform (FFT) to reduce the effects of spectral leakage on the resulting frequency spectrum.
The core kernels of this benchmark (fft1d, filter, reorder) are designed to operate in a streaming manner, using Intel's channels extension to the OpenCL standard. The channelizer accepts eight real samples streaming into the PFB stage and produces eight complex FFT bins per clock cycle."

You need to do the following in this lab:

(1) Compile the source code to generate the OpenCL binaries for both host and FPGA [note: the kernel compilation process can take up to two hours];
(2) Execute the binaries on the FPGA and collect execution results;
(3) Read the reports generated during the compilation phase to understand the kernel analytical data such as area and memory usages, loop structure and kernel pipeline information.

In this lab, you are not required to design new code. However, you should get familiar with the OpenCL development environment, tools and the design flow on an FPGA based platform. You will practice the commands, and perform the compilation and execution steps in a Linux environment. **You must execute the binary on the FPGA board**, instead of running the program in emulation mode. Even though multiple

students can run the compilation tools at the same time, only one student can execute the binary on the single FPGA board at a time. Therefore, we will need to rely on the Doodle to coordinate the exclusive occupancy of the FPGA card. Please use this doodle page to reserve your time: https://doodle.com/poll/4vk3eghngbbmv9b2

Helpful Notes

Start the lab early.
To build the binary for host, run command "**make**".
To build the binary for FPGA, run the following command:
aoc device/channelizer.cl -o bin/channelizer.aocx --fp-relaxed --fpc --board de5net_a7 -v --report

The report file will be located in "bin/channelizer/reports" directory. You can copy the entire reports folder to your local computer and then view the file "report.html"

Deadline

See Piazza course forum and/or course syllabus.

Deliverables

A Lab report that contains the following sections:

1. Description of the lab in your own words
2. Summary of the outcome (final results, working, partial working, etc.). In this lab you will need to capture the outputs from the execution. In addition, you need to choose at least two types of kernel analysis reports (such as area usage and kernel pipeline) to describe how the compiler attempts to optimize the circuit design on FPGA.
3. Main hurdles and difficulties (expected to include some specifics)
4. Things learned from this lab (valuable takeaways)
5. Suggestions (Optional)

Reference

[1] Lab Assignment materials posted on git repository :
https://github.com/ACANETS/eece-6540-fall2017