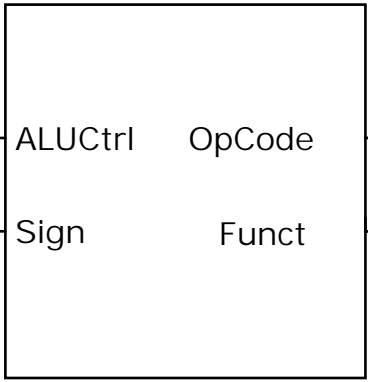
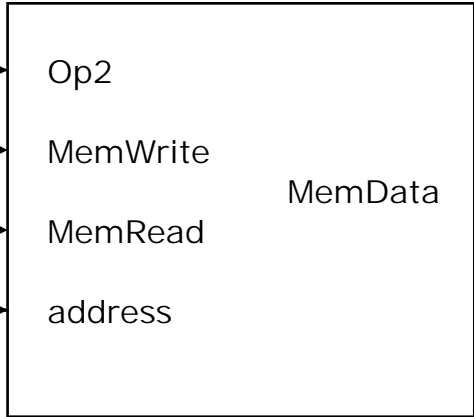


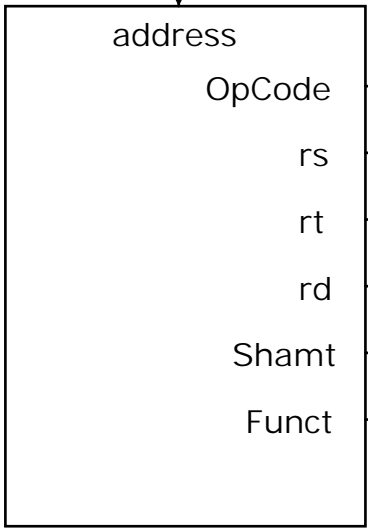
Controller



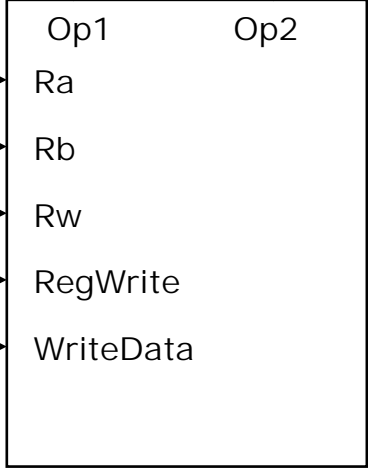
ALU Control



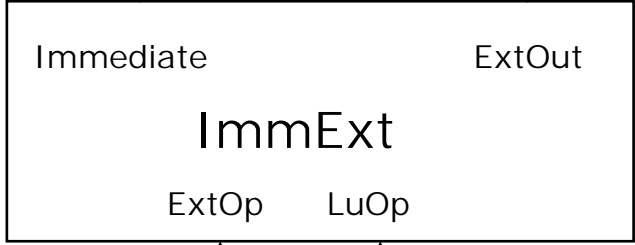
Data Memory



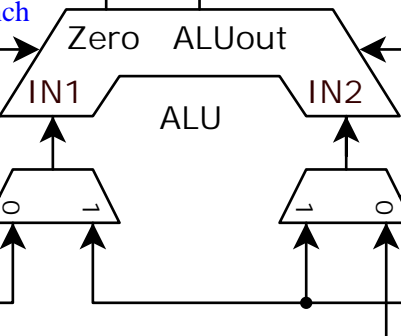
Instructions Memory



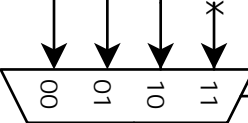
Register File



ImmExt



ALU



MementoReg

ALUctrl

Sign

PCSrc[0]

PCSrc[1]

<31:28>

Branch

ALUctrl

ALUSrc1

MemWrite

MemRead

Sign

ALUSrc2

address

OpCode

rs

rt

rd

Shamt

Funct

Op1

Op2

Ra

Rb

Rw

RegWrite

WriteData

Immediate

ExtOut

ExtOp

LuOp

RegWrite

RegDst

<<2

<<2