|  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Instruction | PCSrc [1:0] | Branch | RegWrite | RegDst [1:0] | MemRead | MemWrite | MemtoReg [1:0] | ALUSrc1 | ALUSrc2 | ExtOp | LuOp |
| lw | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 |
| sw | 0 | 0 | 0 | x | x | 1 | x | 0 | 1 | 1 | 0 |
| lui | 0 | 0 | 1 | 0 | x | 0 | 0 | 0 | 1 | x | 1 |
| add | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| addu | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| sub | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| subu | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| addi | 0 | 0 | 1 | 0 | x | 0 | 0 | 0 | 1 | 1 | 0 |
| addiu | 0 | 0 | 1 | 0 | x | 0 | 0 | 0 | 1 | 1 | 0 |
| and | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| or | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| xor | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| nor | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| andi | 0 | 0 | 1 | 0 | x | 0 | 0 | 0 | 1 | 0 | 0 |
| sll | 0 | 0 | 1 | 1 | x | 0 | 0 | 1 | 0 | x | x |
| srl | 0 | 0 | 1 | 1 | x | 0 | 0 | 1 | 0 | x | x |
| sra | 0 | 0 | 1 | 1 | x | 0 | 0 | 1 | 0 | x | x |
| slt | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| sltu | 0 | 0 | 1 | 1 | x | 0 | 0 | 0 | 0 | x | x |
| slti | 0 | 0 | 1 | 0 | x | 0 | 0 | 0 | 1 | 1 | 0 |
| sltiu | 0 | 0 | 1 | 0 | x | 0 | 0 | 0 | 1 | 1 | 0 |
| beq | zero | 1 | 0 | x | x | 0 | x | 0 | 0 | 1 | x |
| j | 2 | 0 | 0 | x | x | 0 | x | x | x | x | x |
| jal | 2 | 0 | 1 | 2 | x | 0 | 2 | x | x | x | x |
| jr | 3 | 0 | 0 | x | x | 0 | x | x | x | x | x |
| jalr | 3 | 0 | 1 | 1 | x | 0 | 2 | x | x | x | x |