

Part B

An advanced scalable hardware accelerator for optical flow

An Advanced Scalable Hardware Accelerator for Optical Flow

An advanced scalable hardware accelerator for optical flow

Chen Dahan

313428468

An advanced scalable hardware accelerator for optical flow

Ofri Bata

206459612

An advanced scalable hardware accelerator for optical flow

Shahar Gino

22/12/2024

**Acknowledgments**

We would like to express my sincere gratitude to all those who have contributed to the successful completion of this project.

First, our supervisor, Shaher Gino, for his invaluable support, guidance, and encouragement throughout the project. And for the time and dedication he invested in helping us.

We would also like to extend our thanks to the entire staff of the VLSI Lab, Goel Samuel and Riyad Nasrallah for their assistance during the development of this project.

**Table of Contents**

[1.Introduction 10](#_Toc177907818)

[1.1. Optical-Flow background 10](#_Toc177907819)

[1.2. Object-Detection and Video-Registration 13](#_Toc177907820)

[1.3. AMBA APB 15](#_Toc177907821)

[1.4. Paper study 21](#_Toc177907822)

[2. Accelerator Implementation 30](#_Toc177907823)

[2.1. Block diagram 30](#_Toc177907824)

[2.2. Block description (+flow-chart) 31](#_Toc177907825)

[2.3. Pins description 32](#_Toc177907826)

[2.4. Clocks and Resets 33](#_Toc177907827)

[2.5. Interfaces description 33](#_Toc177907828)

[2.6. Sub-units description 34](#_Toc177907829)

[2.6.1 oflow\_core 34](#_Toc177907830)

[2.6.2 oflow\_registration 38](#_Toc177907831)

[2.6.3 oflow\_conflict\_resolve 42](#_Toc177907832)

[2.6.4 oflow\_Mem\_buffer\_wrapper 49](#_Toc177907833)

[2.7. Programmer’s Guide 66](#_Toc177907834)

[3. Zero-order ("aliveness") verification 67](#_Toc177907835)

[3.1. Test-Plan and Test-Results oflow\_top 67](#_Toc177907836)

[3.2. Test-Plan and Test-Results oflow\_core 69](#_Toc177907837)

[3.3. Test-Plan and Test-Results oflow\_registration 72](#_Toc177907838)

[3.4. Test-Plan and Test-Results oflow\_conflict\_resolve 74](#_Toc177907839)

[3.5. Test-Plan and Test-Results oflow\_mem\_buffer\_wrapper 74](#_Toc177907839)

[4. Summary 85](#_Toc177907840)

[4.1 Project's summary 85](#_Toc177907841)

[4.2 Take message home 86](#_Toc177907842)

[4.3 Next steps 86](#_Toc177907843)

[5.References 87](#_Toc177907844)

**Table of Figures**

[Figure 1: Optical Flow Illustration 12](#_Toc179729934)

[Figure 2: BBoxes after object detection 14](#_Toc179729935)

[Figure 3: APB Protocol Interface 16](#_Toc179729936)

[Figure 4: APB - Write transfer with no wait states 17](#_Toc179729937)

[Figure 5: APB - Connection between Master and Slave 18](#_Toc179729938)

[Figure 6: APB - Read transfer with no wait states 19](#_Toc179729939)

[Figure 7: Paper Study - System Architecture 25](#_Toc179729940)

[Figure 8: Paper Study - Finite State Machine 25](#_Toc179729941)

[Figure 9: Paper Study - The relationship between the block radius and AAE 27](#_Toc179729942)

[Figure 10:Top level-external interface 30](#_Toc179729943)

[Figure 11:Top level-block diagram 30](#_Toc179729944)

[Figure 12: Oflow-Core - block diagram 34](#_Toc179729945)

[Figure 13: oflow-pe - block diagram 38](#_Toc179729946)

[Figure 14: oflow-Feature-Extraction - block diagram 43](#_Toc179729947)

[Figure 15: oflow-Feature-Extraction - FSM 44](#_Toc179729948)

[Figure 16: oflow-Mem-Buffer-Wrapper - block diagram 47](#_Toc179729949)

[Figure 17: oflow-Mem-Buffer All-Mem - block diagram 51](#_Toc179729950)

[Figure 18: oflow-Similarity-Metric - block diagram 54](#_Toc179729951)

[Figure 19: oflow-Similarity-Metric - Internal block diagram 56](#_Toc179729952)

[Figure 20: oflow-Similarity-Metric - FSM 57](#_Toc179729953)

[Figure 21: oflow-calc-iou - Block Diagram 63](#_Toc179729954)

[Figure 22: Calc-Iou - IoU Examples 70](#_Toc179729955)

[Figure 23: oflow-Calc-Iou - IoU formula 70](#_Toc179729956)

[Figure 24: Test Results - Reg-File - Write transaction 72](#_Toc179729957)

[Figure 25: Test Results - Reg-File - Read transaction 73](#_Toc179729958)

[Figure 26: Test result - Feature-Extraction 75](#_Toc179729959)

[Figure 27: Test result – oflow-Mem-Buffer - Write transaction 77](#_Toc179729960)

[Figure 28: Test result – oflow-Mem-Buffer - Read transaction 78](#_Toc179729961)

[Figure 29: Test result – oflow-Similarity-Metric - Overlap case - Inputs 79](#_Toc179729962)

[Figure 30: Test result – oflow-Similarity-Metric - Overlap case - Outputs 79](#_Toc179729963)

[Figure 31: Test result – oflow-Similarity-Metric -Without overlap case - Inputs 83](#_Toc179729964)

[Figure 32: Test result - Similarity-Metric -Without overlap case - Outputs 83](#_Toc179729965)

[Figure 33: Test result – oflow-Similarity-Metric - calc iou- With overlap case 86](#_Toc179729966)

[Figure 34: Test result – oflow-Similarity-Metric -calc iou- Without overlap case 88](#_Toc179729967)

**Table of Tables**

[Table 1: Conventions & Terms 7](#_Toc177907881)

[Table 2: Paper Study - Data sequence and Algorithm 23](#_Toc177907882)

[Table 3: Paper Study - Experimental Results 25](#_Toc177907883)

[Table 4: Paper Study - Time Complexity Analysis 27](#_Toc177907884)

[Table 5: Oflow-Top - Pins Description 32](#_Toc177907885)

[Table 6: Oflow-Reg-File - Pins Description 36](#_Toc177907886)

[Table 7: Oflow-Feature-Extraction - Pins Description 39](#_Toc177907887)

[Table 8: Oflow-Mem-Buffer – Structure of the desired memory 44](#_Toc177907888)

[Table 9: Oflow-Mem-Buffer - Pins Description 46](#_Toc177907889)

[Table 10: Oflow-Similarity-Metric - Pins Description 55](#_Toc177907890)

[Table 11: Oflow-Feature-Extraction - Test Plan 68](#_Toc177907891)

[Table 12: Oflow-Similarity-Metric with overlap - Test Plan 76](#_Toc177907892)

[Table 13: Oflow-Similarity-Metric without overlap - Test Plan 78](#_Toc177907893)

[Table 14: Oflow-Calc-Iou with overlap - Test Plan 81](#_Toc177907894)

[Table 15: Oflow-Calc-Iou without overlap - Test Plan 83](#_Toc177907895)

**Conventions & Terms**

|  |  |
| --- | --- |
| **Term** | **Description** |
| CM | Center of Mass |
| TL | Top Left |
| BR | Bottom Right |
| BBOX | Bounding Box |
| IoU | Intersection Over Union |
| WO | With Out |
| PE | Proccess engine |
| OF, oflow | Optical Flow |
| LUT | Look-Up Table |
| CR | Conflict Resolve |

Table 1: Conventions & Terms

**Abstract**

Today the demand for object registration is growing, for example: security cameras and games with multiple players (like soccer).

Software solutions like Byte-Track are not fast enough for this, therefore the request for hardware accelerator increases.

This project deals with this demand by scalable hardware, that performs the object registration in real time, based on object detection that is implemented by external units.

This accelerator has an original and innovative algorithm, especially the conflict resolve unit.

The algorithm divides into 4 main steps. In the first step a DMA send the BBoxes to the feature extraction unit. In this step, new features are calculated for the next steps. The next step is registration unit, this step is responsible for similarity calculation and labeling the BBoxes. In the next stage the conflicts are resolved by unit which is called conflict resolve. In the last step the features and IDs of the BBoxes in the current frame are stored in the memory for further comparison and calculation of the future frames.

# 1.Introduction

**Major Contribution**:

Original and new HW algorithm for the object-registration requirement, especially Conflict Resolve unit.

## 1.1. Optical-Flow background

**definition:**

Optical Flow pattern of apparent motion of objects, surfaces, and edges in a visual scene caused by the relative motion between an observer and a scene.

Optical flow is a powerful tool that can be used to solve a variety of problems in computer vision, including:

* Motion tracking
* Video stabilization
* Structure from motion
* Video compression
* Video object segmentation, etc.

**Estimation:**

In order to estimate motion as either instantaneous image velocities or discrete image displacements, there is a need for a consistent series of images.

there are various methods to calculate the motion between two frames of scene, which are taken at times, t and .

some of the methods are based gradient.

These methods are called differential since they are based on local [Taylor series](https://en.wikipedia.org/wiki/Taylor_series) approximations of the image signal.

for the 2D case:

A voxel at location(x, y, t) with intensity I(x, y, t) will have moved by between 2 frames.

Optical flow works on several assumptions:

1. The pixel intensities of an object do not change between consecutive frames.
2. Neighboring pixels have similar motion.

, with Tylor series:

The next step is to perform linearization; thus, the calculation of the operation point is:

�(�,�,�)=�(�+Δ�,�+Δ�,�+Δ�)

after dividing the equation by the result is:

And after that, re-arrange the equation:

The above equation is called Optical Flow equation. From this equation, Ix and Iy can be found, they are image gradients. Similarly,  is the gradient along time. But () is unknown. This equation cannot be solved with two unknown variables. So, several methods are provided to solve this problem.

A line of red dots

Description automatically generated

Figure 1: Optical Flow Illustration

This figure shows a ball moving in 5 consecutive frames. The arrow shows its displacement vector.

## 1.2. Object-Detection and Video-Registration

**definition**:

**Object-Detection:** Object detection is a computer vision technique for locating instances of objects in images or videos. Object detection algorithms typically leverage machine learning or deep learning to produce meaningful results. It is an important part of many applications, such as surveillance, self-driving cars, or robotics.

**Video-Registration:**

Video-registration is matching the detected instances of objects through the consequent frames in scene. keeping track of each detected objects uniquely among the incoming frames.

**YOLO**:

One of the leading algorithms of object detection is: YOLO (you only look once).

This is a machine learning algorithm. YOLO proposes using an end-to-end fully convolutional neural network (CNN) to process an image by making predictions of bounding boxes and class probabilities all at once. It differs from the approach taken by previous object detection algorithms.

YOLO is a single-shot detector, Single-shot object detection uses a single pass of the input image to make predictions about the presence and location of objects in the image. It processes an entire image in a single pass, making them computationally efficient.

However, single-shot object detection is generally less accurate than other methods, and it’s less effective in detecting small objects.

 YOLO achieved state-of-the-art results, beating other real-time object detection algorithms by a large margin.

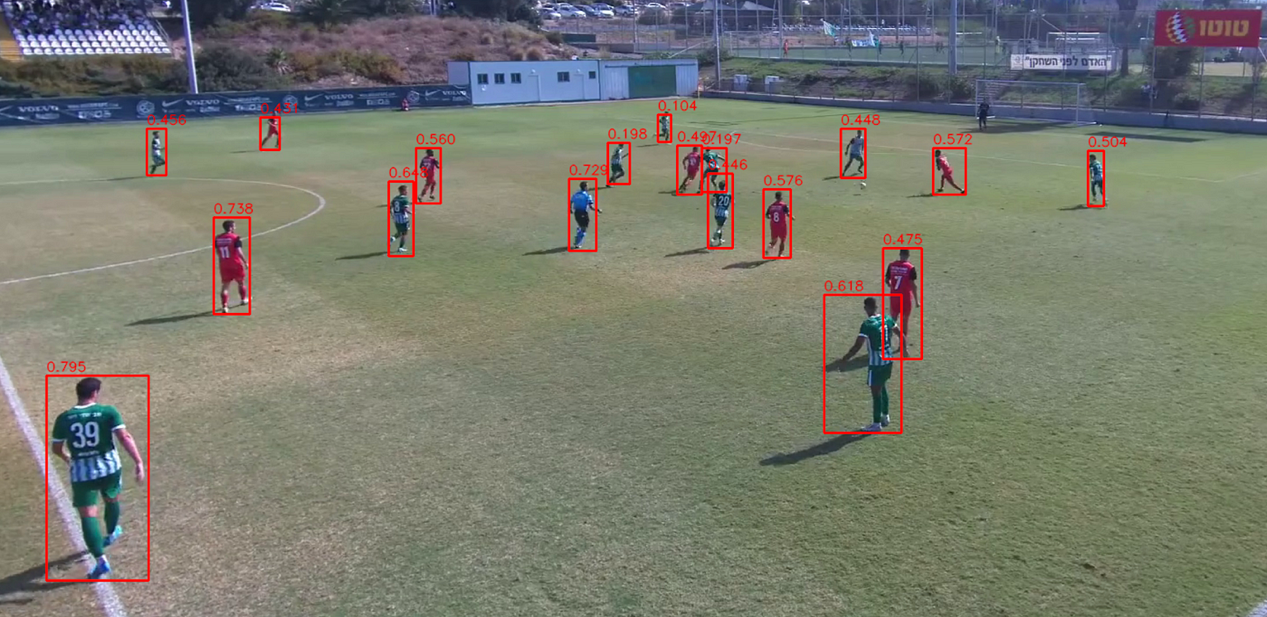


Figure 2: BBoxes after object detection

Figure of bounding box around the object that created by YOLO algorithm.

**The connection to optical flow:**

YOLO can be used in conjunction with optical flow to improve the accuracy of object tracking. Optical flow can be used to track the movement of objects between frames, and this information can be used to improve the accuracy of YOLO's object detections

In objects registration, optical flow can be used to register two images of the same scene taken from different viewpoints. This is done by estimating the optical flow between the two images. The optical flow vectors can then be used to warp one image to match the other image**.**

## 1.3. AMBA APB

Advanced Microcontroller Bus Architecture (AMBA) Advanced Peripheral Bus (APB) Protocol Specification

**definition**:

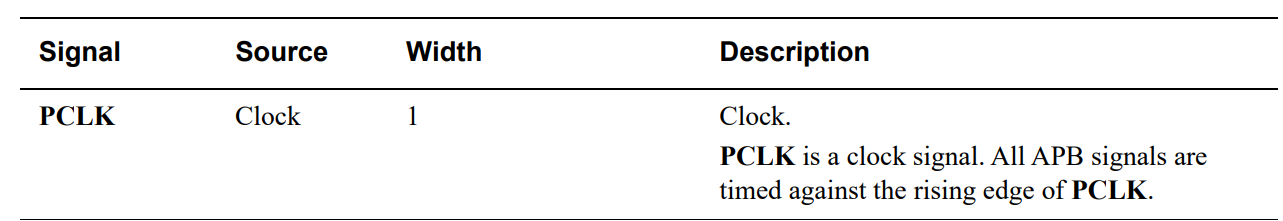
The APB protocol is a low-cost interface, optimized for minimal power consumption and reduced interface complexity. The APB interface is not pipelined and is a simple, synchronous protocol. Every transfer takes at least two cycles to complete.

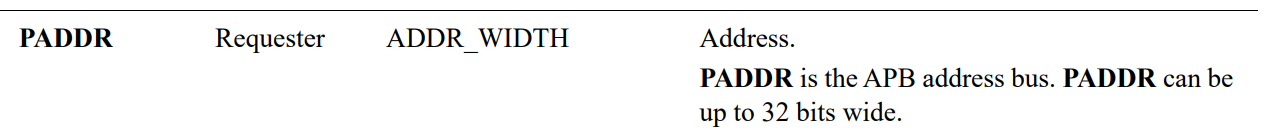
In this project, CPU needs to access the RegFile which resides in the hardware accelerator module. Thus, it will use the APB protocol which is built for these cases.

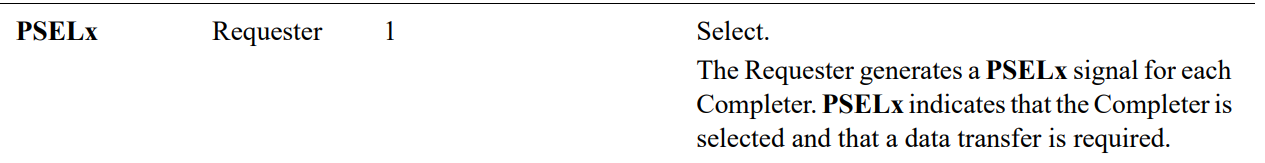
APB peripherals are typically connected to the main memory system using an APB bridge. For example, a bridge from AXI to APB could be used to connect several APB peripherals to an AXI memory system.

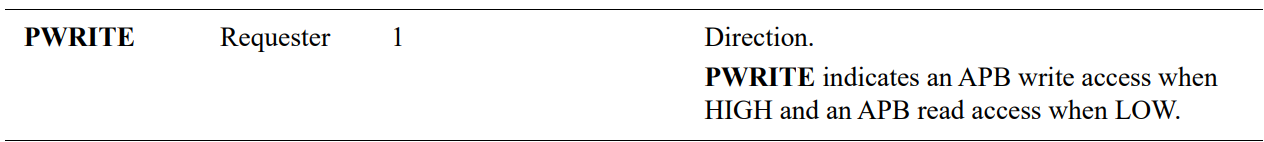
APB transfers are initiated by an APB bridge. APB bridges can also be referred to as a Requester. A peripheral interface responds to requests. APB peripherals can also be referred to as Completer. This specification will use Requester and Completer.

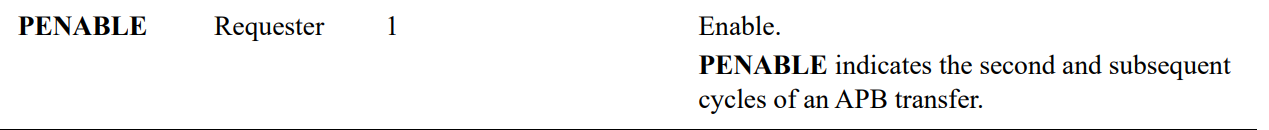
**Signals:**

****

****

****

****

****

**A close-up of a white background

Description automatically generated** ****

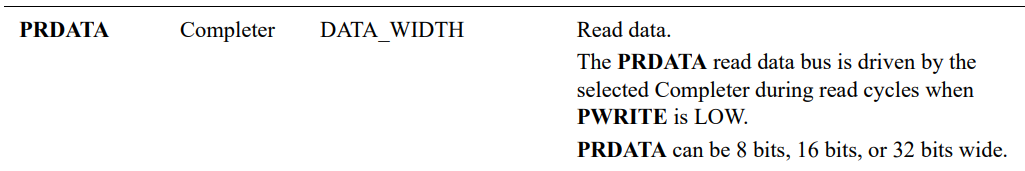
****

Figure 3: APB Protocol Interface

**Write Transfer:**

Write transfers -This section describes the following types of write transfer:

• With no wait states

• With wait states

All signals shown in this section are sampled at the rising edge of PCLK

**with no wait states**

**A diagram of a diagram

Description automatically generated**

Figure 4: APB - Write transfer with no wait states

There are 3 main phases for write transfer**:**

* **The Setup phase** of the write transfer occurs at T1 in Figure 4. The select signal, PSEL, is asserted, which means that PADDR, PWRITE ('1'), and PWDATA must be valid.
* **The Access phase** of the write transfer is shown at T2 in Figure 4 where PENABLE is asserted. PREADY is asserted by the Completer (Slave) at the rising edge of PCLK to indicate that the write data will be accepted at T3. PADDR, PWDATA, and any other control signals must be stable until the transfer is complete.
* **T3-the writing stage**, the data will be written to the Slave register.

At the end of the transfer, PENABLE is de-asserted. PSEL is also de-asserted, unless there is another transfer to the same peripheral.

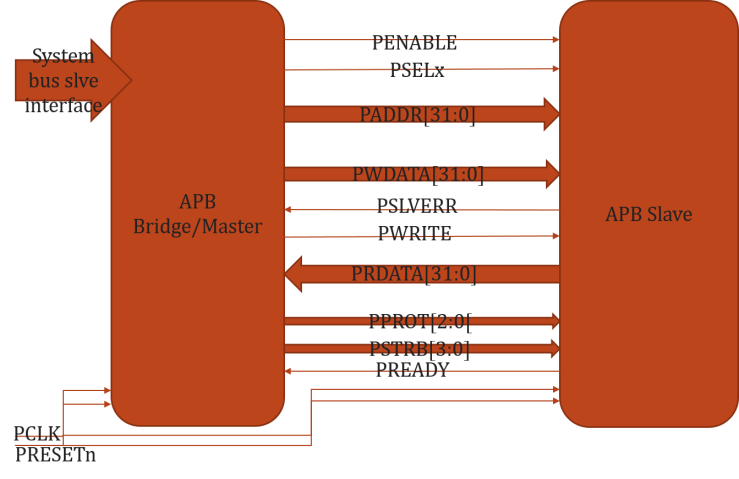


Figure 5: APB - Connection between Master and Slave

**Read transfer:**

Two types of read transfer are described in this section:

• With no wait states

• With wait states

All signals shown in this section are sampled at the rising edge of PCLK. 3.3.1

**With no wait states**

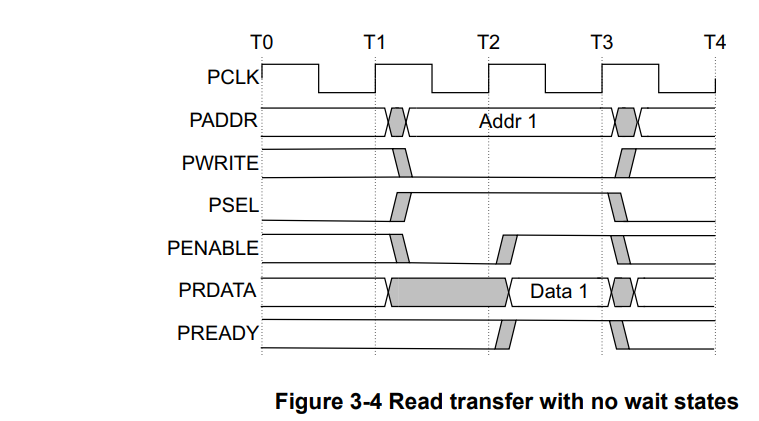
****

Figure 6: APB - Read transfer with no wait states

* **The Setup phase** of the read transfer occurs at T1 in Figure 6. The select signal, PSEL, is asserted, which means that PADDR, PWRITE ('0') must be valid.
* **The Access phase** of the read transfer is shown at T2 in Figure 6 where PENABLE is asserted. PREADY is asserted by the Completer (Slave) at the rising edge of PCLK to indicate that the read data will be accepted at T3. PADDR, PRDATA, and any other control signals must be stable until the transfer completes.
* **T3-the reading stage**, the data will be read to the master.

At the end of the transfer, PENABLE is de-asserted. PSEL is also de-asserted, unless there is another transfer to the same peripheral.

The Completer must provide the data before the end of the read transfer

## 1.4. Paper study

**introduction**:

The paper study proposes an event-based block matching algorithm to calculate OF (Optical Flow) on FPGA. In computer vision, OF describes the motion field induced by camera movement through space. OF methods is a search over possible flows to select the most likely one at each image or feature location. This search with dense image blocks is expensive and difficult to calculate on an embedded platform in real time

The DVS (Dynamic Vision Sensor) is data-driven rather than regular-sample driven. Regular-sample driven means camera sends the output data at a fixed interval; thus, it is called a frame-based camera. However, the DVS output is driven by brightness changes rather than a fixed sample interval. Therefore, new OF methods need to be designed. There are various methods that offered comparable accuracy for sharp and sparse edges, but all fail on textured or low spatial frequency inputs, because the underlying assumptions (e.g. smooth gradients or isolated edges) are violated.

In video technology, OF is called motion estimation (ME). The pipeline for ME includes block matching. Block matching means that rectangular blocks of pixels are matched between frames to find the best match. Block matching is computationally expensive. Therefore, it is recommended to use hardware instead of software, as implemented in this experiment.

**Propose Method**:

The output of DVS is a stream of brightness change events. Each event has:

* microsecond timestamp
* a pixel address
* a binary polarity describing the sign of the brightness change

In this experiment, events are accumulated into time slice frames as binary bitmap frames called slices.

A block is a square centered around the incoming event’s location. Matching is based on a distance metric. In this experiment, they use Hamming Distance (HD). HD is the count of the number of differing bits. For bitmaps, HD is exactly like SAD (Sum-of-Absolute-Differences).

The hardware evaluation system is divided into two parts, one for data sequencing and monitoring and the other for the algorithm implementation.

|  |  |  |
| --- | --- | --- |
| **data sequencing and monitoring** | | **algorithm implementation** |
| Sequencer | Monitor | When event arrives, the next things are chosen:   * on centered block as a reference in slice t-d * 9 blocks in slice t-2d   They will be sent to the HD module to calculate the distance.  The algorithm finds the most similar block on the t-2d slice. According to the brightness-constancy assumption of OF, A similar block in the t-2d slice should be seen for the block that best matches the actual OF. |
| converts the event-based dataset into real-time hardware events sent to the OF FPGA | collects the OF events and sends them over USB to jAER for rendering and analysis | 1. Hamming Distance: The implementation of one HD block is shown in Fig 3. A total of 81 XOR logic gates receive input from corresponding pixels on the slices. The XOR outputs are summed to compute the HD. 2. Minimum Distance Computation: The last step of the algorithm is to find the minimum distance candidate. Part of the novel minimum circuit is shown in Fig 4. It is a parallel implementation that outputs the index of the minimum distance direction. At the end, the part whose sum is zero is the minimum candidate. |
| The target of this stage is to compare software and hardware processing of OF algorithm | | The minimum distance candidate is determined in one clock cycle compared to SW implementation. |

Table 2: Paper Study - Data sequence and Algorithm

The OF architecture (Figure 7) consists of 3 main modules: Finite State Machine (FSM), Slice RAMs and Rotation Control Logic.

FSM consists of 3 main stages: data receiving module, OF calculation module, and data sending module.

A diagram of a computer system

Description automatically generatedA diagram of a machine

Description automatically generated

Figure 7: Paper Study - System Architecture

One is the current collecting slice starting at time t and the other two are the past two slices starting at times t-d and t-2d. d is the slice duration. At intervals of d, the rotation control logic rotates the three slices. The t slice accumulates new data. It starts out emptyotation control logic rotates the three slices. The t slice accumulates new data. It starts out emptyand gradually accumulates events, so it cannot be used for matching to past slices. The two past slices are used for OF, but the OF computation is done at the location of each event stored into the t slice, and thus is driven by these events.

t-2d slice

t-d slice

t slice

Three 240x180-pixel DVS event bitmaps slices

Figure 8: Paper Study - Finite State Machine

**Experimental Results:**

In the experiment, three different sample datasets that are real DVS were tested. They are listed in the table below.

|  |  |  |  |
| --- | --- | --- | --- |
| **Dataset** | **Characterization** | **How was it recorded?** | **Result** |
| Box Translation | edges | the boxes scene has a box in the foreground and clutter in the background and the camera pans to the left | most vectors point correctly east |
| Pavement | sparse points | the camera was down looking and carried by hand | most vectors point southeast |
| Gravel | dense textures | dataset is recorded outside.  movement is eastward | most vectors point east |

Table 3: Paper Study - Experimental Results

Errors are mostly caused by DVS noise or aperture ambiguity for the extended edges.

1. **Accuracy analysis**

two ways to calculate event based OF accuracy:

1. AEE - measures error in the direction of estimated flow includes speed error.
2. AAE - measures error in the direction of estimated flow.

They chose two other algorithms to compare with their algorithm: Lucas-Kanade and Local Plane.

It can be seen that the block matching algorithm has the best accuracy for AEE and second-best for AAE.

In addition, they show in Fig. 6 that bigger block dimension leads to better accuracy. However, larger blocks consume more logic and reduce spatial resolution of the flow.

A graph with a line

Description automatically generated

Figure 9: Paper Study - The relationship between the block radius and AAE

1. **Time complexity analysis**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | Software Implementation | | | FPGA Implementation | | |
| Complexity | Quadratically | | | Linearly | | |
| Processing Part | **reading data from three slices** | **HD calculation** | **looking for the minimum** | **reading data from three slices** | **HD calculation** | **looking for the minimum** |
| Time | linear time to read data from RAM since multiple data cannot be read from one RAM simultaneously. | quadratic | quadratic | linear time to read data from RAM since multiple data cannot be read from one RAM simultaneously. | 1 clock cycle | 1 clock cycle |
| Summary | 4.5 | | | (block dimension + 2) cycles = 0.22 | | |

Table 4: Paper Study - Time Complexity Analysis

**Conclusion**:

In this paper, they invented a new method to estimate the event-based optical flow on FPGA in real time. The software computational cost of Hamming Distance increases quadratically as the block size increases, however, in FPGA, all the bits in the block can be calculated at the same time which leads to a constant time for all block sizes. This greatly reduces the overall computation time for the FPGA implementation, which is 20 times faster than the software implementation.

There are additional possible improvements:

* Considering the speed also
* Explore other distance metrics
* Implement feedback control on the slice duration to better exploit the unique feature of DVS event output that it can be processed at any desired sample rate

# 2. Accelerator Implementation

## 2.1. Block diagram

**oflow\_top overview**

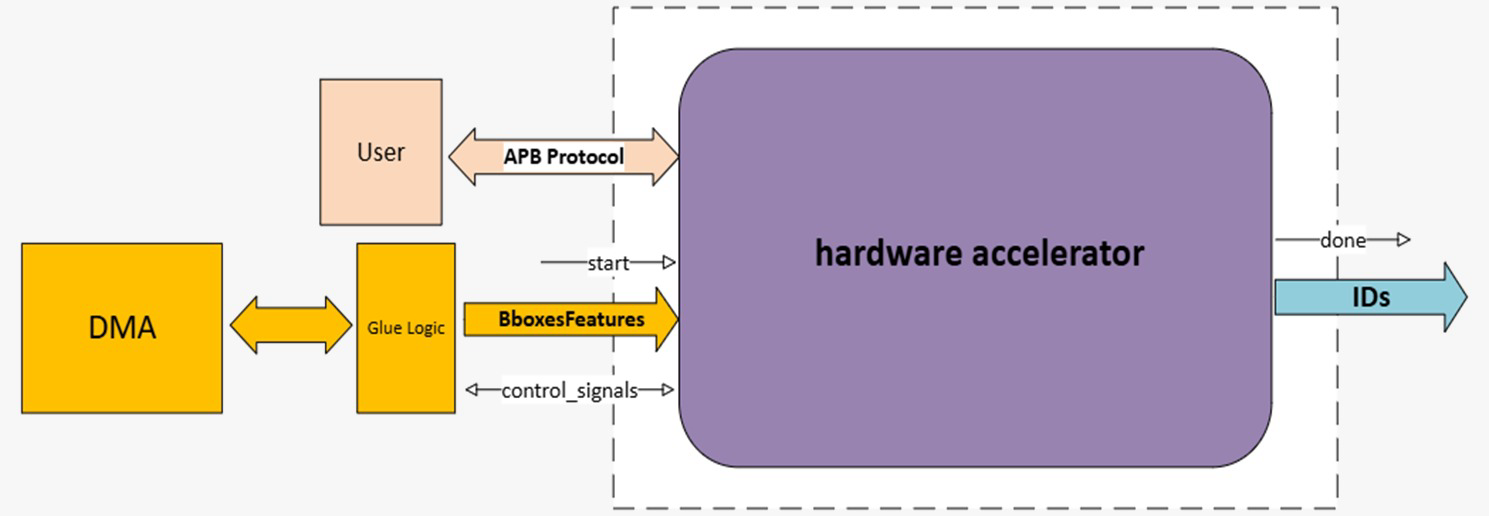
****

Figure 10:Top level-external interface

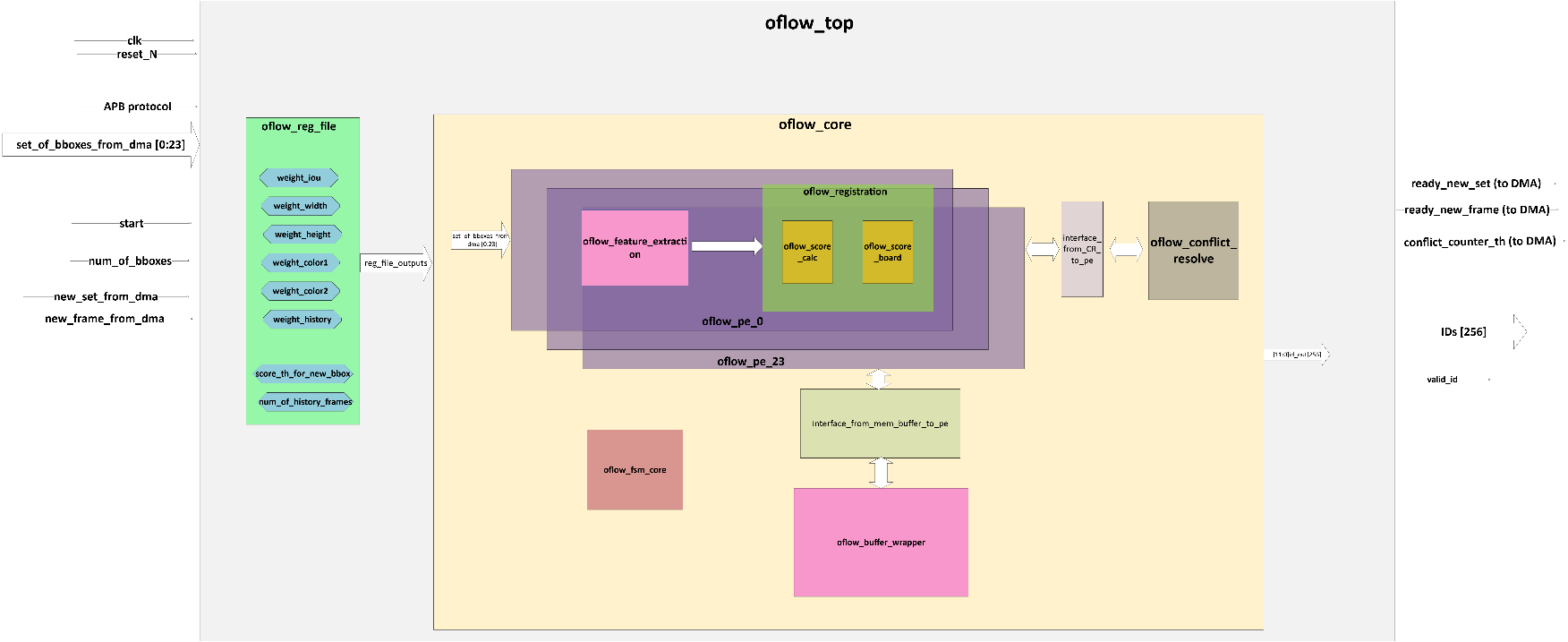


Figure 11:Top level-block diagram

## 2.2. Block description (+flow-chart)

The oflow\_top unit is responsible for processing data received from the GLU logic, specifically handling a set of 24 bounding boxes (BBoxes) for each video frame. The primary function of this unit is to label these bounding boxes on a frame-by-frame basis.

1. **Bounding Box Identification:**
   * **New Bounding Boxes:** For any BBox that is newly identified in a frame (its score is above threshold value), the unit will assign a unique ID.
   * **Existing Bounding Boxes:** If a BBox has been identified in previous frames, the unit will recognize it and assign the same ID that was previously given, ensuring consistent tracking across frames.
2. **Conflict Resolve:**
   * In scenarios where more than 10 BBoxes are erroneously recognized as having the same ID (conflict), the unit will signal the DMA that it had 10 conflicts and reset the process.
   * And if there is a conflict between more than 1 BBox this unit will resolve this by assigning the desired ID to the BBox with the minimum score, which is considered the most appropriate match.
3. **Communication and Control:**
   * The unit interfaces with the user via the Advanced Peripheral Bus (APB). Through this interface, the user can set the weighting for each similarity metric used in BBox identification and can set the score threshold for new BBox and the number of history frames.
   * The unit will signal the GLU logic when it is ready to receive a new set of bounding boxes or a new frame for processing.
   * Upon completion of processing, the unit will publish the final IDs assigned to each BBox.

This unit consists of 2 units: oflow\_reg\_file and oflow\_core which will be explored later.

## 2.3. Pins description

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal\_Name** | **Type** | **Width** | **Description** |
| apb\_control | I/O |  | Ports of apb protocol to connect between user (Master) and the accelerator (slave) |
| start | I | 1 | Indication to start a new flow of frames |
| set\_of\_BBoxes\_ from\_dma[23:0] | I | 86 | Array of BBoxes' features, contains: [x, y, width, height, color1, color2] |
| num\_of\_BBoxes | I | 8 | Total number of the BBoxes in the current frame |
| new\_set\_from\_dma | I | 1 | Indication that new set of the frame is ready |
| new\_frame\_from\_dma | I | 1 | Indication that new frame is ready |
| ready\_new\_set | O | 1 | Indication to DMA (glue logic) that the proccess of the current set in the frame is done, and the accelerator is ready for next set |
| ready\_new\_frame | O | 1 | Indication to DMA (glue logic) that the proccess of the current frame is done and the labels are set |
| conflict\_counter\_th | O | 1 | Indication to user and fsm\_core\_top that there were #MAX\_CONFLICTS and the accelerator need to return to idle and restart the proccess |
| IDs | O | 12x256 | The labling of the BBoxes |
| valid\_id | O | 1 | Indication to user that the ids outputs are valid to read |

Table 5: Oflow-Top - Pins Description

## 2.4. Clocks and Resets

There is one clock for all of the chip, the period of this clock is 5[ns].

The reset is negative, and it is called reset\_N.

## 2.5. Interfaces description

The accelerator has interface with 2 units:

* 1. CPU: the cpu is the main processing unit, which manages the reg-file unit of the accelerator. This unit accesses the reg-file via AMBA-APB protocol.

This unit will get back the labled BBoxes from the accelerator.

* 1. Glue-logic: the glue-logic is responseble for connecting the accelerator with the DMA that stores the BBoxes. This unit fetches from the DMA 24 BBoxes concurrently and transfers them to the accelerator.

It controls the new\_set and new\_frame.

The inputs from the accelerator are: ready\_new\_set, ready\_new\_frame, conflict\_counter\_th.

## 2.6. Sub-units description

### 2.6.1 oflow\_core

A computer screen shot of a computer

Description automatically generated **Block diagram**

Figure 12: Oflow-Core - block diagram

**Block description (+flow-chart)**

The oflow\_core module is the main unit of the accelerator, handling multiple tasks like feature extraction, object registration, and conflict resolve. It integrates several submodules (PEs), working in parallel to process data related to bounding boxes (bboxes) of objects across frames.

**Overview**

* **Purpose**: The oflow\_core module processes sets of bboxes received from a DMA and calculates scores for object similarity across frames. It assigns unique IDs to objects and handles cases where object identities may conflict.

**Features**

1. **Bounding Box Processing**: The module processes multiple bboxes simultaneously, leveraging hardware parallelism (using multiple Processing Elements, PEs). BBoxes are evaluated based on feature similarity (shape, color, position, etc.), and scores are computed.
2. **State Machines and Control**:
   * Several Finite State Machines (FSMs) coordinate different tasks:
     + *Core FSM*: Handles the overall workflow, including reading from memory and writing to it, feature extraction and registration.
3. **Parallel Processing with PEs**: The module uses multiple PEs (processing elements) to handle operations in parallel. Each PE works on a subset of BBoxes to accelerate processing, making it scalable for large datasets. Each PE consists of feature\_extraction and registration units. (The registration unit will be described later here, and the feature\_extraction was described in part A of this project).
4. **Conflict Resolve**: The module resolves conflicts that arise when multiple objects might share similar characteristics (e.g., overlapping bounding boxes). The conflict resolve logic ensures that each object gets a unique ID (until order 2), and alerts when there are at least 10 BBoxes with conflicts.
5. **Buffer Memory Management**: The module reads and writes bbox data to/from memory buffers. This is necessary because the system operates on multiple frames and tracks objects across time.

**Pins description**

|  |  |  |  |
| --- | --- | --- | --- |
| Signal\_Name | Type | Width | Description |
| set\_of\_bboxes\_from\_dma | I | [85:0]x256 | Input array of bounding boxes features from DMA. Each element corresponds to a bounding box feature. |
| new\_set\_from\_dma | I | 1 | Signal indicating that a new set of bounding boxes is ready from Glue\_Logic. |
| start | I | 1 | Start signal for indication to start the process. |
| new\_frame | I | 1 | Signal indicating that a new frame is ready from Glue\_Logic. |
| ready\_new\_set | O | 1 | Indicates the Glue\_Logic that the accelerator is ready to receive a new set of bounding boxes from DMA. |
| ready\_new\_frame | O | 1 | Indicates the Glue\_Logic that the accelerator is ready to receive a new frame from DMA. |
| conflict\_counter\_th | O | 1 | Signal indicating that the number of conflicts has been reached the threshold. |
| iou\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of iou\_metric. |
| w\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of width\_metric. |
| h\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of height\_metric. |
| color1\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of color1\_metric. |
| color2\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of color2\_metric. |
| dhistory\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of history\_metric. |
| score\_th\_for\_new\_bbox | I | 32 | This parameter will be set by the user by apb\_pwdata. It will determine the score threshould for defining BBox as a new BBox. |
| num\_of\_history\_frames | I | 3 | This parameter will be set by the user by apb\_pwdata. It will determine the number of history frames that will be compared with current frame. Eg. 1-5 |
| num\_of\_bbox\_in\_frame | I | 8 | Number of bounding boxes in the current frame. |
| valid\_id | O | 1 | Signal indicating that the output bounding box IDs are valid. |
| ids | O | [11:0]x256 | Array of output bounding box IDs, one for each detected object in the frame. |

Table 6: Oflow-core - Pins Description

**oflow\_pe**

**A screenshot of a computer

Description automatically generated**

Figure 13: oflow-pe - block diagram

**Block description (+flow-chart)**

This unit consists of 2 units: oflow\_feature\_extraction and oflow\_registration.

The oflow\_feature\_extraction was described in detail in part A.

The oflow\_registration will be described later in this part.

The main purpose of this unit is to extract the features of the BBoxes in the current frame and comparing them to the BBoxes in the history frames (from the mem\_buffer) to assist in the labeling process.

This block communicates with two main units with the help of interfaces.

One is for the connection with the oflow\_mem\_buffer\_wrapper (interface\_mem\_buffer\_pe) and the other is for connection with the oflow\_conflict\_resolve (interface\_cr\_pe).

For accelerate the calculation process there are 24 PEsthat work concurrently. Each PE serves one BBox in the current set of the current frame.

**Pins description**

|  |  |  |  |
| --- | --- | --- | --- |
| Signal\_Name | Type | Width | Description |
| iou\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of iou\_metric. |
| w\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of width\_metric. |
| h\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of height\_metric. |
| color1\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of color1\_metric. |
| color2\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of color2\_metric. |
| dhistory\_weight | I | 10 | This parameter will be set by the user by apb\_pwdata. It will determine the weight of history\_metric. |
| bboxes\_from\_dma |  | 86 | Input array of bounding boxes features from DMA. Each element corresponds to a bounding box feature. |
| num\_of\_pe | Input | 5 | The serial number of the current PE. |
| ready\_new\_frame | Input | 1 | Indicates the Glue\_Logic that the accelerator is ready to receive a new frame from DMA. |
| ready\_new\_set | Input | 1 | Indicates the Glue\_Logic that the accelerator is ready to receive a new set of bounding boxes from DMA. |
| flg\_for\_sampling\_last\_set | Input | 1 | Flag indicating if the last set should be sampled. (because there isn’t ready\_new\_set in the last set). |
| num\_of\_sets | Input | 4 | Total Number of data sets to process in each frame. |
| frame\_num | Input | 8 | The serial number of the current frame. |
| start\_fe | Input | 1 | Signal to start feature extraction. |
| not\_start\_fe | Input | 1 | Signal indicating to not start feature extraction in the specific PE (only in last set). |
| start\_registration | Input | 1 | Signal to start object registration. |
| not\_start\_registration | Input | 1 | Signal indicating to not start object registration in the specific PE (only in last set). |
| done\_pe | Input | 1 | Indicates the completion of calculations for all the sets in the frame. |
| done\_read\_to\_pe | Input | 1 | Indicates that the read operation in the mem\_buffer is done. (in each set). |
| data\_to\_pe\_0 | Input | 145 | Data input to similarity\_metric\_0 in the PE (includes history field). We get signal for read mem\_buffer. |
| data\_to\_pe\_1 | Input | 145 | Data input to similarity\_metric\_1 in the PE (includes history field). We get signal for read mem\_buffer. |
| row\_sel\_to\_pe | Input | 4 | Row selection signal for PE, comes from oflow\_core\_fsm\_write. |
| row\_sel\_to\_pe\_from\_cr | Input | 4 | Row selection signal from conflict resolution unit. (for fill\_hist) |
| write\_to\_pointer\_to\_pe | Input | 1 | Write enable signal for pointer in score board that need to change to resolve conflict. |
| write\_to\_id\_to\_pe | Input | 1 | Write enable signal for ID in score board that need to change to set as a new BBox. |
| data\_from\_cr\_pointer\_to\_pe | Input | 1 | Data from conflict resolution unit for writing pointer in score board that need to change to resolve conflict. |
| data\_from\_cr\_id\_to\_pe | Input | 12 | Data from conflict resolution unit for writing ID in score board that need to change to set as a new BBox. |
| row\_to\_change\_to\_pe | Input | 4 | Row selection signal for changing score board data when there is a conflict / new id. |
| done\_fe | Output | 1 | Indicates the completion of feature extraction.  (stays on ‘1’ until new start\_fe). |
| done\_registration | Output | 1 | Indicates the completion of object registration. |
| done\_score\_calc | Output | 1 bit | Indicates the completion of score calculation. |
| control\_for\_read\_new\_line | Output | 1 bit | Control signal to oflow\_core\_fsm\_read to start reading a new line of data. This signal is asserted to '1' two cycles before done similarity metric to prepare new line of data to be ready for the next similarity metric calculation. |
| data\_out\_pe | Output | 142 | Data output from PE for writing to memory. (without d\_history) (concatenates 2 pes data to 1 row) |
| id\_out | Output | 12x11 | Output array containing IDs from score board. |
| score\_to\_cr\_from\_pe | Output | 32 | Score output from PE to conflict resolution unit. |
| id\_to\_cr\_from\_pe | Output | 12 | ID output from PE to conflict resolution unit. |

**Core FSMs**

The oflow\_core consists of 5 FSMs that orchestrate the integration between the rest of the units. Below is their list:

* oflow\_fsm\_core\_top
* oflow\_fsm\_core\_fe
* oflow\_core\_fsm\_registration
* oflow\_core\_fsm\_read
* oflow\_core\_fsm\_write

**oflow\_fsm\_core\_top**

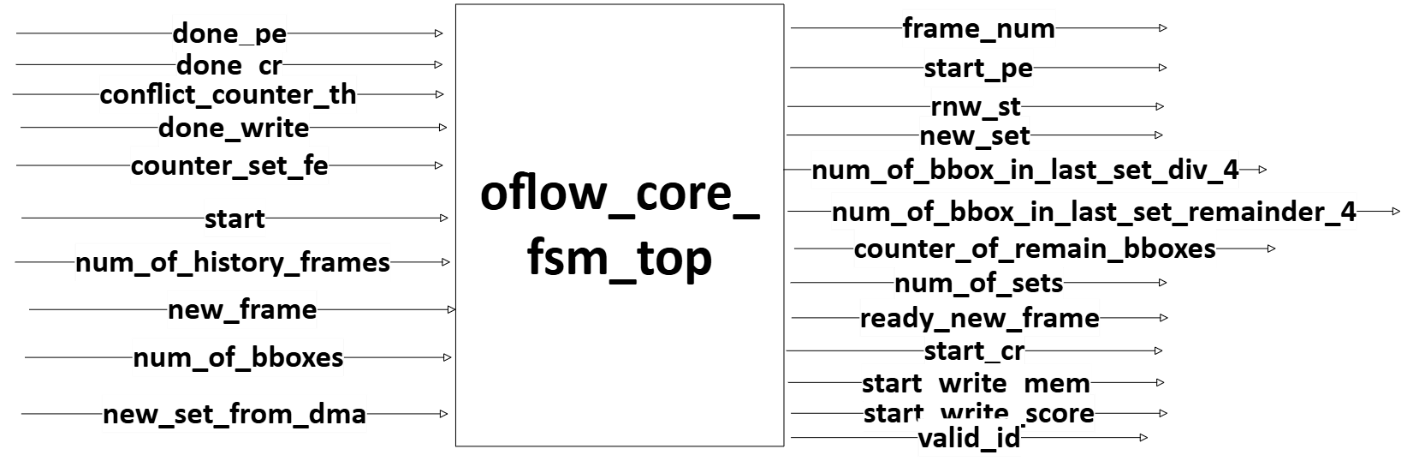


Figure 14: oflow\_core\_fsm\_top - block diagram

A diagram of a program

Description automatically generated

Figure 15: oflow\_core\_fsm\_top - FSM diagram

The oflow\_core\_fsm\_top module is responsible for controlling the overall flow of operations in a hardware system that performs object flow analysis, particularly focusing on feature extraction, registration, and conflict resolve. This module acts as the top-level finite state machine (FSM) for coordinating interactions between various submodules and managing data flow and memory operations. Here's a summary of its states:

* The FSM operates through multiple states, including idle, set\_variables, pe, conflict\_resolve, and write.
* In the idle\_st state, the system awaits new frame.
* In set\_variables\_st, it sets up the necessary variables for processing based on the number of bounding boxes in the frame.
* The pe\_st state activates processing elements (PEs) to handle the feature extraction and registration process.
* If there are conflicts in the data, the conflict\_resolve\_st state handles resolution.
* Finally, the write\_st state manages writing the processed results to memory.

**oflow\_fsm\_core\_fe**

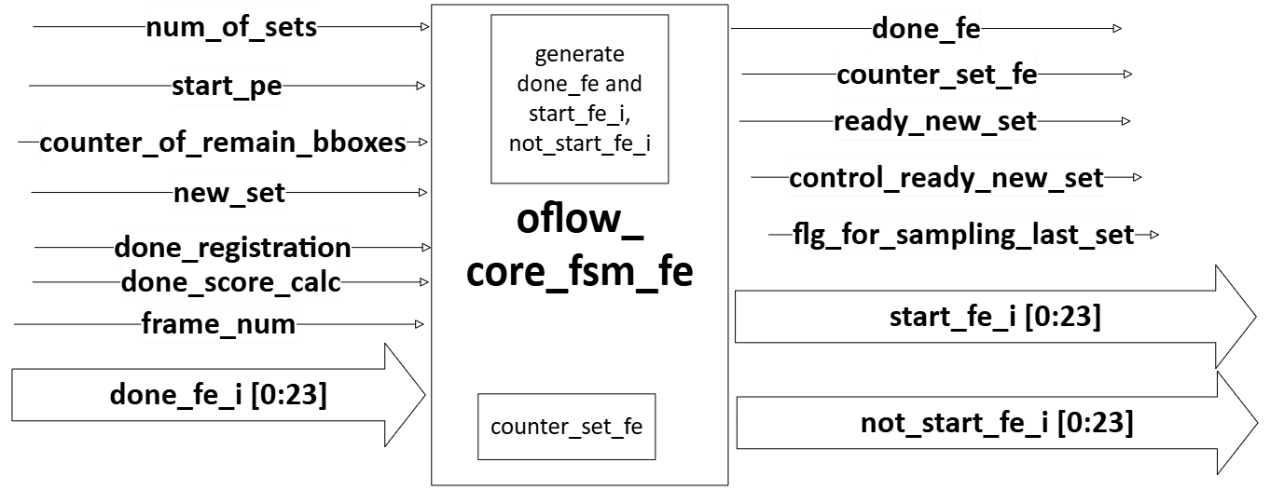


Figure 16: oflow\_core\_fsm\_fe - block diagram

The oflow\_core\_fsm\_fe module is responsible for managing the feature extraction (FE) phase of an optical flow system using a finite state machine (FSM).

* The module distributes the workload across multiple PEs, activating a subset of them based on the number of bounding boxes remaining.
* Manages synchronization signals (done\_fe, ready\_new\_set) to ensure proper progression to the next stage.

**oflow\_fsm\_core\_registration**

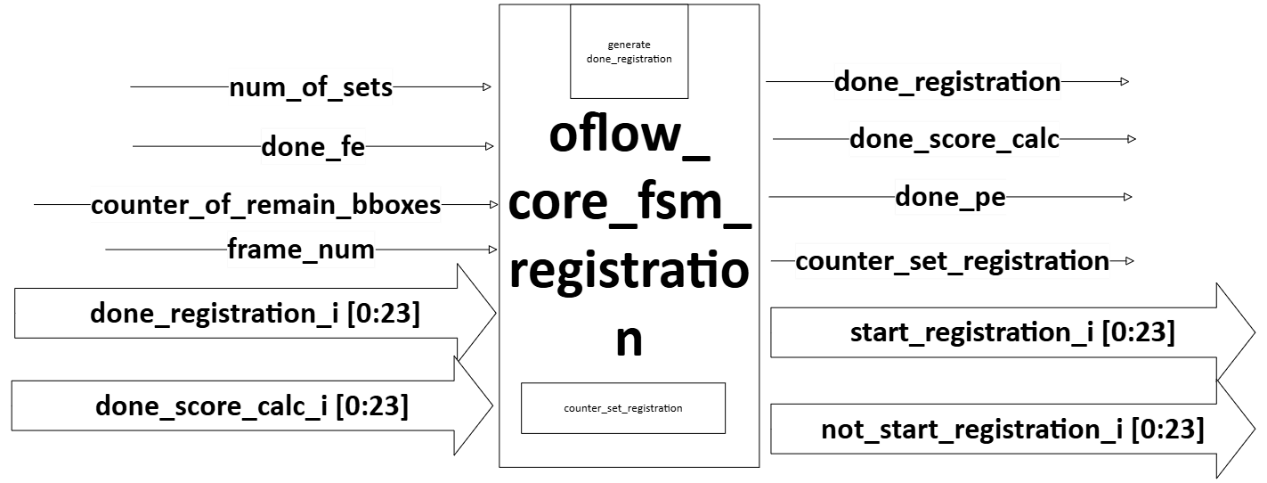


Figure 17: oflow\_core\_fsm\_registration - block diagram

The oflow\_core\_fsm\_registration module handles the registration and score calculation processes.

* Tracks the number of sets processed with a counter (counter\_set\_registration).
* Manages PE activation based on the number of bounding boxes remaining.
* Ensures that registration and score calculation are completed for all sets before progressing.

Overall, the module efficiently controls the registration and score calculation phases using a structured FSM to manage multiple sets and coordinate completion across PEs.

**oflow\_fsm\_core\_read**

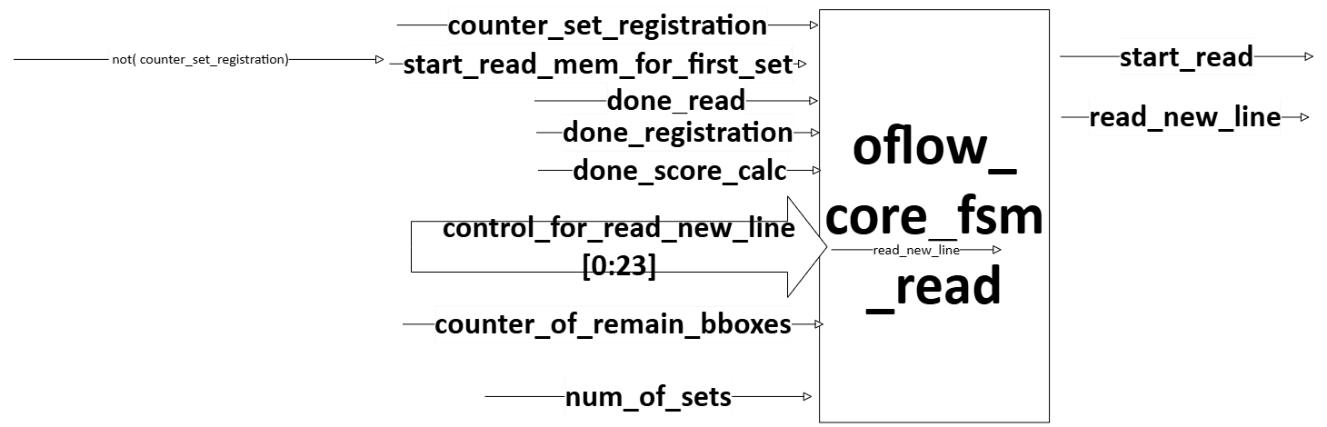
****

Figure 18: oflow\_core\_fsm\_read - block diagram

The oflow\_core\_fsm\_read module is a finite state machine (FSM) responsible for managing the memory read operations in an optical flow system. Its main roles include controlling the start and progression of memory reads, determining when to read new data lines, and coordinating with other FSMs involved in registration.

Functionality:

* The module coordinates memory reads based on the registration.
* It manages transitions between reading data lines and waiting for registration to complete.
* The state machine tracks the number of sets processed using a counter (counter\_set\_registration) and ensures the process continues until all sets are read.

Overall, this module efficiently controls memory read operations, synchronizing data access with other core processes in the system.

**oflow\_fsm\_core\_write**

**A white and black background with black text

Description automatically generated**

Figure 19: oflow\_core\_fsm\_write - block diagram

The oflow\_core\_fsm\_write module is a finite state machine (FSM) that manages the writing process in an optical flow system. It coordinates the selection of rows (each row represents different set) and processing elements (PEs) for writing data to the memory.

* The FSM processes bounding boxes in groups of 4 (because 2 PEs are written together to one row and the writing is to two rows – dual port sram), iterating through rows and PEs.
* It manages transitions between PEs, ensuring each PE streams out the appropriate portion of the data.
* It also handles cases where the last set of bounding boxes does not perfectly divide by 4, adjusting the state machine to process the remaining BBoxes.
* The module outputs control signals (ready\_from\_core, row\_sel, pe\_sel, and remainder) to coordinate writing with the memory buffer.

In summary, this module orchestrates the writing of bounding box data (features + id) into memory, ensuring proper distribution across rows and PEs while handling cases where the number of bounding boxes doesn't perfectly align with the PEs.

### 2.6.2 Registration

**Block diagram**

Figure 20: oflow\_registration - block diagram

**Block description (+flow-chart)**

The oflow\_registration module is a core component of the optical flow system that manages the registration (labeling) process by handling data flow, score calculation, and interaction between feature extraction, memory buffers, and scoreboards. This module is responsible for coordinating various elements such as feature extraction data, score calculation logic, and memory updates to track object registration across frames.

**Submodule Interactions:**

The oflow\_registration module instantiates and coordinates several submodules, each playing a distinct role:

1. **oflow\_score\_calc:** This submodule calculates similarity scores between current and previously feature extraction data. It compares these scores to find the minimum scores and outputs the results (min\_score\_0, min\_id\_0, etc.).
2. **oflow\_score\_board:** This submodule keeps track of the best-matching scores and their corresponding object IDs. It also communicates with the CR to update object registration information and buffer IDs.
3. **oflow\_registration\_fsm:** This FSM orchestrates the overall registration process, managing the start and stop conditions for score calculation, scoreboarding, and feature extraction.
4. **oflow\_registration\_feature\_extraction\_reg\_sb:** Handles feature extraction data by storing the current BBox features and registering the extracted data to feed it into the memory for subsequent calculations.

**Summary of Operation:**

The oflow\_registration.sv module coordinates the optical flow registration process by interacting with various modules, each responsible for score calculation, feature extraction, and memory management. It synchronizes feature extraction data with the score calculation logic, updates the score board, and outputs the final registration results for each BBox in the current frame. The FSM plays a key role in orchestrating this process, ensuring that registration happen smoothly across multiple frames and data sets.

**Pins description**

|  |  |  |  |
| --- | --- | --- | --- |
| Signal\_Name | Type | Width | Description |
| cm\_concate\_cur | I | 22 | Concatenated feature data of the current frame.  (TBD in oflow\_feature\_extraction) |
| position\_concate\_cur | I | 44 | Concatenated position (X\_TL, Y\_TL, X\_BR, Y\_BR) of the bounding box in the current frame. |
| width\_cur | I | 8 | Width of the bounding box in the current frame. |
| height\_cur | I | 8 | Height of the bounding box in the current frame. |
| color1\_cur | I | 24 | RGB color data of the bounding box (object) in the current frame. |
| color2\_cur | I | 24 | RGB color data of the bounding box (background) in the current frame. |
| done\_read | I | 1 | Signal indicating the end of the read operation from mem\_buffer (reading all the history frames from the mem\_buffer) |
| data\_to\_similarity\_metric\_0 | I | 145 | Concatenated feature data of the previous frame, including cm, position, width, height, color and history data. (left part of the row in the mem\_buffer – 1 BBox) |
| data\_to\_similarity\_metric\_1 | I | 145 | Concatenated feature data of the previous frame, including cm, position, width, height, color and history data. (right part of the row in the mem\_buffer – 1 BBox) |
| control\_for\_read\_new\_line | O | 1 | Control signal to oflow\_core\_fsm\_read to start reading a new line of data. This signal is asserted to '1' two cycles before done similarity metric to prepare new line of data to be ready for the next similarity metric calculation. |
| iou\_weight | I | 10 | Weight for the IoU metric in the final similarity score calculation. |
| w\_weight | I | 10 | Weight for the width difference metric in the final similarity score calculation. |
| h\_weight | I | 10 | Weight for the height difference metric in the final similarity score calculation. |
| color1\_weight | I | 10 | Weight for the first color channel difference metric in the final similarity score calculation. |
| color2\_weight | I | 10 | Weight for the second color channel difference metric in the final similarity score calculation. |
| dhistory\_weight | I | 10 | Weight for the d\_history\_metric in the final similarity score calculation. |
| id\_out | O | 12x11 | Output array of IDs from the score board |
| ready\_new\_frame | I | 1 | Indicates the Glue\_Logic that the accelerator is ready to receive a new frame from DMA. |
| row\_sel\_to\_pe | I | 4 | Row selection signal for PE, comes from oflow\_core\_fsm\_write. |
| frame\_num | I | 8 | The serial number of the current frame. |
| ready\_new\_set | I | 1 | Indicates the Glue\_Logic that the accelerator is ready to receive a new set of bounding boxes from DMA. |
| flg\_for\_sampling\_last\_set | I | 1 | Flag indicating if the last set should be sampled. (because there isn’t ready\_new\_set in the last set). |
| num\_of\_sets | I | 4 | Total Number of data sets to process in each frame. |
| done\_fe | I | 1 | Indicates the completion of feature extraction.  (stays on ‘1’ until new start\_fe). |
| start\_registration | I | 1 | Signal to start registration process |
| not\_start\_registration | I | 1 | Signal indicating to not start object registration in the specific PE (only in last set). |
| done\_registration | O | 1 | Indicates the completion of object registration. |
| done\_score\_calc | O | 1 | Indicates the completion of score calculation. |
| num\_of\_pe | I | 5 | The serial number of the current PE. |
| data\_out\_pe | O | 142 | Data output from PE for writing to memory. (without d\_history) (concatenates 2 pes data to 1 row) |
| row\_sel\_to\_pe\_from\_cr | I | 4 | Row selection signal from conflict resolution unit. (for fill\_hist) |
| write\_to\_pointer\_to\_pe | I | 1 | Write enable signal for pointer in score board that need to change to resolve conflict. |
| data\_from\_cr\_pointer\_to\_pe | I | 1 | Data from conflict resolution unit for writing pointer in score board that need to change to resolve conflict. |
| row\_to\_change\_to\_pe | I | 4 | Row selection signal for changing score board data when there is a conflict / new id. |
| write\_to\_id\_to\_pe | I | 1 | Write enable signal for ID in score board that need to change to set as a new BBox. |
| data\_from\_cr\_id\_to\_pe | I | 12 | Data from conflict resolution unit for writing ID in score board that need to change to set as a new BBox. |
| score\_to\_cr\_from\_pe | O | 32 | Score output from PE to conflict resolution unit. |
| id\_to\_cr\_from\_pe | O | 12 | ID output from PE to conflict resolution unit. |

Table 7: oflow\_registration - pins description

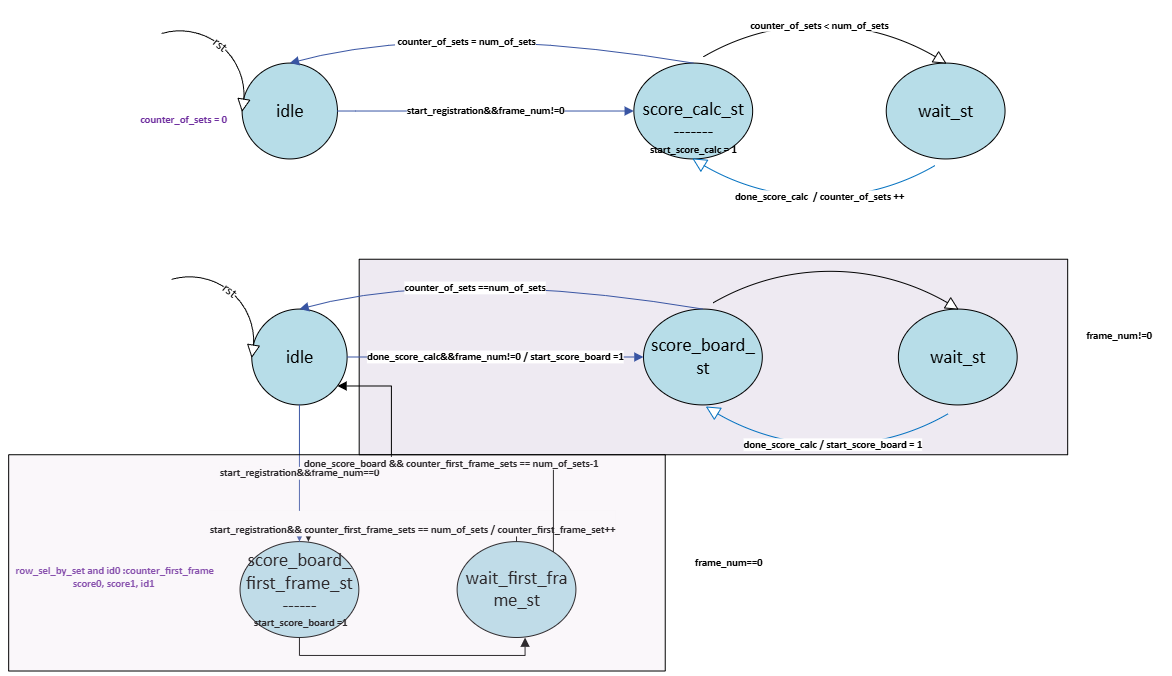
**FSM**

Figure 21: oflow\_registration - FSM

The oflow\_registration\_fsm is responsible for orchestrating the registration process. This FSM interacts with score calculation, scoreboarding, and in a multi-set environment, particularly during the registration of BBoxes across frames.

**Internal Logic:**

* **Counters (counter\_of\_sets, counter\_first\_frame\_sets):** These counters track the sets being processed during registration. Depending on whether it's the first frame or not, either counter\_first\_frame\_sets or counter\_of\_sets is used to control the row selection for the scoreboard.
  + row\_sel\_by\_set: Chooses the row based on the current frame. For subsequent frames (frame\_num != 0), counter\_of\_sets is used; otherwise, counter\_first\_frame\_sets is employed. This signal is for writing to the score\_board in the appropriate register.
  + id\_first\_frame: Computes the IDs for the first frame BBoxes using the number of PEs and the current set.

**Instantiated Modules:**

1. **oflow\_registration\_fsm\_score\_board:**

The oflow\_registration\_fsm\_score\_board is a subcomponent of the overall registration FSM and it specifically manages interactions with the scoreboard during the registration process. The module handles the transition between states, controls when the scoreboard updates, and manages the sets of frames, especially focusing on registration during both the first frame and subsequent frames.

1. **oflow\_registration\_fsm\_score\_calc:**

The oflow\_registration\_fsm\_score\_calc is a submodule within the larger oflow\_registration\_fsm design. Its role is to manage the FSM that controls the score calculation process during the registration phase. This module determines when the score calculation should start and incrementally tracks the sets being processed.

### 2.6.3 Conflict\_Resolve

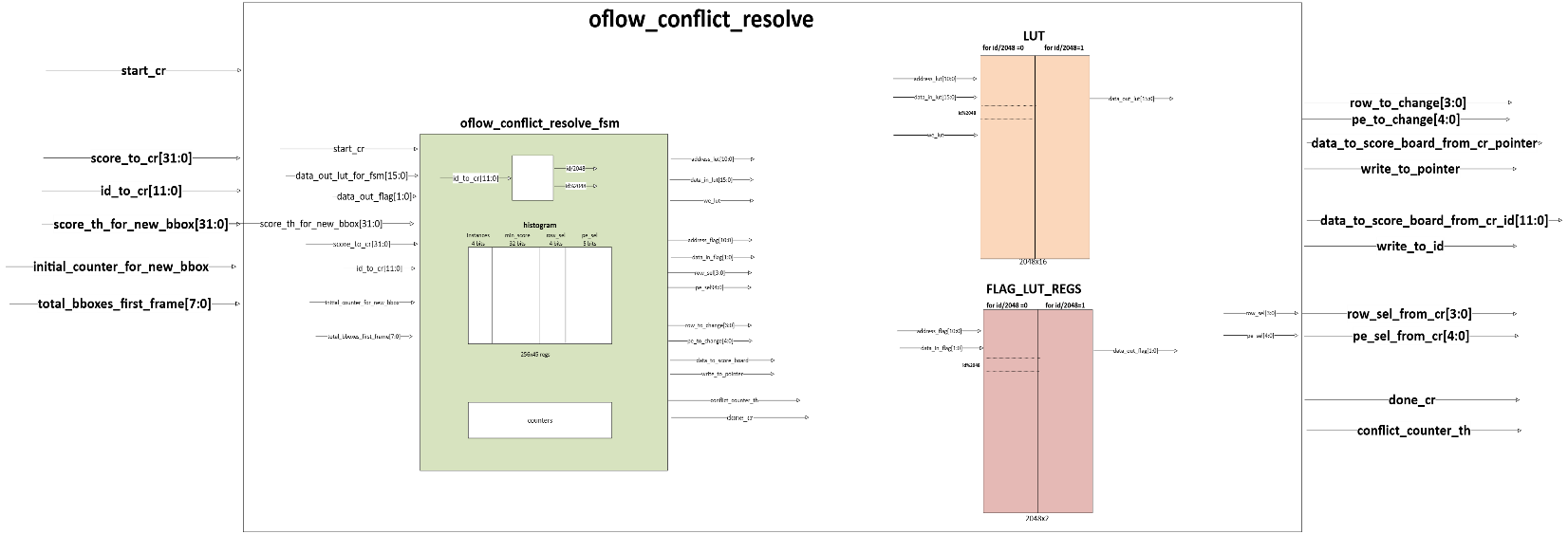
**Block diagram**

Figure 22: oflow\_conflict\_resolve - block diagram

**Block description (+flow-chart)**

**Module Overview:**

The oflow\_conflict\_resolve module is designed to handle conflict resolution in an object registration hardware accelerator. Below is a description of the main features and functionalities:

The oflow\_conflict\_resolve module plays a critical role in managing conflicts that arise during the processing of BBoxes data. It interfaces with various components, such as a scoreboard and a LUT, to resolve conflicts between multiple BBoxes and ensure correct data handling.

**Features:**

1. **Lookup Table (LUT) Management:**
   * A built-in LUT is used to store temporary data related to conflict resolve. The module reads and writes to the LUT using signals such as data\_out\_lut\_for\_fsm, address\_lut, data\_in\_lut, and we\_lut.
   * The LUT addresses represent the ids of the BBoxes and the values in it represent the addresses in the histogram that count the instances of this ids in the current frame. For example: all the instances of id = 12 will be counted in the histogram at address ‘x’, therefore in the LUT at address 12 the value is ‘x’.
2. **Scoreboard Interface:**
   * The module interacts with the scoreboard, receiving scores (score\_to\_cr) and IDs (id\_to\_cr) to determine which bounding box data is involved in conflicts.
   * It provides control signals (row\_sel\_from\_cr, pe\_sel\_from\_cr, row\_to\_change, pe\_to\_change, etc.) to modify the scoreboard entries, ensuring that conflicting bounding boxes are handled correctly.
   * The module writes data back to the scoreboard, managing both pointer updates (write\_to\_pointer, in case of conflict) and ID updates (write\_to\_id, in case of new BBox) as part of the conflict resolution process.
3. **New Bounding Box (BBox) Processing:**
   * The module receives threshold values for new bounding boxes (score\_th\_for\_new\_bbox) and tracks counters (initial\_counter\_for\_new\_bbox) and total bounding boxes (total\_bboxes\_first\_frame) from the first frame of data.
   * These inputs ensure that new boxes are properly integrated into the processing pipeline.
4. **Flag Registers:**
   * The module employs flag registers to keep track of state information during conflict resolution. The flag register is reset when conflict resolve begins and is updated based on LUT writes (we\_lut).
5. **Conflict\_counter\_th:**
   * When the unit more than threshold value of conflicts, it arises a flag to indicate that the number of conflicts is over the threshold and the oflow\_core\_fsm\_top will jump to the idle state and the process is reset (frame\_num 🡪 0).

**Instantiations:**

1. **oflow\_conflict\_resolve\_fsm:**
   * A state machine module handles the core conflict resolution process, controlling the interactions with the scoreboard, LUT, and flag registers.
   * It operates based on the provided input signals, resolving conflicts and communicating the results via the scoreboard interface.
2. **Dual-Port RAM:**
   * The dual-port RAM is instantiated to provide LUT functionality, enabling the module to store and retrieve conflict resolution data.
   * The RAM is read from and written to as needed during conflict resolution, with proper control signals (CEB, WEB, CSB, OEB) managing access to the memory.

**Applications:**

This module is essential in scenarios where multiple BBoxes have the same labeling during real-time object registration processes. The conflict resolve mechanism ensures that data consistency is maintained until order two.

**Pins description**

|  |  |  |  |
| --- | --- | --- | --- |
| Signal\_Name | Type | Width | Description |
| start\_cr | I | 1 | Start signal for the conflict resolve process. |
| done\_cr | O | 1 | Indicates the completion of the conflict resolve process. |
| score\_th\_for\_new\_bbox | I | 32 | Score threshold for setting BBox as a new one (from the reg\_file). |
| initial\_counter\_for\_new\_bbox | I | 1 | Indicates that Initialization of the counter for the new bounding box is needed. (only in frame\_num = 0) |
| total\_bboxes\_first\_frame | I | 8 | Total number of bounding boxes in the first frame. |
| score\_to\_cr | I | 32 | Score output from PE to conflict resolution unit. |
| id\_to\_cr | I | 12 | ID output from PE to conflict resolution unit. |
| row\_sel\_from\_cr | O | 4 | Row selection signal from conflict resolution unit. (for fill\_hist) |
| pe\_sel\_from\_cr | O | 5 | PE selection signal from conflict resolve unit (for fill\_hist) for reading from score board and insert the data into cr. |
| row\_to\_change | O | 4 | Row selection signal for changing score board data when there is a conflict / new id. |
| pe\_to\_change | O | 5 | PE selection signal for changing score board data when there is a conflict / new id. |
| data\_to\_score\_board\_ from\_cr\_pointer | O | 1 | Data from conflict resolution unit for writing pointer in score board that need to change to resolve conflict. |
| write\_to\_pointer | O | 1 | Write enable signal for pointer in score board that need to change to resolve conflict. |
| data\_to\_score\_board\_ from\_cr\_id | O | 12 | Data from conflict resolution unit for writing ID in score board that need to change to set as a new BBox. |
| write\_to\_id | O | 1 | Write enable signal for ID in score board that need to change to set as a new BBox. |
| conflict\_counter\_th | O | 1 | Signal indicating that the number of conflicts has been reached the threshold. |

**FSM**

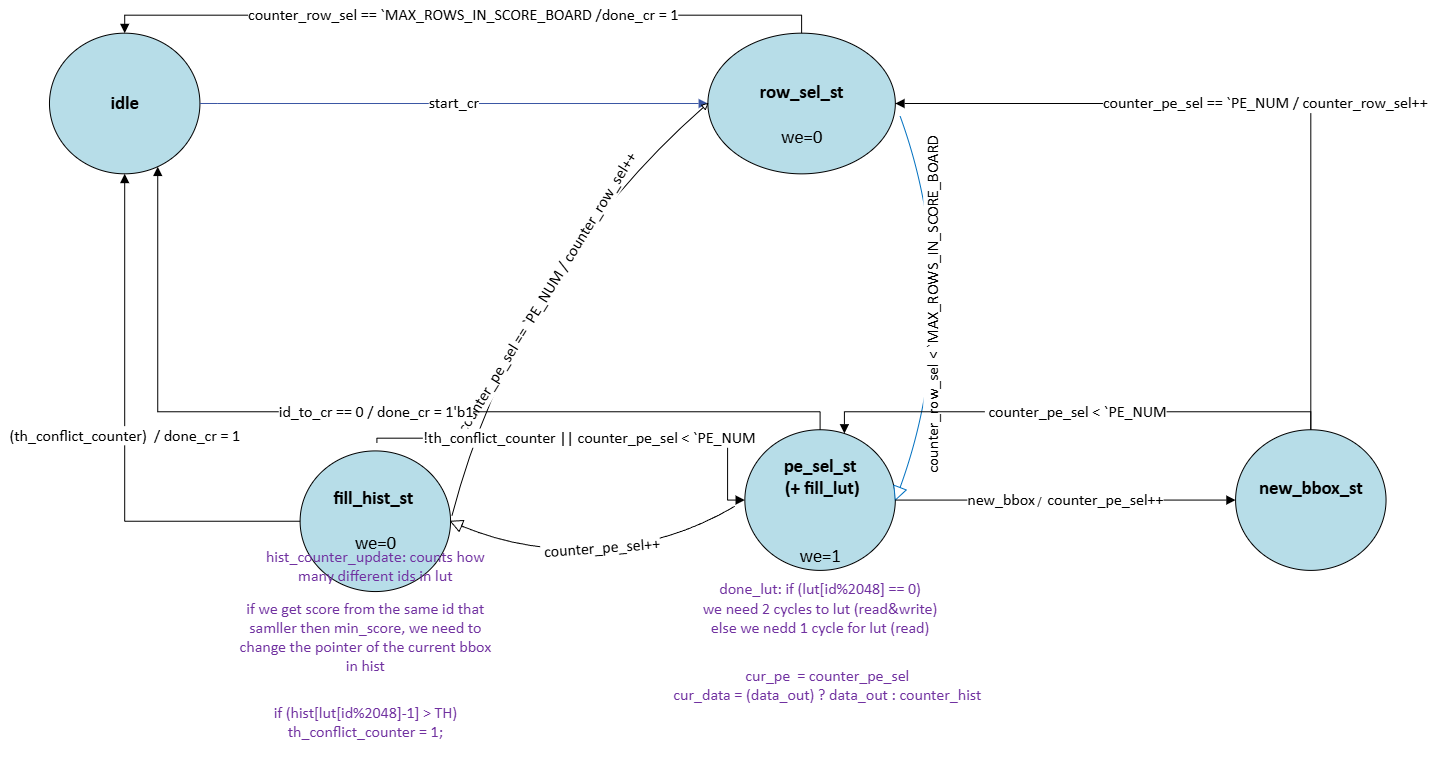


Figure 21: oflow\_conflict\_resolve - FSM

oflow\_conflict\_resolve\_fsm is responsible for handling conflicts that arise when attempting to resolve the object registration between multiple bounding boxes. The module likely operates within a larger framework for object registration, where it interacts with scoreboards, and flags to handle incoming data related to BBoxes in frames. The FSM communicates with the scoreboard to track information such as the scores, IDs, and selections of the PEs and rows involved in the conflict resolve.

**Features of the FSM:**

1. **FSM:** The module operates with several states:
   * **idle\_st:** The module waits for the conflict resolve to start.
   * **row\_sel\_st:** Selects a row to read from the scoreboard.
   * **pe\_sel\_N\_fill\_lut\_st:** Selects a PE and fills the LUT with relevant data.
   * **fill\_hist\_st:** Updates the history registers based on the current state of the LUT and data and determines if conflicts exist.
   * **new\_bbox\_st:** Handles the insertion of new BBoxes.

The FSM checks if the score associated with the bounding box is above a threshold (score\_th\_for\_new\_bbox) and updating the relevant ids in the score\_board. If a conflict exceeds a defined threshold (MAX\_CONFLICTS\_TH), the conflict\_counter\_th is flagged, and the system moves back to the idle state.

### 2.6.4 oflow\_mem\_buffer\_wrapper

A screenshot of a computer

Description automatically generated**Block diagram**

Figure 24: oflow-Mem-Buffer-Wrapper - block diagram

**Block description (+flow-chart)**

The oflow\_mem\_buffer\_wrapper module is a wrapper designed to manage memory operations, integrating both memory buffer and FSM logic to control it. Below is a detailed description of its main components and functionality:

Functions:

1. **Memory Management**: This module interfaces with a memory buffer to store and retrieve data across multiple frames.
2. **Control Signals**:
   * The wrapper uses control signals (rnw\_st, start\_read, start\_write) to handle read and write operations based on the current processing state.
   * The control signals are coordinated with a FSM that synchronizes the memory read and write processes (done\_read, done\_write).
3. **Processing Element (PE) Interface**:
   * Write state: Data inputs from four processing elements (data\_in\_0, data\_in\_1) are accepted and processed.
   * Read state: Corresponding outputs (data\_out\_0, data\_out\_1) are extracted after interacting with the memory buffer.

Internal Logic:

* **Write Enable (WE) Control**:  
  The module determines when to write to memory using we signal, which is set based on the rnw\_st (read/write) signal and the readiness of the core FSM (ready\_from\_core).
* **Chip Select and Output Enable**:  
  Two chip select signals (csb\_0, csb\_1) control the selection of memory banks for reading or writing, with an output enable signal (oeb) controlling when data is driven onto the output bus.
* **Offset Calculations**:  
  The module handles separate offsets (offset\_0, offset\_1) for read and write operations, ensuring proper addressing during memory access.

Module Instantiations:

1. **Memory Buffer (oflow\_MEM\_buffer)**:  
   The module instantiates an oflow\_MEM\_buffer that manages actual data storage, interfacing with the memory using various control signals and data inputs/outputs.
2. **FSM for Memory Buffer Control (oflow\_fsm\_mem\_buffer\_in\_mem\_wrapper)**:  
   A FSM controls the memory operations within the wrapper, synchronizing read and write cycles, and generating the necessary offsets for memory access.

Usage:

This module is intended to be used in designs where efficient memory management for multi-frame object registration is required. It provides an interface for reading and writing data to memory, manages the memory addressing and timing.

This modular design ensures flexibility in handling various object registration tasks while maintaining synchronization with external control units.

This unit also maintains start and end pointers to read only the lines in use from the memory.

**Example of Read & Write Transaction**

1. **Initialization:**
   * Assume frame\_num = 0, num\_of\_history\_frames = 3, and the buffer is reset to zero.

The MEM will be divided into sections: pointers [0] = 0, pointers [1] = 42, pointers [2] = 84.

1. **Data Input:**
   * Input data values for writing (for demonstration purposes):
     + data\_in\_0 = 284'b10101010… (example input for port 0)
     + data\_in\_1 = 284'b11001100… (example input for port 1)
   * Address offsets: (offsets are updated by oflow\_fsm\_write\_buffer)
     + offset\_0 = 3
     + offset\_1 = 4
   * Write Enable:
     + we = 1 (indicating to perform write operation)
2. **Writing data:**
   * On the next clock edge, data will be written to the calculated addresses in the memory.
3. **Reading data:**
   * After the write operation, assume we signal is set to 0 (indicating to perform read operation).
   * The frame\_num gets frame\_num\_to\_read from oflow\_fsm\_buffer\_read and allows calculating which pointers to use based on the modulo operation with num\_of\_history\_frames.
   * For example, to perform a read operation after writing, based on offsets:
     + Calculated addresses would be:
       - addr\_0 = pointers [frame\_num % num\_of\_history\_frames] + offset\_0
       - addr\_1 = pointers [frame\_num % num\_of\_history\_frames] + offset\_1
   * The data can now be read from data\_out\_0 and data\_out\_1. (\*Only data\_out\_0 is used).
4. **Output:**
   * The output will return the values stored in the specified memory positions. After the write operation, the signals will be:
     + data\_out\_0 = 284'b10101010…
     + data\_out\_1 = 284'b11001100…

This example illustrates how the oflow\_MEM\_buffer module processes read and write operations based on the frame structure and input signals.

**Pins Description**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal\_Name** | **Type** | **Width** | **Description** |
| read\_new\_line | I | 1 | Indicates when a new line can be read after the similarity metric 2 cycles before finishes processing one line |
| start\_read | I | 1 | Signal to start reading data |
| start\_write | I | 1 | Signal to start writing data |
| data\_in\_0 | I | 284 | Data input from processing element (PE), will be written to port 0 of the mem  \_buffer |
| data\_in\_1 | I | 284 | Data input from processing element (PE), will be written to port 1 of the mem  \_buffer |
| frame\_num | I | 8 | Serial number of the current frame (0-255) |
| num\_of\_history\_frames | I | 3 | Number of history frames to be stored as fallback |
| num\_of\_bbox\_in\_frame | I | 8 | Indicates the end of the frame memory |
| rnw\_st | I | 1 | Read/Write control signal (1 = read, 0 = write) |
| ready\_from\_core | I | 1 | Ready signal from the core FSM indicating it is ready for new writing |
| done\_read | O | 1 | Indicates the completion of a read operation (reading all the rows in the relevant history frames) |
| done\_write | O | 1 | Indicates the completion of a write operation (writing all the BBoxes in the current frame) |
| data\_out\_0 | O | 284 | Data output to the processing element (PE), port 0 (for reading) |
| data\_out\_1 | O | 284 | Data output to the processing element (PE), port 1 (Not in use because each pe contains 2 similarity\_metric units and each row in memory contains 2 BBoxes, therefore it is enough to use only one port) |
| counter\_of\_history\_frame\_to\_interface | O | 3 | Counter indicating the current history frame being sent to the interface to calc its d\_history |

Table 8: Oflow-Mem-Buffer-wrapper - Pins Description

**FSM**

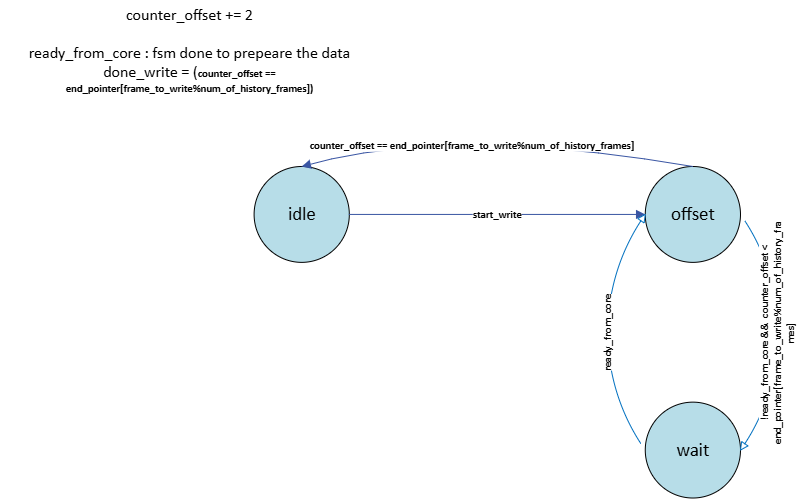
There are 2 FSMs to control the reading and writing to memory.

Each FSM contains 3 states.

The offset state is for generating the offsets to the mem\_buffer for creating the addresses.

In the write FSM, there is wait state to wait for ready\_from\_core.

In the read FSM, there is frame state to determine which history frame should be read.



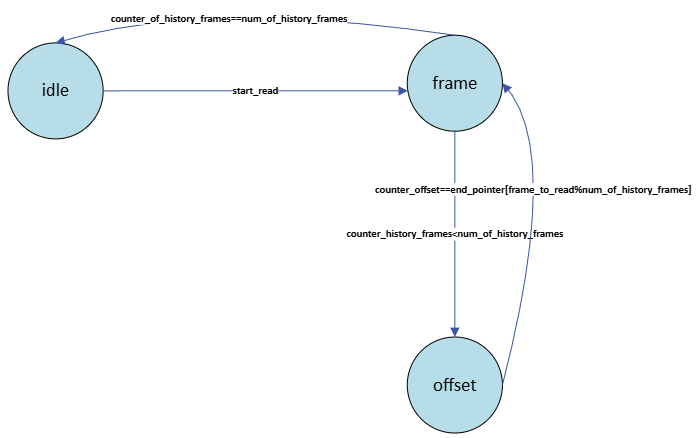


Figure 26: oflow\_mem\_buffer\_wrapper – FSM write

Figure 26: oflow\_mem\_buffer\_wrapper – FSM read

**Constraints of oflow\_MEM\_buffer\_wrapper**

* 1. There is a tradeoff between num\_of\_history\_frames and num of BBoxes in frame. The maximum product between them needs to be 256.

If the user chooses:

1)num of history frames = 1: num\_of\_BBoxes = 256

2)num of history frames = 2: num\_of\_BBoxes = 128

3)num of history frames = 3: num\_of\_BBoxes = 84

4)num of history frames = 4: num\_of\_BBoxes = 64

5)num of history frames = 5: num\_of\_BBoxes = 50

💡 **Explanation about fixed point representation:**[[1]](#footnote-1)

Verilog can generally synthesize addition, subtraction, and multiplication on an FPGA. It cannot synthesize division automatically, but it can multiply by fractional numbers, e.g. multiply by 0.1 instead of dividing by 10.

**Multiplication** works as expected too, but the product contains twice the number of bits. Multiplying two Q4.4 numbers results in a Q8.8 product:

0011.0100 3.2500

x 0010.0001 2.0625

The long multiplication can be done and will produce:

00000110.10110100 = 6.703125

It can be round this to the original Q4.4 format by taking the eight middle bits:

0000[0110.1011]0100 = 0110.1011 = 6.6875

The precision there is lost; this often happens when converting to the original precision after multiplication.

**Division** is less straightforward. It can’t be synthesized with regular Verilog unless it’s by a power of two, which uses a right shift. A right shift truncates the result, so the fractional part lost:

0111 7

>>1 right-shift 1 bit

0011 3

However, with fractional numbers, accurate division by a constant can be achieved using multiplication.

For example, instead of dividing by 2 the alternative way is multiplying by 0.5:

0111.1000 7.5000

x 0000.1000 0.5000

= 00000011.11000000 3.7500

Back in Q4.4: 0011.1100. In this case, the answer is accurate.

**Pins Description**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal\_Name** | **Type** | **Width** | **Description** |
| start | I | 1 | Start signal to initiate the similarity calculation. |
| cm\_concate\_cur | I | 22 | Concatenated feature data of the current frame.  (TBD in oflow\_feature\_extraction) |
| position\_concate\_cur | I | 44 | Concatenated position (X\_TL, Y\_TL, X\_BR, Y\_BR) of the bounding box in the current frame. |
| width\_cur | I | 8 | Width of the bounding box in the current frame. |
| height\_cur | I | 8 | Height of the bounding box in the current frame. |
| color1\_cur | I | 24 | RGB color data of the bounding box (object) in the current frame. |
| color2\_cur | I | 24 | RGB color data of the bounding box (background) in the current frame. |
| features\_of\_prev | I | 145 | Concatenated feature data of the previous frame, including cm, position, width, height, color and history data. |
| iou\_weight | I | 10 | Weight for the IoU metric in the final similarity score calculation. |
| w\_weight | I | 10 | Weight for the width difference metric in the final similarity score calculation. |
| h\_weight | I | 10 | Weight for the height difference metric in the final similarity score calculation. |
| color1\_weight | I | 10 | Weight for the first color channel difference metric in the final similarity score calculation. |
| color2\_weight | I | 10 | Weight for the second color channel difference metric in the final similarity score calculation. |
| dhistory\_weight | I | 10 | Weight for the d\_history\_metric in the final similarity score calculation. |
| valid | O | 1 | Signal indicating the validity of the similarity score output. Also indicates done similarity metric. |
| control\_for\_read\_new\_line | O | 1 | Control signal to oflow\_core\_fsm\_read to start reading a new line of data. This signal is asserted to '1' two cycles before done similarity metric to prepare new line of data to be ready for the next similarity metric calculation. |
| score | O | 32 | Final computed similarity metric score. |
| id | O | 12 | Identifier for the processed bounding box. |

Table 9: Oflow-Similarity-Metric - Pins Description

**Constraints of similarity\_metric**

1. The precision level of the score is 15 bits (for the integer part, and 17 bits for the fraction part.

In addition, 15 bits are chosen for the integer part because according to the calculations of the metrics, the maximum sum of the different metrics is ~1318.

For this:

iou\_metric\_pad = 1, w\_metric = 256 (q8.0), h\_metric = 256 (q8.0), color1\_metric = color\_2\_metric = 256+256+256 = 768,

history metric = 2^5 = 32.

More bits are added for safety.

1. In addition, the weights are represented with 10 bits. (q0.10).

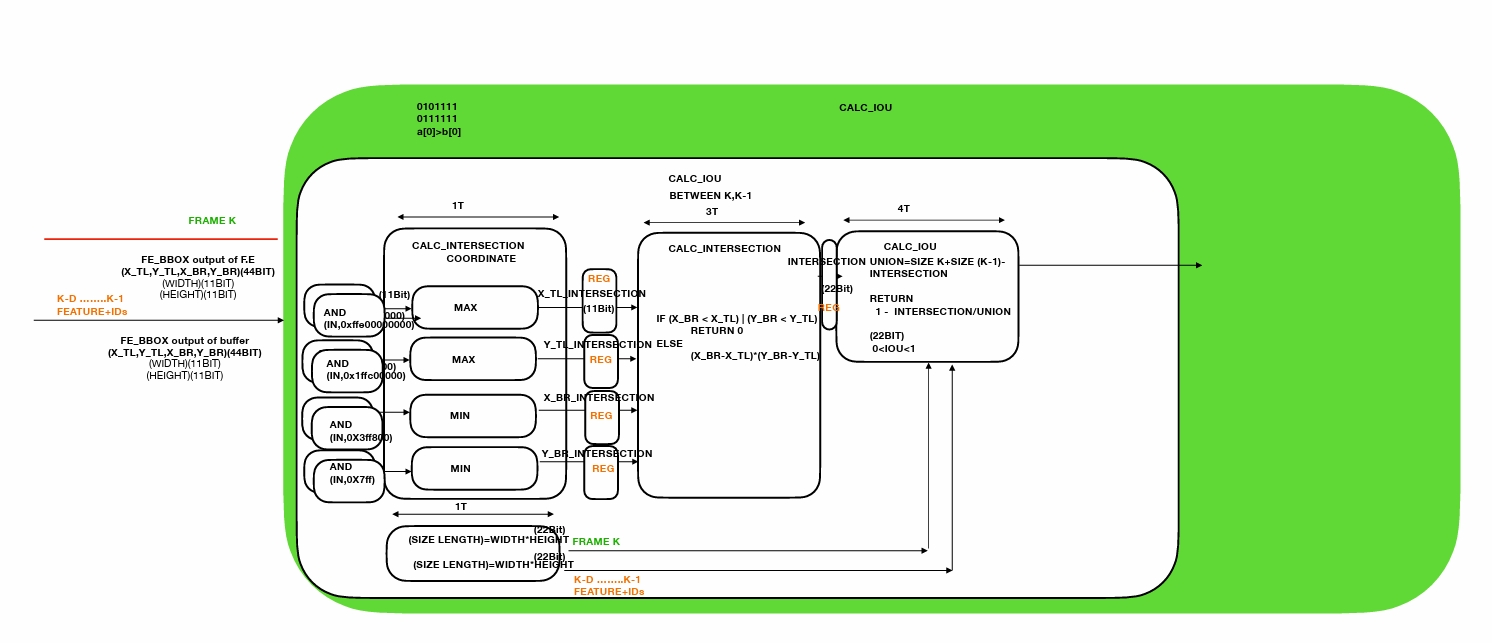
**miscellaneous: oflow\_calc\_iou**

Figure 27: oflow-calc-iou - Block Diagram

The oflow\_calc\_iou module is designed to calculate the Intersection over Union (IoU) metric between two bounding boxes. The IoU is a common metric in object detection and tracking, representing the overlap between two bounding boxes as a fraction of their combined area. Here's a breakdown of how the module works:

**Module Overview**

* **Inputs**:
  + bbox\_position\_frame\_k, bbox\_position\_frame\_history: The positions of the top-left (TL) and bottom-right (BR) corners of the bounding boxes for the current frame and a historical frame.
  + bbox\_w\_frame\_k, bbox\_h\_frame\_k: Width and height of the bounding box in the current frame.
  + bbox\_w\_frame\_history, bbox\_h\_frame\_history: Width and height of the bounding box in the historical frame.
* **Outputs**:
  + valid\_iou: Indicates when the IoU calculation is complete, and the result is valid.
  + iou: The calculated 1-IoU value.

**Internal Logic**

1. **State Machine**:
   * **States**:
     + idle\_st: The module waits for a start signal.
     + coordinate\_st: Calculates the intersection coordinates of the two bounding boxes.
     + intersection\_st: Calculates the area of the intersection between the two bounding boxes.
     + iou\_st: Calculates the 1-IoU using the intersection area and the areas of the individual bounding boxes (union area).
2. **Calculating Intersection Coordinates**:
   * In the coordinate\_st state, the module calculates the intersection coordinates:
     + x\_tl\_intersection and y\_tl\_intersection signals are the maximum of the top-left coordinates of the two bounding boxes.
     + x\_br\_intersection and y\_br\_intersection signals are the minimum of the bottom-right coordinates of the two bounding boxes.
3. **Calculating Intersection Area**:
   * In the intersection\_area\_st state:
     + If the bottom-right coordinates are less than the top-left coordinates, there is no intersection, and the area is set to 0. For example: (x\_br\_min<x\_tl\_max 🡪 no overlap)

A white square with red and green squares

Description automatically generated

X\_TL\_max

X\_BR\_min

\_mi

* + - Otherwise, the intersection area is calculated as the product of the width and height of the intersection area.

1. **Calculating IoU**:
   * In the iou\_st state:
     + temp\_iou= Intersection / (Area of Box 1+Area of Box 2−Intersection)
     + The iou is 1-temp\_IoU
     + The result is adjusted for fixed-point representation, with the final value stored in the iou output signal.
2. **Counters and Timing**:
   * The module uses a counter to control the timing of the state transitions and ensure that the calculations are completed over multiple clock cycles.
   * The valid\_iou signal is asserted once the IoU calculation is complete, signaling that the result is ready.

**Special IP’s that is used in calc iou:**

DW\_div\_seq is used to divide: (intersection\*)/union.

The next parameters and controlled signals are set to:

a\_width (`INTERSECTION\*2),

b\_width (`INTERSECTION),

hold(1'b0).

💡 **Explanation about division in IoU:**[[2]](#footnote-2)

In this module, it is required to divide the intersection over union for the iou and this result is less than 1 because intersection is always less than union.

If the intersection over union is divided, simply with ‘/’ operation or div IP module that returns integer and remainder, this won't work.

For example: 5/7 and 5/9 will yield the same result, and thus it won't be able to distinguish between them and choose the higher iou.

It is necessary want to distinguish between these results, and therefore different calculations are used.

Explanation:

The number was represented by q0.22 bit for better precision.

* + 1. First, the dividend was scaled up (intersection value) by 22 bits (because this is the width of it and of divider), and the result is 44 bits which the upper 22 bits are for the integer and the others for the fraction.
    2. Next, it was divided by the divider (union value, 22 bits length) The result is 22 upper bits which are equal 0 (cause 2^22 multiply by fraction<1 will always be < 2^22)
    3. Now the fraction part which is the 22 bottom bits contain the results is taken. (In decimal it should be scaled to get a better precision. 5/7 = 0.71428.., but it can be calculated it by: (5\*100)/7 = 71.4285(and take the integer fraction), as the scale increase, so does the accuracy).
    4. The last step is to subtract 1(represent by 0.99 which is q0.22={22{1’b1}}) by the results from section 3. And the received result is 1-iou (because the goal is evaluating the score by the minimum and not by the maximum).

Let’s simplify this by example, 5/7= **0.7142857143**:

1. q44.0
2. . close to **0. 7142857143**.

**Examples of IoU:**

**A screenshot of a computer

Description automatically generated**

Figure 28: Calc-Iou - IoU Examples

In the next figure, It can be seen the meaning of CM,TL,BR.

X\_TL, Y\_TL

X\_BR, Y\_BR

X\_CM, Y\_CM

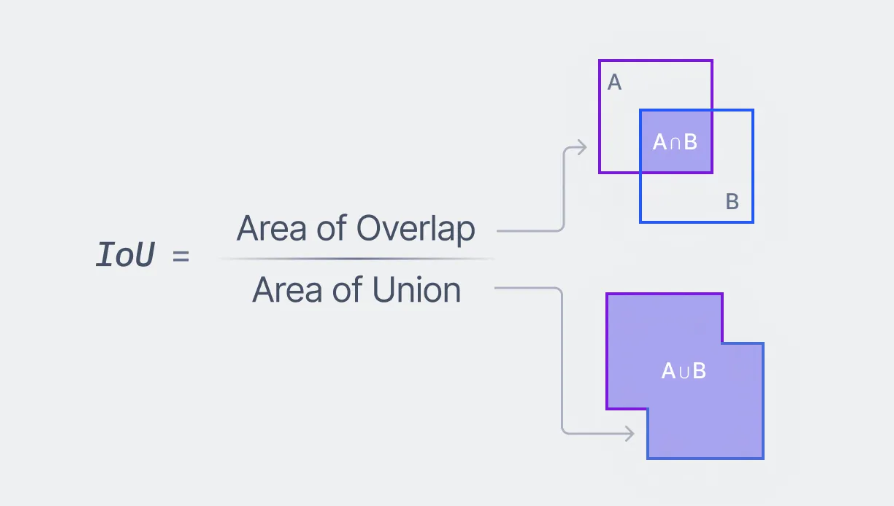


Figure 29: oflow-Calc-Iou - IoU formula

## A book with text on it Description automatically generated 2.7. Programmer’s Guide

The initial step is to update the Reg-File unit.

The user needs to insert to this unit by the APB protocol the parameters:

* + - * Weights of the similarity metrics
      * Threshold value for the score that above it the BBox will be defined as a new BBox
      * Num of history frames: The user can choose how many frames to store in the history.

(There is a tradeoff between this number and the maximum number of BBoxes per frame)

# 3. Zero-order ("aliveness") verification

## 3.1. Test-Plan and Test-Results oflow\_top

|  |  |  |
| --- | --- | --- |
| **Test name** | **Description & Purpose** | **Inputs** |
| **1:** Multiple frames with conflicts under and over the threshold value and not full sets (Number of BBox in the last is less than 24) | Simulate several frames with multiple BBoxes, ensuring that the system maintains proper functionality like managing the conflicts.  The purpose is to test the accelerator’s ability to handle continuous registration, especially the conflict\_resolve over multiple frames with multiple BBoxes. | Frame 0: 72 BBoxes (3 full sets).  Frame 1: 70 BBoxes (3 sets) so there will be less than 10 conflicts in this frame.  Frame 2: 70 BBoxes (3 sets) – 6 BBoxes from each of the two first sets will be the most similar to a specific BBox from previous frame so there will be more than 10 conflicts.  Frame 3: 24 BBoxes (1 set) |
| 2: Multiple frames with new BBoxes to labeling and conflicts |  |  |
|  |  |  |

|  |  |  |
| --- | --- | --- |
| **Test name** | **Expected Outputs** | **Pass Criteria** |
| **1:** Multiple frames with conflicts under and over the threshold value and not full sets (Number of BBox in the last is less than 24) | IDs: Frame 0 – the IDs are expected to be in ascending order (1 🡪 72)  Frame 1 – the IDs of BBoxes that are similar to BBoxes in frame 0 need to be with the same ID and also the BBoxes which have conflicts need to be replaced to the second ID.  conflict\_counter\_th: In frame 2 there are more than 10 conflicts and therefore this signal should be raised, and the next frame need to be reset to frame\_num=0 | Correct transition between the states of the fsm\_core\_top.  Frame 0: idle -> set\_variables -> pe\_st -> write\_st ->  Frame 1: idle -> set\_variables -> pe\_st -> cr\_st -> write\_st  Frame 2: idle -> set\_variables -> pe\_st -> cr\_st |
| 2: Multiple frames with new BBoxes to labeling and conflicts |  |  |
|  |  |  |

Table 10: oflow\_top - test plan

## 3.2. Test-Plan and Test-Results oflow\_registration

|  |  |  |
| --- | --- | --- |
| **Test name** | **Expected Outputs** | **Pass Criteria** |
| **1:** Multiple frames with conflicts under and over the threshold value and not full sets (Number of BBox in the last is less than 24) | Min\_score\_0 & id\_0, min\_score\_1 & id\_1: For specific PE, For each set in frame 1 or above, these outputs need to match to the BBox who’s the most similar to the BBox in this PE.  done read: need to be raised after reading of all the mem\_buffer.  ids\_out: correct ids for specific PE | In this test the focus will be in PE 2 which expected to change the ids from 3->27-> |
| 2: Multiple frames with new BBoxes to labeling and conflicts |  |  |
|  |  |  |

## 3.3. Test-Plan and Test-Results Conflict\_Resolve

**A screenshot of a computer screen

Description automatically generated**

Figure 33: Test result – oflow-Mem-Buffer - Write transaction

A screen shot of a computer

Description automatically generated

Figure 34: Test result – oflow-Mem-Buffer - Read transaction

Here is the read stage to the oflow\_MEM\_buffer.

First, all the desired signals are ready for the negedge clk.

At marker “read1”: address\_0 = 42, csb\_0 = 0 (for activate the memory), web\_0 = 1 (to read) and oeb\_0 = 0 (need to read).

Then in the posedge clk, data out will be ready (=77) as expected.

The next addresses will be read in the same way, and as expected data\_out = 88,99,85.

## 3.4. Test-Plan and Test-Results oflow\_mem\_buffer\_wrapper

|  |  |  |  |
| --- | --- | --- | --- |
| decimal | bits\_width | variable | frame |
| 50 | 11 | x | Current frame BBox |
| 10 | 11 | y |
| {30,55} | 22 | cm\_concate |
| {50,10,60,110} | 44 | position\_concate |
| 10 | 8 | width |
| 100 | 8 | height |
| 128 | 8 | color1-R |
| 127 | 8 | color1-G |
| 78 | 8 | color1-B |
| 204 | 8 | color2-R |
| 205 | 8 | color2-G |
| 209 | 24 | color2-B |
| 52 | 11 | x | Past frame BBox |
| 8 | 11 | y |
| {31,54} | 22 | cm\_concate |
| {52,8,62,108} | 44 | position\_concate |
| 10 | 8 | width |
| 100 | 8 | height |
| 130 |  | color1-R |
| 122 |  | color1-G |
| 90 |  | color1-B |
| 220 |  | color2-R |
| 80 | 24 | color2-G |
| 200 | 24 | color2-B |
| 1 | 3 | history |
| 12 | 12 | id |
|  |  |  |  |
| 52 | 11 | X\_TL\_MAX | calculations |
| 10 | 11 | Y\_TL\_MAX |
| 60 | 11 | X\_BR\_MIN |
| 108 | 11 | Y\_BR\_MIN |
| 784 |  | INTERSECTION |
|  |  |  |
| 1216 |  | UNION |
| 0.355263158 | 22(q0.22) | iou\_metric |
| 0.354492188 | 22(q0.10) | iou\_metric\_pad/truncate |
| 0 | 8(q8.0) | w\_metric |
| 0 | 8(q8.0) | h\_metric |
| 19 | 24(q24.0) | color1\_metric |
| 150 | 24(q24.0) | color2\_metric |
| 2 | 6(q6.0) | history\_metric |
| 0.5 | 10(q0.10) | iou\_weight |
| 0.125 | 10(q0.10) | w\_weight |
| 0.125 | 10(q0.10) | h\_weight |
| 0.083 | 10(q0.10) | color1\_weight |
| 0.083 | 10(q0.10) | color2\_weight |
| 0.083 | 10(q0.10) | history\_weight |
| 14.37158203 | 44(q26.20) | avg\_similarity\_metric |



Table 11: Oflow-Similarity-Metric with overlap - Test Plan

* A screen shot of a computer

  Description automatically generatedExample of similarity\_metric calculaion between BBox in the current frame with BBox in the previous frame **without overlap** :

Figure 37: Test result – oflow-Similarity-Metric -Without overlap case - Inputs

Now the expected results should yield higher score because all the features of prev BBox are the same, execpt of x\_tl which bigger than x\_br of the current BBoxe and therfore there isn't overlap between the bounding boxes and thus the iou\_metric will be higher than the score with overlap.

A screenshot of a computer

Description automatically generated

Figure 38: Test result - Similarity-Metric -Without overlap case - Outputs



decimal

Table 12: Oflow-Similarity-Metric without overlap - Test Plan

In this example (wo overlap), even though the score was truncated by 3 bits from the fractional part the error between score and similarity\_metric\_avg. is still 0.

Pay attention that the IOU metric has the largest weight.

Why? Cause when 2 BBoxes are compared, one from the current frame and one from the past frame. These 2 BBoxes can have similar color (for example soccer player of the same group) and close x, y coordinate, but they don’t share any intersection between each other, which means the BBox from the past doesn’t represent the current BBox.

**Calc Iou**

* **With overlap:**

These features position\_concate, width and height were inserted, and yield overlap. It can be seen that temp\_iou is not 0, and thus the iou (1 – temp\_iou) is less than 1 (intersection < union 🡪 (intersection/union) < 1).

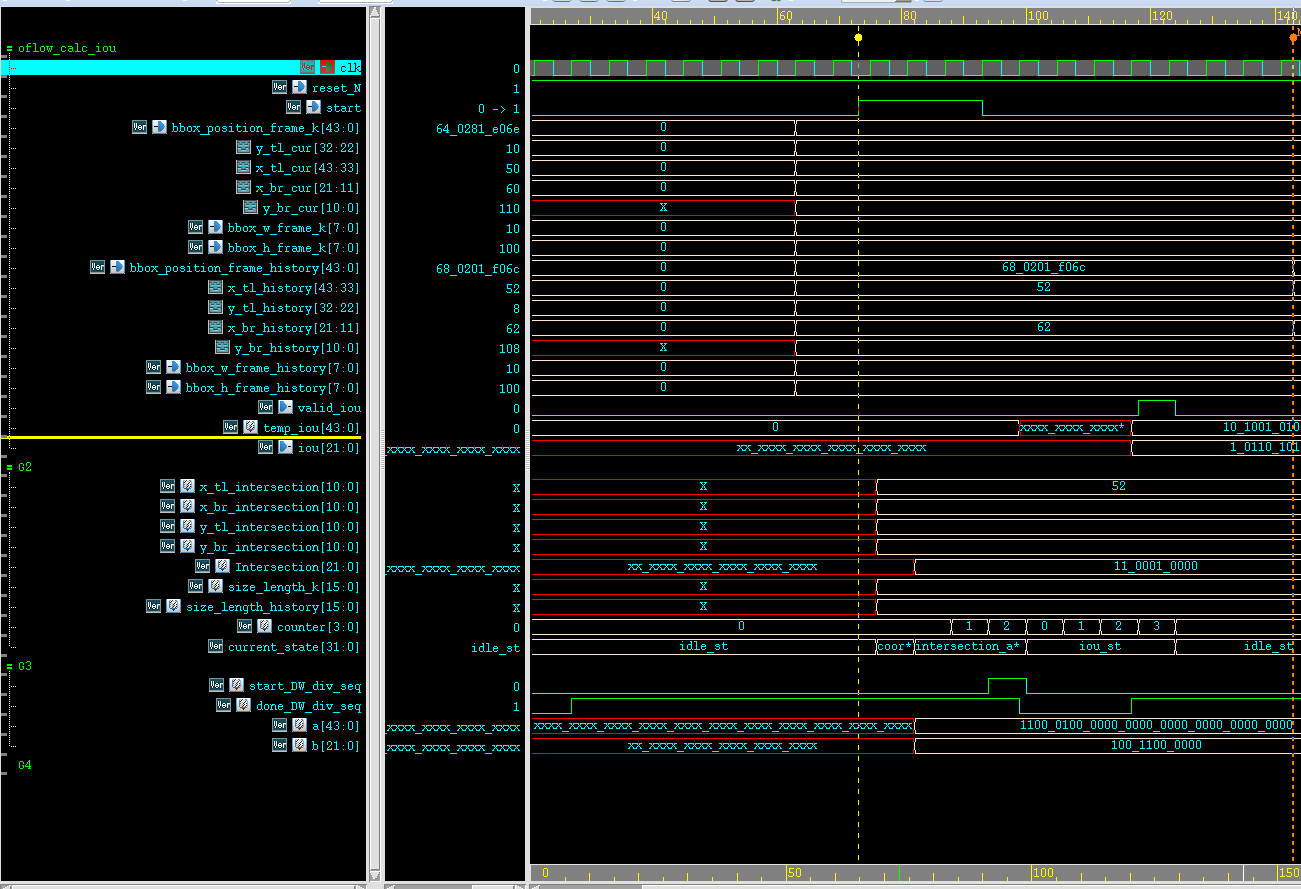


Figure 39: Test result – oflow-Similarity-Metric - calc iou- With overlap case



decimal

Table 13: Oflow-Calc-Iou with overlap - Test Plan



There is a minor error of 4.59081E-05 % between the expected iou to the simulation iou. This is the result of the 22 bits representation of the iou output.

* **Without overlap**:

The features position\_concate, width, height that were inserted here won’t yield overlap. It can be seen that temp\_iou is 0, and thus the iou that is (1 – temp\_iou) is 1 .

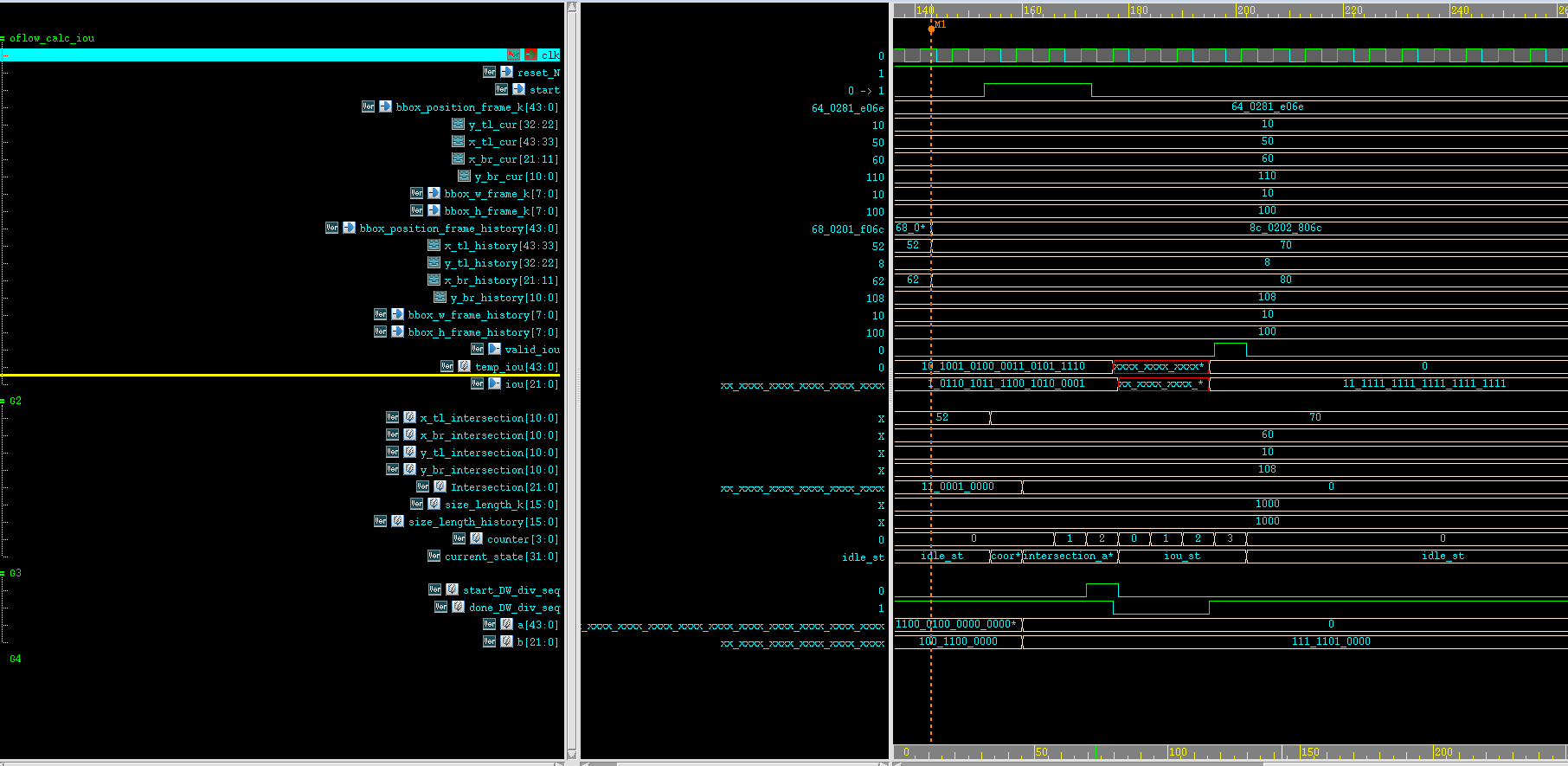


Figure 40: Test result – oflow-Similarity-Metric -calc iou- Without overlap case

decimal



Table 14: Oflow-Calc-Iou without overlap - Test Plan

There is a minor error of 2.384E-05 % between the expected iou to the simulation iou.

# 4. Summary

## 4.1 Project's summary

## 

* In Summary, the goal of the project is to accelerate, by scalable HW, the object registration process.
* Innovation: Original and new HW algorithm, especially Conflict Resolve unit.
* It was achieved by planning a micro-architecture with units that work in parallel (multiple parallel process engine units, multiple ports for read and write transaction and storing of more than one BBox in one row of the memory).
* The main stages of the model are features extraction, similarity calculation, conflict resolve and data storage.
* What has been done in this part of the project?
  + Micro-Architecture (Blocks Diagram)
  + Implementation of all the units
  + Tests and functional simulations of part A units
* What still needs to be done in part B of the project**?**
  + Tests and simulations of the other units
  + Synthesis
  + performance
  + layout

## 4.2 Take message home

* Planning Micro-Architecture involves deep thinking.
* Correct implementation and tests in SV
* Learning new topics, such as fixed-point representation, fixing overflow, how to work with IPs and SRAM (their interface and the way they behave).

## 4.3 Next steps

* Raising the number of the Process Engines to 32 (power of 2), to accelerate the calculation and therefore the total process.
* Raising the number of fallbacks for the oflow\_conflict\_resolve to 5 instead of 2 for precision in the labeling of the BBoxes.
* Enlarge the similarity metric units per PE, to accelerate the process of the registration of the BBoxes.
* Enlarge the number of ports of memory access, to accelerate the process of the registration and the write stages.
* Remove the dependency in the glue logic and work directly with the DMA.

# 5.References

* 1. Optical Flow - <https://en.wikipedia.org/wiki/Optical_flow>
* 2. AMBA APB - https://developer.arm.com/documentation#numberOfResults=48&q=Amba%20apb
* 3. Article: Liu, Min, and Tobi Delbruck. "Block-matching optical flow for dynamic vision sensors: Algorithm and FPGA implementation." 2017 IEEE International Symposium on Circuits and Systems (ISCAS). IEEE, 2017.
* 4. Article – Sport-Analytics with YOLO et al. by Shahar Gino: https://medium.com/p/951b3f26221b
* 5. fixed-point representation: <https://youtu.be/b57jNWbqdmM?si=I5uaxTGcMJB4dMXZ>, https://projectf.io/posts/fixed-point-numbers-in-verilog/

1. (https://projectf.io/posts/fixed-point-numbers-in-verilog/) [↑](#footnote-ref-1)
2. (https://youtu.be/b57jNWbqdmM?si=I5uaxTGcMJB4dMXZ) [↑](#footnote-ref-2)