Product Number: PCIe PCIe Station Unknown User 13/03/2025 10:16:40

L0_EqRx_16GTps_Comp

for PCIe 5.0 System

General		
Offline	False	
Pause before Auto- Align	False	
Channel		
CLB var. ISI pair	5	
Total Channel Loss	-30 dB	
Impairments		
Use Residual SSC (Triangular)	False	
Random Jitter	1 ps	
Sinusoidal Jitter	9.25 ps	
Sinusoidal Jitter Frequency	100 MHz	
Common Mode Sinusoidal Interference	150 mV	
Differential Mode Sinusoidal Interference	24.5 mV	
Generator Launch Voltage	800 mV	
Loopback Training-		
Enable Impairments during Loopback Training	True	
Interactive Training Script File	<pre>C:\ProgramData\BitifEye\ValiFrameK1 \PCIe\Settings\TrainingScripts\Pcie4_16G_M8040A_ILT_Loopback.txt</pre>	
Default Link Training Lane Number for every Lane	uto	
Suppress Loopback Training Messages	False	
Use Gen3 EIEOS	False	
BER Measurement		
BER Mode	FixedTime	
BER Measurement Duration	62.5 s	
Allowed Bit Error	1	
Abort BER Measurement when failed	False	
Relax Time	3 s	
Interactive Link Training		
Generator Full Swing	24	
DUT Target Preset	₽7	
DUT Start Preset Choice Gen4	System Board Defined	
DUT Target Preset Gen4	P7	
Speed Change Control	BERT	
Drop Link Method		
	LTSSM	
Error Detector		
Fast Alignment	False	

Input Range for 400 mV Loopback Training Input Range 400 mV CDR Loop Selection Loop3 Polarity Normal

Manually align error detector sampling

False

point.

Result	Sinusoidal Jitter Frequency [MHz]	Sinusoidal Jitter [ps]	Final Generator Preset	Final Generator Pre-shoot [dB]	Final Generator De- emphasis [dB]	Allowed Bit Errors []	Measured Bit Errors
pass	100.0	9.25	P5	1.5	0.0	1	0