Combining 2-level Logic Families in Grid-based Nanoscale Fabrics

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Abstract—Most proposed architectures for nanoscale computing systems are based on a certain type of 2-level logic family, e.g., AND-OR, NOR-NOR, etc. In this paper, we propose a new fabric architecture that combines different logic families in the same nanofabric. To achieve this we apply very minor modifications on the way a nanogrid is controlled but without changing the basic manufacturing assumptions. This new hybrid 2-level logic based fabric yields higher density for the applications mapped to it. When fault tolerance techniques are added it significantly improves fault tolerance. A nanoscale processor is implemented on this fabric for evaluation purposes. We found that compared with an implementation on a NASIC (Nanoscale Application Specific IC) fabric with one type of 2-level logic, the density of this processor improves by up to 48% by using the hybrid logic. Furthermore, the yield is improved by 22% at 5% defective transistors and by 4X at 10% defect rates. Detailed analysis on density and yield is provided. The approach is applicable in grid-based fabrics in general: e.g., it can be used in both NASIC and CMOL designs.

***Index Terms*—Semiconductor nanowires, nanofabrics, NASIC, CMOL, nanoscale processors.**

I. Introduction

Researchers have shown that they can grow semiconductor nanowires (NWs) and control their electrical properties [1]. They can also assemble these NWs into crossbars [18]. Diodes and FETs can be implemented at the crosspoints of crossbar structures [2]. Furthermore, rapid progress on manufacturing makes computing systems at very high density levels (e.g. 10^{11}~10^{12} transistors/cm^2) a promising direction beyond conventional CMOS.

Integrating nanodevices into computing systems is facing new challenges not encountered in conventional CMOS. Self-assembly based manufacturing [3] imposes doping/layout constraints on nanoscale circuits restricting routing and placement. It is fairly common that nanoscale circuits are based on AND-OR (or equivalent) 2-level logic: this is almost an obvious choice on a grid given the layout restrictions. In 2-level logic complementary signals are typically required to implement arbitrary logic functions.

Several fabric architectures have been proposed based on a certain grid-based 2-level logic family. For example, CMOL [6][15] is using NOR-NOR logic wherein the OR logic is implemented by NWs; CMOS cells provide signal inversion and restoration. NanoPLA [5] uses reprogrammable switches for logic and FETs for signal restoration but overall with a similar logic style. An FET-based nanoscale fabric architecture proposed is NASIC [7]. It uses AND-OR logic or other equivalent 2-level logic family such as NAND-NAND and proposes to mask errors in the circuit itself avoiding the requirement of reconfigurable devices.

This paper proposes a new fabric style that combines two different logic families in the same logic stage in the fabric. We evaluate it in the context of NASIC fabrics. With some simple circuit modifications, AND-OR/NOR 2-level logic is implemented instead of the pure AND-OR logic. This new fabric can easily generate complementary signals and require fewer partial products and thus reduces the number of corresponding NWs. This way a significant reduction can be achieved in the area of nanoscale designs mapped to the fabric. While the techniques in this paper are discussed and evaluated in the context of NASICs, the ideas could be applied in other 2D grid-based architectures such as CMOL. The idea appears almost obvious but, to the best of our knowledge, it has not been proposed or evaluated before. In fact, its beauty is that it can be applied in wide range of fabrics with minor modifications without adding any new manufacturing requirement.

We use the Wire Streaming Processor (WISP-0) [13] design to evaluate the benefits of the modified NASIC fabric with the new logic family. For the purpose of the evaluation, WISP-0 is implemented on both the AND-OR and the AND-OR/NOR fabrics. Furthermore, some of the original defect tolerance techniques used in WISP-0 and NASICs are added in both versions. Several defect/fault-tolerance techniques at different levels have been proposed for the original NASIC designs [7][8]. These include 2-way redundancy, NW interleaving, system-level Triple Modular Redundancy (TMR [17]) in CMOS [9] at key architectural points, built-in error correction circuitry, etc.

The results show that the density of WISP-0 on the new AND-OR/NOR fabric is 48% better than on the original fabric. We similarly found that the new AND-OR/NOR fabric can also improve the efficiency of the built-in fault tolerance techniques. Simulation shows that the yield of WISP-0 with AND-OR/NOR logic is significantly better than WISP-0 with pure AND-OR logic. For example, the yield of WISP-0 when

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both 2-way redundancy and system-level TMR are used can be improved by 22% at 5% defective transistors. The same improvement would be 4.04X at 10% defect rates. It appears that the improvement is increasing further at higher defect rates.

The paper is organized as follows. In Section II, we provide a brief overview of NASICs and WISP-0 to make the paper as self-contained as possible. Section III describes the proposed AND-OR/NOR NASIC fabric architecture in detail through simple circuit examples. The yield and density simulation results for WISP-0 are provided in Section IV. Section V concludes the paper.

II. NANOCIRCUITS, NASICS AND WISP-0 PROCESSOR

A. Dynamic Nanocircuits on Semiconductor Nanowires

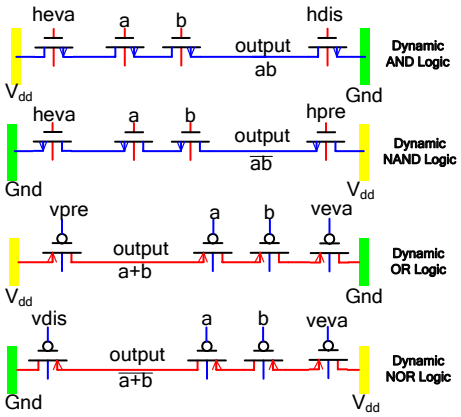

Fig. 1. Dynamic circuits implementing AND, NAND, OR and NOR logic functions on NWs.

Dynamic circuits have been widely used in MOS designs. We can similarly implement dynamic circuits at nanoscale with the help of control signals generated in CMOS. For example, the circuits in Fig. 1 show how to implement basic logic functions (i.e., AND, NAND, OR and NOR) in a dynamic style on semiconductor NWs. It should be noted that the NW FETs assumed here are depletion mode, in contrast to enhancement mode FETs used in conventional CMOS designs. In CMOS, a PMOS transistor can be used only for pull-up and an NMOS transistor only for pull-down. However, this limitation is not present in NASICs because of the difference in threshold voltages between enhancement mode and depletion mode transistors.[1]

A novel aspect of dynamic circuits in NASICs is the addition of the hold phase that is used to enable correct cascading. A variety of schemes have been proposed achieving different throughputs. In NASICs, this hold phase also provides temporary storage of output values on NWs.

Fig. 2 shows a waveform that illustrates the discharge-evaluate-hold phases for AND circuits. Details on dynamic circuits and their applications in NASICs can be found in [10][13].

Comparing dynamic AND and NAND circuits, we find that the only difference between them is their connections to power supply (V_{dd}) and *Gnd*. It can be seen that one can easily generate complementary outputs by interchanging the power and ground NWs. Similar observation can be made for dynamic OR and NOR circuits. This observation is the key to our new fabric proposed in this paper that will be detailed in Section III. But let us first briefly review some more details on the NASIC fabric and the processor design that we will evaluate to allow the introduction of this logic style and associated new NASIC fabric architecture.

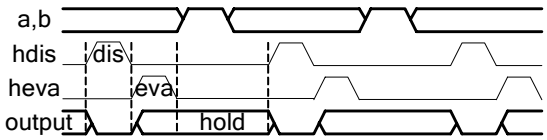

Fig. 2. Waveform for dynamic AND circuit. The hold phase is added for cascading purpose.

B. Overview of NASICs

NASIC designs are based on dynamic circuits implemented on semiconductor NWs; various optimizations are applied to work around layout and manufacturing constraints as well as defects [8][11]. While still based on cascaded 2-level logic style, e.g., AND-OR, NASIC designs are optimized according to specific applications to achieve higher density and defect/fault-masking. The selection of this logic family is due to its simplicity and applicability on a 2-D style fabric where arbitrary placement and routing is not possible. Furthermore, due to manufacturing constraints (such as layout and uniform doping in each NW dimension) it may be impossible to use, for example, complementary devices close to each other, such as in CMOS or orient devices in arbitrary ways. By using dynamic circuits and pipelining on the wires, NASICs eliminate the need for explicit flip-flops in many areas of the design [10] and achieve unique pipelining schemes.

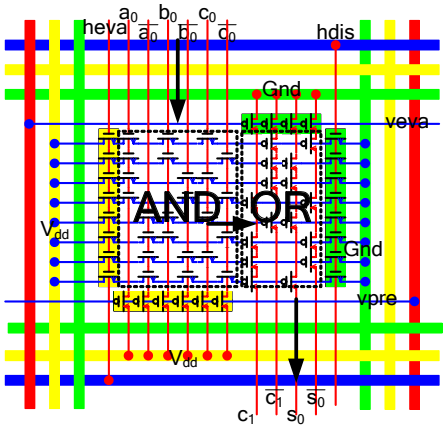

Fig. 3. 1-bit dynamic NASIC full adder using AND-OR cascaded logic. Arrows show propagation of data through the tile.

[1] One known issue with depletion mode FETs is the difficulty to switch off completely. However, preliminary analysis based on I-V characteristics published in [21] suggests that this will not adversely affect circuit functionality. Work on detailed circuit level analysis and simulation is in progress including accounting for noise related faults.

Fig. 3 demonstrates the design of a simple 1-bit NASIC full adder in dynamic AND-OR style [13]. The thinner wires represent NWs. All horizontal NWs are doped to n-type while all vertical NWs are doped to p-type. The signals *hdis*, *heva*, *vpre*, and *veva*, correspond to discharge, evaluation, precharge and evaluation phases on different NWs. Each nanotile is surrounded by microwires (MWs) (thicker wires in the figure), which carry ground (*Gnd*), power supply voltage (V_{dd}), and control signals for the dynamic evaluation of outputs. The control signals are generated in CMOS. As we mentioned before, complementary signals are required to implement arbitrary logic functions in 2-level logic style. In the circuit in Fig. 3, we generate negative outputs $\sim c_1$ and $\sim s_0$ for cascading in multi-tile designs. Please refer to [7][8] [10][11][13] for more details.

NASIC manufacturing may be accomplished through a combination of self-assembly and top-down processes.

- NWs can be grown using seed catalyst techniques or other methods that may ensure uniform NW diameters [1]. NWs may be aligned into parallel sets using Langmuir-Blodgett techniques or nanopatterning.
- Regions on individual NWs where there should be no FET channels will then need to be metallized using a lithographic mask. A 2NW pitch resolution is required but precise shaping is not needed, making this step easier than a CMOS manufacturing step for a comparable feature size.
- An oxide layer may then be grown over the NWs and a 2D grid formed by moving one NW set on top of the other.
- A fine grain metallization step demarcates FET channels, create metallic interconnect between neighboring FETs. This may be achieved by using the top NW as a self-aligning mask as shown in [12].
- Micro-Nano interfacing may be done in conjunction with lithographic process steps.

Although many of the key individual steps required have been demonstrated, combining the necessary steps for reliable manufacturing remains challenging and unproven.

C. Single-Type vs. Complementary Type NASICs

In order to produce complementary FETs, two different types of doped NWs must be used. Complementary FETs have been demonstrated in zinc oxide [20], silicon [1], and germanium [19], but in all cases differences in transport properties were found between the two types, sometimes much greater than those seen in today's traditional CMOS FETs. By suitably modifying the NASIC dynamic control scheme and circuit style, we can implement arbitrary logic functions with one type of FETs in NASICs. A design using only n-type FETs will implement a NAND-NAND cascaded scheme whereas a design using only p-type FETs will implement a NOR-NOR scheme. Fundamentally, these are equivalent with the original AND-OR. These schemes may thus be used with manufacturing processes where complementary devices are difficult to achieve. The 1-bit adder example with nFETs is shown in Fig. 4. A detailed analysis of the control scheme for this circuit is beyond the scope of this paper; we refer the interested reader to [14] for more details.

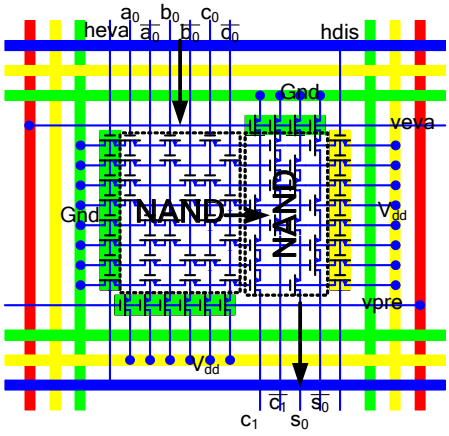

Fig. 4. n-FET only version of a 1-bit adder using the NAND-NAND cascaded logic.

D. Overview of the WISP-0 Processor

WISP-0 is a stream processor that implements a 5-stage pipelined streaming architecture in 5 nanotiles: *PC*, *ROM*, *DEC*, *RF* and *ALU*. Local communication between adjacent nanotiles is provided by NWs. Each nanotile is surrounded by MWs which carry ground, power supply voltage, and some control signals. WISP-0 uses a 3-bit opcode and 2-bit operands. It supports many different arithmetic operations including multiplication.

Fig. 5 shows the layout of WISP-0 with AND-OR logic style. A nanotile is shown as a box surrounded by dashed lines. More details about the various circuits used can be found in [10][11] [13]. In this paper, we use WISP-0 mainly to evaluate our new nanofabric and focus on the density and defect/fault-tolerance related tradeoffs and implications.

E. Built-in Defect/fault-Tolerance Techniques in NASICs

Nanoscale computing systems including NASICs have to deal with the high defect rates of nanodevices and faults introduced by manufacturing of fabrics. In NASICs we consider a fairly generic fault model with both uniform and clustered defects and three main types of permanent defects: NWs may be broken, the transistors at the crosspoints may be stuck-on (no active transistor at crosspoint) or stuck-off (channel is switched off).

We consider defect rates of up to 15% at the finest granularity which is the device level. Our previous work indicates that device-level defect rates greater than 15% would likely eliminate the density benefits of nanoscale fabrics compared to projected CMOS technology, in the context of microprocessor designs. We also assume that the stuck-on transistor is much more prevalent than stuck-off transistors in NASIC fabric due to the metallization process [4] in manufacturing steps. Stuck-off FETs are also less likely in depletion mode fabrics [16]. Note that a 15% defect rate is much higher than say a 50% defect rate at a cell level of designs

(or circuit component level) - that is assumed by some other researchers. Clearly, with 15% device-level defects any reasonable size circuit would be defective so even assuming a rate of 40-50% at a component granularity seems highly unrealistic.

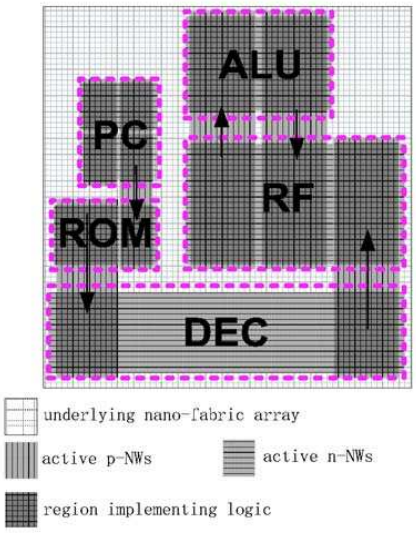

Fig. 5. Floorplan of the WISP-0 processor.

Built-in fault-tolerance techniques are applied at various granularities for NASICs to make NASIC designs functional even in the presence of errors, while carefully managing area tradeoffs. Compared with reconfiguration based approaches, this strategy also simplifies the micro-nano interfacing: no access to every crosspoint in the nanoarray is necessary. Furthermore, a defect map is not needed and the devices used do not have to be reconfigurable.

The built-in fault-tolerance techniques that are applied on the new fabric techniques include 2-way redundancy and system-level voting (i.e., TMR) in CMOS at key architectural points. The density and yield of WISP-0 under different fault-tolerance scenarios are evaluated for the new fabric and compared with the original fabric. Comprehensive description of built-in fault-tolerance techniques in NASICs can be found in [7][9] and is beyond the scope of this paper.

III. Combining Logic Families in NASIC Fabric

In the design shown in Fig. 3, the outputs (c_1, s_0 and their negative versions $\sim c_1, \sim s_0$) are generated in the sum-of-product form of the inputs. The signals on horizontal NWs (excluding the control NWs such as *veva* and *vpre*) correspond to different partial products. For example, the signal on the top horizontal NW corresponds to partial product $a_0b_0c_0$; the signal on the second NW corresponds to partial product $a_0b_0{\sim}c_0$. Each output signal is the sum of selected partial products.

From Fig. 3, we can see that different output signals require different groups of partial products. The output c_1, for example, requires partial products $a_0{\sim}b_0{\sim}c_0$, $\sim a_0b_0{\sim}c_0$, $\sim a_0{\sim}b_0c_0$ and $\sim a_0{\sim}b_0{\sim}c_0$ while the output $\sim c_1$ requires $a_0b_0c_0$, $a_0b_0{\sim}c_0$, $a_0{\sim}b_0c_0$ and $\sim a_0b_0c_0$. The observation here is that *positive output and its negative version will require different partial products if both of them are implemented in the same AND-OR logic planes*.

We have mentioned in Section II.A that the negative outputs can be easily generated by interchanging the power supply and ground connections. This way we can generate negative outputs in AND-NOR style; note that the negative output would need the same partial products as the positive output. We may therefore reduce the number of required partial products (i.e., the number of horizontal NWs) if a different control scheme is used. This thinking leads to our new nanofabric.

We propose to combine AND-OR and AND-NOR logic families into the same NASIC logic plane. This requires some modifications on the OR plane. For comparison, the new circuit for the same 1-bit full adder but in AND-OR/NOR fabric is shown in Fig. 6. Note that in the design of Fig. 3, all output NWs (c_1, s_0, $\sim c_1$ and $\sim s_0$) in the OR plane connect to the *Gnd* MW at the top and to the V_{dd} MW at the bottom.

In the design of Fig. 6, however, all negative output NWs ($\sim c_1$ and $\sim s_0$) are connected to V_{dd} and *Gnd* MWs in the *opposite way*. All positive outputs (c_1 and s_0) of the design in Fig. 6 is generated by AND-OR logic while all negative outputs ($\sim c_1$ and $\sim s_0$) by AND-NOR logic instead.

The right logic plane in Fig. 6 now combines OR and NOR functions *in the same plane*. Compared with the design in Fig. 3, the partial product $a_0b_0c_0$ (corresponding to the top horizontal NW) is not necessary and therefore is removed from the new design in Fig. 6. This way we can reduce the number of horizontal NWs and indirectly the overall number of transistors.

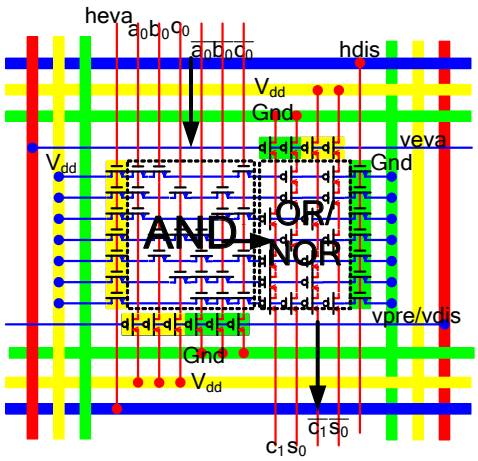

Fig. 6. a 1-bit adder using the AND-OR/NOR logic.

A. Manufacturing Implications

A key advantage of this new fabric is that it effectively improves the density but does not introduce any new manufacturing challenges – for details on proposed manufacturing of NASICs we refer the reader to [7].

The only modifications that are made are at the connections from NWs to V_{dd} and *Gnd* MWs. This manufacturing step is accomplished at microscale in a fashion similar to the original fabric style. Compared with the design in Fig. 3, we have changed the order of vertical NWs in Fig. 6, effectively segregating the OR and NOR logics. This rearrangement of vertical NWs ensures that the nano-micro interfacing is still at the microscale. Hence no additional manufacturing constraints are imposed. As can be seen in Fig. 6, the dynamic control scheme otherwise remains completely unchanged. Positive and negative output NWs share the same control signals as previously.

B. *Fault Tolerance Implications*

Another interesting benefit of the AND-OR/NOR fabric is that it also improves the yield of NASIC designs. The reason is quite simple: The total number of horizontal NWs and associated FETs are reduced compared to the original design – we can get the job done with fewer transistors. For a given defect rate, the expected number of defects in a design is also reduced. A design can therefore achieve better yield in AND-OR/NOR fabric as compared to the original AND-OR. We will evaluate the impact of this for a concrete example in the next section.

C. *Applicability to Other Types of 2-Level Fabrics*

This technique can be easily applied onto nanofabrics based on 2-level logic. For example, on nFET-only NASIC fabrics, we can design circuits based on NAND-NAND/AND logic families.

The approach can be applied in grid-based designs in general. For example, it can also be applied to NOR-NOR based CMOL fabrics. The new logic family for CMOL would be NOR-NOR/OR. We currently are exploring such CMOL designs.

IV. Evaluation

In this section, we design all components of WISP-0 in AND-OR/NOR NASIC fabric and evaluate the improvement on density. To evaluate the improvement on yield, we developed a simulator to estimate the yield of the AND-OR/NOR based WISP-0 for various defect rates and distributions.

A. *WISP-0 on AND-OR/NOR NASIC Fabric*

Table I shows the comparison between WISP-0 designs in the new AND-OR/NOR fabric and the AND-OR fabric. The area of each nanotile and the number of transistors used in the nanoarray are listed. A 10nm pitch between NWs is assumed similar to [7].

We can see that for each tile in WISP-0, the new AND-OR/NOR fabric can save almost 50% of the nanoarray area. The estimate does not include the overhead of the V_{dd}, *Gnd* and control MWs that will be shown in conjunction with fault handling implications in the following section. The number of required transistors in each tile is also reduced. In total, the number of transistors in WISP-0 is reduced by 52%.

Table I
Reduction of area and transistors in AND-OR/NOR fabric

	Nanoarray area (nm^2)		# of transistors	
	AND-OR	AND-OR/NOR	AND-OR	AND-OR/NOR
PC	35,200	22,400	86	54
ROM	26,400	13,200	127	54
DEC	57,600	28,800	36	27
RF	476,000	265,200	340	133
ALU	59,400	28,800	211	114
Total	654,600	358,400	800	382

B. *Density Evaluation of WISP-0*

To get a more accurate evaluation on density, we need to take the area overhead of MWs into account. Technology parameters used in the calculations are listed in Table II. Note that the pitch between MWs in nanoscale WISP-0 also scales down with CMOS technology nodes. The normalized density of WISP-0 for the various scenarios is shown in Fig. 7.

To get a better sense of what the densities actually mean we normalize the density of nanoscale designs to an equivalent WISP-0 processor synthesized in CMOS. We designed this processor in Verilog, synthesized it to 180nm CMOS. We derived the area with the help of the Synopsys Design Compiler tool. Next, we scaled it to various projected technology nodes based on the predicted parameters by ITRS, assuming area scales down quadratically. A similar methodology was applied in [7]. For the purpose of this paper, we assume that the CMOS version of WISP-0 is defect-free and no fault-tolerance technique is applied. It is expected that even CMOS designs would need redundancy and other techniques to deal with defects and mask delay variations due to process parameter variations. This means that our CMOS ASIC numbers are fairly optimistic.

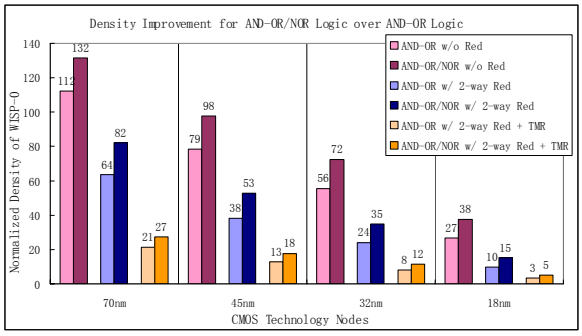

Fig. 7. Density improvement of WISP-0 using hybrid AND-OR/NOR logic under different fault-tolerance scenarios.

In the following pages, we present our simulation results. The notation used in the graphs is: *w/o Red* stands for WISP-0 without fault-tolerance techniques (or baseline); *2-way Red* stands for WISP-0 with 2-way redundancy; *2-way Red+TMR* stands for 2-way redundancy plus micro-scale TMR (i.e., in

CMOS) on the WISP-0 final result; The prefix *AND-OR* represents WISP-0 designed with pure AND-OR logic and the prefix *AND-OR/NOR* stands for WISP-0 with the new hybrid AND-OR/NOR logic. While other combinations are possible, we found these to be insightful and representative.

Table II
Technology Parameters

NW pitch	10nm
NW width	3~4nm
Technology Node (ITRS 2004)	MW pitch
70-nm	170nm
45-nm	108nm
32-nm	76nm
18-nm	42nm

We can see from the results that the new AND-OR/NOR fabric improves the density of WISP-0 significantly for all possible scenarios. For WISP-0 without redundancy, at 45nm CMOS technology node, the improvement is 24%. After applying 2-way redundancy and system level TMR, the improvement of density would be 39%. At 18nm CMOS technology node, the improvement of the density for WISP-0 without redundancy is 41%. After applying 2-way redundancy and system level TMR, the density improvement is 48%.

Overall, the density improvement increases for more advanced CMOS processes. This is because the area overhead of MWs at 18nm technology node is much smaller than at 45nm technology node and thus the corresponding area reduction of the nanoarray is more prominent.

C. Comparison between AND-OR/NOR WISP-0 and CMOS Version

Next we review the comparison between WISP-0 in the new logic family and the advanced CMOS implementations. We found WISP-0 in the AND-OR/NOR NASIC fabric to be 5X (with 2-way redundancy and TMR) and 15X (with 2-way redundancy but without TMR) denser than the corresponding CMOS processor at 18nm technology node.

D. Yield Evaluation of the new WISP-0 Designs with Various Built-in Defect Handling Techniques

We developed a simulator to verify the improvement of the new AND-OR/NOR fabric on the yield of WISP-0. The simulation results for permanent defects are provided in Fig. 8 (assumes defective FETs) and Fig. 9 (assumes broken NWs). This work assumes the defect and fault model as discussed in [7] and its purpose is to show the impact of the logic family if the design also incorporates fault tolerance.

First we present results assuming uniformly distributed defects. Clustered defects are addressed in separate subsequent subsections.

From the results below, we can see that the AND-OR/NOR fabric improves the yield considerably. Compared with the AND-OR approach in *2-way Red+TMR* scenario, the improvement of AND-OR/NOR fabric on the yield of WISP-0 is 22% when the defect rate of transistors is 5% and 4.04X at 10% defect rate. Note that the improvement is greater for higher defect rates. For broken NWs, the improvement of yield is 6% at 5% defect rate and 2.01X at 10% defect rate.

Some defect-masking techniques provide good yield improvement but require relatively large area overhead (e.g., the *2-way Red+TMR* approach). Therefore, it is important to understand the area overhead (or impact on density) of the different fault-tolerance techniques in conjunction with their fault masking ability. To evaluate the tradeoff between yield improvement and area, we also consider the yield and density together in a combined metric. The yield-density product is a comprehensive indicator for the efficiency of different defect-tolerance techniques; it represents the ratio between the benefit (yield of designs) and its cost (area overhead). This will be shown in the next subsection.

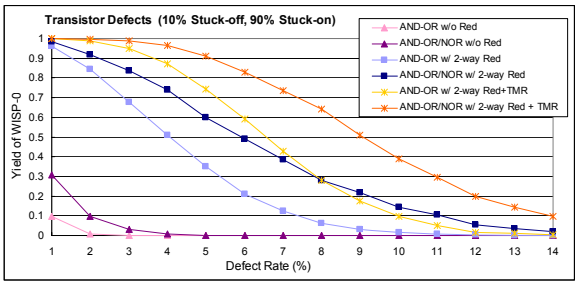

Fig. 8. The yield achieved for WISP-0 with different techniques when only considering defective transistors.

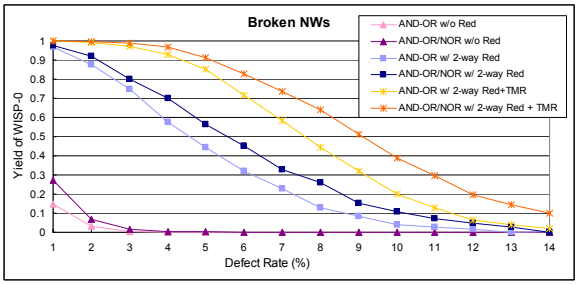

Fig. 9. The yield achieved for WISP-0 with different techniques when only considering broken NWs.

E. WISP-0 Yield-Density Product Evaluation

The yield-density product results for various defect rates are presented in Fig. 10 and Fig. 11 respectively. We can see that significant improvements on the yield-density products of WISP-0 processor are achieved in all scenarios. For example, in the *2-way Red* scenario, the yield-density product of WISP-0 is improved 2.67X when assuming 5% defective transistors and 13.8X at 10% defect rate. Note that it appears that this improvement is beyond what is directly from the density improvement alone.

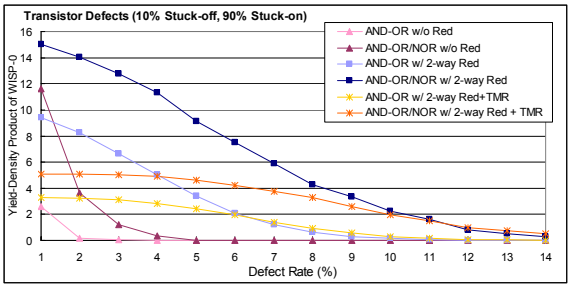

Fig. 10. WISP-0 yield-density products considering defective transistors.

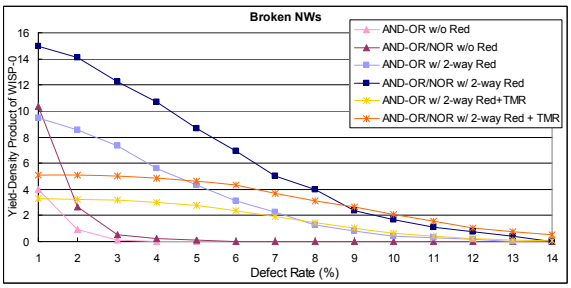

Fig. 11. WISP-0 yield-density products considering broken NWs.

Similar to our original approach in [7], it is clear from the figures that different levels of defect rates may require different types of defect-tolerance techniques: for broken NWs, if the defect rates are lower than 8%, *2-way Red* appears to be sufficient and a good choice. When defect rates increase beyond 8%, *2-way Red+TMR* becomes desirable. Future NASIC CAD tools can take advantage of this and insert appropriate levels of defect tolerance depending on expected defect rates.

F. Impact of Clustered Defects

In our previous results we assumed that all defects are uniformly distributed. However, defects can also be clustered as a group of adjacent FETs or a group of adjacent NWs could be damaged during the manufacturing process.

To evaluate the impact of clustered defects, we need a model for clustered defects. In this paper, we assume the same model as in [7] for comparison purposes. In this model the probability of defects decreases from the center of the cluster towards its margins. The model assumes a uniform cluster shape: we are currently working on modeling the possible cluster shapes (this is due to manufacturing) for more accurate estimates. Nevertheless, from the point of view of this comparison we mainly focus on trends that are due to the new logic style.

Fig. 12 shows the yield of WISP-0 assuming clustered transistor defects; Fig. 13 shows the yield with clustered broken NWs. The results indicate that the AND-OR/NOR fabric also helps to tolerate clustered defects/faults: in Fig. 12 the yield of WISP-0 with *2-way Red+TMR* remains 40% even when the cluster defect rate of transistors is 5% for the parameters simulated. Note that each defect cluster may have multiple defects.

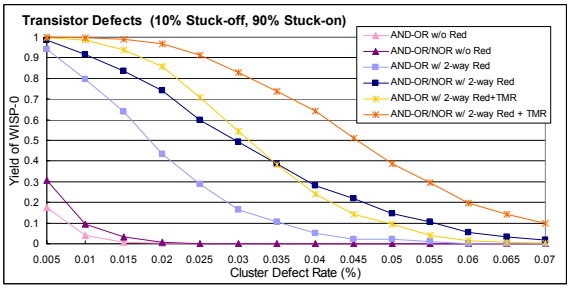

Fig. 12. WISP-0's yield for various cluster rates assuming clustered defective transistors.

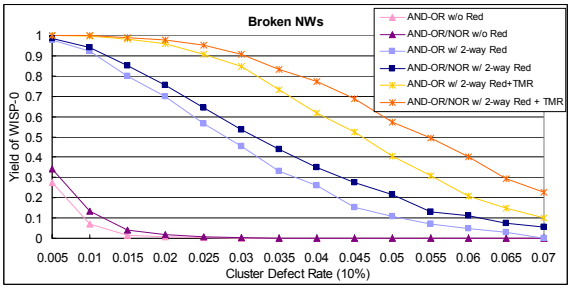

Fig. 13. WISP-0's yield for various cluster rates assuming broken NWs.

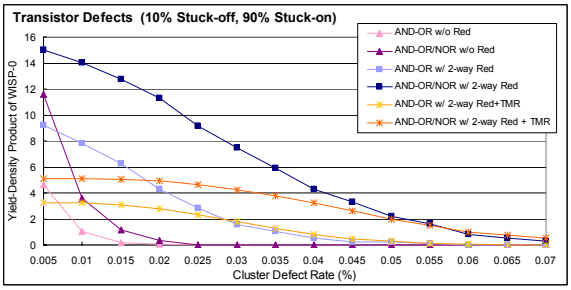

Fig. 14. Yield-density product achieved for WISP-0 considering clustered defective transistors.

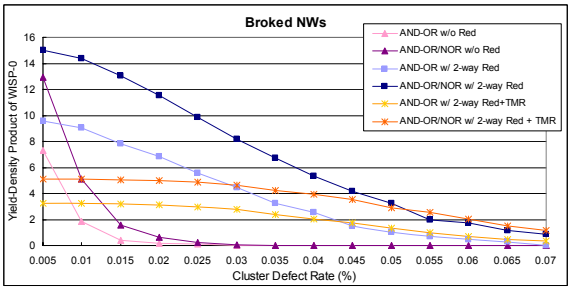

Fig. 15. Yield-density product achieved for WISP-0 when only considering clustered broken NWs

The yield-density product of WISP-0 for clustered defects is shown in and respectively. We can see that the AND-OR/NOR fabric achieves much better yield-density

product values than the AND-OR fabric. The improvement is 2.6X for WISP-0 with 2-way Red when the rate for clustered defective transistors is 2% and 10.8X when cluster defect rate is 5%.

V. CONCLUSIONS

In this paper we demonstrated a new nanofabric that combines two different logic families in the same logic stage in the fabric. While the idea appears simple, it has not been proposed or evaluated before and has several important benefits when applied in nanoscale designs. First, circuit designs in the new fabric could be significantly simplified compared with the previous AND-OR based fabric. Our simulation results show that it is possible to achieve much denser designs compared to other 2-level logic approaches. In addition, the yields of the fault tolerant processor WISP-0 can also be improved significantly on the new fabric – in some cases by up to an order of magnitude. Furthermore, this technique can also be applied in other grid-based nanofabrics than NASICs. We are currently exploring this approach to improve the density of CMOL designs. In addition, we pursue evaluation for wider datapaths to gauge the benefits for larger scale designs.

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