2025 Digital IC Design Homework 4

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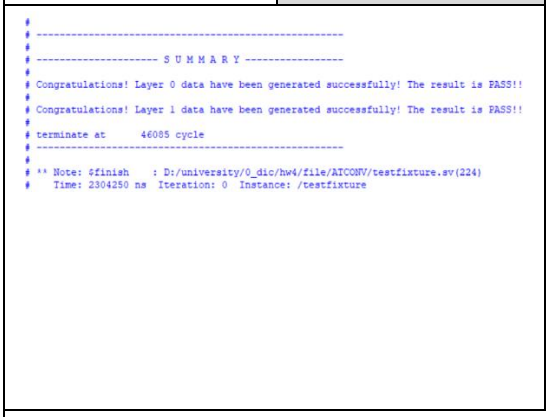
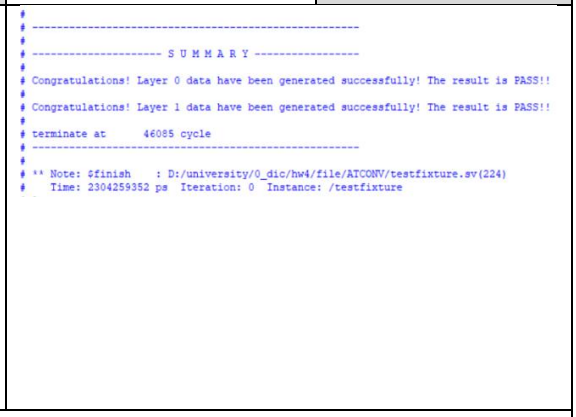
ATCONV Simulation Result

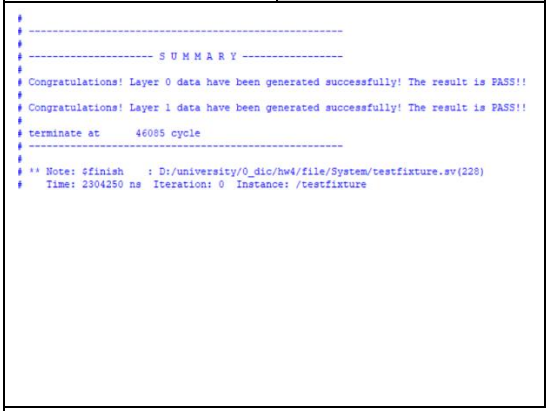
Functional simulation	Pass	Pre-Layout simulation	Pass

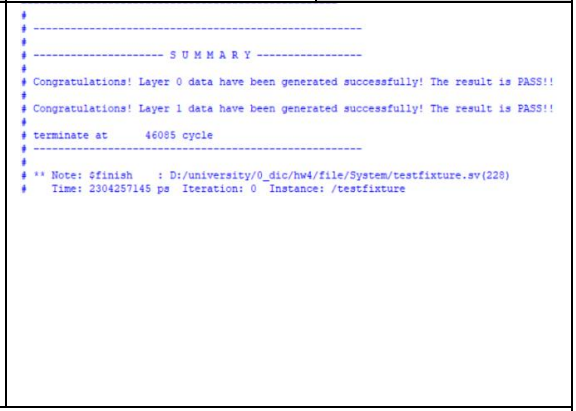




System Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass





ATCONV Synthesis Result

Total logic elements	288
Total memory bits	0
Total registers	91
Embedded multiplier 9-bit elements	2
Total Cycle used	46085

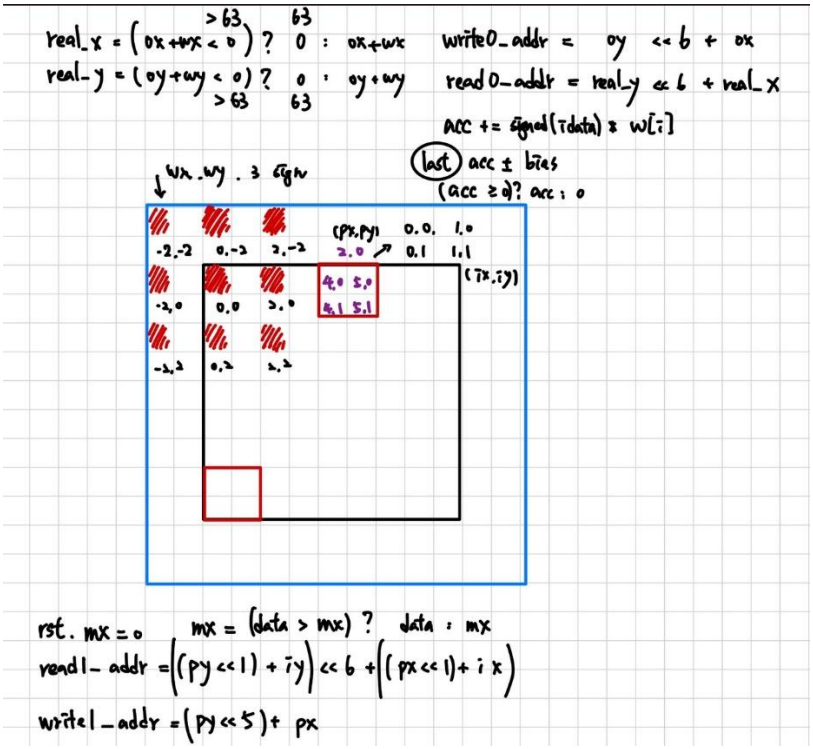
Flow Status	Successful - Sat May 31 04:30:07 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	288 / 55,856 (< 1 %)
Total registers	91
Total pins	124 / 325 (38 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

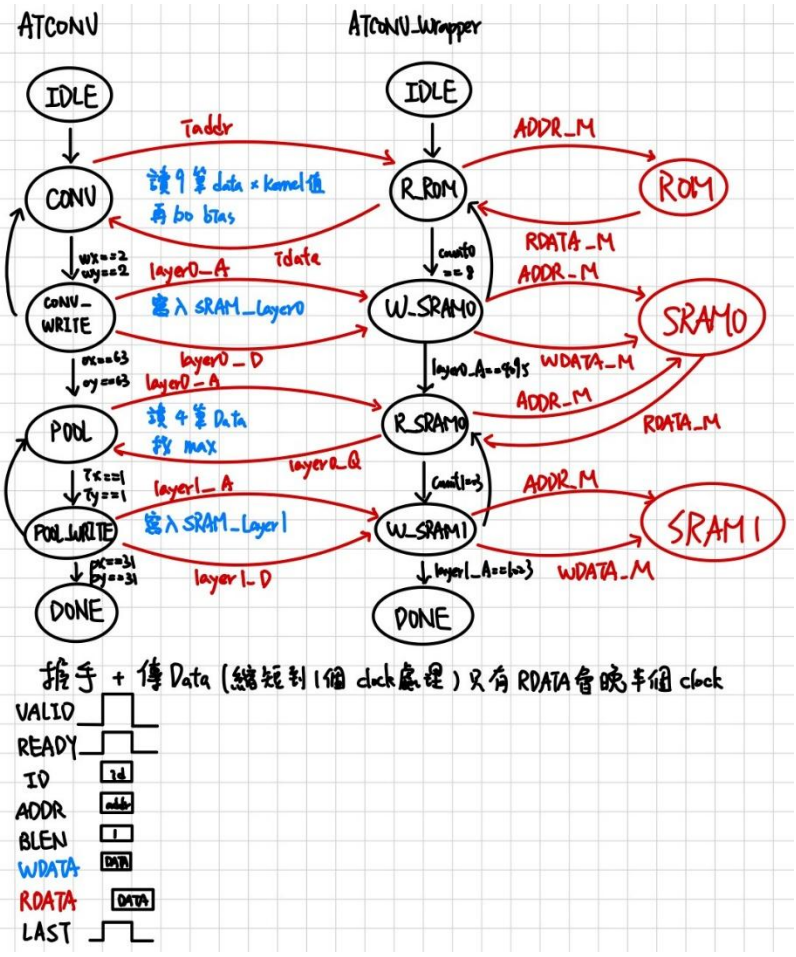
System Synthesis Result

Total logic elements	438
Total memory bits	0
Total registers	101
Embedded multiplier 9-bit elements	2
Total Cycle used	46085

Flow Status	Successful - Sat May 31 04:45:55 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	top
Top-level Entity Name	top
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	438 / 55,856 (< 1 %)
Total registers	101
Total pins	124 / 325 (38 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)

Description of your design





**Master 和 slave 傳資料都會透過 bus(也就是 ATCONV_wrapper 和 ROM、SRAM0、SRAM1 傳資料)