

2025 Digital IC Design Homework 4

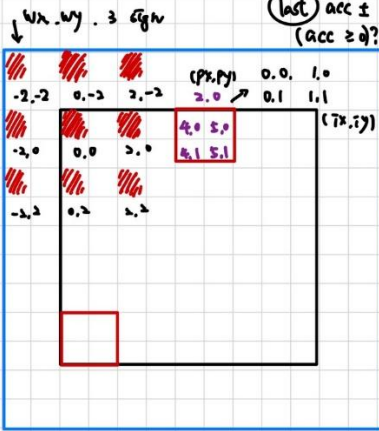
NAME	曾立呈		
Student ID	E94121038		
ATCONV Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
<pre># ----- # ----- SUMMARY ----- # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 46085 cycle # ----- # ** Note: \$finish : D:/university/0_dic/hw4/file/ATCONV/testfixture.sv(224) # Time: 2304250 ns Iteration: 0 Instance: /testfixture</pre>		<pre># ----- # ----- SUMMARY ----- # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 46085 cycle # ----- # ** Note: \$finish : D:/university/0_dic/hw4/file/ATCONV/testfixture.sv(224) # Time: 2304259352 ps Iteration: 0 Instance: /testfixture</pre>	
System Simulation Result			
Functional simulation	Pass	Pre-Layout simulation	Pass
<pre># ----- # ----- SUMMARY ----- # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 46085 cycle # ----- # ** Note: \$finish : D:/university/0_dic/hw4/file/System/testfixture.sv(228) # Time: 2304250 ns Iteration: 0 Instance: /testfixture</pre>		<pre># ----- # ----- SUMMARY ----- # Congratulations! Layer 0 data have been generated successfully! The result is PASS!! # Congratulations! Layer 1 data have been generated successfully! The result is PASS!! # terminate at 46085 cycle # ----- # ** Note: \$finish : D:/university/0_dic/hw4/file/System/testfixture.sv(228) # Time: 2304257145 ps Iteration: 0 Instance: /testfixture</pre>	
ATCONV Synthesis Result			
Total logic elements	288		
Total memory bits	0		
Total registers	91		
Embedded multiplier 9-bit elements	2		
Total Cycle used	46085		

Flow Status	Successful - Sat May 31 04:30:07 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	ATCONV
Top-level Entity Name	ATCONV
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	288 / 55,856 (< 1 %)
Total registers	91
Total pins	124 / 325 (38 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)
System Synthesis Result	
Total logic elements	438
Total memory bits	0
Total registers	101
Embedded multiplier 9-bit elements	2
Total Cycle used	46085
Flow Status	Successful - Sat May 31 04:45:55 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	top
Top-level Entity Name	top
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	438 / 55,856 (< 1 %)
Total registers	101
Total pins	124 / 325 (38 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	2 / 308 (< 1 %)
Total PLLs	0 / 4 (0 %)
Description of your design	

$real_x = (ox + wx < 0) ? 0 : ox + wx$ $write0_addr = oy \ll 6 + ox$
 $real_y = (oy + wy < 0) ? 0 : oy + wy$ $read0_addr = real_y \ll 6 + real_x$

$acc += signed(i_data) * w[i]$

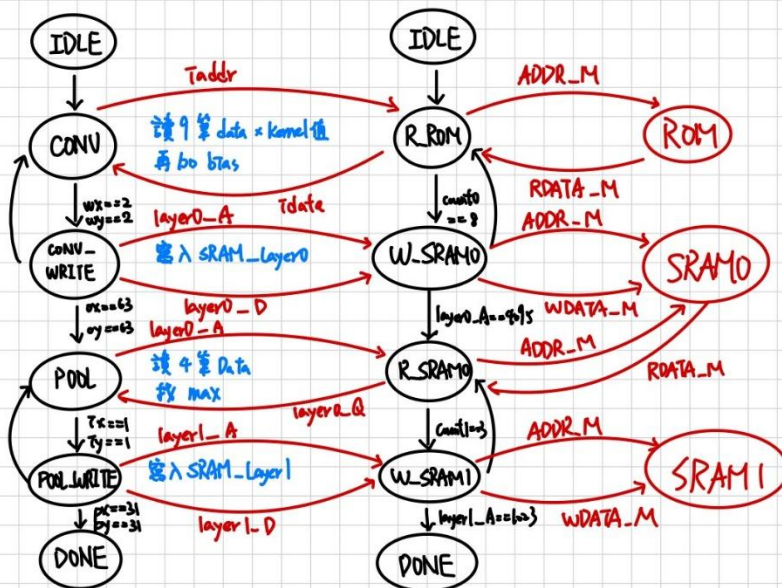
last acc \pm bias
 (acc ≥ 0)? acc : 0



$rst_mx = 0$ $mx = (data > mx) ? data : mx$
 $read1_addr = ((py \ll 1) + iy) \ll 6 + ((px \ll 1) + ix)$
 $write1_addr = (py \ll 5) + px$

ATCONV

ATCONV_wrapper



握手 + 傳 Data (總共 1 個 clock 處理) 只有 RDATA 會晚半個 clock



**Master 和 slave 傳資料都會透過 bus(也就是 ATCONV_wrapper 和 ROM、SRAM0、SRAM1 傳資料)

