2025 Digital IC Design Homework 5

NAME	曾立呈
Student ID	E94121038

Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass

```
================ Running pattern 8 ================
[PASS] Pattern 8: area = 01066
================ Running pattern 9 ================
[PASS] Pattern 9: area = 15e7a
====================== RESULT ======================
All 10 patterns passed!
Cycle: 1589
** Note: $finish    : D:/university/0_dic/hw5/file/testfixture.sv(83)
   Time: 36229200 ps  Iteration: 0  Instance: /testfixture
```

```
================ Running pattern 8 ================
[PASS] Pattern 8: area = 01066
================ Running pattern 9 ================
[PASS] Pattern 9: area = 15e7a
====================== RESULT ======================
All 10 patterns passed!
Cycle: 1589
** Note: $finish    : D:/university/0_dic/hw5/file/testfixture.sv(83)
   Time: 32574500 ps  Iteration: 0  Instance: /testfixture
```

Synthesis Result

Total logic elements	2761
Total memory bits	0
Total registers	388
Embedded multiplier 9-bit elements	4
Clock period (ns)	20.5
Total Cycle used	1589

Flow Status	Successful - Sun Jun 22 17:44:13 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	MCH
Top-level Entity Name	MCH
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	2,761 / 55,856 (5 %)
Total registers	388
Total pins	36 / 325 (11 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	4 / 308 (1 %)
Total PLLs	0 / 4 (0 %)

Description of your design

Read : (count)

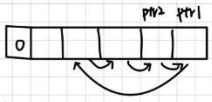
讀資料，跟X/Y_reg[0]比較，若 { Y_reg[0] > Y
Y_reg[0] == Y && X_reg[0] > X

若 X/Y_reg[0] <= X/Y, X/Y_reg[count] <= X/Y_reg[0]

Sort : Insertion sort (ptr1 , ptr2)

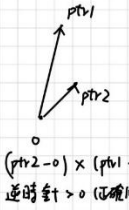
temp1/2 = X/Y_reg[ptr1]

if (ptr2 < 1)
  ptr1 <= ptr1 + 1 ;
  ptr2 <= ptr1 ;
  X/Y_reg[ptr2+1] <= temp1/2 ;



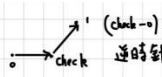
else if [(X_reg[ptr2] - X_reg[0]) * (temp2 - X_reg[0])
  >= (temp1 - X_reg[0]) * (Y_reg[ptr2] - Y_reg[0])] cp ≥ 0
  ptr1 <= ptr1 + 1 ;
  ptr2 <= ptr1 ;
  X/Y_reg[ptr2+1] <= temp1/2 ;

else
  ptr2 <= ptr2 - 1
  X/Y_reg[ptr2+1] <= X/Y_reg[ptr2] ;



(ptr2 - 0) × (ptr1 - 0)
逆時針 > 0 (正確順序)

Delete : (check)



if [((X_reg[check] - X_reg[check-1]) * (Y_reg[check+1] - Y_reg[check])
  <= (X_reg[check+1] - X_reg[check]) * (Y_reg[check] - Y_reg[check-1]))]
  valid <= valid - 1 ;
  for (i = check ; i <= valid - 1 ; i = i + 1)
    X/Y_reg[check] <= X/Y_reg[check+1] ;

if check == valid X_reg[valid]
if check == valid Y_reg[0]
cp ≤ 0

else
  check <= check + 1

calculate : (counter)

area_reg <= area_reg + [X_reg[counter] × Y_reg[counter+1] - X_reg[counter+1] × Y_reg[counter]]

if counter == valid X/Y_reg[0]

area = area_reg

reg signed Cal_X1 Cal_X2 . Cal_Y1 . Cal_Y2

wire signed cp = Cal_X1 × Cal_Y2 - Cal_X2 × Cal_Y1