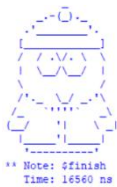



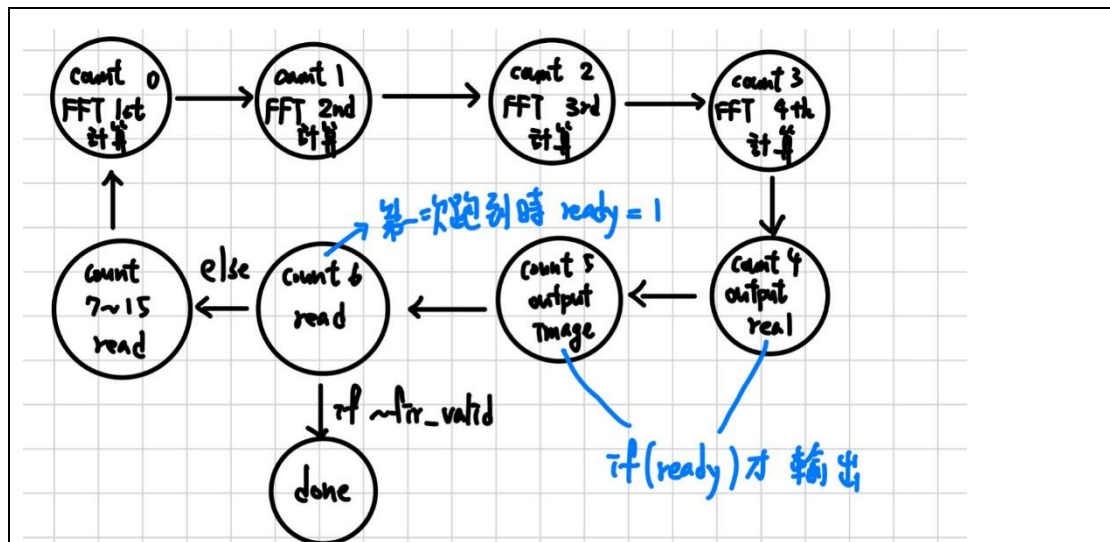


## 2025 Digital IC Design Homework 3

NAME	曾立呈																														
Student ID	E94121038																														
Simulation Result																															
Functional simulation	Pass	Pre-Layout simulation	Pass																												
<div><p>Congratulations! All data have been generated successfully! Total use 1034 cycles to complete simulation.</p><p>** Note: \$finish : D:/university/0_dic/hw3/testfixture.sv(213) Time: 16560 ns Iteration: 0 Instance: /testfixture</p><p>Congratulations! All data have been generated successfully! Total use 1034 cycles to complete simulation.</p><p>** Note: \$finish : D:/university/0_dic/hw3/testfixture.sv(213) Time: 16560 ns Iteration: 0 Instance: /testfixture</p></div>		<div>Please specify your clock width: <u>14</u> (ns)</div> <div><p>Congratulations! All data have been generated successfully! Total use 1035 cycles to complete simulation.</p><p>** Note: \$finish : D:/university/0_dic/hw3/testfixture.sv(213) Time: 14500025 ps Iteration: 0 Instance: /testfixture</p><p>Congratulations! All data have been generated successfully! Total use 1035 cycles to complete simulation.</p><p>** Note: \$finish : D:/university/0_dic/hw3/testfixture.sv(213) Time: 14500025 ps Iteration: 0 Instance: /testfixture</p></div>																													
Synthesis Result																															
Total logic elements		4366																													
Total memory bits		0																													
Total registers		920																													
Embedded multiplier 9-bit elements		152																													
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Description of your design																															



因為精度問題,所以我選擇將data左移 2 bits 來計算

我會在 count == 4 or 5 時將 fft\_valid 拉高，並在這時候將輸出得數值填到 fft\_dx 裡面。

在 count <= 5 時因為還在上一輪的運算，所以先把下一輪的資料存在 temp 裡，在 count == 6 時再把資料填回去。

ready 的目的是在避免第一輪就先輸出，因為第一輪時還沒有收到完整資料。