2025 Digital IC Design Homework 3

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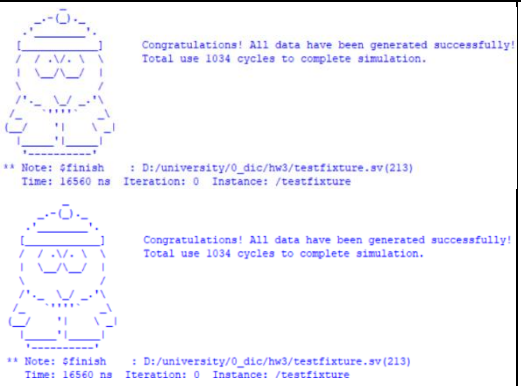
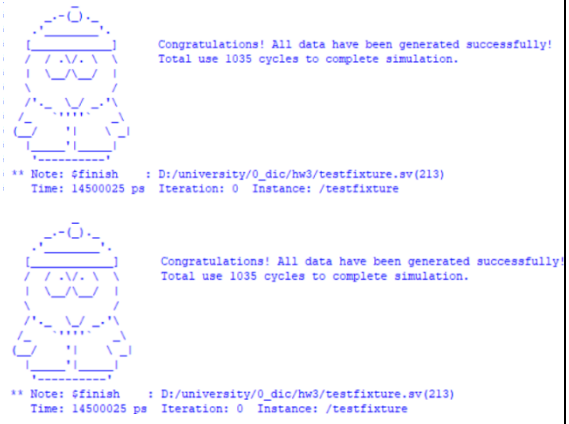
Simulation Result

Functional simulation	Pass	Pre-Layout simulation	Pass



Please specify your clock width: 14 (ns)

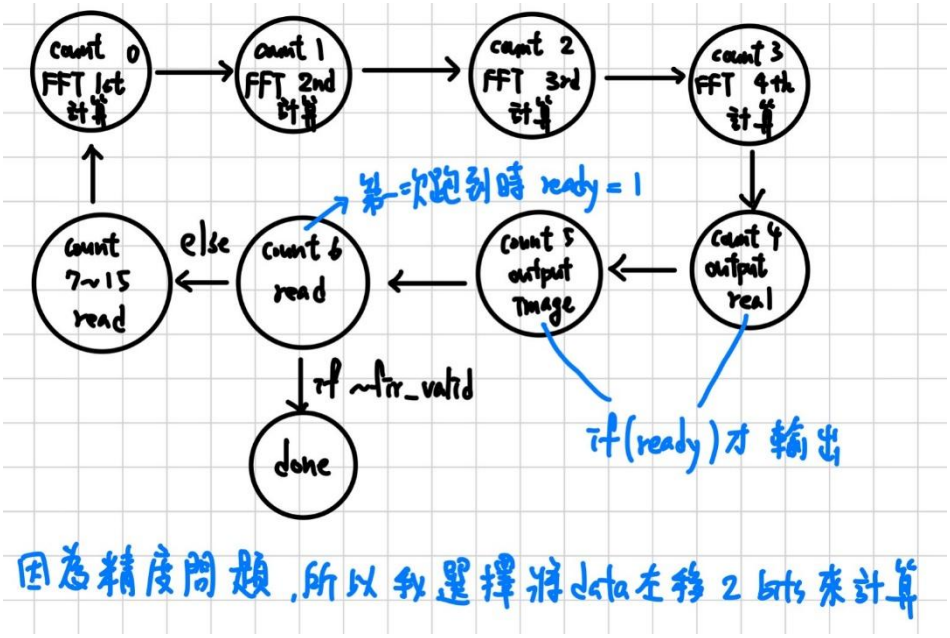


Synthesis Result

Total logic elements	4366
Total memory bits	0
Total registers	920
Embedded multiplier 9-bit elements	152

Flow Status	Successful - Sat May 10 17:51:31 2025
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	FFT
Top-level Entity Name	FFT
Family	Cyclone IV E
Device	EP4CE55F23A7
Timing Models	Final
Total logic elements	4,366 / 55,856 (8 %)
Total registers	920
Total pins	277 / 325 (85 %)
Total virtual pins	0
Total memory bits	0 / 2,396,160 (0 %)
Embedded Multiplier 9-bit elements	152 / 308 (49 %)
Total PLLs	0 / 4 (0 %)

Description of your design



我會在 count == 4 or 5 時將 fft_valid 拉高，並在這時候將輸出得數值填到 fft_dx 裡面。

在 count <= 5 時因為還在做上一輪的運算，所以先把下一輪的資料存在 temp 裡，在 count == 6 時再把資料填回去。

ready 的目的是在避免第一輪就先輸出，因為第一輪時還沒有收到完整資料。