2025 Digital IC Design Homework 2

NAME	曾立呈
Student ID	E94121038

Functional Simulation Result

Pattern1	Pattern2	Pattern3	Pattern4	Pattern5
Pass	Pass	Pass	Pass	Pass

Pattern 1

```
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/university/0_dic/hw2/testfixture.sv(162)
#    Time: 1345 ns  Iteration: 0  Instance: /testfixture
# 1
```

Pattern 2

```
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/university/0_dic/hw2/testfixture.sv(162)
#    Time: 1555 ns  Iteration: 0  Instance: /testfixture
```

Pattern 3

```
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / 0.0  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/university/0_dic/hw2/testfixture.sv(162)
#    Time: 1595 ns  Iteration: 0  Instance: /testfixture
```

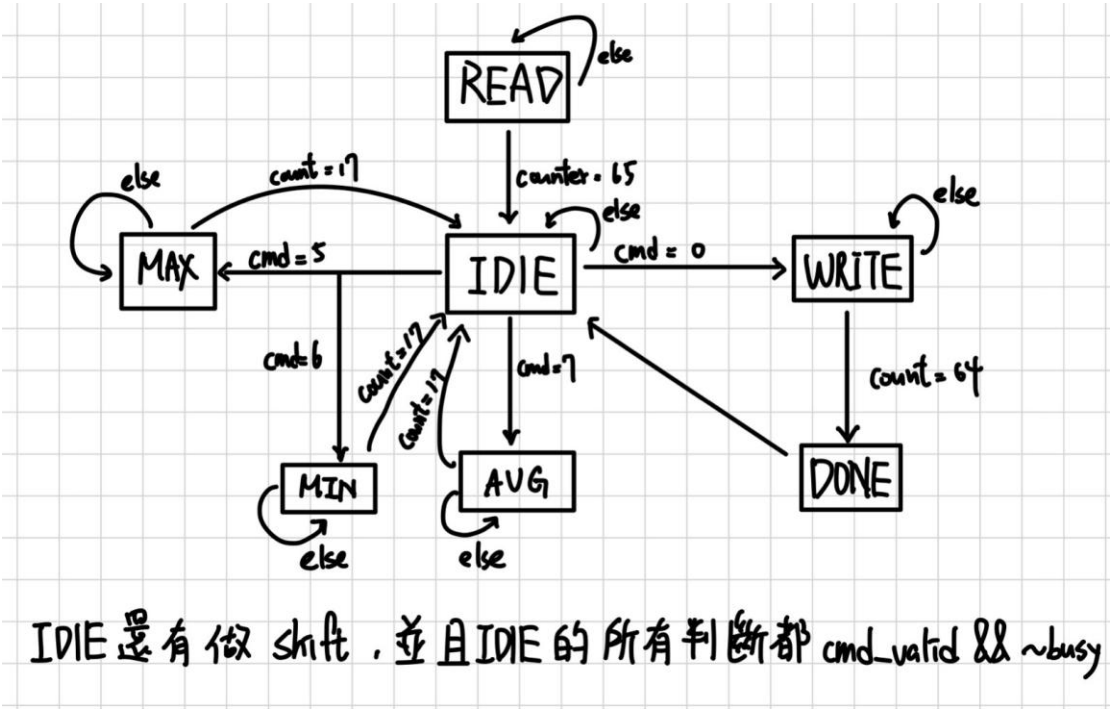
Pattern 4

```
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / O.O  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/university/0_dic/hw2/testfixture.sv(162)
#    Time: 1635 ns  Iteration: 0  Instance: /testfixture
```

Pattern 5

```
# All data have been generated successfully!
#
#                    ////////////////////////
#                    /                      /       |__||
#                    /  Congratulations !!  /      / O.O  |
#                    /                      /    /_____   |
#                    /  Simulation PASS !!  /   /^ ^ ^ \  |
#                    /                      /  |^ ^ ^ ^ |w|
#                    ////////////////////////   \m___m__|_|
#
#
# ** Note: $finish    : D:/university/0_dic/hw2/testfixture.sv(162)
#    Time: 2195 ns  Iteration: 0  Instance: /testfixture
```

LCD_CTRL Finite-State Machine Design:



READ： 讀取 IROM 的資料存到 data 裡

IDLE： 接收 cmd 的地方，若是 Shift 類型指令(只需要一個 clock)就直接在這裡處理完，其他則跳往專門的 state

WRITE： 負責將所有資料存進 IRAM 裡

MAX : 在 **16** 格內找出最大值後，再將 **16** 格所有都改成最大值
MIN : 在 **16** 格內找出最小值後，再將 **16** 格所有都改成最小值
AVG : 在 **16** 格內一格一格累加，最後再向右 **shift4** 位，把 **16** 格都改成這個值
DONE : 顧名思義就是做完所有事後進入的 **state**，負責把 **done** 拉起來