# BOYANG CHENG

## PERSONAL INFORMATION

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## EXPERIENCE

*2025.5-2025.8* **Intern, Logic Pathfinding Lab Research Scientist - DTCO,**
*Samsung Semiconductor, Inc.,* San Jose, CA, USA

*2024.5-2024.8* **Intern, Logic Pathfinding Lab Research Scientist - SRAM,**
*Samsung Semiconductor, Inc.,* San Jose, CA, USA

*2020-2022* **Research Assistant,**
*Southeast University,* Nanjing, Jiangsu, China
Advisor: **Dr. Weiwei Shan**

## EDUCATION

*2022-present* **Ph.D.** *University of Notre Dame, Notre Dame, IN, USA*
Department of Electrical Engineering
Advisor: **Dr. Ningyuan Cao**

*2016-2020* **B.S.** *Southeast University, Nanjing, Jiangsu, China*
School of Internet of Things

## RESEARCH INTERESTS

My current research interests include physical unclonable function (PUF) design, content-addressable memory (CAM) design, compute in memory (CIM), and on-chip entropy source design.

## SELECTED PUBLICATIONS

*Conferences*

*2025* L. Pei, Y. Zhou, X. Wang, X. Zhao, W. Huang, **B. Cheng**, H. Mulaosmanovic, S. Duenkel, D. Kleimaier, S. Beyer, K. Ni, M. Hou, M. Niemier, N. Cao, "Towards Uncertainty-aware Robotic Perception via Mixed-signal BNN Engine Leveraging Probabilistic Quantum Tunneling," in **DAC '25**

*2025* J. Liu, Z. Enciso, **B. Cheng**, L. Pei, S. Davis, Y. Qin, Z. Jia, X. S. Hu, Y. Shi, and N. Cao, "15.3 A 65nm Uncertainty-quantifiable Ventricular Arrhythmia Detection Engine with 1.75 $\mu$J per Inference," in **ISSCC '25**

*2024* L. Pei, Y. Qin, Z. Enciso, **B. Cheng**, J. Liu, S. Davis, Z. Jia, M. Niemier, Y. Shi, X. S. Hu, and N. Cao, "Towards Uncertainty-Quantifiable Biomedical Intelligence: Mixed-signal Compute-in-Entropy for Bayesian Neural Networks," in **ICCAD '24** (**Best Paper Award Nominee**)

*2024* J. Liu, **B. Cheng**, Z. Enciso, S. Davis, and N. Cao, "CIPUF: Towards On-chip Learnable Anomaly Detection with Compute-In-PUF Architecture," in **ISLPED '24**

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| *2024* | **B. Cheng**, J. Liu, S. Davis, Z. Enciso, Y. Zhang, and N. Cao, "VAE-HDC: Efficient and Secure Hyper-dimensional Encoder Leveraging Variation Analog Entropy," in **DAC '24** |
| *2024* | **B. Cheng**, J. Liu, S. Davis, Z. Enciso, L. Pei, M. Chang, and N. Cao, "A 65 nm Neuromorphic Bio-Signal Encoder with Compute-in-Entropy Architecture 7.13 nJ Privacy-Preserving Encoding and 2.38 Mb/mm$^2$ Item Memory Density," in **VLSI '24** |
| *2023* | J. Liu, **B. Cheng**, P. Zeng, S. Davis, M. Chang and N. Cao, "Privacy-by-Sensing with Time-domain Differentially-Private Compressed Sensing," in **DATE '23** |
| *2022* | N. Cao, J. Liu, **B. Cheng**, and M. Chang, "Stochastic Mixed-Signal Circuit Design for In-Sensor Privacy," in **ICCAD '22** |

*Journals*

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| *2025* | J. Liu, **B. Cheng**, X. Zhao, et al., "A Physically-Unclonable Bio-Signal Encoder for Privacy-preserving IoMT Applications," in *IEEE Internet of Things Journal* (**IoTJ**) |
| *2024* | S. Davis, J. Liu, **B. Cheng**, M. Chang and N. Cao, "In-Situ Privacy via Mixed-Signal Perturbation and Hardware-Secure Data Reversibility," in **TCAS-I** |
| *2023* | Y. Du, Z. Chen, **B. Cheng**, and W. Shan, "Design and analysis of leading one/zero detector based approximate multipliers," in *Microelectronics Journal* |
| *2023* | Z. Chen, Y. Du, **B. Cheng**, and W. Shan, "Design of high-efficiency complex multiplier for fault-tolerant computation," in *Integration* |
| *2022* | N. Cao, B. Chatterjee, J. Liu, **B. Cheng**, et al., "A 65 nm Wireless Image SoC Supporting On-Chip DNN Optimization and Real-Time Computation-Communication Trade-Off via Actor-Critical Neuro Controller" in **JSSC** |
| *2021* | Z. Cai, **B. Cheng**, Y. Du, X. Shang and W. Shan, "A Time-Domain Binary CNN Engine With Error-Detection-Based Resilience in 28nm CMOS," in **TCAS-II** |

## PATENTS

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| *2021* | **Ultra-low Power Keyword Spotting Neural Network Circuit**, U.S. Patent |

## PEER REVIEWS

IEEE Transactions on Very Large Scale Integration (VLSI) Systems (**TVLSI**)

IEEE Sensors Letters

IEEE Transactions on Industrial Electronics (**TIE**)

## SKILLS

**Skills:** Analog/Mixed-signal IC, Digital IC, RISC-V, Floor Planning, Customize Layout, Timing Convergence

**Software and Tools**: Virtuoso (SKILL), Innovus, Design Compiler, Python, System C, Catapult, C++, Verilog, Calibre (SVRF)