LGDP4522

176RBGx220-dot, 262,144-color 1-chip TFT LCD driver IC

Rev 0.3.1
2006-04-06

Description

The LGDP4522 is a 262,144-color one-chip controller driver LSI for a TFT liquid crystal display with resolution of 176 RGB x 220 dots, comprising a 528-channel source driver, RAM for graphics data of 176 RGB x 220 dots at maximum, a gate driver and a power supply circuit.

The LGDP4522 supports high-speed parallel interfaces to 8-, 9-, 16-, 18-bit ports and a function to write RAM data in high speed for transferring data efficiently and rewriting RAM graphics data in high speed. In addition, the LGDP4522 incorporates 6-, 16-, 18-bit RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, and DB[17:0]) and a VSYNC interface (system interface + VSYNC) for displaying a moving picture, which, with use of window address function, enable the LGDP4522 to display a moving picture easily at a position specified by a user and still pictures in other areas on the screen simultaneously. Since this combination allows transferring only moving picture data while retaining still picture data in the internal RAM intact, data transfer can be minimized and power consumption by the entire system is reduced.

The LGDP4522 can operate with low I/O interface power supply up to 1.65V, with an incorporated voltage follower circuit to generate voltage levels for driving an LCD. The LGDP4522 also supports a function to display in 8 colors and a standby mode, allowing for precise power control by software. These features make the LGDP4522 an ideal LCD driver for medium or small sized portable products supporting WWW browsers such as digital cellular phones or small PDAs, where long battery life is a measure concern.

Features

- A controller driver for a liquid crystal TFT display with resolution of 176RGB x 220-dot, capable of graphics display in 262,144 colors
- Single chip solution for a liquid crystal TFT display
- System interfaces
  - High-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports
  - Serial Peripheral Interface (SPI)
- Interfaces for moving picture display
  - 6-, 16-, 18-bit RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, DB[17:0])
  - VSYNC interface (System interface + VSYNC)
- Window address function to specify a rectangular area on the internal RAM for moving picture display
  - Facilitate moving picture display at any area on the screen via a moving picture display interface
  - Limit the data rewriting area and reduce data transfer
  - Enable moving and still picture display at the same time
- Bit operation function for facilitating graphics data processing
  - Bit-unit write data mask function
  - Pixel-unit logical/conditional write function
- Abundant functions for color display control
  - γ-correction function enabling display in 262,144 colors
  - Line-unit vertical scrolling function
- Low -power consumption architecture
  - Low operating power supplies: VDD28 = 2.4 to 3.3 V (To generate logic voltage)
Vcc = 1.7 to 1.9 V (internal logic)
IOVcc = 1.65 to 3.3 V (interface I/O)
Vci = 2.5 to 3.3 V (analog)
  - Low voltage drive: DDVDH = 4.5 to 5.5 V
  - Power saving functions (standby mode etc.)
  - Liquid crystal partial drive function, enabling partially driving an LCD panel at positions specified by a user
  - A voltage follower circuit for generating LCD driving voltage levels with a small direct current through bleeder resistors
- Incorporate step-up circuits for stepping up a liquid crystal drive voltage level up to 6 times (x6)
- 95,040 byte internal RAM
- Incorporate a 528-channel source driver and a 220-channel gate driver
- n-line liquid crystal AC drive: invert polarity at an interval of arbitrarily set n lines (n: 0 ~ 64)
- Internal oscillator and hardware reset
- Reversible source driver shift direction
- For Cst structure only
- Internal 32-bit EPROM for VCOMH level setting (4-times programmable)

Power Supply Specifications

Table 1

No.	Item		LGDP4522
1	TFT source lines		528 pins (176 x RGB)
2	TFT gate lines		220 pins
3	Capacitor structure of TFT display		Cst structure only (common Vcom formula)
4	Liquid crystal drive output	S1 to S528	V0 to V63 grayscales
		G1 to G220	VGH to VGL
		Vcom1/11/2/21	VcomH – VcomL: amplitude = electronic volumes VcomH = VcomR: adjusted with an external resistor
5	Input voltage	IOVcc	1.65 – 3.30 V
		VDD28	2.40 – 3.30 V
		Vcc	1.7 – 1.9 V
		Vci	2.50 – 3.30 V
6	Internal step-up circuits	VLOUT1 (DDVDH)	Vci ×2
		VLOUT2 (VGH)	Vci ×2, ×5, ×6
		VLOUT3 (VGL)	Vci ×-3, ×-4, ×-5
		VLOUT4 (VCL)	Vci ×-1

Block Diagram

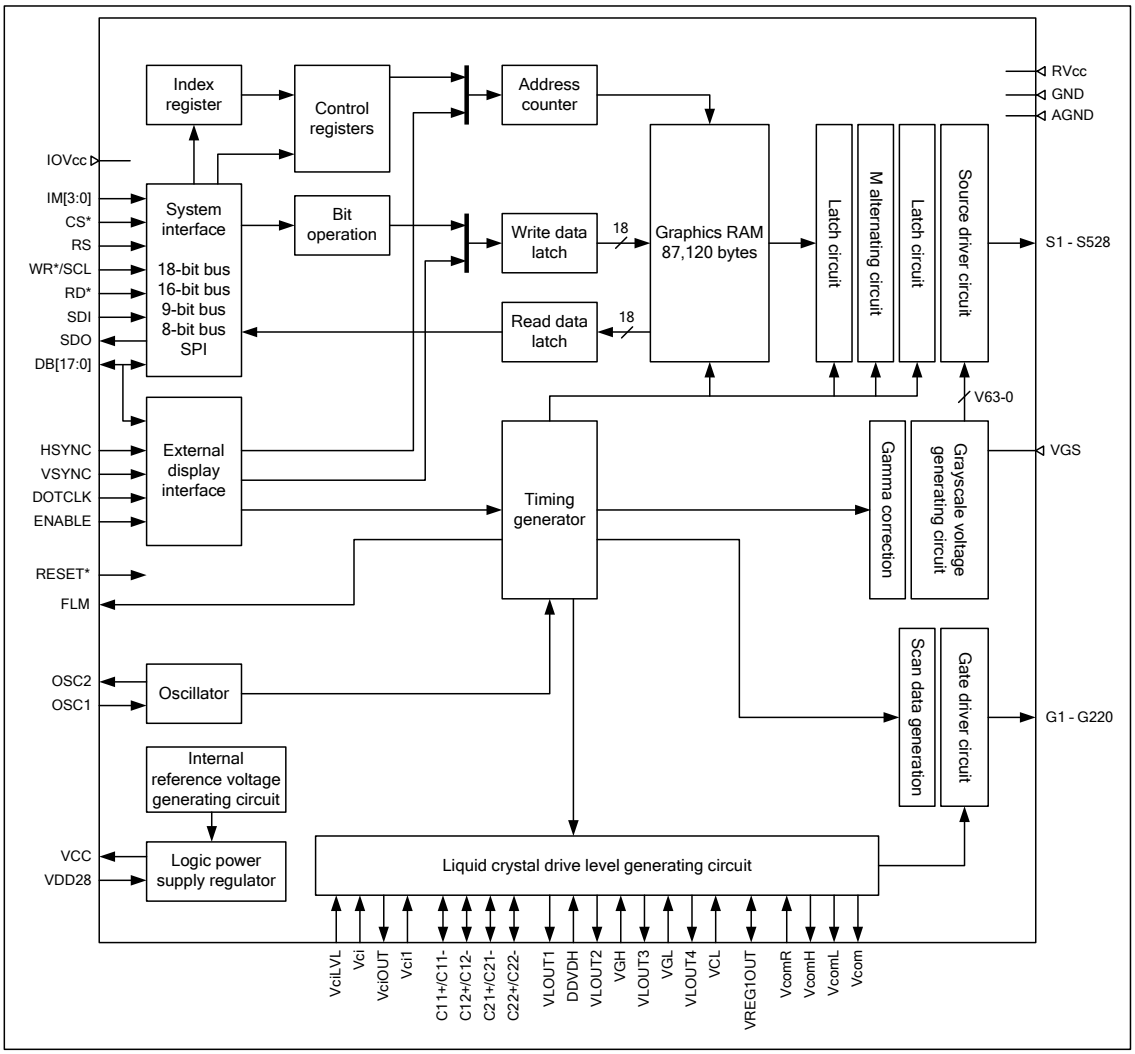


Figure 1

Pin Function

Table 2

<table>
<tr><th>Name</th><th># pins</th><th>I/O</th><th>Connected to</th><th>Function</th></tr>
<tr><td>IM[0]_ID,
IM[3:1]</td><td>4</td><td>I</td><td>GND/IOVcc</td><td>MPU interface mode select signal.
In SPI mode, the IM[0] pin is used to set the ID of device code.

<table><tr><th>IM[3:0]</th><th>Interface mode</th><th>Data pins</th></tr><tr><td>000*</td><td>Setting disabled</td><td>-</td></tr><tr><td>0010</td><td>80-system 16-bit interface</td><td>DB[17:10],
DB[8:1]</td></tr><tr><td>0011</td><td>80-system 8-bit interface</td><td>DB[17:10]</td></tr><tr><td>010*</td><td>Serial peripheral interface (SPI)</td><td>SDI, SDO</td></tr><tr><td>011*</td><td>Setting disabled</td><td>-</td></tr><tr><td>100*</td><td>Setting disabled</td><td>-</td></tr><tr><td>1010</td><td>80-system 18-bit interface</td><td>DB[17:0]</td></tr><tr><td>1011</td><td>80-system 9-bit interface</td><td>DB[17:9]</td></tr><tr><td>11**</td><td>Setting disabled</td><td>-</td></tr></table></td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Chip select signal (active low).
Low: LGDP4522 is selected and accessible.
High: LGDP4522 is not selected and not accessible.
Fix to the GND level when not in use.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Register select signal.
Low: selects the index/status register.
High: selects a control register.</td></tr>
<tr><td>WR*_SCL</td><td>1</td><td>I</td><td>MPU</td><td>Write strobe (active low) in 80-system bus interface mode.
Serial clock input in SPI mode.</td></tr>
<tr><td>RD*</td><td>1</td><td>I</td><td>MPU</td><td>Read strobe (active low) in 80-system bus interface mode.
Fix to either IOVcc or GND level in SPI mode.</td></tr>
<tr><td>SDI</td><td>1</td><td>I</td><td>MPU</td><td>Serial data input in SPI mode.
Data are input on the rising edge of the SCL signal. Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>SDO</td><td>1</td><td>O</td><td>MPU</td><td>Serial data output in SPI mode.
Data are output on the falling edge of the SCL signal. Leave the pin open when not in use.</td></tr>
<tr><td>DB[17:0]</td><td>18</td><td>I/O</td><td>MPU</td><td>Parallel bidirectional data bus.
Unused pins must be fixed either IOVcc or GND level.</td></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU</td><td>Data enable signal in RGB interface mode.
Low: select (accessible).
High: not select (inaccessible).
The EPL bit inverts the polarity of the ENABLE signal. Fix to either IOVcc or GND level when not in use.</td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Frame synchronization signal.
When VSPL = “0”, it is active low.
When VSPL = “1”, it is active high.
Fix to the IOVcc level when not in use.</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU</td><td>Line synchronization signal.
When HSPL = “0”, it is active low.
When HSPL = “1”, it is active high.
Fix to the IOVcc level when not in use.</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU</td><td>Dot clock signal.
When DPL = “0”, input data on the rising edge of DOTCLK.
When DPL = “1”, input data on the falling edge of DOTCLK.
Fix to the IOVcc level when not in use.</td></tr>
<tr><td>RESET*</td><td>1</td><td>I</td><td>MPU or external RC circuit</td><td>Hardware reset (active low).
Be sure to execute a power-on reset after supplying power.</td></tr>
<tr><td>S1 to S528</td><td>528</td><td>O</td><td>LCD</td><td>Source line outputs to LCD.</td></tr>
<tr><td>G1 to G220</td><td>220</td><td>O</td><td>LCD</td><td>Gate line outputs to LCD.</td></tr>
</table>

Name	# pins	I/O	Connected to	Function
Vcom	1	O	TFT panel common electrode	Supply voltage to the common electrode of TFT panel. Vcom is AC voltages alternating between the VcomH and VcomL levels. The alternating cycle is set by M signal. Connect to the common electrode of TFT panel. All outputs come from the same node.
VcomH	1	O	Stabilizing capacitor	The high level of Vcom1/11/2/21 AC voltage. Connect to a stabilizing capacitor.
VcomL	1	O	Stabilizing capacitor or open	The low level of Vcom1/11/2/21 AC voltage. Adjust the VcomL level with the VDV bits. Connect to a stabilizing capacitor. To fix the VcomL level to GND, set VCOMG to “0”. In this case, capacitor connection is not necessary.
VcomR	1	I	Variable resistor or open	Reference level to generate the VcomH level either with an externally connected variable resistor or by setting the register of the LGDP4522. When using a variable resistor, halt the internal VcomH adjusting circuit by setting the register and place the resister between VREG1OUT and GND. When generating the VcomH level by setting the register, leave this pin open.
C11+, C11−	2	-	Step-up capacitor	Pins to connect a capacitor for the internal step-up circuit 1. Leave the pins open when not using the circuit.
C12+, C12−, C21+, C21−, C22+, C22−	2	-	Step-up capacitor	Pins to connect capacitors for the internal step-up circuit 2. Connect capacitors according to step-up rate. Leave the pins open when not using the circuit.
OSC1, OSC2	2	I/O	Oscillation resistor	Pins to connect a resistor for RC oscillation.
FLM	1	O	MPU or open	Frame head pulse signal. This is used when writing RAM data in synchronization with display frame. Leave the pin open when not in use.
Vci	1	I	Power supply	Supply voltage to the analog circuit. Connect to an external power supply of 2.5 to 3.3V.
VciLVL	1	I	Power supply	Reference level to generate the VciOUT/REGP level according to 0the step-up rate set with the VC bits. Be sure to connect VciLVL with Vci on the FPC to prevent noise.
VciOUT	1	O	Stabilizing capacitor, Vci1	Internal reference voltage level of amplitude VciLVL−GND. Place a stabilizing capacitor between GND.
Vci1	1	I/O	VciOUT	Reference voltage input to the step-up circuit 1. When not using the internal reference voltage, connect to an external power supply up to 2.75V.
VLOUT1	1	O	Stabilizing capacitor, DDVDH	Output voltage from the step-up circuit 1. Place a stabilizing capacitor between GND. Place a schottky diode between Vci. VLOUT1 = 4.5 to 5.5V (twice the Vci1 level).
VLOUT2	1	O	Stabilizing capacitor, VGH	An output voltage from the step-up circuit 2. The step-up rate is set with the BT bits. Place a stabilizing capacitor between GND. Place a schottky diode between Vci. VLOUT2 = max 16.5V (4 to 6 times the Vci1 level)
VLOUT3	1	O	Stabilizing capacitor, VGL	An output voltage from the step-up circuit 2. The step-up rate is set with the BT bits. Place a stabilizing capacitor between GND. Place a schottky diode between Vci. VLOUT3 = min −16.5V (−3 to −5 times the Vci1 level)
VLOUT4	1	O	Stabilizing capacitor, VCL	An output voltage from the step-up circuit 2. The step-up rate is set with the BT bits. Place a stabilizing capacitor between GND. Place a schottky diode between Vci. VLOUT4 = 0 to −3.3V (−1 times the Vci1 level)
DDVDH	1	I	VLOUT1	Power supply to the source driver’s LCD output unit and an input voltage to the step-up circuit 2.
VGH	1	I	VLOUT2	A supply voltage to drive gate lines of the TFT panel. Connect to VLOUT2.
VGL	1	I	VLOUT3	A supply voltage to drive gate lines of the TFT panel. Connect to VLOUT3.

Name	# pins	I/O	Connected to	Function
VCL	1	I	VLOUT4	A supply voltage to generate the VcomL level. Connect to VLOUT4.
VREG1OUT	1	I/O	Stabilizing capacitor or power supply	A voltage level of DDVDH−GND, generated from the reference level of Vci−GND according to the rate set with the VRH bits. VREG1OUT is (1) a source driver grayscale reference voltage VDH, (2) a VcomH level reference voltage, and (3) a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 to (DDVDH – 0.5) V
VDD28	1	-	Power supply	Power supply to generate the internal logic power supply. Vcc = 2.4 to 3.3V
Vcc	1	-	Power supply	Generated power supply to the internal logic. Vcc = 1.7 to 1.9V
Vccout	1	I/O	Stabilizing capacitor, Vcc	Internal logic regulator output. Connect Vcc to a stabilizing capacitor.
RVcc	1	-	Power supply	Power supply to the internal RAM. RVcc and Vcc must be at the same electrical potential.
IOVcc	1	-	Power supply	Power supply to the interface pins: IOVcc = 1.65 to 3.3V. IOVcc and the internal logic voltage Vcc must be supplied in the same condition. In case of COG, connect to Vcc on the FPC if IOVcc = Vcc, to prevent noise.
GND	1	-	Power supply	Digital ground: GND = 0V.
AGND	1	-	Power supply	Analog ground: AGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
RGND	1	-	Power supply	Ground to the internal RAM. RGND = 0V. In case of COG, connect to GND on the FPC to prevent noise.
TEST1	1	I	GND	Test pin. Be sure to connect to GND.
VGS	1		GND or external resistor	Reference level for the grayscale voltage generation circuit. The VGS level can be changed by connecting to an external resistor.
VPP	1	I/O	Power Supply	7.2V Power supply for internal EPROM writing
VCMSEL	1	I	GND or VCC or open	If VCMSEL is set to high, VCOM level control comes from EPROM block. If VCMSEL is set to low, VCOM level control comes from internal registers set by MPU. If the setting by this pin is not to be preferable, it can be open.

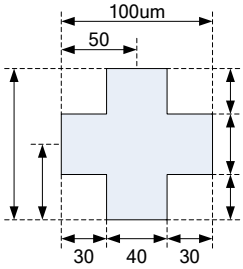
PAD Arrangement

- Chip size: 17.2 um x 1.43 um
  (With seal ring but without scribe line)
- Chip thickness: 400 um
- PAD coordinate: PAD center

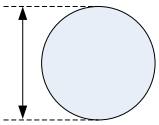
- Au bump size
  1) Nos. 1-241, 1006-1010: 50 um x 80 um
  2) Nos. 242-1005: 19 um x 120 um

- Alignment marks

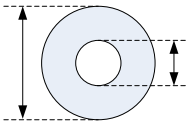
1-a, 1-b) Coordinate (X, Y) = (±8422.0, 536.9)



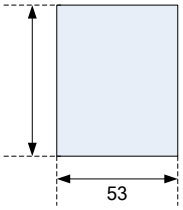
2-a) Coordinate (X, Y) = (-8421.5, -581.5)



2-b) Coordinate (X, Y) = (8421.5, -581.5)



3-a), 3-b) Coordinate (X, Y) = (±8421.5, -505.0)



100um

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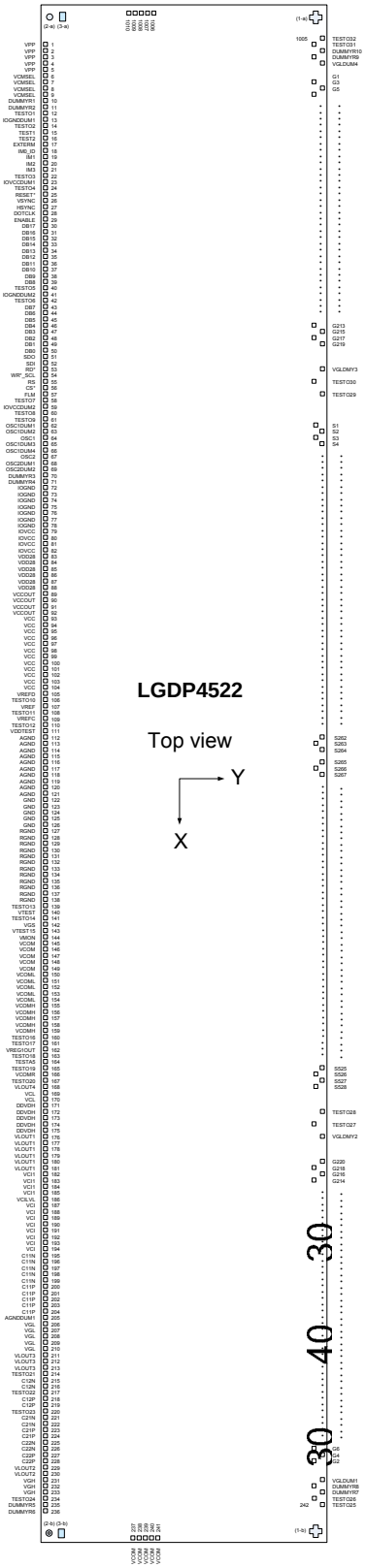


PAD Coordinate

Pad #	Pad name	X	Y
1	**VPP**	-8225	-581.5
2	**VPP**	-8155	-581.5
3	**VPP**	-8085	-581.5
4	**VPP**	-8015	-581.5
5	**VPP**	-7945	-581.5
6	**VCMSEL**	-7875	-581.5
7	**VCMSEL**	-7805	-581.5
8	**VCMSEL**	-7735	-581.5
9	**VCMSEL**	-7665	-581.5
10	DUMMYR1	-7595	-581.5
11	DUMMYR2	-7525	-581.5
12	TESTO1	-7455	-581.5
13	IOGNDDUM1	-7385	-581.5
14	TESTO2	-7315	-581.5
15	TEST1	-7245	-581.5
16	TEST2	-7175	-581.5
17	EXTERM	-7105	-581.5
18	IM0_ID	-7035	-581.5
19	IM1	-6965	-581.5
20	IM2	-6895	-581.5
21	IM3	-6825	-581.5
22	TESTO3	-6755	-581.5
23	IOVCCDUM1	-6685	-581.5
24	TESTO4	-6615	-581.5
25	RESET*	-6545	-581.5
26	VSYNC	-6475	-581.5
27	HSYNC	-6405	-581.5
28	DOTCLK	-6335	-581.5
29	ENABLE	-6265	-581.5
30	DB17	-6195	-581.5
31	DB16	-6125	-581.5
32	DB15	-6055	-581.5
33	DB14	-5985	-581.5
34	DB13	-5915	-581.5
35	DB12	-5845	-581.5
36	DB11	-5775	-581.5
37	DB10	-5705	-581.5
38	DB9	-5635	-581.5
39	DB8	-5565	-581.5
40	TESTO5	-5495	-581.5
41	IOGNDDUM2	-5425	-581.5
42	TESTO6	-5355	-581.5
43	DB7	-5285	-581.5
44	DB6	-5215	-581.5
45	DB5	-5145	-581.5
46	DB4	-5075	-581.5
47	DB3	-5005	-581.5
48	DB2	-4935	-581.5
49	DB1	-4865	-581.5
50	DB0	-4795	-581.5
51	SDO	-4725	-581.5
52	SDI	-4655	-581.5
53	RD*	-4585	-581.5
54	WR*_SCL	-4515	-581.5
55	RS	-4445	-581.5
56	CS*	-4375	-581.5
57	FLM	-4305	-581.5
58	TESTO7	-4235	-581.5
59	IOVCCDUM2	-4165	-581.5
60	TESTO8	-4095	-581.5
61	TESTO9	-4025	-581.5
62	OSC1DUM1	-3955	-581.5
63	OSC1DUM2	-3885	-581.5
64	OSC1	-3815	-581.5
65	OSC1DUM3	-3745	-581.5
66	OSC1DUM4	-3675	-581.5
67	OSC2	-3605	-581.5
68	OSC2DUM1	-3535	-581.5
69	OSC2DUM2	-3465	-581.5
70	DUMMYR3	-3395	-581.5
71	DUMMYR4	-3325	-581.5
72	IOGND	-3255	-581.5
73	IOGND	-3185	-581.5
74	IOGND	-3115	-581.5
75	IOGND	-3045	-581.5
76	IOGND	-2975	-581.5
77	IOGND	-2905	-581.5
78	IOGND	-2835	-581.5
79	IOVCC	-2765	-581.5
80	IOVCC	-2695	-581.5
81	IOVCC	-2625	-581.5
82	IOVCC	-2555	-581.5
83	**VDD28**	-2485	-581.5
84	**VDD28**	-2415	-581.5
85	**VDD28**	-2345	-581.5
86	**VDD28**	-2275	-581.5
87	**VDD28**	-2205	-581.5
88	**VDD28**	-2135	-581.5
89	**VCCOUT**	-2065	-581.5
90	**VCCOUT**	-1995	-581.5
91	**VCCOUT**	-1925	-581.5
92	**VCCOUT**	-1855	-581.5
93	**VCC**	-1785	-581.5
94	**VCC**	-1715	-581.5
95	**VCC**	-1645	-581.5
96	**VCC**	-1575	-581.5
97	**VCC**	-1505	-581.5
98	**VCC**	-1435	-581.5
99	**VCC**	-1365	-581.5
100	**VCC**	-1295	-581.5
101	**VCC**	-1225	-581.5
102	**VCC**	-1155	-581.5
103	**VCC**	-1085	-581.5
104	**VCC**	-1015	-581.5
105	VREFD	-945	-581.5
106	TESTO10	-875	-581.5
107	VREF	-805	-581.5
108	TESTO11	-735	-581.5
109	VREFC	-665	-581.5
110	TESTO12	-595	-581.5
111	VDDTEST	-525	-581.5
112	AGND	-455	-581.5
113	AGND	-385	-581.5
114	AGND	-315	-581.5
115	AGND	-245	-581.5
116	AGND	-175	-581.5
117	AGND	-105	-581.5
118	AGND	-35	-581.5
119	AGND	35	-581.5
120	AGND	105	-581.5
121	AGND	175	-581.5
122	GND	245	-581.5
123	GND	315	-581.5
124	GND	385	-581.5
125	GND	455	-581.5
126	GND	525	-581.5
127	RGND	595	-581.5
128	RGND	665	-581.5
129	RGND	735	-581.5
130	RGND	805	-581.5
131	RGND	875	-581.5
132	RGND	945	-581.5
133	RGND	1015	-581.5
134	RGND	1085	-581.5
135	RGND	1155	-581.5
136	RGND	1225	-581.5
137	RGND	1295	-581.5
138	RGND	1365	-581.5
139	TESTO13	1435	-581.5
140	VTEST	1505	-581.5
141	TESTO14	1575	-581.5
142	VGS	1645	-581.5
143	TESTO15	1715	-581.5
144	VMON	1785	-581.5
145	VCOM	1855	-581.5
146	VCOM	1925	-581.5
147	VCOM	1995	-581.5
148	VCOM	2065	-581.5
149	VCOM	2135	-581.5
150	**VCOML**	2205	-581.5
151	**VCOML**	2275	-581.5
152	**VCOML**	2345	-581.5
153	**VCOML**	2415	-581.5
154	**VCOML**	2485	-581.5
155	**VCOMH**	2555	-581.5
156	**VCOMH**	2625	-581.5
157	**VCOMH**	2695	-581.5
158	**VCOMH**	2765	-581.5
159	**VCOMH**	2835	-581.5
160	TESTO16	2905	-581.5
161	TESTO17	2975	-581.5
162	VREG1OUT	3045	-581.5
163	TESTO18	3115	-581.5
164	TESTA5	3185	-581.5
165	TESTO19	3255	-581.5
166	VCOMR	3325	-581.5
167	TESTO20	3395	-581.5
168	**VLOUT4**	3465	-581.5
169	**VCL**	3535	-581.5
170	**VCL**	3605	-581.5
171	DDVDH	3675	-581.5
172	DDVDH	3745	-581.5
173	DDVDH	3815	-581.5
174	DDVDH	3885	-581.5
175	DDVDH	3955	-581.5
176	**VLOUT1**	4025	-581.5
177	**VLOUT1**	4095	-581.5
178	**VLOUT1**	4165	-581.5
179	VCIOUT	4235	-581.5
180	VCIOUT	4305	-581.5
181	VCIOUT	4375	-581.5
182	VCI1	4445	-581.5
183	VCI1	4515	-581.5
184	VCI1	4585	-581.5
185	VCI1	4655	-581.5
186	VCILVL	4725	-581.5
187	VCI	4795	-581.5
188	VCI	4865	-581.5
189	VCI	4935	-581.5
190	VCI	5005	-581.5
191	VCI	5075	-581.5
192	VCI	5145	-581.5
193	VCI	5215	-581.5
194	VCI	5285	-581.5
195	C11N	5355	-581.5
196	C11N	5425	-581.5
197	C11N	5495	-581.5
198	C11N	5565	-581.5
199	C11N	5635	-581.5
200	C11P	5705	-581.5
201	C11P	5775	-581.5
202	C11P	5845	-581.5
203	C11P	5915	-581.5
204	C11P	5985	-581.5
205	AGNDDUM1	6055	-581.5
206	VGL	6125	-581.5
207	VGL	6195	-581.5
208	VGL	6265	-581.5
209	VGL	6335	-581.5
210	VGL	6405	-581.5
211	**VLOUT3**	6475	-581.5
212	**VLOUT3**	6545	-581.5
213	**VLOUT3**	6615	-581.5
214	TESTO21	6685	-581.5
215	**C12N**	6755	-581.5
216	**C12N**	6825	-581.5
217	TESTO22	6895	-581.5
218	**C12P**	6965	-581.5
219	**C12P**	7035	-581.5
220	TESTO23	7105	-581.5
221	C21N	7175	-581.5
222	C21N	7245	-581.5
223	C21P	7315	-581.5
224	C21P	7385	-581.5
225	C22N	7455	-581.5
226	C22N	7525	-581.5
227	C22P	7595	-581.5
228	C22P	7665	-581.5
229	**VLOUT2**	7735	-581.5
230	**VLOUT2**	7805	-581.5
231	VGH	7875	-581.5
232	VGH	7945	-581.5
233	VGH	8015	-581.5
234	TESTO24	8085	-581.5
235	DUMMYR5	8155	-581.5
236	DUMMYR6	8225	-581.5
237	VCOM	8466.5	-410.7
238	VCOM	8466.5	-340.7
239	VCOM	8466.5	-270.7
240	VCOM	8466.5	-200.7
241	VCOM	8466.5	-130.7
242	TESTO25	8210.5	566.5
243	TESTO26	8189.5	411.5
244	DUMMYR7	8168.5	566.5
245	DUMMYR8	8147.5	411.5
246	VGLDMY1	8126.5	566.5
247	G2	8105.5	411.5
248	G4	8084.5	566.5
249	G6	8063.5	411.5

Pad #	Pad name	X	Y
250	G8	8042.5	566.5
251	G10	8021.5	411.5
252	G12	8000.5	566.5
253	G14	7979.5	411.5
254	G16	7958.5	566.5
255	G18	7937.5	411.5
256	G20	7916.5	566.5
257	G22	7895.5	411.5
258	G24	7874.5	566.5
259	G26	7853.5	411.5
260	G28	7832.5	566.5
261	G30	7811.5	411.5
262	G32	7790.5	566.5
263	G34	7769.5	411.5
264	G36	7748.5	566.5
265	G38	7727.5	411.5
266	G40	7706.5	566.5
267	G42	7685.5	411.5
268	G44	7664.5	566.5
269	G46	7643.5	411.5
270	G48	7622.5	566.5
271	G50	7601.5	411.5
272	G52	7580.5	566.5
273	G54	7559.5	411.5
274	G56	7538.5	566.5
275	G58	7517.5	411.5
276	G60	7496.5	566.5
277	G62	7475.5	411.5
278	G64	7454.5	566.5
279	G66	7433.5	411.5
280	G68	7412.5	566.5
281	G70	7391.5	411.5
282	G72	7370.5	566.5
283	G74	7349.5	411.5
284	G76	7328.5	566.5
285	G78	7307.5	411.5
286	G80	7286.5	566.5
287	G82	7265.5	411.5
288	G84	7244.5	566.5
289	G86	7223.5	411.5
290	G88	7202.5	566.5
291	G90	7181.5	411.5
292	G92	7160.5	566.5
293	G94	7139.5	411.5
294	G96	7118.5	566.5
295	G98	7097.5	411.5
296	G100	7076.5	566.5
297	G102	7055.5	411.5
298	G104	7034.5	566.5
299	G106	7013.5	411.5
300	G108	6992.5	566.5
301	G110	6971.5	411.5
302	G112	6950.5	566.5
303	G114	6929.5	411.5
304	G116	6908.5	566.5
305	G118	6887.5	411.5
306	G120	6866.5	566.5
307	G122	6845.5	411.5
308	G124	6824.5	566.5
309	G126	6803.5	411.5
310	G128	6782.5	566.5
311	G130	6761.5	411.5
312	G132	6740.5	566.5
313	G134	6719.5	411.5
314	G136	6698.5	566.5
315	G138	6677.5	411.5
316	G140	6656.5	566.5
317	G142	6635.5	411.5
318	G144	6614.5	566.5
319	G146	6593.5	411.5
320	G148	6572.5	566.5
321	G150	6551.5	411.5
322	G152	6530.5	566.5
323	G154	6509.5	411.5
324	G156	6488.5	566.5
325	G158	6467.5	411.5
326	G160	6446.5	566.5
327	G162	6425.5	411.5
328	G164	6404.5	566.5
329	G166	6383.5	411.5
330	G168	6362.5	566.5
331	G170	6341.5	411.5
332	G172	6320.5	566.5
333	G174	6299.5	411.5
334	G176	6278.5	566.5
335	G178	6257.5	411.5
336	G180	6236.5	566.5

Pad #	Pad name	X	Y
337	G182	6215.5	411.5
338	G184	6194.5	566.5
339	G186	6173.5	411.5
340	G188	6152.5	566.5
341	G190	6131.5	411.5
342	G192	6110.5	566.5
343	G194	6089.5	411.5
344	G196	6068.5	566.5
345	G198	6047.5	411.5
346	G200	6026.5	566.5
347	G202	6005.5	411.5
348	G204	5984.5	566.5
349	G206	5963.5	411.5
350	G208	5942.5	566.5
351	G210	5921.5	411.5
352	G212	5900.5	566.5
353	G214	5879.5	411.5
354	G216	5858.5	566.5
355	G218	5837.5	411.5
356	G220	5816.5	566.5
357	VGLDMY2	5795.5	411.5
358	TESTO27	5774.5	566.5
359	TESTO28	5554.5	566.5
360	S528	5533.5	411.5
361	S527	5512.5	566.5
362	S526	5491.5	411.5
363	S525	5470.5	566.5
364	S524	5449.5	411.5
365	S523	5428.5	566.5
366	S522	5407.5	411.5
367	S521	5386.5	566.5
368	S520	5365.5	411.5
369	S519	5344.5	566.5
370	S518	5323.5	411.5
371	S517	5302.5	566.5
372	S516	5281.5	411.5
373	S515	5260.5	566.5
374	S514	5239.5	411.5
375	S513	5218.5	566.5
376	S512	5197.5	411.5
377	S511	5176.5	566.5
378	S510	5155.5	411.5
379	S509	5134.5	566.5
380	S508	5113.5	411.5
381	S507	5092.5	566.5
382	S506	5071.5	411.5
383	S505	5050.5	566.5
384	S504	5029.5	411.5
385	S503	5008.5	566.5
386	S502	4987.5	411.5
387	S501	4966.5	566.5
388	S500	4945.5	411.5
389	S499	4924.5	566.5
390	S498	4903.5	411.5
391	S497	4882.5	566.5
392	S496	4861.5	411.5
393	S495	4840.5	566.5
394	S494	4819.5	411.5
395	S493	4798.5	566.5
396	S492	4777.5	411.5
397	S491	4756.5	566.5
398	S490	4735.5	411.5
399	S489	4714.5	566.5
400	S488	4693.5	411.5
401	S487	4672.5	566.5
402	S486	4651.5	411.5
403	S485	4630.5	566.5
404	S484	4609.5	411.5
405	S483	4588.5	566.5
406	S482	4567.5	411.5
407	S481	4546.5	566.5
408	S480	4525.5	411.5
409	S479	4504.5	566.5
410	S478	4483.5	411.5
411	S477	4462.5	566.5
412	S476	4441.5	411.5
413	S475	4420.5	566.5
414	S474	4399.5	411.5
415	S473	4378.5	566.5
416	S472	4357.5	411.5
417	S471	4336.5	566.5
418	S470	4315.5	411.5
419	S469	4294.5	566.5
420	S468	4273.5	411.5
421	S467	4252.5	566.5
422	S466	4231.5	411.5
423	S465	4210.5	566.5

Pad #	Pad name	X	Y
424	S464	4189.5	411.5
425	S463	4168.5	566.5
426	S462	4147.5	411.5
427	S461	4126.5	566.5
428	S460	4105.5	411.5
429	S459	4084.5	566.5
430	S458	4063.5	411.5
431	S457	4042.5	566.5
432	S456	4021.5	411.5
433	S455	4000.5	566.5
434	S454	3979.5	411.5
435	S453	3958.5	566.5
436	S452	3937.5	411.5
437	S451	3916.5	566.5
438	S450	3895.5	411.5
439	S449	3874.5	566.5
440	S448	3853.5	411.5
441	S447	3832.5	566.5
442	S446	3811.5	411.5
443	S445	3790.5	566.5
444	S444	3769.5	411.5
445	S443	3748.5	566.5
446	S442	3727.5	411.5
447	S441	3706.5	566.5
448	S440	3685.5	411.5
449	S439	3664.5	566.5
450	S438	3643.5	411.5
451	S437	3622.5	566.5
452	S436	3601.5	411.5
453	S435	3580.5	566.5
454	S434	3559.5	411.5
455	S433	3538.5	566.5
456	S432	3517.5	411.5
457	S431	3496.5	566.5
458	S430	3475.5	411.5
459	S429	3454.5	566.5
460	S428	3433.5	411.5
461	S427	3412.5	566.5
462	S426	3391.5	411.5
463	S425	3370.5	566.5
464	S424	3349.5	411.5
465	S423	3328.5	566.5
466	S422	3307.5	411.5
467	S421	3286.5	566.5
468	S420	3265.5	411.5
469	S419	3244.5	566.5
470	S418	3223.5	411.5
471	S417	3202.5	566.5
472	S416	3181.5	411.5
473	S415	3160.5	566.5
474	S414	3139.5	411.5
475	S413	3118.5	566.5
476	S412	3097.5	411.5
477	S411	3076.5	566.5
478	S410	3055.5	411.5
479	S409	3034.5	566.5
480	S408	3013.5	411.5
481	S407	2992.5	566.5
482	S406	2971.5	411.5
483	S405	2950.5	566.5
484	S404	2929.5	411.5
485	S403	2908.5	566.5
486	S402	2887.5	411.5
487	S401	2866.5	566.5
488	S400	2845.5	411.5
489	S399	2824.5	566.5
490	S398	2803.5	411.5
491	S397	2782.5	566.5
492	S396	2761.5	411.5
493	S395	2740.5	566.5
494	S394	2719.5	411.5
495	S393	2698.5	566.5
496	S392	2677.5	411.5
497	S391	2656.5	566.5
498	S390	2635.5	411.5
499	S389	2614.5	566.5
500	S388	2593.5	411.5
501	S387	2572.5	566.5
502	S386	2551.5	411.5
503	S385	2530.5	566.5
504	S384	2509.5	411.5
505	S383	2488.5	566.5
506	S382	2467.5	411.5
507	S381	2446.5	566.5
508	S380	2425.5	411.5
509	S379	2404.5	566.5
510	S378	2383.5	411.5

Pad #	Pad name	X	Y
511	S377	2362.5	566.5
512	S376	2341.5	411.5
513	S375	2320.5	566.5
514	S374	2299.5	411.5
515	S373	2278.5	566.5
516	S372	2257.5	411.5
517	S371	2236.5	566.5
518	S370	2215.5	411.5
519	S369	2194.5	566.5
520	S368	2173.5	411.5
521	S367	2152.5	566.5
522	S366	2131.5	411.5
523	S365	2110.5	566.5
524	S364	2089.5	411.5
525	S363	2068.5	566.5
526	S362	2047.5	411.5
527	S361	2026.5	566.5
528	S360	2005.5	411.5
529	S359	1984.5	566.5
530	S358	1963.5	411.5
531	S357	1942.5	566.5
532	S356	1921.5	411.5
533	S355	1900.5	566.5
534	S354	1879.5	411.5
535	S353	1858.5	566.5
536	S352	1837.5	411.5
537	S351	1816.5	566.5
538	S350	1795.5	411.5
539	S349	1774.5	566.5
540	S348	1753.5	411.5
541	S347	1732.5	566.5
542	S346	1711.5	411.5
543	S345	1690.5	566.5
544	S344	1669.5	411.5
545	S343	1648.5	566.5
546	S342	1627.5	411.5
547	S341	1606.5	566.5
548	S340	1585.5	411.5
549	S339	1564.5	566.5
550	S338	1543.5	411.5
551	S337	1522.5	566.5
552	S336	1501.5	411.5
553	S335	1480.5	566.5
554	S334	1459.5	411.5
555	S333	1438.5	566.5
556	S332	1417.5	411.5
557	S331	1396.5	566.5
558	S330	1375.5	411.5
559	S329	1354.5	566.5
560	S328	1333.5	411.5
561	S327	1312.5	566.5
562	S326	1291.5	411.5
563	S325	1270.5	566.5
564	S324	1249.5	411.5
565	S323	1228.5	566.5
566	S322	1207.5	411.5
567	S321	1186.5	566.5
568	S320	1165.5	411.5
569	S319	1144.5	566.5
570	S318	1123.5	411.5
571	S317	1102.5	566.5
572	S316	1081.5	411.5
573	S315	1060.5	566.5
574	S314	1039.5	411.5
575	S313	1018.5	566.5
576	S312	997.5	411.5
577	S311	976.5	566.5
578	S310	955.5	411.5
579	S309	934.5	566.5
580	S308	913.5	411.5
581	S307	892.5	566.5
582	S306	871.5	411.5
583	S305	850.5	566.5
584	S304	829.5	411.5
585	S303	808.5	566.5
586	S302	787.5	411.5
587	S301	766.5	566.5
588	S300	745.5	411.5
589	S299	724.5	566.5
590	S298	703.5	411.5
591	S297	682.5	566.5
592	S296	661.5	411.5
593	S295	640.5	566.5
594	S294	619.5	411.5
595	S293	598.5	566.5
596	S292	577.5	411.5
597	S291	556.5	566.5

Pad #	Pad name	X	Y
598	S290	535.5	411.5
599	S289	514.5	566.5
600	S288	493.5	411.5
601	S287	472.5	566.5
602	S286	451.5	411.5
603	S285	430.5	566.5
604	S284	409.5	411.5
605	S283	388.5	566.5
606	S282	367.5	411.5
607	S281	346.5	566.5
608	S280	325.5	411.5
609	S279	304.5	566.5
610	S278	283.5	411.5
611	S277	262.5	566.5
612	S276	241.5	411.5
613	S275	220.5	566.5
614	S274	199.5	411.5
615	S273	178.5	566.5
616	S272	157.5	411.5
617	S271	136.5	566.5
618	S270	115.5	411.5
619	S269	94.5	566.5
620	S268	73.5	411.5
621	S267	52.5	566.5
622	S266	31.5	411.5
623	S265	10.5	566.5
624	S264	-10.5	411.5
625	S263	-31.5	566.5
626	S262	-52.5	411.5
627	S261	-73.5	566.5
628	S260	-94.5	411.5
629	S259	-115.5	566.5
630	S258	-136.5	411.5
631	S257	-157.5	566.5
632	S256	-178.5	411.5
633	S255	-199.5	566.5
634	S254	-220.5	411.5
635	S253	-241.5	566.5
636	S252	-262.5	411.5
637	S251	-283.5	566.5
638	S250	-304.5	411.5
639	S249	-325.5	566.5
640	S248	-346.5	411.5
641	S247	-367.5	566.5
642	S246	-388.5	411.5
643	S245	-409.5	566.5
644	S244	-430.5	411.5
645	S243	-451.5	566.5
646	S242	-472.5	411.5
647	S241	-493.5	566.5
648	S240	-514.5	411.5
649	S239	-535.5	566.5
650	S238	-556.5	411.5
651	S237	-577.5	566.5
652	S236	-598.5	411.5
653	S235	-619.5	566.5
654	S234	-640.5	411.5
655	S233	-661.5	566.5
656	S232	-682.5	411.5
657	S231	-703.5	566.5
658	S230	-724.5	411.5
659	S229	-745.5	566.5
660	S228	-766.5	411.5
661	S227	-787.5	566.5
662	S226	-808.5	411.5
663	S225	-829.5	566.5
664	S224	-850.5	411.5
665	S223	-871.5	566.5
666	S222	-892.5	411.5
667	S221	-913.5	566.5
668	S220	-934.5	411.5
669	S219	-955.5	566.5
670	S218	-976.5	411.5
671	S217	-997.5	566.5
672	S216	-1018.5	411.5
673	S215	-1039.5	566.5
674	S214	-1060.5	411.5
675	S213	-1081.5	566.5
676	S212	-1102.5	411.5
677	S211	-1123.5	566.5
678	S210	-1144.5	411.5
679	S209	-1165.5	566.5
680	S208	-1186.5	411.5
681	S207	-1207.5	566.5
682	S206	-1228.5	411.5
683	S205	-1249.5	566.5
684	S204	-1270.5	411.5

Pad #	Pad name	X	Y
685	S203	-1291.5	566.5
686	S202	-1312.5	411.5
687	S201	-1333.5	566.5
688	S200	-1354.5	411.5
689	S199	-1375.5	566.5
690	S198	-1396.5	411.5
691	S197	-1417.5	566.5
692	S196	-1438.5	411.5
693	S195	-1459.5	566.5
694	S194	-1480.5	411.5
695	S193	-1501.5	566.5
696	S192	-1522.5	411.5
697	S191	-1543.5	566.5
698	S190	-1564.5	411.5
699	S189	-1585.5	566.5
700	S188	-1606.5	411.5
701	S187	-1627.5	566.5
702	S186	-1648.5	411.5
703	S185	-1669.5	566.5
704	S184	-1690.5	411.5
705	S183	-1711.5	566.5
706	S182	-1732.5	411.5
707	S181	-1753.5	566.5
708	S180	-1774.5	411.5
709	S179	-1795.5	566.5
710	S178	-1816.5	411.5
711	S177	-1837.5	566.5
712	S176	-1858.5	411.5
713	S175	-1879.5	566.5
714	S174	-1900.5	411.5
715	S173	-1921.5	566.5
716	S172	-1942.5	411.5
717	S171	-1963.5	566.5
718	S170	-1984.5	411.5
719	S169	-2005.5	566.5
720	S168	-2026.5	411.5
721	S167	-2047.5	566.5
722	S166	-2068.5	411.5
723	S165	-2089.5	566.5
724	S164	-2110.5	411.5
725	S163	-2131.5	566.5
726	S162	-2152.5	411.5
727	S161	-2173.5	566.5
728	S160	-2194.5	411.5
729	S159	-2215.5	566.5
730	S158	-2236.5	411.5
731	S157	-2257.5	566.5
732	S156	-2278.5	411.5
733	S155	-2299.5	566.5
734	S154	-2320.5	411.5
735	S153	-2341.5	566.5
736	S152	-2362.5	411.5
737	S151	-2383.5	566.5
738	S150	-2404.5	411.5
739	S149	-2425.5	566.5
740	S148	-2446.5	411.5
741	S147	-2467.5	566.5
742	S146	-2488.5	411.5
743	S145	-2509.5	566.5
744	S144	-2530.5	411.5
745	S143	-2551.5	566.5
746	S142	-2572.5	411.5
747	S141	-2593.5	566.5
748	S140	-2614.5	411.5
749	S139	-2635.5	566.5
750	S138	-2656.5	411.5
751	S137	-2677.5	566.5
752	S136	-2698.5	411.5
753	S135	-2719.5	566.5
754	S134	-2740.5	411.5
755	S133	-2761.5	566.5
756	S132	-2782.5	411.5
757	S131	-2803.5	566.5
758	S130	-2824.5	411.5
759	S129	-2845.5	566.5
760	S128	-2866.5	411.5
761	S127	-2887.5	566.5
762	S126	-2908.5	411.5
763	S125	-2929.5	566.5
764	S124	-2950.5	411.5
765	S123	-2971.5	566.5
766	S122	-2992.5	411.5
767	S121	-3013.5	566.5
768	S120	-3034.5	411.5
769	S119	-3055.5	566.5
770	S118	-3076.5	411.5
771	S117	-3097.5	566.5

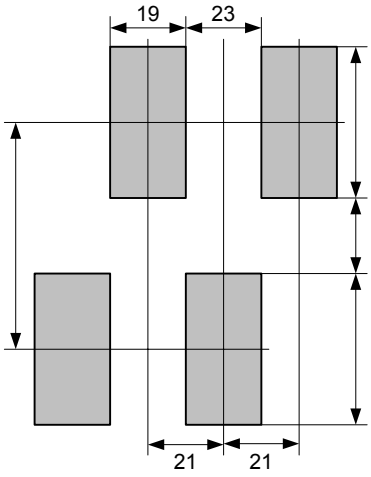
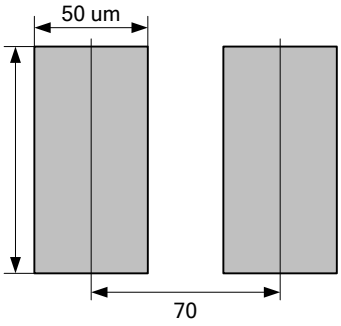
Pad #	Pad name	X	Y
772	S116	-3118.5	411.5
773	S115	-3139.5	566.5
774	S114	-3160.5	411.5
775	S113	-3181.5	566.5
776	S112	-3202.5	411.5
777	S111	-3223.5	566.5
778	S110	-3244.5	411.5
779	S109	-3265.5	566.5
780	S108	-3286.5	411.5
781	S107	-3307.5	566.5
782	S106	-3328.5	411.5
783	S105	-3349.5	566.5
784	S104	-3370.5	411.5
785	S103	-3391.5	566.5
786	S102	-3412.5	411.5
787	S101	-3433.5	566.5
788	S100	-3454.5	411.5
789	S99	-3475.5	566.5
790	S98	-3496.5	411.5
791	S97	-3517.5	566.5
792	S96	-3538.5	411.5
793	S95	-3559.5	566.5
794	S94	-3580.5	411.5
795	S93	-3601.5	566.5
796	S92	-3622.5	411.5
797	S91	-3643.5	566.5
798	S90	-3664.5	411.5
799	S89	-3685.5	566.5
800	S88	-3706.5	411.5
801	S87	-3727.5	566.5
802	S86	-3748.5	411.5
803	S85	-3769.5	566.5
804	S84	-3790.5	411.5
805	S83	-3811.5	566.5
806	S82	-3832.5	411.5
807	S81	-3853.5	566.5
808	S80	-3874.5	411.5
809	S79	-3895.5	566.5
810	S78	-3916.5	411.5
811	S77	-3937.5	566.5
812	S76	-3958.5	411.5
813	S75	-3979.5	566.5
814	S74	-4000.5	411.5
815	S73	-4021.5	566.5
816	S72	-4042.5	411.5
817	S71	-4063.5	566.5
818	S70	-4084.5	411.5
819	S69	-4105.5	566.5
820	S68	-4126.5	411.5
821	S67	-4147.5	566.5
822	S66	-4168.5	411.5
823	S65	-4189.5	566.5
824	S64	-4210.5	411.5
825	S63	-4231.5	566.5
826	S62	-4252.5	411.5
827	S61	-4273.5	566.5
828	S60	-4294.5	411.5
829	S59	-4315.5	566.5
830	S58	-4336.5	411.5
831	S57	-4357.5	566.5
832	S56	-4378.5	411.5
833	S55	-4399.5	566.5
834	S54	-4420.5	411.5
835	S53	-4441.5	566.5
836	S52	-4462.5	411.5
837	S51	-4483.5	566.5
838	S50	-4504.5	411.5
839	S49	-4525.5	566.5
840	S48	-4546.5	411.5
841	S47	-4567.5	566.5
842	S46	-4588.5	411.5
843	S45	-4609.5	566.5
844	S44	-4630.5	411.5
845	S43	-4651.5	566.5
846	S42	-4672.5	411.5
847	S41	-4693.5	566.5
848	S40	-4714.5	411.5
849	S39	-4735.5	566.5
850	S38	-4756.5	411.5
851	S37	-4777.5	566.5
852	S36	-4798.5	411.5
853	S35	-4819.5	566.5
854	S34	-4840.5	411.5
855	S33	-4861.5	566.5
856	S32	-4882.5	411.5
857	S31	-4903.5	566.5
858	S30	-4924.5	411.5

Pad #	Pad name	X	Y
859	S29	-4945.5	566.5
860	S28	-4966.5	411.5
861	S27	-4987.5	566.5
862	S26	-5008.5	411.5
863	S25	-5029.5	566.5
864	S24	-5050.5	411.5
865	S23	-5071.5	566.5
866	S22	-5092.5	411.5
867	S21	-5113.5	566.5
868	S20	-5134.5	411.5
869	S19	-5155.5	566.5
870	S18	-5176.5	411.5
871	S17	-5197.5	566.5
872	S16	-5218.5	411.5
873	S15	-5239.5	566.5
874	S14	-5260.5	411.5
875	S13	-5281.5	566.5
876	S12	-5302.5	411.5
877	S11	-5323.5	566.5
878	S10	-5344.5	411.5
879	S9	-5365.5	566.5
880	S8	-5386.5	411.5
881	S7	-5407.5	566.5
882	S6	-5428.5	411.5
883	S5	-5449.5	566.5
884	S4	-5470.5	411.5
885	S3	-5491.5	566.5
886	S2	-5512.5	411.5
887	S1	-5533.5	566.5
888	TESTO29	-5554.5	411.5
889	TESTO30	-5774.5	566.5
890	VGLDMY3	-5795.5	411.5
891	G219	-5816.5	566.5
892	G217	-5837.5	411.5
893	G215	-5858.5	566.5
894	G213	-5879.5	411.5
895	G211	-5900.5	566.5
896	G209	-5921.5	411.5
897	G207	-5942.5	566.5
898	G205	-5963.5	411.5
899	G203	-5984.5	566.5
900	G201	-6005.5	411.5
901	G199	-6026.5	566.5
902	G197	-6047.5	411.5
903	G195	-6068.5	566.5
904	G193	-6089.5	411.5
905	G191	-6110.5	566.5
906	G189	-6131.5	411.5
907	G187	-6152.5	566.5
908	G185	-6173.5	411.5
909	G183	-6194.5	566.5
910	G181	-6215.5	411.5
911	G179	-6236.5	566.5
912	G177	-6257.5	411.5
913	G175	-6278.5	566.5
914	G173	-6299.5	411.5
915	G171	-6320.5	566.5
916	G169	-6341.5	411.5
917	G167	-6362.5	566.5
918	G165	-6383.5	411.5
919	G163	-6404.5	566.5
920	G161	-6425.5	411.5
921	G159	-6446.5	566.5
922	G157	-6467.5	411.5
923	G155	-6488.5	566.5
924	G153	-6509.5	411.5
925	G151	-6530.5	566.5
926	G149	-6551.5	411.5
927	G147	-6572.5	566.5
928	G145	-6593.5	411.5
929	G143	-6614.5	566.5
930	G141	-6635.5	411.5
931	G139	-6656.5	566.5
932	G137	-6677.5	411.5
933	G135	-6698.5	566.5
934	G133	-6719.5	411.5
935	G131	-6740.5	566.5
936	G129	-6761.5	411.5
937	G127	-6782.5	566.5
938	G125	-6803.5	411.5
939	G123	-6824.5	566.5
940	G121	-6845.5	411.5
941	G119	-6866.5	566.5
942	G117	-6887.5	411.5
943	G115	-6908.5	566.5
944	G113	-6929.5	411.5
945	G111	-6950.5	566.5

Pad #	Pad name	X	Y
946	G109	-6971.5	411.5
947	G107	-6992.5	566.5
948	G105	-7013.5	411.5
949	G103	-7034.5	566.5
950	G101	-7055.5	411.5
951	G99	-7076.5	566.5
952	G97	-7097.5	411.5
953	G95	-7118.5	566.5
954	G93	-7139.5	411.5
955	G91	-7160.5	566.5
956	G89	-7181.5	411.5
957	G87	-7202.5	566.5
958	G85	-7223.5	411.5
959	G83	-7244.5	566.5
960	G81	-7265.5	411.5
961	G79	-7286.5	566.5
962	G77	-7307.5	411.5
963	G75	-7328.5	566.5
964	G73	-7349.5	411.5
965	G71	-7370.5	566.5
966	G69	-7391.5	411.5
967	G67	-7412.5	566.5
968	G65	-7433.5	411.5
969	G63	-7454.5	566.5
970	G61	-7475.5	411.5
971	G59	-7496.5	566.5
972	G57	-7517.5	411.5
973	G55	-7538.5	566.5
974	G53	-7559.5	411.5
975	G51	-7580.5	566.5
976	G49	-7601.5	411.5
977	G47	-7622.5	566.5
978	G45	-7643.5	411.5
979	G43	-7664.5	566.5
980	G41	-7685.5	411.5
981	G39	-7706.5	566.5
982	G37	-7727.5	411.5
983	G35	-7748.5	566.5
984	G33	-7769.5	411.5
985	G31	-7790.5	566.5
986	G29	-7811.5	411.5
987	G27	-7832.5	566.5
988	G25	-7853.5	411.5
989	G23	-7874.5	566.5
990	G21	-7895.5	411.5
991	G19	-7916.5	566.5
992	G17	-7937.5	411.5
993	G15	-7958.5	566.5
994	G13	-7979.5	411.5
995	G11	-8000.5	566.5
996	G9	-8021.5	411.5
997	G7	-8042.5	566.5
998	G5	-8063.5	411.5
999	G3	-8084.5	566.5
1000	G1	-8105.5	411.5
1001	VGLDMY4	-8126.5	566.5
1002	DUMMYR9	-8147.5	411.5
1003	DUMMYR10	-8168.5	566.5
1004	TESTO31	-8189.5	411.5
1005	TESTO32	-8210.5	566.5
1006	VPP1	-8466.5	-130.7
1007	VPP1	-8466.5	-200.7
1008	VPP1	-8466.5	-270.7
1009	VPP1	-8466.5	-340.7
1010	VPP1	-8466.5	-410.7

Alignment mark	X	Y
✚ (1-a)	-8422.0	536.9
✚ (1-b)	8422.0	536.9
● (2-a)	-8421.5	-581.5
○ (2-b)	8421.5	-581.5
▌ (3-a)	-8421.5	-505.0
▌ (3-b)	8421.5	-505.0

Bump Arrangement

S1 – S528 G1 – G220	 Size = 2280 um^2
I/O pins	 Size = 4000 um^2

155 um

80 um

Figure 2

Block Function

System Interface

The LGDP4522 supports 2-system high-speed interfaces: 80-system high-speed interfaces to 8-, 9-, 16-, 18-bit parallel ports and a Serial Peripheral Interface (SPI). The interface mode is selected by setting the IM[3:0] pins.

The LGDP4522 has a 16-bit index register (IR); an 18-bit write-data register (WDR); and an 18-bit read-data register (RDR). The IR is the register to store index information from control registers and the internal GRAM. The WDR is the register to temporarily store data to be written to control registers and the internal GRAM. The RDR is the register to temporarily store data read from the GRAM. Data from the MPU to be written to the internal GRAM are first written to the WDR and then automatically written to the internal GRAM in internal operation. Data are read via the RDR from the internal GRAM. Therefore, invalid data are read out to the data bus when the LGDP4522 read the first data from the internal GRAM. Valid data are read out after the LGDP4522 performs the second read operation.

Instructions are written consecutively as the instruction execution time except starting oscillator takes 0 clock cycle.

Table 3: Register Selection (80-system 8-/9-/16-/18-bit Parallel Interface)

80-system I/F			Function
WR*	RD*	RS	
0	1	0	Write an index to IR
1	0	0	Read an internal status
0	1	1	Write to control registers or the internal GRAM via WDR
1	0	1	Read from the internal GRAM via RDR

Table 4: Register Selection (Serial Peripheral Interface)

Start Byte (SPI)		Function
R/W	RS	
0	0	Write an index to IR
1	0	Read an internal status
0	1	Write into control registers and the internal GRAM via WDR
1	1	Read from the internal GRAM via RDR

External Display Interface

The LGDP4522 supports the RGB interface and the VSYNC interface as the external interface for displaying a moving picture. When the RGB interface is selected, display operations are synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. In RGB interface mode, data (DB[17:0]) are written in synchronization with these signals according to the polarity of enable signal (ENABLE) to prevent flicker on display while updating display data.

In VSYNC interface mode, the display operation is synchronized with the internal clock except frame synchronization, where the operation is synchronized with the VSYNC signal. Display data are written to the internal GRAM via the system interface. In this case, there are constraints in speed and method in writing data to the internal RAM. For details, see the “External Display Interface” section.

The LGDP4522 allows for switching between the external display interface and the system interface by instruction so that the optimum interface is selected for the kind of picture to be displayed on the screen (still and/or moving picture(s)). The RGB interface, by writing all display data to the internal RAM, allows for transferring data only when updating the frames of a moving picture, contributing to low power requirement for moving picture display.

Bit Operations

The LGDP4522 supports a write data mask function for selectively writing data to the internal RAM in units of bits and a logical/compare operation to write data to the GRAM only when a condition is met as a result of comparing the data and the compare register bits. For details, see "**오류! 참조 원본을 찾을 수 없습니다.**" section.

Address Counter (AC)

The address counter (AC) gives an address to the internal GRAM. When the index of the register for setting a RAM address in the AC is written to the IR, the address information is sent from the IR to the AC. As writing data to the internal GRAM, the address in the AC is automatically updated plus or minus 1. The window address function enables writing data only in the rectangular area arbitrarily set by users on the GRAM.

Graphics RAM (GRAM)

GRAM is graphics RAM storing bit-pattern data of 95,040 (176 x 220 x 18/8) bytes, using 18 bits per pixel.

Grayscale Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to grayscale data set in the γ-correction register to display in 262,144 colors. For details, see the "γ-Correction Function" section.

Timing Generator

The timing generator generates a timing signal for operation of internal circuits such as the internal GRAM. The timing for the display operation such as RAM read operation and the timing for the internal operation such as access from the MPU are generated in the way not to interfere each other.

Oscillator (OSC)

The LGDP4522 generates RC oscillation with an external oscillation resistor placed between the OSC1 and OSC2 pins. The oscillation frequency is changed according to the value of an external resistor. Adjust the oscillation frequency in accordance to the operating voltage or the frame frequency. An operating clock can be input externally. During standby mode, RC oscillation is halted to reduce power consumption. For details, see "Oscillator" section.

LCD Driver Circuit

The LCD driver circuit of the LGDP4522 consists of a 528-output source driver (S1 to S528) and a 220-output gate driver (G1 to G220). Display pattern data are latched when the 528th bit data are input. The latched data control the source driver and generate a drive waveform. The gate driver for scanning gate lines outputs either VGH or VGL level. The shift direction of 528-bit source outputs from the source driver is set with the SS bit and the shift direction of gate outputs from the gate driver is set with the GS bit. The scan mode by the gate driver is set with the SM bit. These bits allow setting an appropriate scan method for an LCD module.

LCD Drive Power Supply Circuit

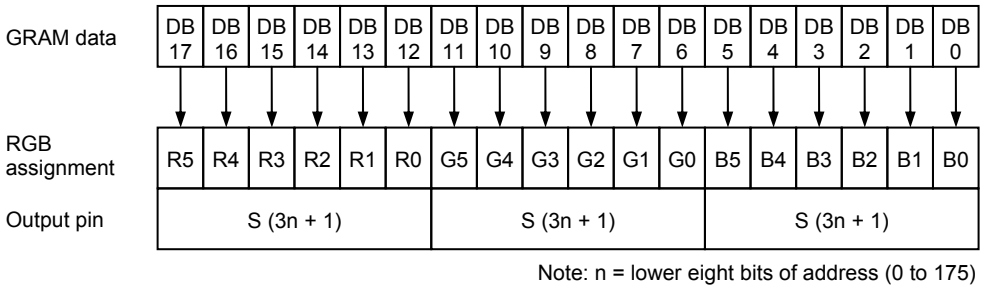
The LCD drive power supply circuit generates the voltage levels VREG1OUT, VGH, VGL and Vcom for driving an LCD.

GRAM Address MAP

Table 5: GRAM address and display panel position (SS = "0", BGR = "0")

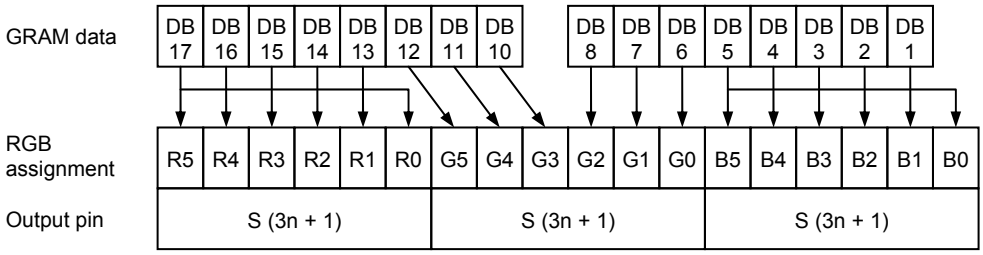
S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G240	0000			0001			0002			0003			…	00AC			00AD			00AE			00AF		
G2	G239	0100			0101			0102			0103			…	01AC			01AD			01AE			01AF		
G3	G238	0200			0201			0202			0203			…	02AC			02AD			02AE			02AF		
G4	G237	0300			0301			0302			0303			…	03AC			03AD			03AE			03AF		
G5	G236	0400			0401			0402			0403			…	04AC			04AD			04AE			04AF		
G6	G235	0500			0501			0502			0503			…	05AC			05AD			05AE			05AF		
G7	G234	0600			0601			0602			0603			…	06AC			06AD			06AE			06AF		
G8	G233	0700			0701			0702			0703			…	07AC			07AD			07AE			07AF		
G9	G232	0800			0801			0802			0803			…	08AC			08AD			08AE			08AF		
G10	G231	0900			0901			0902			0903			…	09AC			09AD			09AE			09AF		
G11	G230	0A00			0A01			0A02			0A03			…	0AAC			0AAD			0AAE			0AAF		
G12	G229	0B00			0B01			0B02			0B03			…	0BAC			0BAD			0BAE			0BAF		
G13	G228	0C00			0C01			0C02			0C03			…	0CAC			0CAD			0CAE			0CAF		
G14	G227	0D00			0D01			0D02			0D03			…	0DAC			0DAD			0DAE			0DAF		
G15	G226	0E00			0E01			0E02			0E03			…	0EAC			0EAD			0EAE			0EAF		
G16	G225	0F00			0F01			0F02			0F03			…	0FAC			0FAD			0FAE			0FAF		
G17	G224	1000			1001			1002			1003			…	10AC			10AD			10AE			10AF		
G18	G223	1100			1101			1102			1103			…	11AC			11AD			11AE			11AF		
G19	G222	1200			1201			1202			1203			…	12AC			12AD			12AE			12AF		
G20	G221	1300			1301			1302			1303			…	13AC			13AD			13AE			13AF		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G233	G8	E800			E801			E802			E803			…	E8AC			E8AD			E8AE			E8AF		
G234	G7	E900			E901			E902			E903			…	E9AC			E9AD			E9AE			E9AF		
G235	G6	EA00			EA01			EA02			EA03			…	EAAC			EAAD			EAAE			EAAF		
G237	G5	EB00			EB01			EB02			EB03			…	EBAC			EBAD			EBAE			EBAF		
G237	G4	EC00			EC01			EC02			EC03			…	ECAC			ECAD			ECAE			ECAF		
G238	G3	ED00			ED01			ED02			ED03			…	EDAC			EDAD			EDAE			EDAF		
G239	G2	EE00			EE01			EE02			EE03			…	EEAC			EEAD			EEAE			EEAF		
G240	G1	EF00			EF01			EF02			EF03			…	EFAC			EFAD			EFAE			EFAF		

18-bit interface (262k colors)



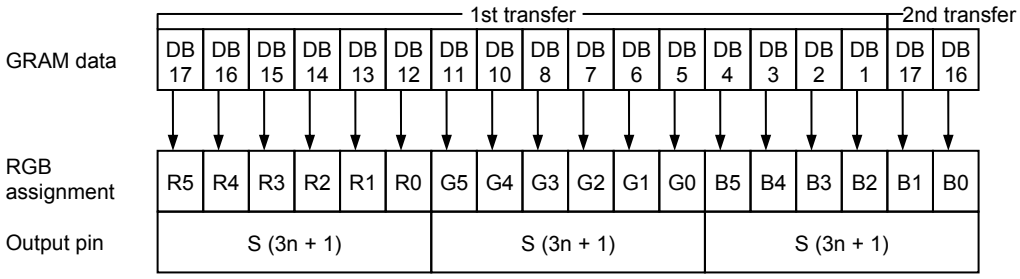
Note: n = lower eight bits of address (0 to 175)

16-bit interface (65k colors) – TRI = "0"



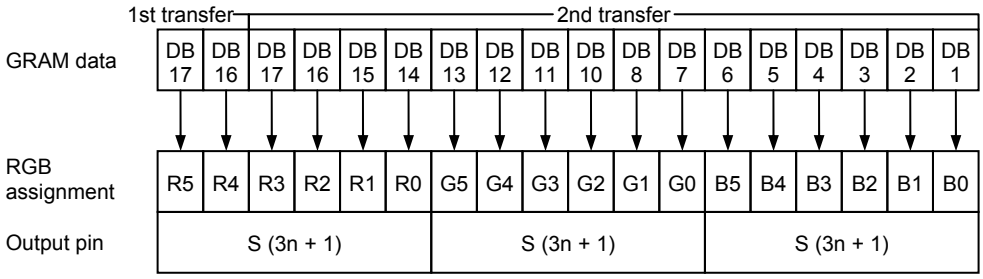
Note: n = lower eight bits of address (0 to 175)

16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

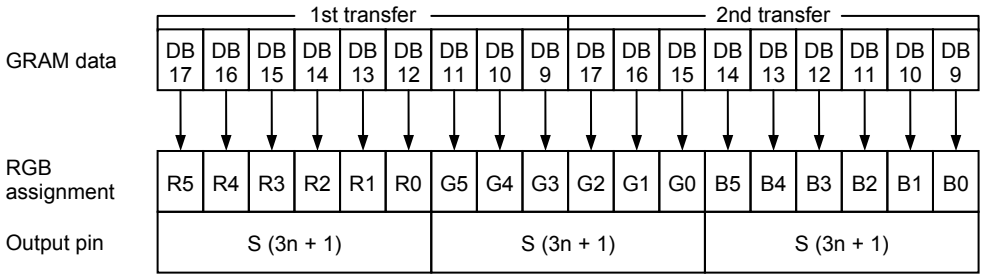
16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

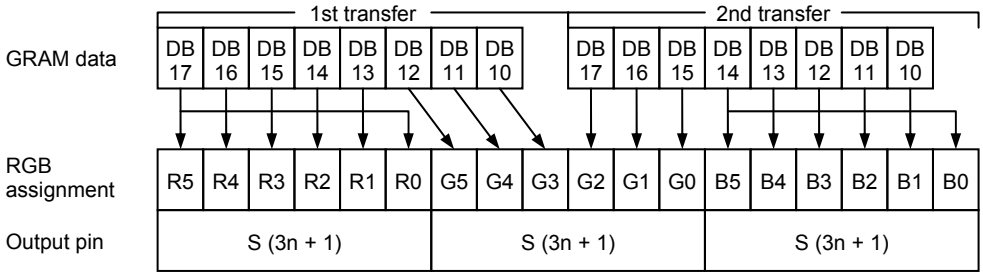
Figure 3: GRAM data and display data: system interface (SS = "0", BGR = "0")

9-bit interface (262k colors)



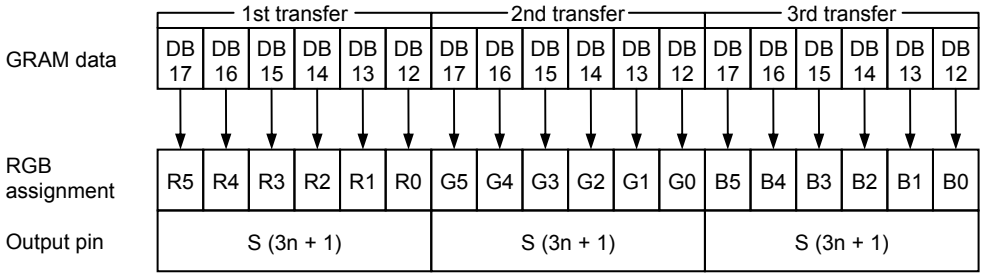
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (2 transfers/pixel, 65k colors) – TRI = "0"



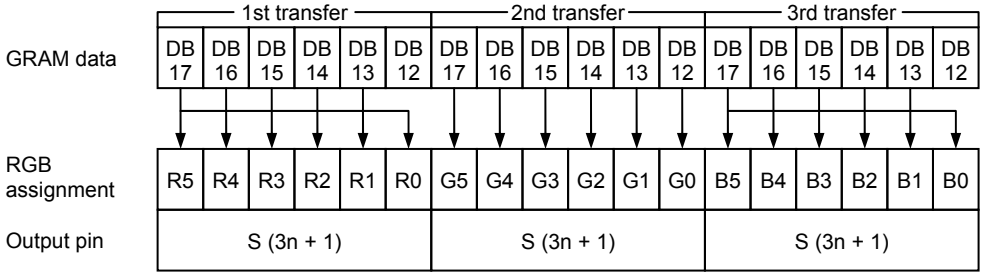
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

8-bit interface (3 transfers/pixel, 65k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

Figure 4: GRAM data and display data: system interface (SS = "0", BGR = "0")

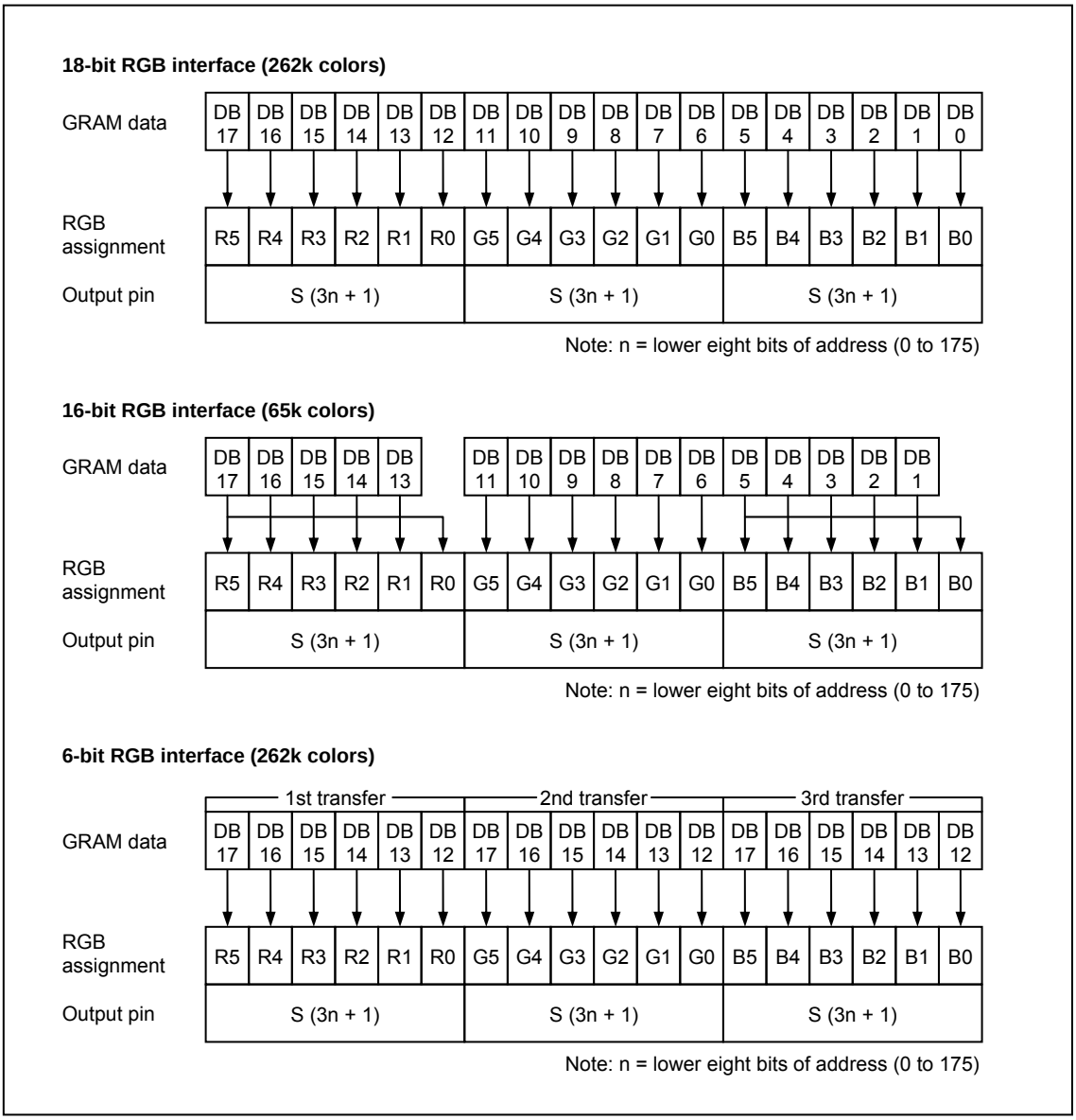
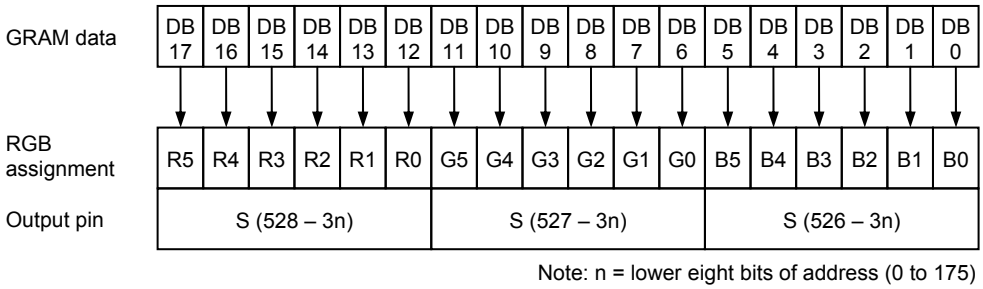


Figure 5: GRAM data and display data: system interface (SS = "0", BGR = "0")

Table 6: GRAM address and display panel position (SS = “1”, BGR = “1”)

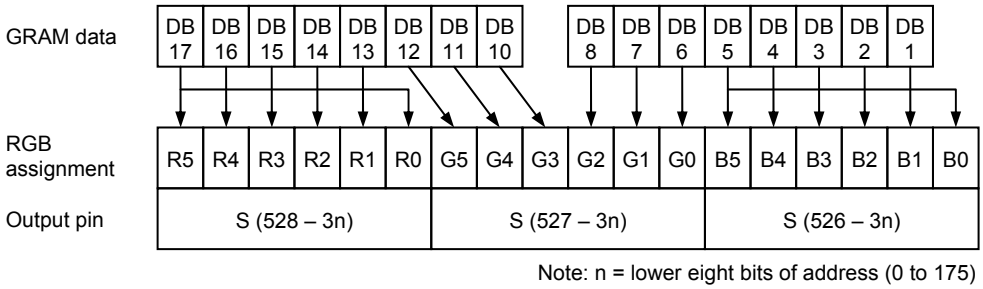
S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	…	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]			…	DB[17:0]			DB[17:0]			DB[17:0]			DB[17:0]		
G1	G240	00AF			00AE			00AD			00AC			…	0003			0002			0001			0000		
G2	G239	01AF			01AE			01AD			01AC			…	0103			0102			0101			0100		
G3	G238	02AF			02AE			02AD			02AC			…	0203			0202			0201			0200		
G4	G237	03AF			03AE			03AD			03AC			…	0303			0302			0301			0300		
G5	G236	04AF			04AE			04AD			04AC			…	0403			0402			0401			0400		
G6	G235	05AF			05AE			05AD			05AC			…	0503			0502			0501			0500		
G7	G234	06AF			06AE			06AD			06AC			…	0603			0602			0601			0600		
G8	G233	07AF			07AE			07AD			07AC			…	0703			0702			0701			0700		
G9	G232	08AF			08AE			08AD			08AC			…	0803			0802			0801			0800		
G10	G231	09AF			09AE			09AD			09AC			…	0903			0902			0901			0900		
G11	G230	0AAF			0AAE			0AAD			0AAC			…	0A03			0A02			0A01			0A00		
G12	G229	0BAF			0BAE			0BAD			0BAC			…	0B03			0B02			0B01			0B00		
G13	G228	0CAF			0CAE			0CAD			0CAC			…	0C03			0C02			0C01			0C00		
G14	G227	0DAF			0DAE			0DAD			0DAC			…	0D03			0D02			0D01			0D00		
G15	G226	0EAF			0EAE			0EAD			0EAC			…	0E03			0E02			0E01			0E00		
G16	G225	0FAF			0FAE			0FAD			0FAC			…	0F03			0F02			0F01			0F00		
G17	G224	10AF			10AE			10AD			10AC			…	1003			1002			1001			1000		
G18	G223	11AF			11AE			11AD			11AC			…	1103			1102			1101			1100		
G19	G222	12AF			12AE			12AD			12AC			…	1203			1202			1201			1200		
G20	G221	13AF			13AE			13AD			13AC			…	1303			1302			1301			1300		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G233	G8	E8AF			E8AE			E8AD			E8AC			…	E803			E802			E801			E800		
G234	G7	E9AF			E9AE			E9AD			E9AC			…	E903			E902			E901			E900		
G235	G6	EAAF			EAAE			EAAD			EAAC			…	EA03			EA02			EA01			EA00		
G237	G5	EBAF			EBAE			EBAD			EBAC			…	EB03			EB02			EB01			EB00		
G237	G4	ECAF			ECAE			ECAD			ECAC			…	EC03			EC02			EC01			EC00		
G238	G3	EDAF			EDAE			EDAD			EDAC			…	ED03			ED02			ED01			ED00		
G239	G2	EEAF			EEAE			EEAD			EEAC			…	EE03			EE02			EE01			EE00		
G240	G1	EFAF			EFAE			EFAD			EFAC			…	EF03			EF02			EF01			EF00		

18-bit interface (262k colors)



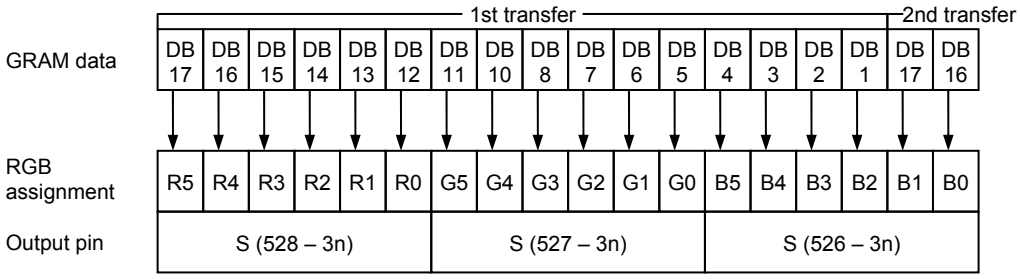
Note: n = lower eight bits of address (0 to 175)

16-bit interface (65k colors) – TRI = "0"



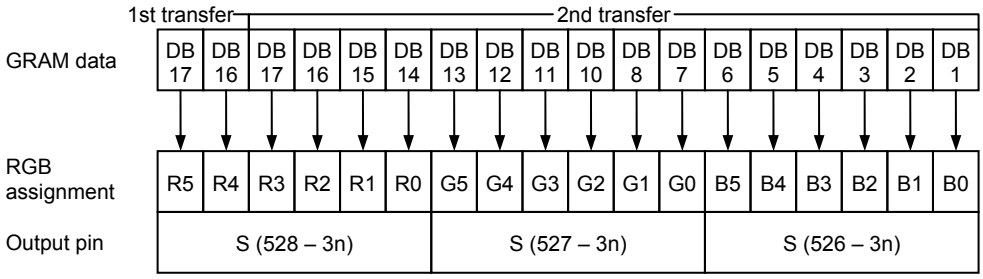
Note: n = lower eight bits of address (0 to 175)

16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

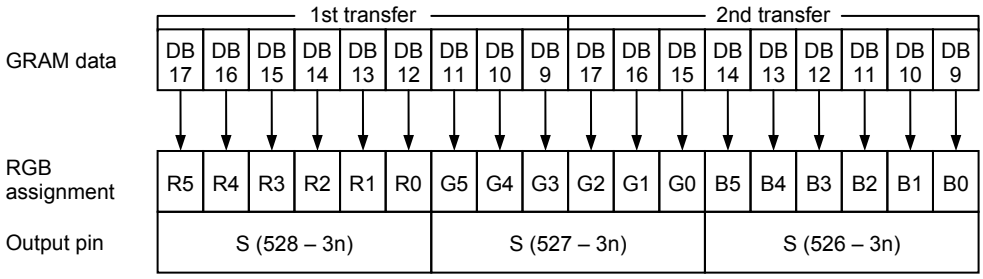
16-bit interface (2 transfers/pixel, 262k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

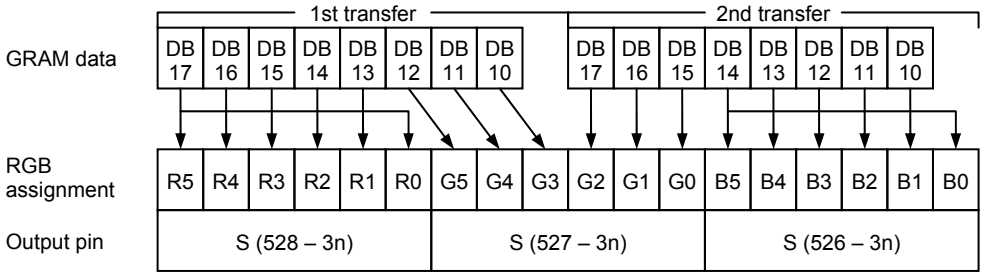
Figure 6: GRAM data and display data: system interface (SS = "1", BGR = "1")

9-bit interface (262k colors)



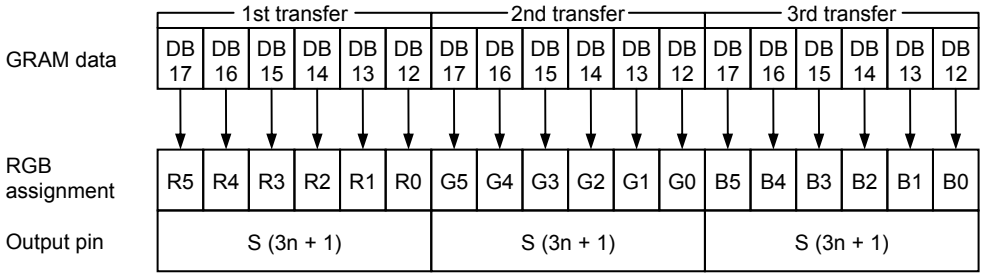
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (2 transfers/pixel, 65k colors) – TRI = "0"



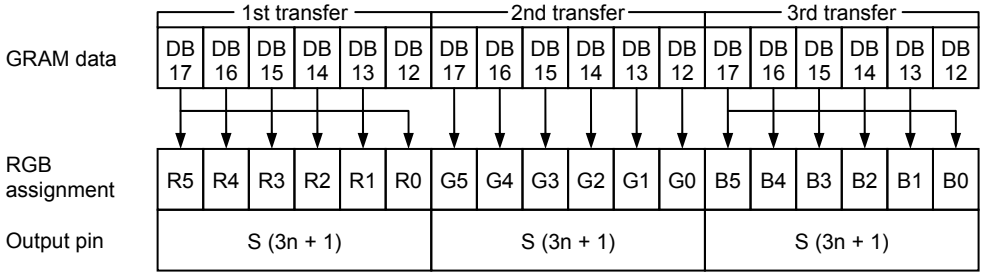
Note: n = lower eight bits of address (0 to 175)

8-bit interface or SPI (3 transfers/pixel, 262k colors) – TRI = "1", DFM = "0"



Note: n = lower eight bits of address (0 to 175)

80-system 8-bit interface (3 transfers/pixel, 65k colors) – TRI = "1", DFM = "1"



Note: n = lower eight bits of address (0 to 175)

Figure 7: GRAM data and display data: system interface (SS = "1", BGR = "1")

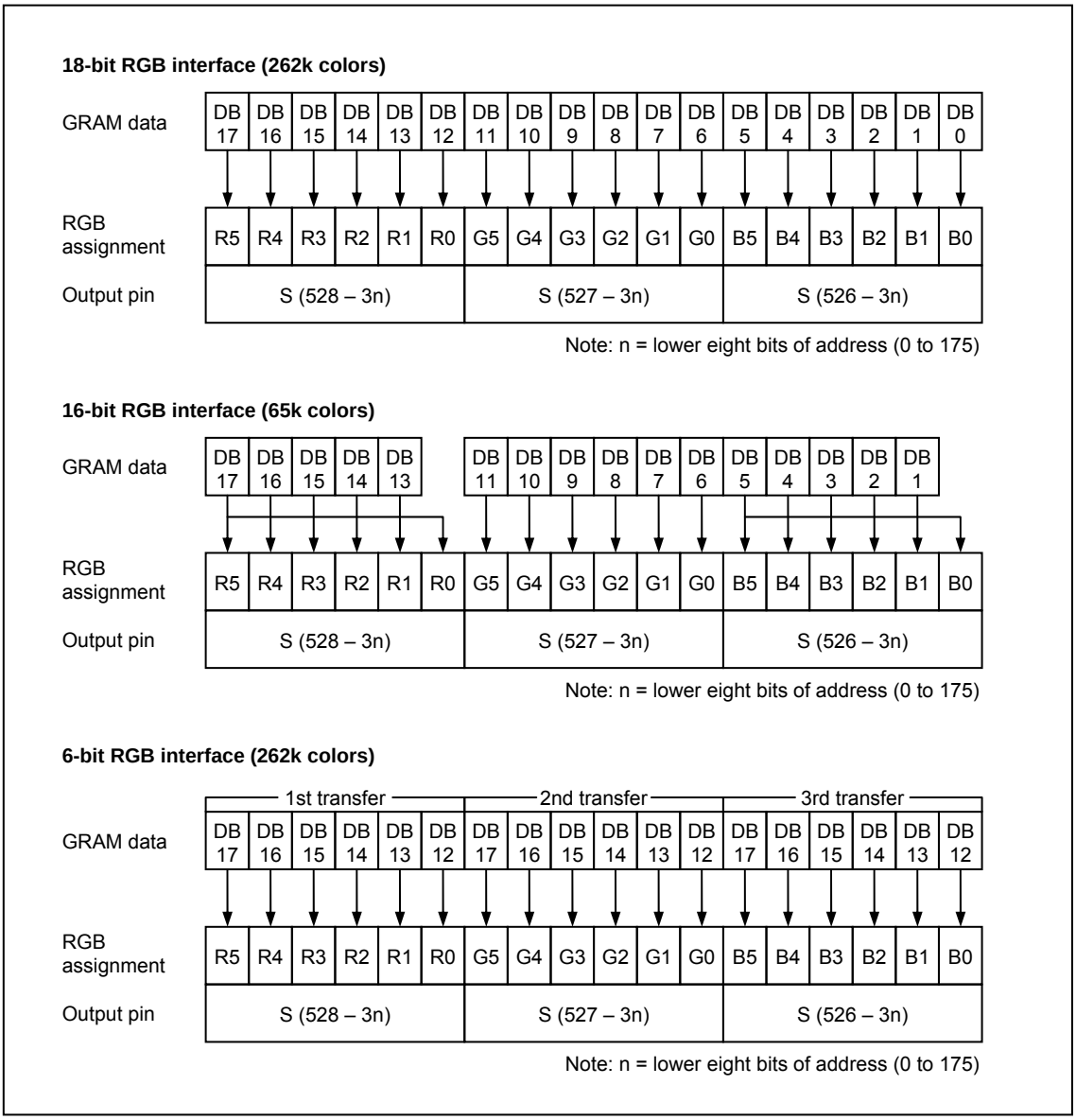


Figure 8: GRAM data and display data: system interface (SS = "1", BGR = "1")

Instructions

Outline

The LGDP4522 adopts 18-bit bus architecture to interface to a high-performance microcomputer. The LGDP4522 starts internal processing after storing control information of externally sent 18-, 16-, 9-, 8-bit data in the instruction register IR and the data register DR. Since internal operations of the LGDP4522 are controlled by the signals sent from the microcomputer, the register selection signal RS, the read/write signal R/W, and the internal 16-bit data bus signals IB[15:0] are called instructions. The LGDP4522 use the 18-bit format internally for operations involving internal GRAM access. The instructions of the LGDP4522 are categorized into the following groups.

1. Specify the index of register
2. Read a status
3. Display control
4. Power management Control
5. Graphics data processing
6. Set internal GRAM address
7. Transfer data to and from the internal GRAM
8. γ-correction

Normally, the instruction for writing data to the internal GRAM is used the most often. Since the LGDP4522 can update internal GRAM address automatically as it writes data to the internal GRAM and minimize data transfer by using the window address function, there is less load on the program in the microcomputer. Since instructions are executed in 0 cycles, it is possible to write instructions consecutively.

As the following figure shows, the way of assigning data to the 16 instruction bits IB[15:0] varies for each interface. Send instructions in accordance with the following data transfer format.

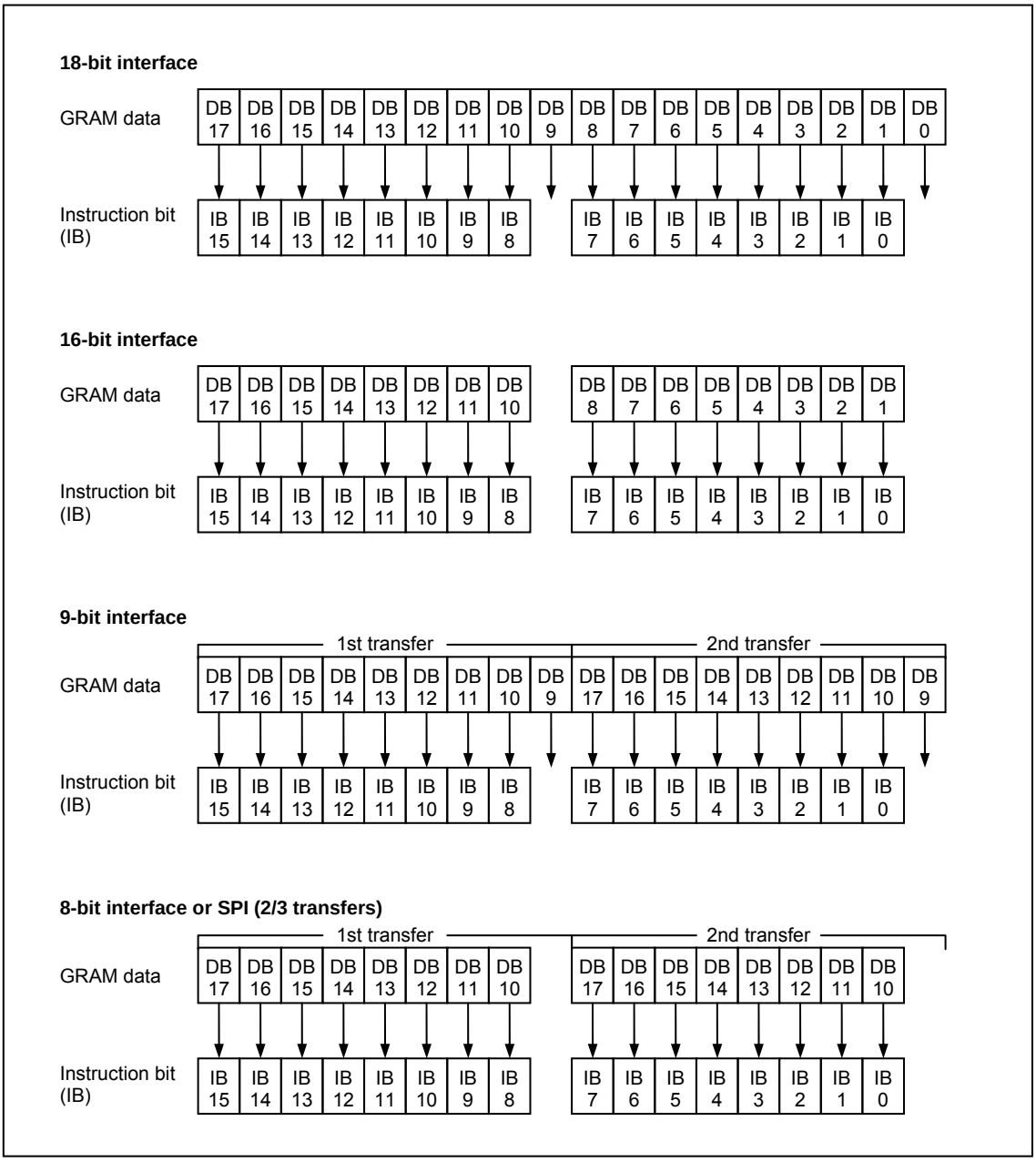


Figure 9: Instruction bits

Explanation of each instruction

The following are detailed explanations of instructions with illustrations of instruction bits IB[15:0] assigned to each interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h to RFFh) of a control register or RAM control to be accessed using binary numbers “000_0000” to “111_1111”. An access to the register as well as instruction bits contained in it is prohibited unless its index is represented in this register.

Status Read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L[7:0]								0	0	0	0	0	0	0	0

The SR bits represent an internal status of the LGDP4522.

L[7:0] – Indicates the position of the line that is currently driving liquid crystal.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	1	0	0	0	1	0	1	0	0	1	0	0	0	1	0

The start oscillation instruction restarts an oscillator in halt state in standby mode. After executing this instruction, wait at least 10 ms for stabilizing oscillator before issuing a next instruction.

The device code 4522h is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL[4:0]				

SS – Selects the shift direction of outputs from the source pins.

If SS = “0”, the source pins output from S1 to S528.
If SS = “1”, the source pins output from S528 to S1.

The combination of SS and BGR bits controls the order of assigning RGB dots to the source driver pins S1 to S528.

If SS = “0” and BGR = “0”, RGB dots are assigned interchangeably from S1 to S528.
If SS = “1” and BGR = “1”, RGB dots are assigned interchangeably from S528 to S1.

When changing SS or BGR bits, RAM data must be rewritten.

GS – Sets the shift direction of outputs from the gate driver. GS enables setting the scan order in accordance to the scan mode adopted in the module.

SM – Sets the scan order by the gate driver. SM enables setting the scan order in accordance to the scan mode adopted in the module. See “Scan Mode Setting” section for details.

EPL – Sets the polarity of the signal from the ENABLE pin in RGB interface mode.

If EPL = “0”, ENABLE is low active.
If EPL = “1”, ENABLE is high active.

The following table shows the relationship between the EPL, ENABLE bits, and RAM access.

Table 7

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Inhibited	Retained
1	0	Inhibited	Retained
1	1	Enabled	Updated

VSPL – Inverts the polarity of signals from the VSYNC pin.

If VSPL = “0”, VSYNC is low active.
If VSPL = “1”, VSYNC is high active.

HSPL – Inverts the polarity of signals from the HSYNC pin.

If HSPL = “0”, HSYNC is low active.
If HSPL = “1”, HSYNC is high active.

DPL – Inverts the polarity of signals from the DOTCLK pin.

If DPL = “0”, data are read on the rising edge of the DOTCLK.
If DPL = “1”, data are read on the falling edge of the DOTCLK.

NL[4:0] – Sets the number of gate lines for driving a liquid crystal display panel at an interval of 8 lines as the following table. The GRAM address mapping is independent from the number of gate lines set with the NL bits. Select the number of gate lines that is equal to or more than that of the panel in use.

Table 8

NL[4:0]	Display size	Lines	Driven gate lines
00h	Setting disabled		
01h	528 x 16 dots	16	G1 to G16
02h	528 x 24 dots	24	G1 to G24
03h	528 x 32 dots	32	G1 to G32
04h	528 x 40 dots	40	G1 to G40
05h	528 x 48 dots	48	G1 to G48
06h	528 x 56 dots	56	G1 to G56
07h	528 x 64 dots	64	G1 to G64
08h	528 x 72 dots	72	G1 to G72
09h	528 x 80 dots	80	G1 to G80
0Ah	528 x 88 dots	88	G1 to G88
0Bh	528 x 96 dots	96	G1 to G96
0Ch	528 x 104 dots	104	G1 to G104
0Dh	528 x 112 dots	112	G1 to G112
0Eh	528 x 120 dots	120	G1 to G120
0Fh	528 x 128 dots	128	G1 to G128
10h	528 x 136 dots	136	G1 to G136
11h	528 x 144 dots	144	G1 to G144
12h	528 x 152 dots	152	G1 to G152
13h	528 x 160 dots	160	G1 to G160
14h	528 x 168 dots	168	G1 to G168
15h	528 x 176 dots	176	G1 to G176
16h	528 x 184 dots	184	G1 to G184
17h	528 x 192 dots	192	G1 to G192
18h	528 x 200 dots	200	G1 to G200
19h	528 x 208 dots	208	G1 to G208
1Ah	528 x 216 dots	216	G1 to G216
1Bh	528 x 220 dots	220	G1 to G220

LCD Driving Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD[1:0]		B/C	EOR	0	0	NW[5:0]					

NW[5:0] – Specifies “n”, the number of gate lines from 1 to 64, to set the interval of inverting polarity when the R61500 is set to generate a C-pattern waveform (B/C = “1”). The polarity is inverted at an interval of n+1 gate lines.

EOR – When EOR = “1”, the polarity is inverted according to the result of EOR (exclusive OR) operation, which is performed on a signal for selecting either odd or even frames and a signal for inverting polarity in units of n lines when the LGDP4522 is set to generate a C-pattern waveform (B/C = “1”). This instruction is used when the number of gate lines for driving an LCD panel is at odds with the interval of n lines set for inverting polarity. For details, see “n-Line Inversion AC Drive” section.

B/C – When the LGDP4522 is set to generate a field-inversion waveform (B/C = “0”), polarity is inverted at an interval of fields. The LGDP4522 inverts polarity at an interval of n lines, when a C-pattern waveform is generated (B/C = “1”) according to NW and EOR bits. For details, see “n-Line Inversion AC Drive”.

FLD[1:0] – Sets the number of fields for n-field interlaced scan. See “Interlaced Scan” for details. The FLD bits are disabled in external display interface mode. When using the external display interface, set FLD[1:0] = “01”.

Table 9

FLD	Number of fields
00	Setting disabled
01	1 field (= 1 frame)
10	Setting disabled
11	3 fields

Entry Mode (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM	0	BGR	0	0	0	0	0	0	I/D[1:0]		AM	0	0	0

The LGDP4522 modifies data sent from a microcomputer before writing them to the internal GRAM in order to write the GRAM data in high speed and reduce software processing load on the microcomputer. See “**오류! 참조 원본을 찾을 수 없습니다.**” section for details.

TRI – When TRI = “1”, data are transferred to the internal RAM in 8-bit x 3 transfers mode via the 8-bit interface. It is also possible to send data via the 16-bit interface or SPI in the transfer mode that realizes display in 262k colors in combination with DFM bits. When not using these interface modes, be sure to set TRI to “0”.

DFM – Sets the mode of transferring data to the internal RAM when TRI = “1”. See the following figures for details.

Table 10

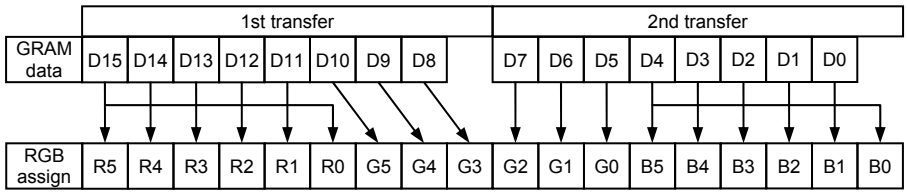
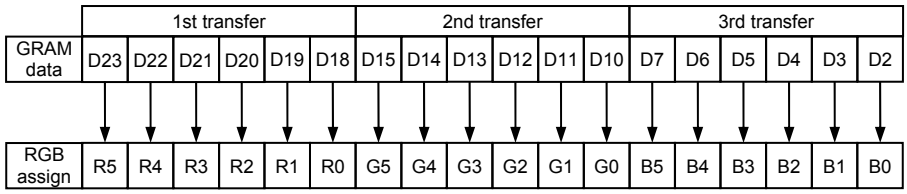
TRI	DFM	RAM write data transfer via serial peripheral interface (SPI)
0	*	SPI (2 transfers/pixel) – 65k colors available 
1	0	SPI (3 transfers/pixel) – 262k colors available 
1	1	Setting disabled

Table 11

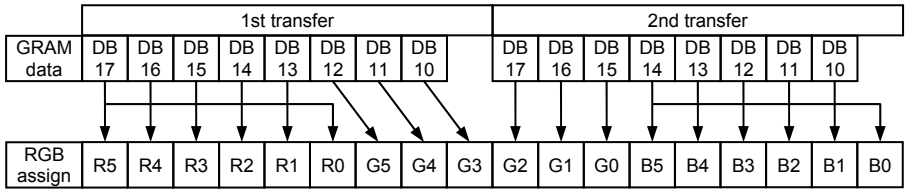
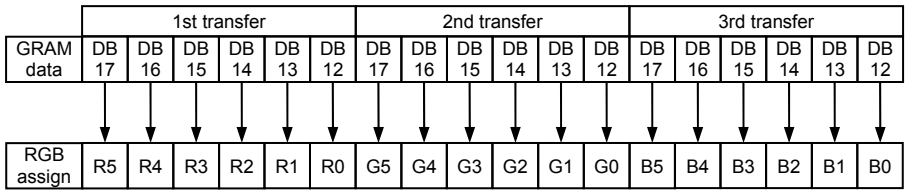
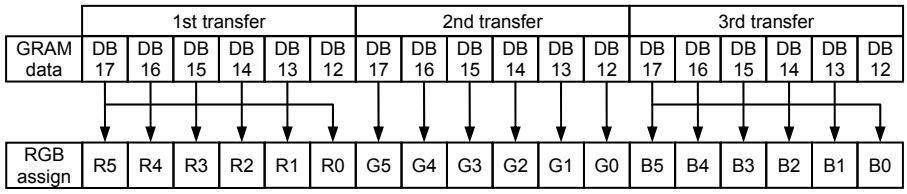
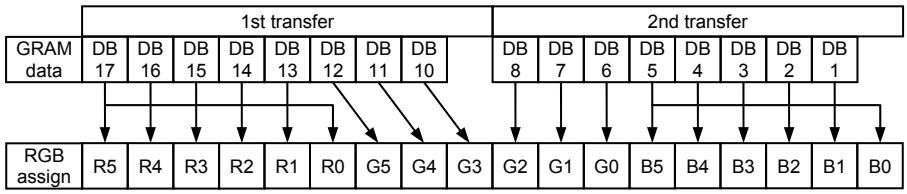
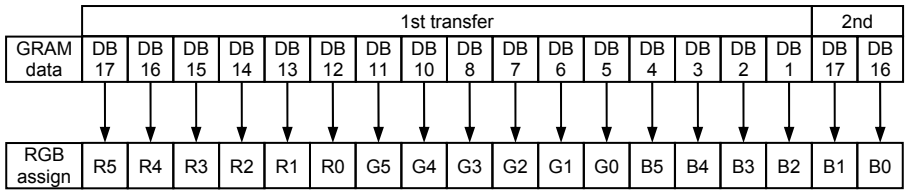
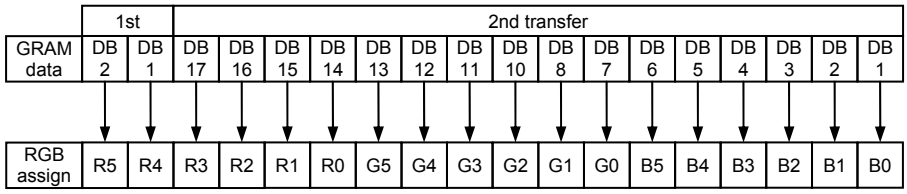
TRI	DFM	RAM write data transfer via 8-bit interface
0	*	8-bit interface (2 transfers/pixel) – 65k colors available 
1	0	8-bit interface (3 transfers/pixel) – 262k colors available 
1	1	8-bit interface (3 transfers/pixel) – 65k colors available 

Table 12

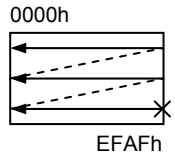
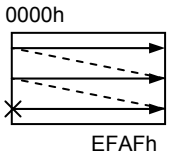
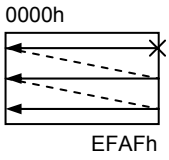
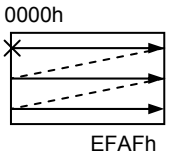
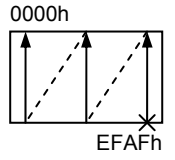
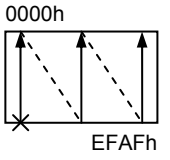
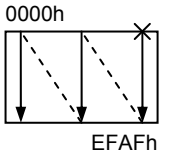
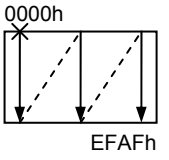
<table>
<tr><th>TRI</th><th>DFM</th><th>RAM write data transfer via 16-bit interface</th></tr>
<tr><td>0</td><td>*</td><td>16-bit interface (1 transfers/pixel) – 65k colors available
 
</td></tr>
<tr><td>1</td><td>0</td><td>16-bit interface MSB mode (2 transfers/pixel) – 262k colors available
 
</td></tr>
<tr><td>1</td><td>1</td><td>16-bit interface LSB mode (2 transfers/pixel) – 262k colors available
 
</td></tr>
</table>

BGR – Reverses the order of RGB dots to BGR when writing 18-bit pixel data to the internal GRAM. Note that the orders of RGB dots in both WM[17:0] and CP[17:0] bits are automatically changed upon setting BGR to “1”.

I/D[1:0] – The address counter is automatically incremented by 1 as writing data to the internal GRAM when I/D = “1”. The address counter is automatically decremented by 1 as writing data to the internal GRAM when I/D = “0”. The increment/decrement can be set separately to each upper (AD[15:8]) / lower (AD[7:0]) byte of address. The transition direction of address (vertical/horizontal) when writing data to the internal GRAM is set with the AM bit.

AM – Sets the direction of automatically updating address for writing data to the internal RAM in the address counter (AC). When AM = “0”, the address is updated in horizontal writing direction. When AM = “1”, the address is updated in vertical writing direction. When a window address area is set, data are written only to the GRAM area specified with window address in the writing direction set with I/D[1:0] and AM bits.

Table 13: Address transition directions

	I/D[1:0] = "00" Horizontal decrement Vertical decrement	I/D[1:0] = "01" Horizontal increment Vertical decrement	I/D[1:0] = "10" Horizontal decrement Vertical increment	I/D[1:0] = "11" Horizontal increment Vertical increment
AM = "0" Horizontal				
AM = "1" Vertical				

Resize Control (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	RCV[1:0]		0	0	RCH[1:0]		0	0	RSZ[1:0]	

RSZ[1:0] – Sets the resizing factor. When the RSZ bits are set for resizing, the LGDP4522 writes the data of the resized image in both horizontal and vertical directions according to the resizing factor on the internal GRAM.

RCH[1:0] – Sets the number of pixels made as the remainder in horizontal direction as a result of resizing a picture. By specifying the number of remainder pixels with RCH bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCH = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

RCV[1:0] – Sets the number of pixels made as the remainder in vertical direction as a result of resizing a picture. By specifying the number of remainder pixels with the RCV bits, the data can be transferred without taking the reminder pixels into consideration. Make sure that RCV = 2'h0 when not using the resizing function (RSZ = 2'h0) or there are no remainder pixels.

Table 14: Resizing scale

RSZ[1:0]	Resizing scale
00	No resizing (x 1)
01	x 1/2
10	Setting disabled
11	x 1/4

Table 15: Surplus pixels in horizontal/vertical directions

RCH[1:0]/RCV[1:0]	Surplus pixels
00	0 pixel
01	1 pixel
10	2 pixels
11	3 pixels

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	PTS[2:0]			VLE[1:0]		SPT	0	0	GON	DTE	CL	REV	D[1:0]	

PTS[2:0] – Sets the kind of source output in non-display area in partial display mode. For details, see the "Partial Display Function" section.

Table 16

PTS	Source output in non-display area		Operating grayscale amplifier in non-display area
	Positive polarity	Negative polarity	
000	V63	V0	V0 to V63
001	Setting disabled	Setting disabled	-
010	GND	GND	V0 to V63
011	High impedance	High impedance	V0 to V63
100	V63	V0	V0, V63
101	Setting disabled	Setting disabled	-
110	GND	GND	V0, V63
111	High impedance	High impedance	V0, V63

VLE[1:0] – When VLE[0] = "1", the first display is scrolled up in vertical direction. When VLE[1] = "1", the second display is scrolled up in vertical direction. The first and second displays cannot be scrolled simultaneously. This function is not available with the external display interface. In this case, set VLE to "00".

Table 17

VLE	2nd display image	1st display image
00	Fixed	Fixed
01	Fixed	Scroll up
10	Scroll up	Fixed
11	Setting disabled	

SPT – When SPT = "1", the LCD is driven in 2 split screens. For details, see the "Partial Display Function" section. This function is not available with the external display interface. In this case, set SPT to "0".

GON, DTE – Sets the output level of gate lines G1 to G220 as follows.

Table 18

GON	DTE	Gate output G1 to G220
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

CL – When CL = "1", the 8-color display mode is selected. For details, see the "8-Color Display Mode" section. The 8-color display mode is not available in external interface mode.

REV – By setting REV = "1", the grayscale levels can be inverted. This means, the REV bit allows both normally black and normally white panels to display a same image from the same data. The source output level during front and back porch periods and a blank period in partial display mode is set with the PTS bits.

Table 19

REV	GRAM data (RGB each)	Source output in display area	
		Positive polarity	Negative polarity
0	00h	V63	V0
	⋮	⋮	⋮
	3Fh	V0	V63
1	00h	V0	V63
	⋮	⋮	⋮
	3Fh	V63	V0

D[1:0] – A graphics display appears on the screen when D[1] = "1", and is turned off upon setting D[1] = "0". When setting D[1] = "0", the graphics display data are retained in the internal GRAM and the display appears instantly on the screen upon setting D[1] to "1". When the D[1] bit is "0", i.e. while no display is shown on the screen, all source outputs are at the GND level to reduce charging/discharging current on liquid crystal cells, which is generated during liquid crystal AC drive.

Upon setting D = “00”, the display is turned off and internal display operations are halted completely.

In combination with the GON, DTE bit, the D[1:0] bits controls ON/OFF of graphics display. For details, see the flowcharts in the “Instruction Setting” section.

Table 20

D[1:0]	Source and Vcom outputs	IC internal operation
00	GND	Halt
01	GND	Operate
10	Non-lit display	Operate
11	Display	Operate

Notes:

1. Data write operations from the microcomputer are performed irrespective of the D[1:0] bits.
2. When D[1:0] = “00”, the LGDP4522 is in the same state as the standby mode. However, this does not mean the D[1:0] bits are written over to “00” upon setting the standby mode.

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP[3:0]				0	0	0	0	BP[3:0]			

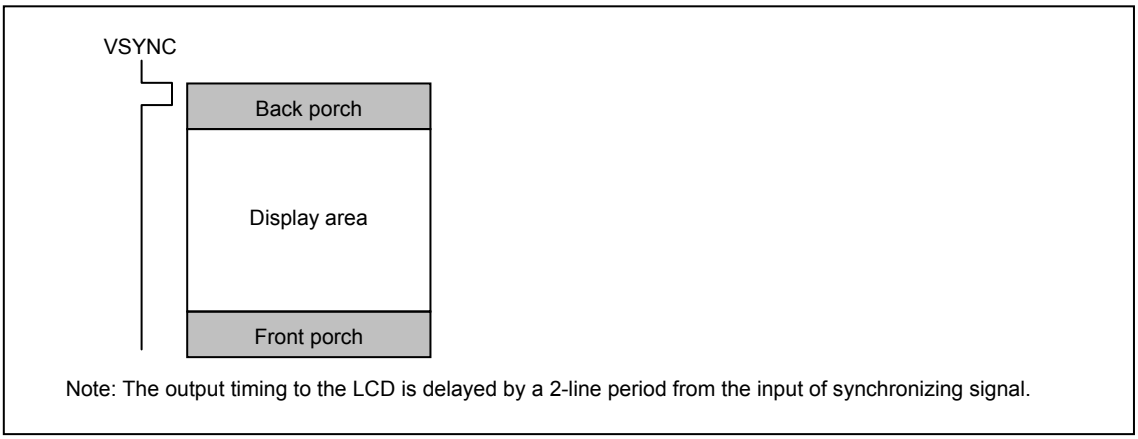
FP[3:0]/BP[3:0] – Sets the blank period made at the beginning and the end of a display (front porch and back porch, respectively). The FP[3:0] and BP[3:0] bits specify the number of lines for the front and back porch periods, respectively. In setting, be sure:

$BP + FP \leq 16$ lines
$FP \geq 2$ lines
$BP \geq 2$ lines

In external display interface mode, a back porch (BP) period starts on the falling edge of the VSYNC signal, followed by a display operation period. After driving the number of lines set with NL bits, a front porch period starts. After the front porch period, a blank period continues until the next input of VSYNC signal.

Table 21

FP/BP	Number of lines for the front/back porches
0	Setting disabled
1	Setting disabled
2	2 lines
3	3 lines
4	4 lines
5	5 lines
6	6 lines
7	7 lines
8	8 lines
9	9 lines
10	10 lines
11	11 lines
12	12 lines
13	13 lines
14	14 lines
15	Setting disabled



Note: The output timing to the LCD is delayed by a 2-line period from the input of synchronizing signal.

Figure 10: Back/front porches

Set the BP[3:0], FP[3:0] bits as follows in each operation mode.

Table 22

Internal clock operation	**FLD[1:0] = "01"**	BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
	FLD[1:0] = "11"	BP = 3 lines	FP = 5 lines	
RGB interface		BP ≥ 2 lines	FP ≥ 2 lines	FP + BP ≤ 16 lines
VSYNC interface		BP ≥ 2 lines	FP ≥ 2 lines	FP + BP = 16 lines

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	PTG[1:0]		ISC[3:0]			

PTG[1:0] – Sets the scan mode by the gate driver in non-display area.

Table 23

PTG	Gate outputs in non-display area
00	Normal scan
01	VGL (fixed)
10	Interval scan
11	Setting disabled

ISC[3:0] – Sets the scan cycle by the gate driver when the PTG bits are set to the interval scan mode in non-display area. The scan cycle can be set as (2 * ISC + 1) frames, where ISC is from 1 to 15. In this case, polarity is inverted as gate lines are scanned.

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO[1:0]		SDT[1:0]		0	0	DIV[1:0]		0	RTN[6:1]						0

RTN[6:0] - Sets the 1H (1 line) period in internal oscillator cycles. RTN[6:0] should be greater than or equal to 44 (= 2Ch).

DIV[1:0] – The internal operation is synchronized with the clock, which is divided with the division ratio set with the DIV bits. Set the RTN and DIV bits to adjust frame frequency. If the number of lines for driving liquid crystal is changed, the frame frequency must also be adjusted. See “Frame-Frequency Adjustment Function”. In RGB interface mode, the DIV bits are disabled.

Table 24

DIV	Division ratio	Internal operation clock frequency
0	1	fosc/1
1	2	fosc/2
2	4	fosc/4
3	8	fosc/8

Note: fosc = Frequency of RC oscillation

Formula to calculate frame frequency

$$Frame\ frequency = \frac{fosc}{(Clock\ cycles\ per\ line * Division\ ratio * (Active\ line + BP + FP))}$$

where

fosc = frequency of RC oscillation,
Active line = number of active lines for driving liquid crystal (NL bits),
Division ratio = DIV bits,
Clock cycles per line = RTN bits,
FP = the number of lines for the front porch period and
BP = the number of lines for the back porch period.

SDT[1:0] – Sets the source output delay from the falling edge of gate output.

Table 25

SDT[1:0]	Source output delay	
	Internal operation (internal oscillator)	RGB I/F operation (DOTCLK)
0	2 clocks	8 clocks
1	4 clocks	16 clocks
2	6 clocks	24 clocks
3	8 clocks	32 clocks

NO[1:0] – Sets the non-overlap period of outputs from adjacent gate lines.

Table 26

NO[1:0]	Gate output non-overlap period	
	Internal operation (internal oscillator)	RGB I/F operation (DOTCLK)
0	0 clocks	0 clocks
1	8 clocks	32 clocks
2	12 clocks	48 clocks
3	16 clocks	64 clocks

Note that the clock mentioned in the above description refers to different clocks according to the interface mode in use as follows.

Table 27

Interface mode in use	Reference clock
Internal operation mode	Internal oscillator
RGB interface mode	DOTCLK
VSYNC interface mode	Internal oscillator

External Display Interface Control 1 (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM[1:0]		0	0	RIM[1:0]	

RM – Selects the interface to access the LGDP4522's internal GRAM. The RAM access is possible only via the interface selected with the RM bit. Set RM to "1" when writing display data via the RGB interface. The LGDP4522 allows for setting the RM bit not constrained by the mode used for the display operation. This means it is possible to rewrite display data via a system interface by setting RM = "0" even while display operations are performed via the RGB interface.

Table 28: RM bit

RM	Interface for RAM access
0	System interface/VSYNC interface
1	RGB interface

RIM[1:0] – Selects one of the following RGB interface modes when the RGB interface mode is selected with the RM and DM bits. Make this setting before display operation via external display interface. Do not make changes to the setting during display operation.

Table 29: RIM[1:0] bits

RIM	RGB interface mode
0	18-bit RGB interface (1 transfer/pixel)
1	16-bit RGB interface (1 transfer/pixel)
2	6-bit RGB interface (3 transfers/pixel)
3	Setting disabled

DM[1:0] – Sets the display operation mode. By setting DM[1:0] as follows, it is possible to switch between the internal clock operation mode and the external display interface mode. Do not switch between different external interface modes (RGB interface and VSYNC interface).

Table 30: DM[1:0] bits

DM	Display operation mode
0	Internal clock operation
1	RGB interface
2	VSYNC interface
3	Setting disabled

Notes:

1. Instructions are set only via the system interface.
2. Be sure that data transfer and dot clock input are performed in units of RGB dots in 6-bit RGB interface mode.

As the following table, the optimum interface for the state of display can be selected by setting the external display interface mode.

Table 31

Display State	Operation mode	RAM access (RM)	Display mode (DM)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 0)	RGB interface (DM = 01)
Rewrite still picture area while display moving pictures	RGB interface (2)	RGB interface (RM = 0)	RGB interface (DM = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM = 10)

Notes:

1. Instructions are set only via the system interface.
2. The RGB-I/F and the VSYNC-I/F are not used simultaneously.
3. Do not make changes to the RGB-I/F mode setting (RIM) while the RGB I/F is in operation.
4. See the “External Display Interface” section for the flowcharts to follow when switching from one mode to another.

Internal clock operation mode

All display operations are synchronized with the signals generated from the internal operating clock in this mode. None of inputs via the external display interface are valid. The internal RAM is accessible only via the system interface.

RGB interface mode (1)

In RGB interface mode, display operations are synchronized with the frame synchronizing signal (VSYNC), the line synchronizing signal (HSYNC), and the dot clock (DOTCLK). These signals must be supplied through a display period using the RGB interface.

Display data are transferred in units of pixels via the DB[17:0] pins. All display data are stored in the internal RAM. The combined use of the high-speed RAM write mode and the widow address function enables not only displaying data in moving picture area and data in the internal RAM in other than the moving picture area at a time but also minimizing data transfer by transferring data only when rewriting screen.

The front porch (FP) and back porch (BP) periods, and the display duration period (NL) are automatically calculated inside the LGDP4522 by internally counting the number of line synchronizing signal clocks (HSYNC) from the falling edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring RGB data via the DB[17:0] pins.

RGB interface mode (2)

The LGDP4522 enables rewriting RAM data via the system interface while the RGB interface is selected for display operation. In this case, Be sure to write RAM data while display data are not being transferred via the RGB interface (ENABLE = High). To return to the display data transfer mode via the RGB interface, change the ENABLE bit first and then set a new address (AD[15:0]) in the AC and the index register to R22h.

VSYNC interface mode

In VSYNC interface mode, internal display operations are synchronized with the frame synchronizing signal (VSYNC). In this mode, a moving picture can be displayed via the system interface by writing data to the internal RAM at more than the minimum speed from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and method. For details, see “External Display Interface”.

No external signal input except VSYNC input is accepted in VSYNC interface mode.

The timings and durations of front porch (FP), back porch (BP) periods and display duration period (NL) are automatically calculated from the falling edge of the frame synchronization signal (VSYNC) according to the instructions set in the relevant registers.

Power Control 1 (R10h)

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP[2:0]			0	BT[2:0]			0	AP[2:0]			0	DK	SLP	STB
W	1	0	0	0	0	0	DC1[2:0]			0	DC0[2:0]			0	VC[2:0]		

SAP[2:0] – Adjusts the constant current in the operational amplifier circuit for the source driver. Setting a larger constant current stabilizes the operational amplifier circuit, but current consumption also increases. Adjust the constant current taking the trade-off between display quality and current consumption into account. During no display period, set SAP[2:0] = "000" to halt the operational amplifier circuit to reduce current consumption.

Table 32

SAP[2:0]	DC current of op-amp
0	Halt
1	Setting disable
2	0.5
3	0.75
4	1
5	1.25
6	1.5
7	1.75

Note: The DC current in the table is shown as the ratio to the DC current when SAP[2:0] = "100".

BT[2:0] – Changes the rate applied to the step-up circuit. Adjust the step-up rate according to the voltage in use. To reduce current consumption, set a smaller step-up rate.

AP[2:0] – Adjusts the constant current in the operational amplifier circuit in the LCD power supply circuit. Setting a larger constant current stabilizes the operational amplifier circuit, but current consumption increases. Adjust the constant current taking the trade-off between display quality and current consumption into account. During no display period, set AP[2:0] = "000" to halt the operational amplifier circuit and step-up circuits to reduce current consumption.

Table 33

AP[2:0]	DC current of op-amp
0	Halt
1	0.25
2	0.5
3	1
4	2
5	3
6	4
7	5

Note: The DC current in the table is shown as the ratio to the DC current when AP[2:0] = "100".

DK – Controls the operation of step-up circuit 1. In supplying power to the LGDP4522, stop generating VLOUT1 for a moment, and wait until the VLOUT2 level is stabilized. Then start generating the VLOUT1 level. For details, see the "Power Supply Setting" section.

SLP – When SLP = "1", the LGDP4522 enters the sleep mode. In sleep mode, internal display operation except RC oscillation is halted to reduce current consumption. In sleep mode, only the following instructions, BT, DC0, DC1, AP, SLP, STB, VRH, VINIT, and VCM, are accepted. No changes to the

GRAM data or other instruction sets are accepted. In sleep mode, the GRAM data and the instruction sets before entering the sleep mode are retained.

STB – When STB = "1", the LGDP4522 enters the standby mode. In standby mode, display operations are completely halted, and all internal operations including internal RC oscillation and reception of external clocks are halted. See the "Instruction Setting" section for the sequence. Only the instruction to exit the standby mode (STB = "0") or that to start oscillators is accepted during standby mode. GRAM data and instruction sets are susceptible to destruction and must be set again after exiting the standby mode.

DC0[2:0] – Selects the operating frequency of the step-up circuit 1. A higher step-up operating frequency enhances the driving capacity of the step-up circuit and the quality of display. Adjust the frequency taking the trade-off between display quality and current consumption into account.

DC1[2:0] – Selects the operating frequency of the step-up circuit 2. A higher step-up operating frequency enhances the driving capacity of the step-up circuit and the quality of display. Adjust the frequency taking the trade-off between display quality and current consumption into account.

Note: Setting step-up cycles of step-up circuits ½, be sure the step-up cycle of the step-up circuit 1 is more than that of the step-up circuit 2 (step-up frequency 1 ≥ step-up frequency 2).

Table 34

DC0[2:0]	fDCDC1
0	Oscillation clock / 16
1	Oscillation clock / 32
2	Oscillation clock / 64
3	Oscillation clock / 128
4	Oscillation clock / 256
5	Oscillation clock / 512
6	Oscillation clock / 1024
7	Oscillation clock / 2048

Table 35

DC1[2:0]	fDCDC2
0	Oscillation clock / 32
1	Oscillation clock / 64
2	Oscillation clock / 128
3	Oscillation clock / 256
4	Oscillation clock / 512
5	Oscillation clock / 1024
6	Oscillation clock / 2048
7	Oscillation clock / 4096

Note: Be sure fDCDC1 ≥ fDCDC2 when setting DC0, DC1.

VC[2:0] – Sets the rate applied to VciLVL to generate the reference voltage for the VREG1OUT and VciOUT levels.

BT[2:0]	VLOUT1 (DDVDH)	VLOUT4 (VCL)	VLOUT2 (VGH)	VLOUT3 (VGL)	Capacitor connection pins
0	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x6]	-(Vci1 + DDVDH x2) [x-5]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
1	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x6]	-(DDVDH x2) [x-4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
2	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x6]	-(Vci1 + DDVDH) [x-3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
3	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 + DDVDH x 2 [x5]	-(Vci1 + DDVDH x2) [x-5]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
4	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 + DDVDH x 2 [x5]	-(DDVDH x2) [x-4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
5	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 + DDVDH x 2 [x5]	-(Vci1 + DDVDH) [x-3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
6	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 2 [x4]	-(DDVDH x2) [x-4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
7	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 2 [x4]	Vci1 + DDVDH) [x-3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±

Notes:

1. The step-up rate from the Vci1 level is shown in the bracket [ ] in the above table.
2. When using the DDVDH, VCL, VGH and VGL voltage levels, connect a capacitor to each capacitor connection pin.
3. Set the following voltages within the limits: DDVDH = max 5.5V, VCL = min –3.3V, VGH = max 16.5V, VGL = min –16.5V.

Table 36

VC[2:0]	VciOUT output voltage
0	VciLVL
1	0.93 x VciLVL
2	0.88 x VciLVL
3	0.82 x VciLVL
4	0.78 x VciLVL
5	0.74 x VciLVL
6	Setting disabled
7	Setting disabled

Table 37

DK	Operation of step-up circuit 1
0	Operate
1	Halt

Power Control 3 (R12h)

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH[3:0]			
W	1	0	0	VCOMG	VDV[4:0]					0	VCM[6:0]						

PON – Controls ON/OFF of VLOUT3 output. To stop VLOUT3 output, set PON to “0”. To start VLOUT3 output, set PON to “1”.

VRH3-0 – Sets the amplifying rate (1.38 to 1.83) applied to REGP to output the VREG1OUT level, which is a reference level for the VCOM level and the grayscale voltage level.

VCOMG – When VCOMG = “1”, the LGDP4522 can output a negative voltage level for VcomL (1.0V to –Vci+0.5V Max.). When VCOMG = “0”, the LGDP4522 halts the amplifier for negative voltage to

save power. When VCOMG = “0”, the VDV bits are disabled. In this case, adjust the amplitude of Vcom AC voltage with the VCM bits (VcomH setting). Set PON to “1” before setting VCOMG to “1”.

VDV[4:0] – Sets the amplitude of Vcom AC voltage. The VDV bits can set the Vcom amplitude 0.6 to 1.23 times the VREG1OUT level. If VCOMG = “0”, the VDV bits are disabled.

VCM[6:0] – Set the VcomH level (the high level of Vcom AC voltage). The VCM bits can set the VcomH level 0.4 to 0.98 times the VREG1OUT level. To stop adjusting VcomH with the internal volume and adjust it with an external resistor from VcomR, set VCM = “11111”.

Table 38: VRH

VRH[4:0]	VREG1OUT voltage
0 to 7	Halt
8	VciOUT x 1.38
9	VciOUT x 1.45
A	VciOUT x 1.53
B	VciOUT x 1.60
C	VciOUT x 1.68
D	VciOUT x 1.75
E	VciOUT x 1.83
F	Setting disable

Table 39

VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH	VCM [6:0]	VcomH
00h	VREG1OUT x 0.400	20h	VREG1OUT x 0.555	40h	VREG1OUT x 0.715	60h	VREG1OUT x 0.875
01h	VREG1OUT x 0.400	21h	VREG1OUT x 0.560	41h	VREG1OUT x 0.720	61h	VREG1OUT x 0.880
02h	VREG1OUT x 0.405	22h	VREG1OUT x 0.565	42h	VREG1OUT x 0.725	62h	VREG1OUT x 0.885
03h	VREG1OUT x 0.410	23h	VREG1OUT x 0.570	43h	VREG1OUT x 0.730	63h	VREG1OUT x 0.890
04h	VREG1OUT x 0.415	24h	VREG1OUT x 0.575	44h	VREG1OUT x 0.735	64h	VREG1OUT x 0.895
05h	VREG1OUT x 0.420	25h	VREG1OUT x 0.580	45h	VREG1OUT x 0.740	65h	VREG1OUT x 0.900
06h	VREG1OUT x 0.425	26h	VREG1OUT x 0.585	46h	VREG1OUT x 0.745	66h	VREG1OUT x 0.905
07h	VREG1OUT x 0.430	27h	VREG1OUT x 0.590	47h	VREG1OUT x 0.750	67h	VREG1OUT x 0.910
08h	VREG1OUT x 0.435	28h	VREG1OUT x 0.595	48h	VREG1OUT x 0.755	68h	VREG1OUT x 0.915
09h	VREG1OUT x 0.440	29h	VREG1OUT x 0.600	49h	VREG1OUT x 0.760	69h	VREG1OUT x 0.920
0Ah	VREG1OUT x 0.445	2Ah	VREG1OUT x 0.605	4Ah	VREG1OUT x 0.765	6Ah	VREG1OUT x 0.925
0Bh	VREG1OUT x 0.450	2Bh	VREG1OUT x 0.610	4Bh	VREG1OUT x 0.770	6Bh	VREG1OUT x 0.930
0Ch	VREG1OUT x 0.455	2Ch	VREG1OUT x 0.615	4Ch	VREG1OUT x 0.775	6Ch	VREG1OUT x 0.935
0Dh	VREG1OUT x 0.460	2Dh	VREG1OUT x 0.620	4Dh	VREG1OUT x 0.780	6Dh	VREG1OUT x 0.940
0Eh	VREG1OUT x 0.465	2Eh	VREG1OUT x 0.625	4Eh	VREG1OUT x 0.785	6Eh	VREG1OUT x 0.945
0Fh	VREG1OUT x 0.470	2Fh	VREG1OUT x 0.630	4Fh	VREG1OUT x 0.790	6Fh	VREG1OUT x 0.950
10h	VREG1OUT x 0.475	30h	VREG1OUT x 0.635	50h	VREG1OUT x 0.795	70h	VREG1OUT x 0.955
11h	VREG1OUT x 0.480	31h	VREG1OUT x 0.640	51h	VREG1OUT x 0.800	71h	VREG1OUT x 0.960
12h	VREG1OUT x 0.485	32h	VREG1OUT x 0.645	52h	VREG1OUT x 0.805	72h	VREG1OUT x 0.965
13h	VREG1OUT x 0.490	33h	VREG1OUT x 0.650	53h	VREG1OUT x 0.810	73h	VREG1OUT x 0.970
14h	VREG1OUT x 0.495	34h	VREG1OUT x 0.655	54h	VREG1OUT x 0.815	74h	VREG1OUT x 0.975
15h	VREG1OUT x 0.500	35h	VREG1OUT x 0.660	55h	VREG1OUT x 0.820	75h	VREG1OUT x 0.980
16h	VREG1OUT x 0.505	36h	VREG1OUT x 0.665	56h	VREG1OUT x 0.825	76h	Setting disabled
17h	VREG1OUT x 0.510	37h	VREG1OUT x 0.670	57h	VREG1OUT x 0.830	77h	Setting disabled
18h	VREG1OUT x 0.515	38h	VREG1OUT x 0.675	58h	VREG1OUT x 0.835	78h	Setting disabled
19h	VREG1OUT x 0.520	39h	VREG1OUT x 0.680	59h	VREG1OUT x 0.840	79h	Setting disabled
1Ah	VREG1OUT x 0.525	3Ah	VREG1OUT x 0.685	5Ah	VREG1OUT x 0.845	7Ah	Setting disabled
1Bh	VREG1OUT x 0.530	3Bh	VREG1OUT x 0.690	5Bh	VREG1OUT x 0.850	7Bh	Setting disabled
1Ch	VREG1OUT x 0.535	3Ch	VREG1OUT x 0.695	5Ch	VREG1OUT x 0.855	7Ch	Setting disabled
1Dh	VREG1OUT x 0.540	3Dh	VREG1OUT x 0.700	5Dh	VREG1OUT x 0.860	7Dh	Setting disabled
1Eh	VREG1OUT x 0.545	3Eh	VREG1OUT x 0.705	5Eh	VREG1OUT x 0.865	7Eh	Setting disabled
1Fh	VREG1OUT x 0.550	3Fh	VREG1OUT x 0.710	5Fh	VREG1OUT x 0.870	7Fh	Setting disabled

Table 40

VDV[4:0]	Vcom amplitude	VDV[4:0]	Vcom amplitude
00h	VREG1OUT x 0.60	10h	VREG1OUT x 1.05
01h	VREG1OUT x 0.63	11h	VREG1OUT x 1.08
02h	VREG1OUT x 0.66	12h	VREG1OUT x 1.11
03h	VREG1OUT x 0.69	13h	VREG1OUT x 1.14
04h	VREG1OUT x 0.72	14h	VREG1OUT x 1.17
05h	VREG1OUT x 0.75	15h	VREG1OUT x 1.20
06h	VREG1OUT x 0.78	16h	VREG1OUT x 1.23
07h	VREG1OUT x 0.81	17h	Setting disabled
08h	VREG1OUT x 0.84	18h	Setting disabled
09h	VREG1OUT x 0.87	19h	Setting disabled
0Ah	VREG1OUT x 0.90	1Ah	Setting disabled
0Bh	VREG1OUT x 0.93	1Bh	Setting disabled
0Ch	VREG1OUT x 0.96	1Ch	Setting disabled
0Dh	VREG1OUT x 0.99	1Dh	Setting disabled
0Eh	VREG1OUT x 1.02	1Eh	Setting disabled
0Fh	Setting disabled	1Fh	Setting disabled

Notes:

1. Adjust VREG1OUT and VCM so that VcomH are set within the range 3.0 to (DDVDH – 0.5)V
2. Adjust VREG1OUT and VDV so that the amplitude of Vcom are set to 6.0V or less.

RAM Address Set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD[15:0]															

AD[15:0] – Represents the GRAM address set in the AC (Address Counter) initially. The address in the AC is automatically updated in accordance with the AM, I/D bits as data are written to the internal GRAM so that data are written consecutively without resetting an address in the AC. The address is not automatically updated when reading data from the internal GRAM.

It is not possible to set an address in the AC when the LGDP4522 is in standby mode. Also be sure to set an address within the window address area.

Notes:

1. When the RGB interface is selected (RM = “1”), the address AD is set in the address counter every frame on the falling edge of VSYNC.
2. When the internal clock operation or the VSYNC interface mode is selected (RM = “0”), the address AD is set when executing an instruction.

Table 41: GRAM address range

AD[15:0]	GRAM setting
0000 – 00AF	Bitmap data for G1
0100 – 01AF	Bitmap data for G2
0200 – 02AF	Bitmap data for G3
0300 – 03AF	Bitmap data for G4
⋮	⋮
EC00 – ECAF	Bitmap data for G237
ED00 – EDAF	Bitmap data for G238
EE00 – EEAF	Bitmap data for G239
EF00 – EFAF	Bitmap data for G240

Write Data to GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	WD[17:0]															

WD[17:0] – If data are less than 18 bits in unit, the LGDP4522 expands the data into 18 bits internally before written to the internal GRAM. How the data are expanded into 18 bits differs for each interface and data transfer mode.

The grayscale level is selected according to GRAM data. The GRAM address is automatically updated according to the AM and I/D bits as data are written to the internal GRAM. In standby mode, no access to the internal GRAM is allowed. When the 8 or 16 bit interface mode is selected, data are expanded into 18 bits internally by writing the MSBs of R and B dots to the LSBs of R and B dots respectively.

When writing data to the GRAM via a system interface while using the RGB interface, be sure there is no conflict between writing operations via respective interfaces (RGB and system interfaces). When the18-bit RGB interface is selected, 18-bit data are written via the DB[17:0] pins and 262,144 colors are available. When the 16-bit RGB interface is selected, the MSBs of R and B dots are also written to the LSBs of R and B dots respectively, and 65,536 colors are available.

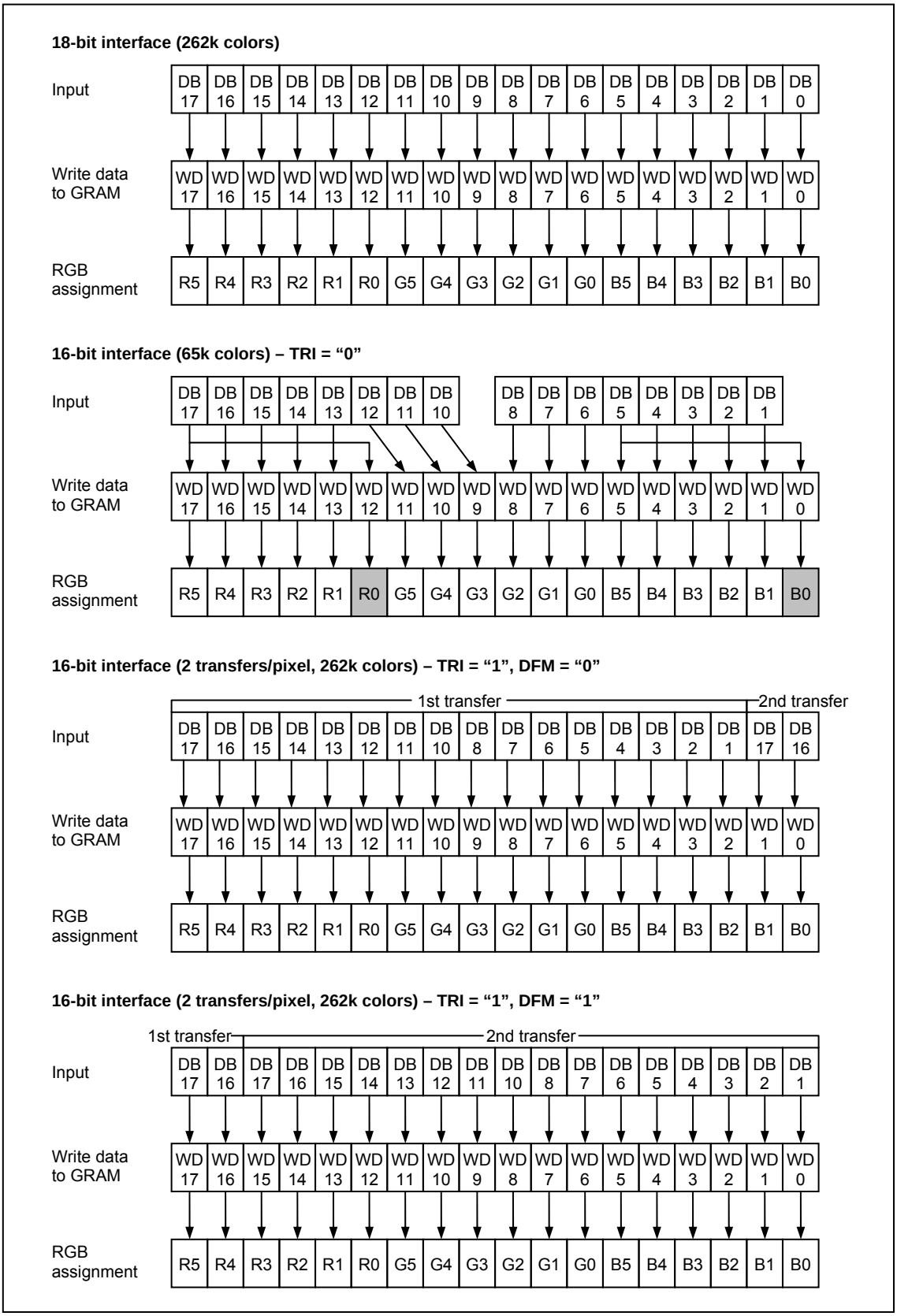


Figure 11: Write data to GRAM in 18-/16-bit interface mode

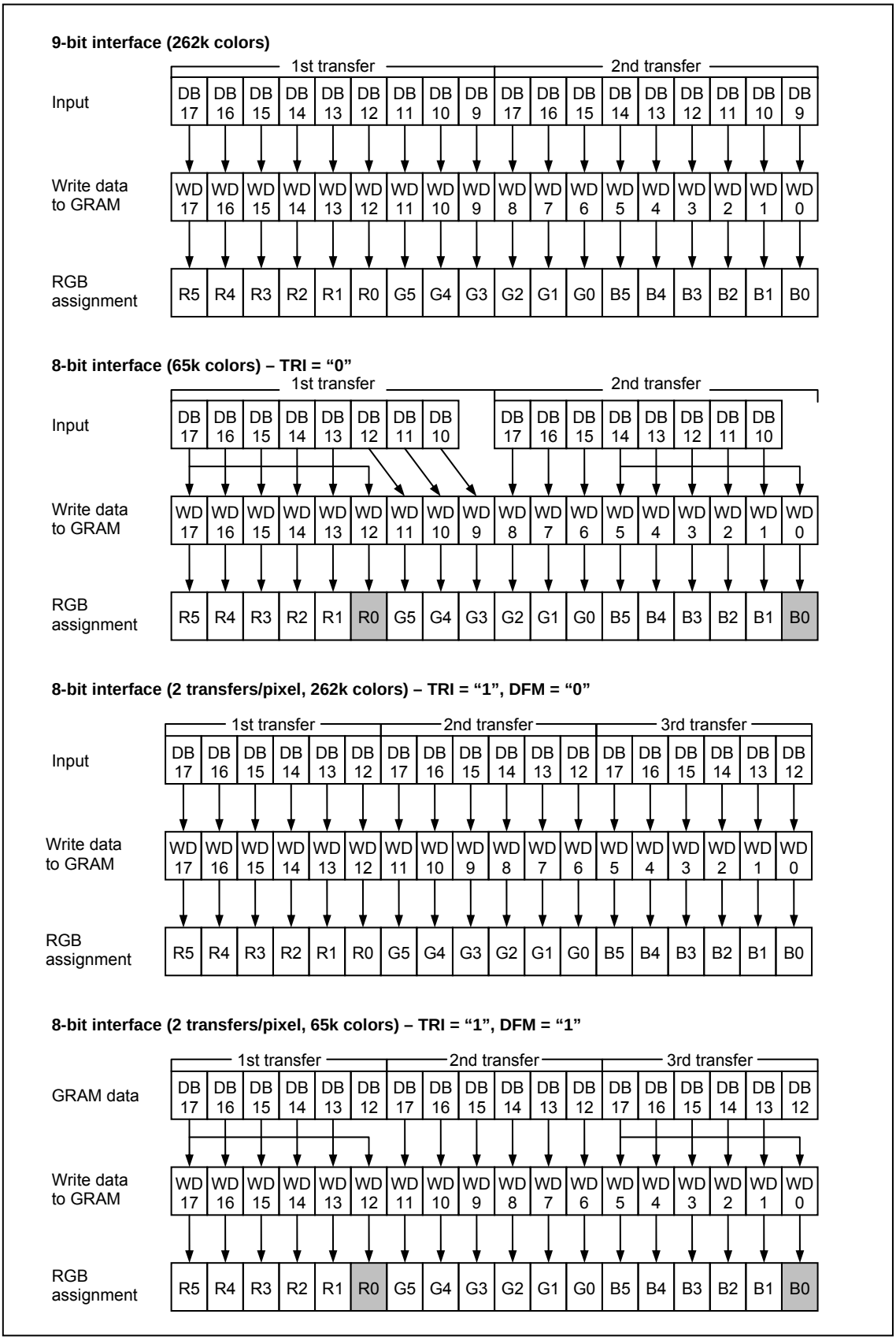


Figure 12: Write data to GRAM in 9-/8-bit interface mode

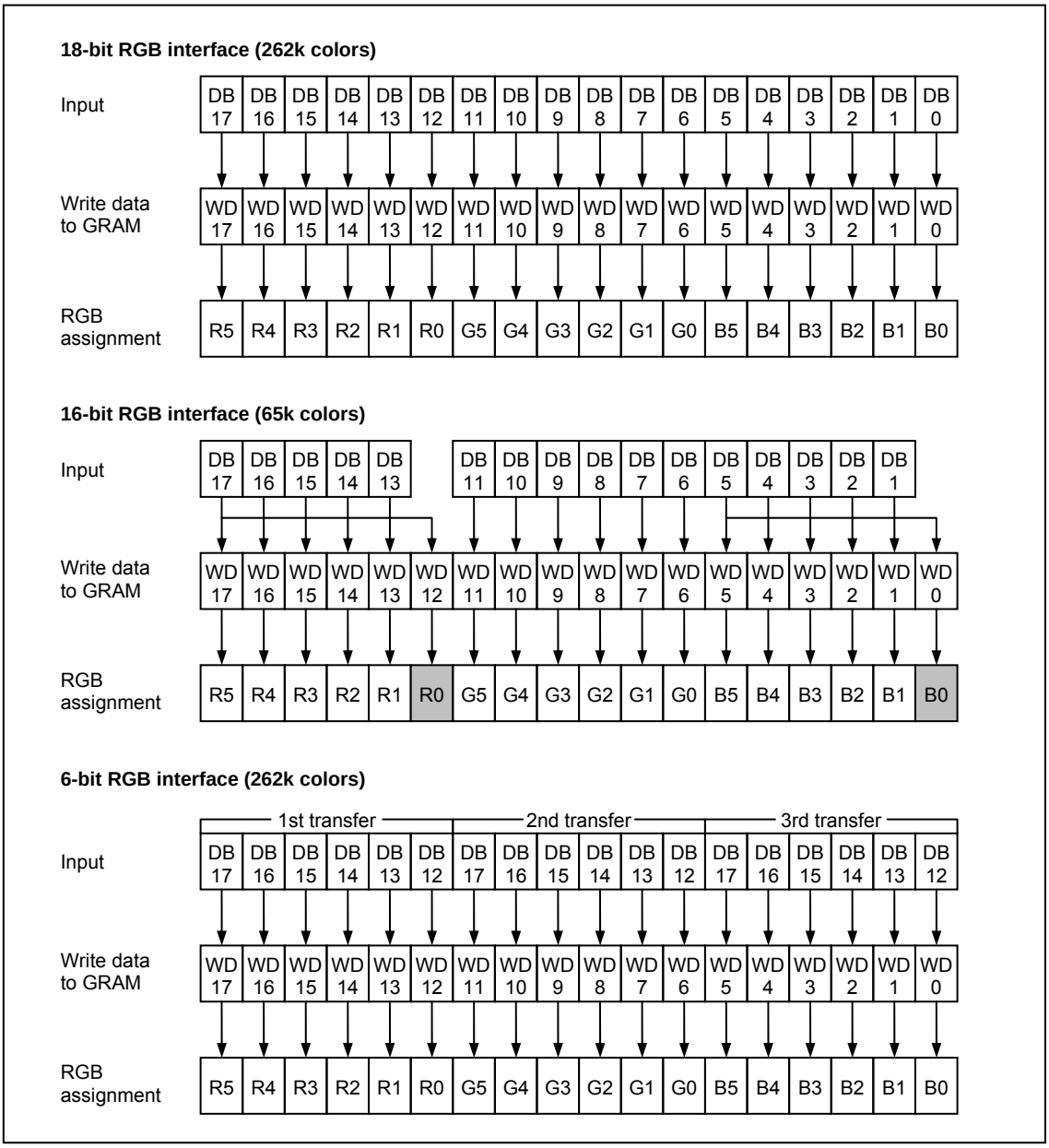


Figure 13: Write data to GRAM in 18-/16-/6-bit RGB interface mode

Table 42: GRAM data and LCD output level

GRAM data setting: RGB each	Grayscale	
	Negative	Positive
0	V0	V63
1	V1	V62
2	V2	V61
3	V3	V60
⋮	⋮	⋮
60	V60	V3
61	V61	V2
62	V62	V1
63	V63	V0

RAM Access via RGB I/F and System I/F

In RGB interface mode, the LGDP4522 stores all display data in the internal RAM, enabling transferring only moving picture data only when updating the frames of a moving picture. While the moving picture frames are not updated, it is possible to write data displayed in the area outside the moving picture area via the system interface.

In RGB interface mode, the LGDP4522 writes data to the internal RAM in synchronization with DOTCLK during ENABLE = “Low”. To access the internal RAM via the system interface while using the RGB interface for display operation, set ENABLE “High” to stop writing via the RGB interface. To start accessing the internal RAM via the RGB interface after accessing the RAM via the system interface, wait at least for a write/read bus cycle time. Data will not be written properly to the internal RAM when writing operations via both RGB and system interfaces are conflicting.

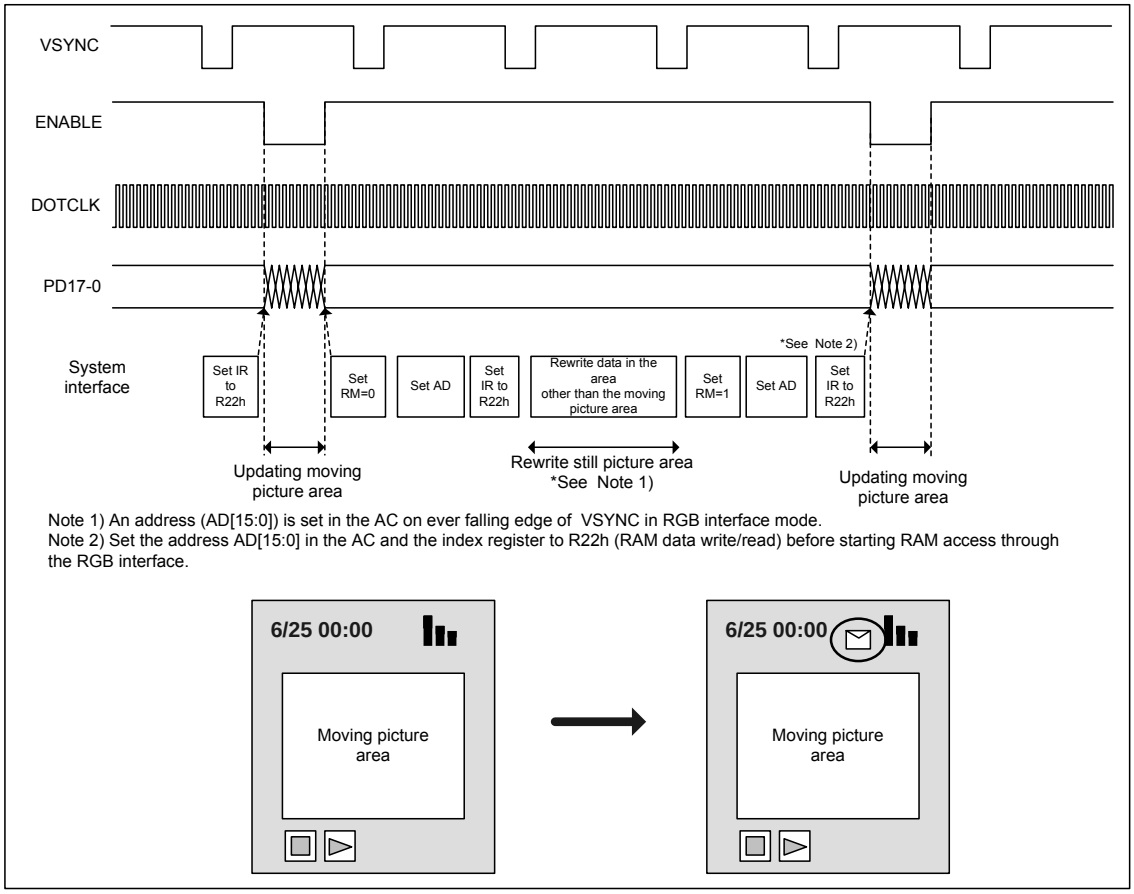


Figure 14

Read Data Read from GRAM (R22h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	RD[17:0]															

RD[17:0] – Reads 18-bit data from the GRAM. The bit assignment between the data read out from the GRAM and the DB[17:0] pins differs for each interface.

When data are read out from the GRAM to the microcomputer, the first word read immediately after executing RAM address set is taken in the internal read data latch and invalid data are sent to the data bus DB[17:0]. Valid data are sent to the data bus as the LGDP4522 reads out the second word data from the internal GRAM.

The 1st word data read into the internal read data latch are used for a bit operation (logical/compare operation) is performed inside the LGDP4522. Accordingly, the bit operation is processed with one read out operation. Note that the bit operation is performed on the data in units of 18 bits.

When the 8 or 16-bit interface is selected, the LSBs of R and B dots are not read out.

Note: This register is not available with the RGB interface.

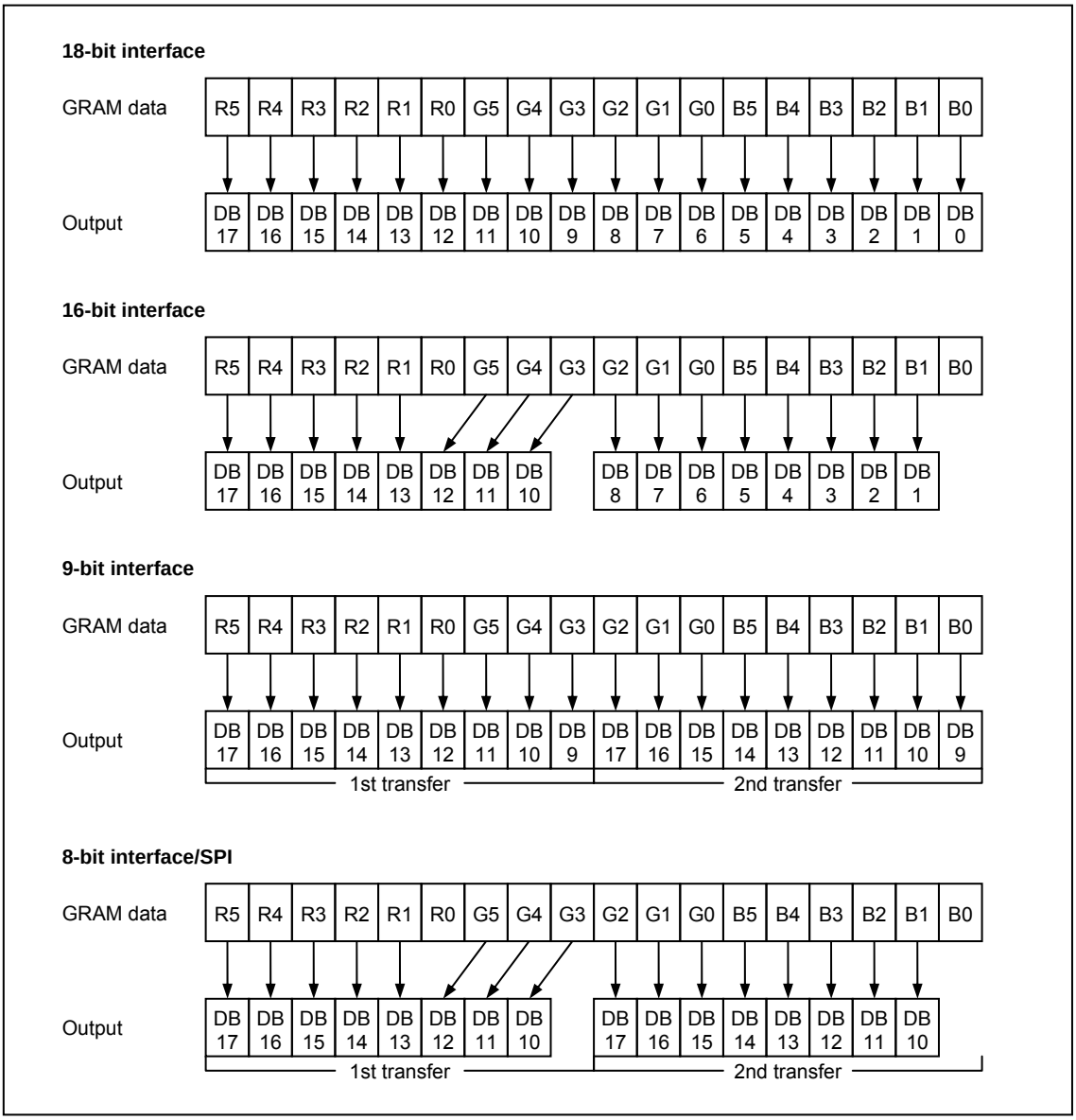


Figure 15: Read data from GRAM

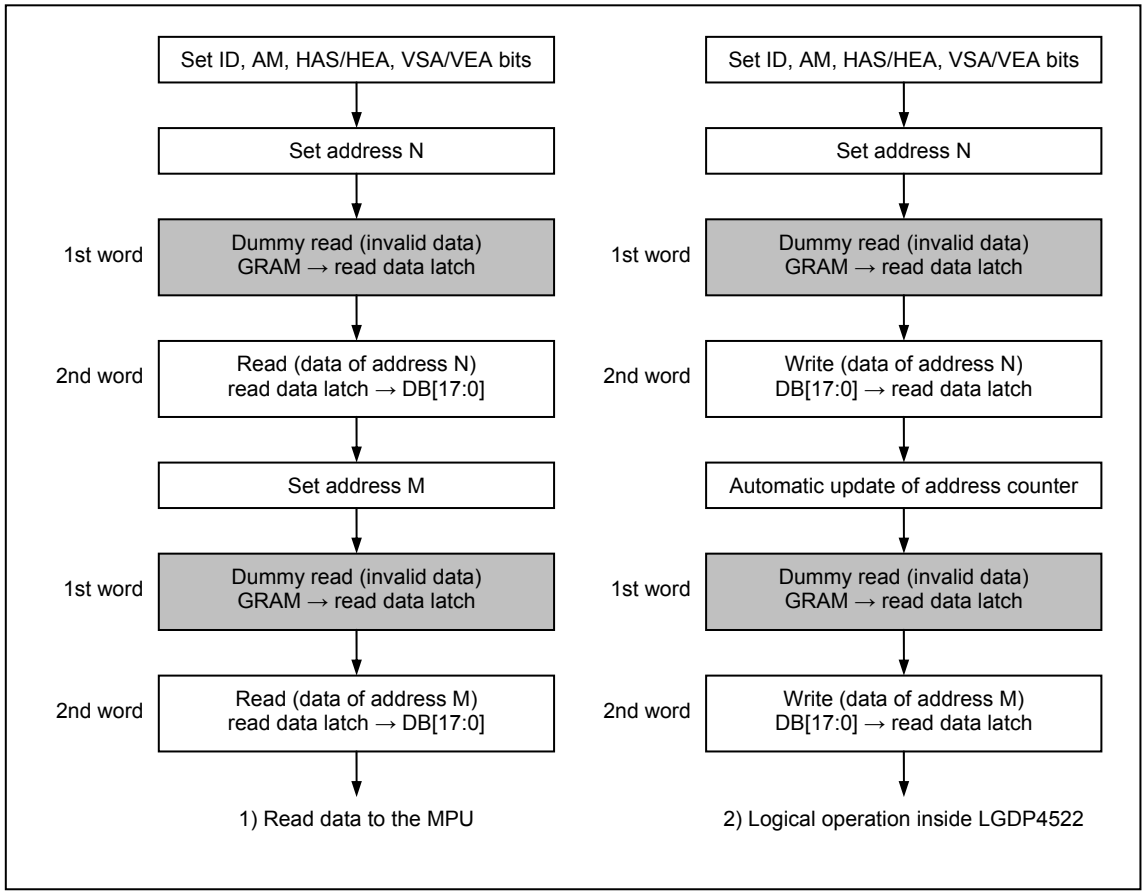


Figure 16: GRAM read sequence

γ Control (R30h to R39h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	PKP1[2:0]			0	0	0	0	0	PKP0[2:0]		
W	1	0	0	0	0	0	PKP3[2:0]			0	0	0	0	0	PKP2[2:0]		
W	1	0	0	0	0	0	PKP5[2:0]			0	0	0	0	0	PKP4[2:0]		
W	1	0	0	0	0	0	PRP1[2:0]			0	0	0	0	0	PRP0[2:0]		
W	1	0	0	0	0	0	PKN1[2:0]			0	0	0	0	0	PKN0[2:0]		
W	1	0	0	0	0	0	PKN3[2:0]			0	0	0	0	0	PKN2[2:0]		
W	1	0	0	0	0	0	PKN5[2:0]			0	0	0	0	0	PKN4[2:0]		
W	1	0	0	0	0	0	PRN1[2:0]			0	0	0	0	0	PRN0[2:0]		
W	1	0	0	0	VRP1[4:0]					0	0	0	0	VRP0[3:0]			
W	1	0	0	0	VRN1[4:0]					0	0	0	0	VRN0[3:0]			

PKP5-0[2:0] – γ fine adjustment register bits for positive polarity

PRP1-0[2:0] – γ gradient adjustment register bits for positive polarity

PKN5-0[2:0] – γ fine adjustment register bits for negative polarity

PRN1-0[2:0] – γ gradient adjustment register bits for negative polarity

VRP0[3:0]/VRP1[4:0] – amplitude adjustment register bits for positive polarity

VRN0[3:0]/VRN1[4:0] – amplitude average adjustment register bits for negative polarity

For details see "γ-Correction Function" section

Gate Scan Position (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN[4:0]				

SCN[4:0] – The LGDP4522 allows specifying the gate line from which the gate driver starts scan by setting the SCN4-0 bits.

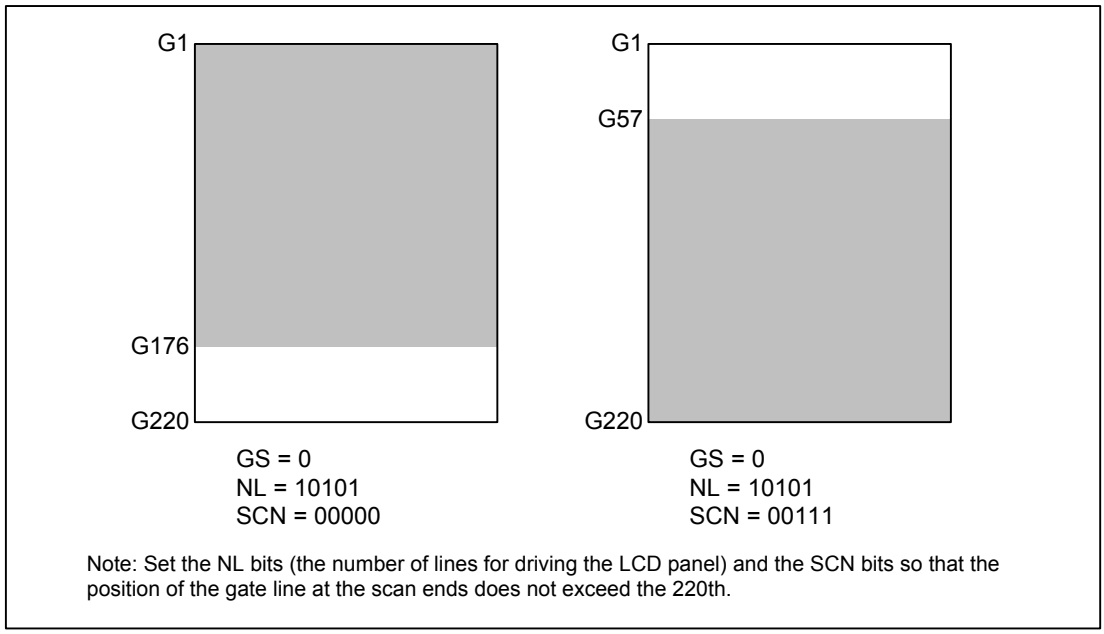


Figure 17

Table 43

SCN[4:0]	Scan start position (gate line)	
	GS = "0"	GS = "1"
00h	G1	G220
01h	G9	G212
02h	G17	G204
03h	G25	G196
04h	G33	G188
05h	G41	G180
06h	G49	G172
07h	G57	G164
08h	G65	G156
09h	G73	G148
0Ah	G81	G140
0Bh	G89	G132
0Ch	G97	G124
0Dh	G105	G116
0Eh	G113	G108
0Fh	G121	G100
10h	G129	G92
11h	G137	G84
12h	G145	G76
13h	G153	G68
14h	G161	G60
15h	G169	G52
16h	G177	G44
17h	G185	G36
18h	G193	G28
19h	G201	G20
1Ah	G209	G12
1Bh	G217	G4

Vertical Scroll Control (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL[7:0]							

VL[7:0] – Sets the scrolling amount of an image on the screen in vertical direction. The scrolling amount can be set from 0 line to 220 lines. The start position for displaying the image is shifted vertically by the number of lines set with the VL bits. The part of the image, which is scrolled out from the end line (the 220th line) as a result of scrolling, is displayed from the 1st line of the physical display. The VL bits are enabled when either first display vertical scroll enable bit VLE[0] or the second display vertical scroll enable bit VLE[1] is set to "1". When VLE[1:0] = "00", the image on the screen is displayed at the position set with the SS and SE bits. The vertical scrolling function is not available with the external display interface.

Table 44

VL[7:0]	Scrolling lines
0	0 line
1	1 line
2	2 lines
⋮	⋮
218	218 line
219	219 lines

1st-Screen Drive Position (R42h)

2nd-Screen Drive Position (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE1[7:0]								SS1[7:0]							
W	1	SE2[7:0]								SS2[7:0]							

SS1[7:0] – Sets the position of the start line from which the first display starts. The gate driver starts scan from the line of the number set with the SS1 bits + 1.

SE1[7:0] – Sets the position of the end line at which the first display ends. The gate driver ends scan at the line of the number set with the SE1 bits + 1. For instance, when SS1 = 07h and SE1 = 10h, the first display is shown on the gate lines from G8 to G17, and gate lines G1 to G7 and G18 thereafter are driven to show a blank screen. Be sure that SS1 ≤ SE1 ≤ EFh. For details, see the “Partial Display Function” section.

SS2[7:0] – Sets the position of the start line from which the second display starts. The gate driver starts scan from the line of the number set with the SS2 bits + 1. The second display is shown when SPT = “1”.

SE2[7:0] – Sets the position of the end line at which the second display ends. The gate driver ends scan at the line of the number set with the SE2 bits + 1. For instance, when SPT = “1”, and SS2 = 20h, SE2 = 4Fh, the second display is shown on the gate lines from G33 to G80.

Be sure that SS1 ≤ SE1 < SS2 ≤ SE2 ≤ EFh. For details, see the “Partial Display Function” section.

Horizontal RAM Address Position (R44h)

Vertical RAM Address Position (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA[7:0]								HSA[7:0]							
W	1	VEA[7:0]								VSA[7:0]							

HSA[7:0]/HEA[7:0] – HSA and HEA represent the respective addresses at the start and end of the window address area in horizontal direction. By setting HSA and HEA bits, it is possible to limit the area on the GRAM horizontally for writing data. The HSA and HEA bits must be set before starting RAM write operation. In setting these bits, be sure 00h ≤ HSA < HEA ≤ AFh.

VSA[7:0]/VEA[7:0] – VSA and VEA represent the respective addresses at the start and end of the window address area in vertical direction. By setting VAS and VEA bits, it is possible to limit the area on the GRAM vertically for writing data. The VSA and VEA bits must be set before starting RAM write operation. In setting, be sure 00h ≤ VSA < VEA ≤ EFh.

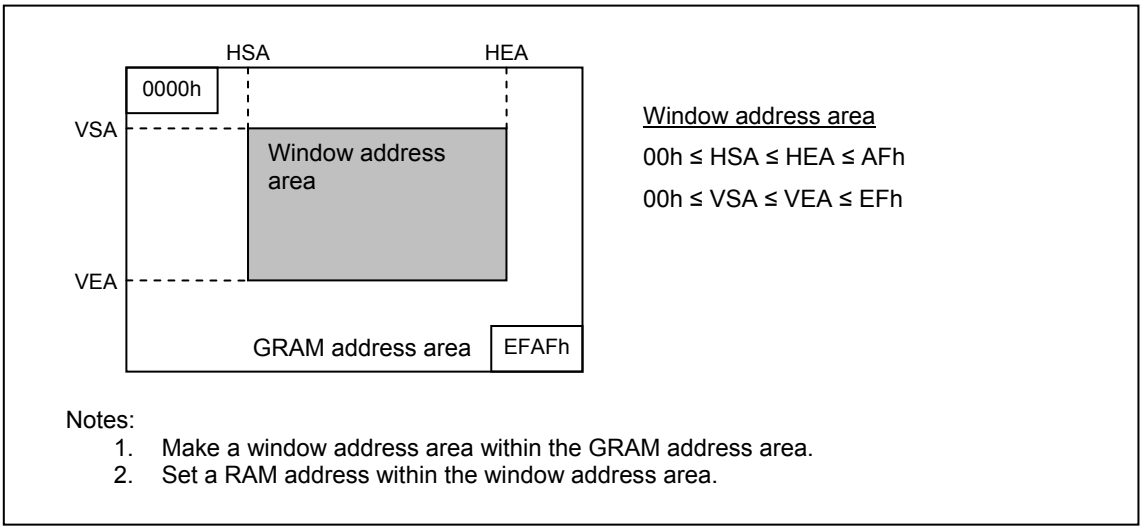


Figure 18: GRAM address and window address area

EPROM Control 1 (R60h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	POR	VPP	PPROG	PWE	PA[1:0]		0	PDIN[6:0]						

EPROM programming control. See “EPROM Control” section.

POR – Power-on reset.

VPP – Power switch control for the VPP pin of the embedded EPROM. When VPP = “1”, the internal VPP is set to 7.2V; otherwise it is set to 1.8V.

PPROG – Program mode enable.

PWE – Write enable.

PA[1:0] – Program address input. This selects one of four banks of the EPROM.

PDIN[6:0] – Data input. This corresponds to VCM[6:0] bits of R13h.

EPROM Control 2 (R61h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	RA[1:0]		VCMSEL[1:0]	

EPROM read control. See “EPROM Control” section.

RA[1:0] – Read address input. This selects one of four banks of the EPROM.

VCMSEL[1:0] – With VCMSEL pin, sets VcomH level from either the register R13h or the EPROM.

Table 45

VCMSEL[1:0]	VCMSEL pin	VcomH level adjustment
00	X	VCM[6:0] of the register R13h
01	X	EPROM data selected by RA[1:0]
1X	0	VCM[6:0] of the register R13h
1X	1	EPROM data selected by RA[1:0]

Test Register 1 (R71h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	T8CL	TPOL[1:0]		0	0	TOSC	TFN

TFN – Sets the chip to function test mode.

TOSC – Sets the pin FLM to output the internal oscillator signal instead of the frame head pulse signal.

TPOL[1:0] – When TPOL[1] = “1”, liquid crystal polarity is fixed to positive polarity if TPOL[0] = “0” or negative polarity if TPOL[0] = “1”. Affected are Vcom and source outputs. When TPOL[0] = “0”, field/line polarity inversion takes place.

T8CL – Fix to “0”.

Instruction List

Table 46

Index	Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Default
00	Start oscillation																1	-
01	Driver output control		VSPL	HSPL	DPL	EPL	SM	GS	SS				NL[4:0]					001B
02	LCD drive AC control					FLD[1:0]		B/C	EOR			NW[5:0]						0400
03	Entry mode	TRI	DFM		BGR							ID[1:0]		AM				0030
04	Resize control							RCV[1:0]				RCH[1:0]				RSZ[1:0]		0000
05	-																	
06	-																	
07	Display control 1			PTS[2:0]			VLE[1:0]		SPT			GON	DTE	CL	REV	D[1:0]		0000
08	Display control 2					FP[3:0]								BP[3:0]				0808
09	Display control 3											PTG[1:0]		ISC[3:0]				0000
0A	-																	
0B	Frame cycle adjustment	NO[1:0]		SDT[1:0]		EQ[1:0]		DIV[1:0]			RTN[6:1]							002C
0C	External display I/F ctrl								RM			DM[1:0]				RIM[1:0]		0000
10	Power control 1		SAP[2:0]				BT[2:0]				AP[2:0]				DK	SLP	STB	0004
11	Power control 2						DC1[2:0]				DC0[2:0]				VC[2:0]			0000
12	Power control 3												PON	VRH[3:0]				0000
13	Power control 4			VCOMG	VDV[4:0]						VCM[6:0]							0341
14	VDD regulator control						RI[2:0]				RV[2:0]					MULTI[1:0]		0000
21	RAM address set	AD[15:0]																0000
22	RAM data R/W	RAM 18-bit R/W data																-
30	Gamma control 1						PKP1[2:0]								PKP0[2:0]			0000
31	Gamma control 2						PKP3[2:0]								PKP2[2:0]			0000
32	Gamma control 3						PKP5[2:0]								PKP4[2:0]			0000
33	Gamma control 4						PRP1[2:0]								PRP0[2:0]			0000
34	Gamma control 5						PKP1[2:0]								PKP0[2:0]			0000
35	Gamma control 6						PKP3[2:0]								PKP2[2:0]			0000
36	Gamma control 7						PKP5[2:0]								PKP4[2:0]			0000
37	Gamma control 8						PRP1[2:0]								PRP0[2:0]			0000
38	Gamma control 9				VRP1[4:0]									VRP0[3:0]				0000
39	Gamma control 10				VRN1[4:0]									VRN0[3:0]				0000
3A	Gamma selection																SREF	0000
40	Gate scan start position												SCN[4:0]					0000
41	Vertical scroll control									VL[7:0]								0000
42	First screen position	SE1[7:0]								SS1[7:0]								FF00
43	Second screen position	SE2[7:0]								SS2[7:0]								FF00
44	Horizontal RAM address	HEA[7:0]								HSA[7:0]								AF00
45	Vertical RAM address	VEA[7:0]								VSA[7:0]								DB00
60	EPROM control 1			POR	VPP	PPROG	PWE	PA[1:0]			PDIN[6:0]							0000
61	EPROM control 2													RA[1:0]		VCMSEL[1:0]		0000
71	Test register 1										T8CL	TPOL[1:0]			TMEM	TOSC	TFN	0000
72	Test register 2											FVCOML	MVCOML					0000

Interface Specifications

The LGDP4522 has the system interface for making instruction setting and other settings, and the external display interface for displaying a moving picture. The LGDP4522 allows selecting an optimum interface for the display (moving or still picture) in order to transfer data efficiently.

As the external display interface, the LGDP4522 has the RGB interface and the VSYNC interface, enabling data rewrite operation without flicker the moving picture on the screen.

In RGB interface mode, display operations are performed in synchronization with synchronizing signals VSYNC, HSYNC, and DOTCLK. Display data are written to the internal RAM according to the polarity of the data enable signal ENABLE via the moving picture display data bus DB[17:0] in synchronization with VSYNC, HSYNC, and DOTCLK. All display data are stored in the LGDP4522's GRAM to limit data transfer to only when switching the frames of a moving picture. By using the window address function, it is possible to limit the RAM area to be rewritten for displaying a moving picture and display both the moving picture and the data written on the RAM at a time.

In VSYNC interface mode, the internal display operations are synchronized with the frame synchronization signal VSYNC. The VSYNC interface enables a moving picture display via the system interface by writing data to the internal GRAM at more than the minimum speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in speed and method for writing data to the internal RAM.

The LGDP4522 operates in one of the following 4 modes in line with the state of display. The mode for display operation is set in the external interface control register. When switching from one mode to another, refer to the sequences mentioned in the sections of RGB and VSYNC interfaces.

Table 47

Operation mode	RAM access setting (RM)	Display operation mode (DM)
Internal operating clock only: Displaying still pictures	System interface (RM = 0)	Internal operating clock (DM = 0)
RGB interface (1): Displaying moving pictures	RGB interface (RM = 1)	RGB interface (DM = 1)
RGB interface (2): Rewriting still pictures while displaying moving pictures	RGB interface (RM = 1)	RGB interface (DM = 1)
VSYNC interface: Displaying moving pictures	System interface (RM = 0)	VSYNC interface (DM = 2)

Notes:

1. Instructions are set only via the system interface.
2. The RGB I/F and the VSYNC I/F are not available simultaneously.
3. Do not make changes to the RGB I/F mode (RIM[1:0] bits) while an RGB I/F is in operation.
4. See the sections of RGB and VSYNC interfaces for the sequences to follow when switching from one mode to another.

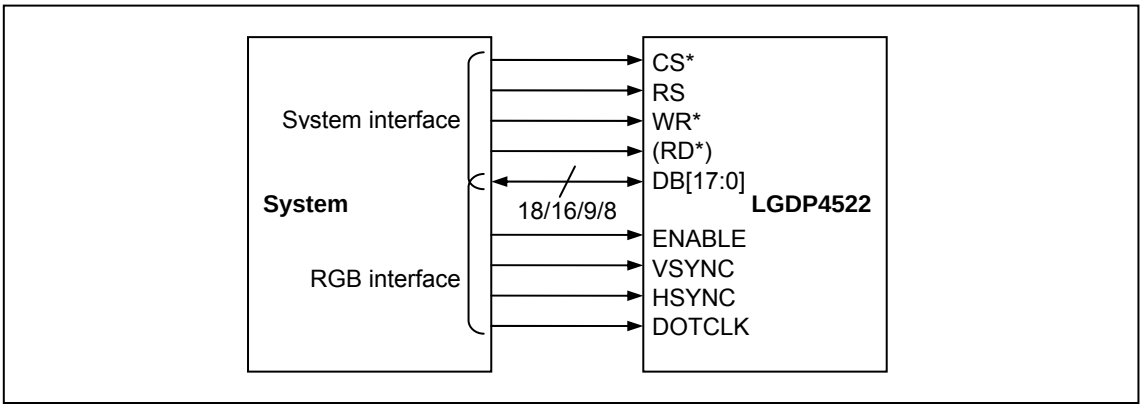


Figure 19: Interfaces between system and LGDP4522

System Interface

The following are the system interfaces available with the LGDP4522. The interface is selected by setting the IM[3:0] pins. The system interface is used for setting instructions and RAM access.

Table 48

IM[3:0]	MPU interface mode	DB pin in use
0000	Setting disabled	-
0001	Setting disabled	-
0010	80-system 16-bit interface	DB[17:10], DB[8:1]
0011	80-system 8-bit interface	DB[17:10]
010*	Serial peripheral interface (SPI)	SDI, SDO
011*	Setting disabled	-
1000	Setting disabled	-
1001	Setting disabled	-
1010	80-system 18-bit interface	DB[17:0]
1011	80-system 9-bit interface	DB[17:9]
11**	Setting disabled	-

80-System 18-Bit Interface

The 80-system 18-bit parallel system interface is selected by setting the IM[3:0] pins to “1010”.

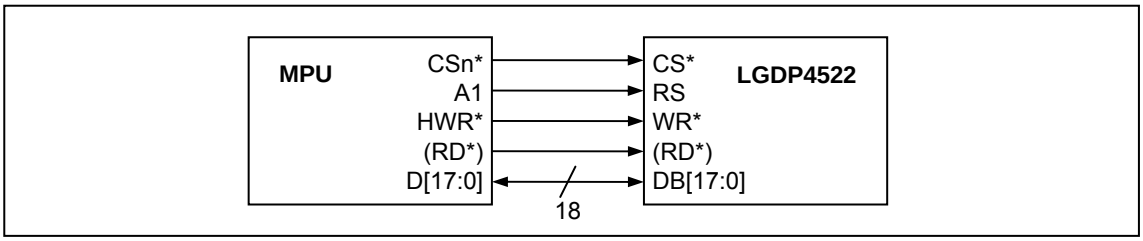


Figure 20: 18-bit microcomputer and LGDP4522

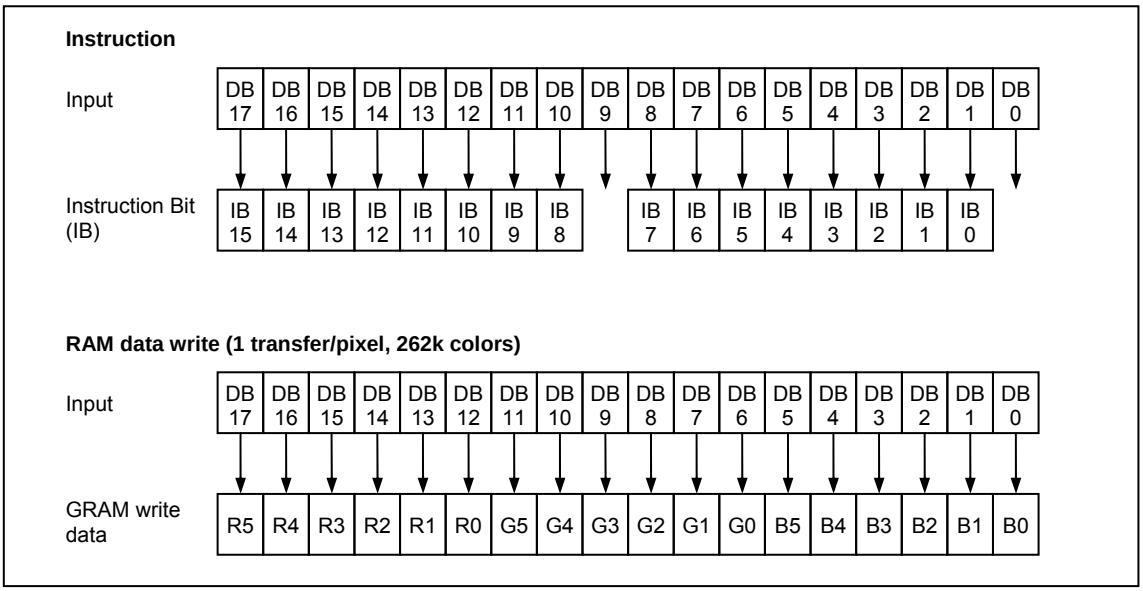


Figure 21: Data format for 18-bit interface

80-System 16-Bit Interface

The 80-system 16-bit parallel system interface is selected by setting the IM[3:0] pins to “0010”.

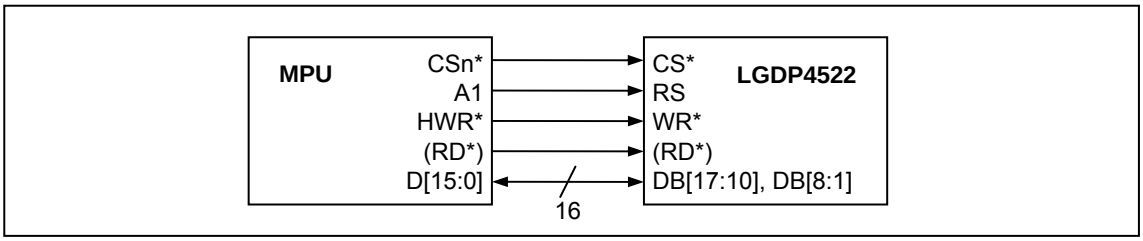


Figure 22: 16-bit microcomputer and LGDP4522

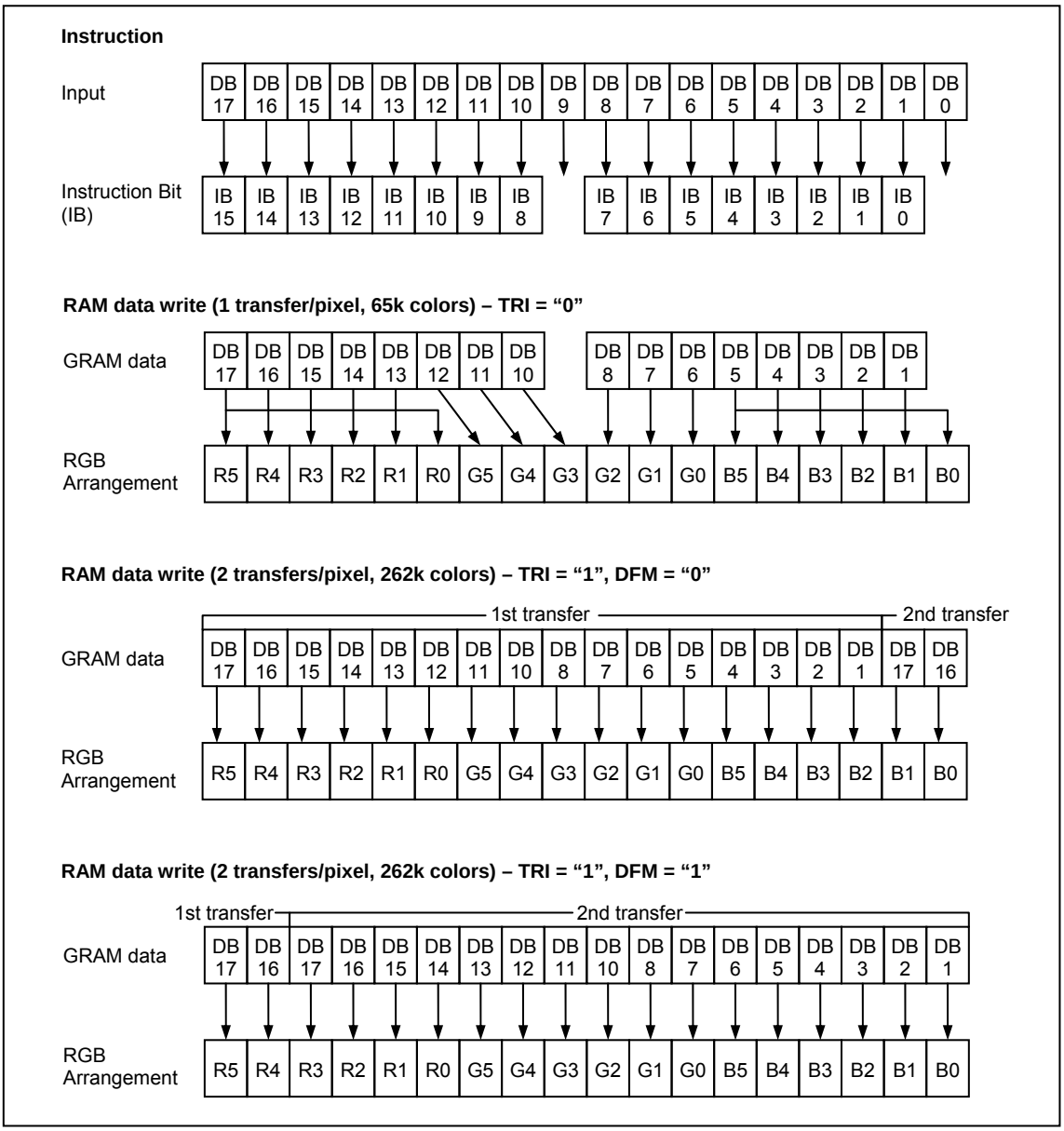


Figure 23: Data format for 16-bit interface

Data Transfer Synchronizing in 16-Bit Bus Interface Mode

The LGDP4522 supports a data transfer synchronization function, which resets the counter to count the numbers of upper 16/2-bit and lower 2/16-bit transfers in 16 bits x 2 transfer mode. When a mismatch occurs in data transfers due to noise and so on, the 000h instruction is written 4 times consecutively to reset the upper and lower counters to restart data transfers from the upper 2/16 bits. The synchronization function, when executed periodically, will prevent the runaway of the display system.

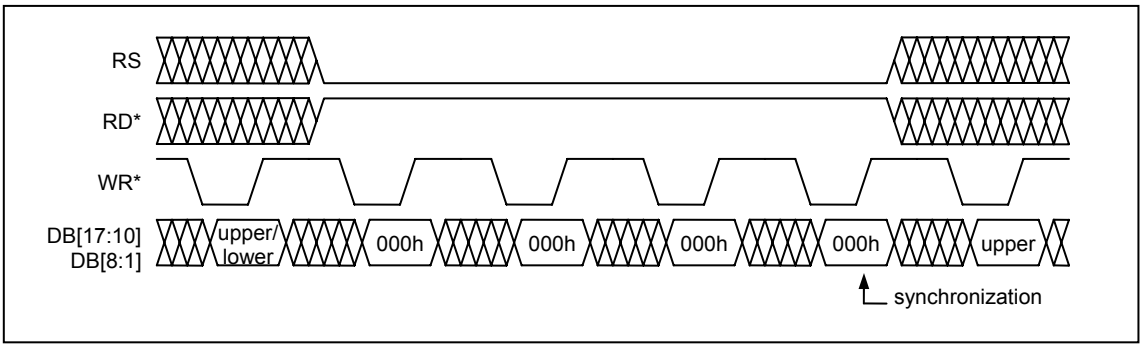


Figure 24: 16-bit data transfer synchronization

80-System 9-Bit Interface

The 80-system 9-bit parallel system interface using the DB17 to DB9 pins is selected by setting the IM[3:0] pins to "1011". When transferring a 16-bit instruction, it is divided into upper and lower 8 bits (the LSB is not used), and the upper 8 bits are transferred first. The RAM write data are also divided into the upper and lower 9 bits, and the upper bits are transferred first. The unused DB[8:0] pins must be fixed at either Vcc or GND level. When writing the index register, the upper byte (8 bits) must be written.

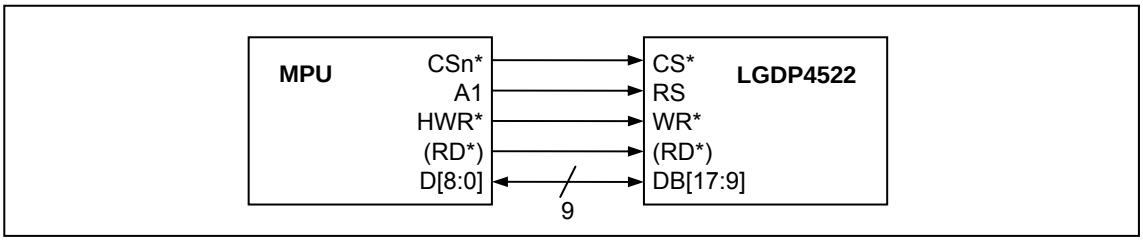


Figure 25: 9-bit microcomputer and LGDP4522

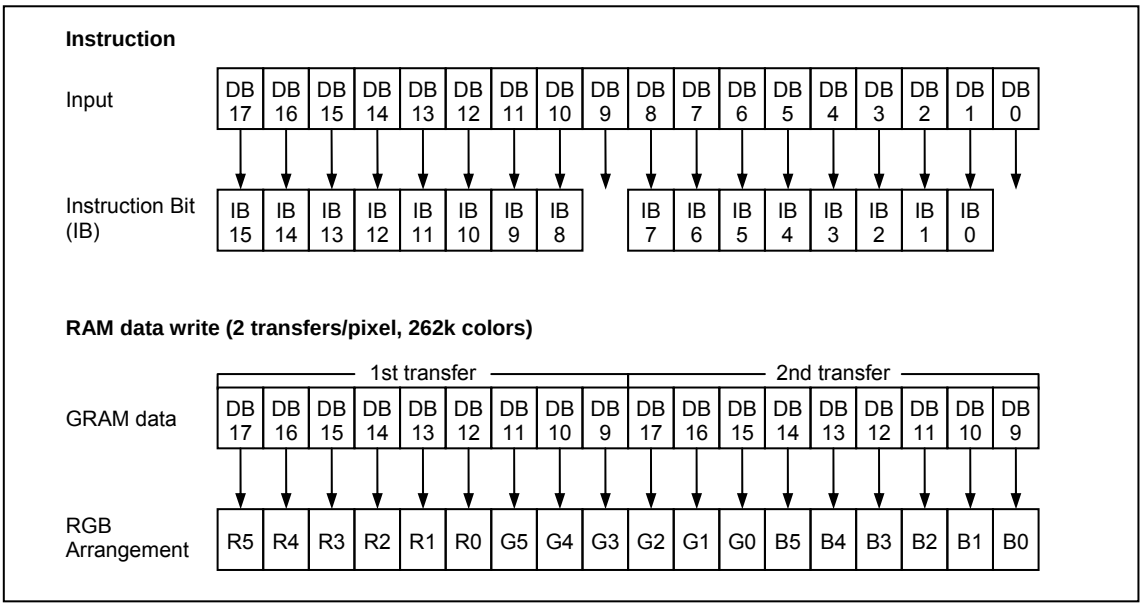


Figure 26: Data format for 9-bit interface

Data Transfer Synchronizing in 9-Bit Bus Interface Mode

The LGDP4522 supports a data transfer synchronization function to reset upper and lower counters counting the number of transfers of upper and lower 9 bits in 9-bit bus interface mode. If a mismatch arises in the numbers of transfers between the upper and lower 9 bit counters due to noise and so on, the 000h instruction is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper 9 bits. This synchronization function, when executed periodically, can effectively prevent runaway of display system.

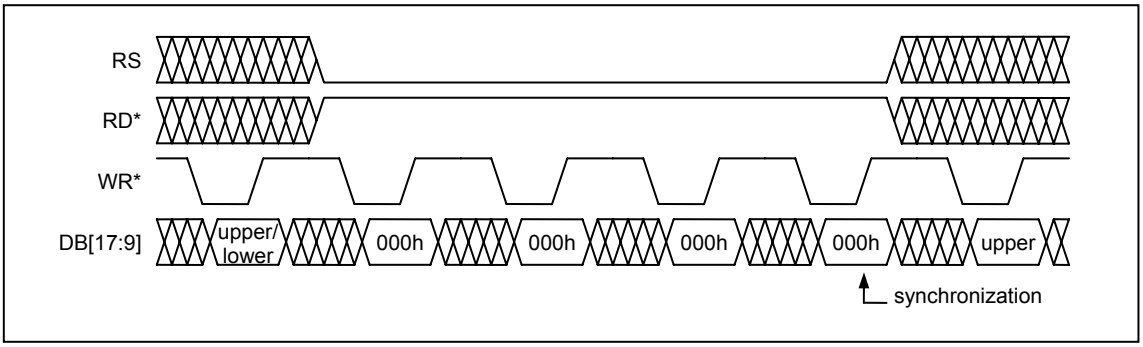


Figure 27: 9-bit data transfer synchronization

80-System 8-Bit Interface

The 80-system 8-bit parallel system interface using the DB17 to DB10 pins is selected by setting the IM[3:0] pins to “0011”. When transferring a 16-bit instruction, it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The RAM data is also divided into the upper and lower 8 bits, and the upper bits are transferred first. The RAM write data are expanded into 18 bits internally (see the figure below). The unused pins DB[9:0] must be fixed at either Vcc or GND level. When writing the index register, the upper byte (8 bits) must be written.

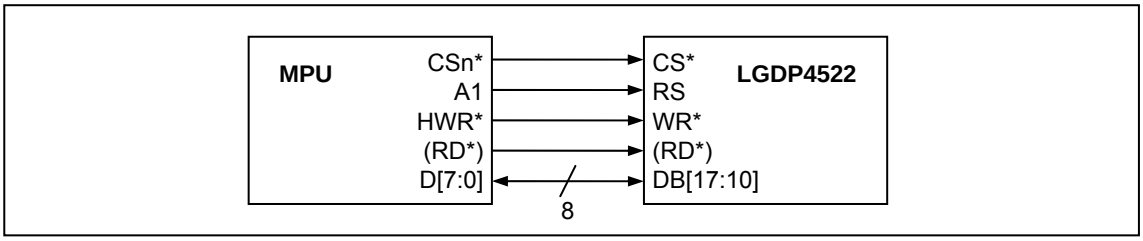


Figure 28: 8-bit microcomputer and LGDP4522

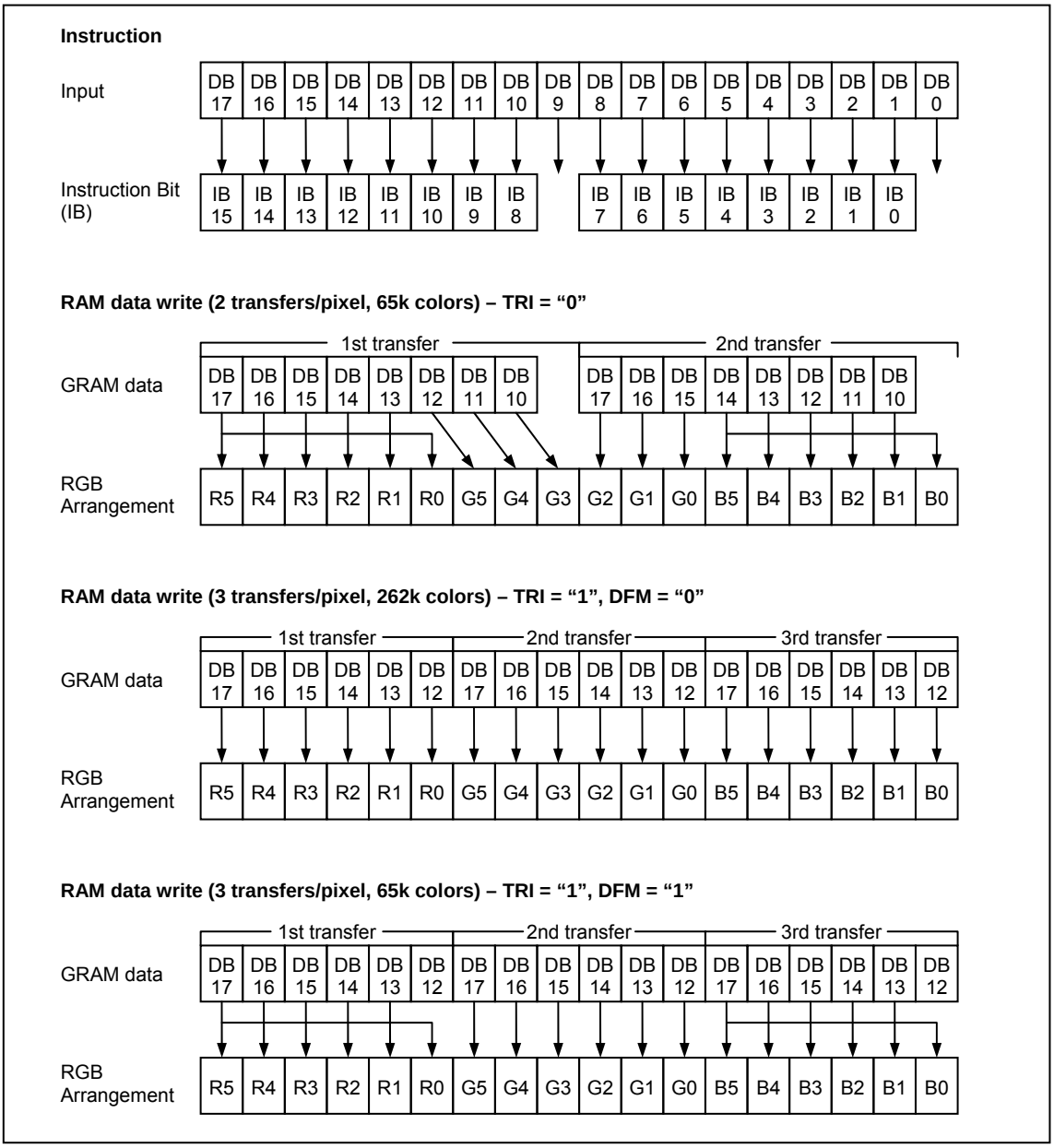


Figure 29: Data format for 8-bit interface

Data Transfer Synchronization in 8-Bit Bus Interface Mode

The LGDP4522 supports a data transfer synchronization function to reset upper and lower counters counting the number of transfers of upper and lower 8 bits in 8-bit bus interface mode. If a mismatch arises in the numbers of transfers between the upper and lower 8 bit counters due to noise and so on, the 00h instruction is written 4 times consecutively to reset the upper and lower counters so that data transfer will restart with a transfer of upper 8 bits. This synchronization function, when executed periodically, can effectively prevent runaway of display system.

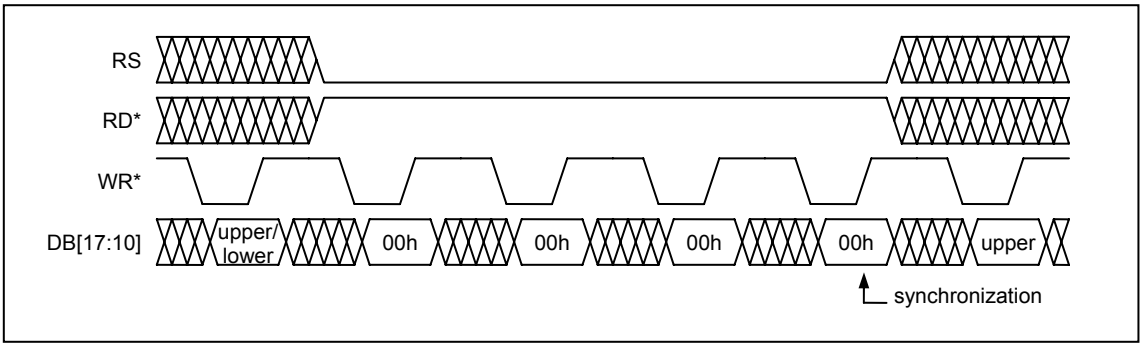


Figure 30: 8-bit data transfer synchronization

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:1] pins to “010”. The SPI is available via the chip select line (CS*), the serial transfer clock line (SCL), the serial data input (SDI), and the serial data output (SDO). In SPI mode, the IM0/ID pin functions as the ID pin and the DB[17:0] pins, which are not used, must be fixed at either IOVcc or GND level.

The LGDP4522 recognizes the start of data transfer on the falling edge of CS* input and transfers the start byte. It recognizes the end of data transfer on the rising edge of CS* input. The LGDP4522 is selected when the 6-bit chip address in the start byte transferred from the transmission unit and the 6-bit device identification code assigned to the LGDP4522 correspond as a result of comparison. When selected, the LGDP4522 starts taking subsequent data. The ID pin sets the least significant bit of the identification code. Send “01110” to the identification code, which is the five upper bits of the start byte. Two different chip addresses must be assigned to the LGDP4522 because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = “0”, either index register write operation or status read operation is executed. When RS = “1”, either instruction write operation or RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). Data are received when the R/W bit is “0”, and are transferred when the R/W bit is “1”.

After receiving the start byte, the LGDP4522 starts transferring or receiving data in units of bytes. Data transfer is executed from the MSB. All instructions of the LGDP4522 take a 16-bit format and are executed internally after transferring two bytes (DB[15:0]) from the MSB. GRAM write data are internally expanded into 18 bits. After receiving the start byte, the LGDP4522 takes the first and the second byte as the upper and the lower eight bits of a 16-bit instruction, respectively.

In SPI mode, invalid data are sent to the data bus until 4-byte data are read out from the internal GRAM after the start byte. Valid data are read out as the LGDP4522 reads out the 5th byte data from the internal GRAM.

Table 49: Start byte format

Transferred bits	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Device ID code						RS	R/W
	0	1	1	1	0	ID		

Note: ID bit is selected by setting the IM0/ID pin.

Table 50

RS	**R/W**	**Function**
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data

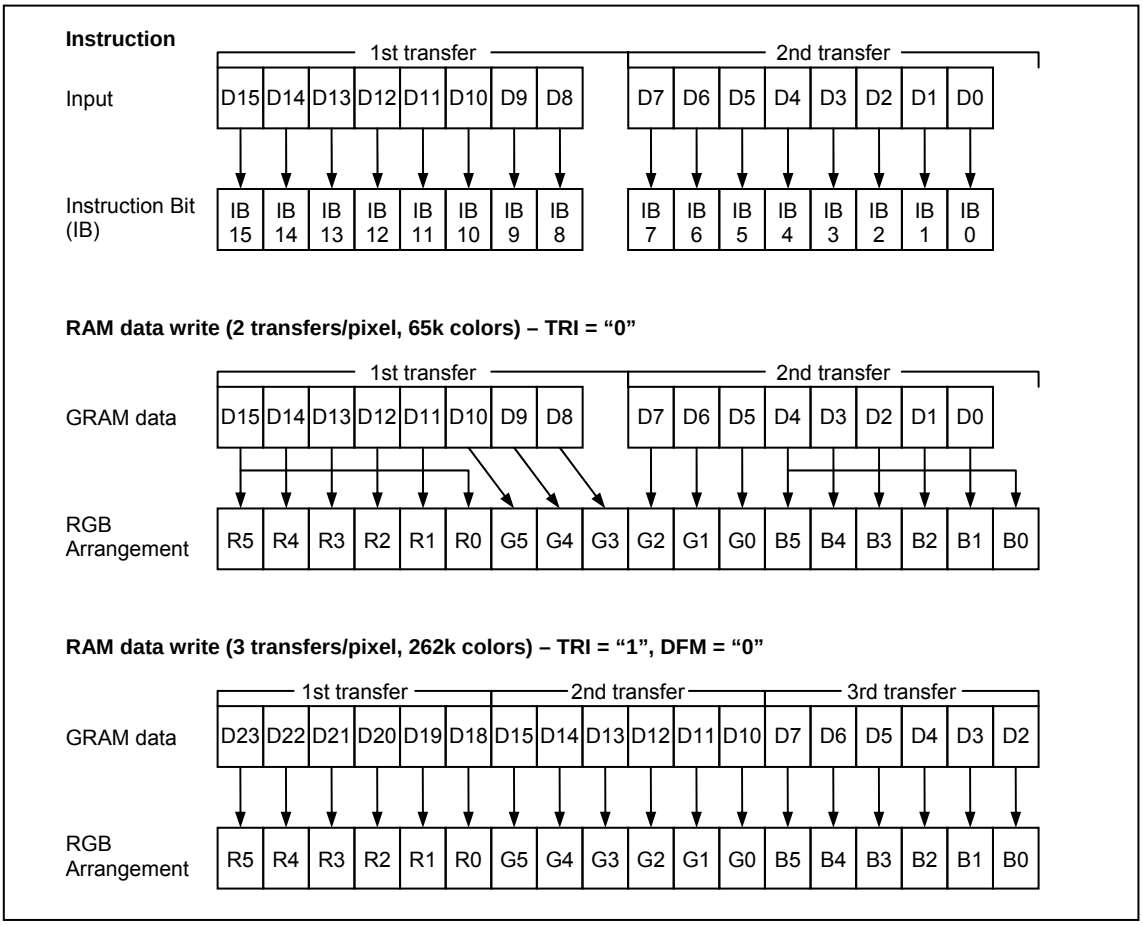


Figure 31: Data format for SPI

VSYNC Interface

The LGDP4522 has the VSYNC interface, which enables moving picture display with the system interface in synchronization with the frame-synchronizing signal (VSYNC). The VSYNC interface enables the system interface to display a moving picture with minimum modification.

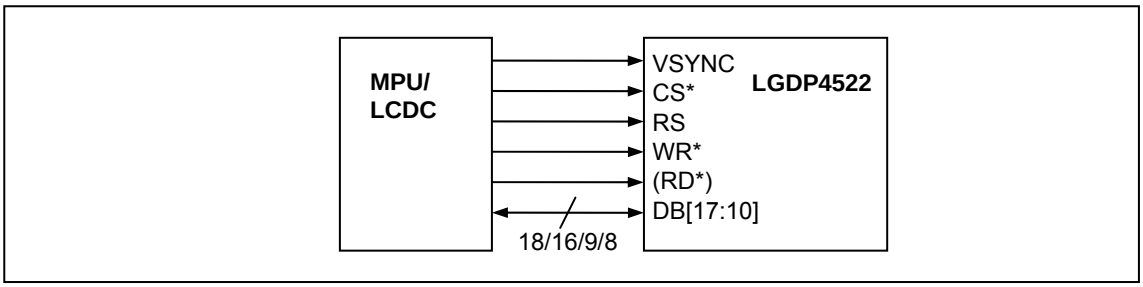


Figure 32: VSYNC interface

The VSYNC interface is selected by setting DM1-0 = "10" and RM = "0". In VSYNC interface mode, the internal display operation is synchronized with the VSYNC signal. By writing data to the internal RAM via the system interface at a speed faster to a certain degree than that of internal display operation, the VSYNC interface enables moving picture display with the system interface and screen rewriting operation without flicker.

The display operation in VSYNC mode is executed in synchronization with the internal clock generated from internal oscillators and VSYNC input. All display data are stored in the internal RAM to limit the data to be transferred to those overwritten on the moving picture RAM area and minimize total data transfer required for moving picture display.

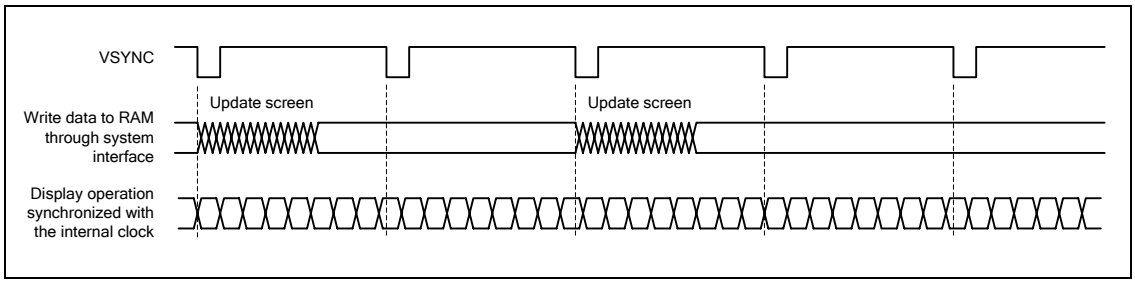


Figure 33: Moving picture data transfer via VSYNC interface

The VSYNC interface has the minimum speed of writing data to the internal RAM via the system interface and the minimum internal clock frequency, which are calculated from the following formulae.

Internal clock frequency (fosc)

$$= FrameFrequency \times (DisplayLines\ (NL) + FrontPorch\ (FP) + BackPorch\ (BP)) \times 16\ clocks \times variance$$

$$RAMWriteSpeed > \frac{176 \times DisplayLines\ (NL)}{(BackPorch\ (BP) + DisplayLines\ (NL) - margins) \times 16\ clocks \times \frac{1}{fosc}}$$

Note: When the RAM write operation does not start on the falling edge of VSYNC, the time from the falling edge of VSYNC until the start of RAM write operation must also be taken into account.

An example of minimum RAM writing speed and internal clock frequency in VSYNC interface mode is as follows.

[Example]	
Display size	176 RGB × 220 lines
Lines	220 lines (NL = 11001)

Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	60 Hz

Internal clock frequency (fosc)
= 60 Hz × (220 + 2 + 14) lines × 44 Clocks × 1.1 / 0.9 = 760 kHz

When setting the internal clock frequency, possible causes of variances must also be taken into consideration. In this example, the calculated internal clock frequency with the above register setting allows for a margin of ±10% for variances and ensures to complete the display operation within one VSYNC cycle.

In this example, variances attributed to the fabrication process of LSI and room temperature are counted in. Other possible causes of variances, such as differences in external resistors or voltage changes are not in consideration. It is necessary to allow for an enough margin if these factors must be incorporated.

Minimum speed for RAM writing
> 176 × 220 / {((14 + 220 - 2) lines × 44 clock) / 760 kHz} = 2.88 MHz

The above theoretical value is calculated on the premise that the LGDP4522 starts writing data to the internal RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical display line where display operation is performed and the RAM line address where data write operation is performed.

The RAM write speed of 2.88MHz or more on the falling edge of VSYNC will guarantee the completion of RAM write operation before the LGDP4522 starts displaying the RAM data on the screen, enabling rewriting the entire screen without flicker.

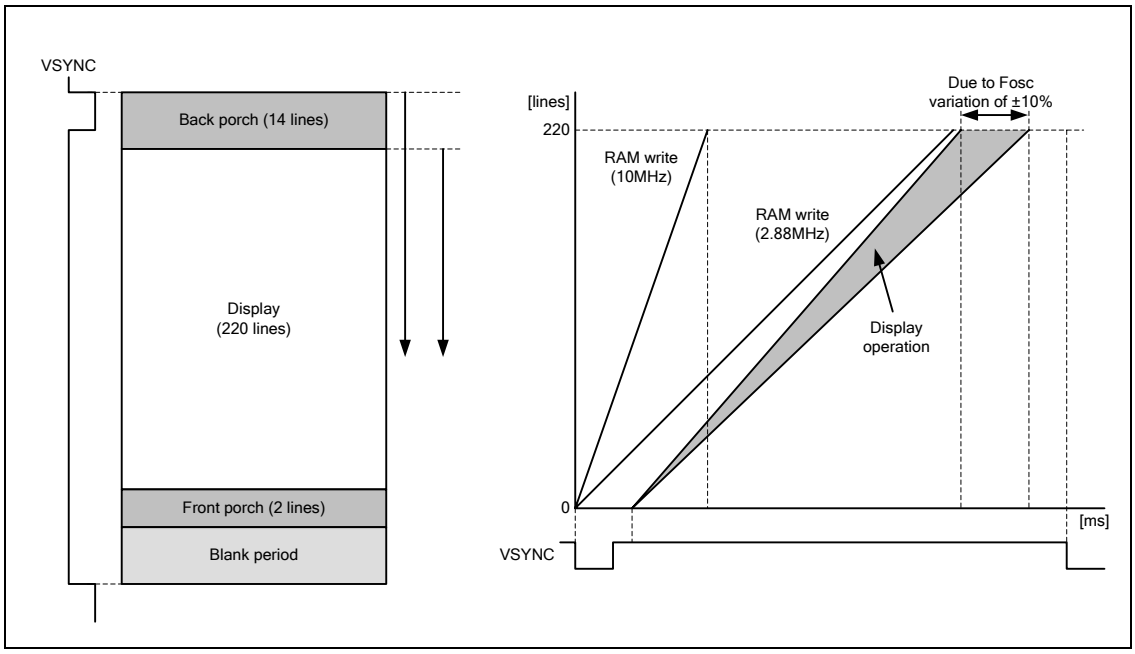


Figure 34: Write/display operation timing via VSYNC interface

Notes in Using the VSYNC Interface

1. The above example of calculation gives a theoretical value. In the actual setting, other possible causes of variances not counted in the above example such as differences in internal oscillators should also be taken into consideration. It is strongly recommended to allow for an enough margin in setting a RAM writing speed.

2. The above example of calculation gives a minimum value in case of rewriting the entire screen. If the moving picture display area is smaller than that, the range for setting a minimum RAM writing speed can have extra margins.
3. After drawing 1 frame, a front porch period continues until the next input of VSYNC is detected.
4. When switching from the internal clock operation mode (DM[1:0] = “00”) to the VSYNC interface mode, or the other way around, it is enabled from the next VSYNC cycle, i.e. after completing the display of the frame, which the LGDP4522 was internally processing when switching the modes.
5. The partial display, vertical scroll, and interlaced scan functions are not available in VSYNC interface mode.
6. In VSYNC interface mode, set the AM bit to “0” to transfer display data in the method mentioned above.

External Display Interface

The following are the external display interface (RGB interface) available with the LGDP4522. The interface is selected by setting the RIM1-0 bits as follows. The RGB interface is used to access RAM.

Table 51

RIM[1:0]	RGB interface	DB pins
00	18-bit RGB interface	DB[17:0]
01	16-bit RGB interface	DB[17:10], DB[8:1]
10	6-bit RGB interface	DB[17:12]
11	Setting disabled	

Note: Multiple RGB interfaces cannot be used simultaneously.

RGB Interface

The display operation via the RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. The RGB interface enables transferring minimum necessary data and rewriting the RAM area need to be overwritten with use of window address function. In RGB interface mode, it is necessary to set back and front porch periods before and after a display period, respectively.

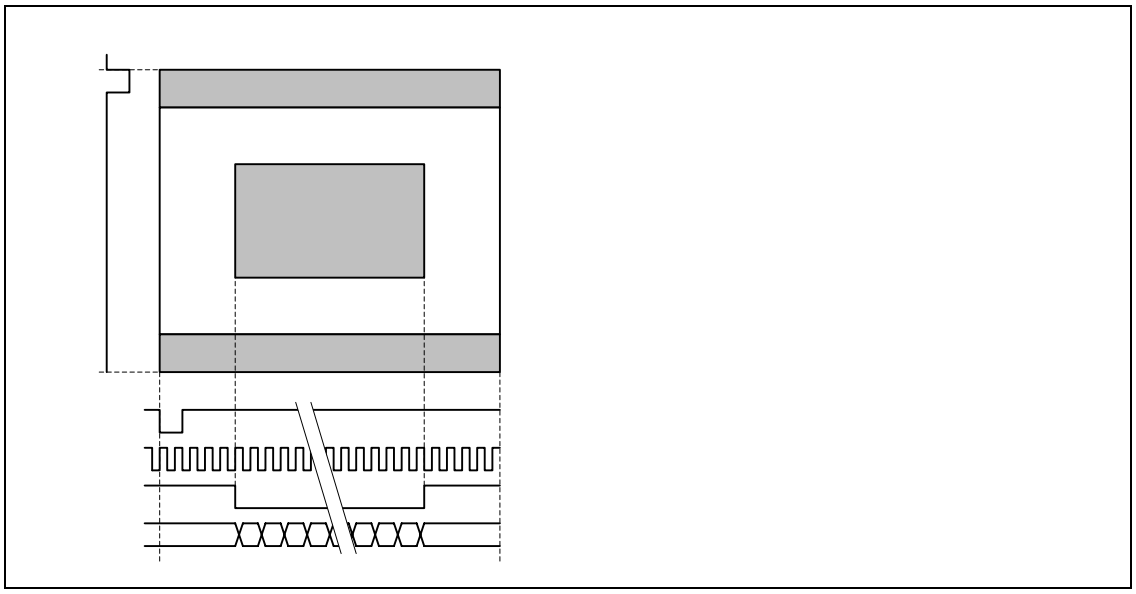


Figure 35: RGB interface

ENABLE Signal

The combinations of EPL and ENABLE bits and the functions are as follows. Note that it is necessary to set both EPL and ENABLE bits to automatically update RAM address in the AC when writing data to the internal RAM. The EPL bit inverts the polarity of ENABLE signal.

Table 52

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

RGB Interface Timing

The timing chart of signals in 16/18-bit RGB interface mode is as follows.

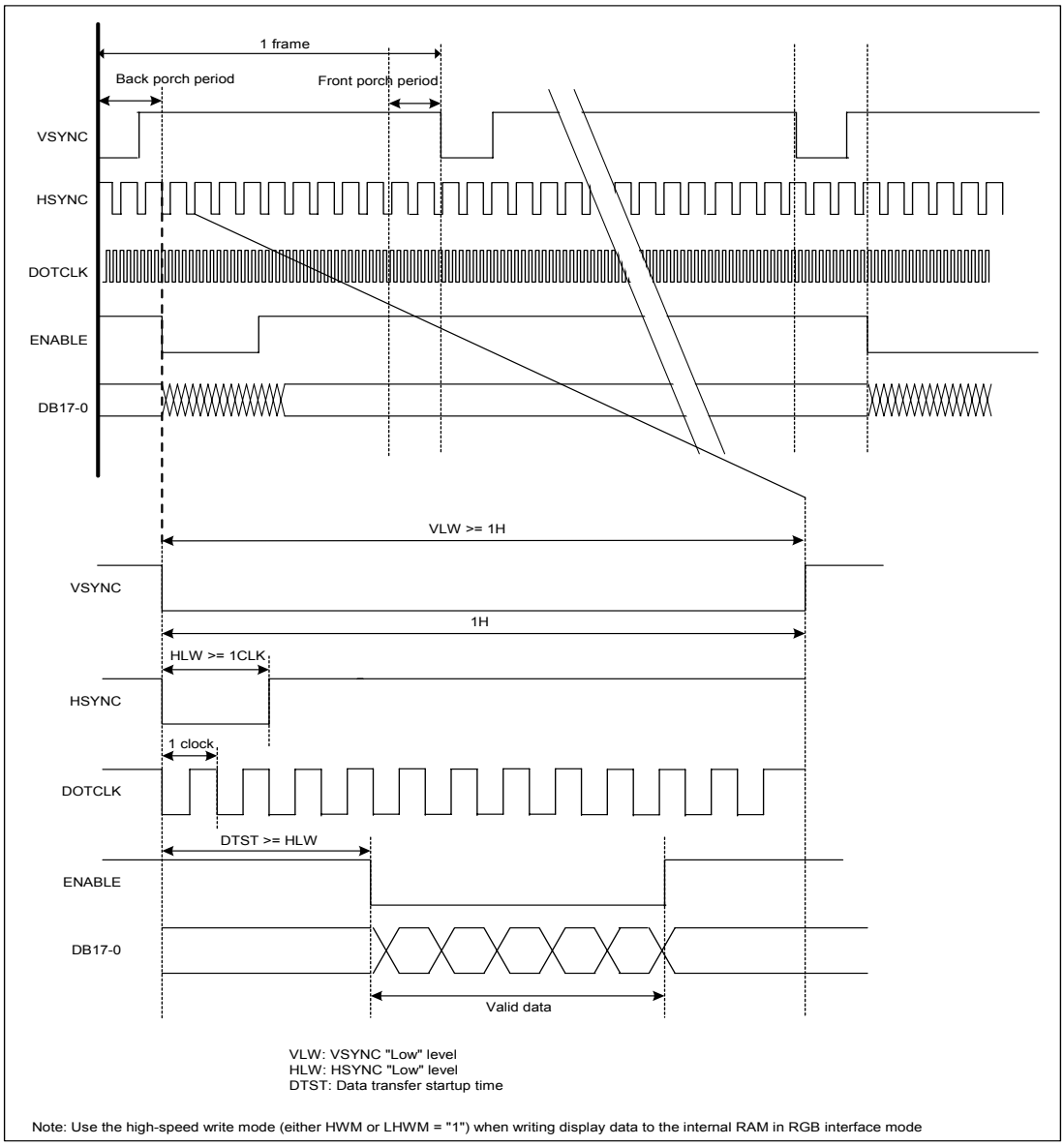


Figure 36: 16-/18-bit RGB Interface Timing

The timing chart of signals in 6-bit RGB interface mode is as follows.

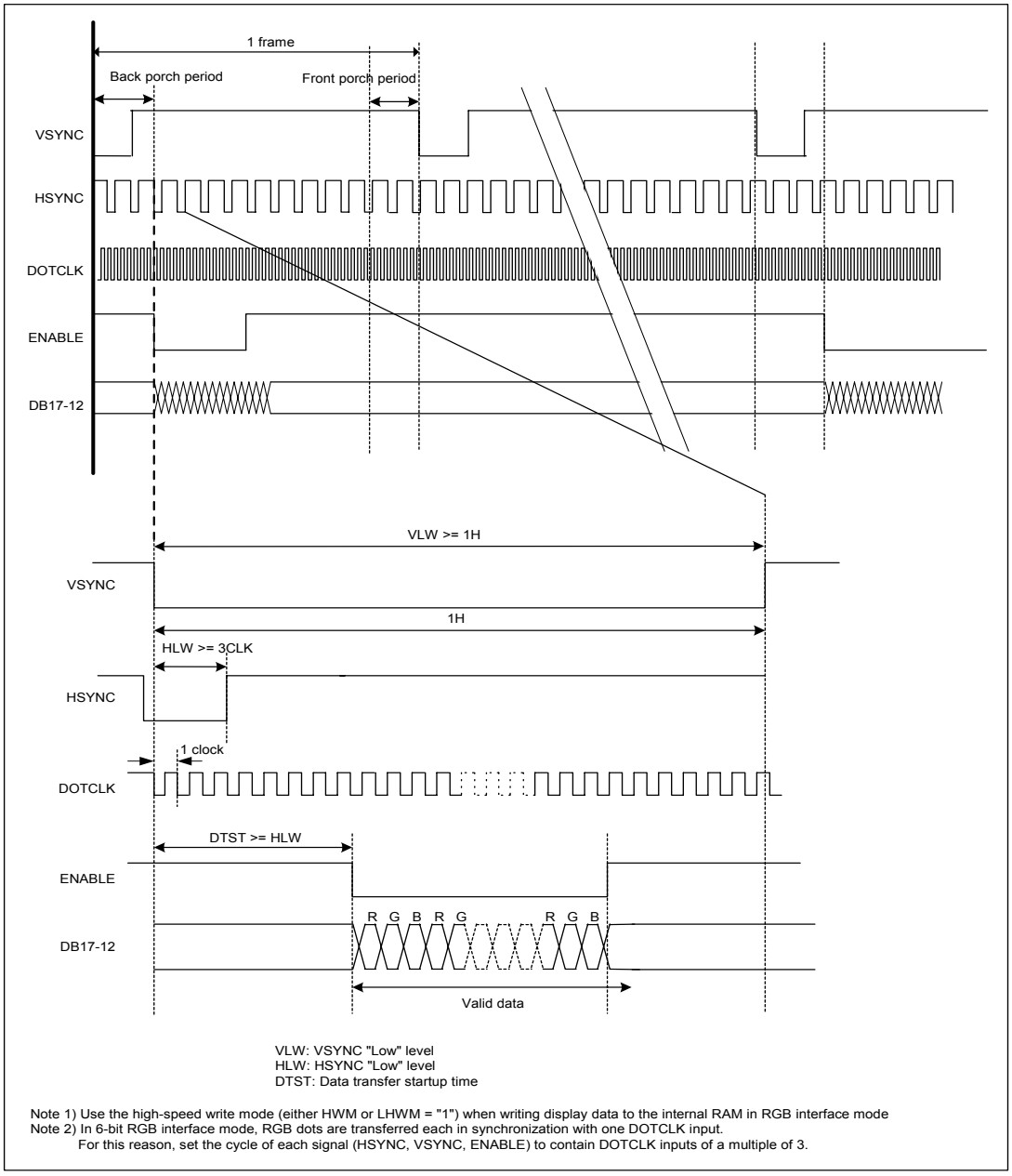


Figure 37: 6-bit RGB Interface Timing

Moving Picture Display

The LGDP4522 has the RGB interface for moving picture display and incorporates RAM for storing moving picture data, which has following merits in displaying a moving picture.

- The window address function enables transferring minimum necessary data to be written on the moving picture RAM area.
- Data are transferred only to the moving picture RAM area.
- The reduction in data transfer contributes to the reduction in power consumption by the entire system.
- Allowing the use of system interface to rewrite data, such as icons, in still picture RAM area while displaying a moving picture.

RAM Access via a System Interface in RGB-I/F Mode

The LGDP4522 allows RAM access via the system interface in RGB interface mode. In RGB interface mode, data are written to the internal RAM in synchronization with DOTCLK while ENABLE is “Low”. When writing data to the internal RAM via the system interface, set ENABLE high” to stop writing data via the RGB interface. Then set RM = “0” to make RAM accessible via the system interface. When restarting RAM access in RGB interface mode, wait a time for one read/write bus cycle. Then, set RM = “1” and the index register to R22h to start accessing RAM via the RGB interface. If RAM accesses via two interfaces conflicts, there is no guarantee that data are written to the internal RAM.

The following figure illustrates the operation of the LGDP4522 when displaying a moving picture via the RGB interface and rewriting data in the still picture RAM area via the system interface.

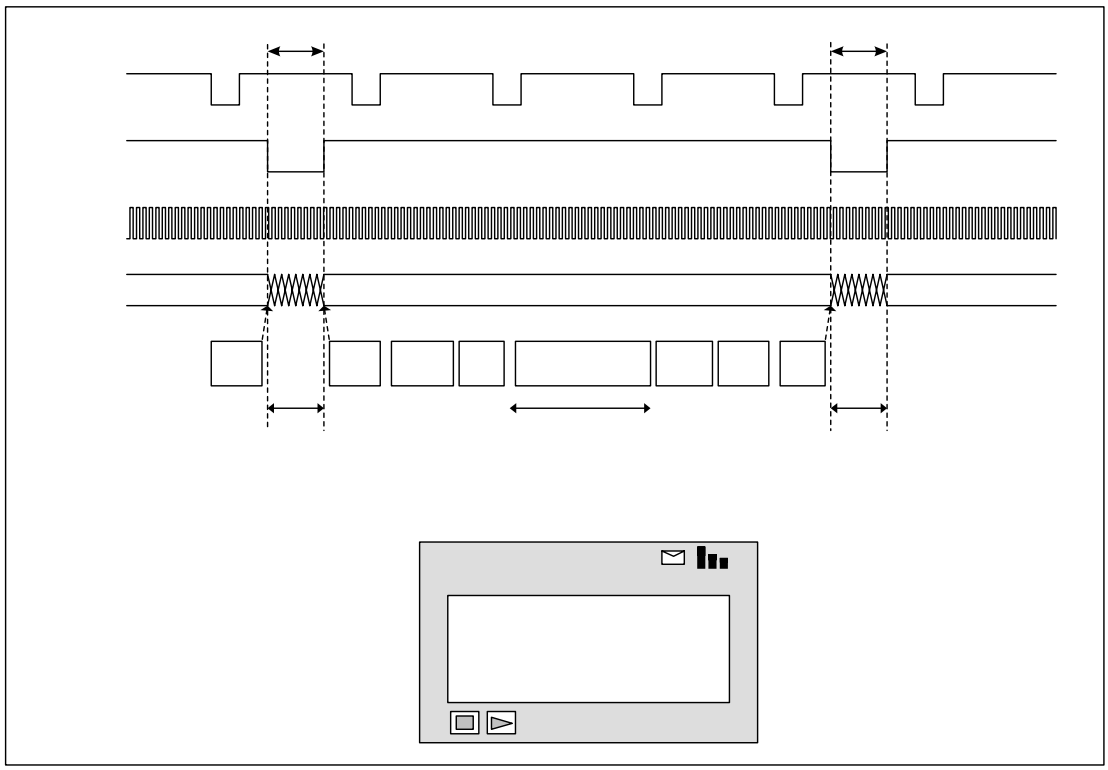


Figure 38

6-Bit RGB Interface

The 6-bit RGB interface is selected by setting the RIM[1:0] bits to “10”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal

RAM in synchronization with the display operation via 6-bit RGB data bus (DB[17:12]) according to the data enable signal (ENABLE). Unused pins (DB[11:0]) must be fixed at either IOVcc or GND level.

Instructions are set only via the system interface.

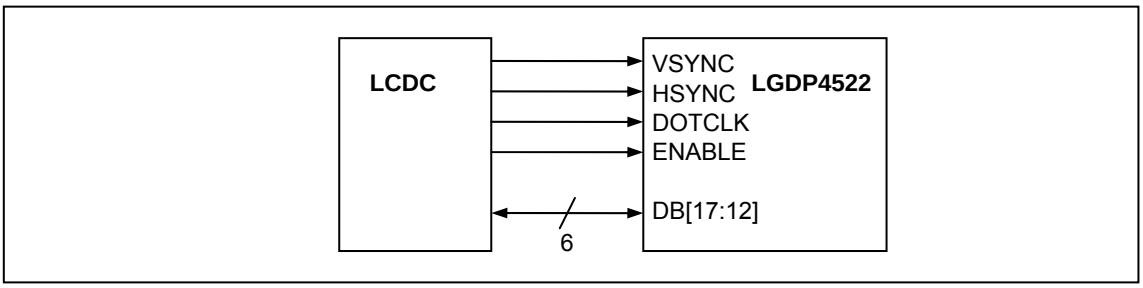


Figure 39: 6-bit RGB interface

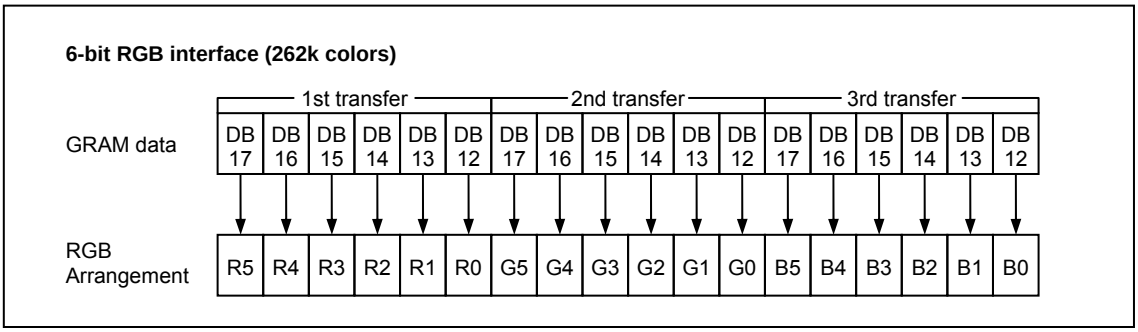


Figure 40: Data format for 6-bit interface

Data Transfer Synchronization in 6-Bit RGB Interface Mode

The LGDP4522 has data transfer counters for counting the first, second, third data transfers in 6-bit RBG interface mode. The transfer counters are always reset to the state of first data transfer on the falling edge of VSYNC. If a mismatch arises in the number of each data transfer, the counters are reset to the state of first data transfer at the start of the frame (i.e. on the falling edge of VSYNC) to restart data transfer in the correct order from the next frame. This function is expedient for moving picture display, which requires consecutive data transfer in light of minimizing effects from failed data transfer and enabling the system to return to a normal state.

Note that internal display operation is performed in units of pixels (RGB: taking 3 inputs of DOTCLK). Accordingly, the number of DOTCLK inputs in one frame period must be a multiple of 3 to complete data transfer correctly. Otherwise it will affect the display of that frame as well as the next frame.

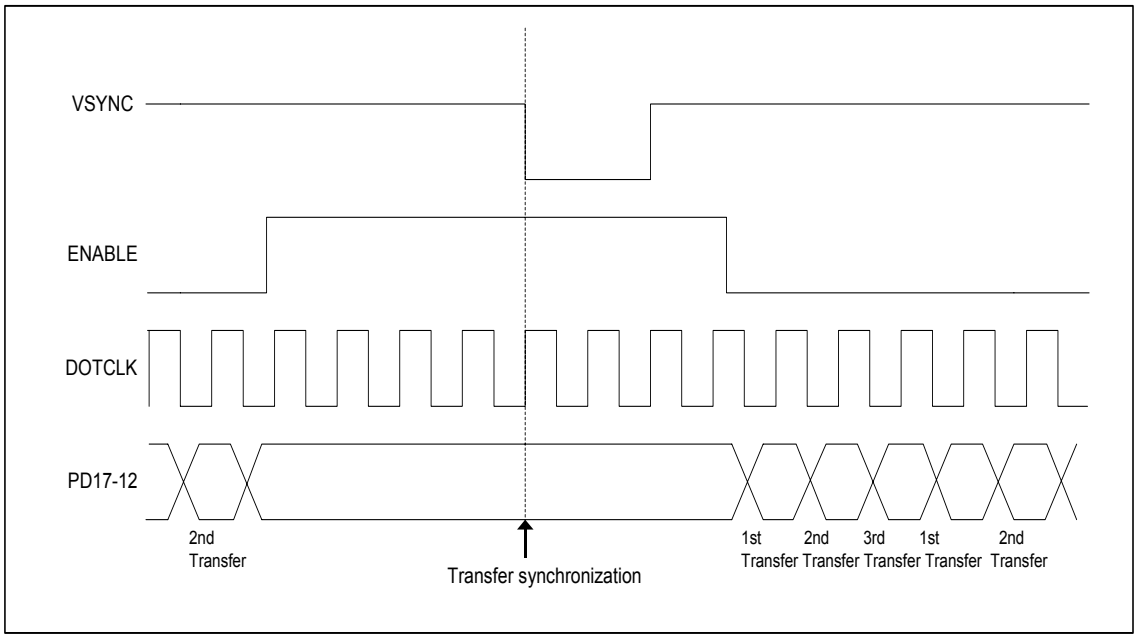


Figure 41: 6-bit data transmission synchronization

16-Bit RGB Interface

The 16-bit RGB interface is selected by setting the RIM1-0 bits to “01”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 16-bit RGB data bus (DB17-10, DB8-1) according to the data enable signal (ENABLE).

Instructions are set only via the system interface.

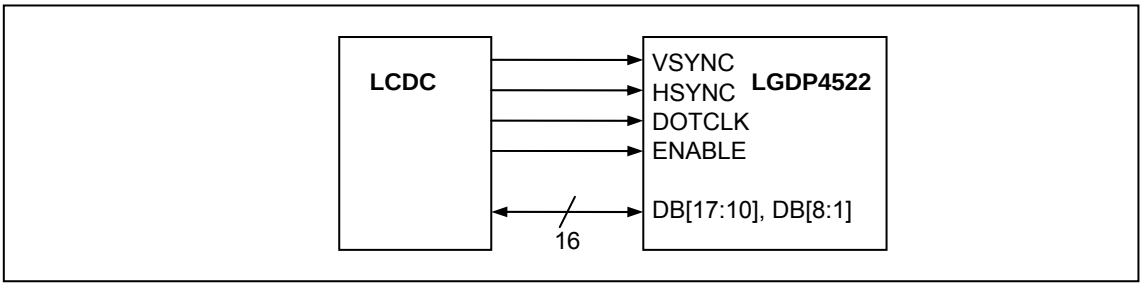


Figure 42: 16-bit RGB interface

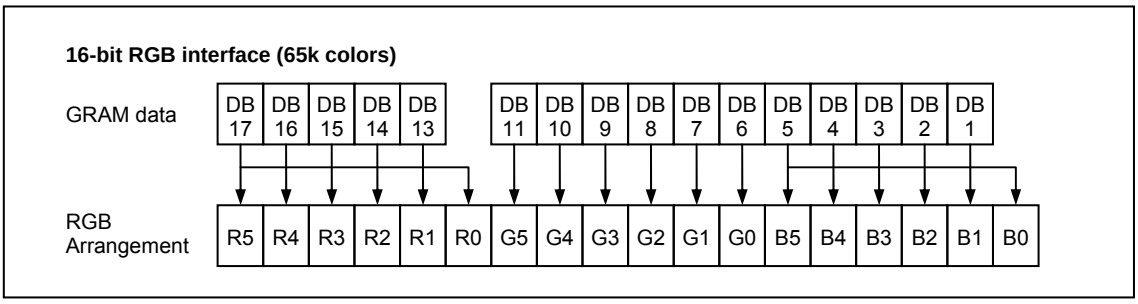


Figure 43: Data format for 16-bit interface

18-Bit RGB Interface

The 18-bit RGB interface is selected by setting the RIM1-0 bits to “00”. The display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation via 18-bit RGB data bus (DB[17:0]) according to the data enable signal (ENABLE).

Instructions are set only via the system interface.

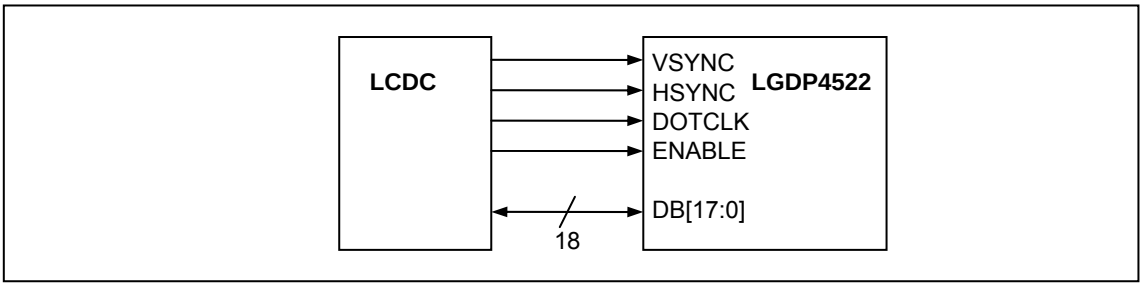


Figure 44: 18-bit RGB interface

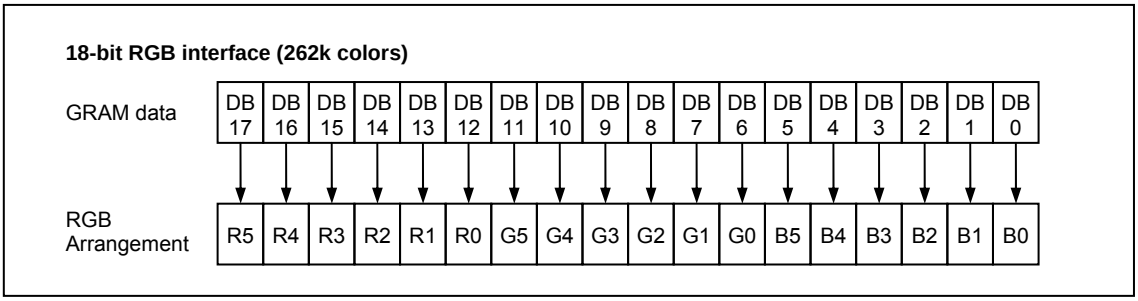


Figure 45: Data format for 18-bit interface

Notes in Using the External Display Interface

1. The following are the functions not available in external display interface mode.

Table 53

Function	External display interface	Internal display operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. VSYNC, HSYNC, and DOTCLK signals must be supplied throughout a display operation period.
3. The periods set with the NO1-0 bits (gate output non-overlap period), STD1-0 bits (source output delay period) and EQ1-0 bits (equalization period) are not based on the internal clock but based on DOTCLK in RGB interface mode.
4. In 6-bit RGB interface mode, each of RGB dots is transferred in synchronization with a DOTCLK input. In other words, it takes 3 DOTCLK inputs to transfer one pixel. Be sure to complete data transfer in units of 3 DOTCLK inputs in 6-bit RGB interface mode.
5. In 6-bit RGB interface mode, data of one pixel, which consists of RGB dots, are transferred in units of 3 DOTCLK. Accordingly, set the cycle of each signal in 6-bit interface mode (VSYNC, HSYNC ENABLE, DB[17:0]) to contain DOTCLK inputs of a multiple of 3 to complete data transfer in units of pixels.
6. When switching from the internal operation mode to the external display interface mode, or the other way around, follow the sequence below.
7. In RGB interface mode, the front porch period continues until the next VSYNC input is detected after drawing one frame.
8. In RGB interface mode, a RAM address (AD15-0) is set in the address counter every frame on the falling edge of VSYNC.

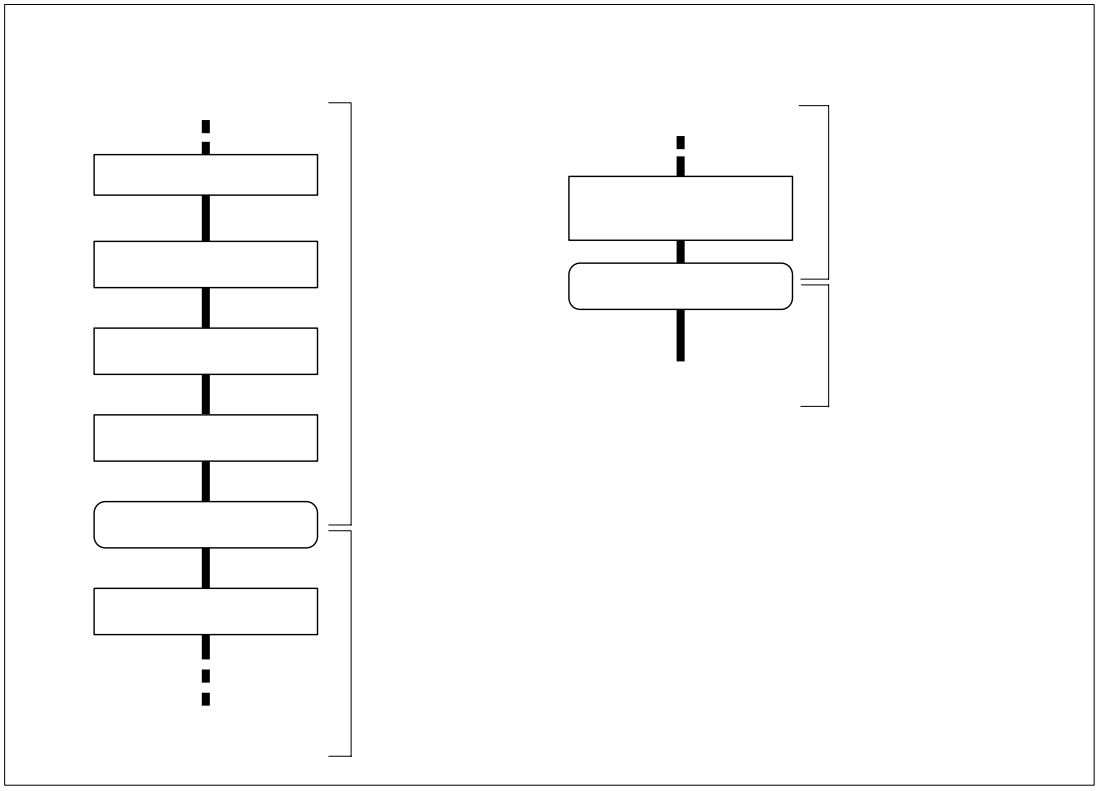


Figure 46: Internal clock operation/RGB interface mode switching sequence

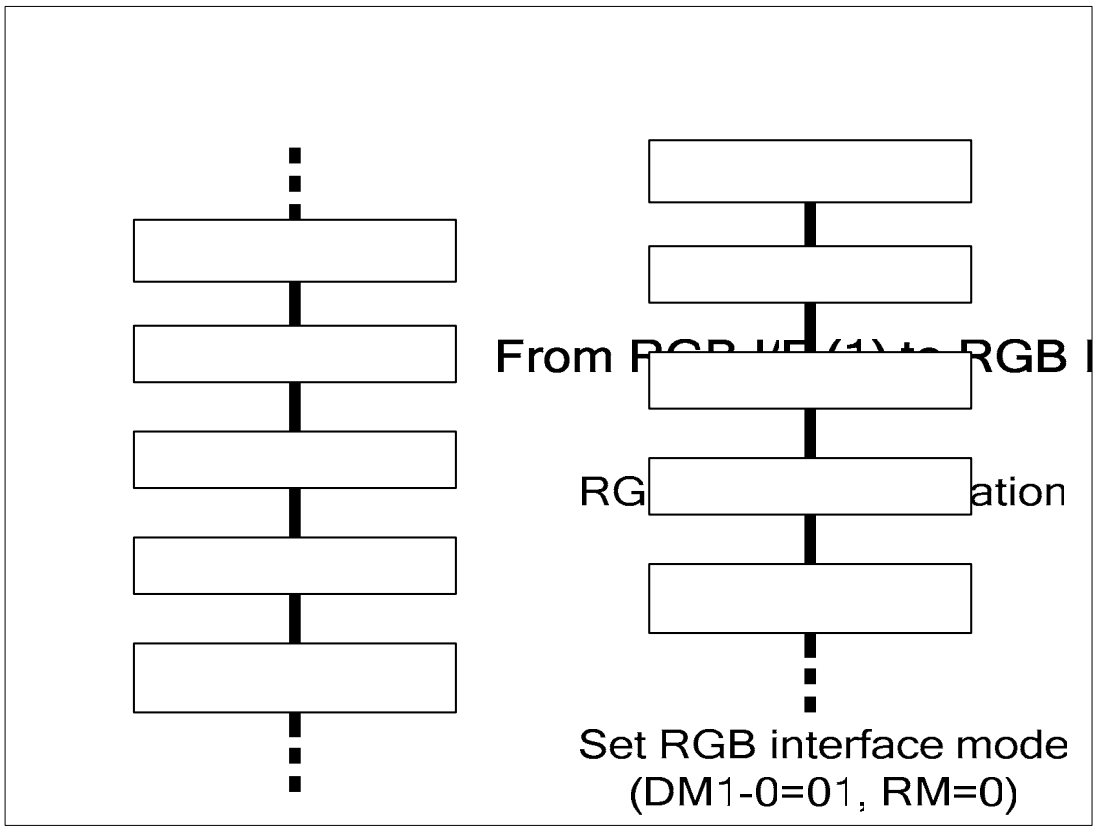


Figure 47: Switching RAM access modes (between system interface and RGB interface modes)

AM = "0"

Set AD15-0

Set IR to R22h
(RAM Data Write)

Write data to RAM
through system interface

Interfacing Timing with LCD Panel

The following are diagrams of interfacing timing with LCD panel control signals in internal operation and RGB interface modes.

RGB I/F Mode

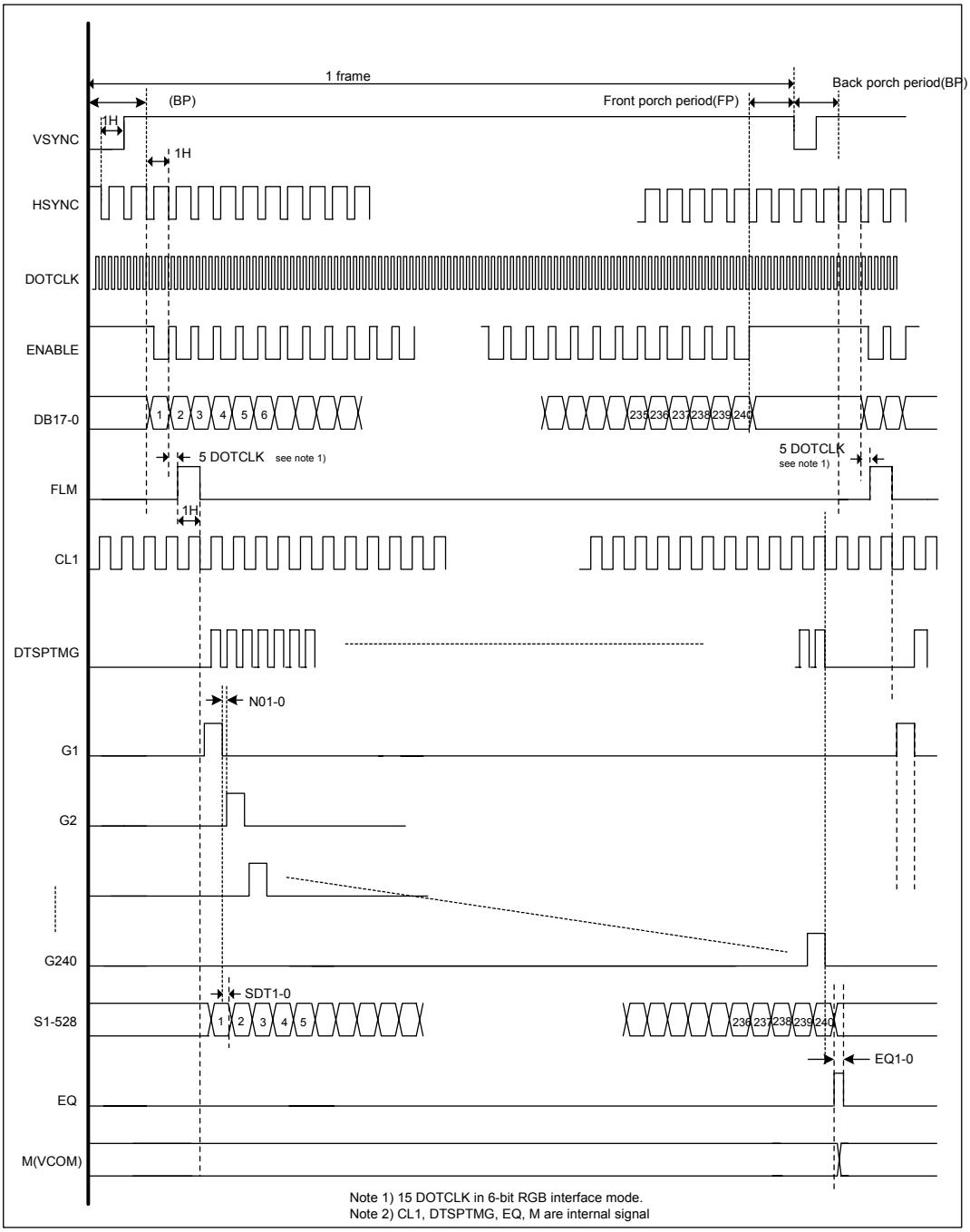


Figure 48

Internal Clock Operation Mode

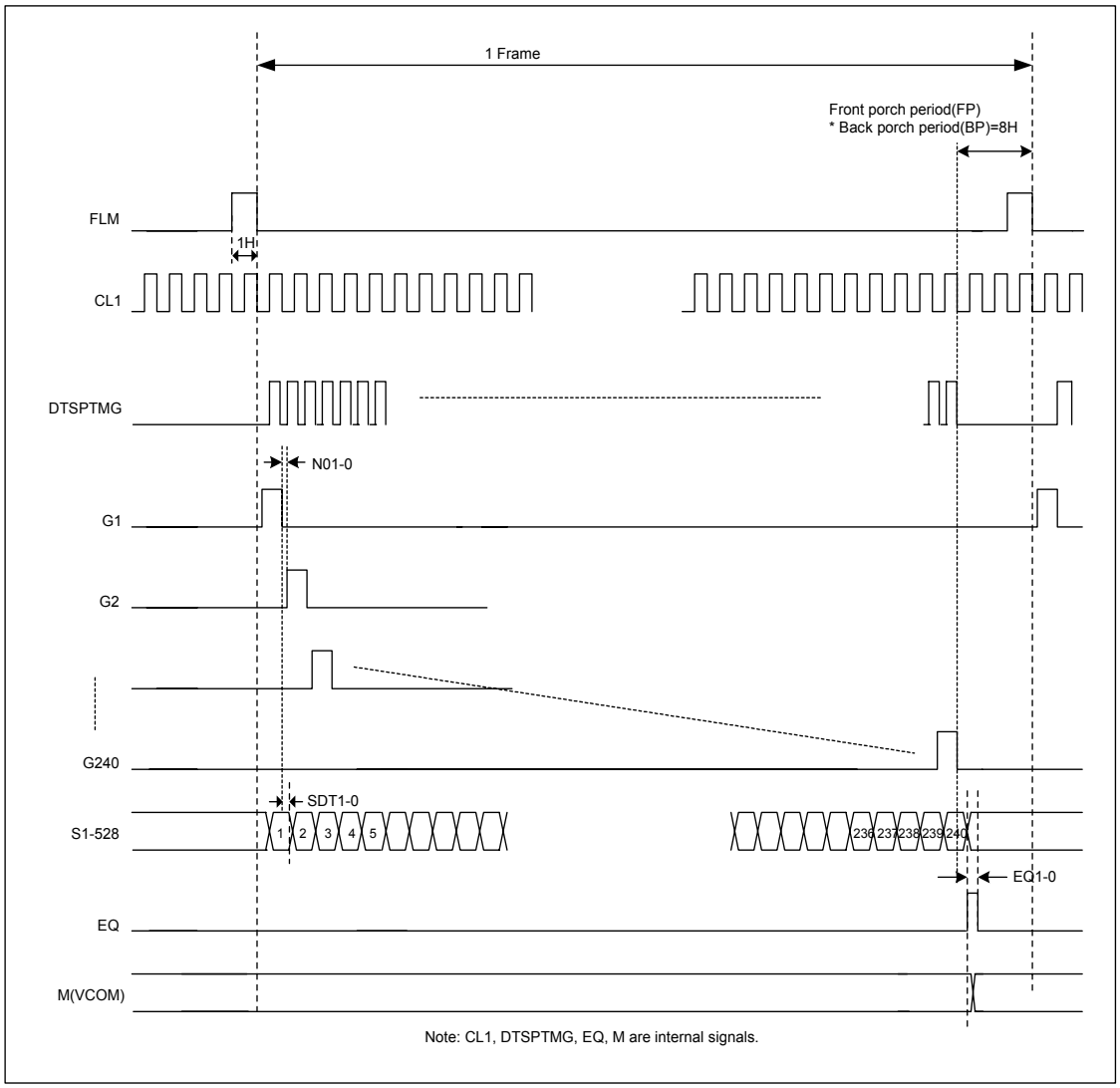


Figure 49

Scan Mode Setting

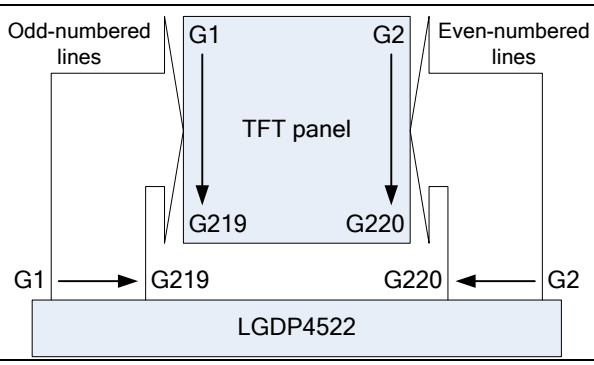
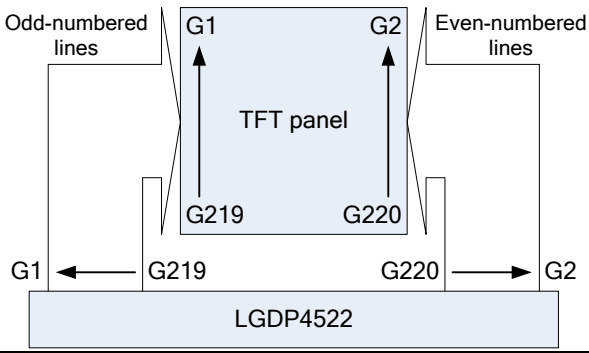
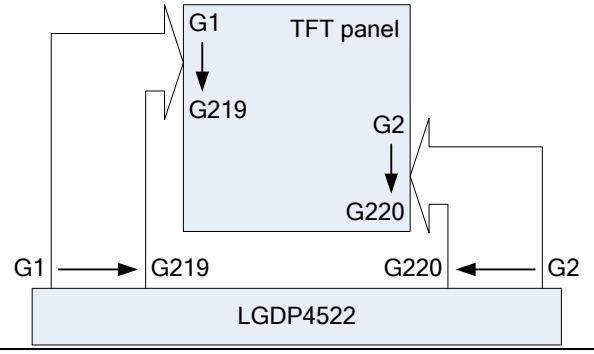
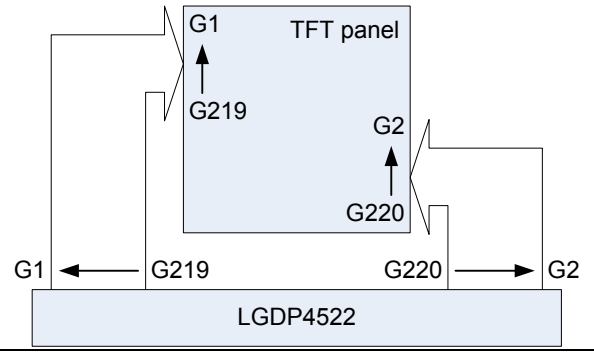
SM	GS	Scan direction	
0	0		G1, G2, G3, G4, …, G218, G219, G220
0	1		G220, G219, G218, …, G4, G3, G2, G1
1	0		G1, G3, G5, …, G217, G219, G2, G4, G6, …, G218, G220
1	1		G220, G218, G216, …, G6, G4, G2, G219, G217, G215, …, G5, G3, G1

Figure 50

γ-Correction Function

The LGDP4522 has the γ-correction function to display in 262,144 colors simultaneously. The γ-correction is performed with 3 groups of registers determining eight reference grayscale levels, which are gradient adjustment, amplitude adjustment and fine-adjustment registers. Each register groups further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the LGDP4522 available with liquid crystal panels of various characteristics.

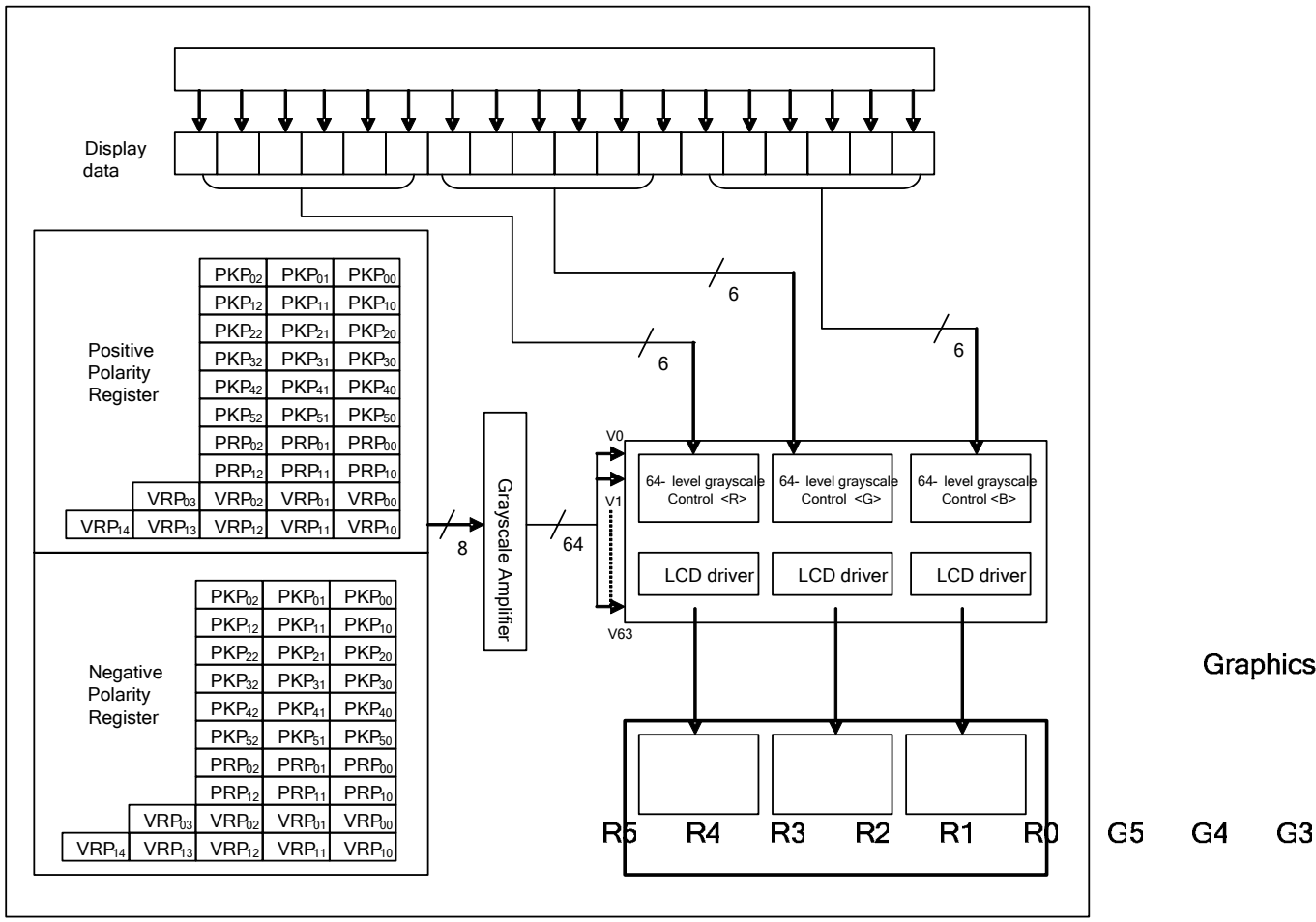


Figure 51

Grayscale Amplifier Unit Configuration

The following figure illustrates the grayscale amplifier unit of the LGDP4522.

To generate 64 grayscale voltages (V0 to V63), the LGDP4522 first generates eight reference grayscale voltages (VINP0-7/VINN0-7). The grayscale amplifier unit then divides eight reference grayscale voltages with the ladder resistors incorporated therein.

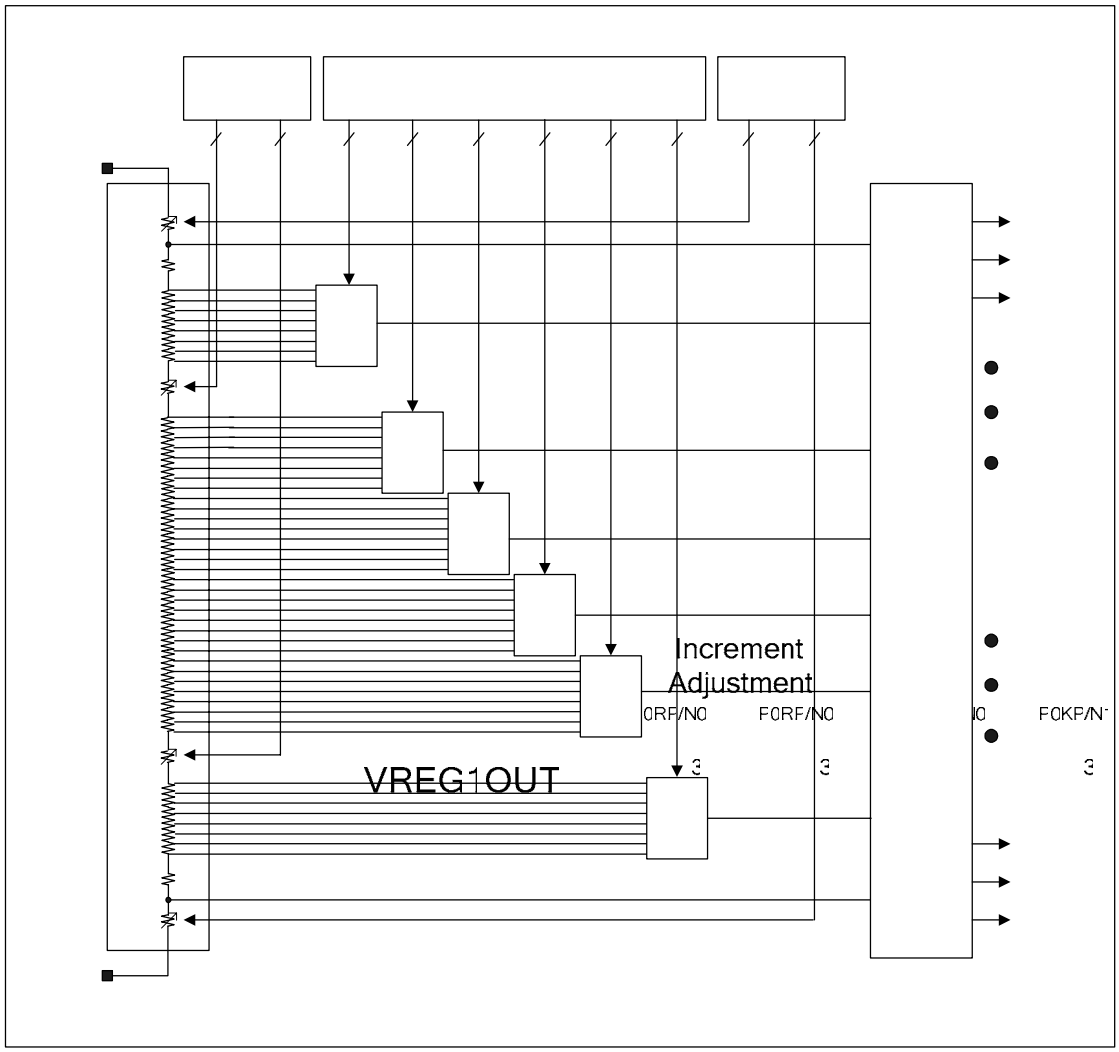


Figure 52: Grayscale amplifier unit

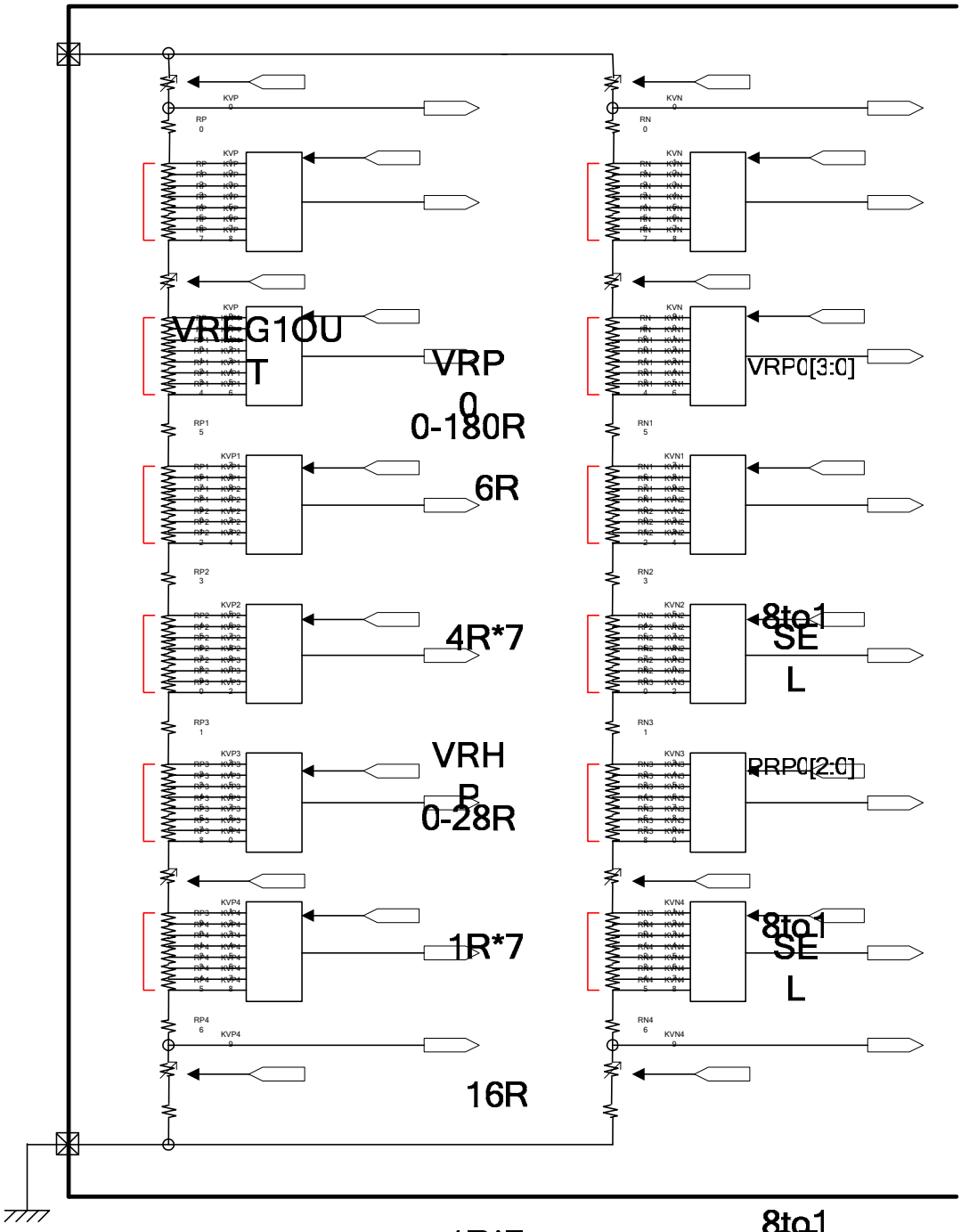


Figure 53: Ladder resistor units and 8-to-1 selectors

γ-Correction Register

The γ-correction registers of the LGDP4522 consist of gradient adjustment, amplitude adjustment, and fine adjustment registers, each of which has registers of positive and negative polarities. Each different register group can be set independently to others, enabling adjustment of grayscale voltage levels in relation to grayscales set optimally for γ-characteristics of a liquid crystal panel. These γ-correction register settings and the reference levels of the 32 grayscales to which the three kinds of adjustments are made (bold lines in the following figure) are common to all RGB dots.

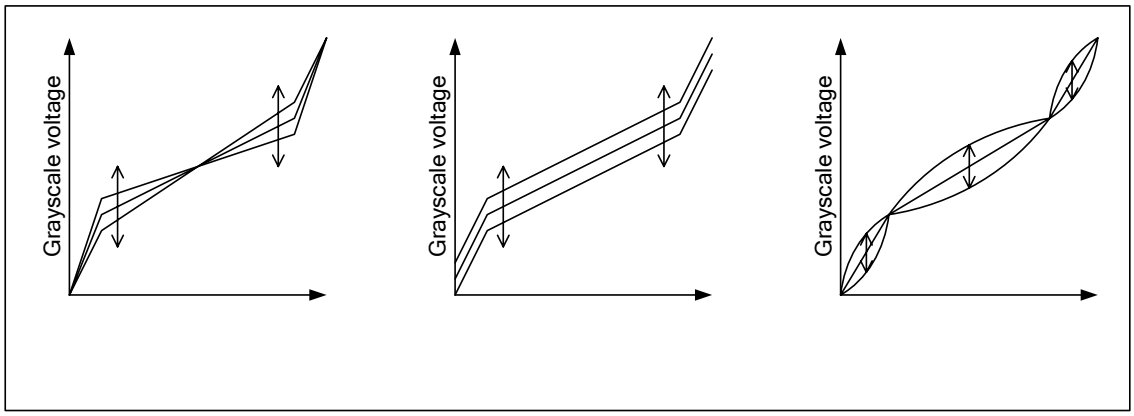


Figure 54

1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient of the curve representing the relationship between the grayscale and the grayscale voltage level around middle grayscales without changing the dynamic range. To adjust the gradient, the resistance values of grayscale reference voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor unit are adjusted. The registers consist of positive and negative polarity registers, allowing asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of grayscale voltages. To adjust the amplitude, the resistance values of the grayscale voltage generating variable resistors (VRP(N)1/0) at the top and bottom of the ladder resistor unit are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of positive and negative polarity registers.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust grayscale voltage levels. To fine-adjust grayscale voltage levels, fine adjustment registers adjust the reference voltage levels, 8 levels for each register generated from the ladder resistor unit, in respective 8-to-1 selectors. Same with other registers, the fine adjustment registers consist of positive and negative polarity registers.

Grayscale number Graysca

Gradient adjustment Amplitude

Table 54

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRHP(N)
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Fine adjustment	PKP0[2:0]	PKN0[2:0]	8-to-1 selector (voltage level of grayscale 1)
	PKP1[2:0]	PKN1[2:0]	8-to-1 selector (voltage level of grayscale 8)
	PKP2[2:0]	PKN2[2:0]	8-to-1 selector (voltage level of grayscale 20)
	PKP3[2:0]	PKN3[2:0]	8-to-1 selector (voltage level of grayscale 43)
	PKP4[2:0]	PKN4[2:0]	8-to-1 selector (voltage level of grayscale 53)
	PKP5[2:0]	PKN5[2:0]	8-to-1 selector (voltage level of grayscale 62)

Ladder Resistors and 8-to-1 Selector

Block Configuration

The reference voltage generating unit as illustrated in page 100 consists of two ladder resistor units including variable resistors and 8-to-1 selectors. Each 8-to-1 selector selects one of the 8 voltage levels generated from the ladder resistor unit to output as a grayscale reference voltage. Both variable resistors and 8-to-1 selectors are controlled according to the γ correction registers. This unit has pins to connect a volume resistor externally to compensate differences in various characteristics of panels.

Variable Resistors

The LGDP4522 uses variable resistors of the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)); amplitude adjustment (1) (VRP(N)0); and the amplitude adjustment (2) (VRP(N)1). The resistance values of these variable resistors are set by gradient adjustment registers and amplitude adjustment registers as follows.

Table 55:

Gradient adjustment

Contents of register PRP(N)0/1[2:0]	Resistance VRHP(N) VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 56:

Amplitude adjustment (1)

Contents of register VRP(N)0[3:0]	Resistance VRHP(N) VRLP(N)
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1110	28R
1111	30R

Table 57:

Amplitude adjustment (2)

Contents of register VRP(N)1[4:0]	Resistance VRHP(N) VRLP(N)
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8-to-1 Selectors

The 8-to-1 selector selects one of eight voltage levels generated from the ladder resistor unit according to the fine adjustment register, and output the selected voltage level as a reference grayscale voltage (VINP(N)1~ VINP(N 6). The table below shows the setting in the fine adjustment register and the selected voltage levels for respective reference grayscale voltages

Table 58: Fine adjustment registers and selected voltage

PKP(N)[2:0]	Selected Voltage					
	VINP(N)1	VINP(N)2	VINP(N3	VINP(N)4	VINP(N)5	VINP(N)6
0	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
1	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
2	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
3	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
4	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
5	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
6	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
7	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale voltage levels for V0~V63 grayscales are calculated from the following formulae.

Table 59: Formulae for calculating voltage (1)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	VREG1OUT - ΔV*VRE0/SUMRP	-	VINP0
KVP1	VREG1OUT - ΔV*(VRE0+6R)/SUMRP	PKP0= 0	VINP1
KVP2	VREG1OUT - ΔV*(VRE0+10R)/SUMRP	PKP0= 1	
KVP3	VREG1OUT - ΔV*(VRE0+14R)/SUMRP	PKP0= 2	
KVP4	VREG1OUT - ΔV*(VRE0+18R)/SUMRP	PKP0= 3	
KVP5	VREG1OUT - ΔV*(VRE0+22R)/SUMRP	PKP0= 4	
KVP6	VREG1OUT - ΔV*(VRE0+26R)/SUMRP	PKP0= 5	
KVP7	VREG1OUT - ΔV*(VRE0+30R)/SUMRP	PKP0= 6	
KVP8	VREG1OUT - ΔV*(VRE0+34R)/SUMRP	PKP0= 7	
KVP9	VREG1OUT - ΔV*(VRE0+34R+VRHP)/SUMRP	PKP1= 0	VINP2
KVP10	VREG1OUT - ΔV*(VRE0+35R+VRHP)/SUMRP	PKP1= 1	
KVP11	VREG1OUT - ΔV*(VRE0+36R+VRHP)/SUMRP	PKP1= 2	
KVP12	VREG1OUT - ΔV*(VRE0+37R+VRHP)/SUMRP	PKP1= 3	
KVP13	VREG1OUT - ΔV*(VRE0+38R+VRHP)/SUMRP	PKP1= 4	
KVP14	VREG1OUT - ΔV*(VRE0+39R+VRHP)/SUMRP	PKP1= 5	
KVP15	VREG1OUT - ΔV*(VRE0+40R+VRHP)/SUMRP	PKP1= 6	
KVP16	VREG1OUT - ΔV*(VRE0+41R+VRHP)/SUMRP	PKP1= 7	
KVP17	VREG1OUT - ΔV*(VRE0+51R+VRHP)/SUMRP	PKP2= 0	VINP3
KVP18	VREG1OUT - ΔV*(VRE0+52R+VRHP)/SUMRP	PKP2= 1	
KVP19	VREG1OUT - ΔV*(VRE0+53R+VRHP)/SUMRP	PKP2= 2	
KVP20	VREG1OUT - ΔV*(VRE0+54R+VRHP)/SUMRP	PKP2= 3	
KVP21	VREG1OUT - ΔV*(VRE0+55R+VRHP)/SUMRP	PKP2= 4	
KVP22	VREG1OUT - ΔV*(VRE0+56R+VRHP)/SUMRP	PKP2= 5	
KVP23	VREG1OUT - ΔV*(VRE0+57R+VRHP)/SUMRP	PKP2= 6	
KVP24	VREG1OUT - ΔV*(VRE0+58R+VRHP)/SUMRP	PKP2= 7	
KVP25	VREG1OUT - ΔV*(VRE0+80R+VRHP)/SUMRP	PKP3= 0	VINP4
KVP26	VREG1OUT - ΔV*(VRE0+81R+VRHP)/SUMRP	PKP3= 1	
KVP27	VREG1OUT - ΔV*(VRE0+82R+VRHP)/SUMRP	PKP3= 2	
KVP28	VREG1OUT - ΔV*(VRE0+83R+VRHP)/SUMRP	PKP3= 3	
KVP29	VREG1OUT - ΔV*(VRE0+84R+VRHP)/SUMRP	PKP3= 4	
KVP30	VREG1OUT - ΔV*(VRE0+85R+VRHP)/SUMRP	PKP3= 5	
KVP31	VREG1OUT - ΔV*(VRE0+86R+VRHP)/SUMRP	PKP3= 6	
KVP32	VREG1OUT - ΔV*(VRE0+87R+VRHP)/SUMRP	PKP3= 7	
KVP33	VREG1OUT - ΔV*(VRE0+97R+VRHP)/SUMRP	PKP4= 0	VINP5
KVP34	VREG1OUT - ΔV*(VRE0+98R+VRHP)/SUMRP	PKP4= 1	
KVP35	VREG1OUT - ΔV*(VRE0+99R+VRHP)/SUMRP	PKP4= 2	
KVP36	VREG1OUT - ΔV*(VRE0+100R+VRHP)/SUMRP	PKP4= 3	
KVP37	VREG1OUT - ΔV*(VRE0+101R+VRHP)/SUMRP	PKP4= 4	
KVP38	VREG1OUT - ΔV*(VRE0+102+VRHP)/SUMRP	PKP4= 5	
KVP39	VREG1OUT - ΔV*(VRE0+103R+VRHP)/SUMRP	PKP4= 6	
KVP40	VREG1OUT - ΔV*(VRE0+104R+VRHP)/SUMRP	PKP4= 7	
KVP41	VREG1OUT - ΔV*(VRE0+104R+VRHP+VRLP)/SUMRP	PKP5= 0	VINP6
KVP42	VREG1OUT - ΔV*(VRE0+108R+VRHP+VRLP)/SUMRP	PKP5= 1	
KVP43	VREG1OUT - ΔV*(VRE0+112+VRHP+VRLP)/SUMRP	PKP5= 2	
KVP44	VREG1OUT - ΔV*(VRE0+116R+VRHP+VRLP)/SUMRP	PKP5= 3	
KVP45	VREG1OUT - ΔV*(VRE0+120R+VRHP+VRLP)/SUMRP	PKP5= 4	
KVP46	VREG1OUT - ΔV*(VRE0+124R+VRHP+VRLP)/SUMRP	PKP5= 5	
KVP47	VREG1OUT - ΔV*(VRE0+128R+VRHP+VRLP)/SUMRP	PKP5= 6	
KVP48	VREG1OUT - ΔV*(VRE0+132R+VRHP+VRLP)/SUMRP	PKP5= 7	
KVP49	VREG1OUT - ΔV*(VRE0+138R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Sum of positive ladder resistors = 144R+VRHP+VRLP+VRP0+VRP1

Table 60: Formulae for calculating voltage (2)

Grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	VINP2+(VINP1-VINP2)*(30/48)
V3	VINP2+(VINP1-VINP2)*(23/48)
V4	VINP2+(VINP1-VINP2)*(16/48)
V5	VINP2+(VINP1-VINP2)*(12/48)
V6	VINP2+(VINP1-VINP2)*(8/48)
V7	VINP2+(VINP1-VINP2)*(4/48)
V8	VINP2
V9	VINP3+(VINP2-VINP3)*(22/24)
V10	VINP3+(VINP2-VINP3)*(20/24)
V11	VINP3+(VINP2-VINP3)*(18/24)
V12	VINP3+(VINP2-VINP3)*(16/24)
V13	VINP3+(VINP2-VINP3)*(14/24)
V14	VINP3+(VINP2-VINP3)*(12/24)
V15	VINP3+(VINP2-VINP3)*(10/24)
V16	VINP3+(VINP2-VINP3)*(8/24)
V17	VINP3+(VINP2-VINP3)*(6/24)
V18	VINP3+(VINP2-VINP3)*(4/24)
V19	VINP3+(VINP2-VINP3)*(2/24)
V20	VINP3
V21	VINP4+(VINP3-VINP4)*(22/23)
V22	VINP4+(VINP3-VINP4)*(21/23)
V23	VINP4+(VINP3-VINP4)*(20/23)
V24	VINP4+(VINP3-VINP4)*(19/23)
V25	VINP4+(VINP3-VINP4)*(18/23)
V26	VINP4+(VINP3-VINP4)*(17/23)
V27	VINP4+(VINP3-VINP4)*(16/23)
V28	VINP4+(VINP3-VINP4)*(15/23)
V29	VINP4+(VINP3-VINP4)*(14/23)
V30	VINP4+(VINP3-VINP4)*(13/23)
V31	VINP4+(VINP3-VINP4)*(12/23)

Grayscale voltage	Formula
V32	VINP4+(VINP3-VINP4)*(11/23)
V33	VINP4+(VINP3-VINP4)*(10/23)
V34	VINP4+(VINP3-VINP4)*(9/23)
V35	VINP4+(VINP3-VINP4)*(8/23)
V36	VINP4+(VINP3-VINP4)*(7/23)
V37	VINP4+(VINP3-VINP4)*(6/23)
V38	VINP4+(VINP3-VINP4)*(5/23)
V39	VINP4+(VINP3-VINP4)*(4/23)
V40	VINP4+(VINP3-VINP4)*(3/23)
V41	VINP4+(VINP3-VINP4)*(2/23)
V42	VINP4+(VINP3-VINP4)*(1/23)
V43	VINP4
V44	VINP5+(VINP4-VINP5)*(22/24)
V45	VINP5+(VINP4-VINP5)*(20/24)
V46	VINP5+(VINP4-VINP5)*(18/24)
V47	VINP5+(VINP4-VINP5)*(16/24)
V48	VINP5+(VINP4-VINP5)*(14/24)
V49	VINP5+(VINP4-VINP5)*(12/24)
V50	VINP5+(VINP4-VINP5)*(10/24)
V51	VINP5+(VINP4-VINP5)*(8/24)
V52	VINP5+(VINP4-VINP5)*(6/24)
V53	VINP5+(VINP4-VINP5)*(4/24)
V54	VINP5+(VINP4-VINP5)*(2/24)
V55	VINP5
V56	VINP6+(VINP5-VINP6)*(44/48)
V57	VINP6+(VINP5-VINP6)*(40/48)
V58	VINP6+(VINP5-VINP6)*(36/48)
V59	VINP6+(VINP5-VINP6)*(32/48)
V60	VINP6+(VINP5-VINP6)*(25/48)
V61	VINP6+(VINP5-VINP6)*(18/48)
V62	VINP6
V63	VINP7

Note: Make sure DDVDH-V0 > 0.5V

Relationship between RAM Data and Voltage Output Levels

The relationship between RAM data and source output voltage levels is as follows. See also Table 42: GRAM data and LCD output level.

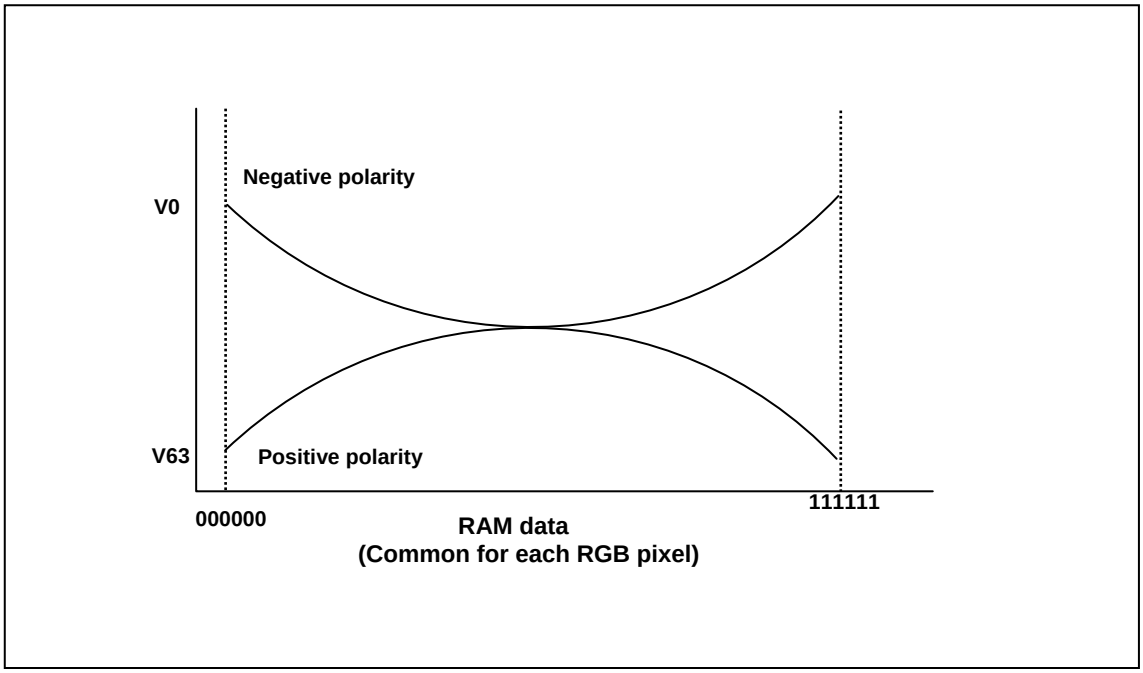


Figure 55: RAM data and the output voltage (REV = "0")

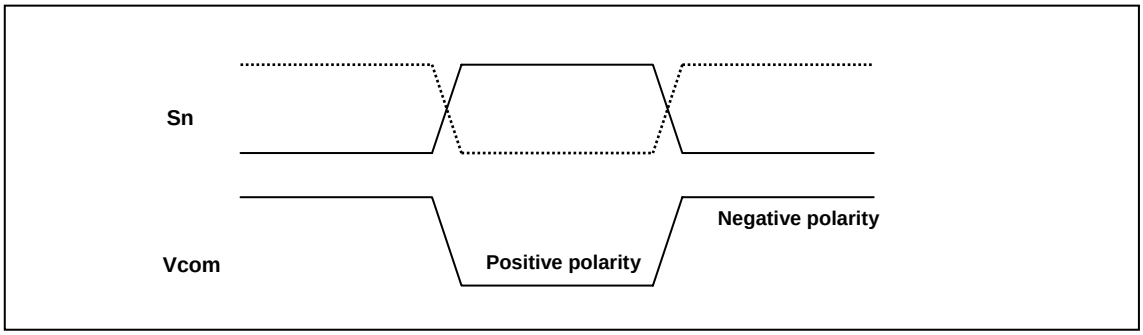


Figure 56: Source output and Vcom

8-Color Display Mode

The LGDP4522 has a function to display in 8colors. In 8-color mode, available grayscale levels are V0 and V63, and the power supplies of other grayscales (V1 to V62) are halted to reduce power consumption.

In 8-color display mode, the MSBs of the respective dot data (R5, G5, B5) are written to the rest of the dot data in order to display in 8 colors without rewriting the RAM data.

The γ- correction registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode.

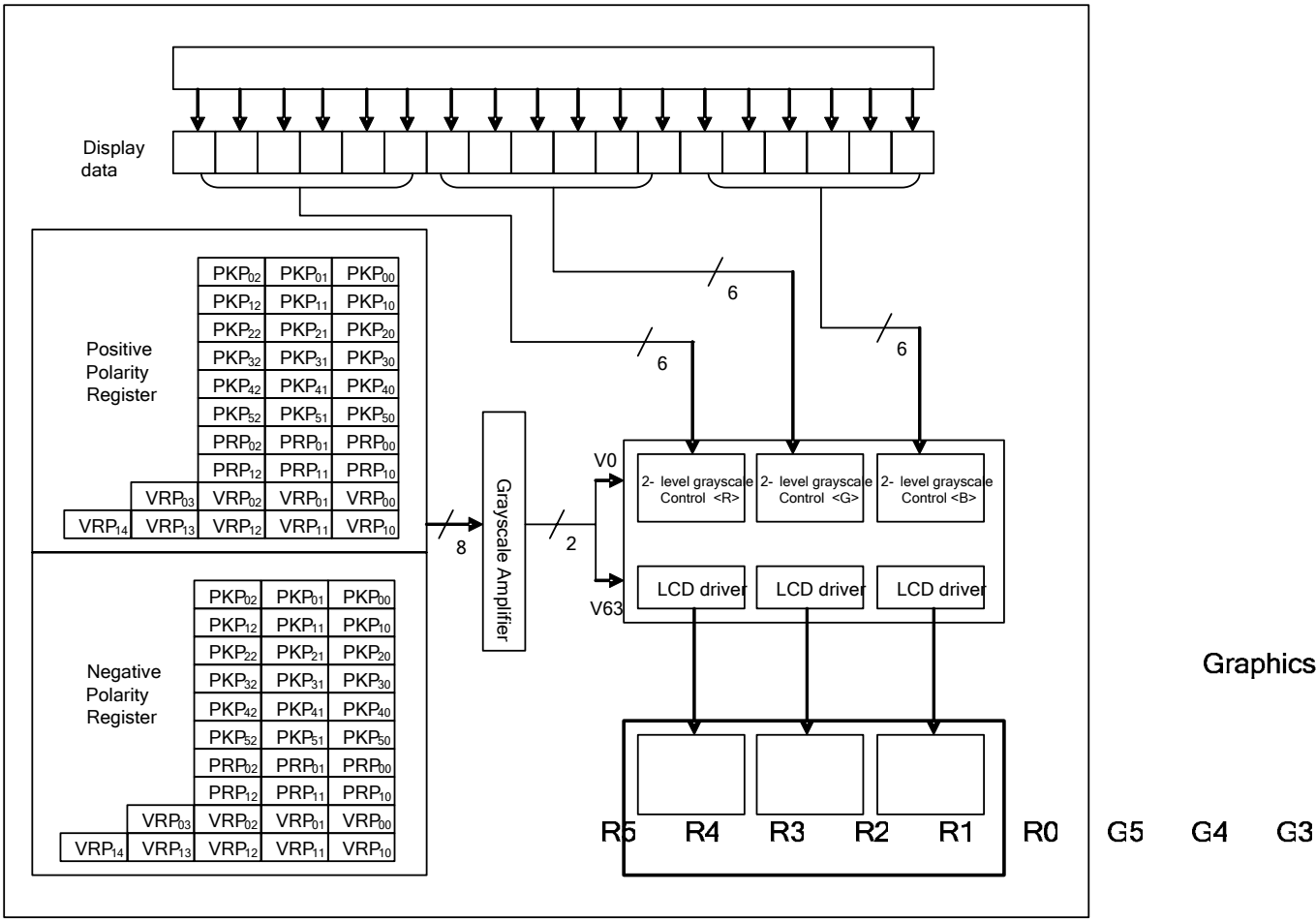


Figure 57

To switch between the 262,144-color mode and 8-color mode, follow the sequence below.

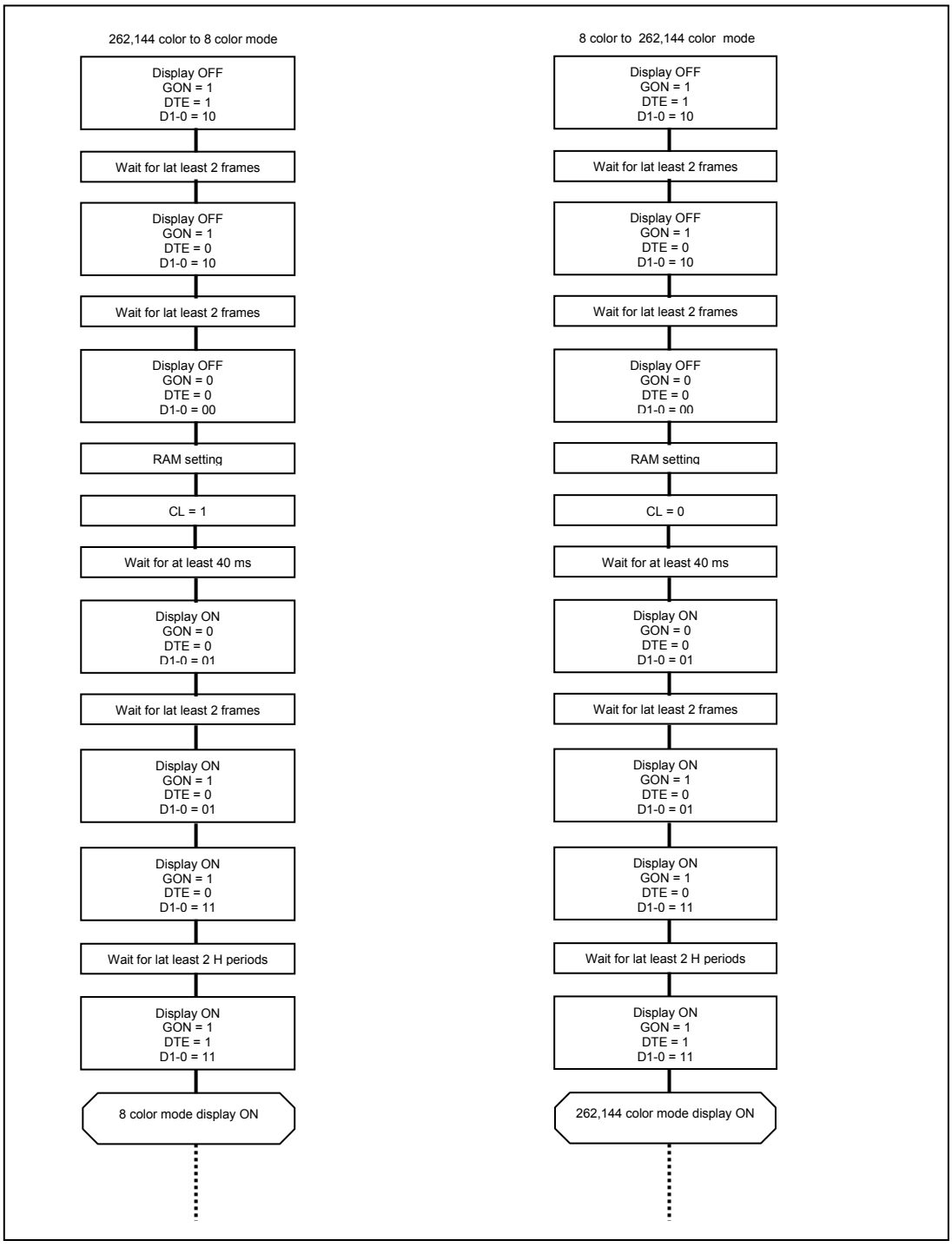
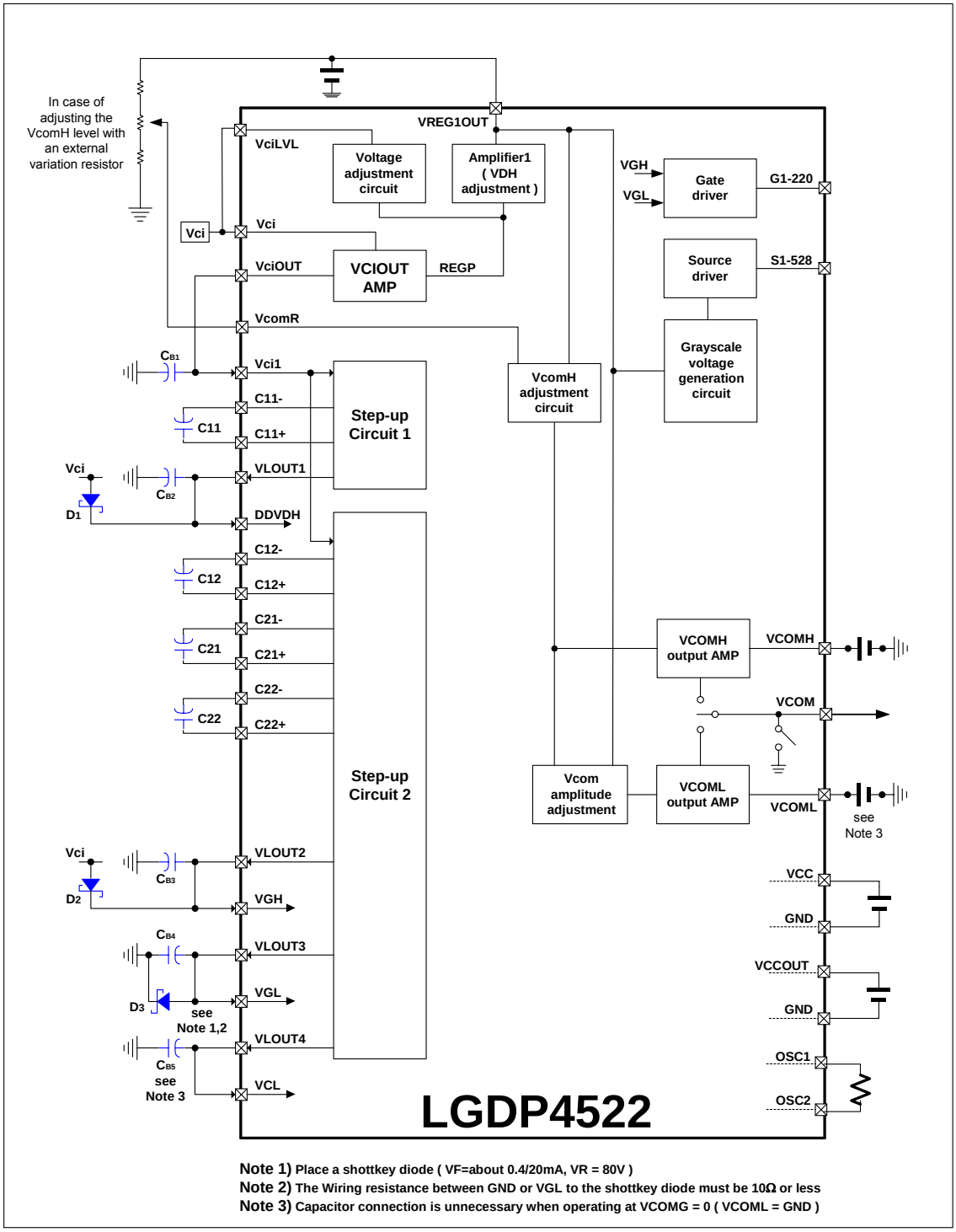


Figure 58

Configuration of Power Supply Circuit

The follow are the configuration of power supply circuit to generate liquid crystal panel drive levels.



Note 1) Place a shottkey diode (VF=about 0.4/20mA, VR = 80V)
Note 2) The Wiring resistance between GND or VGL to the shottkey diode must be 10Ω or less
Note 3) Capacitor connection is unnecessary when operating at VCOMG = 0 (VCOML = GND)

Figure 59

Specification of External Elements Connected to LGDP4522 Power Supply

The follow table shows specifications of external element connected to the LGDP4522's power supply circuit.

Table 61: Capacitor

Capacity	Recommended voltage	Pin connection
1uF (B characteristics)	6V	VREG1OUT, VciOUT, VOUT4 (see note), VcomH, VcomL (see note), C11+/- , C12+/-, VCCOUT
	10V	VLOUT1, C21+/- , C22+/-
	25V	VLOUT2, VLOUT3

Note: Capacitor connection is not necessary in some operation modes.

Table 62: Schottky diode

Feature	Pin connection
VF < 0.4V/20mA at 25°C , VR>30V	GND - VGL (Vci – VGH) (Vci – DDVDH)

Table 63: Variable resistor

Feature	Pin connection
> 200kΩ	VcomR

Instruction Setting

When setting the following instructions, follow respective sequences below.

Display On/Off

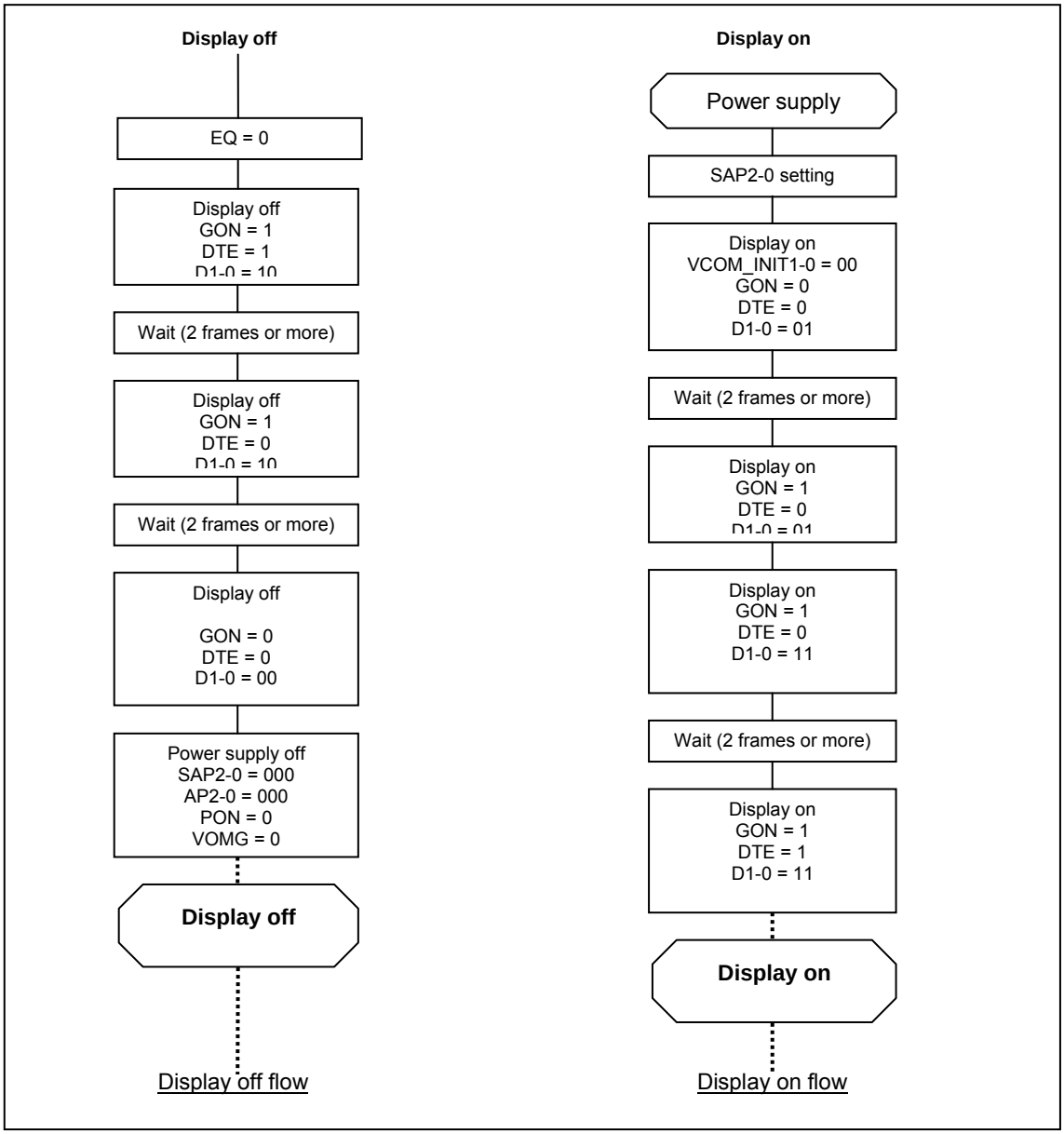


Figure 60

Standby and Sleep Modes

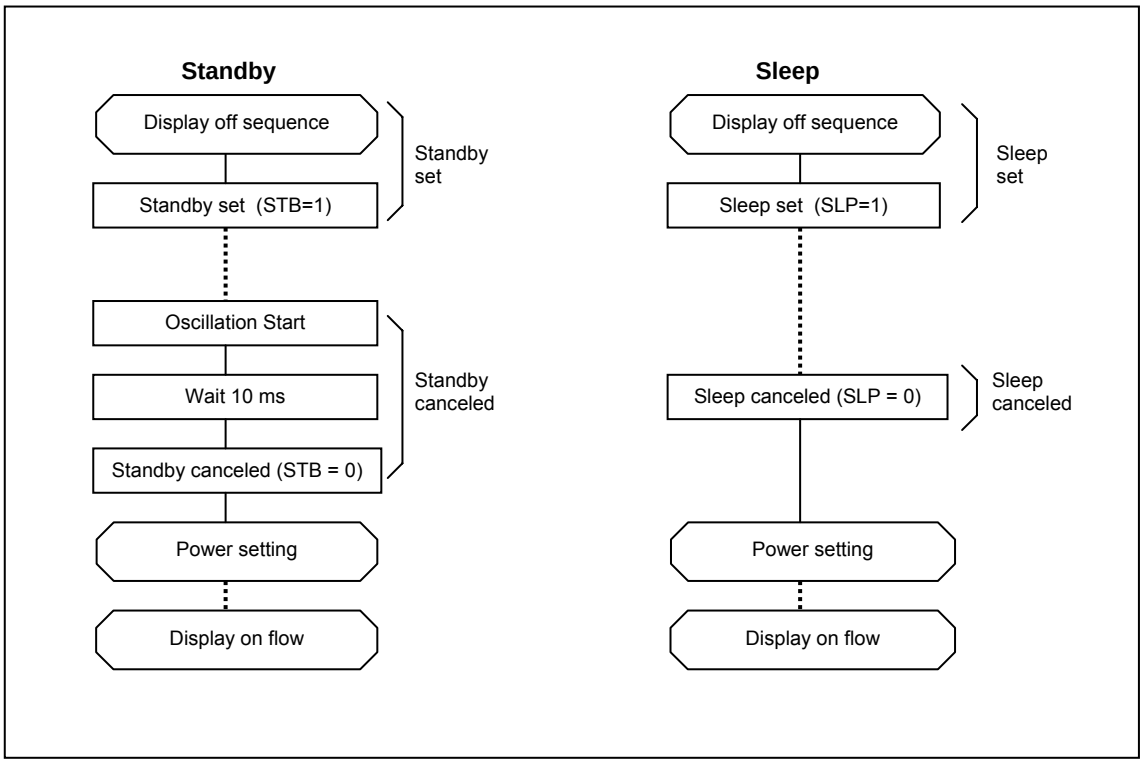


Figure 61

Power Supply Setting

When supplying and cutting off power, follow the sequence below. The setting time for oscillators, step-up circuits and operational amplifiers depends on external resistance and capacitance.

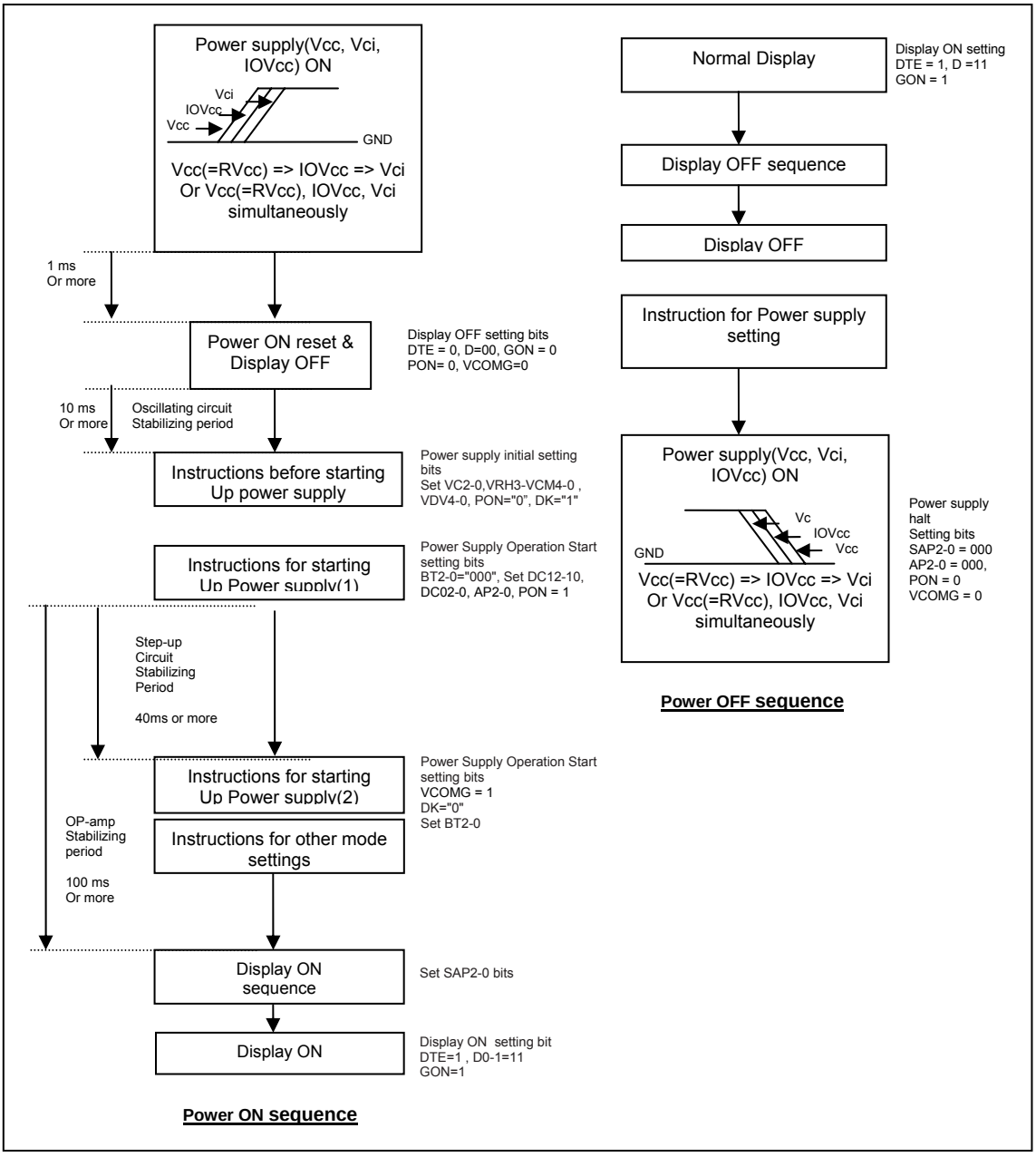


Figure 62

Pattern Diagram for Voltage Setting

The pattern diagram for the voltages and the waveforms of the voltages of the LGDP4522 are as follows.

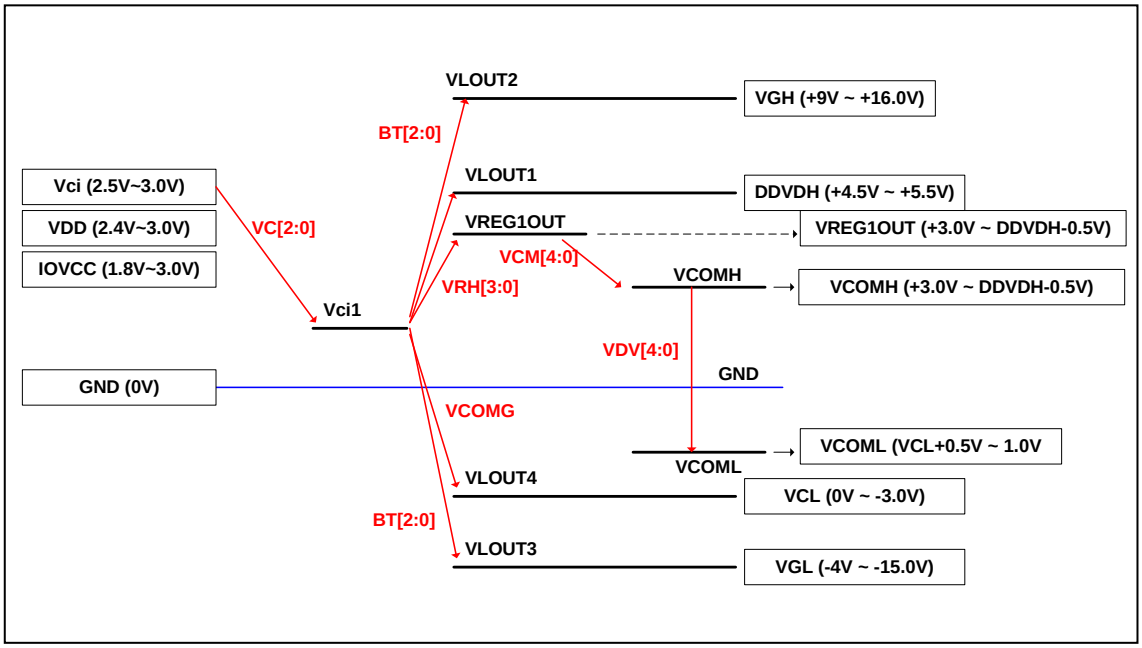


Figure 63

Note: The DDVDH, VGH, VGL, and VCL output voltage levels are lower than their theoretical levels (ideal voltage levels) due to current consumption at respective output. The voltage levels in the following relationships (DDVDH – VREG1OUT) > 0.5V, (VcomL1 – VCL) > 0.5V, (VcomL2 – VCL) > 0.5V are the actual voltage levels. When the alternating cycles of Vcom1 and Vcom2 are set high (e.g. the polarity inverts every line cycle), current consumption is large. In this case, check the voltage before use.

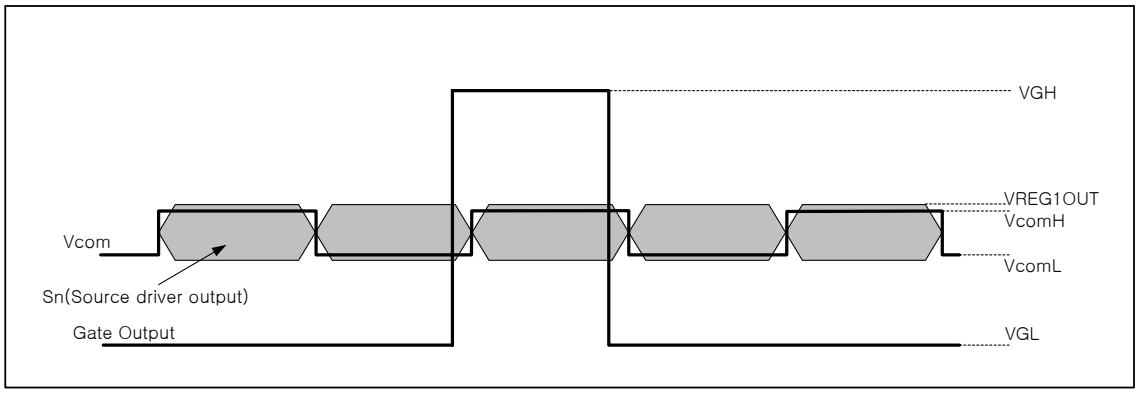


Figure 64: Applied voltage to the TFT display

Oscillator

The LGDP4522 generates oscillation with the LGDP4522's internal RC oscillators by placing an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency varies due to resistance value of external resistor, wiring distance, and operating supply voltage. For example, placing an Rf resistor of a larger resistance value, or lowering the supply voltage level brings down the oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between resistance value of Rf resistor and oscillation frequency.

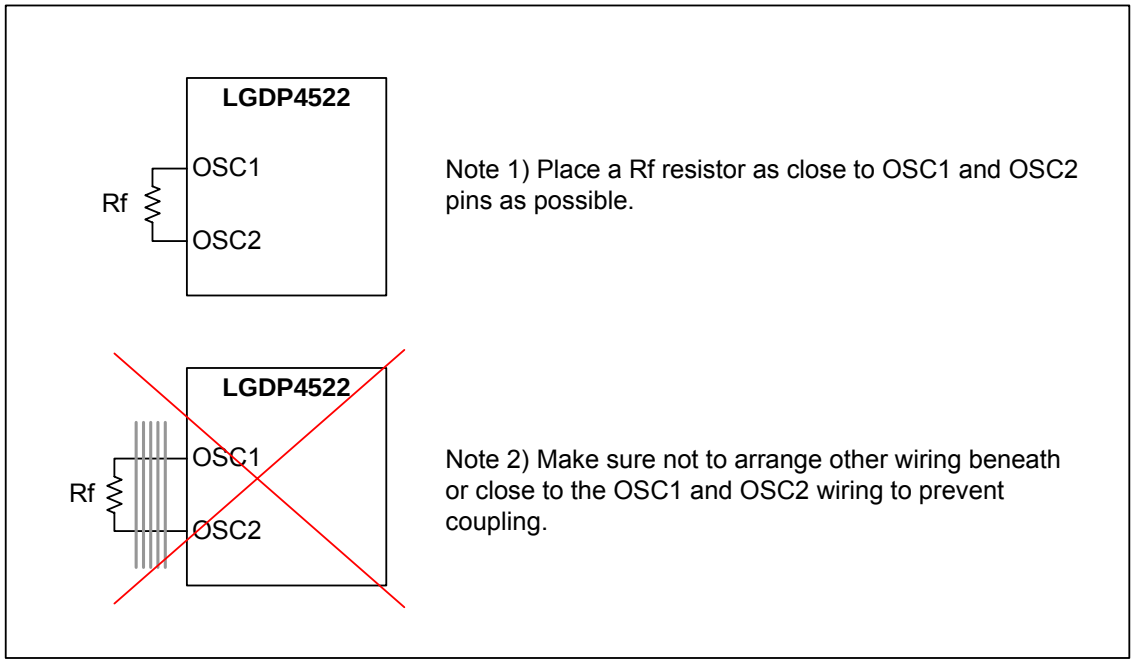


Figure 65

n-Line Inversion AC Drive

The LGDP4522, in addition to the frame-inversion liquid crystal AC drive, supports the n-line inversion AC drive, in which the polarity of liquid crystal is inverted in units of n lines, where n takes a number from 1 to 64. The quality of display will be improved by using n-line inversion AC drive.

In determining n (the value set with the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.

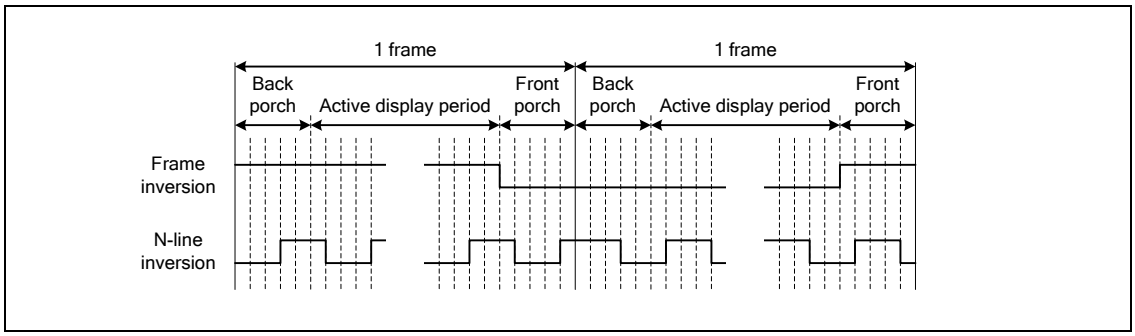


Figure 66

Interlaced Scan

The LGDP4522 supports interlaced scan for driving a frame by splitting it into n fields in order to prevent flicker.

To determine the number of fields (n: value set with the FLD bits), check the quality of display on the liquid crystal panel in use. The following table shows the scanned (gate) lines in each field. When FLD[1:0] = “01”, the number of fields in one frame is one. When FLD[1:0] = “11”, the number of fields in one frame is three. The figure illustrates the output waveforms of 3-field interlaced scan.

Table 64: Interlaced scan (GS = “0”)

FLD[1:0]	01	11		
Field / Gate	-	1	2	3
G1	*	*		
G2	*		*	
G3	*			*
G4	*	*		
G5	*		*	
G6	*			*
G7	*	*		
G8	*		*	
:				
G217	*	*		
G218	*		*	
G219	*			*
G220	*	*		

Table 65: Interlaced scan (GS = “1”)

FLD[1:0]	01	11		
Field / Gate	-	1	2	3
G220	*	*		
G219	*		*	
G218	*			*
G217	*	*		
G216	*		*	
G215	*			*
G214	*	*		
G213	*		*	
:				
G4	*	*		
G3	*		*	
G2	*			*
G1	*	*		

*: scanned gate lines

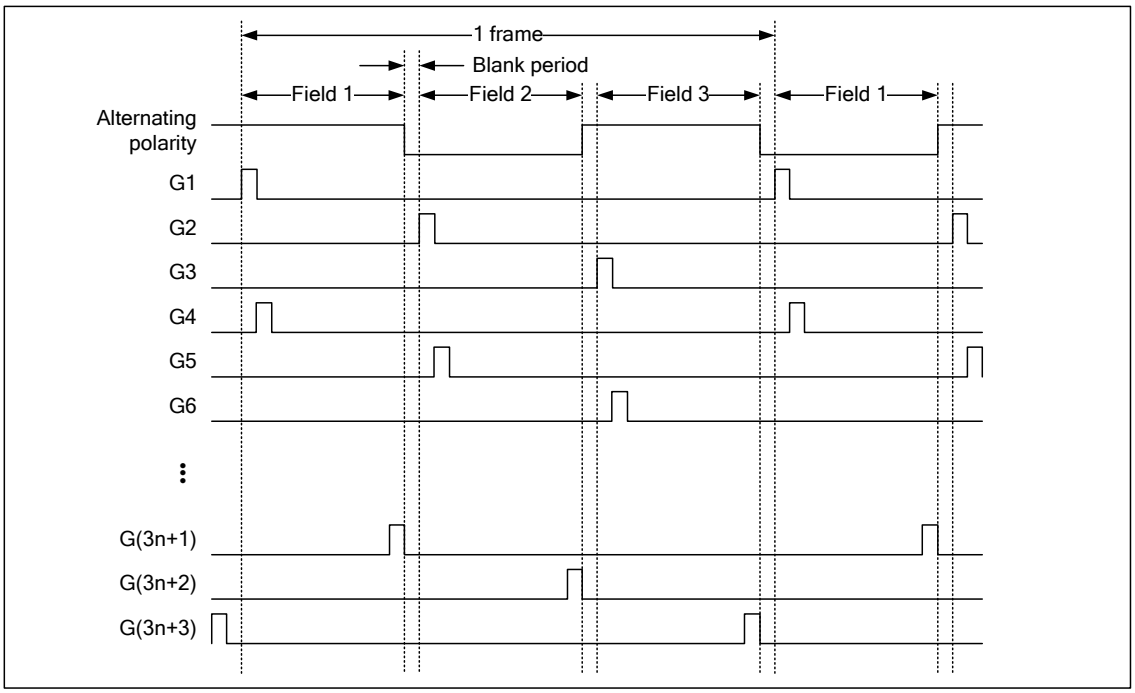


Figure 67: Gate output timing of 3-field interlaced scan

Alternating Timing

The following figure illustrates the timing of liquid crystal polarity inversion in different driving formulae. In case of frame-inversion AC drive, the polarity is inverted after drawing one frame, followed by a blank period lasting for a 16H period, where all outputs from the gate lines become the VGL level. In case of 3-field interlaced scan, polarity is inverted after drawing one field, followed by blank periods that add up to a 16H period in one frame. In case of n-line inversion AC drive, polarity is inverted as drawing n lines, and a blank period lasting for a 16H period is inserted after drawing one frame.

In the interlaced scan, be sure to set the numbers of back and front porches as follows: BP = 3, FP = 5.

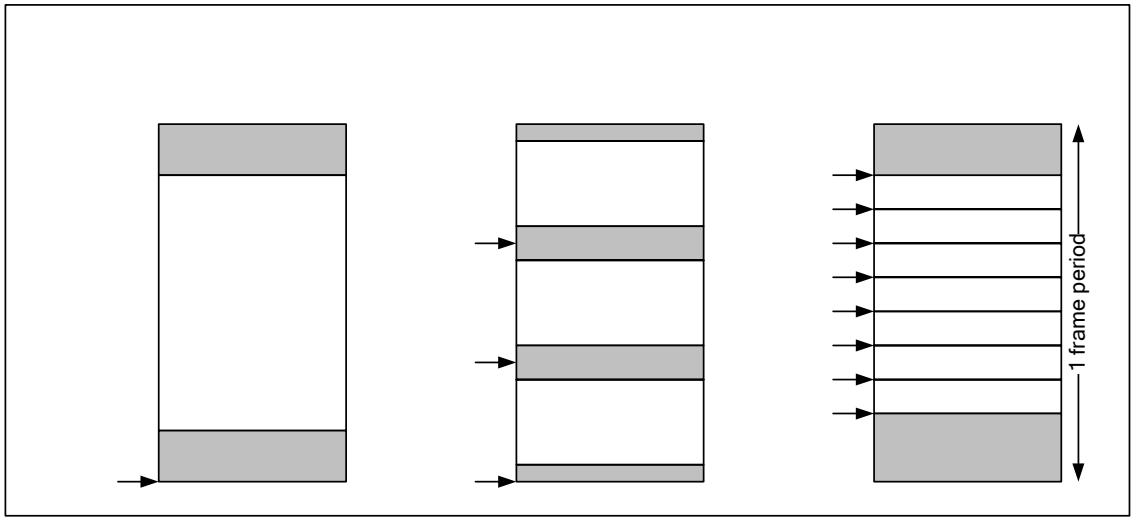


Figure 68

Frame inversion
AC drive

3-fie

Back porch

Alternating
timing

Frame 1

Alternating
timing

Alternating
timing

Front porch

Alternating
timing

Frame Frequency Adjustment Function

The LGDP4522 has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by instructions (using the DIV, RTN bits) without changing the oscillation frequency.

To switch frame frequencies between when displaying a moving picture and when displaying a still picture, set a high oscillation frequency in advance. By doing so, it becomes possible to set a low frame frequency when displaying a still picture for saving power consumption and to set a high frame frequency when displaying a moving picture.

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following formula. The frame frequency is adjusted by instruction using the 1H period adjustment bits (RTN bits) and the operation clock division bits (DIV bits).

$$frame\ frequency = \frac{fosc}{clock\ cycles\ per\ line * division\ ratio * (Line + BP + FP)}$$

where

fosc = RC oscillation frequency,
Line = number of lines to drive the LCD (NL bits),
clock cycle per line = RTN bits,
division ratio: DIV bits,
FP = number of lines for front porch and
BP = number of lines for back porch.

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines to drive the LCD: 220 lines
1H period: 44 clock cycle (RTN[6:0] = 2Ch)
Operational clock division ratio: 1/1

$fosc = 60\ Hz \times (0 + 44)\ clocks \times 1/1 \times (220 + 16)\ lines = 623\ kHz$

In this case, the RC oscillation frequency is 676 kHz. Adjust the external resistor of the RC oscillator to 623 kHz.

Partial Display Function

The LGDP4522 allows selectively driving two images on the screen at arbitrary positions set in the screen drive position registers (R42h and R43h). Only the lines for displaying two images are selectively driven in order to reduce current consumption.

The first display drive position register (R42h) includes the start line setting bits (SS1) and the end line setting bits (SE1) for displaying the first image. The second display drive position register (R43h) includes the start line setting bits (SS2) and the end line setting bits (SE2) for displaying the second image. The second display control is effective when the SPT bit is set to “1”. The total number of lines driven for displaying the first and second display must be less than the number of lines set with the NL bits.

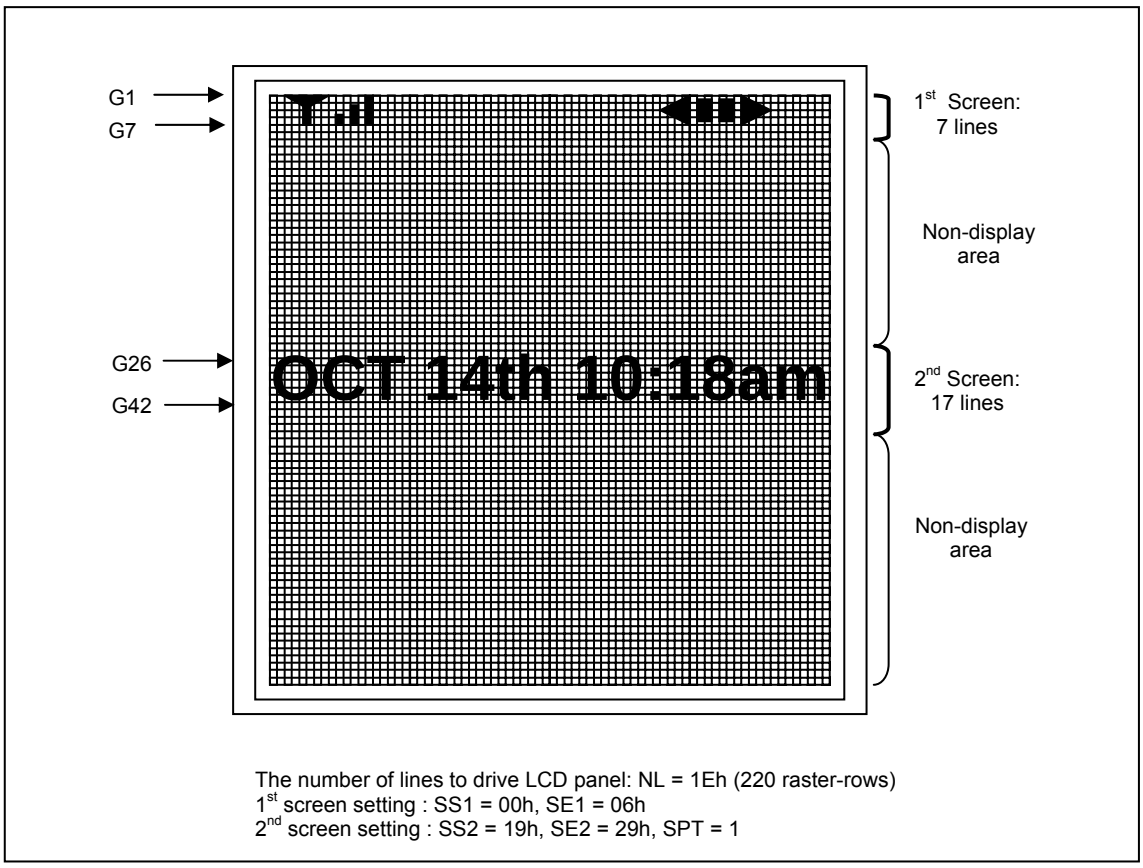


Figure 69

Constraints in Setting the 1st/2nd Screen Drive Position Registers

When setting the start line setting bits (SS1[7:0]) and the end line setting bits (SE1[7:0]) of the first display drive position register (R42h), and the start line setting bits (SS2[7:0]) and the end line setting bits (SE2[7:0]) of the second display drive position register (R43h), it is necessary to satisfy the following conditions to display screens correctly.

Table 66: One screen drive (SPT = "0")

Register Settings	Display Operation
(SE1 – SS1) = NL	Full screen display The area of (SE1 – SS1) is normally displayed.
(SE1 – SS1) < NL	Partial screen display The area of (SE1 – SS1) is normally displayed. The rest of the area is a white display irrespective of data in RAM.
(SE1 – SS1) > NL	Setting disabled

Table 67: Two screen drive (SPT = "1")

Register Settings	Display Operation
((SE1 – SS1) + (SE2 – SS2)) = NL	Full screen display The area of (SE2 – SS1) is normally displayed.
((SE1 – SS1) + (SE2 – SS2)) < NL	Partial screen display The area of (SE2 – SS1) is normally displayed. The rest of the area is a white display irrespective of data in RAM.
((SE1 – SS1) + (SE2 – SS2)) > NL	Setting disabled

Note 1) Be sure that SS1 ≤ SE1 ≤ SS2 ≤ SE2 ≤ EFh.
Note 2) Be sure that (SE2 – SS1) ≤ NL.

The outputs from the source driver in non-display areas of the partial display can be changed as follows. Select the appropriate kind of source outputs according to the characteristics of the display panel.

Table 68

PTS	Source output in non-display area		Operating grayscale amplifier in non-display area
	Positive polarity	Negative polarity	
000	V63	V0	V0 to V63
001	Setting disabled	Setting disabled	-
010	GND	GND	V0 to V63
011	High impedance	High impedance	V0 to V63
100	V63	V0	V0, V63
101	Setting disabled	Setting disabled	-
110	GND	GND	V0, V63
111	High impedance	High impedance	V0, V63

Table 69

PTG	Gate outputs in non-display area
00	Normal scan
01	VGL (fixed)
10	Interval scan
11	Setting disabled

Follow the sequences below when using the partial display function.

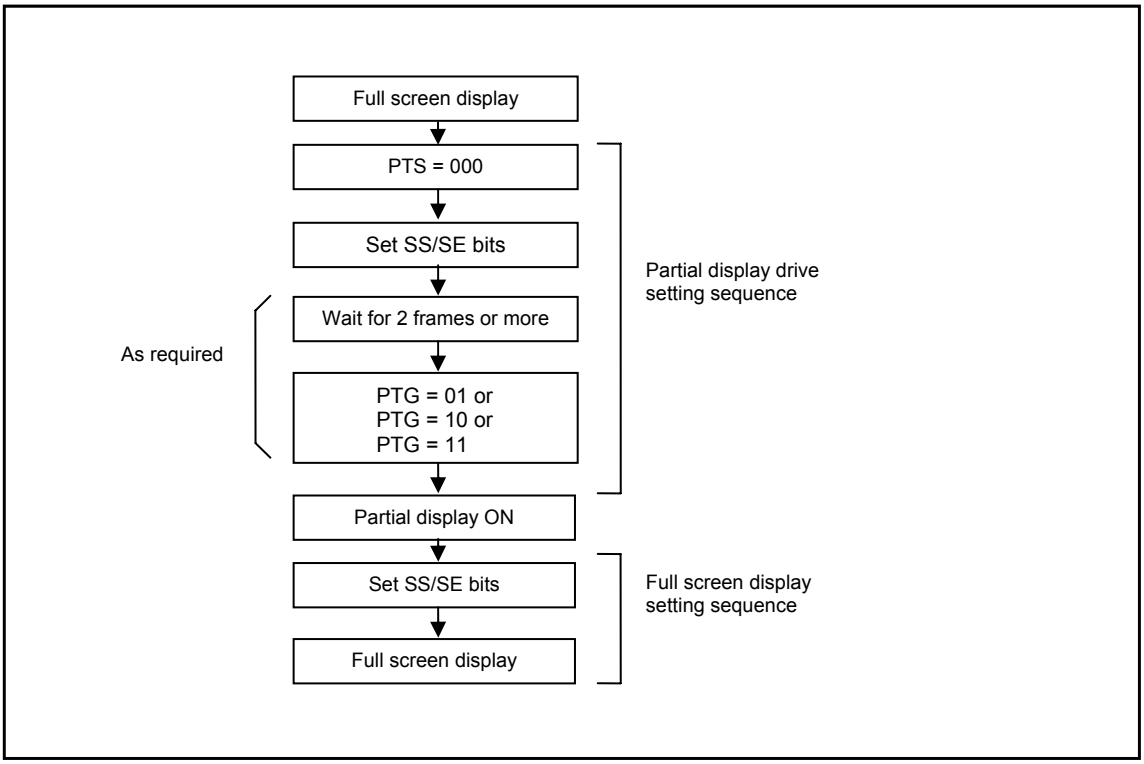

Full screen display
PTS = 000
Set SS/SE bits
Wait for 2 frames or more
PTG = 01 or
PTG = 10 or
PTG = 11
Partial display ON
Set SS/SE bits
Full screen display
As required
Partial display drive
setting sequence
Full screen display
setting sequence

Figure 70

EPROM Control

LGDP4522 has an embedded EPROM which is a 32-bit one-time programmable (OTP) IP from eMemory Technology Inc. (EO01X32GCV1).

EO01X32GCV1 is a CMOS, 1bit (1-bit) program OTP logic device. The main memory block is organized as 8-bits by 4 banks. See the data sheet of EO01X32GCV1.

The pins of the embedded EPROM can be controlled using the EPROM control 1 (R60h) register as shown below.

Table 70: Pin mapping

EO01X32GCV1	Bit fields of register R60h
POR = 0V/1.8V	POR = 0/1
VPP = 1.8V/7.2V	VPP = 0/1
PPROG = 0V/1.8V	PPROG = 0/1
PWE = 0V/1.8V	PWE = 0/1
PA[1:0] = 0V/1.8V	PA[1:0] = 0/1
PDIN[6:0] = 0V/1.8V	PDIN[6:0] = 0/1

The RA[1:0] of register R61h selects one of four EPROM bytes.

Accessing EPROM control registers, follow the timing requirements of read and program cycles.

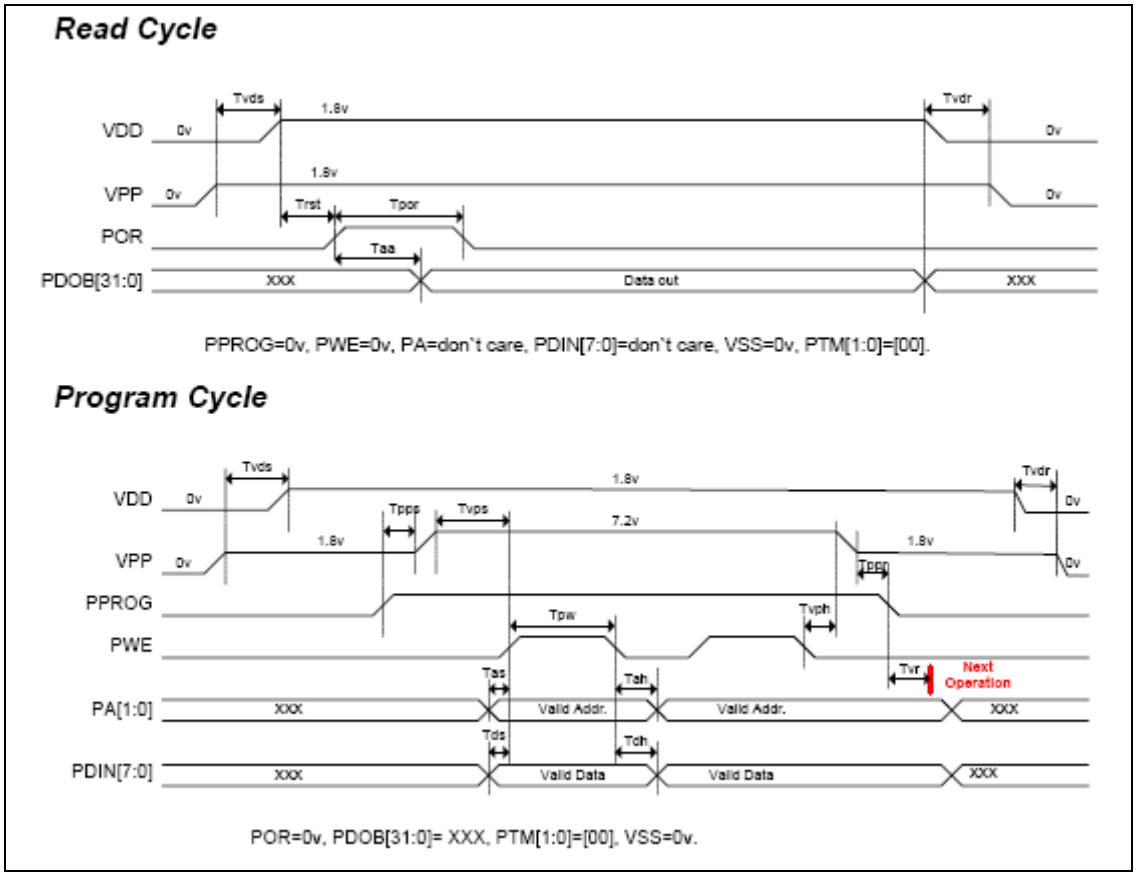


Figure 71: EPROM timings

Panel Wiring Example

TBD

Absolute Maximum Ratings

TBD

Electrical Characteristics

DC Characteristics

TBD

80-System Bus Interface Timing Characteristics (18/16-Bit Bus)

Table 71: See Figure 74 (Condition: IOVcc = 1.65 to 3.30V, Vcc = RVcc = 2.40 to 3.30V)

Item			Symbol	Unit	Min	Typ	Max
Bus cycle time		Write	t_{CYCW}	ns	70	-	-
		Read	t_{CYCR}		250	-	-
Write “Low” level pulse width		Write	PW_{LW}	ns	40	-	-
Read “Low” level pulse width		Read	PW_{LR}		150	-	-
Write “High” level pulse width		Write	PW_{HW}	ns	30	-	-
Read “High” level pulse width		Read	PW_{HR}		100	-	-
Write/Read rise/fall time			t_{WRr}, t_{WRf}	ns	-	-	25
Setup time	Write (RS to CS*/WR*)		t_{AS}	ns	0	-	-
	Read (RS to CS*/RD*)				10	-	-
Address hold time			t_{AH}	ns	2	-	-
Write data setup time			t_{DSW}	ns	25	-	-
Write data hold time			t_{H}	ns	5	-	-
Read data delay time			t_{DDR}	ns	-	-	200
Read data hold time			t_{DHR}	ns	5	-	-

80-System Bus Interface Timing Characteristics (8/9-Bit Bus)

Table 72: See Figure 74 (Condition: IOVcc = 1.65 to 3.30V, Vcc = RVcc = 2.40 to 3.30V)

Item			Symbol	Unit	Min	Typ	Max
Bus cycle time		Write	t_{CYCW}	ns	70	-	-
		Read	t_{CYCR}		250	-	-
Write “Low” level pulse width		Write	PW_{LW}	ns	40	-	-
Read “Low” level pulse width		Read	PW_{LR}		150	-	-
Write “High” level pulse width		Write	PW_{HW}	ns	30	-	-
Read “High” level pulse width		Read	PW_{HR}		100	-	-
Write/Read rise/fall time			t_{WRr}, t_{WRf}	ns	-	-	25
Setup time	Write (RS to CS*/WR*)		t_{AS}	ns	0	-	-
	Read (RS to CS*/RD*)				10	-	-
Address hold time			t_{AH}	ns	2	-	-
Write data setup time			t_{DSW}	ns	25	-	-
Write data hold time			t_{H}	ns	5	-	-
Read data delay time			t_{DDR}	ns	-	-	200
Read data hold time			t_{DHR}	ns	5	-	-

Serial Peripheral Interface Timing Characteristics

Table 73: See Figure 75 (Condition: IOVcc = 1.65 to 3.30V, Vcc = RVcc = 2.40 to 3.30V)

Item		Symbol	Unit	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	ns	100	-	20000
	Read (transmitted)			350	-	20000
Serial clock "High" level pulse width	Write (received)	t_{SCH}	ns	40	-	-
	Read (transmitted)			150	-	-
Serial clock "Low" level pulse width	Write (received)	t_{SCL}	ns	40	-	-
	Read (transmitted)			150	-	-
Serial clock rise/fall time		t_{scr}, t_{scf}	ns	-	-	20
Chip select setup time		t_{CSU}	ns	20	-	-
Chip select hold time		t_{CH}	ns	60	-	-
Serial input data setup time		t_{SISU}	ns	30	-	-
Serial input data hold time		t_{SIH}	ns	30	-	-
Serial output data setup time		t_{SOD}	ns	-	-	130
Serial output data hold time		t_{SOH}	ns	5	-	-

Reset Timing Characteristics

Table 74: See Figure 76 (Condition: IOVcc = 1.65 to 3.30V, Vcc = RVcc = 1.80 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
Reset "Low" level width	t_{RES}	ms	1	-	-
Reset rise time	t_{rRES}	us	-	-	10

RGB Interface Timing Characteristics

Table 75: See Figure 77 (18/16-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = RVcc = 2.40 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	ns	0		
ENABLE setup time	tENS	ns	10		
ENABLE hold time	tENH	ns	20		
DOTCLK "Low" level pulse width	PW_{DL}	ns	40		
DOTCLK "High" level pulse width	PW_{DH}	ns	40		
DOTCLK cycle time	tCYCD	ns	100		
Data setup time	tPDS	ns	10		
Date hold time	tPDH	ns	40		
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns			25

Table 76: See Figure 77 (6-bit I/F, IOVcc = 1.65 to 3.30V, Vcc = RVcc = 2.40 to 3.30V)

Item	Symbol	Unit	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	ns	0		
ENABLE setup time	tENS	ns	10		
ENABLE hold time	tENH	ns	20		
DOTCLK "Low" level pulse width	PW_{DL}	ns	30		
DOTCLK "High" level pulse width	PW_{DH}	ns	30		
DOTCLK cycle time	tCYCD	ns	100		
Data setup time	tPDS	ns	10		
Date hold time	tPDH	ns	40		
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns			25

LCD Driver Output Characteristics

Table 77: See Figure 78.

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Driver output delay time	t_{DD}	us	Vcc=3.0V, DDVDH=5.5V, VREG1OUT=5.0V, RC oscillation: fosc =315kHz (driving 220 lines), Ta=25°C REV=0, SAP=010, AP=010, VRN14-00=0, VRP14-00=0, PKP52-00=0, PKN52-00=0, PRP12-00=0, PRN12-00=0, Load resistance R=10kΩ, Load capacitance C=20pF Time to reach the target voltage level ±35mV from a same grayscale level at all source pins	-	35	-

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following are the configurations of I pin, I/O pin, and O pin.

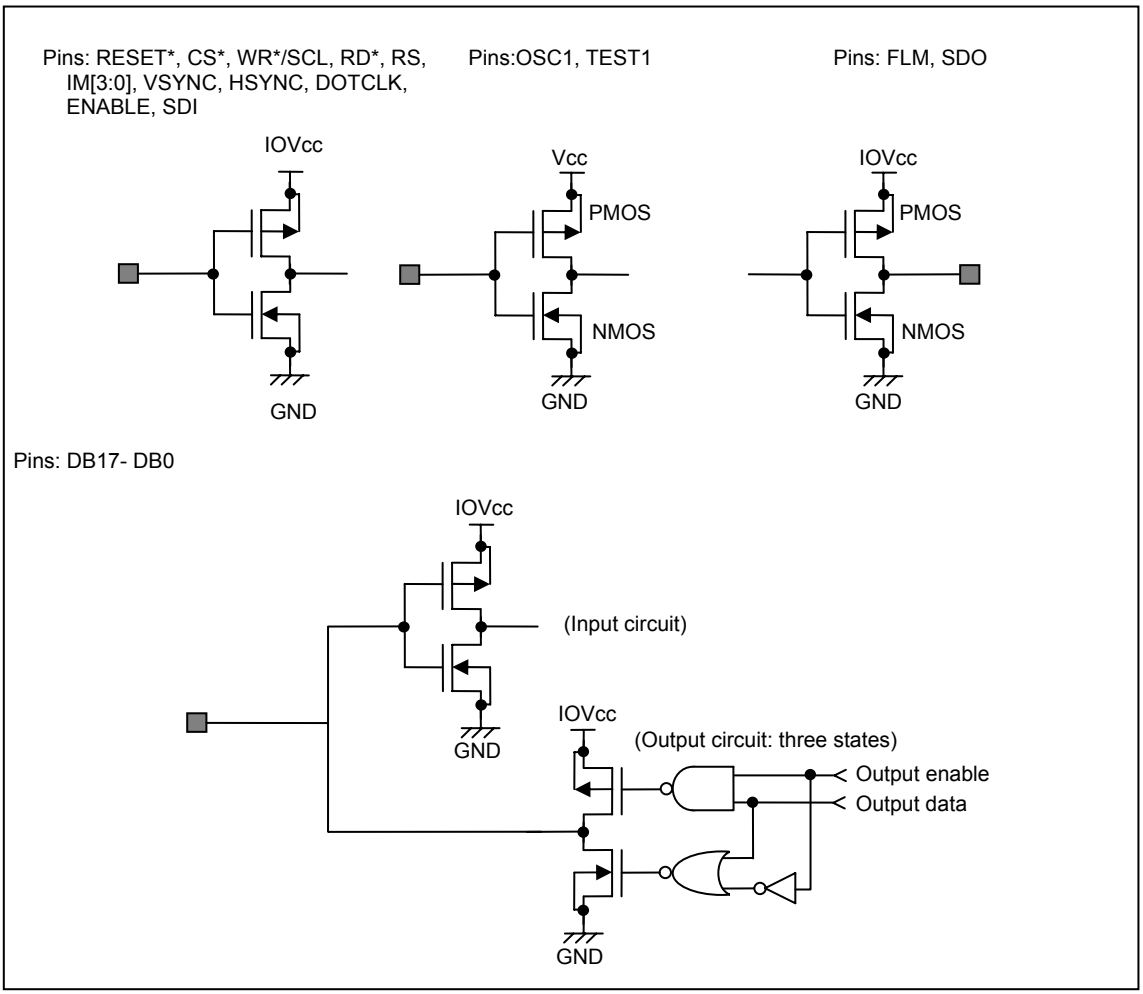


Figure 72

3. The TEST1 pin must be grounded (GND). The IM[3:0] pins must be fixed at either GND or the IOVcc level.
4. This excludes currents though the output drive MOS.
5. This excludes currents flowing through input/output units. Be sure that input levels are fixed to prevent increase in the transient current in input units when a CMOS input level takes medium range. While not accessing via interface pins, current consumption will not change whether the CS* pin is set to “High” or “Low”.
6. This is the case when an external oscillation resistor Rf is used.

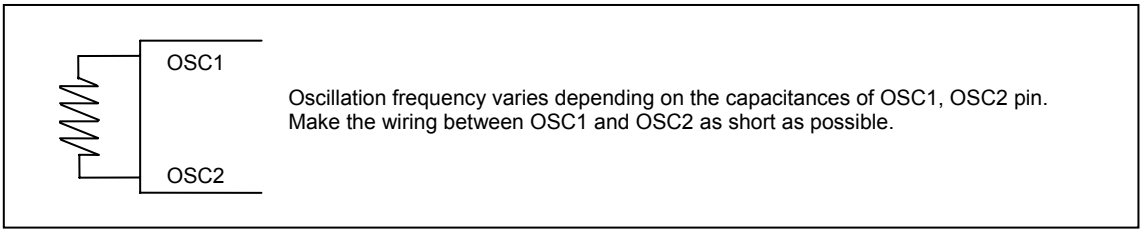


Figure 73

Table 78: Reference Data, Ta=25°C

Oscillation Resistance (kΩ)	RC Oscillation Frequency: fosc (MHz)
	@ VCC = 2.8V
33	1.77
39	1.51
47	1.26
51	1.17
56	1.07
62	0.979
68	0.899
75	0.819
82	0.746
91	0.682
100	0.618
120	0.520
130	0.482

Timing Characteristics Diagram

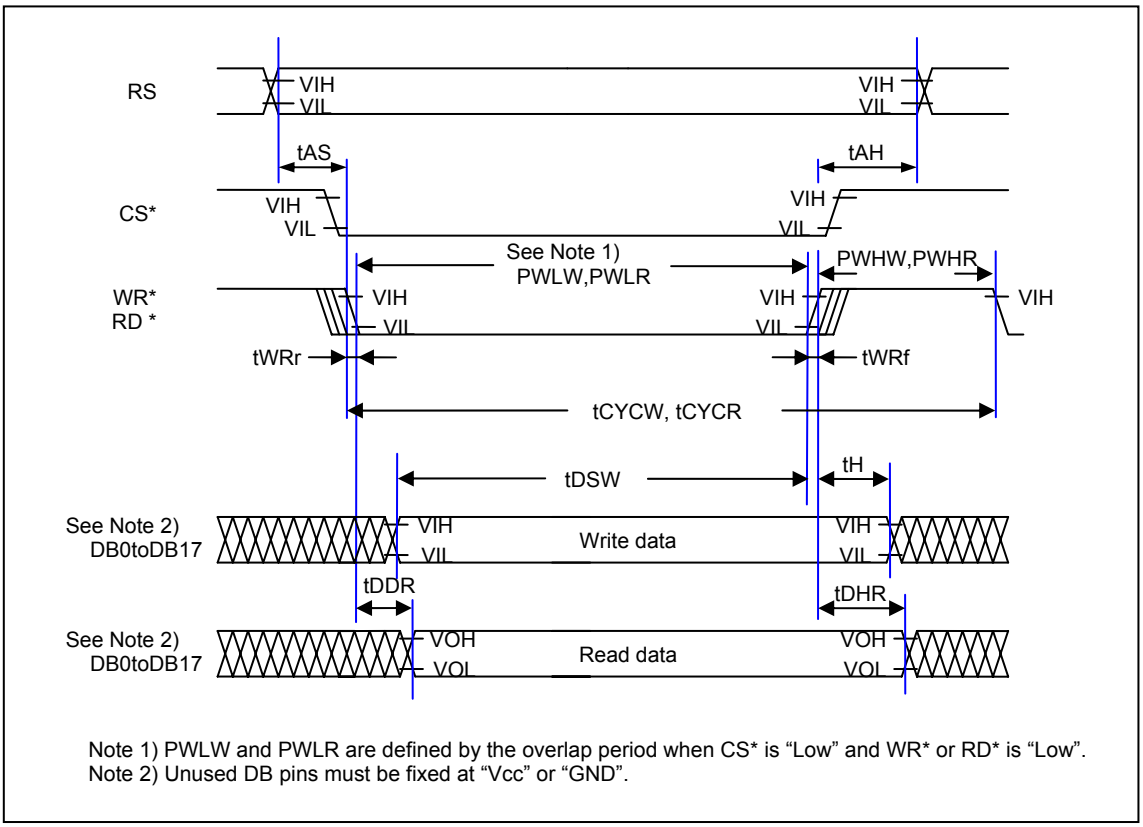


Figure 74: 80-system bus interface operation

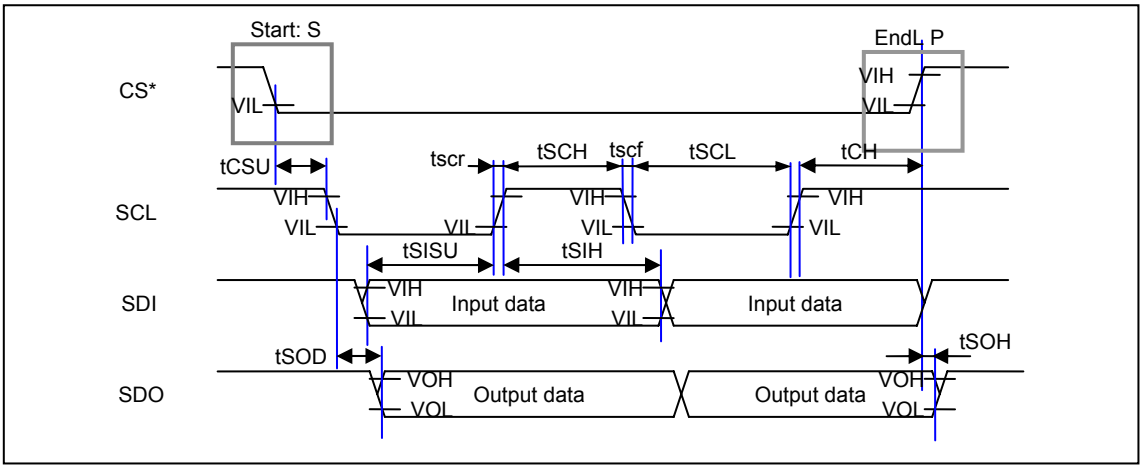


Figure 75: Serial peripheral interface operation

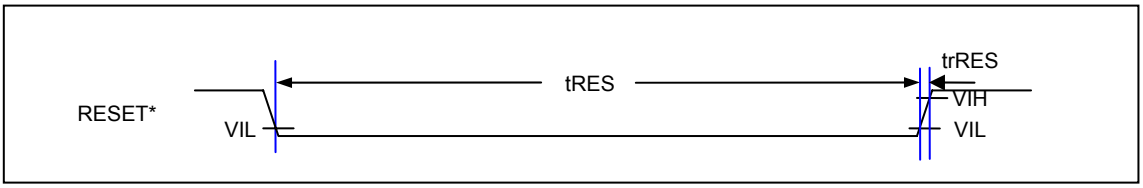


Figure 76: Reset operation

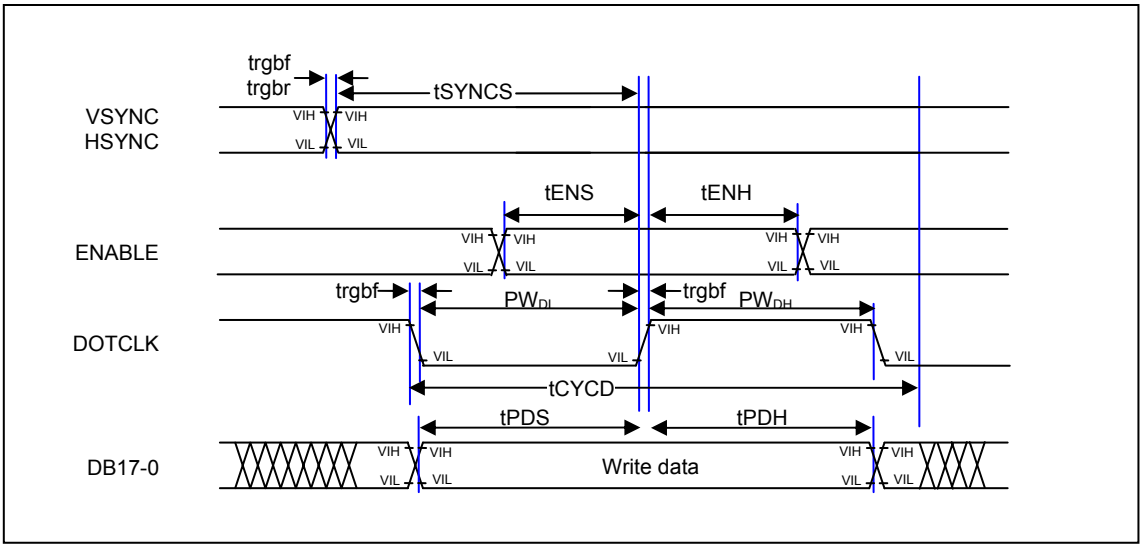


Figure 77: RGB interface

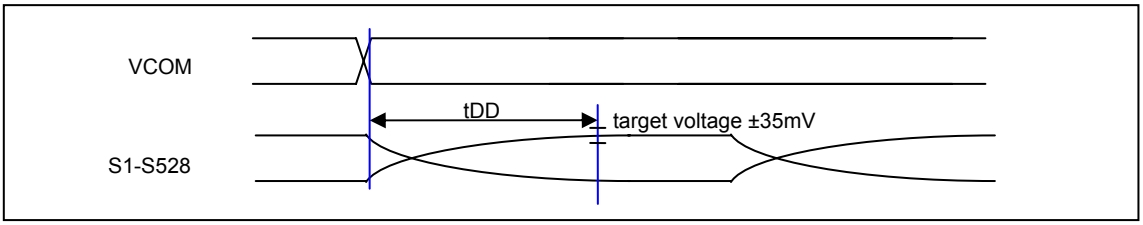


Figure 78: LCD driver outputs