A 17 Gb/s 10.7 pJ/b 4FSK Transceiver System for Point to Point Communication in 65 nm CMOS

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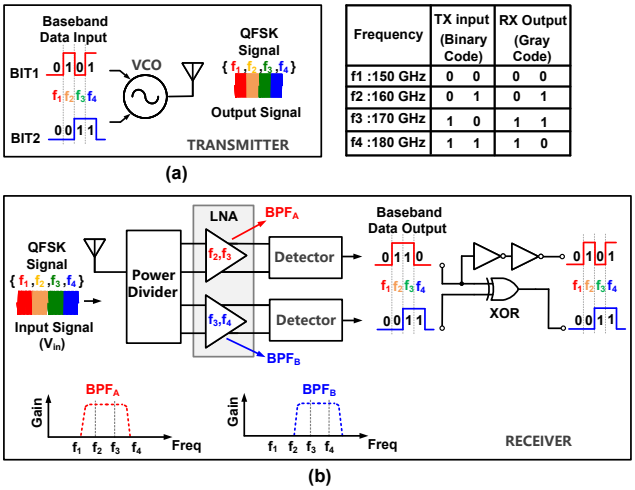
***Abstract*— This paper presents a novel 145-185 GHz transceiver (TRX) with 4 frequency-shift keying (4FSK) modulation. The proposed non-coherent 4FSK design removes the need for separate modulator and demodulator blocks reducing the power consumption and complexity. The proposed TX generates four different RF frequencies based on the two parallel streams of binary input data, and the RX employs a slot power divider to divide the 4FSK RF signal into two paths, where the 4FSK RF signal is demodulated and data is recovered by enveloped detectors and digital buffers. Both the transmitter and receiver are fabricated in a 65 nm CMOS technology with a total core area of 0.6 mm^2. The TRX architecture achieves 17 Gb/s over 18 cm link distance while consuming only 182 mW power.**

***Keywords*— 4FSK modulation, transceiver, CMOS, millimeter wave, data rate**

I. Introduction

Recently, there has been great interest in using millimeter-wave (mm-wave) and Sub-Terahertz (THz) frequency bands for high data rate low power communication systems [1], [2]. Various mm-wave transceivers have utilized digital modulation techniques especially phase-shift keying (PSK), On-Off keying (OOK), and quadrature amplitude modulation (QAM) [3], [4], [5]. A 210-GHz OOK CMOS transceiver that achieves 10 Gb/s at a 3.5 cm distance is presented in [6]. The communication system in [7] achieves 10 Gb/s at a 30 cm distance using QPSK modulation at 60 GHz, while the transceiver in [8] uses 64 QAM modulation to achieve 21.12 Gb/s data rate at 10 cm distance at 60 GHz. Although the reported QAM and PSK TRXs [9] can achieve a multi Gb/s data rate occupying low bandwidth, they suffer from design complexity and high power consumption, because they require coherent architectures. In addition, separate power hungry modulator/demodulator (modem) including data converters are needed in these systems which adds to the power consumption. On the other hand, the OOK [10] systems have simpler structures but can only provide one bit per symbol, limiting the data rate.

Theoretically, the 4FSK modulation scheme is more energy-efficient than OOK and QAM modulations, as it requires less signal-to-noise ratio (SNR) at a fixed bit error rate (BER). In addition, 4FSK modulation scheme can be implemented non-coherently and does not require a separate modem. As a result, the complexity and the power consumption of the system is significantly reduced. Compared to traditional OOK, 4FSK includes two bits per symbol enabling higher data rate systems. Similar to OOK, 4FSK modulation is less bandwidth efficient than PSK/QAM for a specific data rate. Nevertheless, large bandwidths are available at mm-wave frequencies, enabling trade off between bandwidth and power efficiencies.



Frequency	TX input (Binary Code)	RX Output (Gray Code)
f1 :150 GHz	0 0	0 0
f2 :160 GHz	0 1	0 1
f3 :170 GHz	1 0	1 1
f4 :180 GHz	1 1	1 0

Fig. 1. 4FSK transceiver architecture (a) Transmitter (b) Receiver

This work presents a 4FSK TRX at 150 to 180 GHz achieving 17 Gb/s at an 18 cm distance consuming 182 mW in a 65 nm CMOS process. To the best of our knowledge, the proposed design is the first multi Gb/s transceiver based on 4FSK modulation scheme, and achieves the highest energy efficiency for reported TRX systems supporting 17 Gb/s or higher.

II. 4FSK Transceiver Architecture

Fig. 1 presents the conceptual 4FSK TRX architecture. The transmitter consists of only one voltage controlled oscillator (VCO). Two parallel streams of binary data are applied to the input of the transmitter. The VCO generates four different frequencies of f1, f2, f3, and f4 for the input data pairs of (0,0), (0,1), (1,0) and (1,1), respectively. Thus, the transmitter modulates and upconverts the data at the same time resulting in significantly lower power consumption and circuit complexity compared to QAM and PSK transmitters.

Conventional non-coherent 4FSK receivers divide the received signals into four paths for frequency detection. However, four-way power dividers at high frequencies (>100GHz) can be very lossy, increasing the noise figure of the receiver. In addition, four-path receivers are high power consuming. In this design, the 4FSK signal at the RX input is divided into two paths. The LNA in the first path is tuned

2022 IEEE Radio Frequency Integrated Circuits Symposium (RFIC) | 978-1-6654-9611-7/22/$31.00 ©2022 IEEE | DOI: 10.1109/RFIC54546.2022.9863100

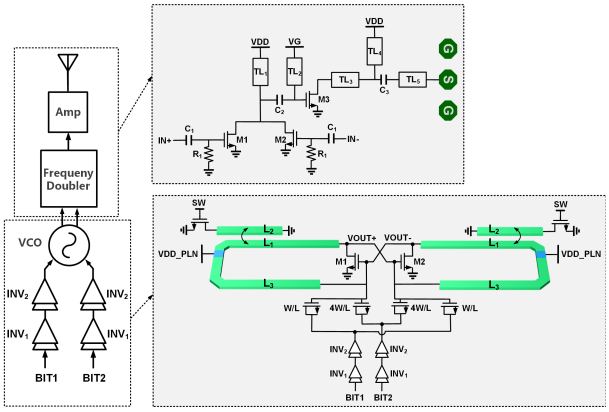


Fig. 2. 4FSK transmitter blocks

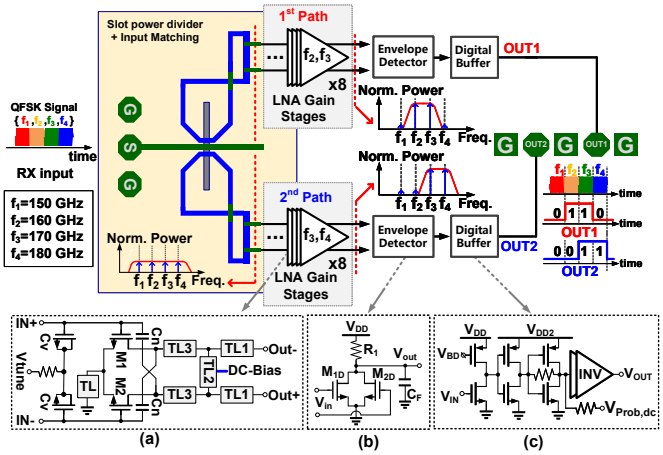


Fig. 3. 4FSK receiver blocks (a) LNA schematic (b) Envelop detector schematic (c) Digital buffer schematic

as a band-pass filter (BPF_A) at f2 and f3 frequencies and the LNA in the second path is tuned as a band-pass filter (BPF_B) at f3 and f4 frequencies. The following detector can detect the power of the signal at the output of the LNA and generate data bits accordingly. For example, if the frequency of the signal at the input of the receiver is f1, the signal is filtered by both paths, and the (0,0) bits are generated at the output of the detector. Similarly, If the input frequency is f2, f3 and f4, the detectors generate (0,1), (1,1) and (1,0), respectively. While the data bits at the transmitter input are binary code, the output of the receiver is gray code. A simple digital logic circuit can be used at the output of the receiver (Fig. 1) to recover the exact bits sent by the transmitter.

The minimum Nyquist bandwidth for a given data rate is fb/2 and the minimum Null to Null bandwidth for zero BER for non-coherent 4FSK modulation is 2.5fb, where fb is the data rate. Thus, for a 20 Gb/s data rate 4FSK modulation, the minimum Nyquist bandwidth is 10 GHz and the Null to Null bandwidth is 50 GHz. In this design f1, f2, f3 and f4 frequencies are 150, 160, 170, and 180 GHz, respectively. That corresponds to 10 GHz spacing between frequencies and 40 GHz of bandwidth. Each stream of binary data is 10 Gb/s which makes the total data rate 20 Gb/s.

III. Circuit Implementation

A. 4FSK Transmitter

Fig. 2 shows the circuit details of the 4FSK transmitter. The VCO is a cross-coupled oscillator which includes two sets of varactors. The voltage across the varactors is controlled by the BIT1 and BIT2 data streams. Therefore, the varactors can provide four distinct capacitances to the cross-coupled VCO. The NMOS varactors are sized such that the VCO's four frequencies are 75, 80, 85, and 90 GHz. The VCO tank inductor contains L1 and L3 transmission lines which are in parallel in the tank. L1 and L2 are coupled and therefore the impedance looking into L1 is a function of the impedance of L2 in series with the switch, SW. The switch can perform fine frequency tuning if the four frequencies are not exactly the required values. A frequency doubler is designed to increase the frequency of the signal at the output of the VCO, and the following amplifier is used to increase its output power. The frequency doubler and amplifier schematic is shown in Fig. 2. The output matching of the amplifier is designed to cover 150-180 GHz bandwidth and to make sure the output power of the signal at all four frequencies is the same. The simulated conversion gain of the frequency doubler followed by the amplifier is -7 dB at 165 GHz.

B. 4FSK Receiver

Fig. 3 shows the circuit blocks of proposed 4FSK direct-demodulation receiver. A slot power divider similar to [11] is used at the receiver input to split the input signal equally between the two paths. To support the 4FSK signal in this design, the receiver should cover the frequencies from 145 GHz to 185 GHz. The slot power divider covers the same bandwidth with a simulated insertion loss of 1.8 dB at 165 GHz. To ensure proper operation of the power divider the input matching of the LNA's first stage is also designed to have the same bandwidth (145-185 GHz). However, subsequent LNA stages cover specific frequency bands: 155-175 GHz for the first path and 165-185 GHz for the second path. Neutralization technique is used at each LNA stage (Fig. 3(a)) to boost the gain of each stage and to better isolate the power divider from the rest of the LNA stages. A transmission line is added to the source of the transistors to provide better stability. The power supply voltage of the LNA is 0.75 V. While larger bandwidth for each path can support higher data speed, it also increases the integrated noise and the leakage of the undesired frequencies, reducing the SNR. Therefore, the optimum bandwidth of the LNA is designed to be around 15 GHz. To compensate for the frequency shifts due to the process variation, NMOS varactors are added at the gate of the transistors in each LNA stage. The maximum simulated NF of the RX path is 15 dB.

The NMOS transistors of the differential envelope detector (Fig. 3(b)) are class AB biased for better sensitivity [12]. The bandwidth of the R_1-C_F lowpass network at the output of the detector is designed to be 25 GHz and to create a balance

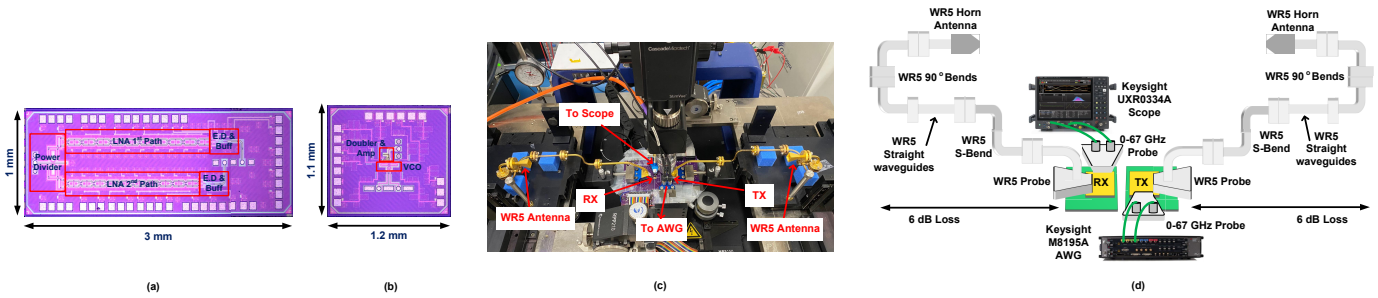


Fig. 4. (a) Chip micrograph of the receiver (b) Chip micrograph of the transmitter (c) Measurement setup picture (d) Measurement setup diagram

Channel	Data Rate	Distance	BER	Eye Diagram
Out 1	15 Gb/s	18 cm	No Error Detected	
Out 2	15 Gb/s	18 cm	No Error Detected	
Out 1	17 Gb/s	18 cm	10^{-12}	
Out 2	17 Gb/s	18 cm	10^{-12}	

(a)

Channel	Data Rate	Distance	BER	Eye Diagram
Out 1	14 Gb/s	28 cm	No Error Detected	
Out 2	14 Gb/s	28 cm	No Error Detected	
Out 1	16 Gb/s	28 cm	10^{-9}	
Out 2	16 Gb/s	28 cm	10^{-10}	

(b)

Channel	Data Rate	Distance	BER	Eye Diagram
Out 1	8 Gb/s	40 cm	No Error Detected	
Out 2	8 Gb/s	40 cm	No Error Detected	
Out 1	10 Gb/s	40 cm	10^{-10}	
Out 2	10 Gb/s	40 cm	10^{-10}	

(c)

Fig. 5. Measured performance of the 4FSK transceiver for different link distances (a) 18 cm (b) 28 cm (c) 40 cm

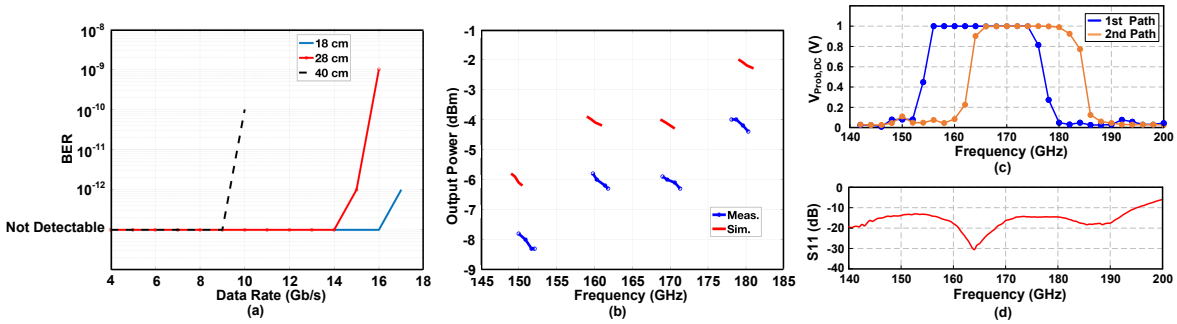


Fig. 6. (a) Measured BER performance versus data rate (b) Output power of the TX (c) Measured normalized gain of the RX (d) Measured S11 of the RX

between data recovery and SNR. Higher bandwidth helps with the data recovery, but at the same time increases the noise, thus decreasing the SNR. The following digital buffers block in Fig. 3(c) is used to amplify the demodulated signal and convert it into digital signals. The first stage of the buffer as a voltage level shifter can be used to tune the threshold of the inverter, calibrating the receiver for different input power levels. The last inverter stage is implemented to drive a 50 Ohm load.

IV. Fabrication and Measurement Results

The circuit was fabricated in a 65 nm CMOS process. Fig. 4(a) and Fig. 4(b) present the chip micrograph of the receiver and transmitter, respectively. The TRX BER measurement was carried out by utilizing the setup shown in Fig. 4(c) and Fig. 4(d). WR5 probes, waveguides, and also 23 dBi horn antennas are used to link the TX and RX chips. The distance between TX and RX antennas can be controlled by changing the length of the straight waveguides. The total loss of the WR5 probe and waveguides is 6 dB for 18 cm distance. Two streams of data bits are generated by a Keysight M8195A arbitrary waveform generator (AWG). The transmitter modulates this data and radiates the signal to the RX chip where the data is demodulated and sent to a Keysight UXR0334A real-time scope for BER measurement.

Fig. 5 presents the measured performance of the 4FSK TRX for different link distances. Data rates of 17, 16, and 10 Gb/s were achieved at 18, 28, and 40 cm link distances, respectively. The BER of the transceiver is calculated based on the measured eye diagram of the demodulated signals. Fig. 6(a) presents the BER versus data rate for different link distances. It can be seen that the BER is 1E-12 at 17 Gb/s, 1E-9 at 16 Gb/s, and 1E-10 at 10 Gb/s for 18, 28, and 40 cm link distances, respectively. Fig. 6(b) depicts the simulated and measured output power of TX for different frequencies which is downconverted by an even harmonic WR5 mixer and measured by an Anritsu MS2830A spectrum analyzer and a VDI Erickson PM4 power meter. To characterize the frequency response of the RX paths, the DC voltage $V_{Prob,dc}$ (Fig. 3(c)), at the output of the inverter-based amplifiers was

Table 1. Performance comparison with State-of-The-Art transceivers

Reference	Frequency [GHz]	Modulation	Integration	Total Antenna Gain [5]	Power Consumption [mW]	Data Rate [Gb/s]	Distance [cm]	BER	Energy Efficiency (TRX) [pJ/Bit]	Core Area [mm^2]	Technology
[3]	60	16 QAM	TX, RX, LO, w/o PLL [1]	PCB 3.5 dBi	TX: 210 RX: 110	27.8	5	0.7E-3	11.5	3.9	65 nm CMOS
[4]	265	16 QAM	TX, RX, LO, w/o PLL [1]	Horn 18 dBi	TX: 890 RX: 897	80	3	1E-3	22.4	NA	40 nm CMOS
[5]	60	BPOOK	TX, RX, LO, Digital IO [2]	Probing	TX: 78 RX: 22	3	NA	1E-3	33.3	1.56	65 nm CMOS
[6]	210	OOK	TX, RX, LO	On-Chip 4.5 dBi	TX: 240 RX: 68	10 [*]	3.5	1E-5	30.8	4.62	32 nm SOI CMOS
[7]	60	QPSK	TX, RX, LO Digital IO, BB [3]	PCB 7 dBi	TX:124, RX:146 Dem:70 [**]	10	30	NA	34	NA	65 nm CMOS
[8]	60	64 QAM	TX, RX, LO [1]	Horn 14 dBi	TX: 169 RX: 139	21.12	10	1E-3	14.58	2.81	65 nm CMOS
[9]	60	64 QAM	TX, RX, LO BB [1]	On-Chip 12 dBi	TX: 670 RX: 431	10.5	100	1E-3	105	NA	28 nm CMOS
[10]	130	OOK	TX, RX, LO, Lens	Package 26 dBi [4]	TX: 59 RX: 38	12.5	500	1E-6	7.76	0.4	55 nm BiCMOS
This Work	**165**	**4FSK**	**TX, RX, Digital IO, Mod, Demod**	**Horn 17 dBi**	**TX: 62 RX: 120**	**10**	**40**	**1E-10**	**18.2**	**0.6**	**65 nm CMOS**
						16	**28**	**1E-9**	**11.37**		
						17	**18**	**1E-12**	**10.7**		

[1] Modulator and Demodulator are not integrated
[2] Requires external oversampling clock
[3] Demodulator is MATLAB Simulink
[4] Antenna in-package with lens
[5] Gain of the antenna minus measurement setup loss
[*] Estimated
[**] Simulation

measured while continuous wave signals with equal power (-17 dBm) but different frequencies are applied to the RX input. Fig. 6(c) shows the normalized gain of the RX paths. The 3 dB bandwidth of both paths is around 20 GHz. In addition, a N5247A PNA-X network analyzer with WR-05.1 VDI frequency extender module are used to measure the return loss of the slot power divider at the RX input, which is shown in Fig. 6(d). The measured return loss at the input port is lower than -10 dB from 140 GHz to 194 GHz.

The performance of the proposed 4FSK TRX is summarized and compared to the state-of-the-art transceivers in Table 1. To the best of authors knowledge, this work presents the first multi-Gb/s TRX system with FSK modulation. The proposed TRX system achieves one of the best energy efficiencies compared to full bit-in-bit-out transceiver works with 17 Gb/s data rate or higher. This work also achieves a higher data rate compared to OOK TRXs.

V. Conclusion

A 4FSK TRX in 65 nm CMOS is presented. The proposed non-coherent design achieves 17 Gb/s at an 18 cm link distance with a 10.7 pJ/Bit efficiency. The design employs a novel 2-path RX and a simple TX architectures and is considered the first multi-Gb/s TRX system with FSK modulation.

Acknowledgment

This work was sponsored by National Science Foundation (NSF). The authors would like to thank Meta.

References

[1] H.-J. Song and T. Nagatsuma, "Present and Future of Terahertz Communications," *IEEE Transactions on Terahertz Science and Technology*, vol. 1, no. 1, pp. 256–263, 2011.

[2] H. Afzal, R. Abedi, R. Kananizadeh, P. Heydari, and O. Momeni, "An mm-Wave Scalable PLL-Coupled Array for Phased-Array Applications in 65-nm CMOS," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 2, pp. 1439–1452, 2021.

[3] S. Daneshgar, K. Dasgupta, and et al, "A 27.8Gb/s 11.5pJ/b 60GHz transceiver in 28nm CMOS with polarization MIMO," in *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, 2018, pp. 166–168.

[4] S. Lee, S. Hara, and et al, "An 80-Gb/s 300-GHz-Band Single-Chip CMOS Transceiver," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 12, pp. 3577–3588, 2019.

[5] Y. Wang, B. Liu, and et al, "A 60-GHz 3.0-Gb/s Spectrum Efficient BPOOK Transceiver for Low-Power Short-Range Wireless in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1363–1374, 2019.

[6] Z. Wang, P.-Y. Chiang, and et al, "A CMOS 210-GHz Fundamental Transceiver With OOK Modulation," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 564–580, 2014.

[7] W. Deng, Z. Song, and et al, "An Energy-Efficient 10-Gb/s CMOS Millimeter-Wave Transceiver With Direct-Modulation Digital Transmitter and I/Q Phase-Coupled Frequency Synthesizer," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 8, pp. 2027–2042, 2020.

[8] J. Pang, S. Maki, and et al, "A 50.1-Gb/s 60-GHz CMOS Transceiver for IEEE 802.11ay With Calibration of LO Feedthrough and I/Q Imbalance," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 5, pp. 1375–1390, 2019.

[9] G. Mangraviti, K. Khalaf, and et al, "13.5 A 4-antenna-path beamforming transceiver for 60GHz multi-Gb/s communication in 28nm CMOS," in *2016 IEEE International Solid-State Circuits Conference (ISSCC)*, 2016, pp. 246–247.

[10] N. Dolatsha, B. Grave, and et al, "17.8 A compact 130GHz fully packaged point-to-point wireless system with 3D-printed 26dBi lens antenna achieving 12.5Gb/s at 1.55pJ/b/m," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 306–307.

[11] H. Bameri and O. Momeni, "A 200-GHz Power Amplifier With a Wideband Balanced Slot Power Combiner and 9.4-dBm P_{sat} in 65-nm CMOS: Embedded Power Amplification," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 11, pp. 3318–3330, 2021.

[12] J. Lee, Y. Chen, and Y. Huang, "A Low-Power Low-Cost Fully-Integrated 60-GHz Transceiver System With OOK Modulation and On-Board Antenna Assembly," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 264–275, 2010.