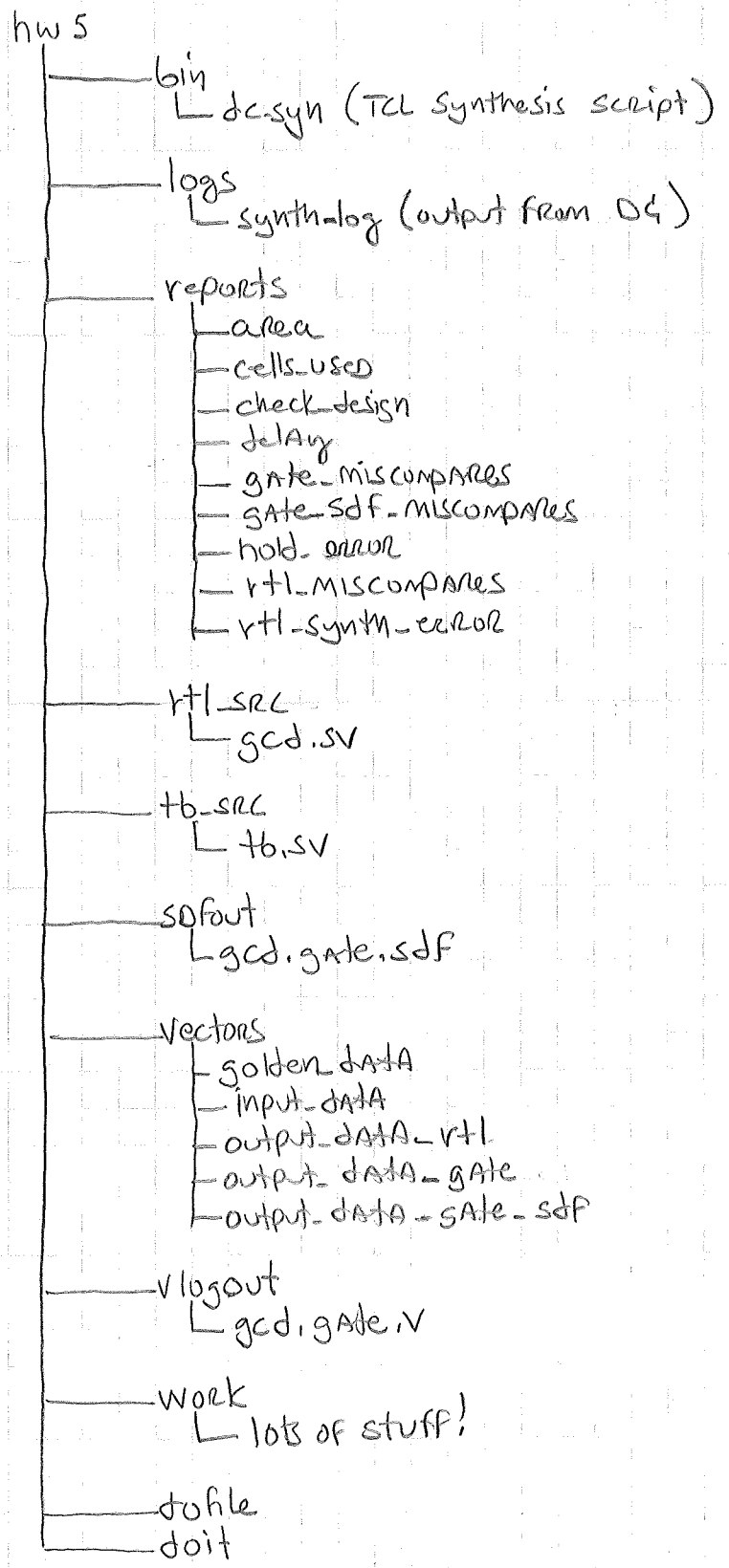
hw5
bin
dc_syn (TCL synthesis script)
logs
synth.log (output from DC)
reports
area
cells_used
check_design
delay
gate_miscompares
gate_sdf_miscompares
hold_error
rtl_miscompares
rtl_synth_error
rtl_src
gcd.sv
tb_src
tb.sv
sdfout
gcd.gate.sdf
vectors
golden_data
input_data
output_data_rtl
output_data_gate
output_data_gate_sdf
vlogout
gcd.gate.v
work
lots of stuff!
dofile
doit