Guokai Chen

Master student at ICT, CAS
chenguokai17@mails.ucas.ac.cn
@chenguokai on GitHub

PROFILE

Highly motivated master student at Institute of Computing Technology, Chinese Academy of Sciences. Skilled in the design of modern out-of-order RISC-V processor with experience in XiangShan team. I will enroll in EPFL EDIC PhD program this fall.

RESEARCH INTERESTS

Computer Architecture, Domain Specific Architecture and Operating System

EDUCATION

University of Chinese Academy of Sciences/Institute of Computing Technology, CAS, Beijing, China - Master of Computer Technology, 2021.9 - 2024.6 (Expected)

University of California, Berkeley, (Remote) - Visiting student, 2020.8 - 2020.12

University of Chinese Academy of Sciences, Beijing, China - Bachelor of Computer Science and Technology, 2017.9 - 2021.6 Ranked 39/112

SKILLS

Familiar with RISC-V and MIPS, modern processors, Linux kernel and Gem 5

Programming languages: C/CPP, Chisel, Verilog, LaTeX, Assembly, Makefile, Markdown, Python and others

TOEFL: 108 (Reading 29 Listening 30 Speaking 22 Writing 27)

AWARDS

1. 2nd Prize on 4th NSCSCC(Loongson Cup), 2020
   - Designed a five-stage pipelined MIPS processor that is capable of running Linux
2. Lenovo master student scholarship, 2022

EXPERIENCES

1. Student of COOSCA (One chip per student) 2nd Gen 2020.8 - 2021.1
2. Teaching Assistant at Introduction to Computer Science 2020.9 - 2021.1
3. Intern at Beijing Institute of Open Source Chips (BOSC) 2022.3 - present
   - **Leader** of the frontend group of XiangShan open source processor
   - Technical representative of BOSC at OpenHW community
   - Implemented oracle branch predictor, indirect branch predictor, loop cache, non-volatile RAS predictor and BPU unit test of XiangShan
   - Implemented indirect branch predictor, non-volatile RAS predictor on Gem 5

- Maintaining Linux kernel, OpenSBI and bare metal device test support

PUBLICATIONS

1. Yinan Xu, ZiHao Yu, Dan Tang, **Guokai Chen** et al, Towards Developing High Performance RISC-V Processors Using Agile Methodology. in 55th IEEE/ACM International Symposium on Microarchitecture(MICRO), 2022.
2. Kaifan Wang, Yinan Xu, Zihao Yu, Dan Tang, **Guokai Chen** et al. XiangShan Open-Source High Performance RISC-V Processor Design and Implementation[J]. Journal of Computer Research and Development, 2023, 60(3): 476-493.

REPORTS

- Performance evaluation tools for XiangShan Processor, RISC-V Summit China 2022
  - The implementation of Oracle Branch Predictor and BPU test framework
- XiangShan Tutorial, RISC-V Summit China 2022
- Kprobe optimization algorithm for RISC architectures, China Linux Kernel Developer Conference 2022
  - Adopt Kprobe jump optimization to RISC architectures
  - Find spare register for jump target storage by analyzing instruction flow data dependency
- Tutorial of Wenquxing (a lightweight Spike NN acceleration instruction set extension based on RISC-V) 2023
- The Evolution of XiangShan (Kunminghu) Frontend, RISC-V Summit China 2023

PATENTS

- CN115629917B, Data recovery method and device, electronic equipment and readable storage medium, **Guokai Chen** and Huaqiang Wang
- CN116048627B, Instruction buffer method, device, processor, electronic equipment and readable storage medium, **Guokai Chen** and Lingrui Gou

OPEN SOURCE PROJECTS

- Open Source Promotion Plan (OSPP) 2020 Port RT-Thread to RISC-V QEMU
  - Outstanding student of the year (**20 out of 151**)
- OSPP 2021 Mentor of Simple-XX community
- OSPP 2022 Optimize Kprobe on RISC-V architecture
  - Reported on China Linux Kernel Developer Conference 2022
  - Outstanding student of the year (**20 out of 350**)
- OSPP 2023 Mentor of Simple-XX community