Pin Information for the MAX®10 10M50SC Device
Version 2017.02.21
Note *(1)*

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 *(2)*
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	6
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	7
1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	8
1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	10
1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	11
1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	12
1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	13
1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	14
1B	VREFB1N0	IO		JTAGEN				15
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L17n	DIFFOUT_L17n	Low_Speed	16
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L17p	DIFFOUT_L17p	Low_Speed	17
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L18n	DIFFOUT_L18n	Low_Speed	18
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L18p	DIFFOUT_L18p	Low_Speed	19
1B	VREFB1N0	IO			DIFFIO_RX_L20n	DIFFOUT_L20n	Low_Speed	20
1B	VREFB1N0	IO			DIFFIO_RX_L20p	DIFFOUT_L20p	Low_Speed	21
1B	VREFB1N0	IO			DIFFIO_RX_L22n	DIFFOUT_L22n	Low_Speed	22
1B	VREFB1N0	IO			DIFFIO_RX_L22p	DIFFOUT_L22p	Low_Speed	23
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L28n	DIFFOUT_L28n	High_Speed	25
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L28p	DIFFOUT_L28p	High_Speed	26
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L36n	DIFFOUT_L36n	High_Speed	27
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L36p	DIFFOUT_L36p	High_Speed	28
2	VREFB2N0	IO	VREFB2N0					29
2	VREFB2N0	IO						30
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L59n	DIFFOUT_L59n	High_Speed	32
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L59p	DIFFOUT_L59p	High_Speed	33
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	38
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	39
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	40
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	41
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	42
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	43
3	VREFB3N0	IO			DIFFIO_TX_RX_B15n	DIFFOUT_B15n	High_Speed	46
3	VREFB3N0	IO	VREFB3N0					44
3	VREFB3N0	IO			DIFFIO_TX_RX_B15p	DIFFOUT_B15p	High_Speed	49
3	VREFB3N0	IO						50
3	VREFB3N0	IO	CLK6n		DIFFIO_TX_RX_B18n	DIFFOUT_B18n	High_Speed	51
3	VREFB3N0	IO	CLK6p		DIFFIO_TX_RX_B18p	DIFFOUT_B18p	High_Speed	52
3	VREFB3N0	IO	CLK7n		DIFFIO_TX_RX_B20n	DIFFOUT_B20n	High_Speed	53
3	VREFB3N0	IO	CLK7p		DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed	55
4	VREFB4N0	IO	VREFB4N0					57
4	VREFB4N0	IO						58
4	VREFB4N0	IO			DIFFIO_TX_RX_B39n	DIFFOUT_B39n	High_Speed	60
4	VREFB4N0	IO			DIFFIO_TX_RX_B39p	DIFFOUT_B39p	High_Speed	61
4	VREFB4N0	IO						62
4	VREFB4N0	IO			DIFFIO_TX_RX_B45n	DIFFOUT_B45n	High_Speed	63
4	VREFB4N0	IO			DIFFIO_TX_RX_B45p	DIFFOUT_B45p	High_Speed	64
4	VREFB4N0	IO			DIFFIO_TX_RX_B49n	DIFFOUT_B49n	High_Speed	65
4	VREFB4N0	IO			DIFFIO_TX_RX_B49p	DIFFOUT_B49p	High_Speed	66
4	VREFB4N0	IO			DIFFIO_TX_RX_B57n	DIFFOUT_B57n	High_Speed	69
4	VREFB4N0	IO			DIFFIO_TX_RX_B57p	DIFFOUT_B57p	High_Speed	70
5	VREFB5N0	IO	RUP		DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	76
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	74
5	VREFB5N0	IO	RDN		DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	77
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	75
5	VREFB5N0	IO			DIFFIO_RX_R29p	DIFFOUT_R29p	High_Speed	82
5	VREFB5N0	IO						80
5	VREFB5N0	IO			DIFFIO_RX_R29n	DIFFOUT_R29n	High_Speed	83
5	VREFB5N0	IO	VREFB5N0					81
5	VREFB5N0	IO			DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	85
5	VREFB5N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	84
5	VREFB5N0	IO			DIFFIO_RX_R32n	DIFFOUT_R32n	High_Speed	87
5	VREFB5N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	86
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R38p	DIFFOUT_R38p	High_Speed	88
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R38n	DIFFOUT_R38n	High_Speed	89
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R40p	DIFFOUT_R40p	High_Speed	90
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R40n	DIFFOUT_R40n	High_Speed	91
6	VREFB6N0	IO			DIFFIO_RX_R42p	DIFFOUT_R42p	High_Speed	92
6	VREFB6N0	IO			DIFFIO_RX_R42n	DIFFOUT_R42n	High_Speed	93
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R50p	DIFFOUT_R50p	High_Speed	96
6	VREFB6N0	IO	VREFB6N0					97
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R50n	DIFFOUT_R50n	High_Speed	98
6	VREFB6N0	IO			DIFFIO_RX_R51p	DIFFOUT_R51p	High_Speed	99
6	VREFB6N0	IO			DIFFIO_RX_R52p	DIFFOUT_R52p	High_Speed	100
6	VREFB6N0	IO			DIFFIO_RX_R51n	DIFFOUT_R51n	High_Speed	101
6	VREFB6N0	IO			DIFFIO_RX_R52n	DIFFOUT_R52n	High_Speed	102
6	VREFB6N0	IO			DIFFIO_RX_R69p	DIFFOUT_R69p	High_Speed	105
6	VREFB6N0	IO			DIFFIO_RX_R69n	DIFFOUT_R69n	High_Speed	106
7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed	110
7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed	111
7	VREFB7N0	IO	VREFB7N0					116
7	VREFB7N0	IO			DIFFIO_RX_T20p	DIFFOUT_T20p	High_Speed	117
7	VREFB7N0	IO			DIFFIO_RX_T20n	DIFFOUT_T20n	High_Speed	118
7	VREFB7N0	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	High_Speed	119
7	VREFB7N0	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	High_Speed	120
8	VREFB8N0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	Low_Speed	123
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T42n	DIFFOUT_T42n	Low_Speed	124
8	VREFB8N0	IO		DEV_OE				125
8	VREFB8N0	IO	VREFB8N0					126
8	VREFB8N0	IO		CONFIG_SEL				128
8	VREFB8N0	IO			DIFFIO_RX_T45p	DIFFOUT_T45p	Low_Speed	127
8	VREFB8N0	Input_only		nCONFIG				130

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 *(2)*
8	VREFB8N0	IO			DIFFIO_RX_T45n	DIFFOUT_T45n	Low_Speed	129
8	VREFB8N0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	Low_Speed	131
8	VREFB8N0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	Low_Speed	132
8	VREFB8N0	IO			DIFFIO_RX_T48p	DIFFOUT_T48p	Low_Speed	133
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T48n	DIFFOUT_T48n	Low_Speed	134
8	VREFB8N0	IO						135
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T50p	DIFFOUT_T50p	Low_Speed	136
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T50n	DIFFOUT_T50n	Low_Speed	138
8	VREFB8N0	IO			DIFFIO_RX_T52p	DIFFOUT_T52p	Low_Speed	140
8	VREFB8N0	IO			DIFFIO_RX_T52n	DIFFOUT_T52n	Low_Speed	141
		GND						3
		GND						79
		GND						4
		GND						95
		GND						68
		GND						59
		GND						56
		GND						48
		GND						142
		GND						137
		GND						121
		GND						115
		GND						112
		GND						104
		VCCIO1A						9
		VCCIO1B						24
		VCCIO2						31
		VCCIO3						54
		VCCIO3						45
		VCCIO4						67
		VCCIO5						78
		VCCIO6						94
		VCCIO6						103
		VCCIO7						113
		VCCIO8						139
		VCCIO8						122
		VCCA1						35
		VCCA2						34
		VCCA3						5
		VCCA3						107
		VCCA4						143
		VCCA5						71
		VCCA6						2
		VCC_ONE						73
		VCC_ONE						72
		VCC_ONE						47
		VCC_ONE						37
		VCC_ONE						36
		VCC_ONE						144
		VCC_ONE						114
		VCC_ONE						109
		VCC_ONE						108
		VCC_ONE						1

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the
MAX 10 FPGA Device Family Pin Connection Guidelines.

(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.

Date	Version	Changes Made
September 2014	2014.09.22	Initial release.
December 2014	2014.12.15	-Updated the BOOT_SEL pin name to CONFIG_SEL pin name. -Removed differential pair pins for non-differential function support.
May 2015	2015.05.08	Added note (2) to Pin List E144.
December 2016	2016.12.23	Removed I/O performance for single-ended pins.
February 2017	2017.02.21	Rebranded as Intel.