**Objectives**

* CMOS Sensor -> FPGA -> Serializer -> Deserializer -> Display on Monitor (Host Computer)
* **Objective #1**: FPGA Schematic → [Luyao Han](mailto:luyao_han@ucsb.edu)
  + *Key result #1:* Determine which blocks (A/B also known as I/O banks) to use (Mar. 25th)
  + *Key result #2:* Wire schematic symbol (Mar. 25th)
    - Python480 → FPGA I/O banks → Serializer
    - Power supply Power regulators
  + *Key result #3:* Find KiCaD symbol/footprints (10M50SCE1448G) file for necessary BANKS only (Mar. 30th)
    - SnapEDA
    - *Note*: There are several variations of the Intel’s FPGA even for the 10M50 family
  + *Key result #4:* Determine if we need an isolated crystal clock (or we can use the clock from the FPGA) for the Python480 (CLK PLL) → [Emmanuel Kayede](mailto:ekayede@ucsb.edu)
* **Objective #2:** New Serializer with MIPI CSI-2 input → [Emmanuel Kayede](mailto:ekayede@ucsb.edu)
  + *Key result #1:* Determine TI-Serializer with MIPI CSI-2 input & high bandwidth
  + *Key result* #2: Design serializer schematic version #2
    - To do: Add Evaluation Steps
* **Objective #3:** PCB Vendor → [Ian Wu](mailto:cheng-yan@ucsb.edu)
  + *Key result #1:* Check if Laritech is a PCB approved vendor for UCSB
  + *Key result #2:* Look for approved PCB vendors
* **Objective #4** VHDL On Development Board→ [Ian Wu](mailto:cheng-yan@ucsb.edu)
  + *Key result #1:* Develop VHDL for capturing image video from camera using MIPI CSI-2
  + *Key result #2:*  Develop VHDL for capturing image video from camera using GPIO
* <https://coda.io/d/MouseCam-Project_dUAaTnJw_Dn/MouseCam-Project_suDY4#_lu-Fz> → Ian
* TO DO:
  + Volume Sketches
  + Evaluation of key results
  + 3) Optional: CAD design
    - Note: Components will be 3D printed