0401 校队 训练 第一次

笔记本：	笔记本
创建时间：	2017/3/23 15:18
更新时间：	2017/3/30 21:07
位置：	四川省, 中国
标签：	笔记, 编程, 电子, 竞赛, 通知

https://github.com/pidan1231239/frequency_control/

@全体成员 开工啦.校队初次训练题按照每个人为单位进行制作，具体题目要求参照群文件《2017初次训练题.pdf》，所用基本元器件由校队统一进行发放。
元件发放时间：3月25日星期六上午9:30~11:30;
元件发放地点：立人楼B306
发放单份元件列表为：
DAC0832×2，TL082×2，DIP20芯片座×2，DIP8芯片座×2，杜邦线20P×1，洞洞板×1,8P拨码开关×1，其他所需电阻电容可在元件发放时间内在B306适量自取。
同时校队提供MSPEXP430F5529LP评估板借用，如有需要，请在该次训练题测评当天及时归还。
另外本次训练题不提供额外的元件申请。

可编程状态变量型低通滤波器

一、任务

使用两片 TL082、两片 DAC0832、一个 8 位的拨码开关和一个按键开关，以及若干的电阻和电容，设计并制作一个可编程的状态变量型低通滤波器，其组成如下图所示。

二、要求

1. 基本要求

滤波器的通带增益为 12dB，截止频率 f_c 在 200Hz~3kHz 的范围内可调，在 $2f_c$ 处滤波器的增益不超过 2dB。f_c 通过拨码开关设置，按键 K 用于对设置进行确认。

2. 发挥部分

在滤波器电路板上增加一个 2.54mm 的 12 针 IDC 插座，电路板通过该插座与单片机连接。一旦连接了单片机，拨码开关和按键开关对滤波器的设置就不再起作用了，而是由单片机来设置滤波器的 f_c 并显示所设置的频率；如果没有连接单片机，则任然由拨码开关和按键开关来设置滤波器的 f_c。

提示：要想办法让拨码开关和按键开关的驱动能力远低于单片机的驱动能力。

三、说明

1. 该题目面向校队的每个队员，也欢迎院队的同学选作；
2. 制作所需元器件由大学生创新基地统一发放；
3. 学生在规定时间内（一周内）完成制作调试，4 月 2 日（星期日）上午 9:30-11:30 交至基地。作品统一到基地测试，由教师给出成绩，具体测试时间稍后通知。

DAC0830 Series Application Hints (Continued)

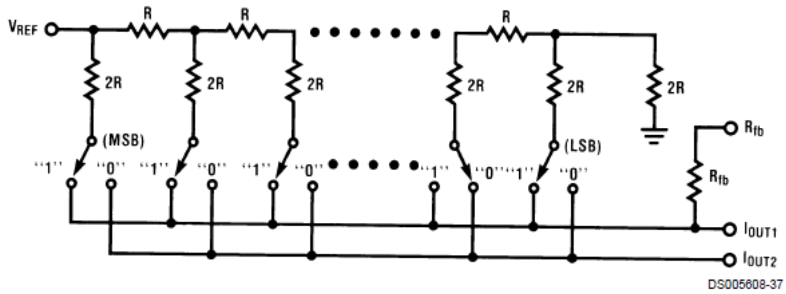


FIGURE 6.

可编程有源滤波器.doc
2017/3/26 11:57, 108 KB

图 9－13 是可编程低通滤波器，基本上是一种 2 阶巴特沃兹滤波器。为使 $Q = 0.707$，反馈放大器的增益 $A = 3-(1/Q) = 1.586$。输入放大器是差动输入型，但任一输入接地均可作为单端输入放大器。滤波器通带增益为 1.586，放大器增益为 0 dB。反馈电阻 $R_3 = 100\ k\Omega/1.586 = 63\ k\Omega$。

采用最容易获得的电容 C_1 和 C_2（0.1 μF），根据最低频率 $f = 10$ Hz 时，计算出电阻 R_0，则 $R_0 = 1/2\pi \times 1 \times 10^{-6} \times 10 = 159.2\ k\Omega$，当频率为 20 Hz 时，$R_0$ 为 10 Hz 的一半，即为 79.6 kΩ；当频率为 40 Hz 时为 39.8 kΩ。设定频率为 30 Hz 时，位 A 和 B 都为低电平，R_0 为 53.33 kΩ。通过设定 A～B 的 1～15 状态，截止频率可在 10 Hz～150 Hz 范围内改变。因要串联模拟开关的导通电阻，为了尽量减小误差，R_0 采用了较高阻值。当 R_0 采用最低阻值为 20 kΩ 时，模拟开关若导通电阻为 50 Ω，则截止频率比计算值低 0.25%。本电路的步进频率为 10 Hz，若步进频率为 100 Hz，电容 C_1 和 C_2 可改为 0.01 μF。

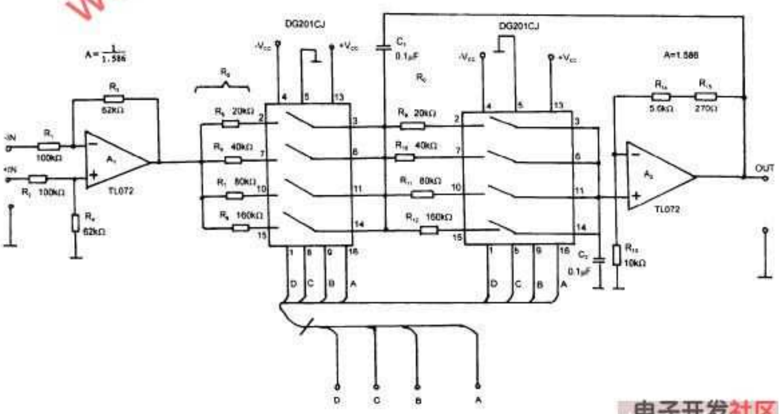


图 9－13 可编程低通滤波器

四、典型D/A转换DAC0832芯片

8位并行、中速(建立时间1us)、电流型、低廉(10~20元)

① 引脚和逻辑结构

② DAC0832与微机系统的连接

③ 应用举例

National Semiconductor

March 2002

DAC0830/DAC0832
8-Bit μP Compatible, Double-Buffered D to A Converters

General Description

The DAC0830 is an advanced CMOS/Si-Cr 8-bit multiplying DAC designed to interface directly with the 8080, 8048, 8085, Z80®, and other popular microprocessors. A deposited silicon-chromium R-2R resistor ladder network divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.05% of Full Scale Range maximum linearity error over temperature). The circuit uses CMOS current switches and control logic to achieve low power consumption and low output leakage current errors. Special circuitry provides TTL logic input voltage level compatibility.

Double buffering allows these DACs to output a voltage corresponding to one digital word while holding the next digital word. This permits the simultaneous updating of any number of DACs.

The DAC0830 series are the 8-bit members of a family of microprocessor-compatible DACs (MICRO-DAC™).

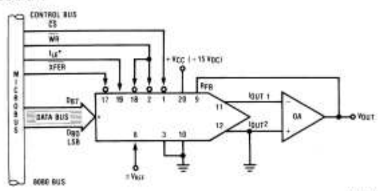
Features

- Double-buffered, single-buffered or flow-through digital data inputs
- Easy interchange and pin-compatible with 12-bit DAC1230 series
- Direct interface to all popular microprocessors
- Linearity specified with zero and full scale adjust only— NOT BEST STRAIGHT LINE FIT.
- Works with ±10V reference-full 4-quadrant multiplication
- Can be used in the voltage switching mode
- Logic inputs which meet TTL voltage level specs (1.4V logic threshold)
- Operates "STAND ALONE" (without μP) if desired
- Available in 20-pin small-outline or molded chip carrier package

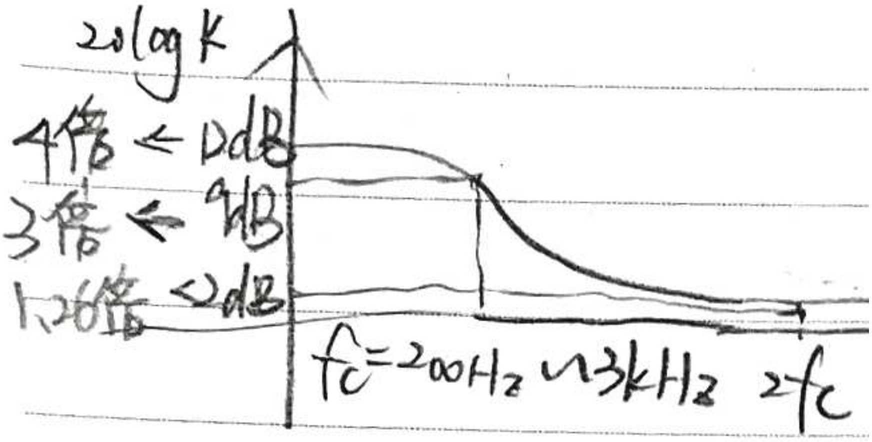
Key Specifications

- Current settling time: 1 μs
- Resolution: 8 bits
- Linearity: 8, 9, or 10 bits (guaranteed over temp.)
- Gain Tempco: 0.0002% FS/°C
- Low power dissipation: 20 mW
- Single power supply: 5 to 15 V_{DC}

Typical Application



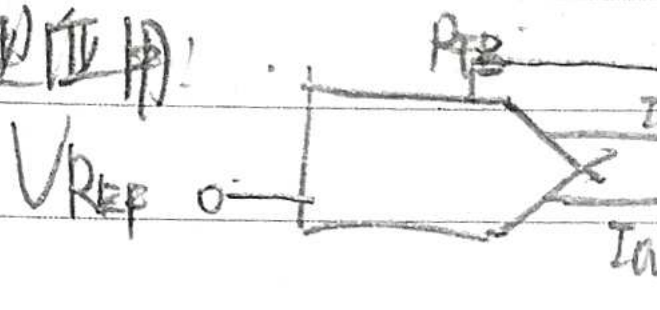
可编程状态变量型低通滤



TL082 双运放 ±18V

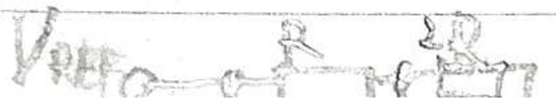
DAC0832 8位 DAC +5V

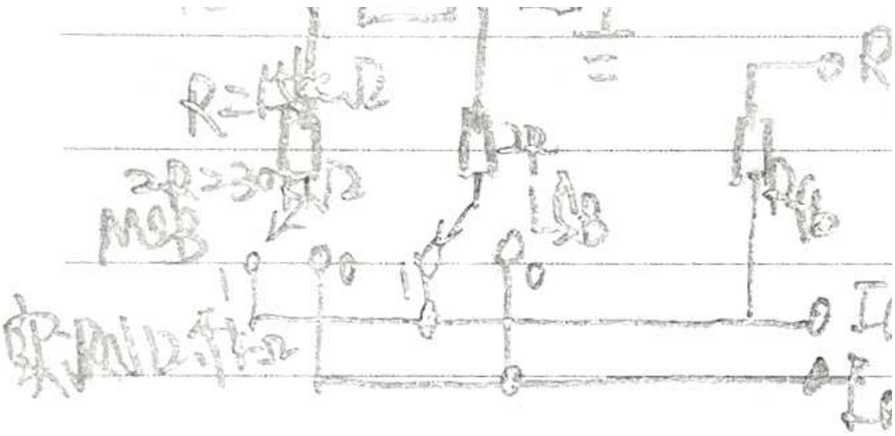
典型应用:



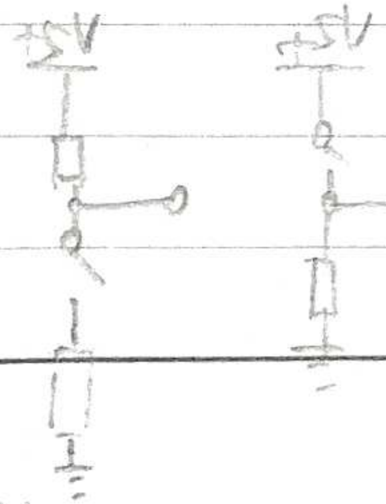
$$I_{OUT1} = \frac{V_{REF}}{15k\Omega} \times \frac{\text{Digita}}{2}$$

$$I_{OUT2} = \frac{V_{REF}}{15k\Omega} \times \frac{255 -}{2}$$





编码开关



ANALOG DEVICES

AN-209 APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

8th Order Programmable Low Pass Analog Filter Using Dual 12-Bit DACs

by Bill Slattery

INTRODUCTION

This application note describes the design of a low pass analog filter whose cutoff frequency can be programmed from 100Hz to 50kHz. The filter is designed as a plug in expansion board for IBM PC AT/XT* or compatibles. A high order filter function is implemented, giving a very fast roll-off in the transition band. This design realizes an 8th order function with a roll-off equalling 48dB/octave. The note also discusses some of the tradeoffs and practical limitations which must be considered when designing a filter.

The design is based on a 2nd order universal active filter, as shown in Figure 1. The required performance is achieved by cascading four of these 2nd order stages.

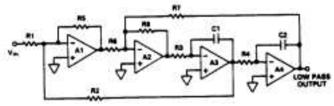


Figure 1. Universal Active Filter

The cutoff frequency of the filter is determined by R3, R4, C1 and C2. Digital control of the cutoff frequency is achieved by replacing resistors R3 and R4 in each stage by CMOS Multiplying Digital to Analog Converters (DACs). The DAC is in effect configured as a digitally programmable resistance.

To have accurate control of cutoff frequency, R3 and R4 within each stage must be closely matched. This is best achieved by replacing these two resistors with a monolithic dual 12-bit DAC. Analog Devices produces a range of suitable dual 12-bit DACs, the AD7537, AD7547 and AD7549. Since these have two DACs on one chip, DAC resistance matching will be in the order of 0.5%. Additionally, the use of 12-bit DACs ensures excellent resolution over the wide range of cutoff frequencies which can be programmed to the filter.

Applications for this filter include Industrial Process Control, Automatic Test Equipment (ATE), Sonar Signal Processing, Instrumentation, Audio Systems and Data Acquisition Systems. In Digital Signal Processing (DSP) applications, it can be used as the front end, low pass, anti-alias filter. 8

THE FILTER FUNCTION

A 2nd order low pass filter function is given by

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{A_O \omega_O^2}{s^2 + \frac{\omega_O}{Q} s + \omega_O^2} \tag{1}$$

where $s = j\omega$

ω_O = 3dB bandwidth (cutoff frequency)

Q = circuit Q factor

A_O = gain at $\omega = \omega_O$

The universal active filter shown in Figure 1 has a 2nd order low pass transfer function given by

$$\frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{\frac{R5\,R8}{R1\,R6}\left(\frac{1}{C1\ R3}\right)^2}{s^2 + \frac{R5\,R8}{R2\,R6}\left(\frac{1}{C1\ R3}\right)s + \left(\frac{1}{C1\ R3}\right)^2} \tag{2}$$

when $R3 = R4$

$R7 = R8$

and $C1 = C2$

By comparing coefficients between Equations (1) and (2) we see that

$$A_O = \frac{R5\,R8}{R1\,R6} \tag{3}$$

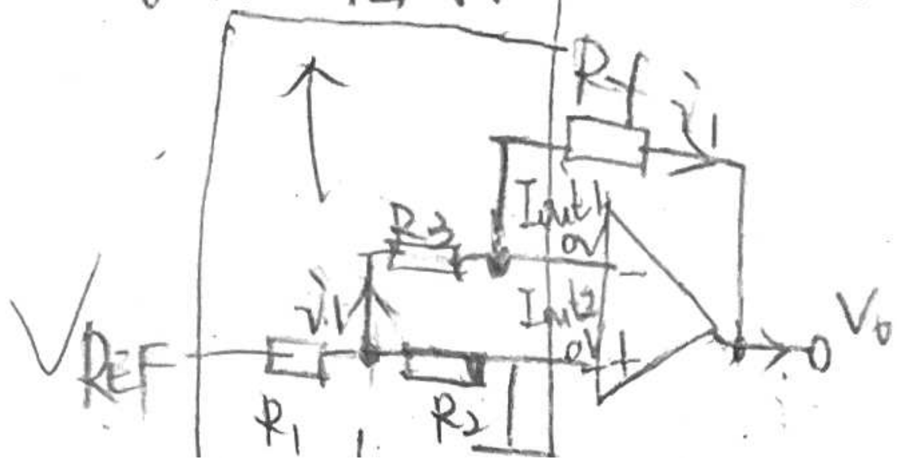
$$Q = \frac{R2\,R6}{R5\,R8} \tag{4}$$

$$\omega_O = \frac{1}{C1\,R3} \tag{5}$$

hence $$f_O = \frac{1}{2\pi\,C1\,R3} \text{ (filter cutoff frequency)} \tag{6}$$

*IBM PC AT/XT is a trademark of International Business Machines Corp.

倒T型电阻网络



$$i_1 = V_{REF}\frac{R_2||R_3}{R_1+R_2||R_3} / R_3$$

$$V_O = -i_1 R_f$$

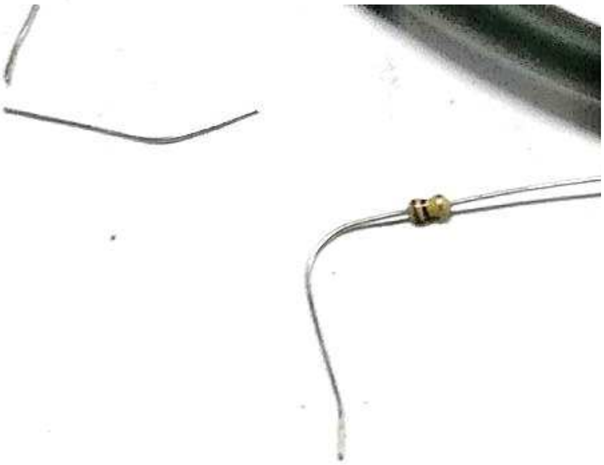
$k=$

$200 \times k=$

$$\frac{0.37}{2\pi \cdot 2k \times 15k \times C} = 200$$

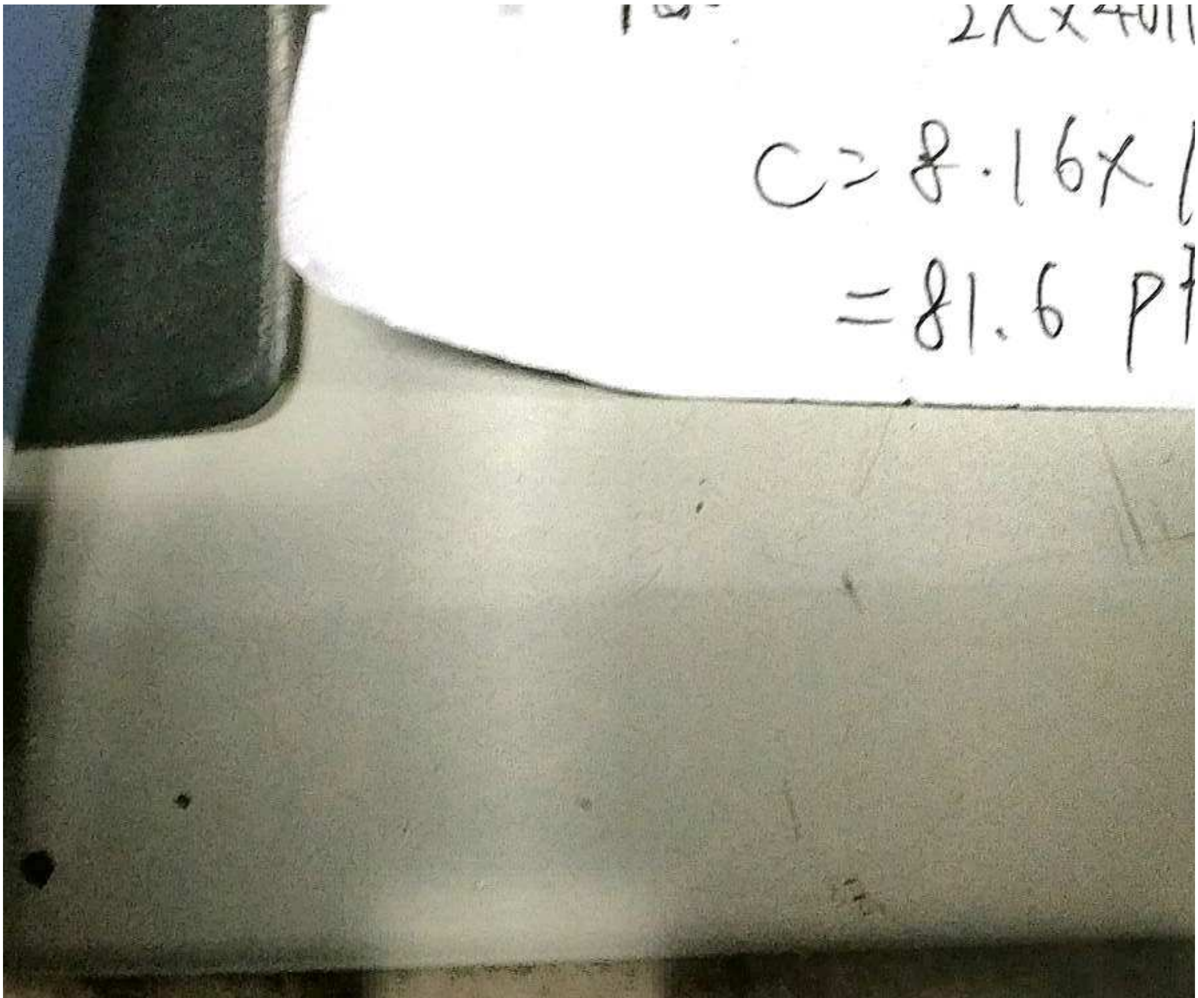
$$C = 7.67 \times 10^{-11}\ F$$

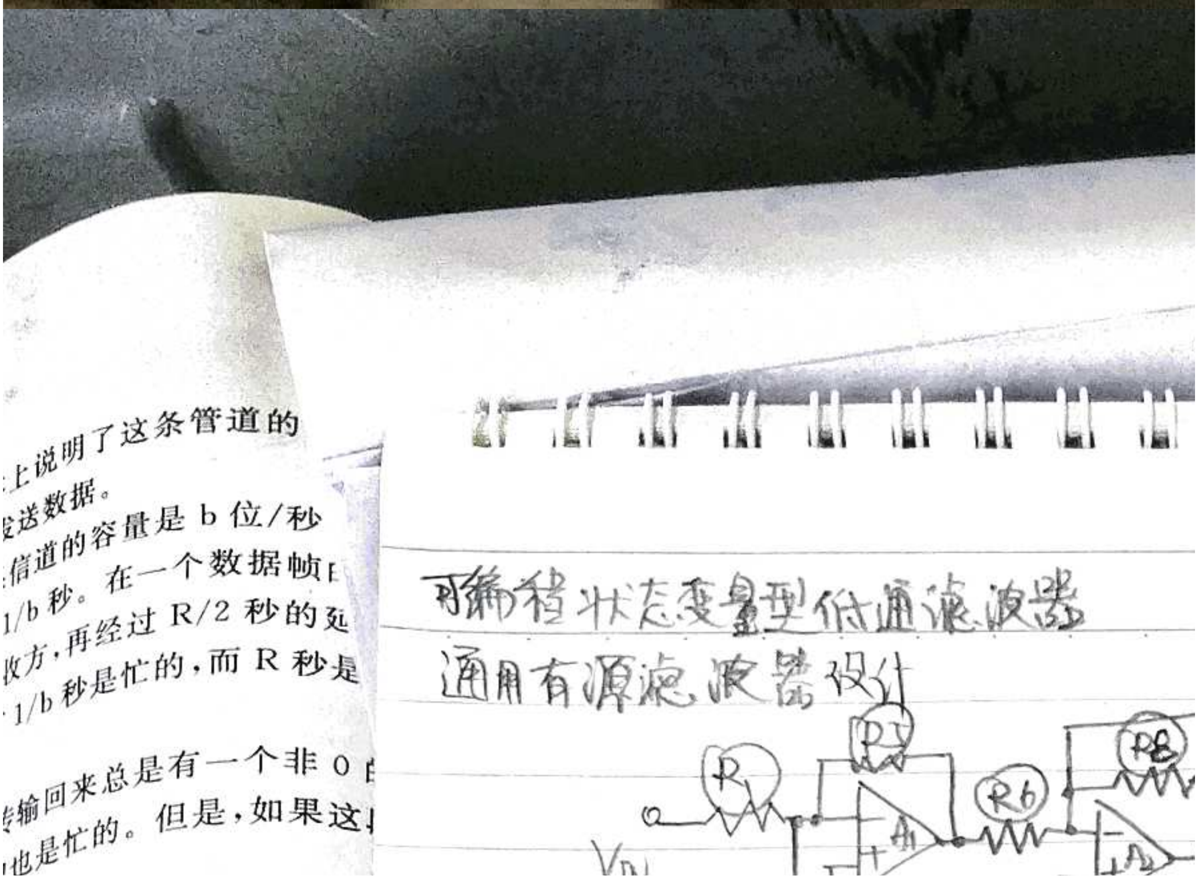
$$= 7.67\ nF$$



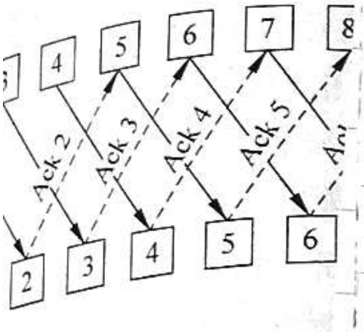
$$f_p = \frac{0.37}{2\pi RC}$$

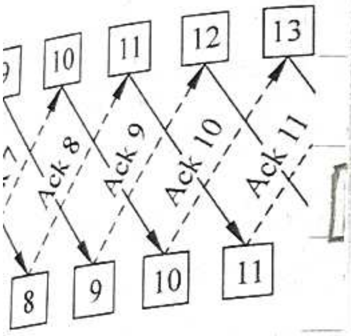
$$180 = \frac{0.3}{\ldots}$$


C=8.16×
=81.6 p


上说明了这条管道的
发送数据。
信道的容量是 b 位/秒
1/b 秒。在一个数据帧
收方，再经过 R/2 秒的
1/b 秒是忙的，而 R 秒是
传输回来总是有一个非 0
也是忙的。但是，如果这
可编程状态变量型低通滤波器
通用有源滤波器设计
R
R7
R6
R8
A1
A2

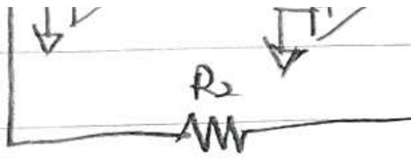
帧也会引起一些严重的问
失了，那该怎么办呢？在
。当一个被损坏的帧到达
后续到达的正确帧呢？前
层。在图 3.16 中，我们
考察这个问题。





果恢复
；(b) 接收方的窗口尺

处理错误。一种方



$A_0 = \frac{R5R8}{R1R6}$ $Q = \frac{R2R6}{R5R8}$

(R3=R4 R7=R8

① $\frac{1}{2\pi C_1R_3} = 200 \sim \boxed{3000}$

$\frac{1}{2\pi C_1 \times 12k} = 3000$, C_1 =

② $A_0 = \frac{R5R8}{R1R6} = 4$ Q

R7 =

R5 = 2k ; R8 = 2k, R

$$f_p = \frac{0.37}{2\pi RC}$$

$$180 = \frac{0.37}{2\pi \times 4011 \times 10^3 \times C}$$

$$C = 8.16 \times 10^{-11}$$

$$= 81.6\ pF$$