Research on Biomedical Engineering
rbejournal.org
Volume , Number , p. ,
DOI: http://dx.doi.org/10.1590/2446-4740.04217

An automatic gain control circuit to improve ECG acquisition

Marco Rovetta[1], João Fernando Refosco Baggio[2], Raimes Moraes[3]*

[1] *Independent scholar, Brescia, Italy.*
[2] *2BiTS, Erbusco, Brescia, Italy.*
[3] *Electrical and Electronic Engineering Department, Federal University of Santa Catarina, Florianópolis, SC, Brazil.*

Abstract **Introduction:** Long-term electrocardiogram (ECG) recordings are widely employed to assist the diagnosis of cardiac and sleep disorders. However, variability of ECG amplitude during the recordings hampers the detection of QRS complexes by algorithms. This work presents a simple electronic circuit to automatically normalize the ECG amplitude, improving its sampling by analog to digital converters (ADCs). **Methods:** The proposed circuit consists of an analog divider that normalizes the ECG amplitude using its absolute peak value as reference. The reference value is obtained by means of a full-wave rectifier and a peak voltage detector. The circuit and tasks of its different stages are described. **Results:** Example of the circuit performance for a bradycardia ECG signal (40bpm) is presented; the signal has its amplitude suddenly halved, and later, restored. The signal is automatically normalized after 5 heart beats for the amplitude drop. For the amplitude increase, the signal is promptly normalized. **Conclusion:** The proposed circuit adjusts the ECG amplitude to the input voltage range of ADC, avoiding signal to noise ratio degradation of the sampled waveform in order to allow a better performance of processing algorithms.

Keywords Biopotential amplifier, QRS detection, Amplitude normalization, AGC, SNR.

Introduction

Discrete-time signal processing techniques are commonly applied to electrocardiogram (ECG) signals in order to obtain indices to assist diagnosis of cardiopathies and sleep disorders. The performance of such techniques is highly affected by the signal to noise ratio (SNR) of the sampled signals (Elgendi et al., 2014). However, ECG usually contains interferences caused by electromyogram and power lines. Instrumentation amplifier, driven-right-leg circuit, and filtering are widely employed in ECG amplifiers to attenuate such noise (Webster, 2010). Even though, devices for long term ECG monitoring require improvements to measure discernible QRS and P waveforms in the presence of noise (Lobodzinski and Laks, 2012). The inter-individual variability of ECG amplitude also has impact on the quality of sampled signals. A low amplitude signal, when compared to the input range of analog to digital converters (ADCs), has a poor quantization, reducing the SNR (Oppenheim and Schafer, 2010). In order to improve that, ECG amplifiers usually have their gain manually adjusted for each subject and each lead. During long-term acquisition, intra-individual variability of ECG amplitude is also observed, mainly as consequence of electrolyte drying or electrodes displacement. To circumvent that, techniques to modify the amplifier gain during ECG acquisition have been proposed (Jha et al., 2015; Komorowski et al., 2013; Romero et al., 2012; Yamakawa et al., 2012). This work describes a simple electronic circuit to automatically adjust the highest magnitude wave of the ECG to the ADC input range in order to improve resolution and avoid saturation. Example of ECG amplitude adjustment is presented. The proposed circuit contributes to obtain better quality ECG recordings.

Methods

The proposed circuit aims to normalize the ECG amplitude by its highest magnitude wave (usually, the R wave) during each cardiac cycle, according to:

$$V_{norm} = -K \frac{V_{in}}{|V_{peak}|} \quad (1)$$

where K is a scaling constant related to component used in the circuit, $|V_{peak}|$ is the absolute peak voltage of the

How to cite this article: Rovetta M, Baggio JFR, Moraes R. An automatic gain control circuit to improve ECG acquisition. Res Biomed Eng. *;* :. DOI: 10.1590/2446-4740.04217.

**Corresponding Author:* Electrical and Electronic Engineering Department, Federal University of Santa Catarina, Rua Delfino Conti, s/n, Trindade, CEP 88040-900, Florianópolis, SC, Brazil. E-mail: raimes@eel.ufsc.br

Received: 24 July 2017 / *Accepted*: 29 October 2017

$$Vout = Vin\frac{R3}{R1+R2+R3} \quad (5)$$

The circuit works as balanced full-wave rectifier after making the gain of the inverting amplifier equal to the resistive divider, that is:

$$\frac{R2}{R1} = \frac{R3}{R1+R2+R3} \quad (6)$$

Using the resistors values shown in Figure 2 ($R2/R1 = 1/2$), the full-wave rectifier halves the amplitude of the ECG ($V_{out} = |V_{in}|/2$). The peak value of this rectified signal ($V'_{out} = |V_{peak}|/2$) is used as input of the analog multiplier instead of $|V_{peak}|$ in Figure 1. For this particular case, Equation 1 becomes:

$$V_{norm} = -K\frac{V_{in}}{\frac{|V_{peak}|}{2}} = -2K\frac{V_{in}}{|V_{peak}|} \quad (7)$$

This is not a drawback since the voltage output will be adjusted by the analog divider, as discussed later on.

The peak detector works as a voltage follower when the input is above the value hold by the capacitor *C1* (Figure 2b); the diode *D2* is forward biased and *C1* is charged by the op amp *OP2*. The negative feedback takes into account the capacitor voltage to compensate the voltage drop across *D2* When the input is below *C1* voltage, *D2* is reverse biased and the capacitor holds its charge since there is no leakage current through the high impedance inputs of *OP2* and *OP3*. However, a discharge resistor (*R4*) is placed in parallel to the capacitor *C1* in order to allow V_{norm} to adapt to an ECG amplitude reduction. Between two successive ECG peaks, the diode *D2* is non-conductive and the capacitor *C1* slowly discharges through the resistor R4, until a new peak voltage (above *C1* voltage value) recharges the capacitor. If there is a decrease of the ECG amplitude, the capacitor *C1* keeps discharging through *R4* until its voltage reaches the new peak value. There is a trade-off related to the time constant of the peak detector ($\tau = C1*R4$); the capacitor *C1* has to keep its voltage value as constant as possible along a cardiac cycle in order to obtain a suitable normalization of the waveform by the analog divider. On the other hand, if the time constant is too large, the capacitor discharges very slowly and the proposed circuit will have a large recovery time to adapt to the ECG amplitude decrease. The voltage follower built with OP3 avoids the discharging of *C1* through the multiplier input impedance; its removal reduces the number of required circuit parts, but the time constant (τ) of the peak detector will change, depending on the input impedance of the used multiplier.

As shown in Figure 2, the analog divider (Figure 1) has *R5* (100kΩ) and *R6* (7.5kΩ) as input and feedback resistors, respectively. Since they do not have the same value, as initially proposed in Figure 1, an additional modification is introduced to Equation 7:

$$V_{norm} = -2\frac{R6}{R5}K\frac{V_{in}}{|V_{peak}|} = -(0.15)K\frac{V_{in}}{|V_{peak}|} = -1.5\frac{V_{in}}{|V_{peak}|}Volts \quad (8)$$

Observing that the scaling constant (*K*) of the multiplier (AD633) is 10. Therefore, the proposed circuit restrains the ECG amplitude between -/+1.5V, since the maximum absolute value of V_{in} is $|V_{peak}|$. This voltage range was chosen because microcontrollers are very often used to digitize analog signals and handle the digital samples (for instance, process, store or transmit digital data to a remote computer); for such purpose, many microcontrollers have ADC built-in. Typically, the maximum input voltage of such ADCs is close to 3V. Equation 1 shows that the analog divider inverts the normalized signal. The last circuit block, the inverting summing amplifier (Figure 2c), has the task to invert back the normalized ECG while adding a DC offset (1.5V) to the ECG signal such that its amplitude spans the range from 0 to 3V (typical ADC input voltage range of microcontrollers).

A capacitor (*C2*) inserted between ground and the virtual ground of *OP4* removes high frequency switching noise generated by the AD633.

Results

An example of the circuit behavior is shown for a simulated ECG (corresponding to a 40bpm heart rate) which has a sudden 50% drop of its R wave amplitude (Figure 3). Such slow heart rate was chosen because the required time constant (τ) to keep the peak detector voltage suitably constant between two R waves has impact on the recovery time of the ECG amplitude. The ECG signal was generated by means of a digital to analog converter belonging to a commercial microcontroller development board (STM32F429I-DISCO – STMicroelectronics). The simulated ECG was filtered (0.05 to 150Hz - circuit not shown). Figure 3 shows the simulated ECG and the peak detector output ($|V_{peak}|/2$); while the R waves keep their amplitudes in 3V, the peak detector output has a 200mV drop along an interval of 1.5s. After a 50% drop of R wave amplitude, the capacitor *C1* keeps discharging through *R4* until it reaches its new peak value, corresponding to the new R wave amplitude. For a sudden amplitude increase, the peak detector promptly holds the new voltage value, avoiding saturation of the ADC.

In order to keep the ECG amplitude relatively constant for a heart rate as low as 40bpm, the time constant of the peak detector was chosen to be equal to 10s. In this case, the recovery time for a sudden amplitude drop of

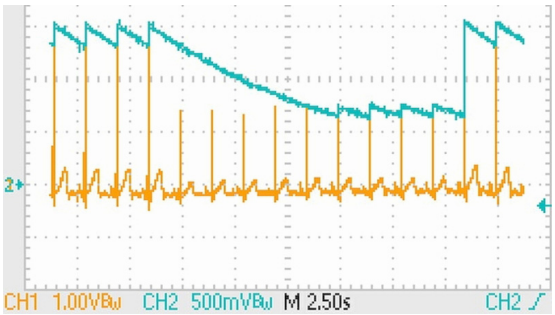

Figure 3. Simulated ECG (0.05-150Hz) and the output of the peak detector sampled by a dual channel oscilloscope (Tektronix – TDS2002C). As the rectifier circuit halves the amplitude of the ECG, the voltage scale of the channel 1 is twice (in terms of volts per division) that of the channel 2 to allow the superposition of the two curves. After few cycles, the simulated ECG amplitude was halved; the voltage across the capacitor of the peak detector drops exponentially until it reaches the new peak value.

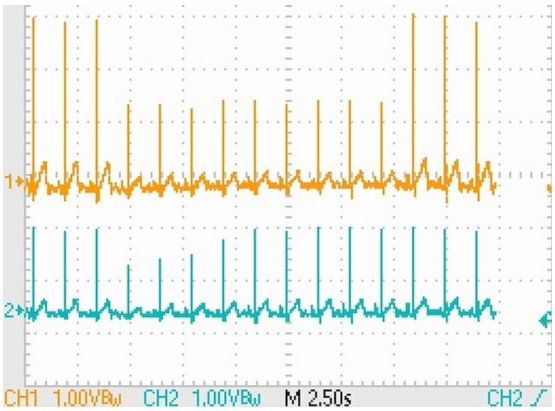

Figure 4. Simulated ECG (0.05-150Hz) and the output of the proposed circuit (AC coupling). After the sudden drop of the ECG amplitude, the circuit starts increasing its gain to recover the ECG amplitude; that is accomplished when the peak detector achieves the new peak value.

50% is close to 7s, taking about 5 cardiac cycles for a 40bpm heart rate (Figure 4).

The values of *C1* and *R4* may be chosen to make the peak detector output steadier along the cardiac cycle; on the other hand, the amplification of the ECG to compensate an amplitude drop will be slower, recalling that a 40bpm heart rate corresponds to bradycardia.

Discussion

A common approach for automatic gain control (AGC) of ECG involves a microcontroller that samples the highest amplitude of each ECG cycle and verifies if it is close to the ADC full-scale input range; if not, the amplifier gain of an analog front end is modified to regulate the amplitude. A peak detector has been used to obtain the highest amplitude value of each ECG cycle. The amplitude adjustment depends on the amplifier design being usually digitally controlled; therefore, the amplifier gain has discrete resolution (Komorowski et al., 2013; Romero et al., 2012; Yamakawa et al., 2012). Cascade of digitally controlled amplifiers may be used to reduce the gain step (Komorowski et al., 2013). Algorithm executed by the microcontroller analyzes the peak amplitude of each cardiac cycle and modifies the amplifier gain taking into account its gain step.

Instead of a microcontroller, Jha et al. (2015) used a digital decoder modeled as a Moore machine in their AGC that is part of an analog front end implemented in 0.18µm CMOS technology. This AGC has also a peak detector and a comparator to assess the amplitude range. Based on the comparator output, the decoder generates a digital value to modify the amplifier gain if necessary.

The response time of each proposed method may be affected by the amplitude variation (ΔV), heart rate (RR interval), algorithm, and maximum error after adjustment. However, the referred works did not provide enough information on such aspects to allow their comparison. Some figures are here presented to give a general idea about their performance. Komorowski et al. (2013) reported that their AGC takes about 15 seconds to achieve a stable output for a three-fold increase of ECG amplitude; for a five-fold decrease of amplitude, a steady output is reached after 10 seconds. Yamakawa et al. (2012) stated that their implementation adjusts the amplitude in 10 seconds. These two works did not mention if the heart rate has impact on the response time. Romero et al. (2012) informed that the response time of their circuit depends on the peak detector time constant. Jha et al. (2015) did not report the response time. Since the employed amplifiers have discrete steps of gain, the amplitude adjustment may not always achieve an optimal normalized value. However, such aspect was not characterized in the different works.

The response time of the AGC here proposed is related to the exponential voltage decay of the RC circuit belonging to the peak detector ($\tau = 10$ s). For any heart rate, the response time would be 16s for an amplitude decrease of 80%. The output is promptly normalized if the ECG amplitude increases (Figure 4). These results can be readily compared to those presented elsewhere (Komorowski et al., 2013).

The described AGC circuit has advantages when compared to other techniques since it can be implemented using commercial ICs without requiring processing time from a microcontroller. Besides, the adjusted amplitude is not constrained by discrete steps of gain.

The ICs used in this implementation can be replaced by other commercial parts according to the needs of a specific design in terms of cost, power consumption, and available voltage sources.