Hanzhi Chen

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Education

Nanyang Technological University Singapore, Singapore

M.S. Signal Processing; ***GPA: 3.81/5.00*** *Aug. 2021 – Jun. 2022*

Main Courses: Digital Communication System, Advance Digital Signal Processing, Video Signal Processing, Probability and Random Processes, System Analysis(Optimization course), Genetic Algorithms and Machine Learning, Distributed Multimedia Systems, Image Analysis and Pattern Recognition.

University of Electronic Science and Technology of China Chengdu, China

B.Eng. Electronic Information Engineering; ***GPA: 3.67/4.00*** *Sep. 2017 – Jun. 2021*

Main Courses: Signals and Systems, Digital Signal Processing, Digital Image Processing, Random Signal Analyse, Modern Communication Principles and Technology, Information Theory and Coding of Information, C Programme, Basic Technology of Software, Electronic Circuits and Circuit Analyse, Design and Application of Digital Logic, etc

Publications

"A Novel Low Channel Resistance LDMOS with Planar and Trench Gates." 2019 IEEE International Conference on Integrated Circuits, Technologies and Applications (ICTA) 13-15 Nov. 2019.

"Simulation Study on Novel High Voltage Transient Voltage Suppression Diodes." 2019 International Conference on ASIC (ASICON) 20 Oct.-1 Nov. 2019.

"Self-biased split gate trench type power MOSFET device." C.N. Patent CN110739345A, and issued Mar. 30th 2021.

"High-voltage transient-voltage suppression diode." C.N. Patent CN110504324A, and issued Jun. 1st 2021.

Research Experience

CUHK-SZ, Shenzhen Research Institute of Big Data Advisor: Dr. Guangxu Zhu

Research Assistant *May. 2023 – Now*

Project I: Modeling and Optimization of 5G Network Performance.

- Proposed a diffusion based method to model 5G cellular wireless communication channel for localized channel modeling so that local radio propagation characteristics can be captured.
- Modeling network performance using modeled wireless channels and other information from base station side for downstream optimization.
- This project is part of the SRCON (Digital Twin network optimization system) project led by Zhi-Quan Luo, an academician of the Chinese Academy of Engineering.

Project II: Multi-modal robust edge AI over noisy channel.

- Proposed a method to improve the robustness of edge AI scenarios by utilizing overlapped information from sources of different modalities.

HKUST, Smart Mobility Lab Advisor: Prof. Sisi Jian

Graduate Research Assistant *Sept. 2022 – Apr. 2023*

Project I: Integration of passenger and freight flow under stochastic demand.

- Applying stochastic programming algorithms to model the real-world decisions.
- Introduce two-stage decomposition to decompose strategic and operational decisions.
- Solve plans benefiting all participants in the proposed transportation scheme.

NTU Singapore, Rapid-Rich Object Search (ROSE) Lab Advisor: Prof. Kot Chichung, Alex

Master Dissertation *Aug. 2021 – Jun. 2022*

Project I: Deep Learning-Based Fake News Detection.

- Research on context-based detection methods for AI-generated news.
- Fine-tuning large language model (BERT) to include background information.
- Implementing various models on popular datasets and apply cross comparison.

UESTC, School of Information and Communication Advisor: Prof. Shuyuan Zhu

Bachelor Dissertation *Nov. 2020 – Jun. 2021*

Project I: Object detection of low-quality images.

- Applying enhancement algorithms for images shot under bad illumination conditions and compressed images.
- The proposed method is verified for images in both scenarios and the detection accuracy has been improved by 5%.

UESTC,State Key Lab of Electronic Thin Films & Integrated Devices Advisor: Prof. Moufu Kong

Graduate Research Assistant *Nov. 2018 – Jun. 2020*

Project I: A novel self-biased split-gate trench power MOSFET device.

- Propose a novel structure for MOSFET Device which could supply biased voltage to split-gate within device.
- Run simulation to test proposed structure in circuit-level and device-level.
- This work has been authorised for China patent.

Project II: High-voltage transient-voltage suppression diode.

- Run simulation to verify the feasibility of proposed method.
- This work has been published in ASICON 2019 and authorised for China patent.

Project III: LDMOS with low channel resistance.

- Propose part of LDMOS device structure and run simulation to verify the feasibility of proposed method.
- This work has been published in ICTA 2019.

Awards

Model Student Scholarship in Academic Year 2019-2020

Outstanding Member of Library Student Council in Academic Year 2018-2019

Outstanding Student Scholarship in Acedemic Year 2018-2019

Outstanding Member Scholarship of Summer Oversea Programs in 2018

Skills & Interests

Programming: C, Python, MATLAB and Pytorch

Language Proficiency: Mandarin Native Speaker, IELTS - 6.5, CET6 - 540, CET4 - 567

Leadership: Team leader of UESTC for summer program in Oxford

Music: Chinese flute player, got the Third Prize of Lyrics Contest

Sports: Swimming, badminton and jogging