Postlab for Lab 10

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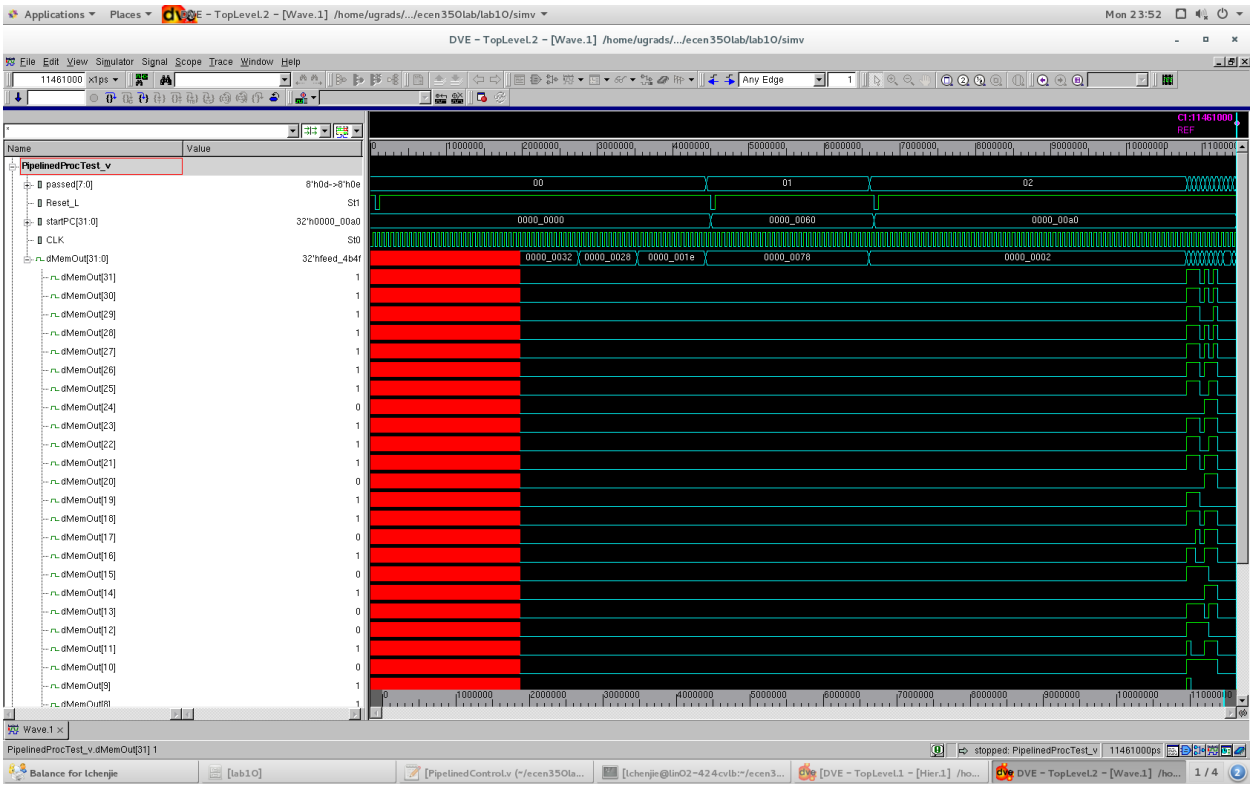

For this lab, our purpose is to design a pipelined processor. And the sample programs we tested were actually the same as lab 9. The main difficulty I think in this lab is Hazard detection. The basic idea in this part is we build a finite state machine. The machine should contain No Hazard state, 2 bubble states, 1 Jump stage and 3 Branch states. The reason why we need three branch states is in this lab we don't change the stage function of each stage and no forwarding unit. Thus, branch being taken or not will be decided at the beginning of MEM stage. Three cycles will be needed in this case. As for bubble stages, that's for dealing with the data hazard. If $rd in mth instruction will be needed in (m+1)th instruction, there should be two cycles of stalls. Similarly, if (m+2)th instruction will need the data, only one stall will be needed. In other cases, there should not have any data hazard.