ECEN 714 Lab 10
Chenjie Luo

1. **Total Wirelength = 13718 um**

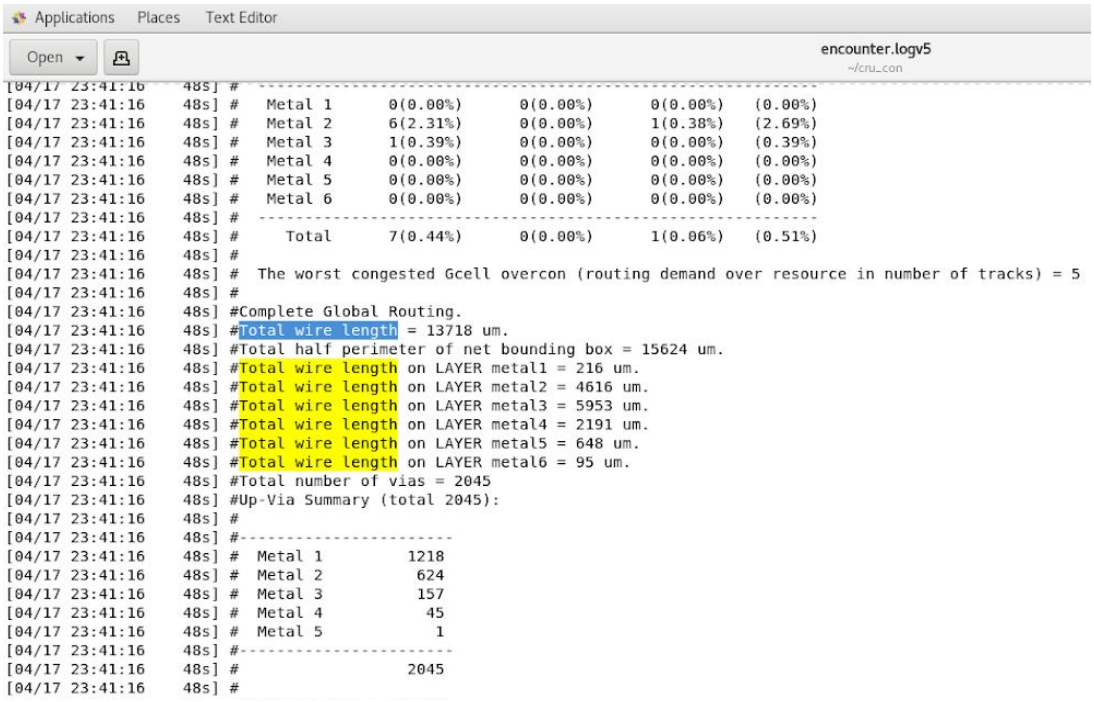

Fig.1 Log file screenshot of total Wirelength

2. Number of vias = 2045

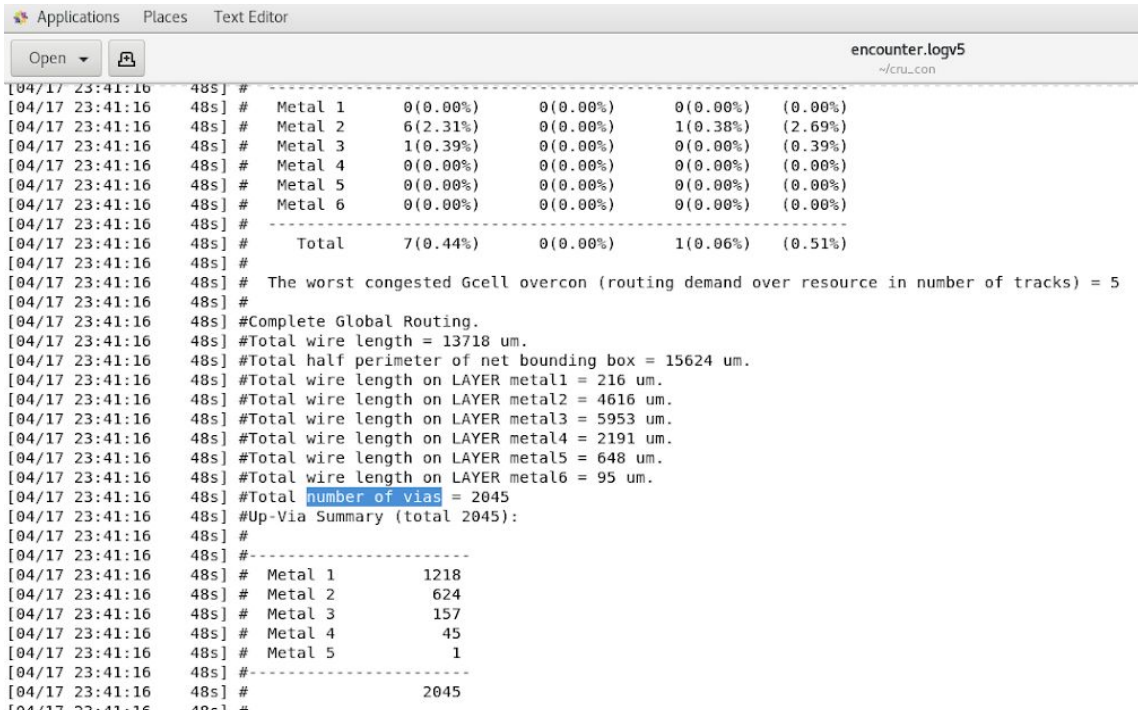

Fig.2 Log file screenshot of number of vias

3. Number of standard cells = 405

Applications Places Text Editor

Open encounter.logv5 ~/cru_con

```
[04/17 23:40:14    37s] *** Starting placeDesign default flow ***
[04/17 23:40:14    37s] *** Start deleteBufferTree ***
[04/17 23:40:14    37s] Info: Detect buffers to remove automatically.
[04/17 23:40:14    37s] Analyzing netlist ...
[04/17 23:40:14    37s] Updating netlist
[04/17 23:40:14    37s]
[04/17 23:40:14    37s] *summary: 0 instances (buffers/inverters) removed
[04/17 23:40:14    37s] *** Finish deleteBufferTree (0:00:00.0) ***
[04/17 23:40:14    37s] *** Starting "NanoPlace(TM) placement v#1 (mem=462.9M)" ...
[04/17 23:40:14    37s] Options: clkGateAware ignoreScan pinGuide congEffort=auto gpeffort=medium
[04/17 23:40:14    37s] **WARN: (ENCSP-9042):   Scan chains were not defined, -ignoreScan option will be ignored.
[04/17 23:40:14    37s] Define the scan chains before using this option.
[04/17 23:40:14    37s] Type 'man ENCSP-9042' for more detail.
[04/17 23:40:14    37s] #std cell=405 (0 fixed + 405 movable) #block=0 (0 floating + 0 preplaced)
[04/17 23:40:14    37s] #ioInst=0 #net=426 #term=1348 #term/net=3.16, #fixedIo=0, #floatIo=0, #fixedPin=0, #floatPin=26
[04/17 23:40:14    37s] stdCell: 405 single + 0 double + 0 multi
[04/17 23:40:14    37s] Total standard cell length = 1.4184 (mm), area = 0.0142 (mm^2)
[04/17 23:40:14    37s] Core basic site is core
[04/17 23:40:14    37s] Layer info - lib-1st H=1, V=2.  Cell-FPin=1. Top-pin=2
[04/17 23:40:14    37s] Average module density = 0.758.
[04/17 23:40:14    37s] Density for the design = 0.758.
[04/17 23:40:14    37s]        = stdcell_area 1773 sites (14184 um^2) / alloc_area 2340 sites (18720 um^2).
[04/17 23:40:14    37s] Pin Density = 0.760.
[04/17 23:40:14    37s]             = total # of pins 1348 / total Instance area 1773.
[04/17 23:40:14    37s] === lastAutoLevel = 5
```

Fig. 3 Log file screenshot of number of standard cells

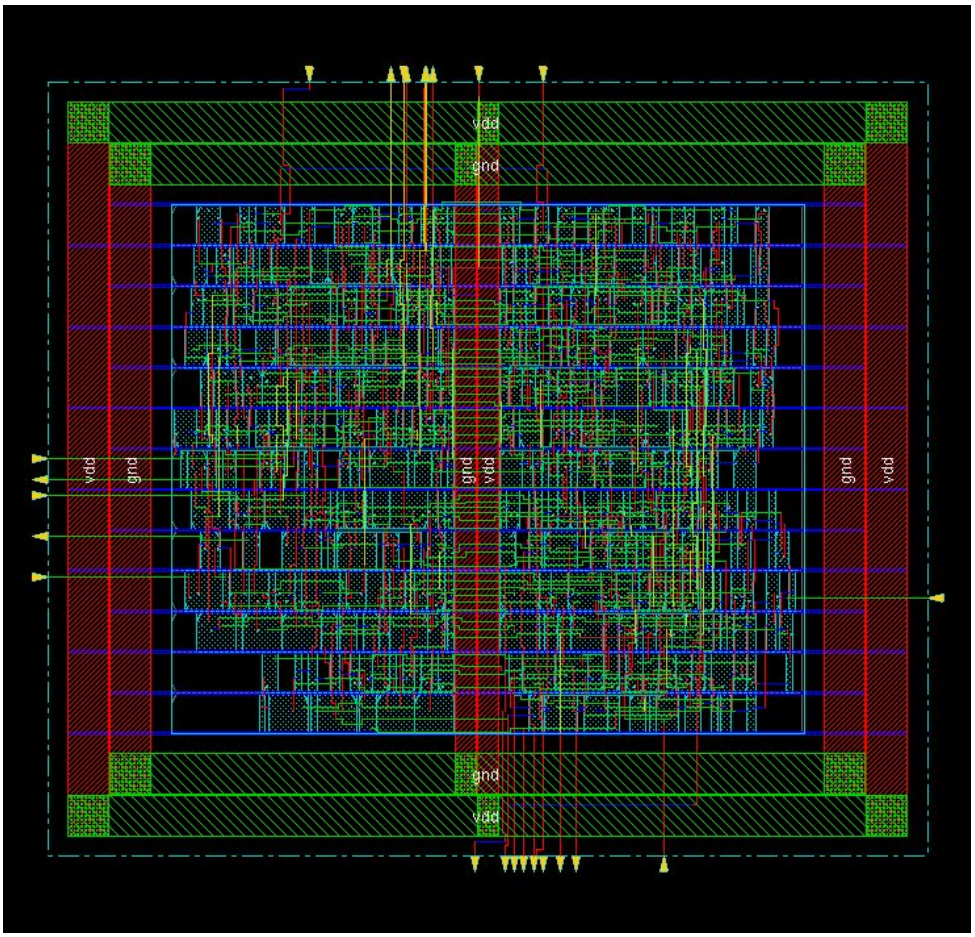

Fig. 4 Layout

Encounter.log:

```
[04/17 23:36:26    0s] Checking out Encounter license ...
[04/17 23:36:26    0s]          edsxl                DENIED:          "Encounter_Digital_Impl_Sys_XL"
[04/17 23:36:26    0s]          edsl                 DENIED:          "Encounter_Digital_Impl_Sys_L"
[04/17 23:36:26    0s]          encblk               DENIED:          "Encounter_Block"
[04/17 23:36:26    0s]          fegxl                DENIED:          "First_Encounter_GXL"
[04/17 23:36:26    0s]          fexl                 DENIED:          "FE_GPS"
[04/17 23:36:26    0s]          nru                  DENIED:          "NanoRoute_Ultra"
[04/17 23:36:26    0s]          vdixl                DENIED:          "Virtuoso_Digital_Implem_XL"
[04/17 23:36:26    0s]          vdi                  CHECKED OUT:     "Virtuoso_Digital_Implem"
[04/17 23:36:26    0s] Virtuoso_Digital_Implem 14.2 license checkout succeeded.
[04/17 23:36:26    0s]          Maximum number of instance allowed (1 x 50000).
[04/17 23:36:34    4s] ********************************************************************
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********************************************************************

[04/17 23:36:34    4s] @(#)CDS: Encounter v14.28-s033_1 (64bit) 03/21/2016 13:34 (Linux 2.6.18-194.el5)
[04/17 23:36:34    4s] @(#)CDS: NanoRoute v14.28-s005 NR160313-1959/14_28-UB (database version 2.30, 267.6.1)
{superthreading v1.25}
[04/17 23:36:34    4s] @(#)CDS: CeltIC v14.28-s006_1 (64bit) 03/08/2016 00:08:23 (Linux 2.6.18-194.el5)
[04/17 23:36:34    4s] @(#)CDS: AAE 14.28-s002 (64bit) 03/21/2016 (Linux 2.6.18-194.el5)
[04/17 23:36:34    4s] @(#)CDS: CTE 14.28-s007_1 (64bit) Mar  7 2016 23:11:05 (Linux 2.6.18-194.el5)
[04/17 23:36:34    4s] @(#)CDS: CPE v14.28-s006
[04/17 23:36:34    4s] @(#)CDS: IQRC/TQRC 14.2.2-s217 (64bit) Wed Apr 15 23:10:24 PDT 2015 (Linux 2.6.18-194.el5)
[04/17 23:36:34    4s] @(#)CDS: OA 22.50-p011 Tue Nov 11 03:24:55 2014
[04/17 23:36:34    4s] @(#)CDS: SGN 10.10-p124 (19-Aug-2014) (64 bit executable)
[04/17 23:36:34    4s] @(#)CDS: RCDB 11.5
[04/17 23:36:34    4s] --- Starting "Encounter v14.28-s033_1" on Wed Apr 17 23:36:34 2019 (mem=94.3M) ---
[04/17 23:36:34    4s] --- Running on lin16-324cvlb.ece.tamu.edu (x86_64 w/Linux 3.10.0-957.10.1.el7.x86_64) ---
[04/17 23:36:34    4s] This version was compiled on Mon Mar 21 13:34:48 PDT 2016.
[04/17 23:36:34    4s] Set DBUPerIGU to 1000.
[04/17 23:36:34    4s] Set net toggle Scale Factor to 1.00
[04/17 23:36:34    4s] Set Shrink Factor to 1.00000
[04/17 23:36:35    4s]
[04/17 23:36:35    4s] **INFO:  MMMC transition support version v31-84
[04/17 23:36:35    4s]
[04/17 23:36:35    4s] <CMD> set_global _enable_mmmc_by_default_flow      $CTE::mmmc_default
[04/17 23:36:35    4s] <CMD> suppressMessage ENCEXT-2799
[04/17 23:36:35    4s] <CMD> win
[04/17 23:37:52   16s] <CMD> init_design
```

[04/17 23:37:52 16s]
[04/17 23:37:52 16s] Loading LEF file iit018_stdcells.lef ...
[04/17 23:37:52 16s] **WARN: (ENCLF-108): There is no overlap layer defined in any LEF file
[04/17 23:37:52 16s] so you are unable to create rectilinear partition in a hierarchical flow.
[04/17 23:37:52 16s] Set DBUPerIGU to M2 pitch 800.
[04/17 23:37:52 16s]
[04/17 23:37:52 16s] viaInitial starts at Wed Apr 17 23:37:52 2019
**WARN: (ENCPP-557): A single-layer VIARULE GENERATE for turn-vias is obsolete and is being ignored. Remove this statement from LEF file: VIARULE TURN1 GENERATE.
[04/17 23:37:52 16s] Type 'man ENCPP-557' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCPP-557): A single-layer VIARULE GENERATE for turn-vias is obsolete and is being ignored. Remove this statement from LEF file: VIARULE TURN2 GENERATE.
[04/17 23:37:52 16s] Type 'man ENCPP-557' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCPP-557): A single-layer VIARULE GENERATE for turn-vias is obsolete and is being ignored. Remove this statement from LEF file: VIARULE TURN3 GENERATE.
[04/17 23:37:52 16s] Type 'man ENCPP-557' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCPP-557): A single-layer VIARULE GENERATE for turn-vias is obsolete and is being ignored. Remove this statement from LEF file: VIARULE TURN4 GENERATE.
[04/17 23:37:52 16s] Type 'man ENCPP-557' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCPP-557): A single-layer VIARULE GENERATE for turn-vias is obsolete and is being ignored. Remove this statement from LEF file: VIARULE TURN5 GENERATE.
[04/17 23:37:52 16s] Type 'man ENCPP-557' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCPP-557): A single-layer VIARULE GENERATE for turn-vias is obsolete and is being ignored. Remove this statement from LEF file: VIARULE TURN6 GENERATE.
[04/17 23:37:52 16s] Type 'man ENCPP-557' for more detail.
[04/17 23:37:52 16s] viaInitial ends at Wed Apr 17 23:37:52 2019
*** Begin netlist parsing (mem=343.6M) ***
[04/17 23:37:52 16s] Reading netlist ...
[04/17 23:37:52 16s] Backslashed names will retain backslash and a trailing blank character.
[04/17 23:37:52 16s] Reading verilog netlist 'chenjie_design_netlist.v'
[04/17 23:37:52 16s]
[04/17 23:37:52 16s] *** Memory Usage v#1 (Current mem = 344.598M, initial mem = 94.340M) ***
[04/17 23:37:52 16s] *** End netlist parsing (cpu=0:00:00.0, real=0:00:00.0, mem=344.6M) ***
[04/17 23:37:52 16s] Set top cell to chenjie_module.
[04/17 23:37:52 16s] *** End library_loading (cpu=0.00min, mem=0.0M, fe_cpu=0.27min, fe_real=1.43min, fe_mem=344.6M) ***
[04/17 23:37:52 16s] Starting recursive module instantiation check.
[04/17 23:37:52 16s] No recursion found.
[04/17 23:37:52 16s] Building hierarchical netlist for Cell chenjie_module ...
[04/17 23:37:52 16s] *** Netlist is unique.
[04/17 23:37:52 16s] ** info: there are 36 modules.
[04/17 23:37:52 16s] ** info: there are 405 stdCell insts.
[04/17 23:37:52 16s]
[04/17 23:37:52 16s] *** Memory Usage v#1 (Current mem = 351.348M, initial mem = 94.340M) ***
[04/17 23:37:52 16s] *info: set bottom ioPad orient R0
[04/17 23:37:52 16s] Horizontal Layer M1 offset = 500 (guessed)
[04/17 23:37:52 16s] Vertical Layer M2 offset = 400 (derived)
[04/17 23:37:52 16s] Suggestion: specify LAYER OFFSET in LEF file
[04/17 23:37:52 16s] Reason: hard to extract LAYER OFFSET from standard cells
[04/17 23:37:52 16s] Generated pitch 1.2 in metal6 is different from 1.6 defined in technology file in preferred direction.
[04/17 23:37:52 16s] Set Default Net Delay as 1000 ps.
[04/17 23:37:52 16s] Set Default Net Load as 0.5 pF.
[04/17 23:37:52 16s] Set Input Pin Transition Delay as 120 ps.
[04/17 23:37:52 16s] **WARN: (ENCOPT-3465): The buffer cells were automatically identified. The command setBufFootPrint is ignored. If you want to force the tool to honor this setting, you have to load a footprint file through the loadFootPrint command.
[04/17 23:37:52 16s] Type 'man ENCOPT-3465' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCOPT-3466): The inverter cells were automatically identified. The command setInvFootPrint is ignored. If you want to force the tool to honor this setting, you have to load a footprint file through the loadFootPrint command.

[04/17 23:37:52 16s] Type 'man ENCOPT-3466' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCOPT-3467): The delay cells were automatically identified. The command setDelayFootPrint is ignored. If you want to force the tool to honor this setting, you have to load a footprint file through the loadFootPrint command.
[04/17 23:37:52 16s] Type 'man ENCOPT-3467' for more detail.
[04/17 23:37:52 16s] **WARN: (ENCSYT-7328): The design has been initialized in physical-only mode because the init_mmmc_file global variable was not defined. Timing analysis will not be possible within this session. You can only use commands that do not depend on timing data. If you need to use timing, you need to restart with an init_mmmc_file to define the timing setup, or you can save this design and use restore_design -mmmc_file <viewDef.tcl> to add the timing setup information.
[04/17 23:37:52 16s]
[04/17 23:37:52 16s] *** Summary of all messages that are not suppressed in this session:
[04/17 23:37:52 16s] Severity ID Count Summary
[04/17 23:37:52 16s] WARNING ENCLF-108 1 There is no overlap layer defined in any...
[04/17 23:37:52 16s] WARNING ENCSYT-7328 1 The design has been initialized in physi...
[04/17 23:37:52 16s] WARNING ENCPP-557 6 A single-layer VIARULE GENERATE for turn...
[04/17 23:37:52 16s] WARNING ENCOPT-3467 1 The delay cells were automatically ident...
[04/17 23:37:52 16s] WARNING ENCOPT-3466 1 The inverter cells were automatically id...
[04/17 23:37:52 16s] WARNING ENCOPT-3465 1 The buffer cells were automatically iden...
[04/17 23:37:52 16s] *** Message Summary: 11 warning(s), 0 error(s)
[04/17 23:37:52 16s]
[04/17 23:38:13 19s] <CMD> getIoFlowFlag
[04/17 23:38:38 23s] <CMD> setIoFlowFlag 0
[04/17 23:38:38 23s] <CMD> floorPlan -site core -r 0.9 0.7 30 30 30 30
[04/17 23:38:38 23s] Horizontal Layer M1 offset = 500 (guessed)
[04/17 23:38:38 23s] Vertical Layer M2 offset = 400 (derived)
[04/17 23:38:38 23s] Suggestion: specify LAYER OFFSET in LEF file
[04/17 23:38:38 23s] Reason: hard to extract LAYER OFFSET from standard cells
[04/17 23:38:38 23s] Generated pitch 1.2 in metal6 is different from 1.6 defined in technology file in preferred direction.
[04/17 23:38:38 23s] **WARN: (ENCFP-325): Floorplan of the design is resized. All current floorplan objects are automatically derived based on specified new floorplan. This may change blocks, fixed standard cells, existing routes and blockages.
[04/17 23:38:38 23s] <CMD> uiSetTool select
[04/17 23:38:38 23s] <CMD> getIoFlowFlag
[04/17 23:38:38 23s] <CMD> fit
[04/17 23:38:49 24s] <CMD> set sprCreateIeRingNets {}
[04/17 23:38:49 24s] <CMD> set sprCreateIeRingLayers {}
[04/17 23:38:49 24s] <CMD> set sprCreateIeRingWidth 1.0
[04/17 23:38:49 24s] <CMD> set sprCreateIeRingSpacing 1.0
[04/17 23:38:49 24s] <CMD> set sprCreateIeRingOffset 1.0
[04/17 23:38:49 24s] <CMD> set sprCreateIeRingThreshold 1.0
[04/17 23:38:49 24s] <CMD> set sprCreateIeRingJogDistance 1.0
[04/17 23:39:12 28s] <CMD> addRing -skip_via_on_wire_shape Noshape -skip_via_on_pin Standardcell -center 1 -stacked_via_top_layer metal6 -type core_rings -jog_distance 0.8 -threshold 0.8 -nets {gnd vdd} -follow core -stacked_via_bottom_layer metal1 -layer {bottom metal3 top metal3 right metal2 left metal2} -width 10 -spacing 0.5 -offset 0.8
[04/17 23:39:12 28s]
[04/17 23:39:12 28s] The power planner created 8 wires.
[04/17 23:39:12 28s] *** Ending Ring Generation (totcpu: 0:00:00.0,real: 0:00:00.0, mem: 452.6M) ***
[04/17 23:39:32 31s] <CMD> set sprCreateIeStripeNets {}
[04/17 23:39:32 31s] <CMD> set sprCreateIeStripeLayers {}
[04/17 23:39:32 31s] <CMD> set sprCreateIeStripeWidth 10.0
[04/17 23:39:32 31s] <CMD> set sprCreateIeStripeSpacing 2.0
[04/17 23:39:32 31s] <CMD> set sprCreateIeStripeThreshold 1.0
[04/17 23:39:56 34s] <CMD> addStripe -skip_via_on_wire_shape Noshape -block_ring_top_layer_limit metal3 -max_same_layer_jog_length 1.0 -padcore_ring_bottom_layer_limit metal1 -set_to_set_distance 100 -skip_via_on_pin Standardcell -stacked_via_top_layer metal6 -padcore_ring_top_layer_limit metal3 -spacing 0.5 -xleft_offset 70 -merge_stripes_value 0.8 -layer metal2 -block_ring_bottom_layer_limit metal1 -width 5 -nets {gnd vdd} -stacked_via_bottom_layer metal1
[04/17 23:39:56 34s]
[04/17 23:39:56 34s] Starting stripe generation ...
[04/17 23:39:56 34s] Non-Default setAddStripeOption Settings :

[04/17 23:39:56 34s] NONE
[04/17 23:39:56 34s] Stripe generation is complete; vias are now being generated.
[04/17 23:39:56 34s] The power planner created 2 wires.
[04/17 23:39:56 34s] *** Ending Stripe Generation (totcpu: 0:00:00.0,real: 0:00:00.0, mem: 455.6M) ***
[04/17 23:40:05 36s] <CMD> sroute -connect { blockPin padPin padRing corePin floatingStripe } -layerChangeRange { metal1 metal6 } -blockPinTarget { nearestTarget } -padPinPortConnect { allPort oneGeom } -padPinTarget { nearestTarget } -corePinTarget { firstAfterRowEnd } -floatingStripeTarget { blockring padring ring stripe ringpin blockpin followpin } -allowJogging 1 -crossoverViaLayerRange { metal1 metal6 } -allowLayerChange 1 -blockPin useLef -targetViaLayerRange { metal1 metal6 }
[04/17 23:40:05 36s] *** Begin SPECIAL ROUTE on Wed Apr 17 23:40:05 2019 ***
[04/17 23:40:05 36s] SPECIAL ROUTE ran on directory: /home/grads/l/lchenjie/cru_con
[04/17 23:40:05 36s] SPECIAL ROUTE ran on machine: lin16-324cvlb.ece.tamu.edu (Linux 3.10.0-957.10.1.el7.x86_64 x86_64 2.44Ghz)
[04/17 23:40:05 36s]
[04/17 23:40:05 36s] Begin option processing ...
[04/17 23:40:05 36s] srouteConnectPowerBump set to false
[04/17 23:40:05 36s] routeSpecial set to true
[04/17 23:40:05 36s] srouteBlockPin set to "useLef"
[04/17 23:40:05 36s] srouteBottomLayerLimit set to 1
[04/17 23:40:05 36s] srouteBottomTargetLayerLimit set to 1
[04/17 23:40:05 36s] srouteConnectConverterPin set to false
[04/17 23:40:05 36s] srouteCrossoverViaBottomLayer set to 1
[04/17 23:40:05 36s] srouteCrossoverViaTopLayer set to 6
[04/17 23:40:05 36s] srouteFloatingStripeTarget set to "blockring padring ring stripe ringpin blockpin followpin"
[04/17 23:40:05 36s] srouteFollowCorePinEnd set to 3
[04/17 23:40:05 36s] srouteJogControl set to "preferWithChanges differentLayer"
[04/17 23:40:05 36s] sroutePadPinAllPorts set to true
[04/17 23:40:05 36s] sroutePreserveExistingRoutes set to true
[04/17 23:40:05 36s] srouteRoutePowerBarPortOnBothDir set to true
[04/17 23:40:05 36s] srouteStopBlockPin set to "nearestTarget"
[04/17 23:40:05 36s] srouteTopLayerLimit set to 6
[04/17 23:40:05 36s] srouteTopTargetLayerLimit set to 6
[04/17 23:40:05 36s] End option processing: cpu: 0:00:00, real: 0:00:00, peak: 1078.00 megs.
[04/17 23:40:05 36s]
[04/17 23:40:05 36s] Reading DB technology information...
[04/17 23:40:05 36s] Finished reading DB technology information.
[04/17 23:40:05 36s] Reading floorplan and netlist information...
[04/17 23:40:05 36s] Finished reading floorplan and netlist information.
[04/17 23:40:05 36s] Read in 12 layers, 6 routing layers, 0 overlap layer
[04/17 23:40:05 36s] Read in 33 macros, 19 used
[04/17 23:40:05 36s] Read in 19 components
[04/17 23:40:05 36s] 19 core components: 19 unplaced, 0 placed, 0 fixed
[04/17 23:40:05 36s] Read in 26 logical pins
[04/17 23:40:05 36s] Read in 26 nets
[04/17 23:40:05 36s] Read in 2 special nets, 2 routed
[04/17 23:40:05 36s] Begin power routing ...
[04/17 23:40:05 36s] **WARN: (ENCSR-1253): Cannot find any standard cell pin connected to net vdd.
[04/17 23:40:05 36s] Run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as 'USE POWER' or 'USE GROUND'.
[04/17 23:40:05 36s] **WARN: (ENCSR-1254): Cannot find any block pin of net vdd. Check netlist, or change option to include the pin.
[04/17 23:40:05 36s] **WARN: (ENCSR-1256): Cannot find any CORE class pad pin of net vdd. Change routing area or layer to include the expected pin, or check netlist, or change port class in LEF file.
[04/17 23:40:05 36s] Type 'man ENCSR-1256' for more detail.
[04/17 23:40:05 36s] Cannot find any AREAIO class pad pin of net vdd. Check net list, or change port class in LEF file, or change option to include pin in given range.
[04/17 23:40:05 36s] **WARN: (ENCSR-1253): Cannot find any standard cell pin connected to net gnd.

[04/17 23:40:05 36s] Run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as 'USE POWER' or 'USE GROUND'.
[04/17 23:40:05 36s] **WARN: (ENCSR-1254): Cannot find any block pin of net gnd. Check netlist, or change option to include the pin.
[04/17 23:40:05 36s] **WARN: (ENCSR-1256): Cannot find any CORE class pad pin of net gnd. Change routing area or layer to include the expected pin, or check netlist, or change port class in LEF file.
[04/17 23:40:05 36s] Type 'man ENCSR-1256' for more detail.
[04/17 23:40:05 36s] Cannot find any AREAIO class pad pin of net gnd. Check net list, or change port class in LEF file, or change option to include pin in given range.
[04/17 23:40:05 36s] **WARN: (ENCSR-468): Cannot find any standard cell pin connected to net vdd.
[04/17 23:40:05 36s] Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".
[04/17 23:40:05 36s] **WARN: (ENCSR-468): Cannot find any standard cell pin connected to net vdd.
[04/17 23:40:05 36s] Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".
[04/17 23:40:05 36s] CPU time for FollowPin 0 seconds
[04/17 23:40:05 36s] **WARN: (ENCSR-468): Cannot find any standard cell pin connected to net gnd.
[04/17 23:40:05 36s] Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".
[04/17 23:40:05 36s] **WARN: (ENCSR-468): Cannot find any standard cell pin connected to net gnd.
[04/17 23:40:05 36s] Use setSrouteMode -corePinReferenceMacro <standard cell> to specify a reference macro for followpin connection, or run globalNetConnect command or change CPF file to make sure that the netlist reflects the correct power ground connections. The standard cell pins must be defined as "USE POWER" or "USE GROUND".
[04/17 23:40:05 36s] CPU time for FollowPin 0 seconds
[04/17 23:40:05 36s] Number of IO ports routed: 0
[04/17 23:40:05 36s] Number of Block ports routed: 0
[04/17 23:40:05 36s] Number of Stripe ports routed: 0
[04/17 23:40:05 36s] Number of Core ports routed: 28
[04/17 23:40:05 36s] Number of Pad ports routed: 0
[04/17 23:40:05 36s] Number of Power Bump ports routed: 0
[04/17 23:40:05 36s] Number of Followpin connections: 14
[04/17 23:40:05 36s] End power routing: cpu: 0:00:00, real: 0:00:00, peak: 1084.00 megs.
[04/17 23:40:05 36s]
[04/17 23:40:05 36s]
[04/17 23:40:05 36s]
[04/17 23:40:05 36s] Begin updating DB with routing results ...
[04/17 23:40:05 36s] Updating DB with 9 via definition ...Extracting standard cell pins and blockage .....
[04/17 23:40:05 36s] Pin and blockage extraction finished
[04/17 23:40:05 36s]
[04/17 23:40:05 36s]
sroute post-processing starts at Wed Apr 17 23:40:05 2019
The viaGen is rebuilding shadow vias for net gnd.
[04/17 23:40:05 36s] sroute post-processing ends at Wed Apr 17 23:40:05 2019

sroute post-processing starts at Wed Apr 17 23:40:05 2019
The viaGen is rebuilding shadow vias for net vdd.
[04/17 23:40:05 36s] sroute post-processing ends at Wed Apr 17 23:40:05 2019
sroute: Total CPU time used = 0:0:0
[04/17 23:40:05 36s] sroute: Total Real time used = 0:0:0
[04/17 23:40:05 36s] sroute: Total Memory used = 7.30 megs
[04/17 23:40:05 36s] sroute: Total Peak Memory used = 462.86 megs
[04/17 23:40:14 37s] <CMD> setPlaceMode -fp false
[04/17 23:40:14 37s] <CMD> placeDesign
[04/17 23:40:14 37s] **WARN: (ENCSP-9513): Timing constraint file does not exist

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[04/17 23:40:14    37s] **WARN: (ENCSP-9514):    Non-TimingDriven placement will be performed.
[04/17 23:40:14    37s] *** Starting placeDesign default flow ***
[04/17 23:40:14    37s] *** Start deleteBufferTree ***
[04/17 23:40:14    37s] Info: Detect buffers to remove automatically.
[04/17 23:40:14    37s] Analyzing netlist ...
[04/17 23:40:14    37s] Updating netlist
[04/17 23:40:14    37s]
[04/17 23:40:14    37s] *summary: 0 instances (buffers/inverters) removed
[04/17 23:40:14    37s] *** Finish deleteBufferTree (0:00:00.0) ***
[04/17 23:40:14    37s] *** Starting "NanoPlace(TM) placement v#1 (mem=462.9M)" ...
[04/17 23:40:14    37s] Options: clkGateAware ignoreScan pinGuide congEffort=auto gpeffort=medium
[04/17 23:40:14    37s] **WARN: (ENCSP-9042):    Scan chains were not defined, -ignoreScan option will be ignored.
[04/17 23:40:14    37s] Define the scan chains before using this option.
[04/17 23:40:14    37s] Type 'man ENCSP-9042' for more detail.
[04/17 23:40:14    37s] #std cell=405 (0 fixed + 405 movable) #block=0 (0 floating + 0 preplaced)
[04/17 23:40:14    37s] #ioInst=0 #net=426 #term=1348 #term/net=3.16, #fixedIo=0, #floatIo=0, #fixedPin=0, #floatPin=26
[04/17 23:40:14    37s] stdCell: 405 single + 0 double + 0 multi
[04/17 23:40:14    37s] Total standard cell length = 1.4184 (mm), area = 0.0142 (mm^2)
[04/17 23:40:14    37s] Core basic site is core
[04/17 23:40:14    37s] Layer info - lib-1st H=1, V=2.  Cell-FPin=1. Top-pin=2
[04/17 23:40:14    37s] Average module density = 0.758.
[04/17 23:40:14    37s] Density for the design = 0.758.
[04/17 23:40:14    37s]       = stdcell_area 1773 sites (14184 um^2) / alloc_area 2340 sites (18720 um^2).
[04/17 23:40:14    37s] Pin Density = 0.760.
[04/17 23:40:14    37s]            = total # of pins 1348 / total Instance area 1773.
[04/17 23:40:14    37s] === lastAutoLevel = 5
[04/17 23:40:14    37s] Clock gating cells determined by native netlist tracing.
[04/17 23:40:15    37s] Iteration  1: Total net bbox = 3.929e-12 (3.93e-12 0.00e+00)
[04/17 23:40:15    37s]              Est.  stn bbox = 4.111e-12 (4.11e-12 0.00e+00)
[04/17 23:40:15    37s]              cpu = 0:00:00.0 real = 0:00:00.0 mem = 464.9M
[04/17 23:40:15    37s] Iteration  2: Total net bbox = 3.929e-12 (3.93e-12 0.00e+00)
[04/17 23:40:15    37s]              Est.  stn bbox = 4.111e-12 (4.11e-12 0.00e+00)
[04/17 23:40:15    37s]              cpu = 0:00:00.0 real = 0:00:00.0 mem = 464.9M
[04/17 23:40:15    37s] Iteration  3: Total net bbox = 2.976e+00 (1.17e+00 1.80e+00)
[04/17 23:40:15    37s]              Est.  stn bbox = 3.220e+00 (1.27e+00 1.95e+00)
[04/17 23:40:15    37s]              cpu = 0:00:00.0 real = 0:00:00.0 mem = 464.9M
[04/17 23:40:15    37s] Iteration  4: Total net bbox = 8.996e+03 (5.70e+03 3.30e+03)
[04/17 23:40:15    37s]              Est.  stn bbox = 9.701e+03 (6.07e+03 3.63e+03)
[04/17 23:40:15    37s]              cpu = 0:00:00.1 real = 0:00:00.0 mem = 464.9M
[04/17 23:40:16    38s] Iteration  5: Total net bbox = 1.037e+04 (6.61e+03 3.76e+03)
[04/17 23:40:16    38s]              Est.  stn bbox = 1.133e+04 (7.09e+03 4.24e+03)
[04/17 23:40:16    38s]              cpu = 0:00:00.1 real = 0:00:01.0 mem = 464.9M
[04/17 23:40:16    38s] Iteration  6: Total net bbox = 1.125e+04 (6.98e+03 4.27e+03)
[04/17 23:40:16    38s]              Est.  stn bbox = 1.226e+04 (7.45e+03 4.81e+03)
[04/17 23:40:16    38s]              cpu = 0:00:00.1 real = 0:00:00.0 mem = 464.9M
[04/17 23:40:16    38s] Iteration  7: Total net bbox = 1.166e+04 (6.79e+03 4.87e+03)
[04/17 23:40:16    38s]              Est.  stn bbox = 1.266e+04 (7.24e+03 5.42e+03)
[04/17 23:40:16    38s]              cpu = 0:00:00.1 real = 0:00:00.0 mem = 464.9M
[04/17 23:40:16    38s] Congestion driven padding in post-place stage.
[04/17 23:40:16    38s] Congestion driven padding increases utilization from 0.757 to 0.949
[04/17 23:40:16    38s] Congestion driven padding runtime: cpu = 0:00:00.0 real = 0:00:00.0 mem = 466.9M
[04/17 23:40:16    38s] Iteration  8: Total net bbox = 1.322e+04 (7.14e+03 6.08e+03)
[04/17 23:40:16    38s]              Est.  stn bbox = 1.446e+04 (7.72e+03 6.74e+03)
[04/17 23:40:16    38s]              cpu = 0:00:00.2 real = 0:00:00.0 mem = 466.9M
[04/17 23:40:16    38s] Iteration  9: Total net bbox = 1.322e+04 (7.14e+03 6.08e+03)
[04/17 23:40:16    38s]              Est.  stn bbox = 1.446e+04 (7.72e+03 6.74e+03)
[04/17 23:40:16    38s]              cpu = 0:00:00.0 real = 0:00:00.0 mem = 466.9M
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[04/17 23:40:16    38s] *** cost = 1.322e+04 (7.14e+03 6.08e+03) (cpu for global=0:00:00.7) real=0:00:02.0***
[04/17 23:40:16    38s] Info: 0 clock gating cells identified, 0 (on average) moved
[04/17 23:40:16    38s] Core Placement runtime cpu: 0:00:00.7 real: 0:00:02.0
[04/17 23:40:16    38s] **WARN: (ENCSP-9025):    No scan chain specified/traced.
[04/17 23:40:16    38s] Type 'man ENCSP-9025' for more detail.
[04/17 23:40:16    38s] Core basic site is core
[04/17 23:40:16    38s] Layer info - lib-1st H=1, V=2.  Cell-FPin=1. Top-pin=2
[04/17 23:40:16    38s] *** Starting refinePlace (0:00:38.4 mem=466.9M) ***
[04/17 23:40:16    38s] Total net length = 1.324e+04 (7.144e+03 6.095e+03) (ext = 3.012e+03)
[04/17 23:40:16    38s] Starting refinePlace ...
[04/17 23:40:16    38s] Move report: placeLevelShifters moves 0 insts, mean move: 0.00 um, max move: 0.00 um
[04/17 23:40:16    38s]   Spread Effort: high, pre-route mode, useDDP on.
[04/17 23:40:16    38s] [CPU] RefinePlace/preRPlace (cpu=0:00:00.1, real=0:00:00.0, mem=466.9MB) @(0:00:38.4 - 0:00:38.5).
[04/17 23:40:16    38s] Move report: preRPlace moves 405 insts, mean move: 3.92 um, max move: 13.02 um
[04/17 23:40:16    38s]            Max move on inst (U461): (101.80, 140.39) --> (98.40, 150.00)
[04/17 23:40:16    38s]            Length: 2 sites, height: 1 rows, site name: core, cell type: INVX1
[04/17 23:40:16    38s]            Violation at original loc: Placement Blockage Violation
[04/17 23:40:16    38s] wireLenOptFixPriorityInst 0 inst fixed
[04/17 23:40:16    38s] Placement tweakage begins.
[04/17 23:40:16    38s] wire length = 1.540e+04
[04/17 23:40:16    38s] wire length = 1.453e+04
[04/17 23:40:16    38s] Placement tweakage ends.
[04/17 23:40:16    38s] Move report: tweak moves 162 insts, mean move: 5.31 um, max move: 24.00 um
[04/17 23:40:16    38s]            Max move on inst (U495): (89.60, 100.00) --> (93.60, 120.00)
[04/17 23:40:16    38s] Move report: legalization moves 0 insts, mean move: 0.00 um, max move: 0.00 um
[04/17 23:40:16    38s] [CPU] RefinePlace/Legalization (cpu=0:00:00.0, real=0:00:00.0, mem=466.9MB) @(0:00:38.5 - 0:00:38.5).
[04/17 23:40:16    38s] Move report: Detail placement moves 405 insts, mean move: 4.94 um, max move: 17.90 um
[04/17 23:40:16    38s]            Max move on inst (U495): (90.10, 105.59) --> (93.60, 120.00)
[04/17 23:40:16    38s]            Runtime: CPU: 0:00:00.1 REAL: 0:00:00.0 MEM: 466.9MB
[04/17 23:40:16    38s] Statistics of distance of Instance movement in refine placement:
[04/17 23:40:16    38s]   maximum (X+Y) =        17.90 um
[04/17 23:40:16    38s]   inst (U495) with max move: (90.104, 105.595) -> (93.6, 120)
[04/17 23:40:16    38s]   mean    (X+Y) =         4.94 um
[04/17 23:40:16    38s] Total instances flipped for WireLenOpt: 19
[04/17 23:40:16    38s] Summary Report:
[04/17 23:40:16    38s] Instances move: 405 (out of 405 movable)
[04/17 23:40:16    38s] Mean displacement: 4.94 um
[04/17 23:40:16    38s] Max displacement: 17.90 um (Instance: U495) (90.104, 105.595) -> (93.6, 120)
[04/17 23:40:16    38s]            Length: 3 sites, height: 1 rows, site name: core, cell type: NOR2X1
[04/17 23:40:16    38s] Total instances moved : 405
[04/17 23:40:16    38s] Total net length = 1.316e+04 (6.855e+03 6.310e+03) (ext = 2.997e+03)
[04/17 23:40:16    38s] Runtime: CPU: 0:00:00.1 REAL: 0:00:00.0 MEM: 466.9MB
[04/17 23:40:16    38s] [CPU] RefinePlace/total (cpu=0:00:00.1, real=0:00:00.0, mem=466.9MB) @(0:00:38.4 - 0:00:38.5).
[04/17 23:40:16    38s] *** Finished refinePlace (0:00:38.5 mem=466.9M) ***
[04/17 23:40:16    38s] Total net length = 1.316e+04 (6.844e+03 6.312e+03) (ext = 3.014e+03)
[04/17 23:40:16    38s] *** End of Placement (cpu=0:00:00.9, real=0:00:02.0, mem=466.9M) ***
[04/17 23:40:16    38s] Core basic site is core
[04/17 23:40:16    38s] Layer info - lib-1st H=1, V=2.  Cell-FPin=1. Top-pin=2
[04/17 23:40:16    38s] default core: bins with density >  0.75 =   50 % ( 2 / 4 )
[04/17 23:40:16    38s] Density distribution unevenness ratio = 2.254%
[04/17 23:40:16    38s] Starting IO pin assignment...
[04/17 23:40:16    38s] Completed IO pin assignment.
[04/17 23:40:16    38s] Starting congestion repair ...
[04/17 23:40:16    38s] congRepair options: -clkGateAware 1 -rplaceIncrNPClkGateAwareMode 4.
[04/17 23:40:16    38s] *** Starting trialRoute (mem=466.9M) ***
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] There are 0 guide points passed to trialRoute for fixed pins.
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[04/17 23:40:16    38s] There are 0 guide points passed to trialRoute for pinGroup/netGroup/pinGuide pins.
[04/17 23:40:16    38s] triMarkNetsWithAllFixedWires runtime= 0:00:00.0
[04/17 23:40:16    38s] Options:  -noPinGuide
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] routingBox: (0 0) (216700 190000)
[04/17 23:40:16    38s] coreBox:    (30400 30000) (186300 160000)
[04/17 23:40:16    38s] Number of multi-gpin terms=74, multi-gpins=158, moved blk term=0/0
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Phase 1a route (0:00:00.0 466.9M):
[04/17 23:40:16    38s] Est net length = 1.331e+04um = 7.127e+03H + 6.182e+03V
[04/17 23:40:16    38s] Usage: (13.6%H 13.8%V) = (8.683e+03um 1.705e+04um) = (2155 1705)
[04/17 23:40:16    38s] Obstruct: 0 = 0 (0.0%H) + 0 (0.0%V)
[04/17 23:40:16    38s] Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Phase 1b route (0:00:00.0 467.9M):
[04/17 23:40:16    38s] Usage: (13.6%H 13.8%V) = (8.679e+03um 1.705e+04um) = (2154 1705)
[04/17 23:40:16    38s] Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Phase 1c route (0:00:00.0 467.9M):
[04/17 23:40:16    38s] Usage: (13.6%H 13.8%V) = (8.675e+03um 1.702e+04um) = (2153 1702)
[04/17 23:40:16    38s] Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Phase 1d route (0:00:00.0 467.9M):
[04/17 23:40:16    38s] Usage: (13.6%H 13.8%V) = (8.675e+03um 1.702e+04um) = (2153 1702)
[04/17 23:40:16    38s] Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Phase 1a-1d Overflow: 0.00% H + 0.00% V (0:00:00.0 467.9M)

[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Phase 1e route (0:00:00.0 468.9M):
[04/17 23:40:16    38s] Usage: (13.6%H 13.8%V) = (8.675e+03um 1.702e+04um) = (2153 1702)
[04/17 23:40:16    38s] Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Overflow: 0.00% H + 0.00% V (0:00:00.0 468.9M)

[04/17 23:40:16    38s] Usage: (13.6%H 13.8%V) = (8.675e+03um 1.702e+04um) = (2153 1702)
[04/17 23:40:16    38s] Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Congestion distribution:
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Remain              cntH                    cntV
[04/17 23:40:16    38s] ------------------------------------
[04/17 23:40:16    38s] ------------------------------------
[04/17 23:40:16    38s]   4:      0             0.00%     1             0.11%
[04/17 23:40:16    38s]   5:      893         100.00%   892         99.89%
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Global route (cpu=0.0s real=0.0s 468.9M)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] *** After '-updateRemainTrks' operation:
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Usage: (14.1%H 14.0%V) = (9.007e+03um 1.723e+04um) = (2236 1723)
[04/17 23:40:16    38s] Overflow: 0 = 0 (0.00% H) + 0 (0.00% V)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Phase 1l Overflow: 0.00% H + 0.00% V (0:00:00.0 476.9M)

[04/17 23:40:16    38s]
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[04/17 23:40:16    38s] Congestion distribution:
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Remain               cntH                    cntV
[04/17 23:40:16    38s] ------------------------------------
[04/17 23:40:16    38s] ------------------------------------
[04/17 23:40:16    38s]   4:      0            0.00%     7            0.78%
[04/17 23:40:16    38s]   5:      893          100.00%  886          99.22%
[04/17 23:40:16    38s]
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] *** Completed Phase 1 route (0:00:00.0 476.9M) ***
[04/17 23:40:16    38s]
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Total length: 1.476e+04um, number of vias: 2500
[04/17 23:40:16    38s] M1(H) length: 0.000e+00um, number of vias: 1322
[04/17 23:40:16    38s] M2(V) length: 5.702e+03um, number of vias: 1004
[04/17 23:40:16    38s] M3(H) length: 6.994e+03um, number of vias: 168
[04/17 23:40:16    38s] M4(V) length: 2.032e+03um, number of vias: 5
[04/17 23:40:16    38s] M5(H) length: 3.240e+01um, number of vias: 1
[04/17 23:40:16    38s] M6(V) length: 5.000e-01um
[04/17 23:40:16    38s] *** Completed Phase 2 route (0:00:00.0 476.9M) ***
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] *** Finished all Phases (cpu=0:00:00.0 mem=476.9M) ***
[04/17 23:40:16    38s] dbSprFixZeroViaCodes runtime= 0:00:00.0
[04/17 23:40:16    38s] Peak Memory Usage was 476.9M
[04/17 23:40:16    38s] TrialRoute+GlbRouteEst total runtime= +0:00:00.0 = 0:00:00.0
[04/17 23:40:16    38s]   TrialRoute full (called once) runtime= 0:00:00.0
[04/17 23:40:16    38s]   GlbRouteEst (called once) runtime= 0:00:00.0
[04/17 23:40:16    38s] *** Finished trialRoute (cpu=0:00:00.0 mem=476.9M) ***
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] Local HotSpot Analysis: normalized max congestion hotspot area = 0.00, normalized total congestion hotspot
area = 0.00 (area is in unit of 4 std-cell row bins)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] ** np local hotspot detection info verbose **
[04/17 23:40:16    38s] level 0: max group area = 0.00 (0.00%) total group area = 0.00 (0.00%) threshold area = 88.00 (area is in
unit of 4 std-cell row bins)
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] describeCongestion: hCong = 0.00 vCong = 0.00
[04/17 23:40:16    38s] Trial Route Overflow 0.000000(H) 0.000000(V).
[04/17 23:40:16    38s] Start repairing congestion with level 1.
[04/17 23:40:16    38s] Skipped repairing congestion.
[04/17 23:40:16    38s] End of congRepair (cpu=0:00:00.0, real=0:00:00.0)
[04/17 23:40:16    38s] *** Finishing placeDesign default flow ***
[04/17 23:40:16    38s] **placeDesign ... cpu = 0: 0: 1, real = 0: 0: 2, mem = 464.9M **
[04/17 23:40:16    38s]
[04/17 23:40:16    38s] *** Summary of all messages that are not suppressed in this session:
[04/17 23:40:16    38s] Severity  ID               Count  Summary
[04/17 23:40:16    38s] WARNING   ENCSP-9513           1  Timing constraint file does not exist
[04/17 23:40:16    38s] WARNING   ENCSP-9514           1  Non-TimingDriven placement will be perfo...
[04/17 23:40:16    38s] WARNING   ENCSP-9025           1  No scan chain specified/traced.
[04/17 23:40:16    38s] WARNING   ENCSP-9042           1  Scan chains were not defined, -ignoreSca...
[04/17 23:40:16    38s] *** Message Summary: 4 warning(s), 0 error(s)
[04/17 23:40:16    38s]
[04/17 23:41:01    46s] <CMD> create_library_set -name iit018_stdcells -timing {iit018_stdcells.tlf}
[04/17 23:41:01    46s] Reading iit018_stdcells timing library '/home/grads/l/lchenjie/cru_con/iit018_stdcells.tlf' ...
[04/17 23:41:01    46s] **WARN: (TECHLIB-436):   Attribute 'fanout_load' on 'input/inout' pin 'A' of cell 'AND2X1' is not defined in the
library.
```

[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'B' of cell 'AND2X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'max_fanout' on 'output/inout' pin 'Y' of cell 'AND2X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'A' of cell 'AND2X2' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'B' of cell 'AND2X2' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'max_fanout' on 'output/inout' pin 'Y' of cell 'AND2X2' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'A' of cell 'AOI21X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'B' of cell 'AOI21X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'C' of cell 'AOI21X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'max_fanout' on 'output/inout' pin 'Y' of cell 'AOI21X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'A' of cell 'AOI22X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'B' of cell 'AOI22X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'C' of cell 'AOI22X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'D' of cell 'AOI22X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'max_fanout' on 'output/inout' pin 'Y' of cell 'AOI22X1' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'A' of cell 'BUFX2' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'max_fanout' on 'output/inout' pin 'Y' of cell 'BUFX2' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'A' of cell 'BUFX4' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'max_fanout' on 'output/inout' pin 'Y' of cell 'BUFX4' is not defined in the library.
[04/17 23:41:01 46s] **WARN: (TECHLIB-436): Attribute 'fanout_load' on 'input/inout' pin 'A' of cell 'CLKBUF1' is not defined in the library.
[04/17 23:41:01 46s] Message <TECHLIB-436> has exceeded the message display limit of '20'.
setMessageLimit/set_message_limit sets the limit. unsetMessageLimit/unset_message_limit can be used to reset this.
[04/17 23:41:01 46s] Read 32 cells in library 'iit018_stdcells'
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -timingEngine {}
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -routeWithTimingDriven 1
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -routeWithSiPostRouteFix 0
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -drouteStartIteration default
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -routeTopRoutingLayer default
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -routeBottomRoutingLayer default
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -drouteEndIteration default
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -routeWithTimingDriven true
[04/17 23:41:15 48s] <CMD> setNanoRouteMode -quiet -routeWithSiDriven false
[04/17 23:41:15 48s] Running Native NanoRoute ...
[04/17 23:41:15 48s] <CMD> routeDesign -globalDetail
[04/17 23:41:15 48s] #routeDesign: cpu time = 00:00:00, elapsed time = 00:00:00, memory = 479.69 (MB), peak = 482.75 (MB)
[04/17 23:41:15 48s] #WARNING (NRIG-96) Selected single pass global detail route "-globalDetail". Clock eco and post optimizations will not be run. See "man NRIG-96" for more details.
[04/17 23:41:15 48s] Core basic site is core
[04/17 23:41:15 48s] Layer info - lib-1st H=1, V=2. Cell-FPin=1. Top-pin=2

[04/17 23:41:15 48s] Begin checking placement ... (start mem=497.8M, init mem=497.8M)
[04/17 23:41:15 48s] *info: Placed = 405
[04/17 23:41:15 48s] *info: Unplaced = 0
[04/17 23:41:15 48s] Placement Density:75.77%(14184/18720)
[04/17 23:41:15 48s] Finished checkPlace (cpu: total=0:00:00.0, vio checks=0:00:00.0; mem=497.8M)
[04/17 23:41:15 48s] #**INFO: honoring user setting for routeWithTimingDriven set to true
[04/17 23:41:15 48s] #**INFO: honoring user setting for routeWithSiDriven set to false
[04/17 23:41:15 48s] #WARNING (NRIG-87) Timing file "" not found, resetting timing engine to default for this session.
[04/17 23:41:15 48s]
[04/17 23:41:15 48s] changeUseClockNetStatus Option : -noFixedNetWires
[04/17 23:41:15 48s] *** Changed status on (0) nets in Clock.
[04/17 23:41:15 48s] *** End changeUseClockNetStatus (cpu=0:00:00.0, real=0:00:00.0, mem=497.8M) ***
[04/17 23:41:15 48s]
[04/17 23:41:15 48s] globalDetailRoute
[04/17 23:41:15 48s]
[04/17 23:41:15 48s] #setNanoRouteMode -routeWithSiDriven false
[04/17 23:41:15 48s] #setNanoRouteMode -routeWithTimingDriven true
[04/17 23:41:15 48s] #Start globalDetailRoute on Wed Apr 17 23:41:15 2019
[04/17 23:41:15 48s] #
[04/17 23:41:15 48s] #Generating timing graph information, please wait...
[04/17 23:41:15 48s] #426 total nets, 0 already routed, 0 will ignore in trialRoute
[04/17 23:41:15 48s] #Dump tif for version 2.1
[04/17 23:41:15 48s] **WARN: (ENCEXT-3530): The process node is not set. Use the command setDesignMode -process <process node> prior to extraction for maximum accuracy and optimal automatic threshold setting.
[04/17 23:41:15 48s] **WARN: (ENCEXT-6197): Capacitance table file not specified. This will result in lower parasitic accuracy using preRoute extraction or postRoute extraction with effort level 'low'. It is recommended to generate the capacitance table file using 'generateCapTbl' command and specify it before extraction.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[3] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[3] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[2] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[1] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[4] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[0] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[5] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[6] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[5] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[4] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[3] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[2] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[1] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[6] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[0] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.

[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_speed_reg[7] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance speed_reg[7] term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance cruise_on_reg term CLK has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCEXT-2882): Unable to find resistance for via 'M2_M1' in capacitance table or LEF files. Check the capacitance table and LEF files. Assigning default value of 4.0 ohms.
[04/17 23:41:15 48s] **WARN: (ENCEXT-2882): Unable to find resistance for via 'M3_M2' in capacitance table or LEF files. Check the capacitance table and LEF files. Assigning default value of 4.0 ohms.
[04/17 23:41:15 48s] **WARN: (ENCEXT-2882): Unable to find resistance for via 'M4_M3' in capacitance table or LEF files. Check the capacitance table and LEF files. Assigning default value of 4.0 ohms.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance U600 term B has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (ENCESI-2013): The power rail of instance U600 term B has zero voltage, resetting the power rail to default vdd. Check the power specification of this instance.
[04/17 23:41:15 48s] **WARN: (EMS-63): Message <ENCESI-2013> has exceeded the default message display limit of 20.
[04/17 23:41:15 48s] To avoid this warning, increase the display limit per unique message by
[04/17 23:41:15 48s] using the set_message -limit <number> command.
[04/17 23:41:15 48s] The message limit can be removed by using the set_message -no_limit command.
[04/17 23:41:15 48s] Note that setting a very large number using the set_message -limit command
[04/17 23:41:15 48s] or removing the message limit using the set_message -no_limit command can
[04/17 23:41:15 48s] significantly increase the log file size.
[04/17 23:41:15 48s] To suppress a message, use the set_message -suppress command.
[04/17 23:41:15 48s] **WARN: (ENCEXT-2882): Unable to find resistance for via 'M5_M4' in capacitance table or LEF files. Check the capacitance table and LEF files. Assigning default value of 4.0 ohms.
[04/17 23:41:15 48s] **WARN: (ENCEXT-2882): Unable to find resistance for via 'M6_M5' in capacitance table or LEF files. Check the capacitance table and LEF files. Assigning default value of 4.0 ohms.
[04/17 23:41:15 48s] AAE_MTTC: End Timing Check Calculation. (CPU Time=0:00:00.0, Real Time=0:00:00.0)
[04/17 23:41:15 48s] AAE_THRD: End delay calculation. (MEM=645.965 CPU=0:00:00.0 REAL=0:00:00.0)
[04/17 23:41:15 48s] #Write timing file took: cpu time = 00:00:00, elapsed time = 00:00:00, memory = 515.95 (MB), peak = 523.95 (MB)
[04/17 23:41:15 48s] #Done generating timing graph information.
[04/17 23:41:15 48s] ### Ignoring a total of 3 master slice layers:
[04/17 23:41:15 48s] ### nwell nactive pactive
[04/17 23:41:15 48s] #WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
[04/17 23:41:15 48s] #WARNING (NRDB-2005) SPECIAL_NET gnd has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
[04/17 23:41:15 48s] #WARNING (NRDB-976) The TRACK STEP 1.2000 for preferred direction tracks is smaller than the PITCH 1.6000 for LAYER metal6. This will cause routability problems for NanoRoute.
[04/17 23:41:15 48s] #Start reading timing information from file .timing_file_17335.tif.gz ...
[04/17 23:41:15 48s] #WARNING (NRDB-194)
[04/17 23:41:15 48s] #No setup time constraints read in
[04/17 23:41:15 48s] #Read in timing information for 26 ports, 405 instances from timing file .timing_file_17335.tif.gz.
[04/17 23:41:15 48s] #NanoRoute Version v14.28-s005 NR160313-1959/14_28-UB
[04/17 23:41:15 48s] #Bottom routing layer is M1, bottom routing layer for shielding is M1, bottom shield layer is M1
[04/17 23:41:15 48s] #Start routing data preparation.
[04/17 23:41:15 48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal1 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal2 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal1 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal2 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal2 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal3 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal2 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal3 is not specified for width 0.300.
[04/17 23:41:15 48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal3 is not specified for width 0.300.

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[04/17 23:41:15    48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal4 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal3 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal4 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal4 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal5 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal4 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal5 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal5 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal6 is not specified for width 0.500.
[04/17 23:41:15    48s] #WARNING (NRDB-2077) The below via enclosure for LAYER metal5 is not specified for width 0.300.
[04/17 23:41:15    48s] #WARNING (NRDB-2078) The above via enclosure for LAYER metal6 is not specified for width 0.500.
[04/17 23:41:16    48s] # metal1      H   Track-Pitch = 1.000    Line-2-Via Pitch = 0.650
[04/17 23:41:16    48s] # metal2      V   Track-Pitch = 0.800    Line-2-Via Pitch = 0.650
[04/17 23:41:16    48s] # metal3      H   Track-Pitch = 1.000    Line-2-Via Pitch = 0.650
[04/17 23:41:16    48s] # metal4      V   Track-Pitch = 0.800    Line-2-Via Pitch = 0.650
[04/17 23:41:16    48s] # metal5      H   Track-Pitch = 1.000    Line-2-Via Pitch = 0.650
[04/17 23:41:16    48s] # metal6      V   Track-Pitch = 1.200    Line-2-Via Pitch = 1.000
[04/17 23:41:16    48s] #Regenerating Ggrids automatically.
[04/17 23:41:16    48s] #Auto generating G-grids with size=15 tracks, using layer metal2's pitch = 0.800.
[04/17 23:41:16    48s] #Using automatically generated G-grids.
[04/17 23:41:16    48s] #Done routing data preparation.
[04/17 23:41:16    48s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 548.27 (MB), peak = 548.27 (MB)
[04/17 23:41:16    48s] #Merging special wires...
[04/17 23:41:16    48s] #Number of eco nets is 0
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Start data preparation...
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Data preparation is done on Wed Apr 17 23:41:16 2019
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Analyzing routing resource...
[04/17 23:41:16    48s] #Routing resource analysis is done on Wed Apr 17 23:41:16 2019
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #  Resource Analysis:
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #               Routing  #Avail      #Track     #Total     %Gcell
[04/17 23:41:16    48s] #  Layer        Direction   Track     Blocked      Gcell    Blocked
[04/17 23:41:16    48s] #  ---------------------------------------------------------------
[04/17 23:41:16    48s] #  Metal 1        H         190          0         288    42.71%
[04/17 23:41:16    48s] #  Metal 2        V         208         63         288     9.72%
[04/17 23:41:16    48s] #  Metal 3        H         148         42         288    11.11%
[04/17 23:41:16    48s] #  Metal 4        V         271          0         288     0.00%
[04/17 23:41:16    48s] #  Metal 5        H         190          0         288     0.00%
[04/17 23:41:16    48s] #  Metal 6        V         180          0         288     0.00%
[04/17 23:41:16    48s] #  ---------------------------------------------------------------
[04/17 23:41:16    48s] #  Total                   1187       7.56%    1728    10.59%
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 548.53 (MB), peak = 548.59 (MB)
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #start global routing iteration 1...
[04/17 23:41:16    48s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.12 (MB), peak = 549.33 (MB)
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #start global routing iteration 2...
[04/17 23:41:16    48s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.33 (MB), peak = 549.37 (MB)
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #
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[04/17 23:41:16    48s] #Total number of trivial nets (e.g. < 2 pins) = 2 (skipped).
[04/17 23:41:16    48s] #Total number of routable nets = 426.
[04/17 23:41:16    48s] #Total number of nets in the design = 428.
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #426 routable nets have only global wires.
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Routed nets constraints summary:
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #        Rules   Unconstrained
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #      Default            426
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #        Total            426
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Routing constraints summary of the whole design:
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #        Rules   Unconstrained
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #      Default            426
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #        Total            426
[04/17 23:41:16    48s] #-----------------------------
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #  Congestion Analysis: (blocked Gcells are excluded)
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #               OverCon       OverCon       OverCon
[04/17 23:41:16    48s] #                #Gcell        #Gcell        #Gcell    %Gcell
[04/17 23:41:16    48s] #    Layer         (1-2)         (3-4)          (5)   OverCon
[04/17 23:41:16    48s] #  -------------------------------------------------------------
[04/17 23:41:16    48s] #   Metal 1      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
[04/17 23:41:16    48s] #   Metal 2      6(2.31%)      0(0.00%)      1(0.38%)   (2.69%)
[04/17 23:41:16    48s] #   Metal 3      1(0.39%)      0(0.00%)      0(0.00%)   (0.39%)
[04/17 23:41:16    48s] #   Metal 4      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
[04/17 23:41:16    48s] #   Metal 5      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
[04/17 23:41:16    48s] #   Metal 6      0(0.00%)      0(0.00%)      0(0.00%)   (0.00%)
[04/17 23:41:16    48s] #  -------------------------------------------------------------
[04/17 23:41:16    48s] #     Total      7(0.44%)      0(0.00%)      1(0.06%)   (0.51%)
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #  The worst congested Gcell overcon (routing demand over resource in number of tracks) = 5
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Complete Global Routing.
[04/17 23:41:16    48s] #Total wire length = 13718 um.
[04/17 23:41:16    48s] #Total half perimeter of net bounding box = 15624 um.
[04/17 23:41:16    48s] #Total wire length on LAYER metal1 = 216 um.
[04/17 23:41:16    48s] #Total wire length on LAYER metal2 = 4616 um.
[04/17 23:41:16    48s] #Total wire length on LAYER metal3 = 5953 um.
[04/17 23:41:16    48s] #Total wire length on LAYER metal4 = 2191 um.
[04/17 23:41:16    48s] #Total wire length on LAYER metal5 = 648 um.
[04/17 23:41:16    48s] #Total wire length on LAYER metal6 = 95 um.
[04/17 23:41:16    48s] #Total number of vias = 2045
[04/17 23:41:16    48s] #Up-Via Summary (total 2045):
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #-----------------------
[04/17 23:41:16    48s] #  Metal 1         1218
[04/17 23:41:16    48s] #  Metal 2          624
```

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[04/17 23:41:16    48s] #  Metal 3          157
[04/17 23:41:16    48s] #  Metal 4           45
[04/17 23:41:16    48s] #  Metal 5            1
[04/17 23:41:16    48s] #-----------------------
[04/17 23:41:16    48s] #                 2045
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Max overcon = 5 tracks.
[04/17 23:41:16    48s] #Total overcon = 0.51%.
[04/17 23:41:16    48s] #Worst layer Gcell overcon rate = 0.39%.
[04/17 23:41:16    48s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.44 (MB), peak = 549.45 (MB)
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Start data preparation for track assignment...
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #Data preparation is done on Wed Apr 17 23:41:16 2019
[04/17 23:41:16    48s] #
[04/17 23:41:16    48s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.46 (MB), peak = 549.46 (MB)
[04/17 23:41:16    48s] #Start Track Assignment.
[04/17 23:41:16    49s] #Done with 385 horizontal wires in 1 hboxes and 443 vertical wires in 1 hboxes.
[04/17 23:41:16    49s] #Done with 64 horizontal wires in 1 hboxes and 88 vertical wires in 1 hboxes.
[04/17 23:41:16    49s] #Complete Track Assignment.
[04/17 23:41:16    49s] #Total wire length = 13100 um.
[04/17 23:41:16    49s] #Total half perimeter of net bounding box = 15624 um.
[04/17 23:41:16    49s] #Total wire length on LAYER metal1 = 206 um.
[04/17 23:41:16    49s] #Total wire length on LAYER metal2 = 4279 um.
[04/17 23:41:16    49s] #Total wire length on LAYER metal3 = 5732 um.
[04/17 23:41:16    49s] #Total wire length on LAYER metal4 = 2155 um.
[04/17 23:41:16    49s] #Total wire length on LAYER metal5 = 632 um.
[04/17 23:41:16    49s] #Total wire length on LAYER metal6 = 95 um.
[04/17 23:41:16    49s] #Total number of vias = 2045
[04/17 23:41:16    49s] #Up-Via Summary (total 2045):
[04/17 23:41:16    49s] #
[04/17 23:41:16    49s] #-----------------------
[04/17 23:41:16    49s] #  Metal 1         1218
[04/17 23:41:16    49s] #  Metal 2          624
[04/17 23:41:16    49s] #  Metal 3          157
[04/17 23:41:16    49s] #  Metal 4           45
[04/17 23:41:16    49s] #  Metal 5            1
[04/17 23:41:16    49s] #-----------------------
[04/17 23:41:16    49s] #                 2045
[04/17 23:41:16    49s] #
[04/17 23:41:16    49s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 518.20 (MB), peak = 549.48 (MB)
[04/17 23:41:16    49s] #
[04/17 23:41:16    49s] #Cpu time = 00:00:00
[04/17 23:41:16    49s] #Elapsed time = 00:00:00
[04/17 23:41:16    49s] #Increased memory = 5.61 (MB)
[04/17 23:41:16    49s] #Total memory = 518.20 (MB)
[04/17 23:41:16    49s] #Peak memory = 549.48 (MB)
[04/17 23:41:16    49s] #
[04/17 23:41:16    49s] #Start Detail Routing..
[04/17 23:41:16    49s] #start initial detail routing ...
[04/17 23:41:16    49s] #    number of violations = 0
[04/17 23:41:16    49s] #cpu time = 00:00:01, elapsed time = 00:00:01, memory = 557.19 (MB), peak = 557.19 (MB)
[04/17 23:41:16    49s] #start 1st optimization iteration ...
[04/17 23:41:16    49s] #    number of violations = 0
[04/17 23:41:16    49s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 557.19 (MB), peak = 557.19 (MB)
[04/17 23:41:16    49s] #Complete Detail Routing.
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[04/17 23:41:16 49s] #Total wire length = 13834 um.
[04/17 23:41:16 49s] #Total half perimeter of net bounding box = 15624 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal1 = 844 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal2 = 5706 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal3 = 6167 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal4 = 927 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal5 = 98 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal6 = 92 um.
[04/17 23:41:16 49s] #Total number of vias = 2309
[04/17 23:41:16 49s] #Up-Via Summary (total 2309):
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #-----------------------
[04/17 23:41:16 49s] # Metal 1 1257
[04/17 23:41:16 49s] # Metal 2 960
[04/17 23:41:16 49s] # Metal 3 82
[04/17 23:41:16 49s] # Metal 4 9
[04/17 23:41:16 49s] # Metal 5 1
[04/17 23:41:16 49s] #-----------------------
[04/17 23:41:16 49s] # 2309
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Total number of DRC violations = 0
[04/17 23:41:16 49s] #Cpu time = 00:00:01
[04/17 23:41:16 49s] #Elapsed time = 00:00:01
[04/17 23:41:16 49s] #Increased memory = 39.01 (MB)
[04/17 23:41:16 49s] #Total memory = 557.20 (MB)
[04/17 23:41:16 49s] #Peak memory = 557.20 (MB)
[04/17 23:41:16 49s] #WARNING (NRDB-2005) SPECIAL_NET gnd has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
[04/17 23:41:16 49s] #WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Start Post Route wire spreading..
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Start data preparation for wire spreading...
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Data preparation is done on Wed Apr 17 23:41:16 2019
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 557.22 (MB), peak = 557.22 (MB)
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Spread distance (# of tracks): min = 0.500000; max = 2.000000
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Start Post Route Wire Spread.
[04/17 23:41:16 49s] #Done with 130 horizontal wires in 1 hboxes and 67 vertical wires in 1 hboxes.
[04/17 23:41:16 49s] #Complete Post Route Wire Spread.
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Total wire length = 14149 um.
[04/17 23:41:16 49s] #Total half perimeter of net bounding box = 15624 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal1 = 844 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal2 = 5778 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal3 = 6392 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal4 = 945 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal5 = 98 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal6 = 92 um.
[04/17 23:41:16 49s] #Total number of vias = 2309
[04/17 23:41:16 49s] #Up-Via Summary (total 2309):
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #-----------------------

[04/17 23:41:16 49s] # Metal 1 1257
[04/17 23:41:16 49s] # Metal 2 960
[04/17 23:41:16 49s] # Metal 3 82
[04/17 23:41:16 49s] # Metal 4 9
[04/17 23:41:16 49s] # Metal 5 1
[04/17 23:41:16 49s] #-----------------------
[04/17 23:41:16 49s] # 2309
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 524.57 (MB), peak = 557.23 (MB)
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Post Route wire spread is done.
[04/17 23:41:16 49s] #Total wire length = 14149 um.
[04/17 23:41:16 49s] #Total half perimeter of net bounding box = 15624 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal1 = 844 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal2 = 5778 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal3 = 6392 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal4 = 945 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal5 = 98 um.
[04/17 23:41:16 49s] #Total wire length on LAYER metal6 = 92 um.
[04/17 23:41:16 49s] #Total number of vias = 2309
[04/17 23:41:16 49s] #Up-Via Summary (total 2309):
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #-----------------------
[04/17 23:41:16 49s] # Metal 1 1257
[04/17 23:41:16 49s] # Metal 2 960
[04/17 23:41:16 49s] # Metal 3 82
[04/17 23:41:16 49s] # Metal 4 9
[04/17 23:41:16 49s] # Metal 5 1
[04/17 23:41:16 49s] #-----------------------
[04/17 23:41:16 49s] # 2309
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #WARNING (NRDB-2005) SPECIAL_NET gnd has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
[04/17 23:41:16 49s] #WARNING (NRDB-2005) SPECIAL_NET vdd has special wires but no definitions for instance pins or top level pins. This will cause routability problems later.
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #Start DRC checking..
[04/17 23:41:16 49s] # number of violations = 0
[04/17 23:41:16 49s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.03 (MB), peak = 557.23 (MB)
[04/17 23:41:16 49s] # number of violations = 0
[04/17 23:41:16 49s] #cpu time = 00:00:00, elapsed time = 00:00:00, memory = 549.03 (MB), peak = 557.23 (MB)
[04/17 23:41:16 49s] #CELL_VIEW chenjie_module,init has no DRC violation.
[04/17 23:41:16 49s] #Total number of DRC violations = 0
[04/17 23:41:16 49s] #detailRoute Statistics:
[04/17 23:41:16 49s] #Cpu time = 00:00:01
[04/17 23:41:16 49s] #Elapsed time = 00:00:01
[04/17 23:41:16 49s] #Increased memory = 30.83 (MB)
[04/17 23:41:16 49s] #Total memory = 549.03 (MB)
[04/17 23:41:16 49s] #Peak memory = 557.23 (MB)
[04/17 23:41:16 49s] #
[04/17 23:41:16 49s] #globalDetailRoute statistics:
[04/17 23:41:16 49s] #Cpu time = 00:00:01
[04/17 23:41:16 49s] #Elapsed time = 00:00:01
[04/17 23:41:16 49s] #Increased memory = 69.38 (MB)
[04/17 23:41:16 49s] #Total memory = 549.15 (MB)
[04/17 23:41:16 49s] #Peak memory = 557.23 (MB)
[04/17 23:41:16 49s] #Number of warnings = 28

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[04/17 23:41:16    49s] #Total number of warnings = 30
[04/17 23:41:16    49s] #Number of fails = 0
[04/17 23:41:16    49s] #Total number of fails = 0
[04/17 23:41:16    49s] #Complete globalDetailRoute on Wed Apr 17 23:41:16 2019
[04/17 23:41:16    49s] #
[04/17 23:41:16    49s] #routeDesign: cpu time = 00:00:01, elapsed time = 00:00:01, memory = 549.15 (MB), peak = 557.23 (MB)
[04/17 23:41:16    49s]
[04/17 23:41:16    49s] *** Summary of all messages that are not suppressed in this session:
[04/17 23:41:16    49s] Severity  ID               Count  Summary
[04/17 23:41:16    49s] WARNING   ENCEXT-6197          1  Capacitance table file not specified. Th...
[04/17 23:41:16    49s] WARNING   ENCEXT-2882          5  Unable to find resistance for via '%s' i...
[04/17 23:41:16    49s] WARNING   ENCEXT-3530          1  The process node is not set. Use the com...
[04/17 23:41:16    49s] WARNING   ENCESI-2013       1348  The power rail of instance %s term %s ha...
[04/17 23:41:16    49s] *** Message Summary: 1355 warning(s), 0 error(s)
[04/17 23:41:16    49s]
[04/17 23:45:36    83s] <CMD> dumpToGIF chenjie_module.jpg
```