

ECEN 714 Lab 5 Report
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4-bit adder

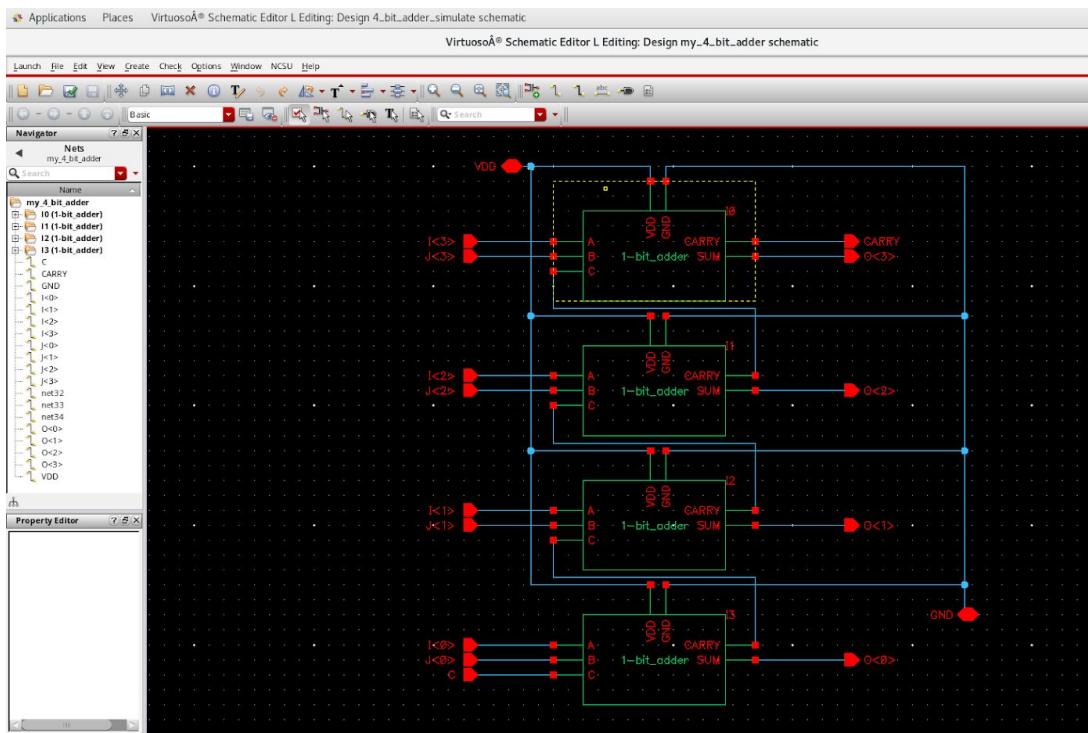


Fig.1 Schematics of my 4-bit adder

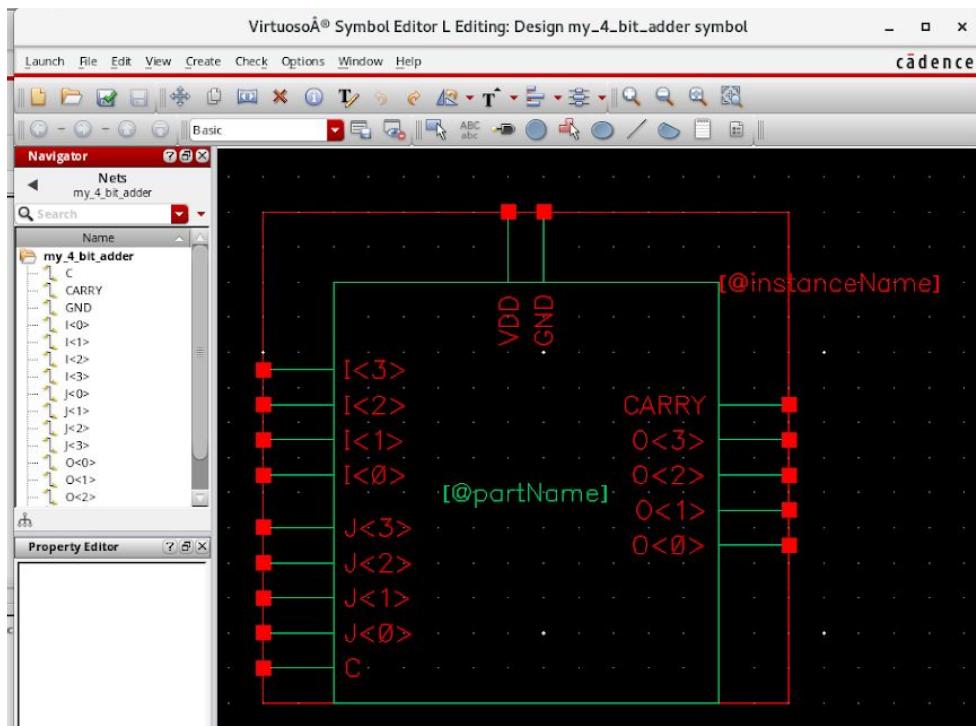


Fig.2 Symbol of my 4-bit adder



Fig.3 Layout of my 4-bit adder

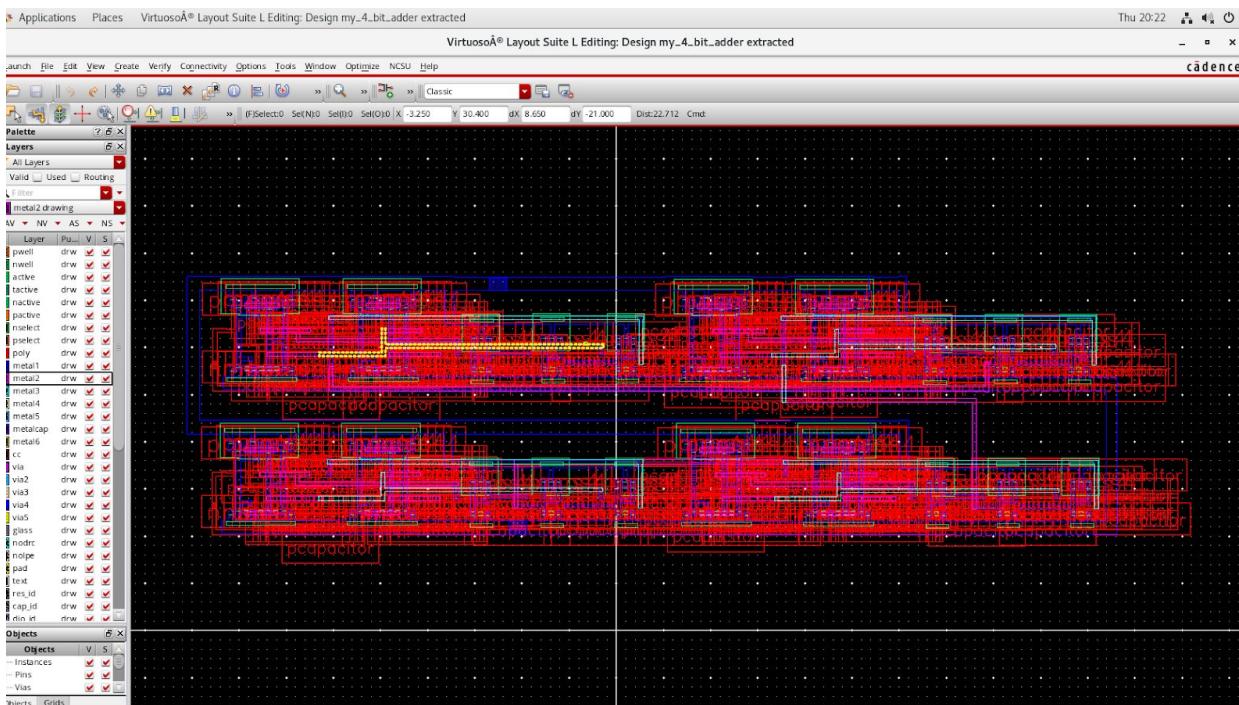


Fig.4 Extracted file from my 4-bit adder

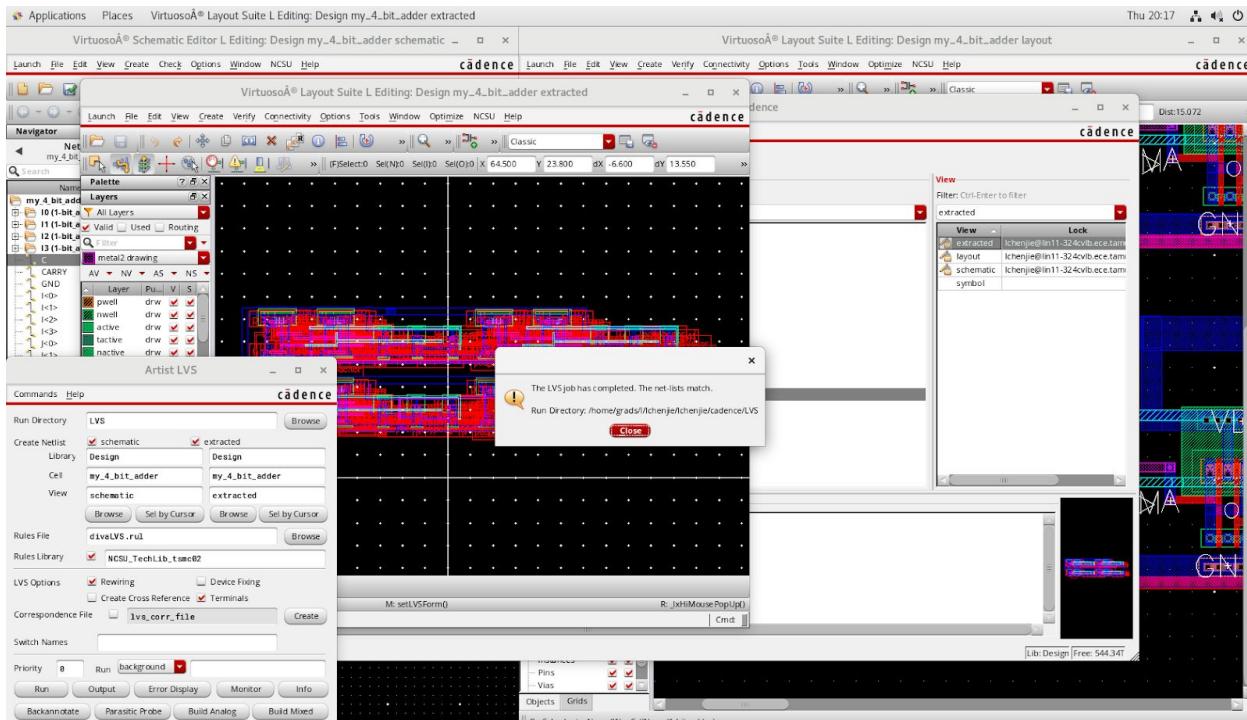


Fig.5 LVS output matches

Below is the LVS report

@(#)\$CDS: LVS version 6.1.7-64b 01/24/2017 19:46 (sjfhw310) \$

Command line: /softwares/Linux/cadence/IC617/tools.lnx86/dfl/bin/64bit/LVS -dir /home/grads/l/lchenjie/lchenjie/cadence/LVS -l -s -t
 /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout
 /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic

Like matching is enabled.

Net swapping is enabled.

Using terminal names as correspondence points.

Compiling Diva LVS rules...

```
Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout/netlist
count
91          nets
16          terminals
72          pmos
72          nmos
```

```
Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic/netlist
count
```

91	nets
16	terminals
72	pmos
72	nmos

Terminal correspondence points

N82	N18	C
N90	N0	CARRY
N79	N1	GND
N87	N6	I<0>
N86	N12	I<1>
N85	N4	I<2>
N84	N2	I<3>
N83	N14	J<0>
N81	N10	J<1>
N78	N11	J<2>
N76	N7	J<3>
N80	N17	O<0>
N77	N5	O<1>
N75	N16	O<2>
N88	N3	O<3>
N89	N8	VDD

Devices in the netlist but not in the rules:

pcapacitor

Devices in the rules but not in the netlist:

cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	144	144
total	144	144

	nets	
un-matched	0	0
merged	0	0

pruned	0	0
active	91	91
total	91	91

terminals		
un-matched	0	0
matched but different type	0	0
total	16	16

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

Audit.out:

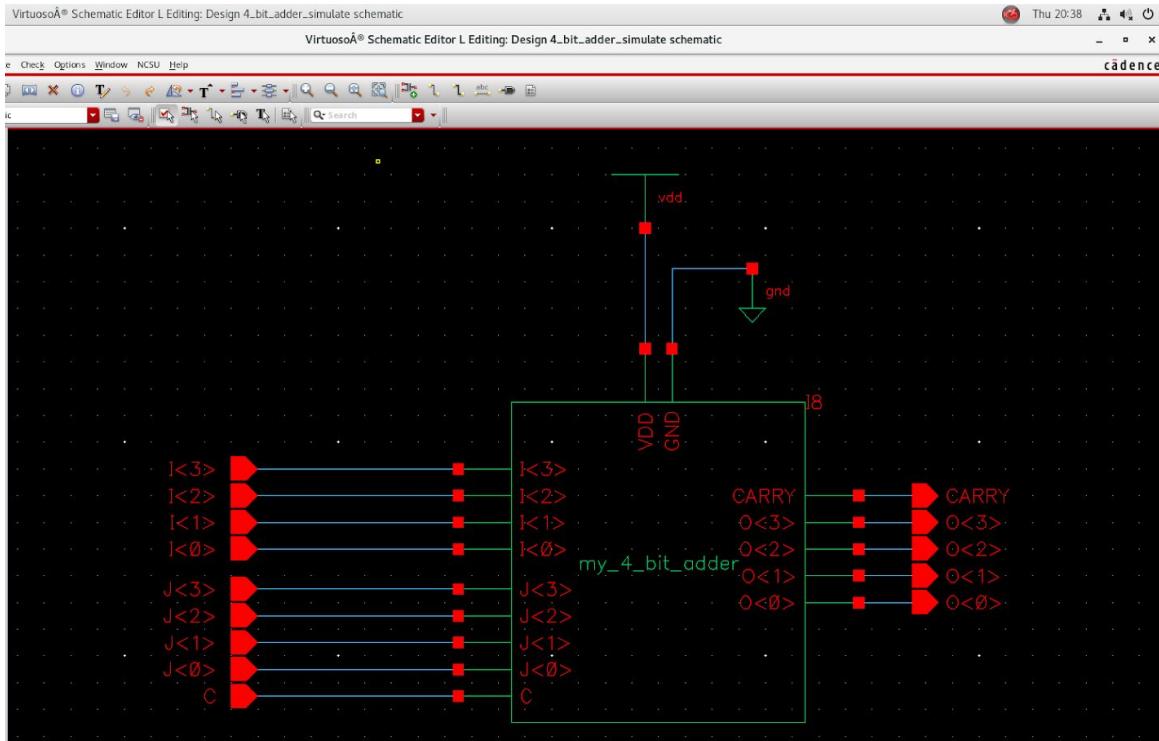


Fig.6 Simulation schematic of my 4-bit adder

```

Applications Places Text Editor
simout.tmp ~/lchenjie/cadence/4_bit_adder_simulate_run1 Save
Open ↗ simout.tmp
lhn1/cds08/netlist
lhn1/cds1/netlist
lhn1/cds2/netlist
lhn1/cds4/netlist
lhn1/cds3/netlist
hdFileDir/cds_globals.v
+nostdout
+nocopyright
+ncvlogargs+ "-neverwarn -nostdout -nocopyright"
+ncelabargs+ "-neg_tchk -nonotifier -sdf NOCheck_celltype -access +r -pulse_e 100 -pulse_r 100 -
neverwarn -timescale 1ns/1ns -nostdout -nocopyright"
+ncsimargs+ "-neverwarn -nocopyright -gui -input /home/grads/l/lchenjie/lchenjie/cadence/
4_bit_adder_simulate_run1.simTmpNCmd"
+mpsession+virtuso22667
+mpsshost+lin11-32cvlb.ece.tamu.edu
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxmode: *W,DLCVAR (/home/grads/l/lchenjie/cds.lib,1): cds.lib Invalid environment variable ''.
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxmode: *W,DLCVAR (/home/grads/l/lchenjie/cds.lib,1): cds.lib Invalid environment variable ''.
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxmode: *W,DLCVAR (/home/grads/l/lchenjie/cds.lib,1): cds.lib Invalid environment variable ''.
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxmode: *W,DLCVAR (/home/grads/l/lchenjie/cds.lib,1): cds.lib Invalid environment variable ''.
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncxmode: *W,DLCVAR (/home/grads/l/lchenjie/cds.lib,1): cds.lib Invalid environment variable ''.
SOFTINCLUDE $SYSTEM_CDS_LIB_DIR/cds.lib
|
ncsim>
Relinquished control to SimVision...
ncsim>
ncsim> source /softwares/Linux/cadence/INCISIV102/tools/inca/files/ncsimrc
ncsim> database -open shmWave -shm -default -into shm.db
Created default SHM database shmWave
ncsim> probe -create -shm test -all -depth 1
Created probe 1
ncsim> probe -create cds_globals -shm
Created probe 2
ncsim> run
      0 I<3:0>=0000, J<3:0>=0000, C=0, CARRY=0, O<3:0>=0000
      50 I<3:0>=0000, J<3:0>=1111, C=1, CARRY=1, O<3:0>=0000
      100 I<3:0>=1010, J<3:0>=0101, C=0, CARRY=0, O<3:0>=1111
      150 I<3:0>=1010, J<3:0>=0101, C=1, CARRY=1, O<3:0>=0000
      200 I<3:0>=1100, J<3:0>=1000, C=0, CARRY=1, O<3:0>=0100
ncsim>

```

Fig.7 Simulation output

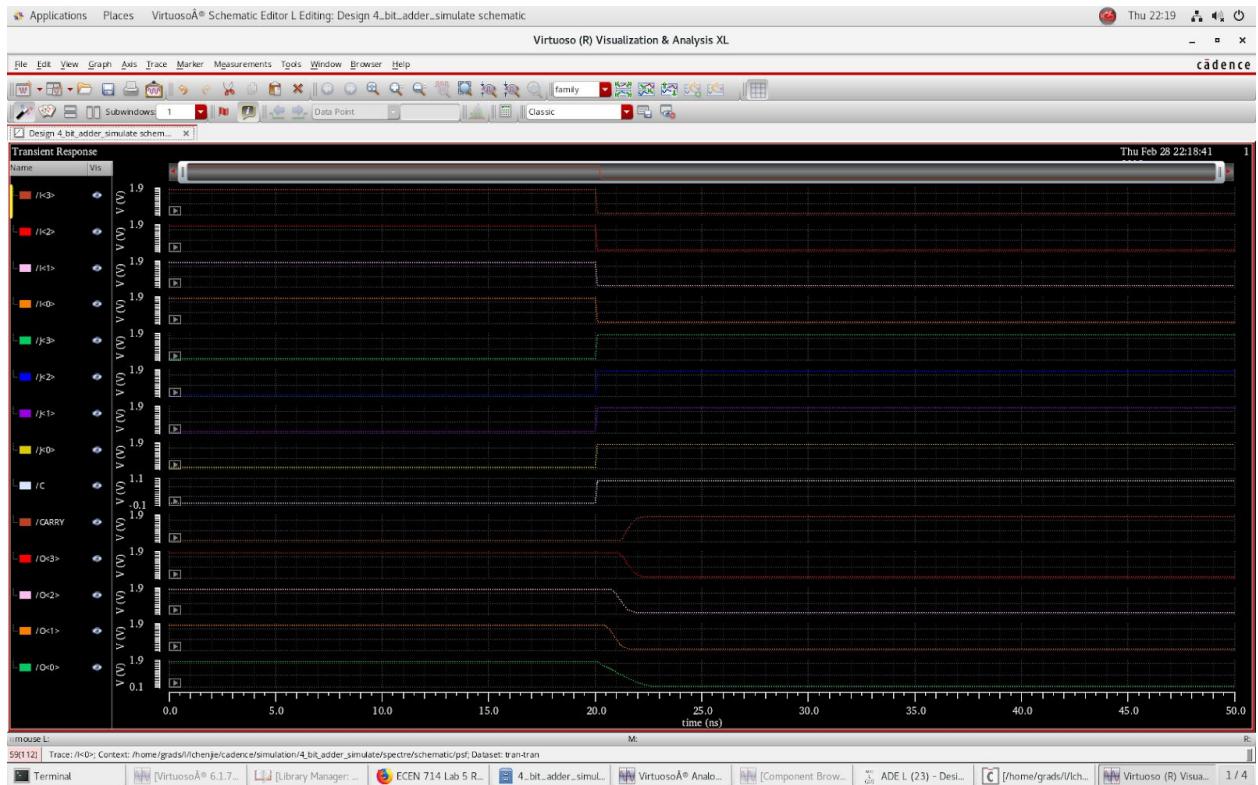


Fig.8 0000+1111 carry in 1

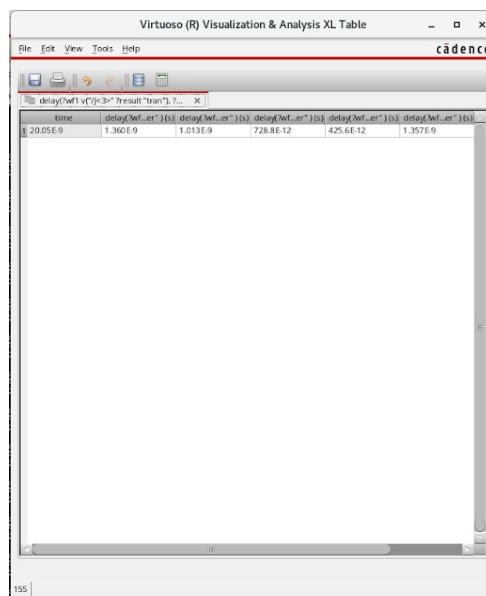


Fig.9 O<3:0> and CARRY delay

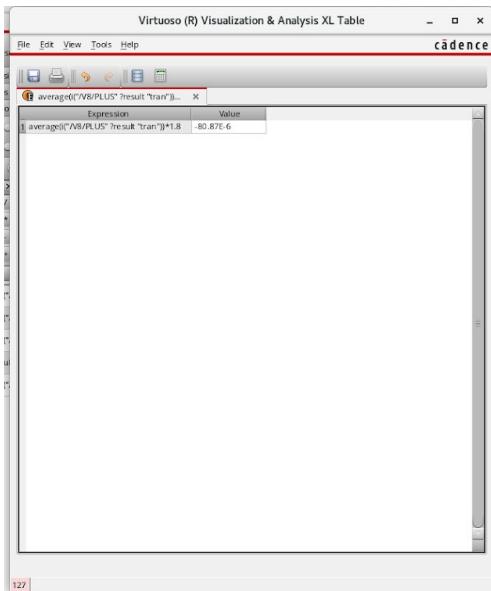


Fig.10 Power of first case

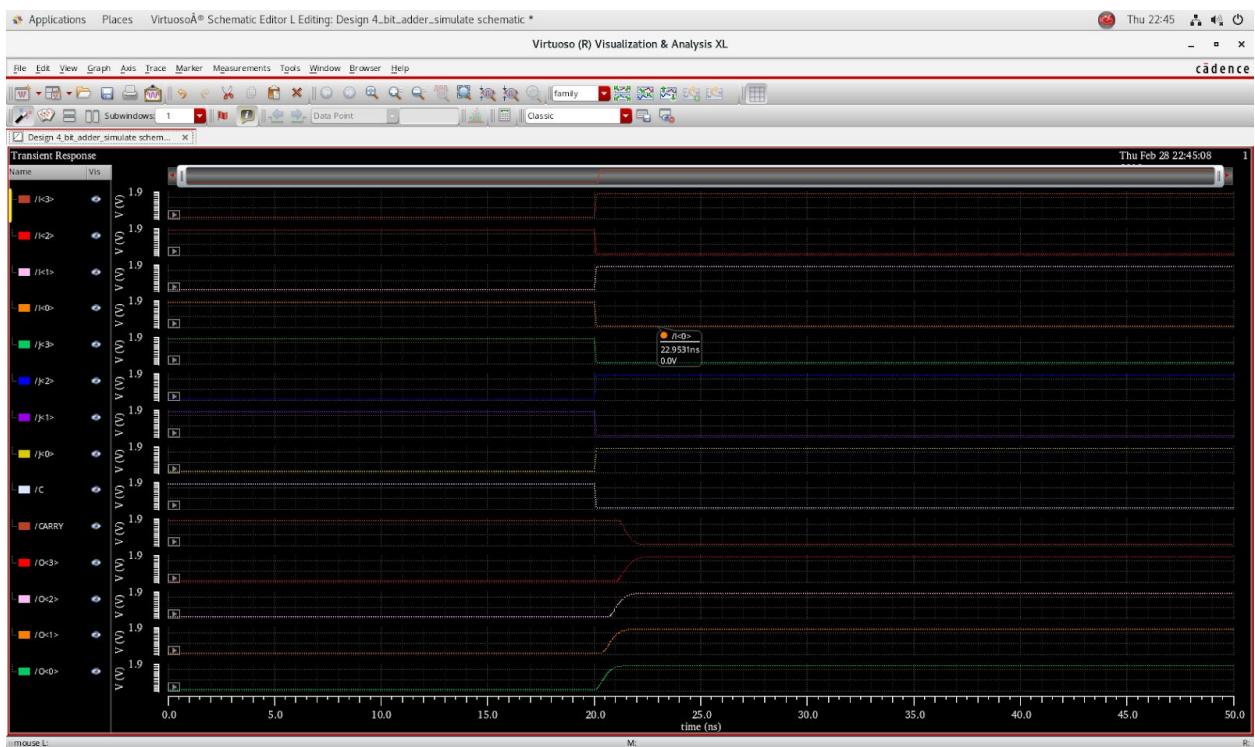


Fig. 11 1010+0101 carry in 0

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help cādence

delay(Wf_V[7]<3>"result "tran"),7...

time	delay(?) (s)	delay(Wf_en") (s)	delay(Wf_en") (s)	delay(Wf_en") (s)	delay(Wf_en") (s)
2.05E-9	1.438E-9	1.055E-9	736.0E-12	420.1E-12	1.472E-9

135 | Trace /O>2; Context: /home/grads/kchen/jcadence/simulation4_bit_adder_simulate/spectre/schematic/pdf; Data

Fig. 12 Delay of O<3:0> and CARRY

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help cādence

average("V8/PLUS" result "tran")...

Expression	Value
average("V8/PLUS" result "tran")*1.8	-23.05E-6

134 |

Fig. 13 Power on second case

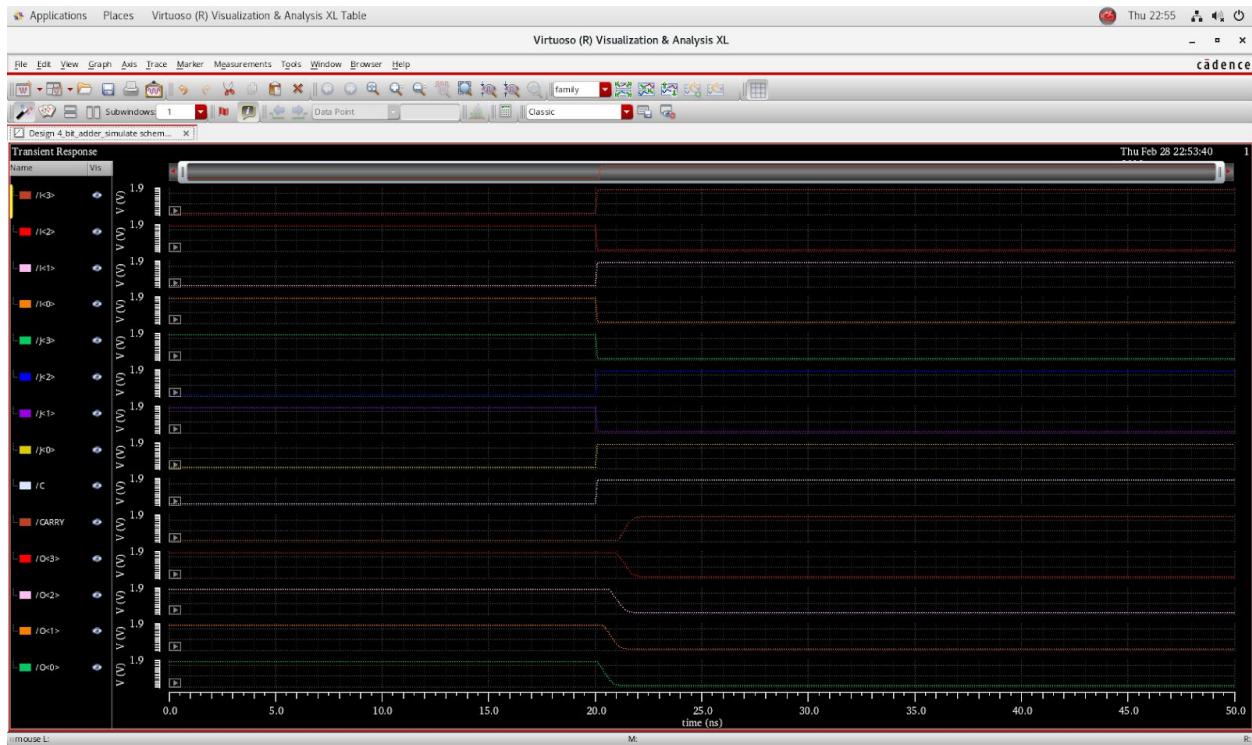


Fig. 14 $1010 + 0101$ carry in 1

Virtuoso (R) Visualization & Analysis XL Table					
time	delay(wf1.v["/J<3>"]?result="tran")	delay(wf1_cr")	delay(wf1_cr")	delay(wf1_cr")	delay(wf1_cr")
2.05E-9	1.356E-9	1.009E-9	725.3E-12	425.6E-12	1.353E-9

Fig. 15 O<3:0> and CARRY delay

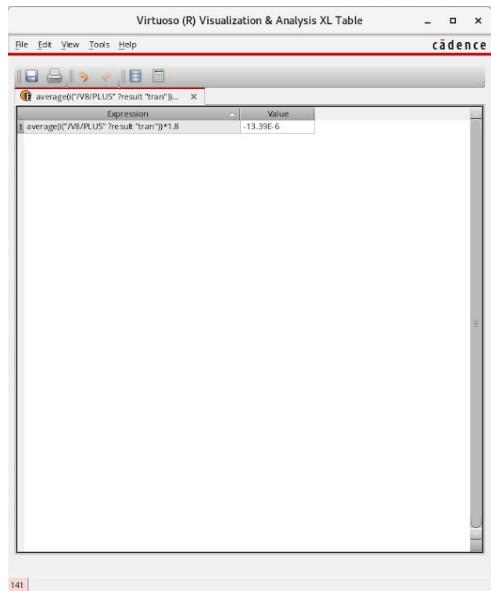


Fig. 16 Power of third case

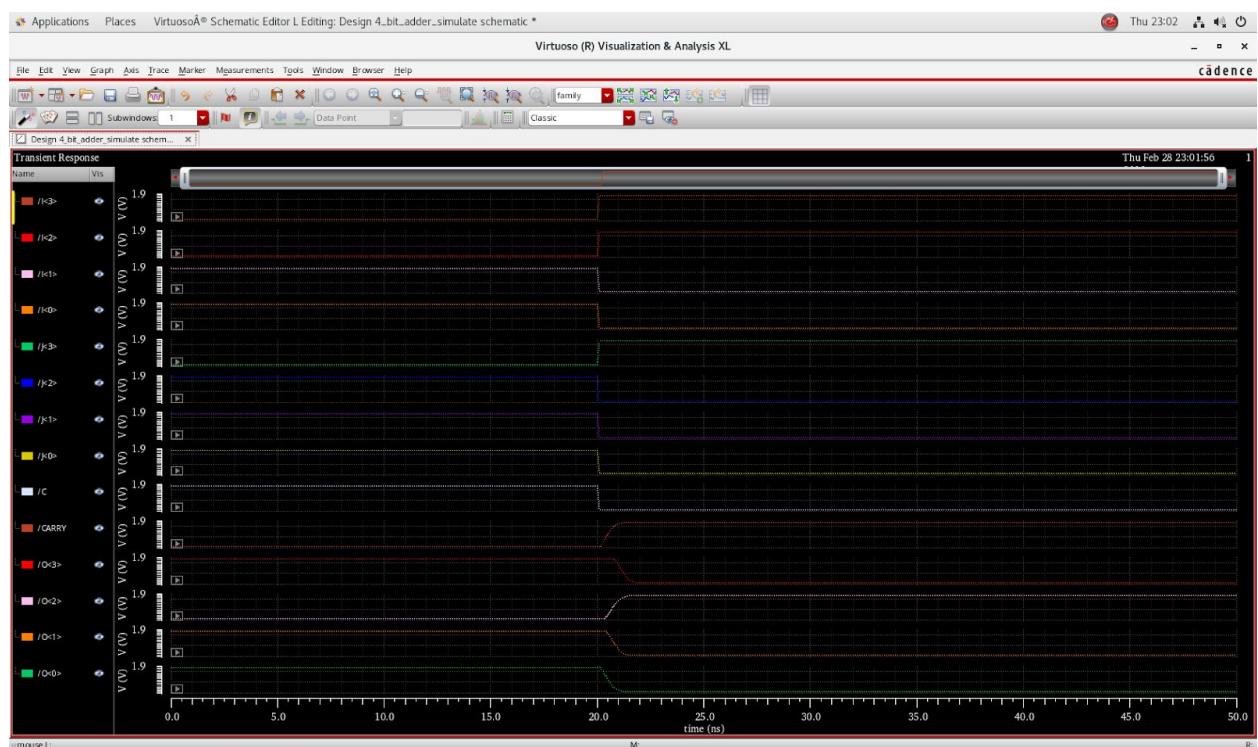


Fig. 17 1100 + 1000 carry in 0

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help

delay(wf.vf?>3>?result="tran");...

time	delay(wf..er") (s)				
2.05E-9	1.120E-9	691.0E-12	743.8E-12	467.4E-12	438.2E-12

Fig. 18 O<3:0> and CARRY delay

Virtuoso (R) Visualization & Analysis XL Table

File Edit View Tools Help

average@("VB/PLUS"?result="tran");...

Expression	Value
average@("VB/PLUS"?result="tran")@1.8	-17.57E-6

Fig. 19 Power on fourth case