ECEN714 lab3 report
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1. Inverter

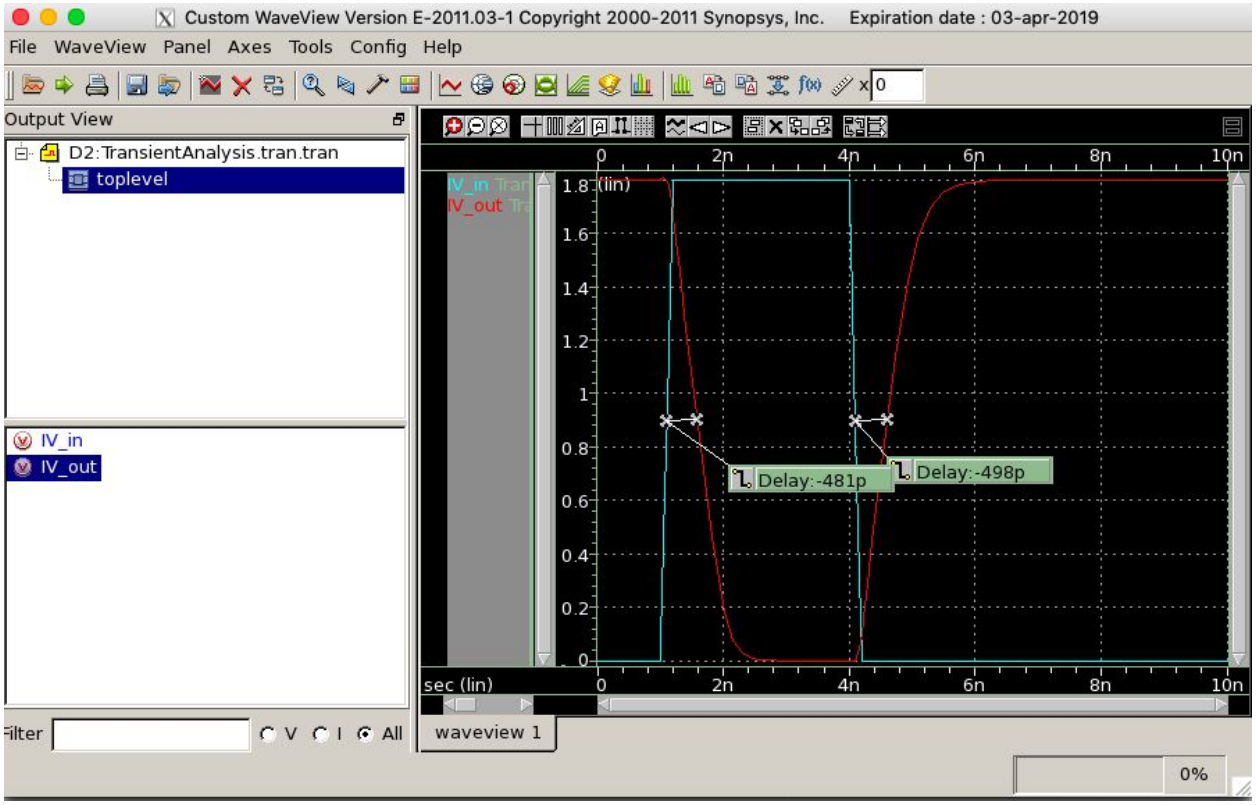

Fig.1 waveforms of Vin and Vout

The rising delay is 497ps and falling delay is 403ps.

Capacitance	Rising delay	Error ratio on rising delay	Falling delay	Error ratio on falling delay
1f	45.2	0.400442478	27.1	0.667896679
10f	101	0.15049505	85.8	0.177156177
20f	144	0.090277778	131	0.099236641
25f	166	0.078313253	153	0.08496732
30f	188	0.069148936	175	0.074285714

40f	232	0.056034483	219	0.059360731
45f	255	0.058823529	240	0.0625
50f	277	0.054151625	262	0.057251908
60f	321	0.046728972	306	0.049019608
70f	368	0.046195652	351	0.048433048
75f	389	0.043701799	372	0.045698925
80f	410	0.041463415	393	0.043256997
85f	430	0.03255814	416	0.033653846
90f	451	0.026607539	439	0.027334852
100f	498	0.034136546	481	0.035343035

Tab.1 Inverter's delay table

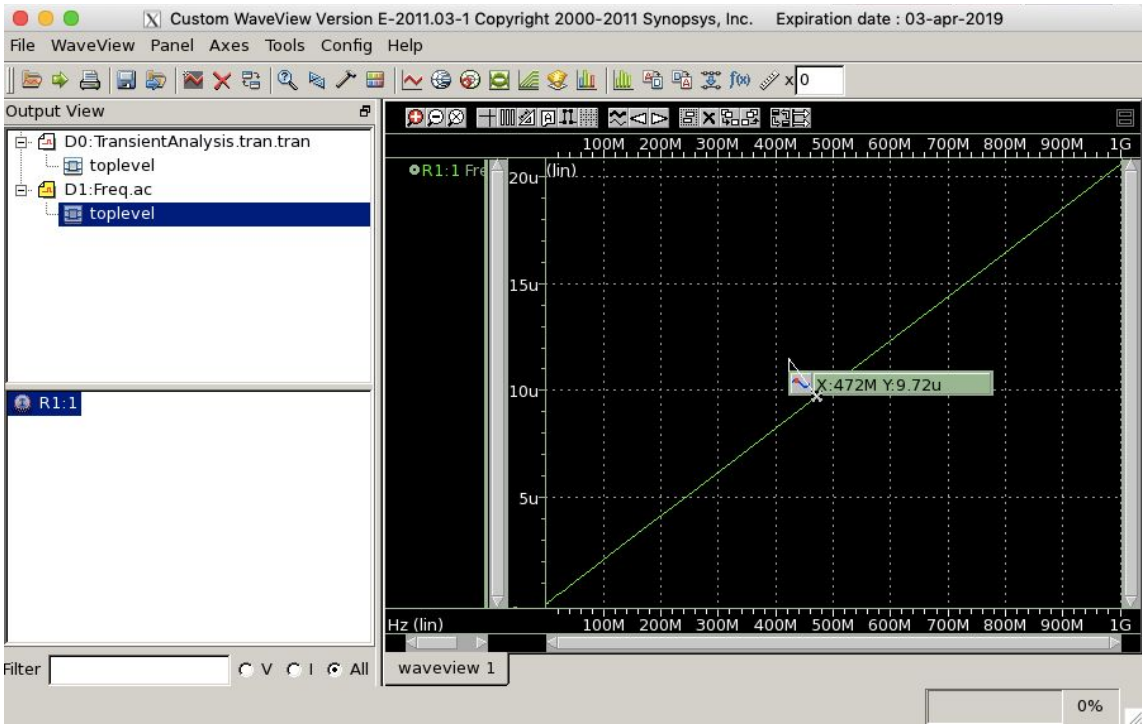

Fig.2 AC simulation of inverter

Ten samples from AC simulation:

Frequency(MHz)	Current(uA)	Capacitance(fF)
147	3.02	3.271
204	4.2	3.278
251	5.17	3.279
313	6.44	3.276
340	7	3.278
391	8.04	3.274
416	8.57	3.244
466	9.59	3.278
547	11.3	3.289
620	12.8	3.287

The average sink capacitance is 3.27fF

2. NAND

Capacitance	Rising delay	Error ratio on rising delay	Falling delay	Error ratio on falling delay
1f	57.7	0.386481802	35.4	0.629943503
10f	125	0.144	107	0.168224299
20f	189	0.111111111	168	0.125
25f	221	0.104072398	198	0.116161616
30f	254	0.098425197	229	0.109170306
40f	320	0.090625	291	0.099656357
45f	349	0.083094556	320	0.090625
50f	382	0.081151832	351	0.088319088
60f	447	0.073825503	414	0.079710145
70f	511	0.072407045	474	0.078059072
75f	541	0.068391867	504	0.073412698
80f	575	0.073043478	533	0.07879925
85f	605	0.066115702	565	0.07079646
90f	637	0.065934066	595	0.070588235
100f	701	0.064194009	656	0.068597561

Tab.2 NAND delay table

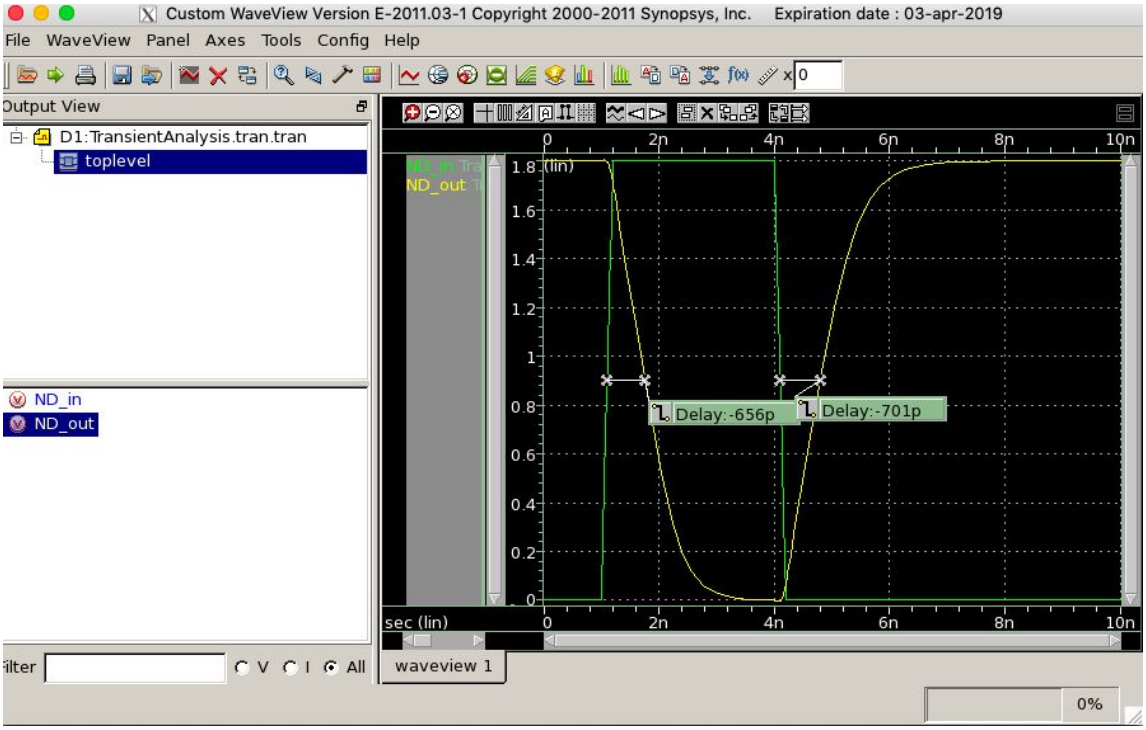

Fig.3 NAND rising delay and falling delay

The rising delay is 701 ps and falling delay is 656 ps

10 sample points picked out from AC analysis:

Frequency	Current	Capacitance(fF)
272M	5.6u	3.278
359M	7.38u	3.273
382M	7.85u	3.272
402M	8.27u	3.275
517M	10.6u	3.264
623M	12.8u	3.271
684M	14.1u	3.282
728M	15u	3.280
753M	15.5u	3.278
828M	17u	3.269

Thus, the average sink capacitance is 3.274 fF.

3. XOR

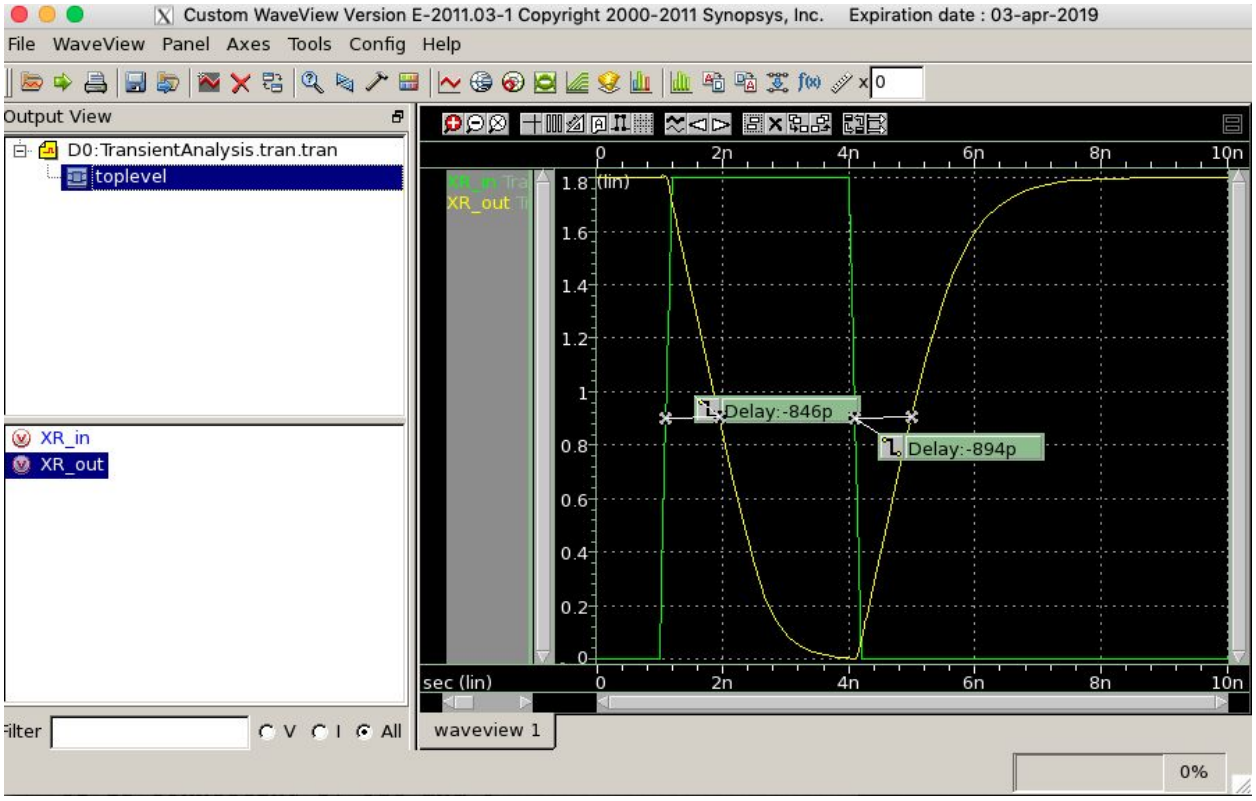

Fig.5 XOR rising delay and falling delay when C = 100fF

The rising delay is 894 ps while falling delay is 846 ps

Capacitance	Rising delay	Error ratio on rising delay	Falling delay	Error ratio on falling delay
1f	53.1	0.282485876	38.1	0.393700787
10f	137	0.138686131	118	0.161016949
20f	223	0.103139013	200	0.115
25f	266	0.093984962	241	0.10373444
30f	307	0.081433225	282	0.088652482
40f	393	0.076335878	363	0.082644628

45f	433	0.066974596	404	0.071782178
50f	475	0.065263158	444	0.06981982
60f	563	0.06749556	525	0.072380952
70f	645	0.060465116	606	0.064356436
75f	686	0.058309038	646	0.061919505
80f	728	0.057692308	686	0.06122449
85f	771	0.058365759	726	0.061983471
90f	813	0.057810578	766	0.061357702
100f	894	0.053691275	846	0.056737589

Tab. 3 XOR delay table

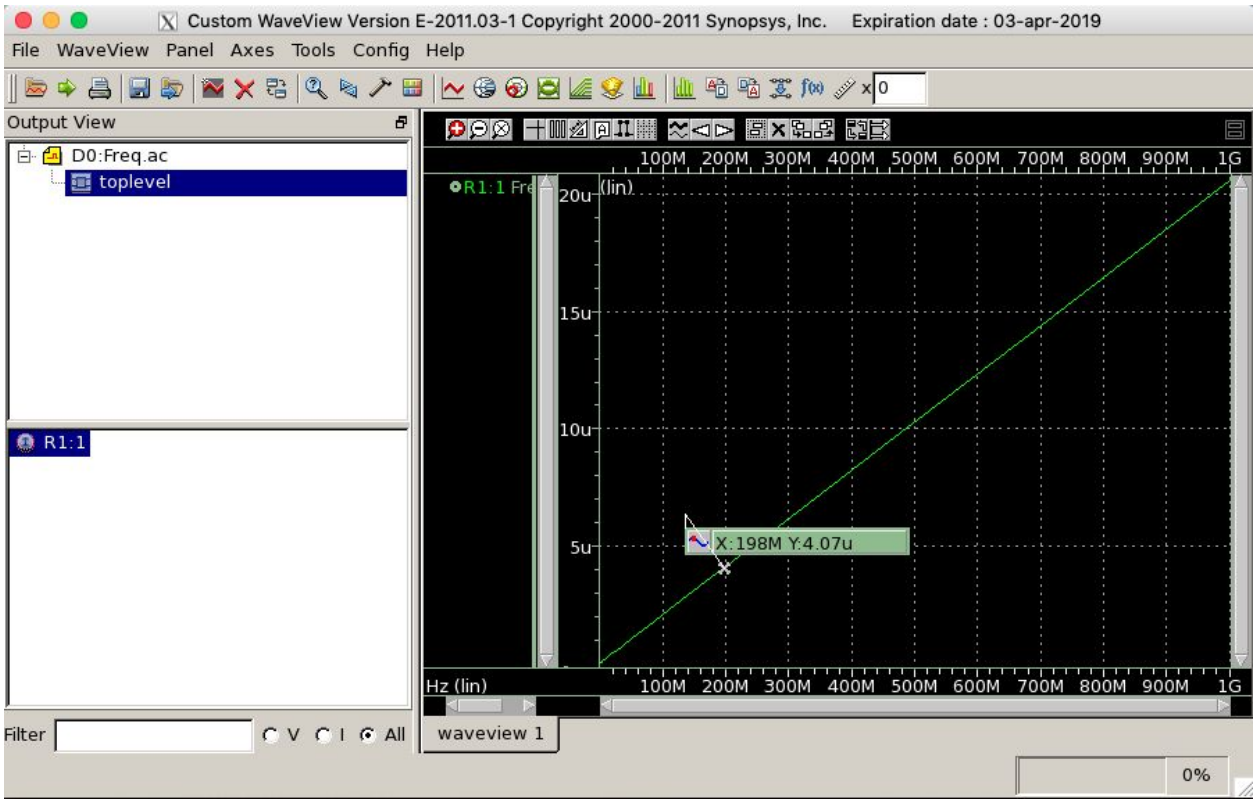

Fig. 6 XOR AC simulation

Frequency(MHz)	Current(uA)	Capacitance(fF)
198	4.07	3.273
263	5.4	3.26
323	6.65	3.278
397	8.17	3.276
444	9.15	3.281
564	11.6	3.275
595	12.2	3.265
621	12.8	3.282
659	13.6	3.286
703	14.5	3.284

The average sink capacitance is 3.277 fF.

Inverter.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/lchenjie/cadence/lab3/model18.spi"
include "~/lchenjie/cadence/lab3/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=0.6u lp=0.2u wn=0.3u ln=0.2u

;R1 (IV_out 1) resistor r=1
C1 (IV_out 0) capacitor c=10f

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

NAND.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/lchenjie/cadence/lab3/model18.spi"
include "~/lchenjie/cadence/lab3/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (ND_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (ND_in vdd ND_out vdd gnd) ND wp=0.6u lp=0.2u wn=0.3u ln=0.2u

;R1 (ND_out 1) resistor r=1
C1 (ND_out 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save ND_in ND_out
```

XOR.spi

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/lchenjie/cadence/lab3/model18.spi"
include "~/lchenjie/cadence/lab3/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (XR_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (XR_in vdd XR_out vdd gnd) XR wp=0.9u lp=0.2u wn=0.4u ln=0.2u wp1=0.9u lp=0.2u
wn=0.2u ln=0.2u

;R1 (XR_out 1) resistor r=1
C1 (XR_out 0) capacitor c=90f

TransientAnalysis tran start=0 stop=10ns step=1ps
save XR_in XR_out
```

cell18.spi

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
	parameters wp=0.9u lp=0.2u wn=0.4u ln=0.2u
	M1 output input VDD VDD tsmc18P w=wp l=lp
	M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV

subckt ND (input1 input2 output VDD VSS)
	parameters wp=0.9u lp=0.2u wn=0.4u ln=0.2u
	M1 output input1 VDD VDD tsmc18P w=wp l=lp
	M2 output input2 VDD VDD tsmc18P w=wp l=lp
	M3 temp input2 VSS VSS tsmc18N w=wn l=ln
	M4 output input1 temp VSS tsmc18N w=wn l=ln
ends ND

subckt XR (input1 input2 output VDD VSS)
	parameters wp=0.9u lp=0.2u wn=0.4u ln=0.2u wp1=0.9u lp1=0.2u wn1=0.15u ln1=0.2u
	M1 ivA input1 VDD VDD tsmc18P w=wp l=lp
	M2 VSS input1 ivA VSS tsmc18N w=wn l=ln
	M3 ivB input2 VDD VDD tsmc18P w=wp l=lp
	M4 VSS input2 ivB VSS tsmc18N w=wn l=ln

	M5 temp1 input2 VDD VDD tsmc18P w=wp1 l=lp1
	M6 output ivA temp1 VDD tsmc18P w=wp1 l=lp1
	M7 temp2 ivB VDD VDD tsmc18P w=wp1 l=lp1
	M8 output input1 temp2 VDD tsmc18P w=wp1 l=lp1

	M9 output ivA temp3 VSS tsmc18N w=wn1 l=ln1
	M10 temp3 ivB VSS VSS tsmc18N w=wn1 l=ln1
	M11 output input1 temp4 VSS tsmc18N w=wn1 l=ln1
	M12 temp4 input2 VSS VSS tsmc18N w=wn1 l=ln1
ends XR
```