ECEN 714 Lab 11
Chenjie Luo

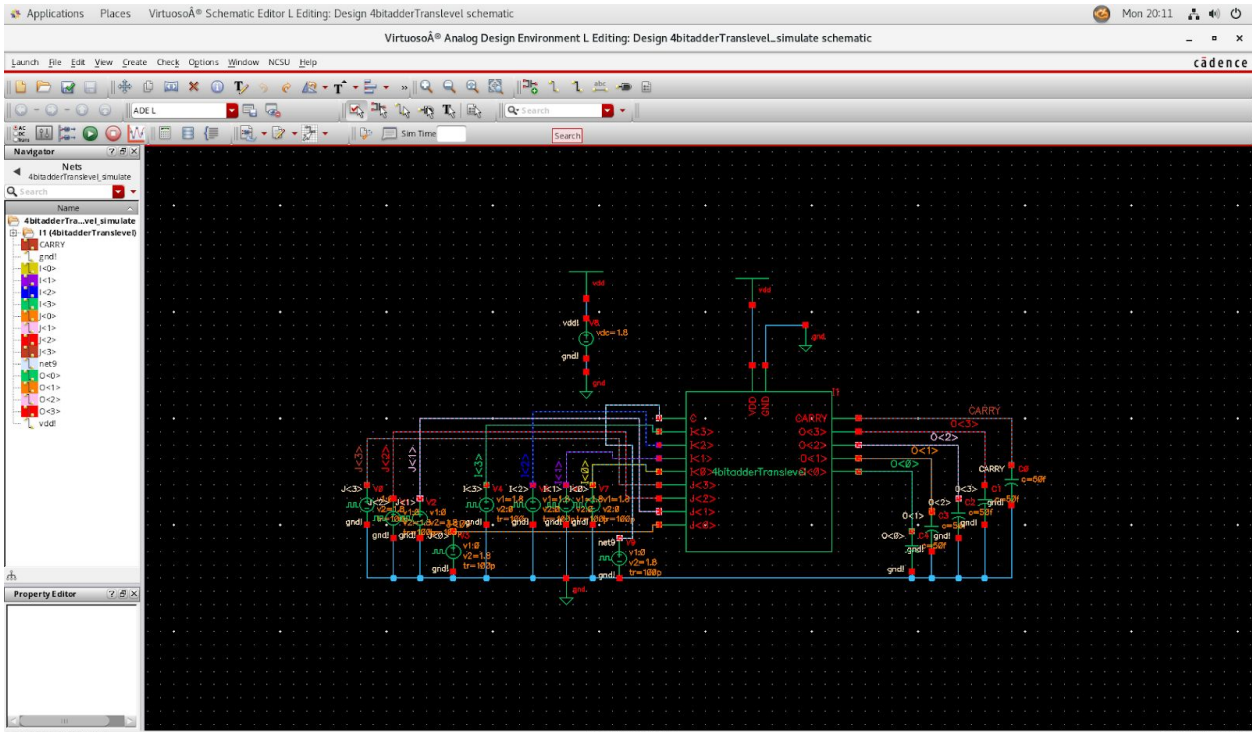

Fig. 1 Simulation of my 4-bit adder

The critical path is the path starting from I<0> or J<0> pass one XOR(stage 1) and then NAND(stage 2) and NAND(stage 3) and then go through second one-bit adder from C to CARRY and go on. In the end, the path will exit at CARRY. Until now the whole path consists of 1 XOR and 8 NAND gates.

Firstly, $G = \pi g_i$, and for the ~~longest~~ critical path, there are 8 NAND gates and 1 XOR.

$g_{NAND} = \frac{C_{in}}{C_{inverter}} = 1.1875$

$g_{XOR} = \frac{2(W_P + W_N)}{\frac{1}{2}(W_P + W_N)} = 4$

As for electrical effort, since we have our design size from lab 4 and lab 5,

$H = \frac{C_{out-path}}{C_{in-path}} = \frac{C_{load}}{C_{input}} = \frac{30\times10^{-15}F}{\text{size of XOR} \times \text{Gate capacitance of XOR}} = 3.87$

And size of XOR = size of Inverter + NMOS + PMOS = 0.9 + 0.4 + 1.2 + 0.3 = 2.8μm.

And Branching effort.

$b_i = \frac{C_{XOR}+C_{NAND}}{C_{XOR}} \cdot \frac{C_{XOR}+C_{NAND}}{C_{NAND}} = 4$, $i = 1, 2, 3$

$b_i = \left(\frac{C_{XOR}+C_{NAND}}{C_{NAND}}\right)^3 = 8.01$, $i = 4, \cdots, 9$

So $B = \pi b_i = 1.69\times10^7$

Thus, $f = (GBH)^{\frac{1}{4}} = 10.038$

Take new $f_{new} = 3$, which is between 2.7 and 4.

Thus, take into $C_{out}' = \begin{cases} C_{in(next\ stage)} + C_{XOR} & \text{for stage } 1,3,5,7 \\ C_{in(next\ stage)} & \text{for stage } 2,4,6,8,9 \end{cases}$

Then set $C_{out\ new} = \max(C_{out}', C_{out\_old})$ for every stage, We can get resized transistors.

For example, the last stage is NAND gate,

Firstly $C_{in} = C_{out} \cdot g_i / f = 1.187\times10^{-14}F$

And this C_{in} is also C_{out} of stage 8.

And since we set $\frac{P_{MOS}}{N_{MOS}}$ ratio $= \frac{0.65}{0.3}$

PMOS new size $= \frac{0.65}{0.3} \times \frac{\text{new } C_{in}}{\text{old } C_{in}} = 2.357$ μm

NMOS new size $= \frac{0.3}{0.65} \times$ PMOS new size $= 1.08$ μm.

Then solve for stage 8, stage 7, ···· stage 1 similarly.

Fig.2 Calculation Steps

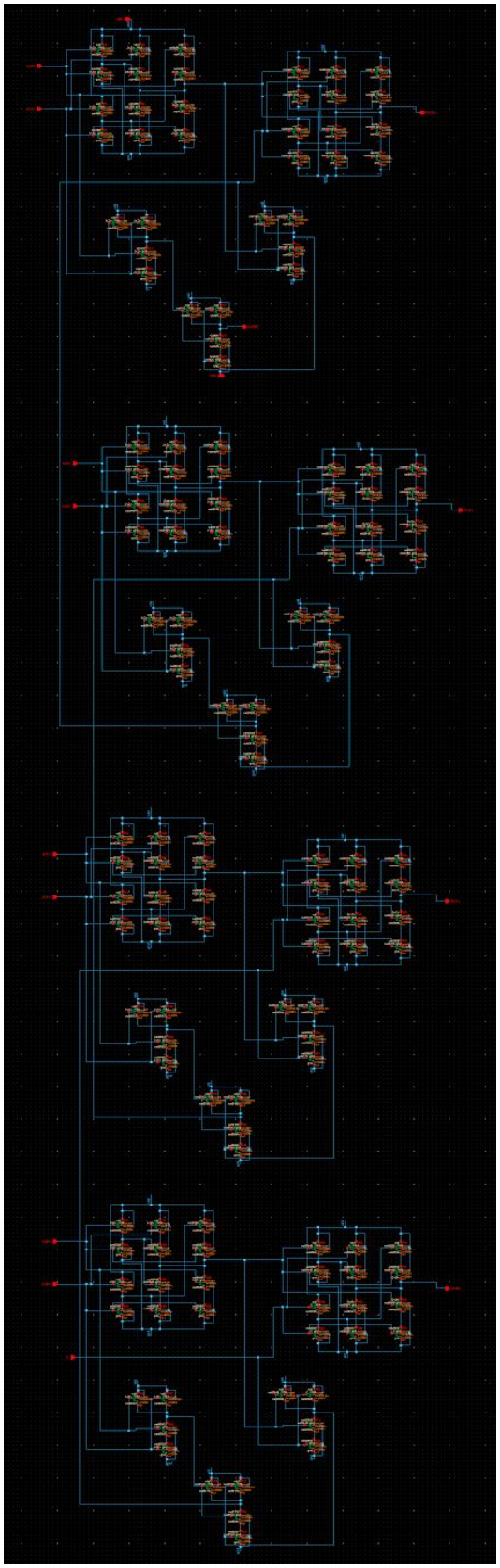

Fig. 3 Schematics of my resized 4-bit adder in transistor level

Fig. 4 Critical Path on the Schematics

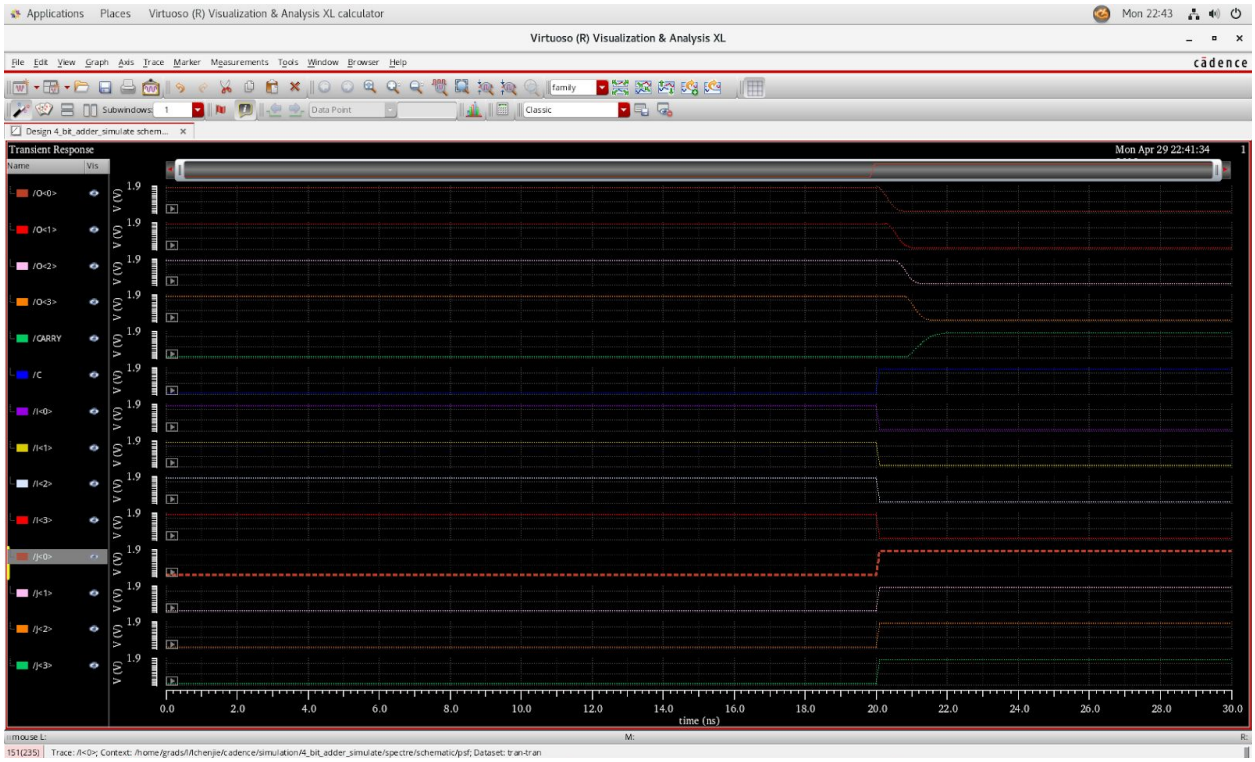

Fig.5 Waveform of 1111 + 0000 CARRY In 1

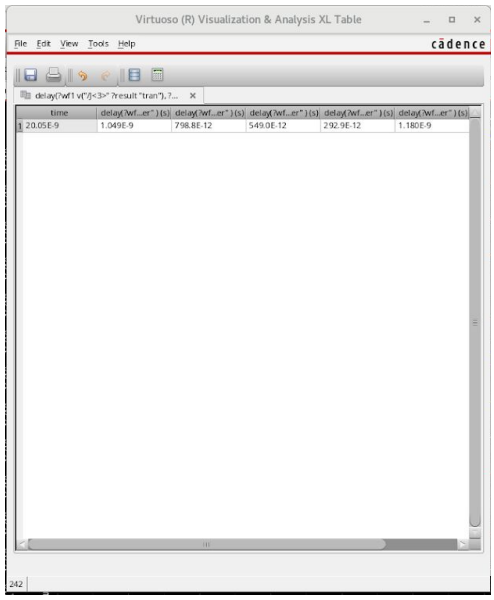

Fig. 6 Delay of O<3:0> and CARRY

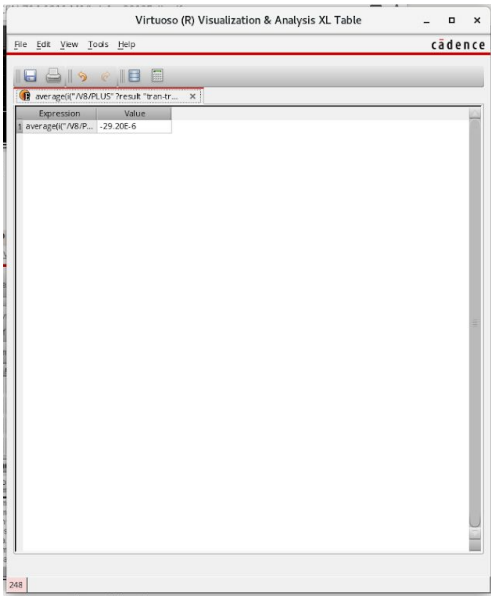

Fig. 7 Power from VDD

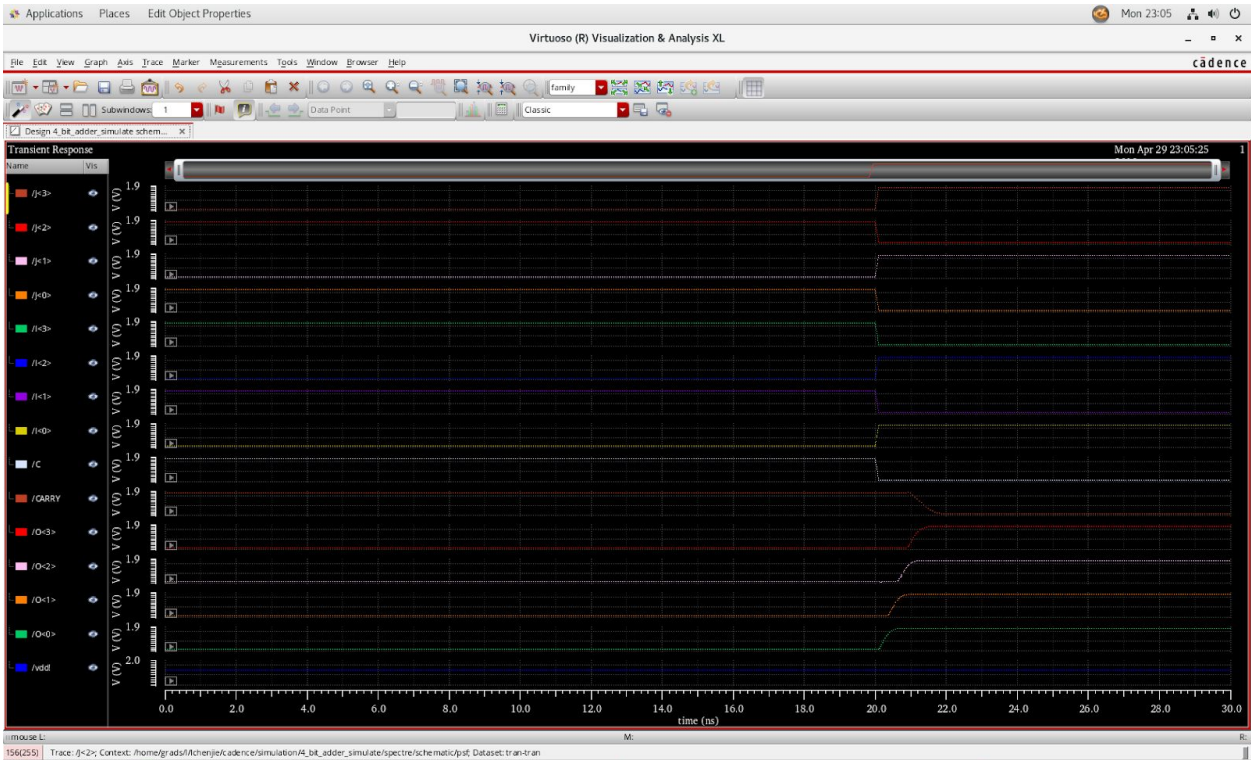

Fig. 8 1010+0101 carry in 0

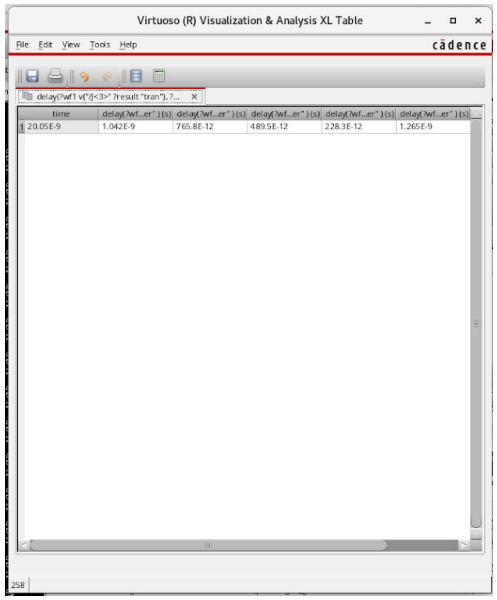

Fig. 9 Delay of O<3:0> and CARRY

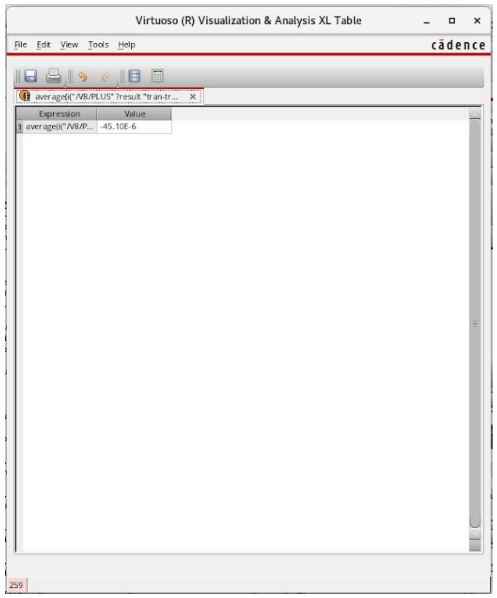

Fig.10 Power from VDD

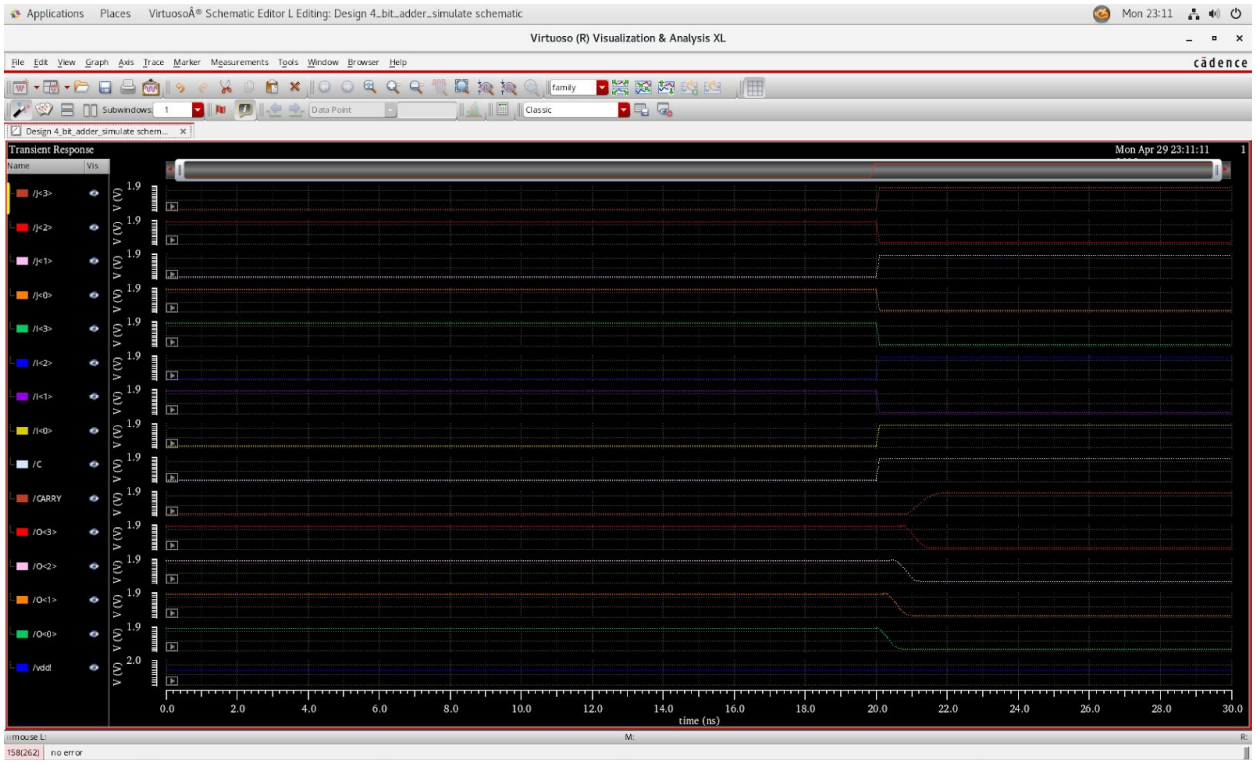

Fig. 11 1010+0101 carry in 1

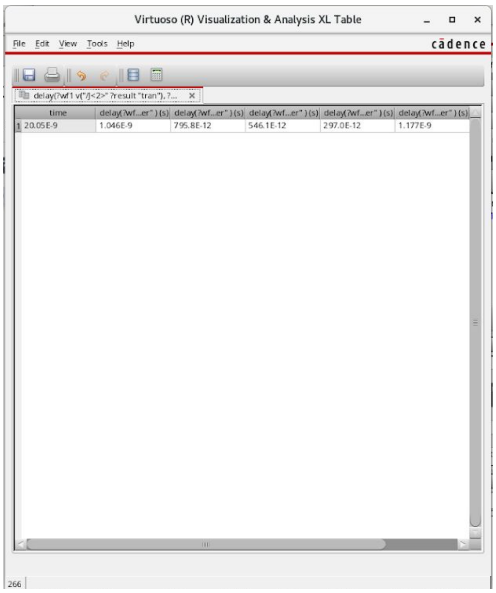

Fig. 12 Delay of O<3:0> and CARRY

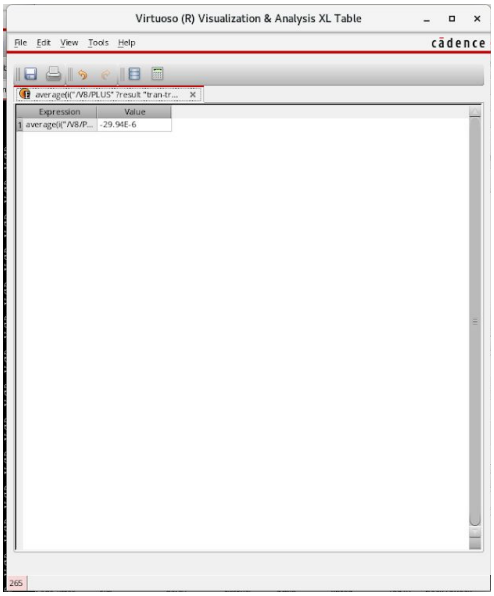

Fig. 13 Power from VDD

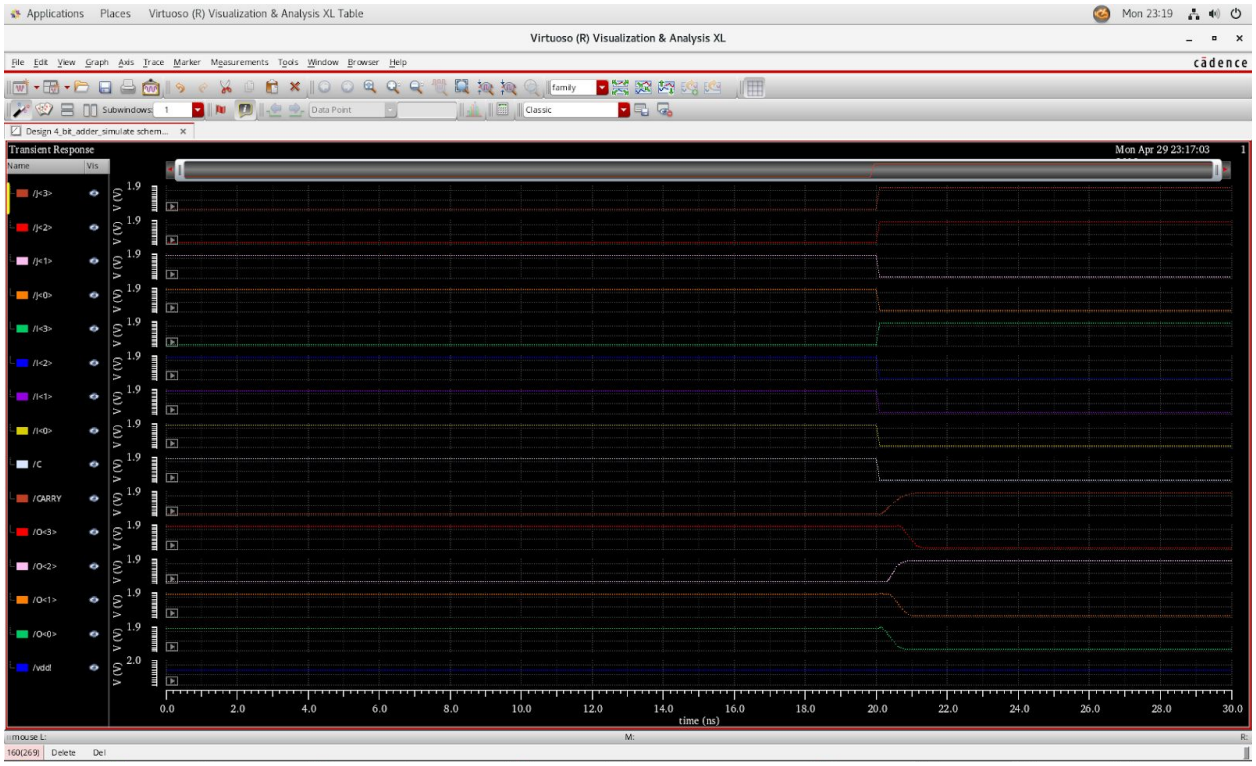

Fig. 14 1100 + 1000 Carry in 0

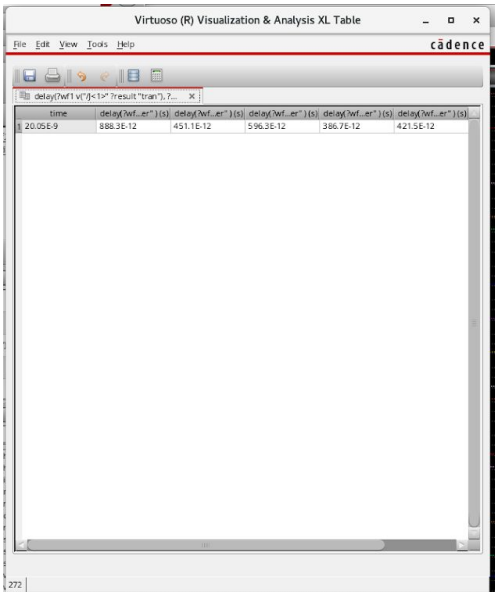

Fig. 15 Delay of O<3:0> and CARRY

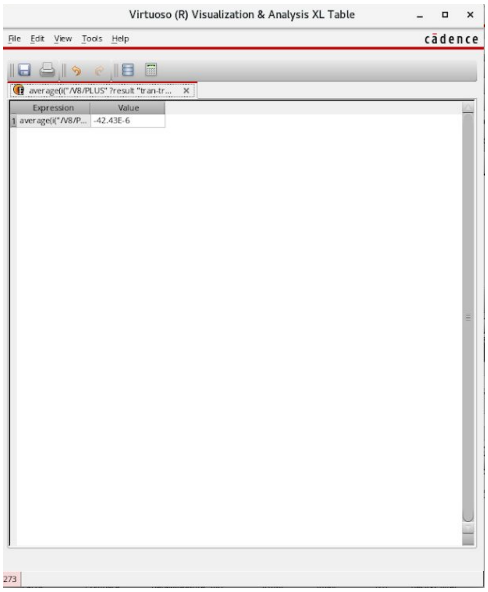

Fig.16 Power from VDD