ECEN 714 Lab 9
Chenjie Luo

1. **Report_constraint**

Information: Updating graph... (UID-83)
Information: Updating design information... (UID-85)

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Report : constraint
        -all_violators
        -verbose
Design : chenjie_module
Version: D-2010.03-SP2
Date   : Thu Apr 10 23:38:07 2019
****************************************
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This design has no violated constraints.

2. Report_areas

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****************************************
Report : area
Design : chenjie_module
Version: D-2010.03-SP2
Date   : Thu Apr 10 23:38:49 2019
****************************************

Library(s) Used:

    iit018_stdcells (File: /home/grads/l/lchenjie/lchenjie/tutorial/syn/iit018_stdcells.db)

Number of ports:              26
Number of nets:              414
Number of cells:             391
Number of references:         20

Combinational area:       11279.000000
Noncombinational area:     2400.000000
Net Interconnect area:      undefined  (No wire load specified)

Total cell area:          13679.000000
Total area:                undefined
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3. chenjie_module_netlist.v

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module chenjie_module_DW01_inc_0 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;

  wire   [7:2] carry;

  HAX1 U1_1_6 ( .A(A[6]), .B(carry[6]), .YC(carry[7]), .YS(SUM[6]) );
  HAX1 U1_1_5 ( .A(A[5]), .B(carry[5]), .YC(carry[6]), .YS(SUM[5]) );
  HAX1 U1_1_4 ( .A(A[4]), .B(carry[4]), .YC(carry[5]), .YS(SUM[4]) );
  HAX1 U1_1_3 ( .A(A[3]), .B(carry[3]), .YC(carry[4]), .YS(SUM[3]) );
  HAX1 U1_1_2 ( .A(A[2]), .B(carry[2]), .YC(carry[3]), .YS(SUM[2]) );
  HAX1 U1_1_1 ( .A(A[1]), .B(A[0]), .YC(carry[2]), .YS(SUM[1]) );
  INVX2 U1 ( .A(A[0]), .Y(SUM[0]) );
  XOR2X1 U2 ( .A(carry[7]), .B(A[7]), .Y(SUM[7]) );
endmodule


module chenjie_module_DW01_inc_1 ( A, SUM );
  input [7:0] A;
  output [7:0] SUM;

  wire   [7:2] carry;

  HAX1 U1_1_6 ( .A(A[6]), .B(carry[6]), .YC(carry[7]), .YS(SUM[6]) );
  HAX1 U1_1_5 ( .A(A[5]), .B(carry[5]), .YC(carry[6]), .YS(SUM[5]) );
  HAX1 U1_1_4 ( .A(A[4]), .B(carry[4]), .YC(carry[5]), .YS(SUM[4]) );
  HAX1 U1_1_3 ( .A(A[3]), .B(carry[3]), .YC(carry[4]), .YS(SUM[3]) );
  HAX1 U1_1_2 ( .A(A[2]), .B(carry[2]), .YC(carry[3]), .YS(SUM[2]) );
  HAX1 U1_1_1 ( .A(A[1]), .B(A[0]), .YC(carry[2]), .YS(SUM[1]) );
  INVX2 U1 ( .A(A[0]), .Y(SUM[0]) );
  XOR2X1 U2 ( .A(carry[7]), .B(A[7]), .Y(SUM[7]) );
endmodule


module chenjie_module ( clk, reset, throttle, set, accel, coast, cancel,
       resume, brake, speed, cruise_speed, cruise_on );
  output [7:0] speed;
  output [7:0] cruise_speed;
  input clk, reset, throttle, set, accel, coast, cancel, resume, brake;
  output cruise_on;
  wire   n471, n472, n473, n474, n475, n476, n477, n478, n479, n480, n481,
        n482, n483, n484, n485, n486, n487, N36, N37, N38, N39, N40, N41, N42,
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    N43, N46, N47, N48, N49, N50, N51, N52, N53, N63, N64, N65, N66, N67,
    N68, N69, N70, N71, N74, N75, N76, N77, N78, N79, N80, N81, N129,
    N130, N131, N132, N133, N134, N135, N147, N149, N151, N173, N174,
    N175, N176, N177, N178, N179, N196, N197, N198, N199, N200, N201,
    N202, N203, N205, N210, N212, N213, N214, N215, N216, N217, N234,
    N239, N241, N243, N245, N247, N249, N251, N253, N255, N257, N259,
    N261, N263, N265, N267, N269, n178, n179, n180, n181, n182, n183,
    n184, n185, n186, n187, n188, n189, n190, n191, n192, n193, n194,
    \gt_52/B[0] , \gt_52/B[2] , \gt_52/B[3] , \gt_52/B[4] , \gt_52/B[5] ,
    \gt_52/B[6] , \gt_52/B[7] , \sub_73/carry[7] , \sub_73/carry[6] ,
    \sub_73/carry[5] , \sub_73/carry[4] , \sub_73/carry[3] , n203, n204,
    n205, n211, n216, n218, n220, n222, n224, n226, n228, n231, n232,
    n233, n234, n235, n236, n237, n238, n239, n240, n241, n242, n243,
    n244, n245, n246, n247, n248, n249, n250, n251, n252, n253, n254,
    n255, n256, n257, n258, n259, n260, n261, n262, n263, n264, n265,
    n266, n267, n268, n269, n270, n271, n272, n273, n274, n275, n276,
    n277, n278, n279, n280, n281, n282, n283, n284, n285, n286, n287,
    n288, n289, n290, n291, n292, n293, n294, n295, n296, n297, n298,
    n299, n300, n301, n302, n303, n304, n305, n306, n307, n308, n309,
    n310, n311, n312, n313, n314, n315, n316, n317, n318, n319, n320,
    n321, n322, n323, n324, n325, n326, n327, n328, n329, n330, n331,
    n332, n333, n334, n335, n336, n337, n338, n339, n340, n341, n342,
    n343, n344, n345, n346, n347, n348, n349, n350, n351, n352, n353,
    n354, n355, n356, n357, n358, n359, n360, n361, n362, n363, n364,
    n365, n366, n367, n368, n369, n370, n371, n372, n373, n374, n375,
    n376, n377, n378, n379, n380, n381, n382, n383, n384, n385, n386,
    n387, n388, n389, n390, n391, n392, n393, n394, n395, n396, n397,
    n398, n399, n400, n401, n402, n403, n404, n405, n406, n407, n408,
    n409, n410, n411, n412, n413, n414, n415, n416, n417, n418, n419,
    n420, n421, n422, n423, n424, n425, n426, n427, n428, n429, n430,
    n431, n432, n433, n434, n435, n436, n437, n438, n439, n440, n441,
    n442, n443, n444, n445, n446, n447, n448, n449, n450, n451, n452,
    n453, n454, n455, n456, n457, n458, n459, n460, n461, n462, n463,
    n464, n465, n466, n467, n468, n469, n470;
wire   [7:0] cached_speed;

DFFPOSX1 \cached_speed_reg[0]  ( .D(n194), .CLK(set), .Q(cached_speed[0]) );
DFFPOSX1 cruise_on_reg ( .D(n193), .CLK(clk), .Q(n487) );
DFFPOSX1 \speed_reg[7]  ( .D(n192), .CLK(clk), .Q(n471) );
DFFPOSX1 \cruise_speed_reg[7]  ( .D(N196), .CLK(clk), .Q(n479) );
DFFPOSX1 \speed_reg[0]  ( .D(n191), .CLK(clk), .Q(n478) );
DFFPOSX1 \speed_reg[6]  ( .D(n190), .CLK(clk), .Q(n472) );
DFFPOSX1 \speed_reg[1]  ( .D(n189), .CLK(clk), .Q(n477) );
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DFFPOSX1 \speed_reg[2]  ( .D(n188), .CLK(clk), .Q(n476) );
DFFPOSX1 \speed_reg[3]  ( .D(n187), .CLK(clk), .Q(n475) );
DFFPOSX1 \speed_reg[4]  ( .D(n186), .CLK(clk), .Q(n474) );
DFFPOSX1 \speed_reg[5]  ( .D(n185), .CLK(clk), .Q(n473) );
DFFPOSX1 \cached_speed_reg[1]  ( .D(n184), .CLK(set), .Q(cached_speed[1]) );
DFFPOSX1 \cached_speed_reg[2]  ( .D(n183), .CLK(set), .Q(cached_speed[2]) );
DFFPOSX1 \cached_speed_reg[3]  ( .D(n182), .CLK(set), .Q(cached_speed[3]) );
DFFPOSX1 \cached_speed_reg[4]  ( .D(n181), .CLK(set), .Q(cached_speed[4]) );
DFFPOSX1 \cached_speed_reg[5]  ( .D(n180), .CLK(set), .Q(cached_speed[5]) );
DFFPOSX1 \cached_speed_reg[6]  ( .D(n179), .CLK(set), .Q(cached_speed[6]) );
DFFPOSX1 \cruise_speed_reg[6]  ( .D(N197), .CLK(clk), .Q(n480) );
DFFPOSX1 \cruise_speed_reg[5]  ( .D(N198), .CLK(clk), .Q(n481) );
DFFPOSX1 \cruise_speed_reg[0]  ( .D(N203), .CLK(clk), .Q(n486) );
DFFPOSX1 \cruise_speed_reg[4]  ( .D(N199), .CLK(clk), .Q(n482) );
DFFPOSX1 \cruise_speed_reg[1]  ( .D(N202), .CLK(clk), .Q(n485) );
DFFPOSX1 \cruise_speed_reg[2]  ( .D(N201), .CLK(clk), .Q(n484) );
DFFPOSX1 \cruise_speed_reg[3]  ( .D(N200), .CLK(clk), .Q(n483) );
DFFPOSX1 \cached_speed_reg[7]  ( .D(n178), .CLK(set), .Q(cached_speed[7]) );
chenjie_module_DW01_inc_0 r97 ( .A({N239, N241, N243, N245, N247, N249, N251,
    N253}), .SUM({N43, N42, N41, N40, N39, N38, N37, N36}) );
chenjie_module_DW01_inc_1 add_47 ( .A({N255, N257, N259, N261, N263, N265,
    N267, N269}), .SUM({N53, N52, N51, N50, N49, N48, N47, N46}) );
AND2X2 U243 ( .A(coast), .B(N71), .Y(n203) );
XOR2X1 U244 ( .A(N241), .B(n254), .Y(n204) );
XNOR2X1 U245 ( .A(N239), .B(n255), .Y(n205) );
INVX8 U246 ( .A(n296), .Y(speed[6]) );
INVX8 U247 ( .A(n305), .Y(speed[3]) );
INVX8 U248 ( .A(n311), .Y(speed[5]) );
INVX8 U249 ( .A(n302), .Y(speed[2]) );
INVX8 U250 ( .A(n290), .Y(speed[7]) );
INVX2 U251 ( .A(n487), .Y(n211) );
INVX8 U252 ( .A(n211), .Y(cruise_on) );
INVX8 U253 ( .A(n273), .Y(speed[0]) );
INVX8 U254 ( .A(n454), .Y(cruise_speed[0]) );
INVX8 U255 ( .A(n299), .Y(speed[1]) );
INVX2 U256 ( .A(n479), .Y(n216) );
INVX8 U257 ( .A(n216), .Y(cruise_speed[7]) );
INVX2 U258 ( .A(n480), .Y(n218) );
INVX8 U259 ( .A(n218), .Y(cruise_speed[6]) );
INVX2 U260 ( .A(n481), .Y(n220) );
INVX8 U261 ( .A(n220), .Y(cruise_speed[5]) );
INVX2 U262 ( .A(n482), .Y(n222) );
INVX8 U263 ( .A(n222), .Y(cruise_speed[4]) );
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INVX2 U264 ( .A(n485), .Y(n224) );
INVX8 U265 ( .A(n224), .Y(cruise_speed[1]) );
INVX2 U266 ( .A(n484), .Y(n226) );
INVX8 U267 ( .A(n226), .Y(cruise_speed[2]) );
INVX2 U268 ( .A(n483), .Y(n228) );
INVX8 U269 ( .A(n228), .Y(cruise_speed[3]) );
INVX8 U270 ( .A(n308), .Y(speed[4]) );
INVX2 U271 ( .A(n280), .Y(n340) );
INVX2 U272 ( .A(n203), .Y(n231) );
INVX2 U273 ( .A(reset), .Y(n332) );
OR2X2 U274 ( .A(n465), .B(n466), .Y(n368) );
XNOR2X1 U275 ( .A(N173), .B(\sub_73/carry[7] ), .Y(N217) );
OR2X1 U276 ( .A(\sub_73/carry[6] ), .B(N174), .Y(\sub_73/carry[7] ) );
XNOR2X1 U277 ( .A(N174), .B(\sub_73/carry[6] ), .Y(N216) );
OR2X1 U278 ( .A(\sub_73/carry[5] ), .B(N175), .Y(\sub_73/carry[6] ) );
XNOR2X1 U279 ( .A(N175), .B(\sub_73/carry[5] ), .Y(N215) );
OR2X1 U280 ( .A(\sub_73/carry[4] ), .B(N176), .Y(\sub_73/carry[5] ) );
XNOR2X1 U281 ( .A(N176), .B(\sub_73/carry[4] ), .Y(N214) );
OR2X1 U282 ( .A(\sub_73/carry[3] ), .B(N177), .Y(\sub_73/carry[4] ) );
XNOR2X1 U283 ( .A(N177), .B(\sub_73/carry[3] ), .Y(N213) );
OR2X1 U284 ( .A(N179), .B(N178), .Y(\sub_73/carry[3] ) );
XNOR2X1 U285 ( .A(N178), .B(N179), .Y(N212) );
NAND2X1 U286 ( .A(n323), .B(N74), .Y(n232) );
OAI21X1 U287 ( .A(N74), .B(n323), .C(n232), .Y(N75) );
NOR2X1 U288 ( .A(n232), .B(N68), .Y(n234) );
AOI21X1 U289 ( .A(n232), .B(N68), .C(n234), .Y(n233) );
NAND2X1 U290 ( .A(n234), .B(n326), .Y(n235) );
OAI21X1 U291 ( .A(n234), .B(n326), .C(n235), .Y(N77) );
NOR2X1 U292 ( .A(n235), .B(N66), .Y(n237) );
AOI21X1 U293 ( .A(n235), .B(N66), .C(n237), .Y(n236) );
NAND2X1 U294 ( .A(n237), .B(n328), .Y(n238) );
OAI21X1 U295 ( .A(n237), .B(n328), .C(n238), .Y(N79) );
XNOR2X1 U296 ( .A(N64), .B(n238), .Y(N80) );
NOR2X1 U297 ( .A(N64), .B(n238), .Y(n239) );
XOR2X1 U298 ( .A(N63), .B(n239), .Y(N81) );
INVX2 U299 ( .A(N70), .Y(N74) );
INVX2 U300 ( .A(n233), .Y(N76) );
INVX2 U301 ( .A(n236), .Y(N78) );
NAND2X1 U302 ( .A(n322), .B(n429), .Y(n240) );
OAI21X1 U303 ( .A(n429), .B(n322), .C(n240), .Y(N129) );
NOR2X1 U304 ( .A(n240), .B(\gt_52/B[2] ), .Y(n242) );
AOI21X1 U305 ( .A(n240), .B(\gt_52/B[2] ), .C(n242), .Y(n241) );
NAND2X1 U306 ( .A(n242), .B(n417), .Y(n243) );
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OAI21X1 U307 ( .A(n242), .B(n417), .C(n243), .Y(N131) );
NOR2X1 U308 ( .A(n243), .B(\gt_52/B[4] ), .Y(n245) );
AOI21X1 U309 ( .A(n243), .B(\gt_52/B[4] ), .C(n245), .Y(n244) );
NAND2X1 U310 ( .A(n245), .B(n407), .Y(n246) );
OAI21X1 U311 ( .A(n245), .B(n407), .C(n246), .Y(N133) );
XNOR2X1 U312 ( .A(\gt_52/B[6] ), .B(n246), .Y(N134) );
NOR2X1 U313 ( .A(\gt_52/B[6] ), .B(n246), .Y(n247) );
XOR2X1 U314 ( .A(\gt_52/B[7] ), .B(n247), .Y(N135) );
INVX2 U315 ( .A(n244), .Y(N132) );
INVX2 U316 ( .A(n241), .Y(N130) );
NAND2X1 U317 ( .A(n256), .B(n257), .Y(n248) );
OAI21X1 U318 ( .A(n257), .B(n256), .C(n248), .Y(N147) );
NOR2X1 U319 ( .A(n248), .B(N249), .Y(n250) );
AOI21X1 U320 ( .A(n248), .B(N249), .C(n250), .Y(n249) );
NAND2X1 U321 ( .A(n250), .B(n333), .Y(n251) );
OAI21X1 U322 ( .A(n250), .B(n333), .C(n251), .Y(N149) );
NOR2X1 U323 ( .A(n251), .B(N245), .Y(n253) );
AOI21X1 U324 ( .A(n251), .B(N245), .C(n253), .Y(n252) );
NAND2X1 U325 ( .A(n253), .B(n334), .Y(n254) );
OAI21X1 U326 ( .A(n253), .B(n334), .C(n254), .Y(N151) );
NOR2X1 U327 ( .A(N241), .B(n254), .Y(n255) );
INVX2 U328 ( .A(N251), .Y(n256) );
INVX2 U329 ( .A(N253), .Y(n257) );
NOR2X1 U330 ( .A(N63), .B(N64), .Y(n260) );
NAND3X1 U331 ( .A(N67), .B(N68), .C(N69), .Y(n258) );
OAI21X1 U332 ( .A(n261), .B(N66), .C(N65), .Y(n259) );
NAND2X1 U333 ( .A(n260), .B(n259), .Y(N71) );
INVX2 U334 ( .A(n258), .Y(n261) );
OAI21X1 U335 ( .A(N203), .B(N202), .C(N201), .Y(n262) );
OAI21X1 U336 ( .A(n265), .B(n262), .C(n266), .Y(n263) );
AOI21X1 U337 ( .A(N198), .B(n263), .C(N196), .Y(n264) );
NAND2X1 U338 ( .A(n264), .B(n267), .Y(N205) );
INVX2 U339 ( .A(N200), .Y(n265) );
INVX2 U340 ( .A(N199), .Y(n266) );
INVX2 U341 ( .A(N197), .Y(n267) );
NOR2X1 U342 ( .A(speed[7]), .B(n472), .Y(n270) );
NAND3X1 U343 ( .A(speed[3]), .B(speed[2]), .C(n477), .Y(n268) );
OAI21X1 U344 ( .A(n271), .B(speed[4]), .C(speed[5]), .Y(n269) );
NAND2X1 U345 ( .A(n270), .B(n269), .Y(N234) );
INVX2 U346 ( .A(n268), .Y(n271) );
MUX2X1 U347 ( .B(n272), .A(n273), .S(N234), .Y(n194) );
INVX1 U348 ( .A(cached_speed[0]), .Y(n272) );
INVX1 U349 ( .A(n274), .Y(n193) );
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OAI21X1 U350 ( .A(n275), .B(n276), .C(n277), .Y(n274) );
OAI21X1 U351 ( .A(n278), .B(n279), .C(n280), .Y(n276) );
OAI21X1 U352 ( .A(n281), .B(n282), .C(N205), .Y(n279) );
NAND3X1 U353 ( .A(n283), .B(n284), .C(n285), .Y(n282) );
NOR2X1 U354 ( .A(N176), .B(N175), .Y(n285) );
NAND3X1 U355 ( .A(n286), .B(n287), .C(n288), .Y(n281) );
NOR2X1 U356 ( .A(N178), .B(N177), .Y(n288) );
INVX1 U357 ( .A(resume), .Y(n278) );
NOR2X1 U358 ( .A(cancel), .B(n289), .Y(n275) );
OAI21X1 U359 ( .A(n290), .B(n291), .C(n292), .Y(n192) );
MUX2X1 U360 ( .B(n293), .A(N217), .S(brake), .Y(n292) );
OAI21X1 U361 ( .A(n273), .B(n291), .C(n294), .Y(n191) );
MUX2X1 U362 ( .B(n295), .A(N210), .S(brake), .Y(n294) );
OAI21X1 U363 ( .A(n296), .B(n291), .C(n297), .Y(n190) );
MUX2X1 U364 ( .B(n298), .A(N216), .S(brake), .Y(n297) );
OAI21X1 U365 ( .A(n299), .B(n291), .C(n300), .Y(n189) );
MUX2X1 U366 ( .B(n301), .A(n286), .S(brake), .Y(n300) );
OAI21X1 U367 ( .A(n302), .B(n291), .C(n303), .Y(n188) );
MUX2X1 U368 ( .B(n304), .A(N212), .S(brake), .Y(n303) );
OAI21X1 U369 ( .A(n305), .B(n291), .C(n306), .Y(n187) );
MUX2X1 U370 ( .B(n307), .A(N213), .S(brake), .Y(n306) );
OAI21X1 U371 ( .A(n308), .B(n291), .C(n309), .Y(n186) );
MUX2X1 U372 ( .B(n310), .A(N214), .S(brake), .Y(n309) );
OAI21X1 U373 ( .A(n311), .B(n291), .C(n312), .Y(n185) );
MUX2X1 U374 ( .B(n313), .A(N215), .S(brake), .Y(n312) );
NAND2X1 U375 ( .A(n314), .B(n277), .Y(n291) );
MUX2X1 U376 ( .B(n315), .A(n299), .S(N234), .Y(n184) );
INVX1 U377 ( .A(cached_speed[1]), .Y(n315) );
MUX2X1 U378 ( .B(n316), .A(n302), .S(N234), .Y(n183) );
INVX1 U379 ( .A(cached_speed[2]), .Y(n316) );
MUX2X1 U380 ( .B(n317), .A(n305), .S(N234), .Y(n182) );
INVX1 U381 ( .A(cached_speed[3]), .Y(n317) );
MUX2X1 U382 ( .B(n318), .A(n308), .S(N234), .Y(n181) );
INVX1 U383 ( .A(n474), .Y(n308) );
INVX1 U384 ( .A(cached_speed[4]), .Y(n318) );
MUX2X1 U385 ( .B(n319), .A(n311), .S(N234), .Y(n180) );
INVX1 U386 ( .A(n473), .Y(n311) );
INVX1 U387 ( .A(cached_speed[5]), .Y(n319) );
MUX2X1 U388 ( .B(n320), .A(n296), .S(N234), .Y(n179) );
INVX1 U389 ( .A(cached_speed[6]), .Y(n320) );
MUX2X1 U390 ( .B(n321), .A(n290), .S(N234), .Y(n178) );
INVX1 U391 ( .A(n471), .Y(n290) );
INVX1 U392 ( .A(cached_speed[7]), .Y(n321) );
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INVX1 U393 ( .A(n323), .Y(N69) );
AOI22X1 U394 ( .A(accel), .B(N47), .C(n324), .D(cruise_speed[1]), .Y(n323)
      );
INVX1 U395 ( .A(n325), .Y(N68) );
AOI22X1 U396 ( .A(accel), .B(N48), .C(n324), .D(cruise_speed[2]), .Y(n325)
      );
INVX1 U397 ( .A(n326), .Y(N67) );
AOI22X1 U398 ( .A(accel), .B(N49), .C(n324), .D(cruise_speed[3]), .Y(n326)
      );
INVX1 U399 ( .A(n327), .Y(N66) );
AOI22X1 U400 ( .A(accel), .B(N50), .C(n324), .D(cruise_speed[4]), .Y(n327)
      );
INVX1 U401 ( .A(n328), .Y(N65) );
AOI22X1 U402 ( .A(accel), .B(N51), .C(n324), .D(cruise_speed[5]), .Y(n328)
      );
INVX1 U403 ( .A(n329), .Y(N64) );
AOI22X1 U404 ( .A(accel), .B(N52), .C(n324), .D(cruise_speed[6]), .Y(n329)
      );
INVX1 U405 ( .A(n330), .Y(N63) );
AOI22X1 U406 ( .A(accel), .B(N53), .C(n324), .D(cruise_speed[7]), .Y(n330)
      );
INVX1 U407 ( .A(n331), .Y(n324) );
AND2X1 U408 ( .A(n332), .B(cruise_speed[1]), .Y(N267) );
AND2X1 U409 ( .A(n332), .B(cruise_speed[2]), .Y(N265) );
AND2X1 U410 ( .A(n332), .B(cruise_speed[3]), .Y(N263) );
AND2X1 U411 ( .A(n332), .B(cruise_speed[4]), .Y(N261) );
AND2X1 U412 ( .A(n332), .B(cruise_speed[5]), .Y(N259) );
AND2X1 U413 ( .A(n332), .B(cruise_speed[6]), .Y(N257) );
AND2X1 U414 ( .A(n332), .B(cruise_speed[7]), .Y(N255) );
INVX1 U415 ( .A(n333), .Y(N247) );
INVX1 U416 ( .A(n334), .Y(N243) );
NAND2X1 U417 ( .A(n335), .B(n336), .Y(N203) );
AOI22X1 U418 ( .A(N74), .B(n337), .C(n338), .D(N46), .Y(n336) );
AOI22X1 U419 ( .A(n339), .B(cruise_speed[0]), .C(n340), .D(cached_speed[0]),
    .Y(n335) );
NAND2X1 U420 ( .A(n341), .B(n342), .Y(N202) );
AOI22X1 U421 ( .A(n337), .B(N75), .C(n338), .D(N47), .Y(n342) );
AOI22X1 U422 ( .A(n339), .B(cruise_speed[1]), .C(n340), .D(cached_speed[1]),
    .Y(n341) );
NAND2X1 U423 ( .A(n343), .B(n344), .Y(N201) );
AOI22X1 U424 ( .A(n337), .B(N76), .C(n338), .D(N48), .Y(n344) );
AOI22X1 U425 ( .A(n339), .B(cruise_speed[2]), .C(n340), .D(cached_speed[2]),
    .Y(n343) );
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NAND2X1 U426 ( .A(n345), .B(n346), .Y(N200) );
AOI22X1 U427 ( .A(n337), .B(N77), .C(n338), .D(N49), .Y(n346) );
AOI22X1 U428 ( .A(n339), .B(cruise_speed[3]), .C(n340), .D(cached_speed[3]),
    .Y(n345) );
NAND2X1 U429 ( .A(n347), .B(n348), .Y(N199) );
AOI22X1 U430 ( .A(n337), .B(N78), .C(n338), .D(N50), .Y(n348) );
AOI22X1 U431 ( .A(n339), .B(cruise_speed[4]), .C(n340), .D(cached_speed[4]),
    .Y(n347) );
NAND2X1 U432 ( .A(n349), .B(n350), .Y(N198) );
AOI22X1 U433 ( .A(n337), .B(N79), .C(n338), .D(N51), .Y(n350) );
AOI22X1 U434 ( .A(n339), .B(cruise_speed[5]), .C(n340), .D(cached_speed[5]),
    .Y(n349) );
NAND2X1 U435 ( .A(n351), .B(n352), .Y(N197) );
AOI22X1 U436 ( .A(n337), .B(N80), .C(n338), .D(N52), .Y(n352) );
AOI22X1 U437 ( .A(n339), .B(cruise_speed[6]), .C(n340), .D(cached_speed[6]),
    .Y(n351) );
NAND2X1 U438 ( .A(n353), .B(n354), .Y(N196) );
AOI22X1 U439 ( .A(n337), .B(N81), .C(n338), .D(N53), .Y(n354) );
INVX1 U440 ( .A(n355), .Y(n338) );
NAND3X1 U441 ( .A(n356), .B(n280), .C(n357), .Y(n355) );
INVX1 U442 ( .A(n358), .Y(n337) );
NAND3X1 U443 ( .A(n203), .B(n280), .C(n357), .Y(n358) );
AOI22X1 U444 ( .A(n339), .B(cruise_speed[7]), .C(n340), .D(cached_speed[7]),
    .Y(n353) );
INVX1 U445 ( .A(n359), .Y(n339) );
OAI21X1 U446 ( .A(n360), .B(n361), .C(n362), .Y(n359) );
NOR2X1 U447 ( .A(reset), .B(n340), .Y(n362) );
OAI21X1 U448 ( .A(n363), .B(n364), .C(set), .Y(n280) );
NAND2X1 U449 ( .A(n283), .B(n284), .Y(n364) );
AOI21X1 U450 ( .A(n365), .B(n366), .C(n367), .Y(n363) );
NAND3X1 U451 ( .A(N178), .B(N179), .C(N177), .Y(n365) );
INVX1 U452 ( .A(n357), .Y(n361) );
INVX1 U453 ( .A(n287), .Y(N210) );
AOI21X1 U454 ( .A(n478), .B(n314), .C(n295), .Y(n287) );
OAI21X1 U455 ( .A(N253), .B(n368), .C(n369), .Y(n295) );
AOI22X1 U456 ( .A(N36), .B(n370), .C(n429), .D(n371), .Y(n369) );
INVX1 U457 ( .A(n286), .Y(N179) );
AOI21X1 U458 ( .A(n477), .B(n314), .C(n301), .Y(n286) );
OAI21X1 U459 ( .A(n368), .B(n372), .C(n373), .Y(n301) );
AOI22X1 U460 ( .A(N37), .B(n370), .C(N129), .D(n371), .Y(n373) );
INVX1 U461 ( .A(N147), .Y(n372) );
OAI21X1 U462 ( .A(n302), .B(n374), .C(n375), .Y(N178) );
INVX1 U463 ( .A(n304), .Y(n375) );
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OAI21X1 U464 ( .A(n368), .B(n249), .C(n376), .Y(n304) );
AOI22X1 U465 ( .A(N38), .B(n370), .C(N130), .D(n371), .Y(n376) );
INVX1 U466 ( .A(n476), .Y(n302) );
OAI21X1 U467 ( .A(n305), .B(n374), .C(n377), .Y(N177) );
INVX1 U468 ( .A(n307), .Y(n377) );
OAI21X1 U469 ( .A(n368), .B(n378), .C(n379), .Y(n307) );
AOI22X1 U470 ( .A(N39), .B(n370), .C(N131), .D(n371), .Y(n379) );
INVX1 U471 ( .A(N149), .Y(n378) );
INVX1 U472 ( .A(n314), .Y(n374) );
INVX1 U473 ( .A(n475), .Y(n305) );
INVX1 U474 ( .A(n366), .Y(N176) );
AOI21X1 U475 ( .A(speed[4]), .B(n314), .C(n310), .Y(n366) );
OAI21X1 U476 ( .A(n368), .B(n252), .C(n380), .Y(n310) );
AOI22X1 U477 ( .A(N40), .B(n370), .C(N132), .D(n371), .Y(n380) );
INVX1 U478 ( .A(n367), .Y(N175) );
AOI21X1 U479 ( .A(speed[5]), .B(n314), .C(n313), .Y(n367) );
OAI21X1 U480 ( .A(n368), .B(n381), .C(n382), .Y(n313) );
AOI22X1 U481 ( .A(N41), .B(n370), .C(N133), .D(n371), .Y(n382) );
INVX1 U482 ( .A(N151), .Y(n381) );
INVX1 U483 ( .A(n284), .Y(N174) );
AOI21X1 U484 ( .A(n472), .B(n314), .C(n298), .Y(n284) );
OAI21X1 U485 ( .A(n368), .B(n204), .C(n383), .Y(n298) );
AOI22X1 U486 ( .A(N42), .B(n370), .C(N134), .D(n371), .Y(n383) );
INVX1 U487 ( .A(n283), .Y(N173) );
AOI21X1 U488 ( .A(speed[7]), .B(n314), .C(n293), .Y(n283) );
OAI21X1 U489 ( .A(n368), .B(n205), .C(n384), .Y(n293) );
AOI22X1 U490 ( .A(N43), .B(n370), .C(N135), .D(n371), .Y(n384) );
INVX1 U491 ( .A(n385), .Y(n371) );
OAI21X1 U492 ( .A(n289), .B(n386), .C(n387), .Y(n370) );
NAND2X1 U493 ( .A(n388), .B(n389), .Y(n386) );
INVX1 U494 ( .A(n390), .Y(n388) );
NOR2X1 U495 ( .A(n391), .B(n392), .Y(n314) );
OAI21X1 U496 ( .A(n393), .B(n289), .C(n385), .Y(n392) );
NAND2X1 U497 ( .A(n357), .B(n390), .Y(n385) );
OAI21X1 U498 ( .A(n394), .B(n395), .C(n396), .Y(n390) );
OAI21X1 U499 ( .A(\gt_52/B[7] ), .B(n397), .C(n398), .Y(n396) );
OAI21X1 U500 ( .A(n399), .B(n400), .C(n401), .Y(n398) );
OAI21X1 U501 ( .A(\gt_52/B[6] ), .B(n402), .C(n403), .Y(n401) );
AOI22X1 U502 ( .A(n404), .B(n405), .C(n406), .D(n407), .Y(n403) );
INVX1 U503 ( .A(n408), .Y(n406) );
NAND2X1 U504 ( .A(\gt_52/B[5] ), .B(n408), .Y(n404) );
OAI21X1 U505 ( .A(n409), .B(n410), .C(n411), .Y(n408) );
OAI21X1 U506 ( .A(\gt_52/B[4] ), .B(n412), .C(n413), .Y(n411) );
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AOI22X1 U507 ( .A(n414), .B(n415), .C(n416), .D(n417), .Y(n413) );
INVX1 U508 ( .A(n418), .Y(n416) );
NAND2X1 U509 ( .A(\gt_52/B[3] ), .B(n418), .Y(n414) );
OAI21X1 U510 ( .A(n419), .B(n420), .C(n421), .Y(n418) );
OAI21X1 U511 ( .A(\gt_52/B[2] ), .B(n422), .C(n423), .Y(n421) );
AOI22X1 U512 ( .A(n424), .B(n322), .C(n425), .D(n426), .Y(n423) );
NAND2X1 U513 ( .A(n427), .B(\gt_52/B[0] ), .Y(n425) );
AOI22X1 U514 ( .A(n389), .B(N37), .C(n477), .D(n393), .Y(n322) );
NAND3X1 U515 ( .A(n428), .B(\gt_52/B[0] ), .C(n427), .Y(n424) );
INVX1 U516 ( .A(n429), .Y(\gt_52/B[0] ) );
AOI22X1 U517 ( .A(n389), .B(N36), .C(n478), .D(n393), .Y(n429) );
INVX1 U518 ( .A(n419), .Y(\gt_52/B[2] ) );
AOI22X1 U519 ( .A(speed[2]), .B(n393), .C(n389), .D(N38), .Y(n419) );
INVX1 U520 ( .A(n417), .Y(\gt_52/B[3] ) );
AOI22X1 U521 ( .A(speed[3]), .B(n393), .C(n389), .D(N39), .Y(n417) );
INVX1 U522 ( .A(n409), .Y(\gt_52/B[4] ) );
AOI22X1 U523 ( .A(speed[4]), .B(n393), .C(n389), .D(N40), .Y(n409) );
INVX1 U524 ( .A(n407), .Y(\gt_52/B[5] ) );
AOI22X1 U525 ( .A(speed[5]), .B(n393), .C(n389), .D(N41), .Y(n407) );
INVX1 U526 ( .A(n399), .Y(\gt_52/B[6] ) );
AOI22X1 U527 ( .A(n472), .B(n393), .C(n389), .D(N42), .Y(n399) );
INVX1 U528 ( .A(n394), .Y(\gt_52/B[7] ) );
AOI22X1 U529 ( .A(speed[7]), .B(n393), .C(n389), .D(N43), .Y(n394) );
NOR2X1 U530 ( .A(n289), .B(throttle), .Y(n357) );
NOR2X1 U531 ( .A(n389), .B(reset), .Y(n393) );
OAI21X1 U532 ( .A(N239), .B(n397), .C(n430), .Y(n389) );
OAI21X1 U533 ( .A(n395), .B(n431), .C(n432), .Y(n430) );
OAI21X1 U534 ( .A(N241), .B(n402), .C(n433), .Y(n432) );
INVX1 U535 ( .A(n434), .Y(n433) );
AOI21X1 U536 ( .A(n402), .B(N241), .C(n435), .Y(n434) );
OAI22X1 U537 ( .A(n334), .B(n436), .C(n405), .D(n437), .Y(n435) );
AND2X1 U538 ( .A(n405), .B(n437), .Y(n436) );
OAI22X1 U539 ( .A(n438), .B(n439), .C(N245), .D(n412), .Y(n437) );
INVX1 U540 ( .A(n410), .Y(n412) );
INVX1 U541 ( .A(n440), .Y(N245) );
OAI21X1 U542 ( .A(n441), .B(n415), .C(n442), .Y(n439) );
INVX1 U543 ( .A(n443), .Y(n442) );
AOI21X1 U544 ( .A(n441), .B(n415), .C(n333), .Y(n443) );
OAI21X1 U545 ( .A(n231), .B(n444), .C(n445), .Y(n415) );
AOI22X1 U546 ( .A(N49), .B(n356), .C(cruise_speed[3]), .D(n360), .Y(n445) );
INVX1 U547 ( .A(N77), .Y(n444) );
OAI21X1 U548 ( .A(N249), .B(n422), .C(n446), .Y(n441) );
OAI21X1 U549 ( .A(n420), .B(n447), .C(n448), .Y(n446) );
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AOI21X1 U550 ( .A(N251), .B(n428), .C(n449), .Y(n448) );
INVX1 U551 ( .A(n450), .Y(n449) );
OAI22X1 U552 ( .A(N251), .B(n428), .C(N253), .D(n427), .Y(n450) );
INVX1 U553 ( .A(n451), .Y(n427) );
OAI21X1 U554 ( .A(N70), .B(n231), .C(n452), .Y(n451) );
AOI22X1 U555 ( .A(N46), .B(n356), .C(n486), .D(n360), .Y(n452) );
OAI22X1 U556 ( .A(N269), .B(n453), .C(n331), .D(n454), .Y(N70) );
NOR2X1 U557 ( .A(n454), .B(reset), .Y(N269) );
INVX1 U558 ( .A(n486), .Y(n454) );
INVX1 U559 ( .A(n426), .Y(n428) );
OAI21X1 U560 ( .A(n231), .B(n455), .C(n456), .Y(n426) );
AOI22X1 U561 ( .A(N47), .B(n356), .C(cruise_speed[1]), .D(n360), .Y(n456) );
INVX1 U562 ( .A(N75), .Y(n455) );
INVX1 U563 ( .A(n420), .Y(n422) );
OAI21X1 U564 ( .A(n231), .B(n233), .C(n457), .Y(n420) );
AOI22X1 U565 ( .A(N48), .B(n356), .C(cruise_speed[2]), .D(n360), .Y(n457) );
INVX1 U566 ( .A(n447), .Y(N249) );
NOR2X1 U567 ( .A(n410), .B(n440), .Y(n438) );
OAI21X1 U568 ( .A(n231), .B(n236), .C(n458), .Y(n410) );
AOI22X1 U569 ( .A(N50), .B(n356), .C(cruise_speed[4]), .D(n360), .Y(n458) );
OAI21X1 U570 ( .A(n231), .B(n459), .C(n460), .Y(n405) );
AOI22X1 U571 ( .A(N51), .B(n356), .C(cruise_speed[5]), .D(n360), .Y(n460) );
INVX1 U572 ( .A(N79), .Y(n459) );
INVX1 U573 ( .A(n400), .Y(n402) );
OAI21X1 U574 ( .A(n231), .B(n461), .C(n462), .Y(n400) );
AOI22X1 U575 ( .A(N52), .B(n356), .C(cruise_speed[6]), .D(n360), .Y(n462) );
INVX1 U576 ( .A(N80), .Y(n461) );
INVX1 U577 ( .A(n395), .Y(n397) );
OAI21X1 U578 ( .A(n231), .B(n463), .C(n464), .Y(n395) );
AOI22X1 U579 ( .A(N53), .B(n356), .C(cruise_speed[7]), .D(n360), .Y(n464) );
NOR2X1 U580 ( .A(n331), .B(n203), .Y(n360) );
NAND2X1 U581 ( .A(n332), .B(n453), .Y(n331) );
NOR2X1 U582 ( .A(n453), .B(n203), .Y(n356) );
INVX1 U583 ( .A(accel), .Y(n453) );
INVX1 U584 ( .A(N81), .Y(n463) );
NAND3X1 U585 ( .A(n332), .B(n387), .C(n368), .Y(n391) );
OAI21X1 U586 ( .A(n467), .B(n468), .C(n289), .Y(n466) );
NAND2X1 U587 ( .A(cruise_on), .B(n332), .Y(n289) );
NAND3X1 U588 ( .A(n334), .B(n440), .C(n469), .Y(n468) );
NOR2X1 U589 ( .A(N241), .B(N239), .Y(n469) );
INVX1 U590 ( .A(n431), .Y(N239) );
NAND2X1 U591 ( .A(n471), .B(n332), .Y(n431) );
NOR2X1 U592 ( .A(n296), .B(reset), .Y(N241) );
```

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  INVX1 U593 ( .A(n472), .Y(n296) );
  NAND2X1 U594 ( .A(n474), .B(n332), .Y(n440) );
  NAND2X1 U595 ( .A(n473), .B(n332), .Y(n334) );
  NAND3X1 U596 ( .A(n333), .B(n447), .C(n470), .Y(n467) );
  NOR2X1 U597 ( .A(N253), .B(N251), .Y(n470) );
  NOR2X1 U598 ( .A(n299), .B(reset), .Y(N251) );
  INVX1 U599 ( .A(n477), .Y(n299) );
  NOR2X1 U600 ( .A(n273), .B(reset), .Y(N253) );
  INVX1 U601 ( .A(n478), .Y(n273) );
  NAND2X1 U602 ( .A(n476), .B(n332), .Y(n447) );
  NAND2X1 U603 ( .A(n475), .B(n332), .Y(n333) );
  NAND2X1 U604 ( .A(n277), .B(n387), .Y(n465) );
  INVX1 U605 ( .A(brake), .Y(n277) );
  INVX1 U606 ( .A(throttle), .Y(n387) );
endmodule
```

The number of DFFSR is 0 in my netlist.

4. **max_paths.txt**

```
****************************************
Report : timing
         -path_type full
         -delay_type max
         -slack_lesser_than 3.00
         -max_paths 3
         -sort_by slack
Design : chenjie_module
Version: L-2016.06-SP1
Date   : Thu Apr 11 21:42:44 2019
****************************************


  Startpoint: brake (input port clocked by clk)
  Endpoint: cruise_design_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: max

  Point                              Incr       Path
  -----------------------------------------------------------
  clock clk (rise edge)                 0.00       0.00
  clock network delay (ideal)           0.00       0.00
  input external delay                  4.00       4.00 f
```

```
brake (in)                                0.10       4.10 f
U475/Y (NOR2X1)                           0.08       4.18 r
U474/Y (OAI21X1)                          0.08       4.26 f
U449/Y (INVX1)                            0.06       4.32 r
U448/Y (AOI21X1)                          0.06       4.38 f
U447/Y (NAND3X1)                          0.39       4.77 r
U416/Y (MUX2X1)                           0.19       4.96 f
U415/Y (INVX1)                            0.18       5.14 r
U241/Y (OR2X1)                            0.17       5.31 r
U239/Y (OR2X1)                            0.16       5.47 r
U238/Y (OR2X1)                            0.16       5.63 r
U236/Y (OR2X1)                            0.16       5.79 r
U204/Y (XOR2X1)                           0.13       5.92 r
U389/Y (OAI21X1)                          0.07       5.99 f
U388/Y (INVX1)                            0.12       6.10 r
U387/Y (OAI21X1)                          0.06       6.17 f
U386/Y (OAI21X1)                          0.58       6.75 r
U382/Y (NAND2X1)                          0.38       7.13 f
U381/Y (NOR2X1)                           0.37       7.50 r
U298/Y (MUX2X1)                           0.19       7.69 f
U297/Y (OAI21X1)                          0.10       7.79 r
U283/Y (NAND3X1)                          0.06       7.85 f
U286/Y (INVX2)                            0.05       7.90 r
U284/Y (OAI21X1)                          0.06       7.96 f
U285/Y (NAND2X1)                          0.06       8.02 r
U312/Y (OAI21X1)                          0.06       8.08 f
U311/Y (OAI21X1)                          0.08       8.16 r
U310/Y (AOI21X1)                          0.07       8.23 f
U309/Y (NOR2X1)                           0.07       8.30 r
cruise_design_reg/D (DFFPOSX1)            0.00       8.30 r
data arrival time                                    8.30

clock clk (rise edge)                    10.00      10.00
clock network delay (ideal)               0.00      10.00
clock reconvergence pessimism             0.00      10.00
cruise_design_reg/CLK (DFFPOSX1)                    10.00 r
library setup time                       -0.19       9.81
data required time                                   9.81
-----------------------------------------------------------
data required time                                   9.81
data arrival time                                   -8.30
-----------------------------------------------------------
slack (MET)                                          1.51
```

```
Startpoint: brake (input port clocked by clk)
Endpoint: cruise_speed_reg[0]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point                                 Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                 0.00       0.00
clock network delay (ideal)           0.00       0.00
input external delay                  4.00       4.00 f
brake (in)                            0.10       4.10 f
U475/Y (NOR2X1)                       0.08       4.18 r
U474/Y (OAI21X1)                      0.08       4.26 f
U449/Y (INVX1)                        0.06       4.32 r
U448/Y (AOI21X1)                      0.06       4.38 f
U447/Y (NAND3X1)                      0.39       4.77 r
U416/Y (MUX2X1)                       0.19       4.96 f
U415/Y (INVX1)                        0.18       5.14 r
U241/Y (OR2X1)                        0.17       5.31 r
U239/Y (OR2X1)                        0.16       5.47 r
U238/Y (OR2X1)                        0.16       5.63 r
U236/Y (OR2X1)                        0.16       5.79 r
U204/Y (XOR2X1)                       0.12       5.91 f
U389/Y (OAI21X1)                      0.10       6.01 r
U388/Y (INVX1)                        0.11       6.11 f
U387/Y (OAI21X1)                      0.09       6.20 r
U386/Y (OAI21X1)                      0.43       6.63 f
U382/Y (NAND2X1)                      0.48       7.11 r
U381/Y (NOR2X1)                       0.39       7.49 f
U230/Y (AND2X2)                       0.30       7.79 f
U379/Y (NOR2X1)                       0.30       8.09 r
U350/Y (AOI22X1)                      0.10       8.19 f
U349/Y (OAI21X1)                      0.09       8.27 r
cruise_speed_reg[0]/D (DFFPOSX1)      0.00       8.27 r
data arrival time                                8.27

clock clk (rise edge)                 10.00      10.00
clock network delay (ideal)           0.00       10.00
clock reconvergence pessimism         0.00       10.00
cruise_speed_reg[0]/CLK (DFFPOSX1)                10.00 r
```

library setup time	-0.19	9.81
data required time		9.81
data required time		9.81
data arrival time		-8.27
slack (MET)		1.54

Startpoint: brake (input port clocked by clk)
Endpoint: cruise_speed_reg[4]
(rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: max

Point	Incr	Path
clock clk (rise edge)	0.00	0.00
clock network delay (ideal)	0.00	0.00
input external delay	4.00	4.00 f
brake (in)	0.10	4.10 f
U475/Y (NOR2X1)	0.08	4.18 r
U474/Y (OAI21X1)	0.08	4.26 f
U449/Y (INVX1)	0.06	4.32 r
U448/Y (AOI21X1)	0.06	4.38 f
U447/Y (NAND3X1)	0.39	4.77 r
U416/Y (MUX2X1)	0.19	4.96 f
U415/Y (INVX1)	0.18	5.14 r
U241/Y (OR2X1)	0.17	5.31 r
U239/Y (OR2X1)	0.16	5.47 r
U238/Y (OR2X1)	0.16	5.63 r
U236/Y (OR2X1)	0.16	5.79 r
U204/Y (XOR2X1)	0.12	5.91 f
U389/Y (OAI21X1)	0.10	6.01 r
U388/Y (INVX1)	0.11	6.11 f
U387/Y (OAI21X1)	0.09	6.20 r
U386/Y (OAI21X1)	0.43	6.63 f
U382/Y (NAND2X1)	0.48	7.11 r
U381/Y (NOR2X1)	0.39	7.49 f
U230/Y (AND2X2)	0.30	7.79 f
U379/Y (NOR2X1)	0.30	8.09 r
U341/Y (AOI22X1)	0.10	8.19 f
U340/Y (OAI21X1)	0.09	8.27 r

```
  cruise_speed_reg[4]/D (DFFPOSX1)         0.00       8.27 r
  data arrival time                                   8.27

  clock clk (rise edge)                   10.00      10.00
  clock network delay (ideal)              0.00      10.00
  clock reconvergence pessimism            0.00      10.00
  cruise_speed_reg[4]/CLK (DFFPOSX1)                 10.00 r
  library setup time                      -0.19       9.81
  data required time                                  9.81
  ----------------------------------------------------------
  data required time                                  9.81
  data arrival time                                  -8.27
  ----------------------------------------------------------
  slack (MET)                                         1.54
```

Warning: report_timing has satisfied the max_paths criteria. There are 6 further endpoints which have paths of interest with slack less than 3.00 that were not considered when generating this report. (UITE-502)

1

5. min_paths.txt

```
****************************************
Report : timing
        -path_type full
        -delay_type min
        -slack_lesser_than 3.00
        -max_paths 3
        -sort_by slack
Design : chenjie_module
Version: L-2016.06-SP1
Date   : Thu Apr 11 21:43:08 2019
****************************************


  Startpoint: cancel (input port clocked by clk)
  Endpoint: cruise_design_reg
            (rising edge-triggered flip-flop clocked by clk)
  Path Group: clk
  Path Type: min

  Point                                Incr       Path
  -----------------------------------------------------------
```

clock clk (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
input external delay 0.00 0.00 f
cancel (in) 0.01 0.01 f
U318/Y (NOR2X1) 0.07 0.08 r
U310/Y (AOI21X1) 0.06 0.14 f
U309/Y (NOR2X1) 0.05 0.19 r
cruise_design_reg/D (DFFPOSX1) 0.00 0.19 r
data arrival time 0.19

clock clk (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
clock reconvergence pessimism 0.00 0.00
cruise_design_reg/CLK (DFFPOSX1) 0.00 r
library hold time 0.00 0.00
data required time 0.00
---
data required time 0.00
data arrival time -0.19
---
slack (MET) 0.19

Startpoint: rst (input port clocked by clk)
Endpoint: speed_reg[0]
(rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Point Incr Path
---
clock clk (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
input external delay 0.00 0.00 f
rst (in) 0.13 0.13 f
U354/Y (NOR2X1) 0.10 0.23 r
speed_reg[0]/D (DFFPOSX1) 0.00 0.23 r
data arrival time 0.23

clock clk (rise edge) 0.00 0.00
clock network delay (ideal) 0.00 0.00
clock reconvergence pessimism 0.00 0.00
speed_reg[0]/CLK (DFFPOSX1) 0.00 r

```
library hold time                      0.00       0.00
data required time                                0.00
-----------------------------------------------------------
data required time                                0.00
data arrival time                                -0.23
-----------------------------------------------------------
slack (MET)                                       0.22


Startpoint: rst (input port clocked by clk)
Endpoint: speed_reg[1]
          (rising edge-triggered flip-flop clocked by clk)
Path Group: clk
Path Type: min

Point                                   Incr       Path
-----------------------------------------------------------
clock clk (rise edge)                  0.00       0.00
clock network delay (ideal)            0.00       0.00
input external delay                   0.00       0.00 f
rst (in)                               0.13       0.13 f
U364/Y (NOR2X1)                        0.10       0.23 r
speed_reg[1]/D (DFFPOSX1)              0.00       0.23 r
data arrival time                                 0.23

clock clk (rise edge)                  0.00       0.00
clock network delay (ideal)            0.00       0.00
clock reconvergence pessimism          0.00       0.00
speed_reg[1]/CLK (DFFPOSX1)                       0.00 r
library hold time                      0.00       0.00
data required time                                0.00
-----------------------------------------------------------
data required time                                0.00
data arrival time                                -0.23
-----------------------------------------------------------
slack (MET)                                       0.22
```

Warning: report_timing has satisfied the max_paths criteria. There are 14 further endpoints which have paths of interest with slack less than 3.00 that were not considered when generating this report. (UITE-502)