ECEN 714 Lab 7 report
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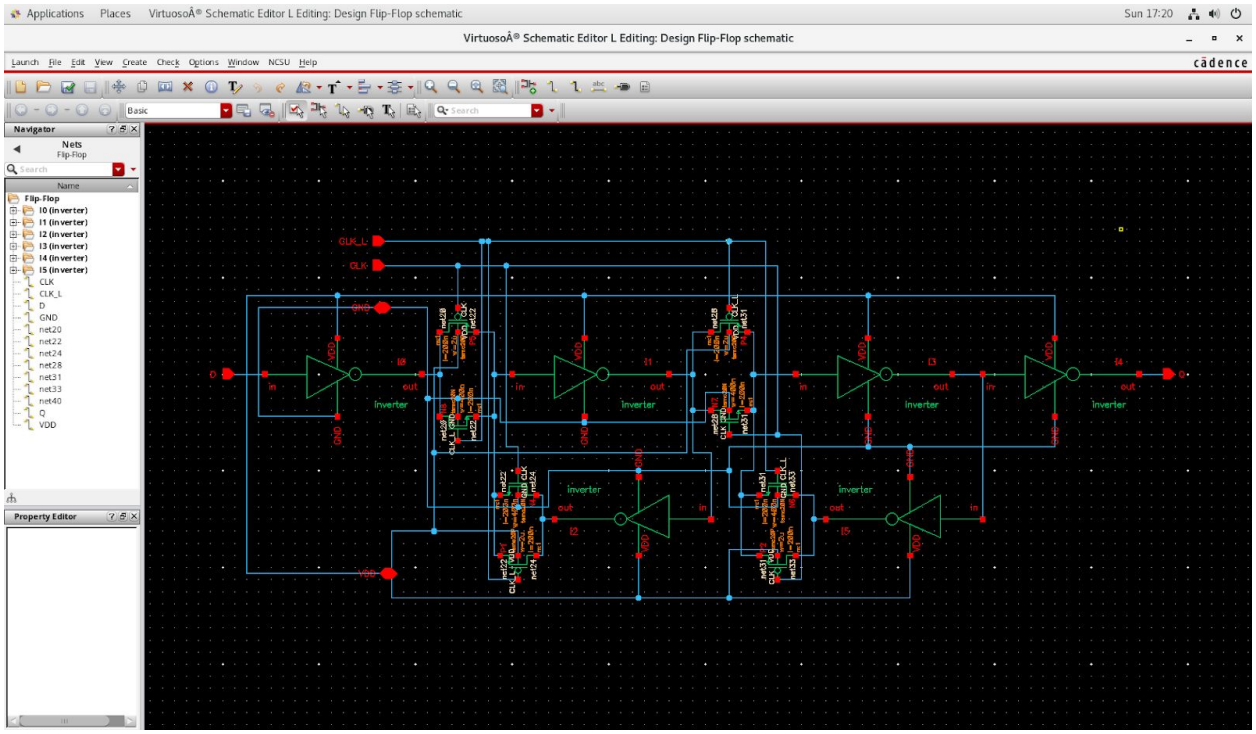

Fig. Schematic of my Flip-Flop

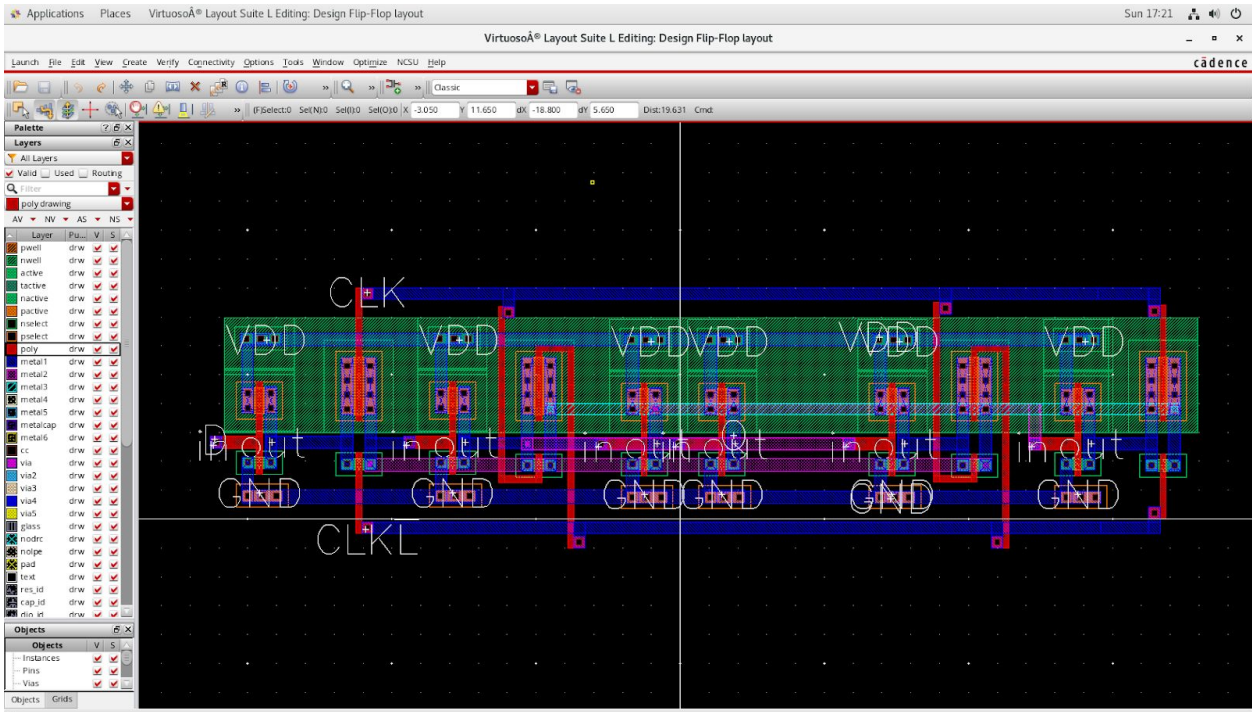

Fig. Layout of my Flip-Flop

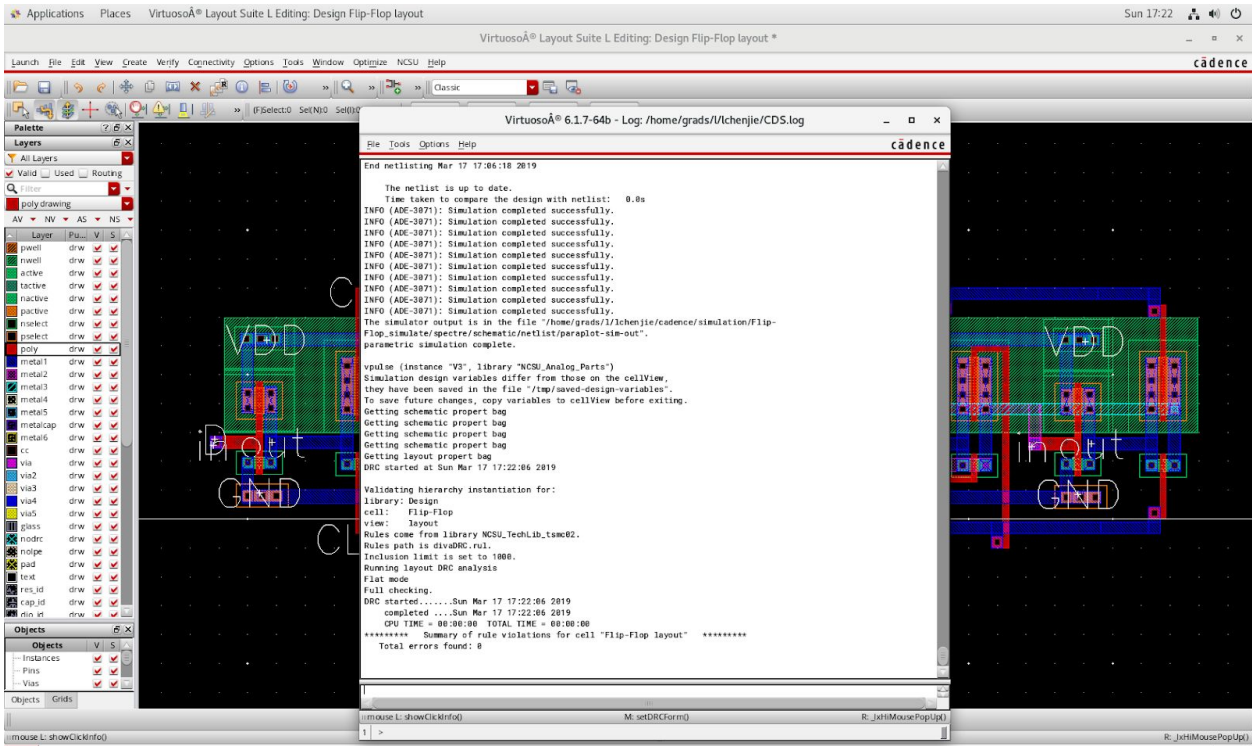

Fig. DRC log

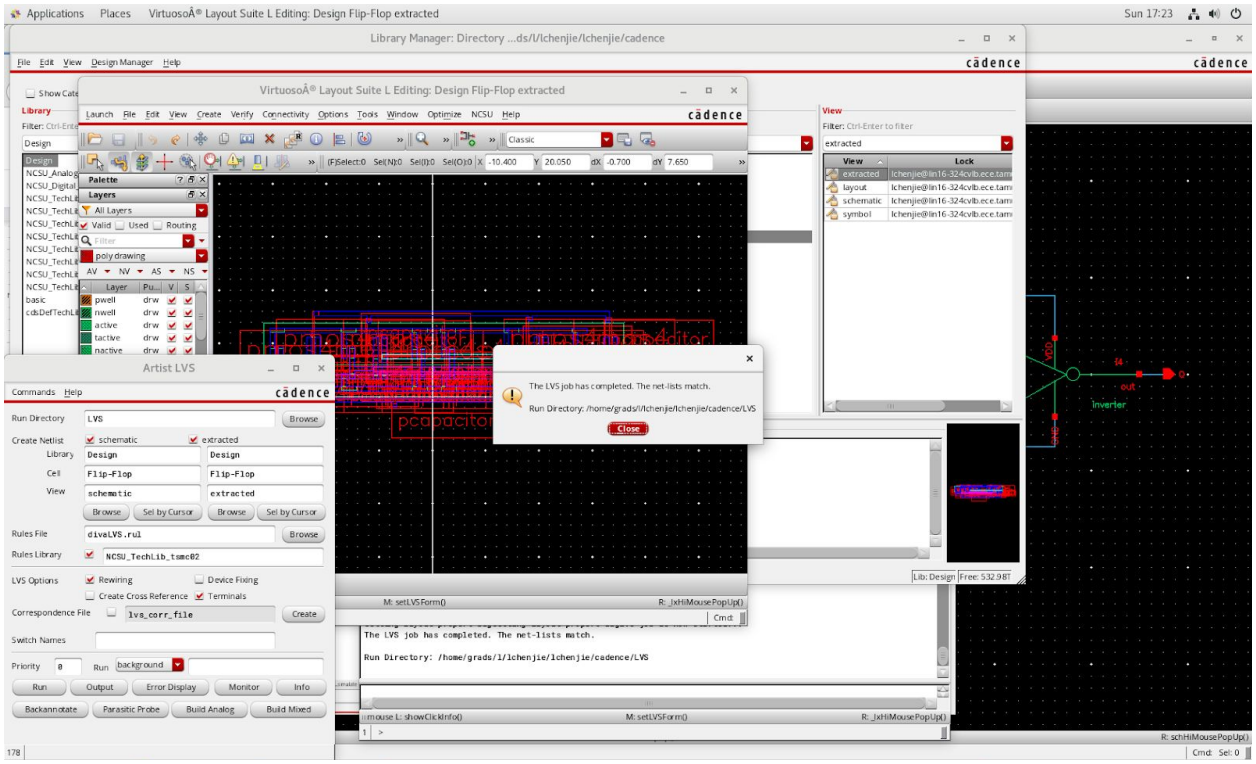

Fig. LVS result

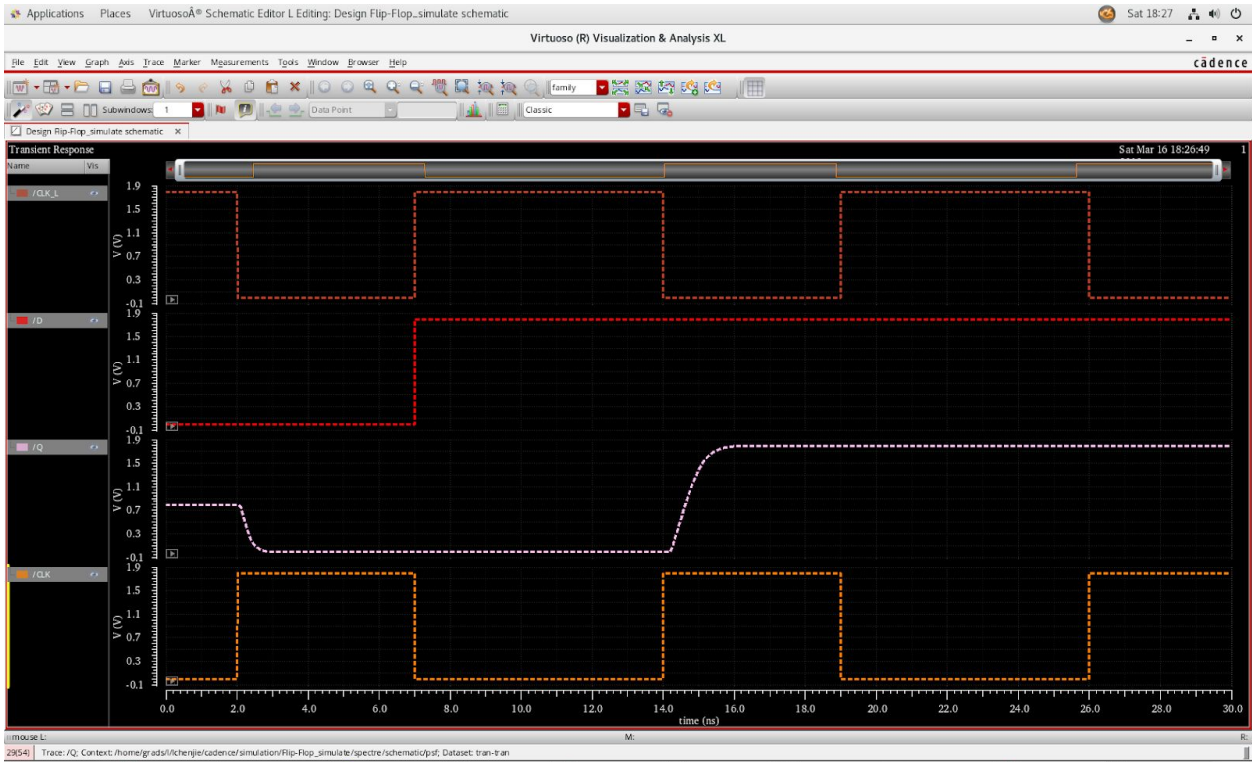

Fig. Functionality of my Flip-Flop meets the requirement

Tab.1 rising and falling clock-to-Q of my Flip-Flop

Output Load(fF)	Rising delay(ns)	Falling delay(ns)	difference/ Rising delay(%)	difference / Falling delay(%)
1	0.2262	0.2173	3.934571176	4.095720202
10	0.275	0.2652	3.563636364	3.695324284
20	0.3215	0.3073	4.416796267	4.620891637
30	0.3663	0.3454	5.705705706	6.050955414
40	0.4106	0.3823	6.892352655	7.402563432
50	0.4549	0.4186	7.979775775	8.67176302
60	0.4989	0.4549	8.819402686	9.672455485
70	0.5436	0.491	9.676232524	10.71283096
80	0.587	0.527	10.22146508	11.38519924
90	0.6315	0.5432	13.98258116	16.25552283
100	0.6804	0.5578	18.01881246	21.97920402

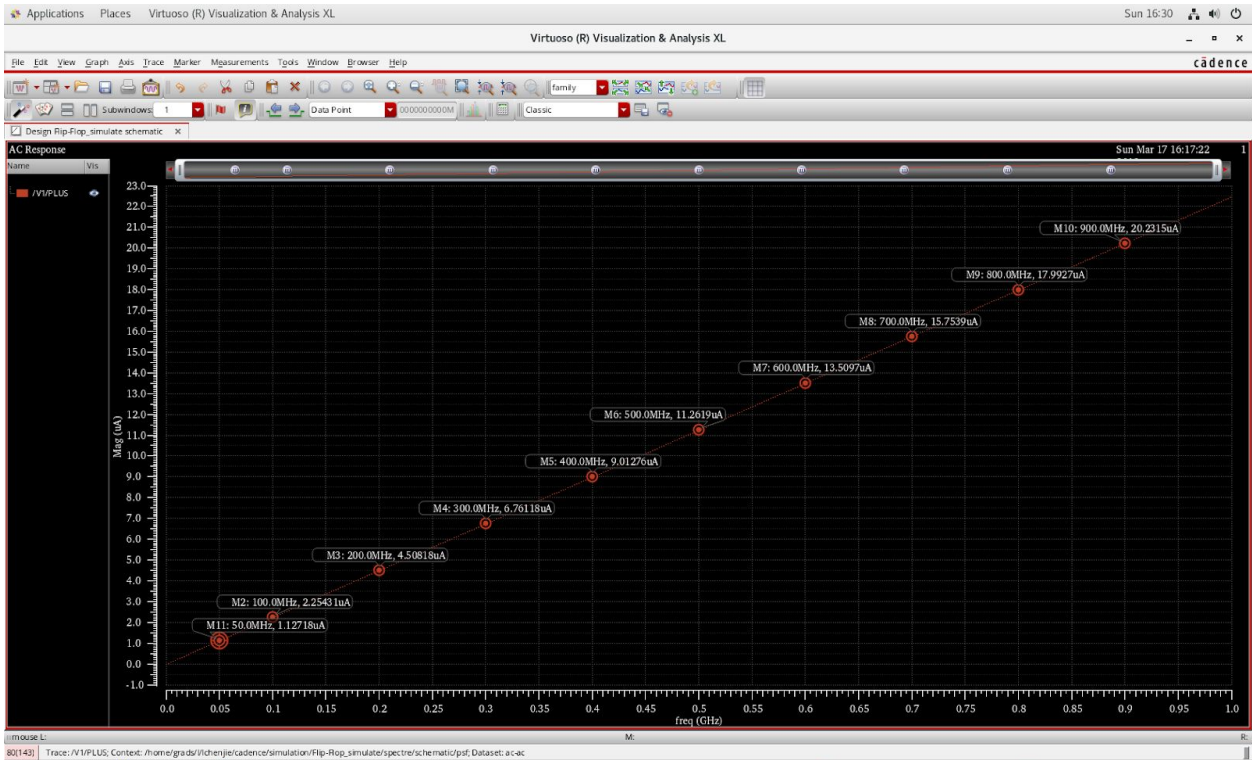

Fig. input current vs. frequency in AC simulation

Tab.2 Input capacitance

Current(uA)	Frequency(MHz)	Capacitance(fF)
1.12718	**50**	3.589745223
2.25431	**100**	3.589665605
4.50818	**200**	3.589315287
6.76118	**300**	3.58873673
9.01276	**400**	3.587882166
11.2619	**500**	3.586592357
13.5097	**600**	3.585376858
15.7539	**700**	3.583689718
17.9927	**800**	3.581349522
20.2315	**900**	3.57952937

Thus, the average input capacitance is 3.586188284 fF.

LVS report:

@(#)$CDS: LVS version 6.1.7-64b 01/24/2017 19:46 (sjfhw310) $

Command line: /softwares/Linux/cadence/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/l/lchenjie/lchenjie/cadence/LVS -l -s -t /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout/netlist

count	
13	nets
6	terminals
10	pmos
10	nmos

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic/netlist

count	
13	nets
6	terminals
10	pmos
10	nmos

Terminal correspondence points

N10	N6	CLK
N7	N12	CLK_L
N11	N11	D
N8	N9	GND
N9	N8	Q
N12	N10	VDD

Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

layout schematic

	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	20	20
total	20	20

	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	13	13
total	13	13

	terminals	
un-matched	0	0
matched but different type	0	0
total	6	6

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

Audit.out:

Fig. Sweeping posedge of D signal along clk rising edge

As we can see, when D signal arrives later than 2.7 ns, Q be will updated with previous D signal. Thus, set up time for positive edge is 3.0 ns - 2.7 ns = 0.3ns.

Fig. Sweep negedge of D singal along clk rising edge

Similarly, When falling edge of D arrives later than 14.8 ns while posedge of clk signal arrives at 15.0 ns, Q will be updated with previous signal. Therefore, set up time for falling edge is 0.2 ns

Since the set up time is supposed to be satisfy both posedge and negedge conditions, **set up time = 0.3 ns.**