ECEN 714 Lab 8
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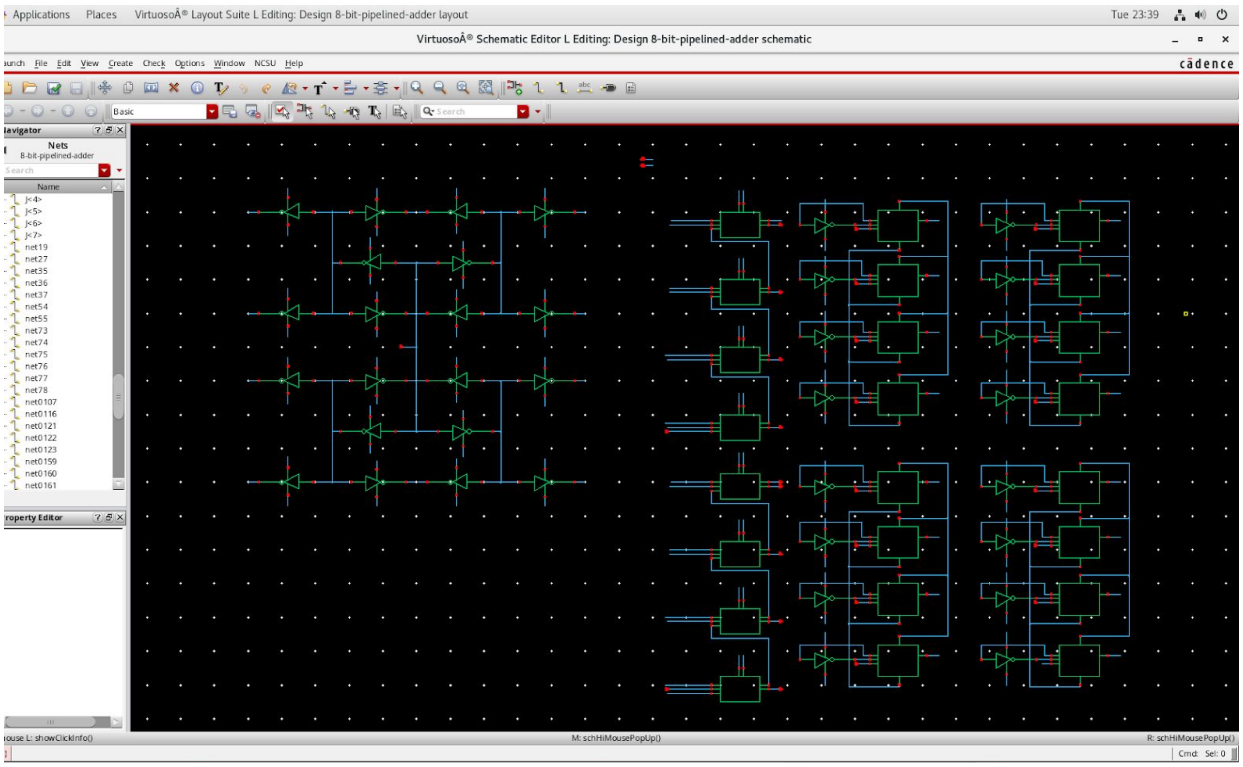


Fig. Schematic of my 8 bit pipelined adder

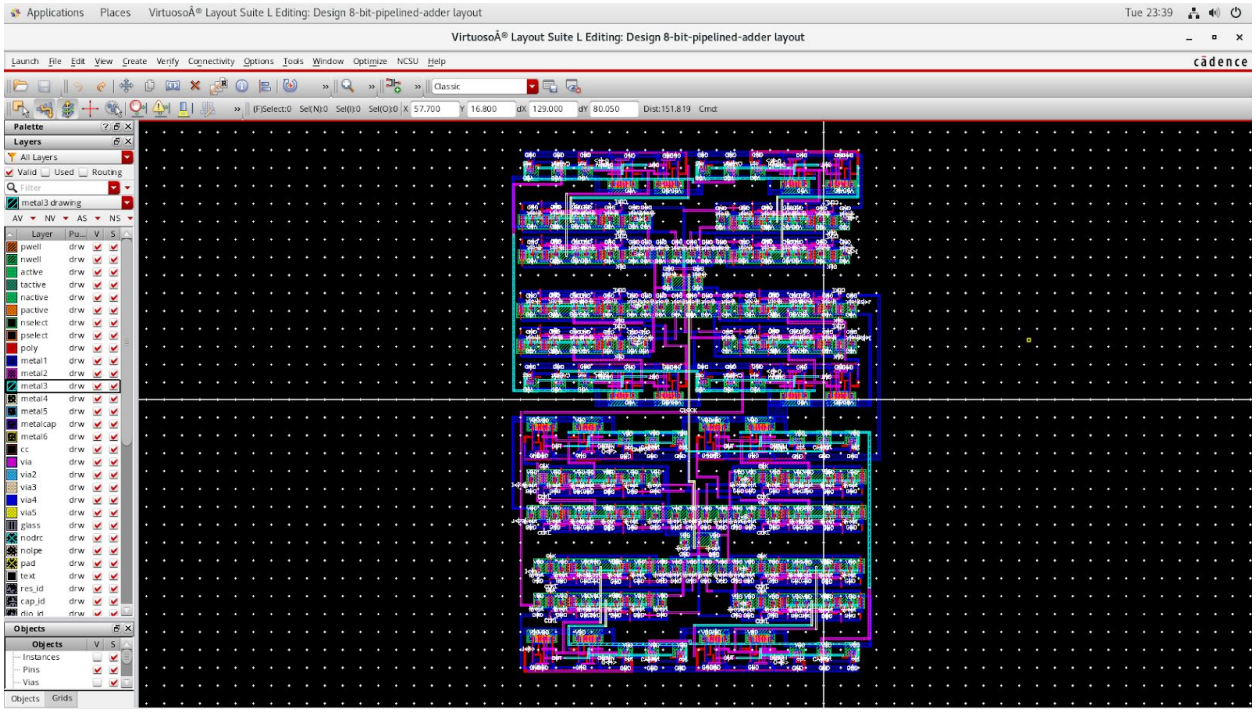


Fig. Layout of my 8-bit pipelined adder

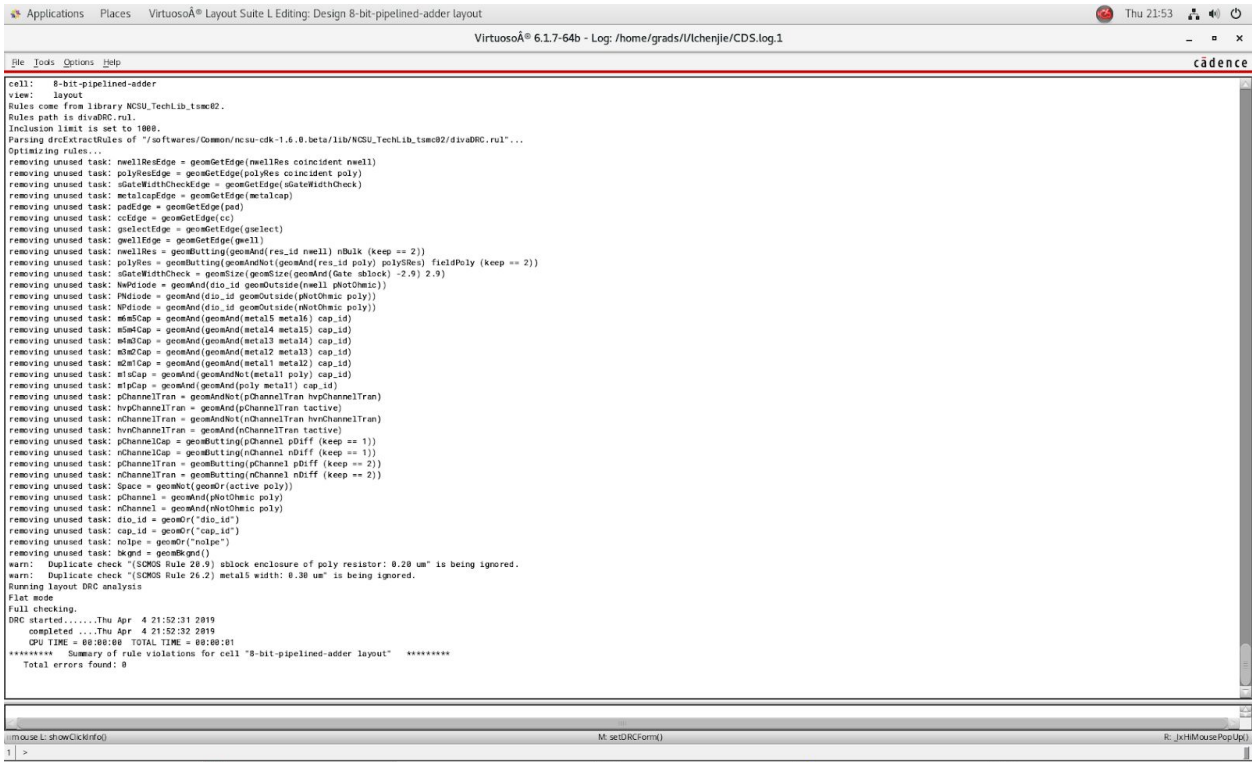


Fig. DRC check

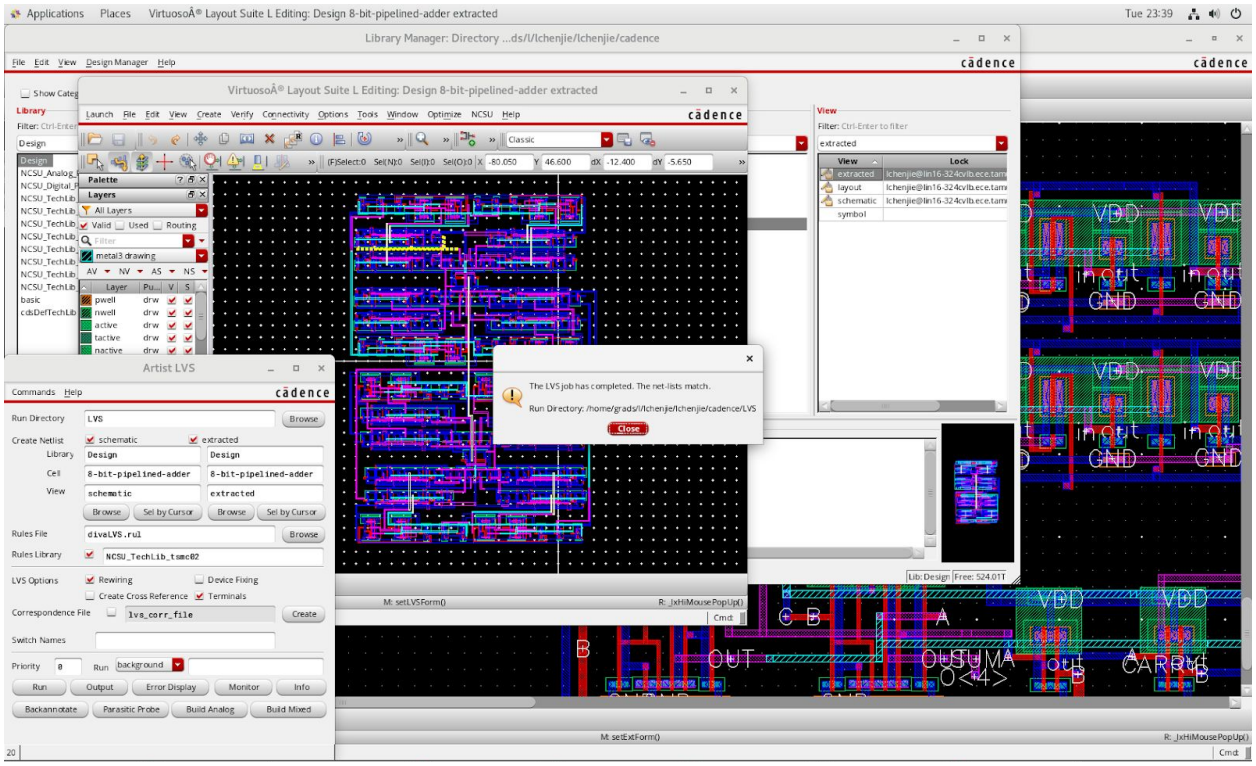


Fig. LVS check

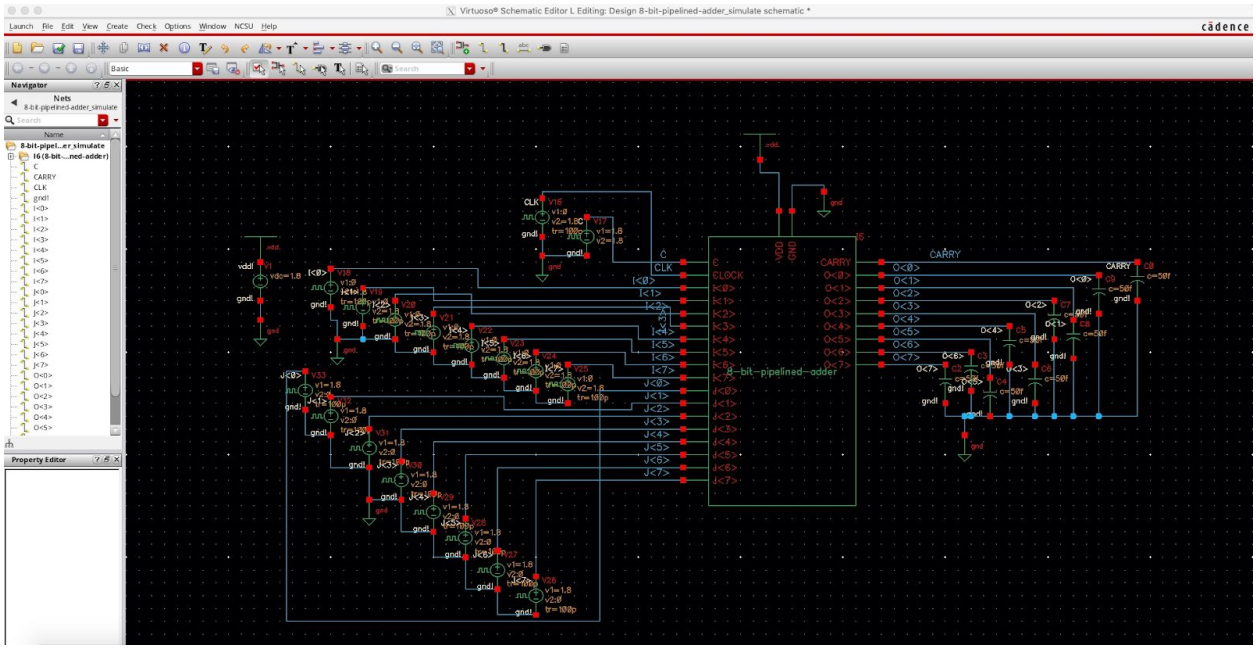


Fig. Simulation of my 8-bit pipelined adder

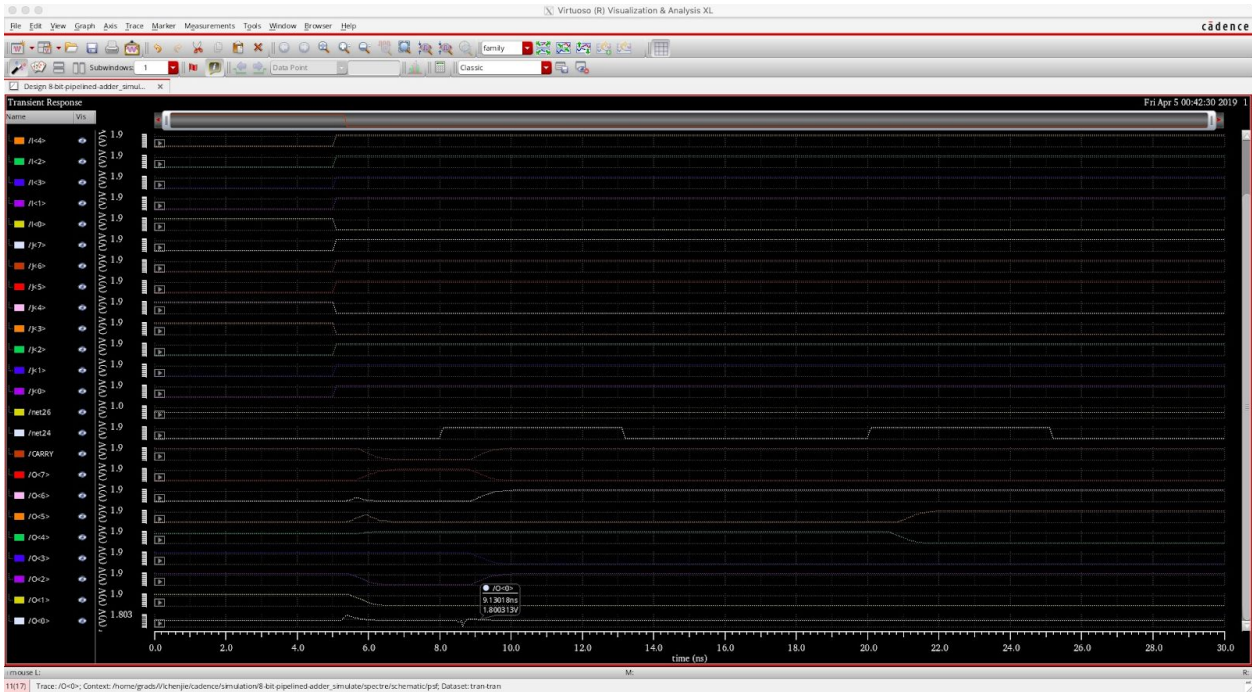


Fig. Output of 01111110 + 11100111 + 0

The output of 01111110 + 11100111 + CARRY 0 is read as CARRY 1 + 01100101

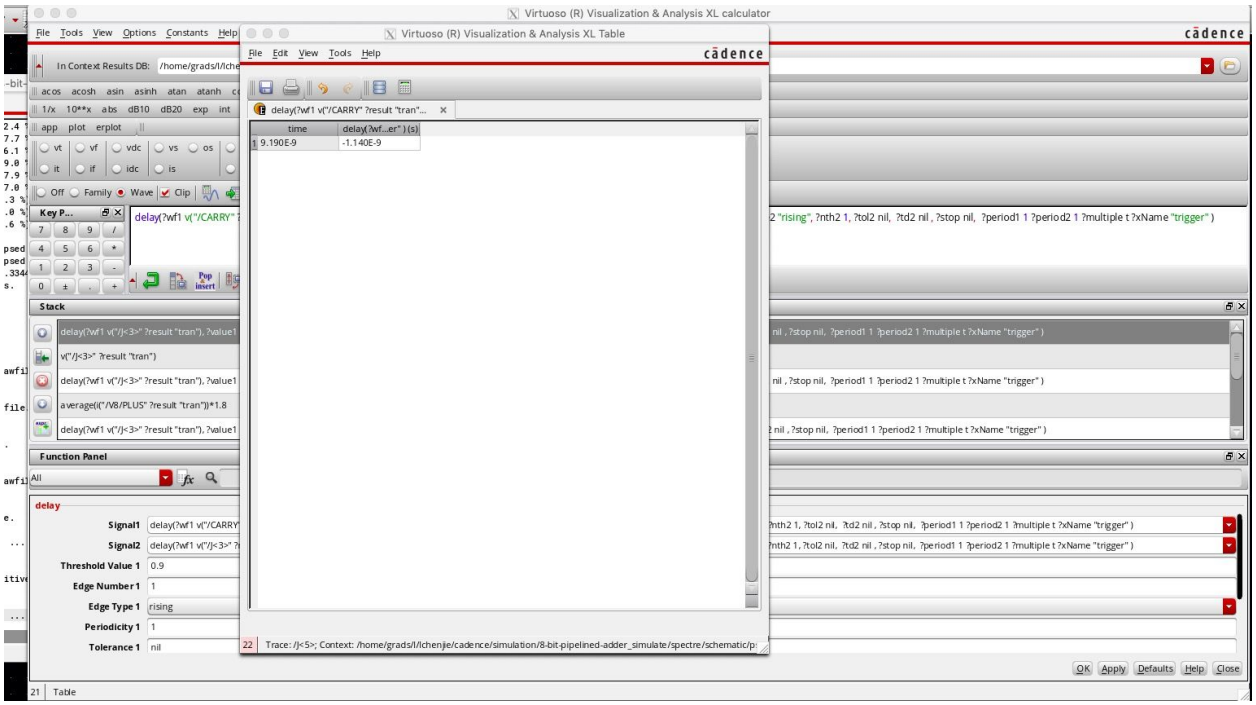


Fig. td for first case

Since setup time obtained in lab 7 is 0.3ns. Therefore, clock period needs to be greater than 0.3ns + 1.14ns = 1.44ns

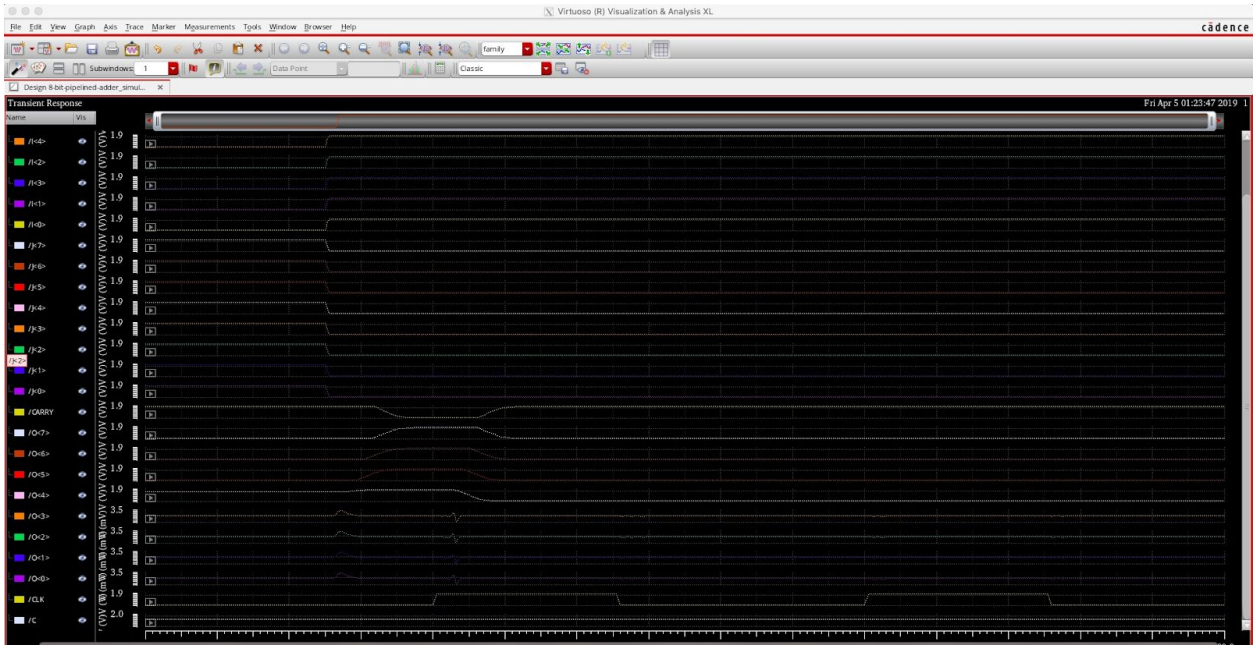


Fig. Output of 11111111+00000000+1

The output of 11111111+00000000+1 is 00000000 CARRY 1. Notice unit of O<3:0> in above figure is mV. Thus, they are actually logically low.

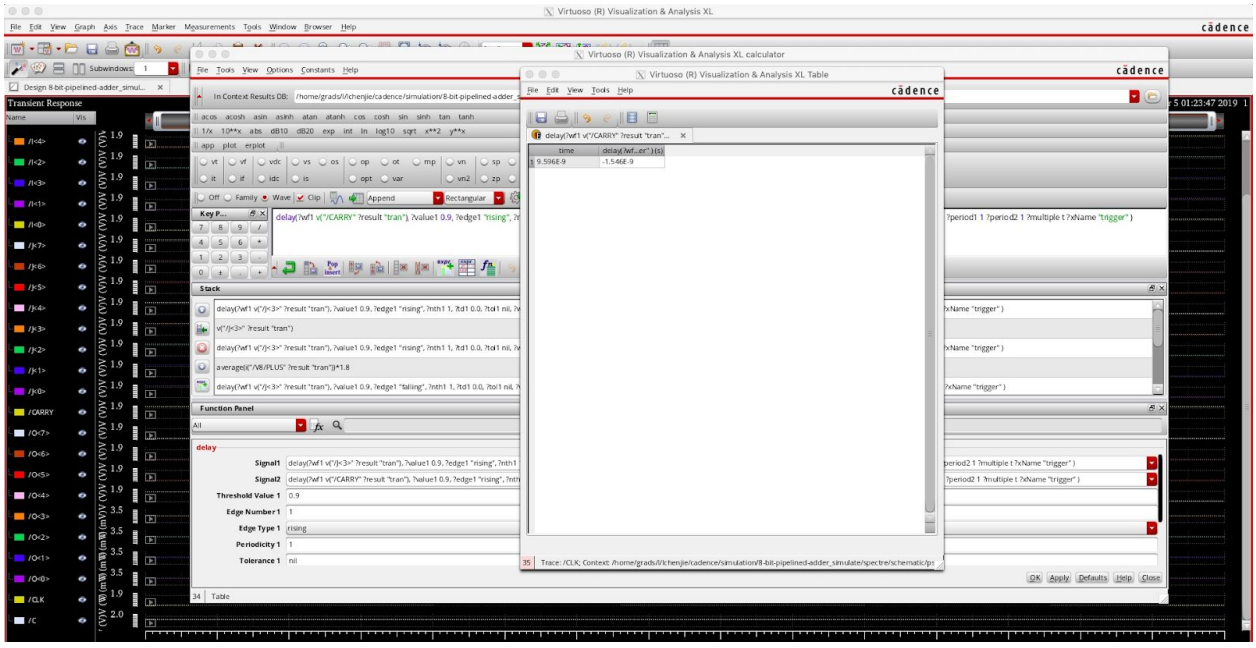
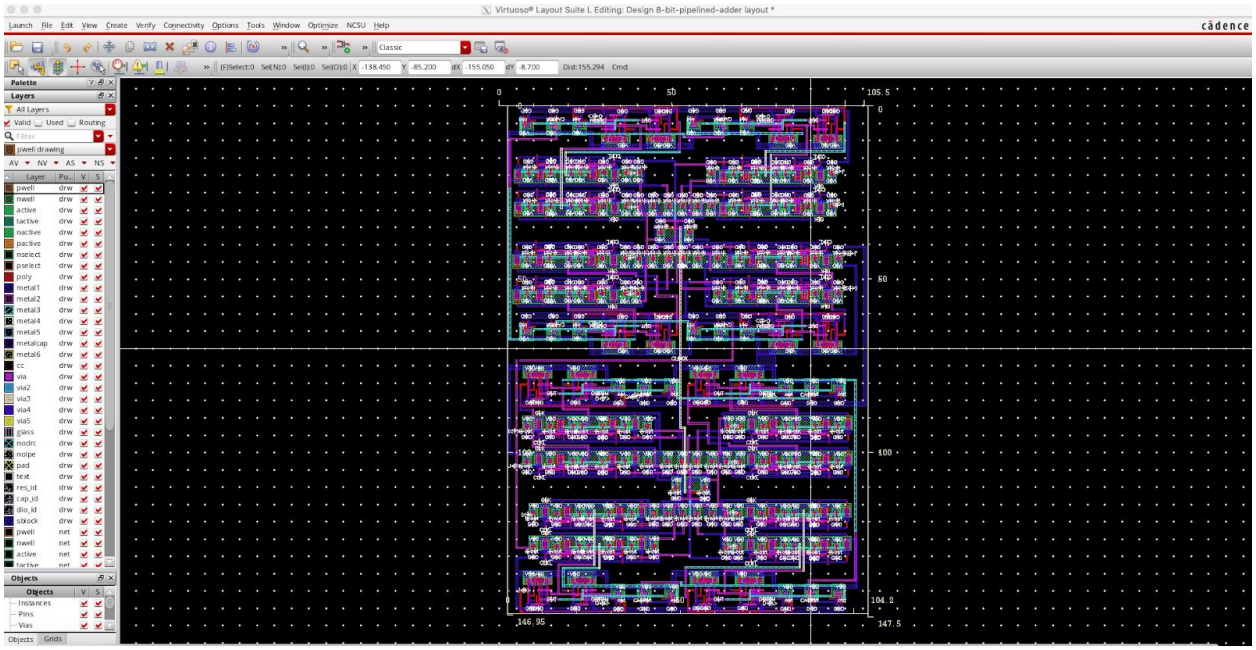


Fig. td of second case

Again since setup time is 0.3ns, clock period needs to be greater than 0.3ns + 1.54ns = 1.84ns



The area I used is 104.2*146.5 = 15265.3