ECEN 714 Lab 2 report
Chenjie Luo

1.Inverter

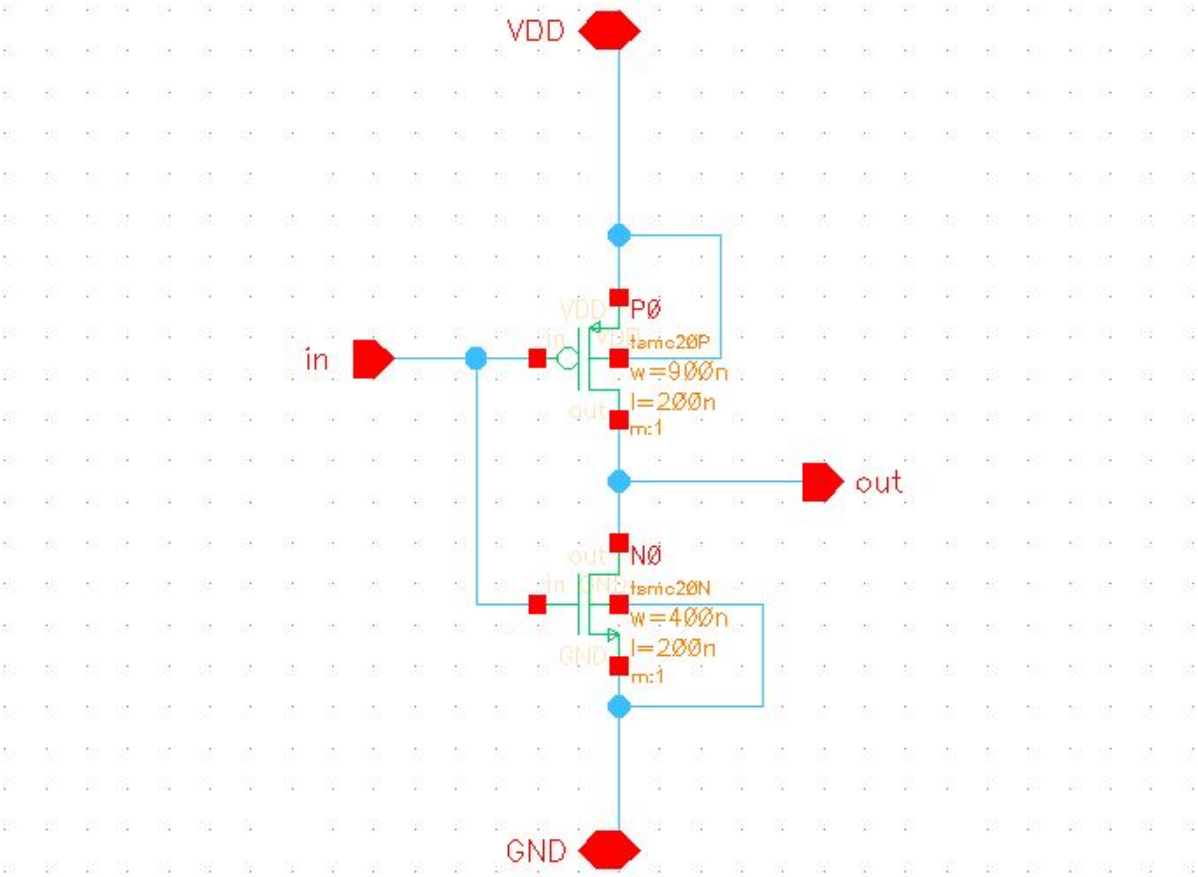

Fig.1 Schematics for inverter

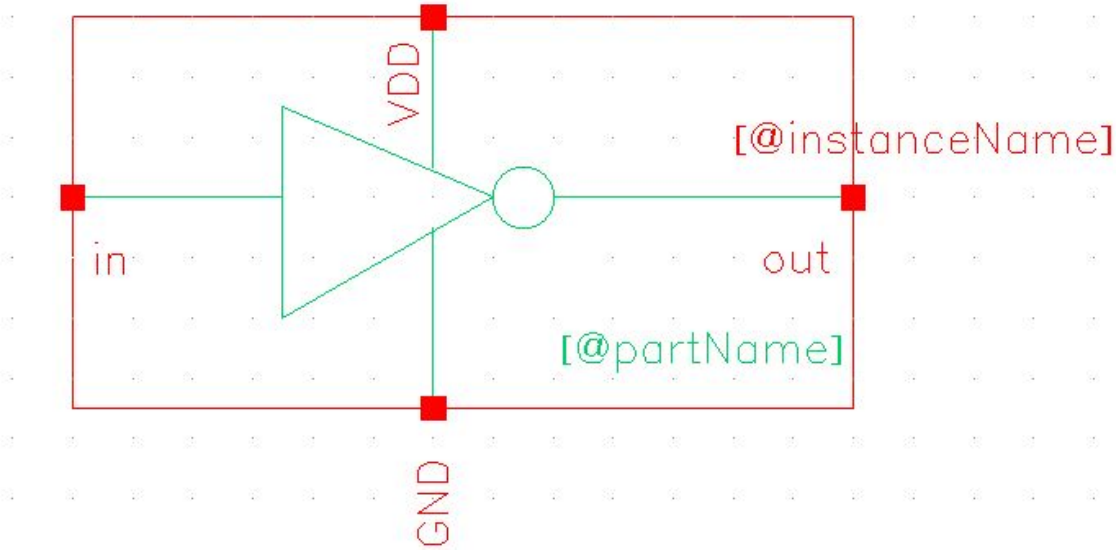

Fig.2 Symbol for inverter

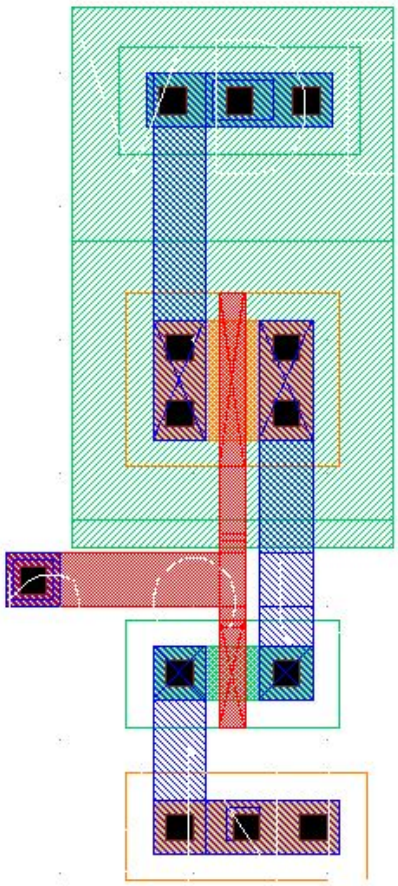

Fig.3 Layout for inverter

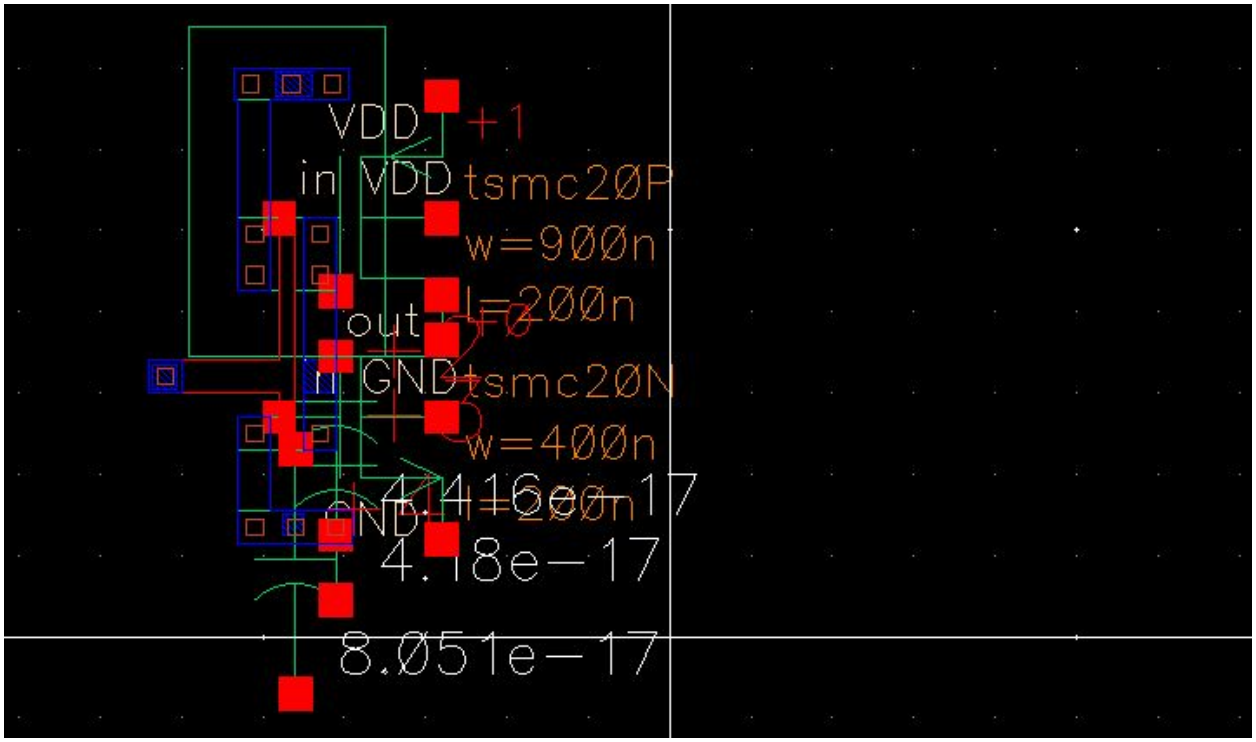

Fig.4 Extracted from inverter

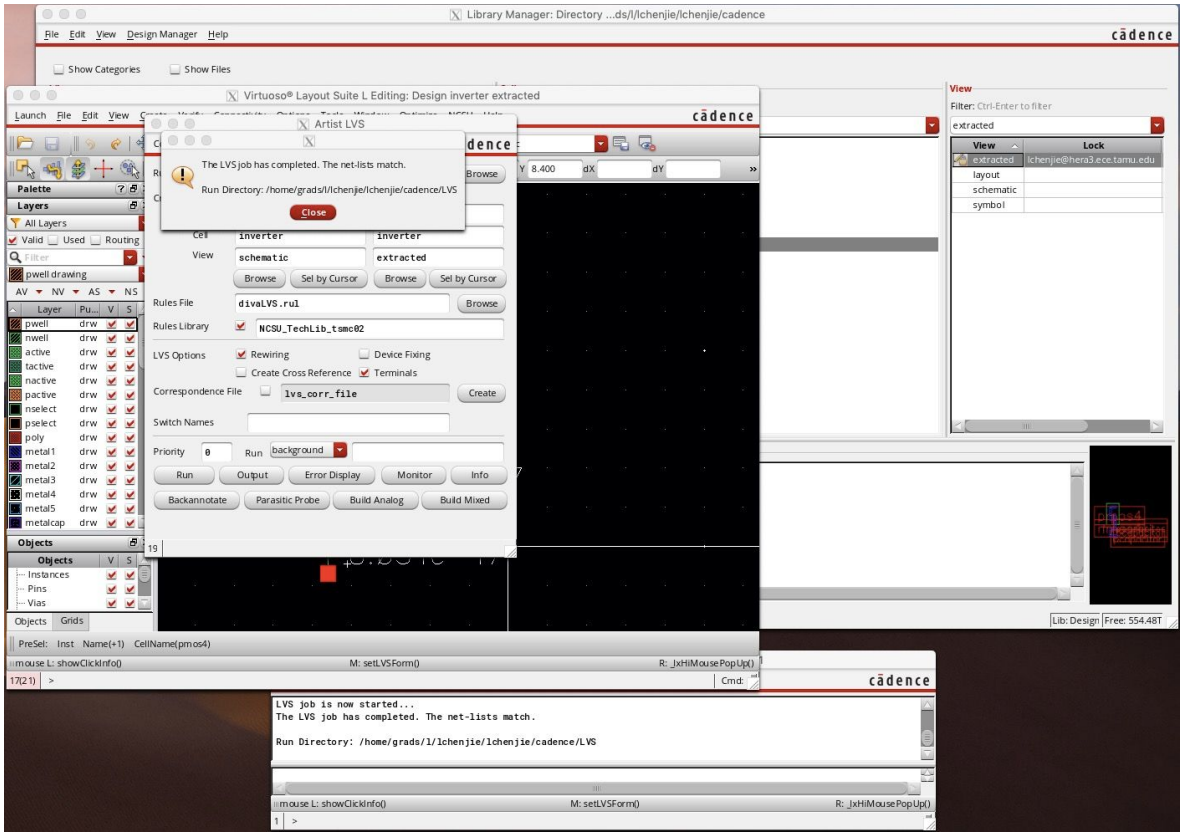

Fig.5 LVS result succeeds

2. NAND

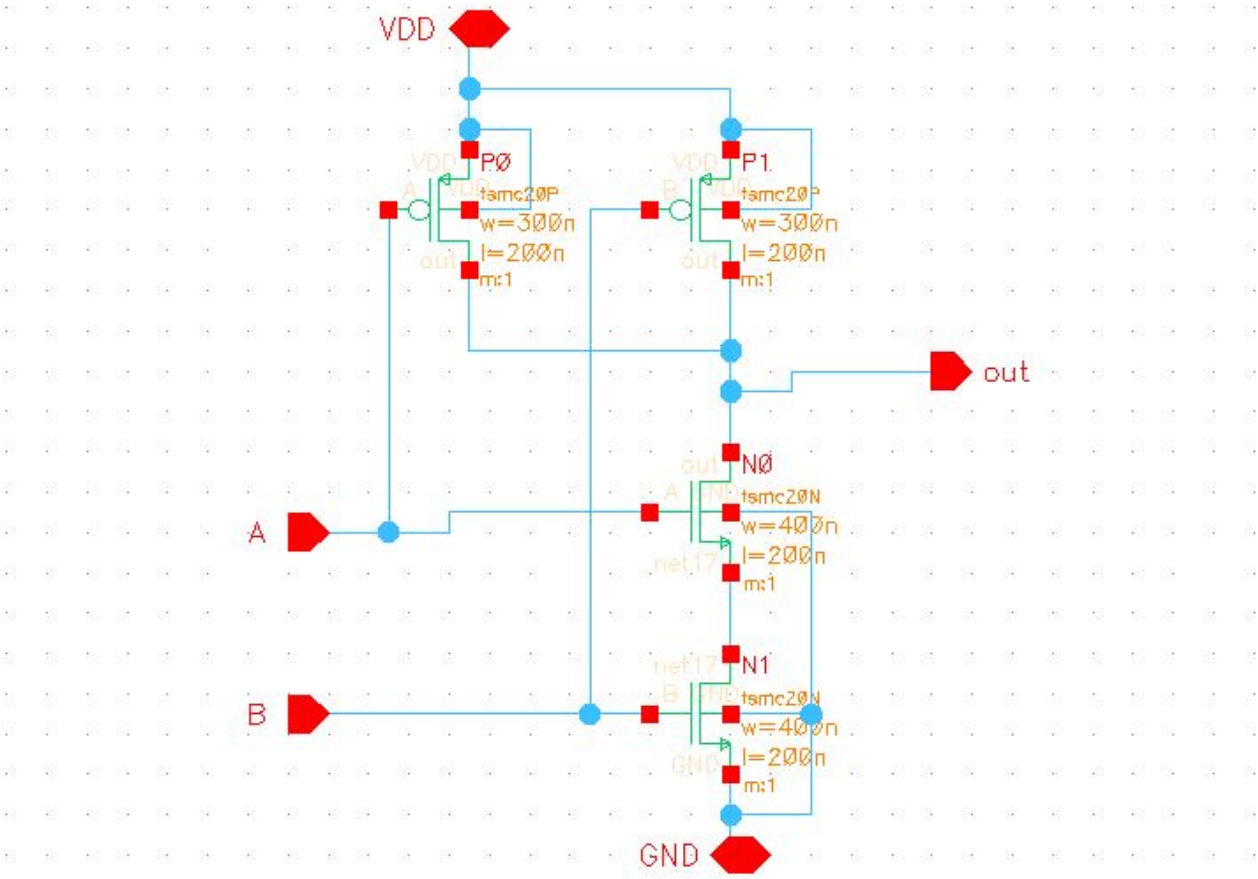

Fig.6 schematics for NAND

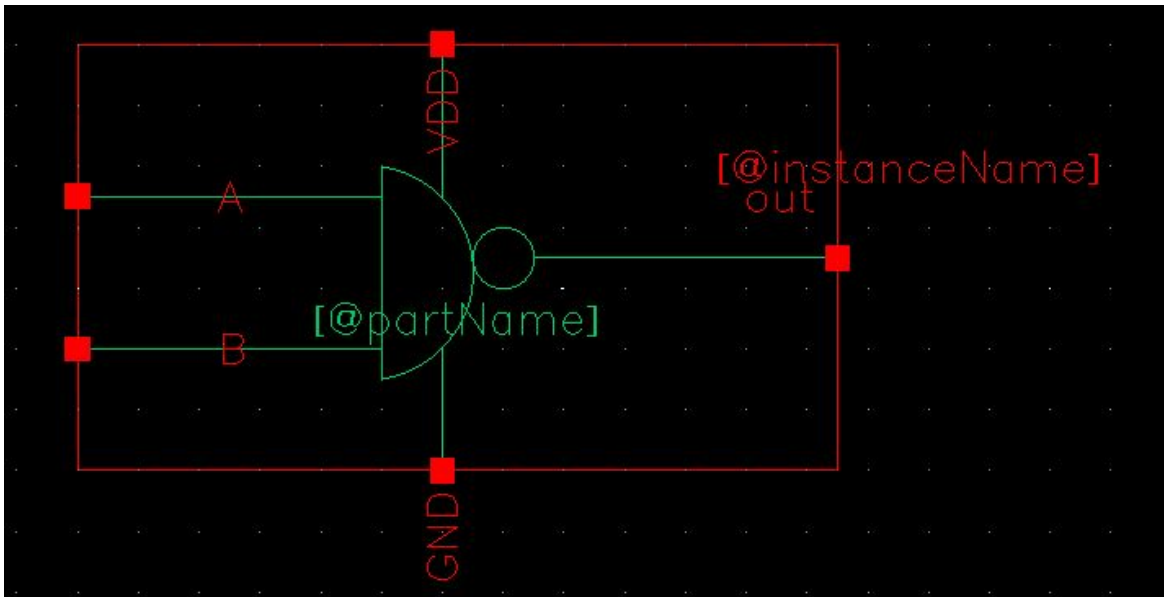

Fig.7 Symbol for NAND

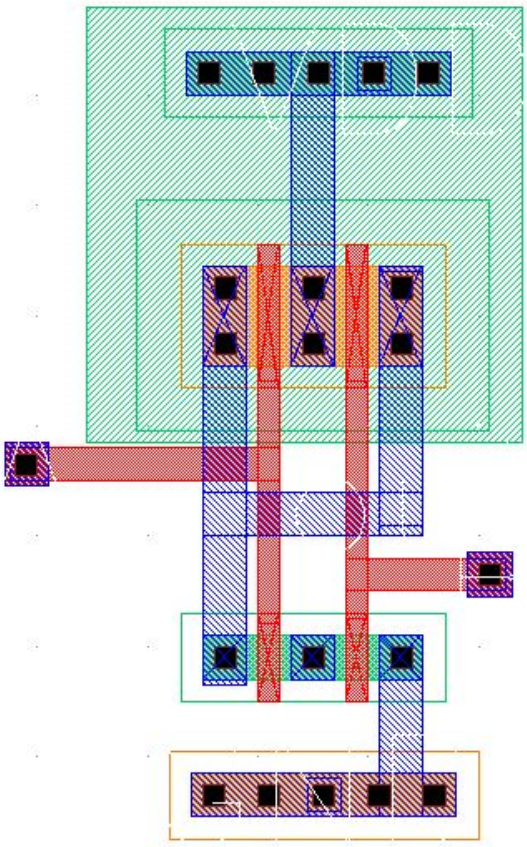

Fig.8 Layout for NAND

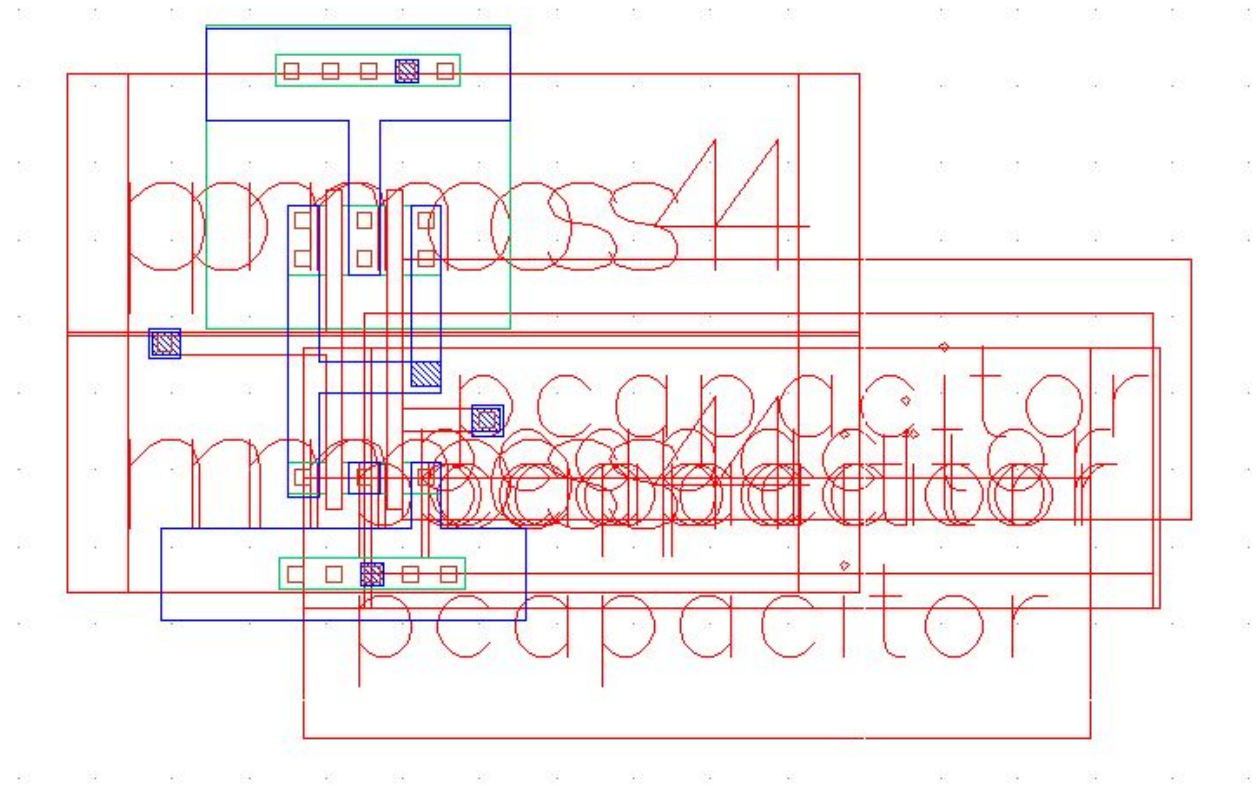

Fig.9 Extracted from NAND

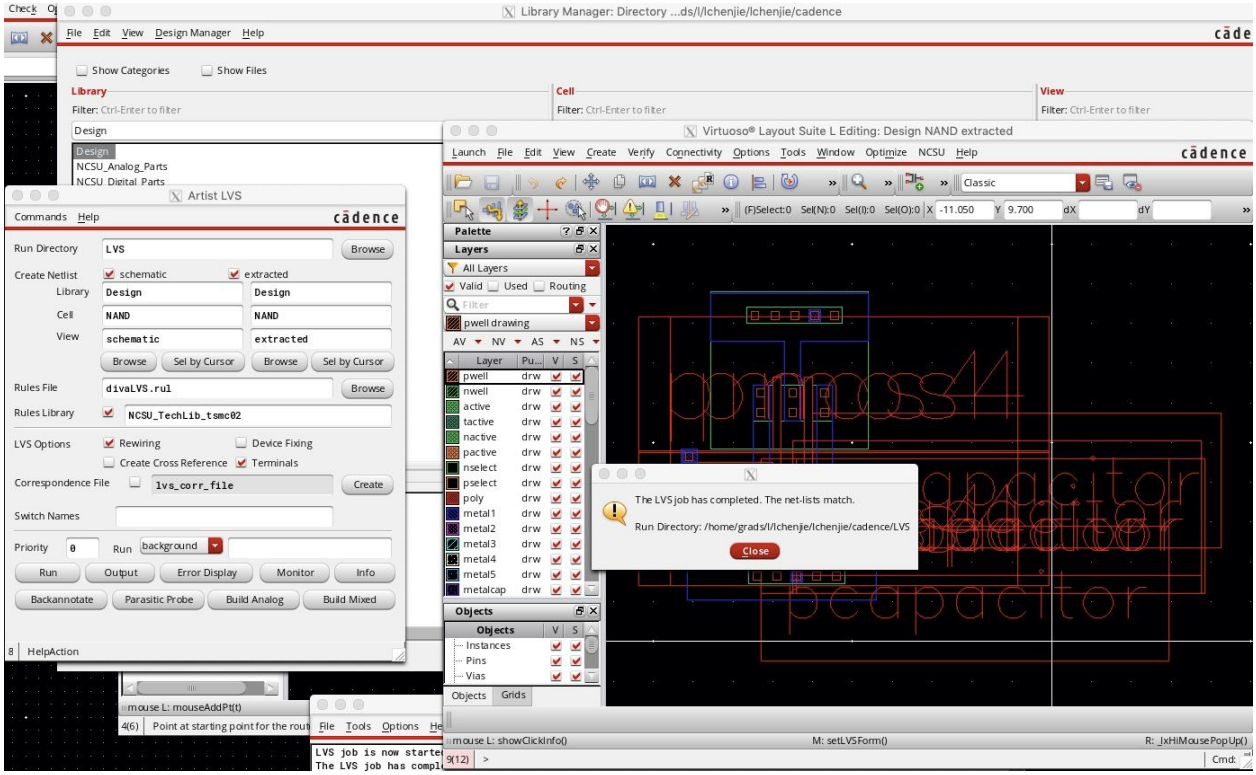

Fig.10 LVS result succeeds

3.XOR

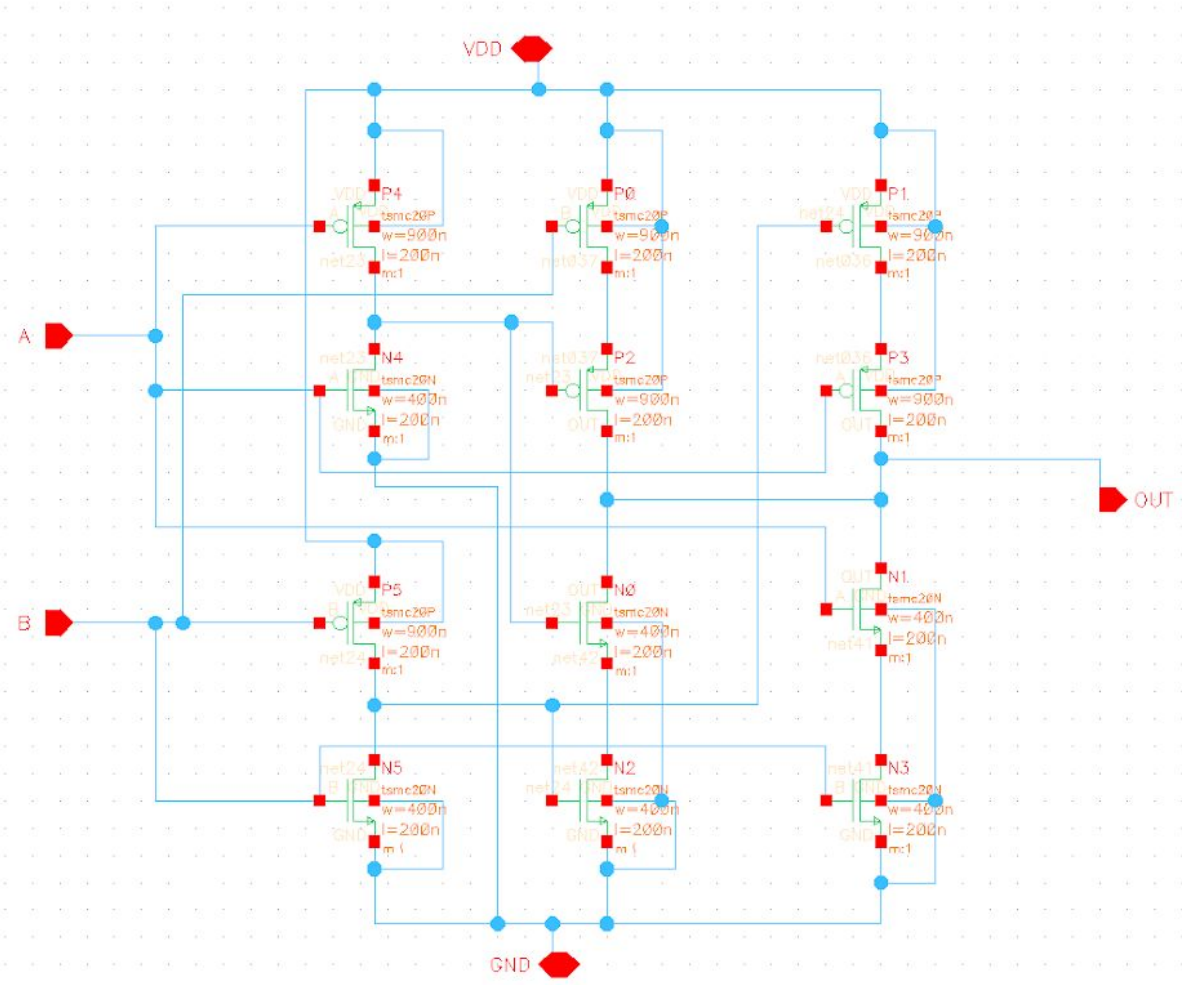

Fig.11 Schematics for XOR

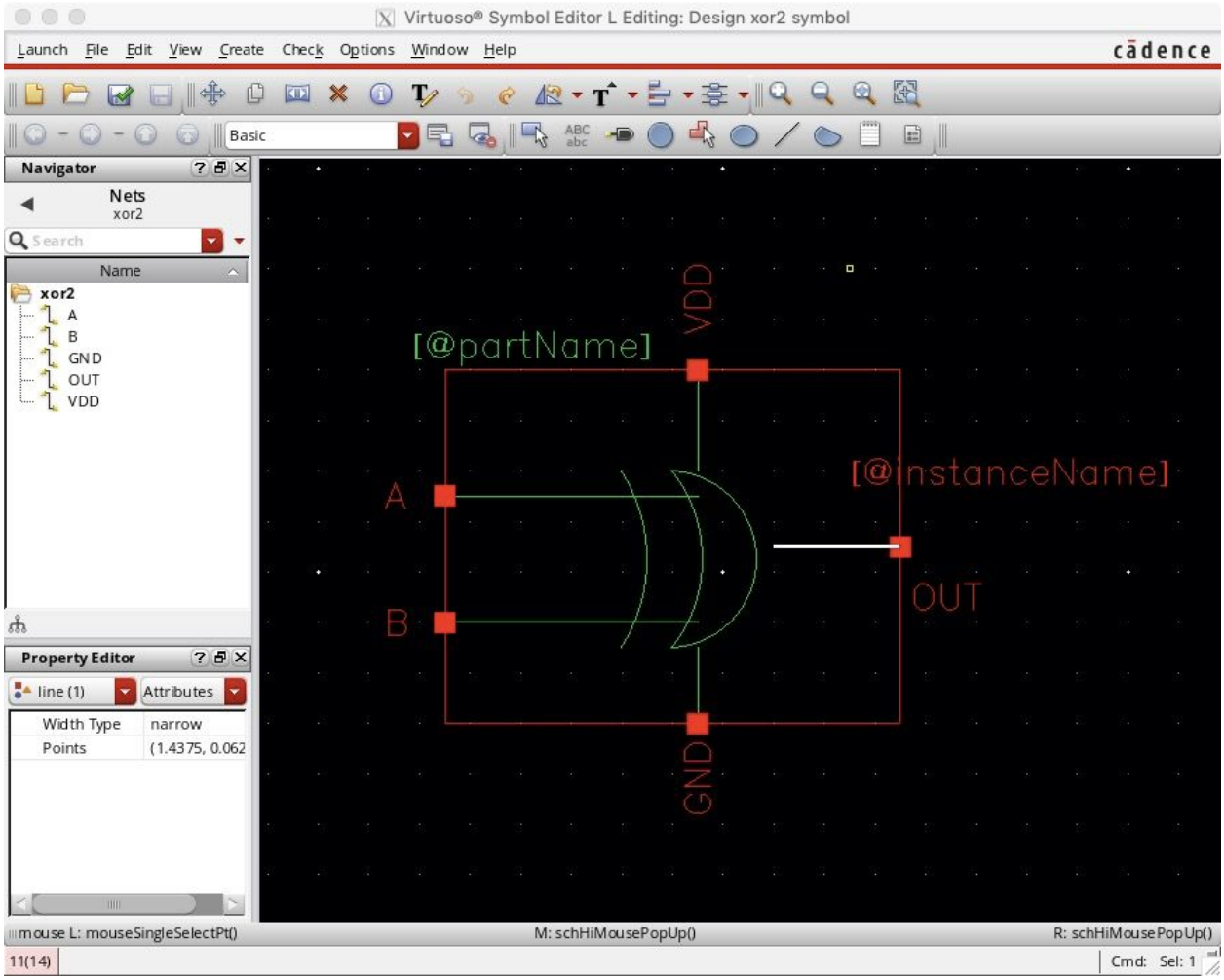

Fig.12 Symbol for XOR

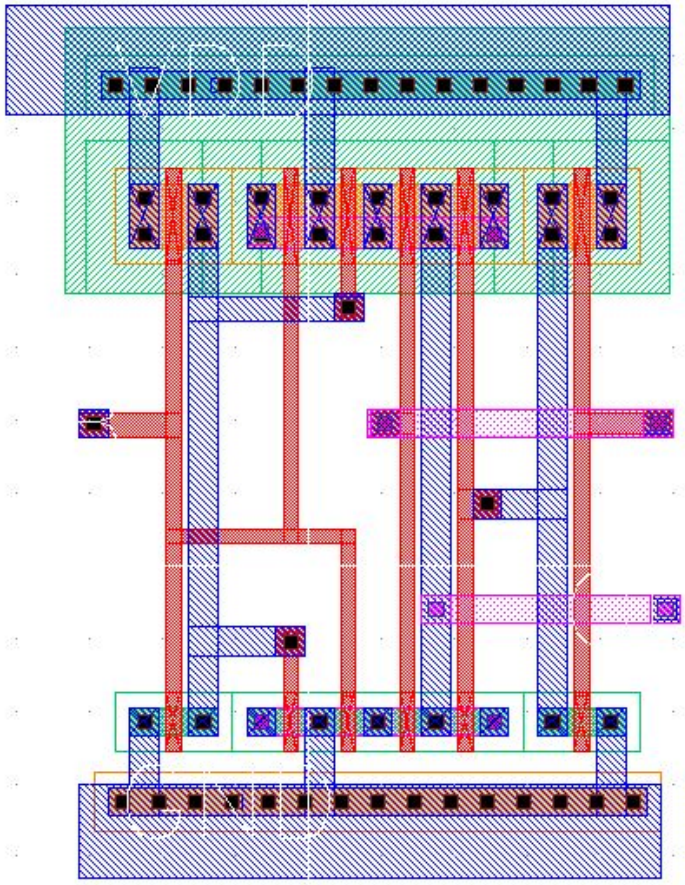

Fig.13 Layout for XOR

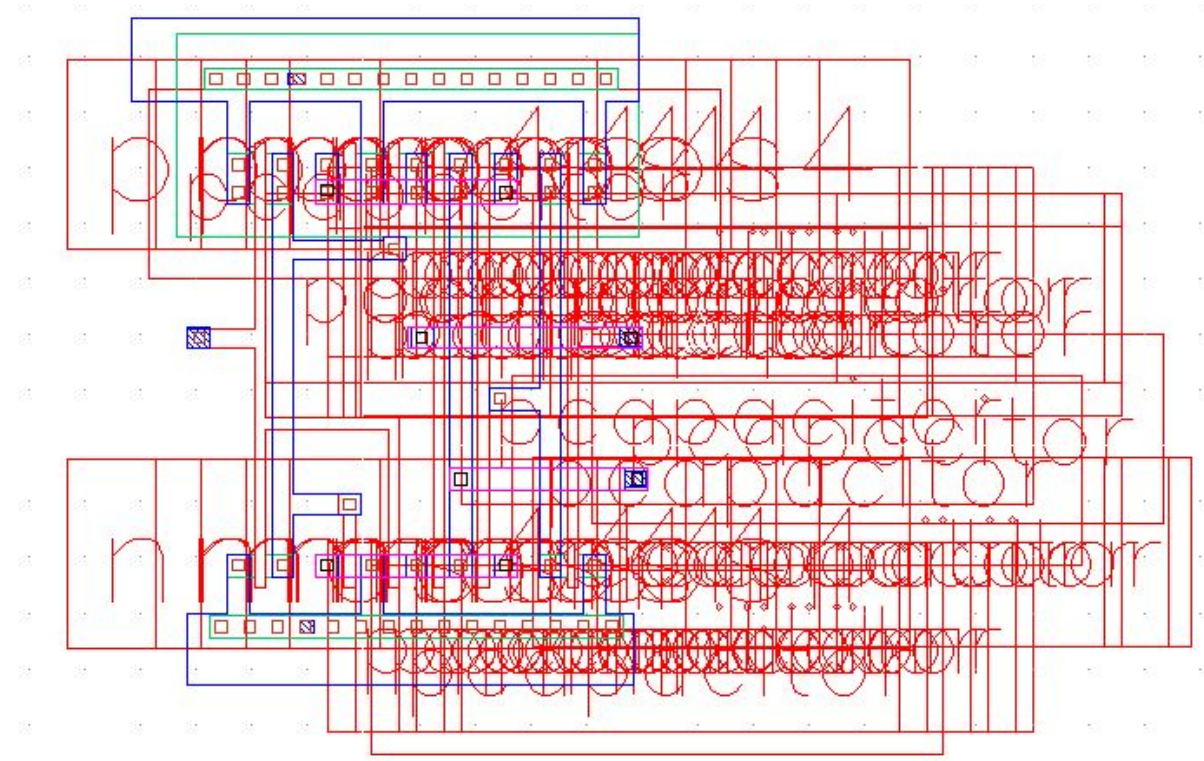

Fig.14 Extracted from XOR

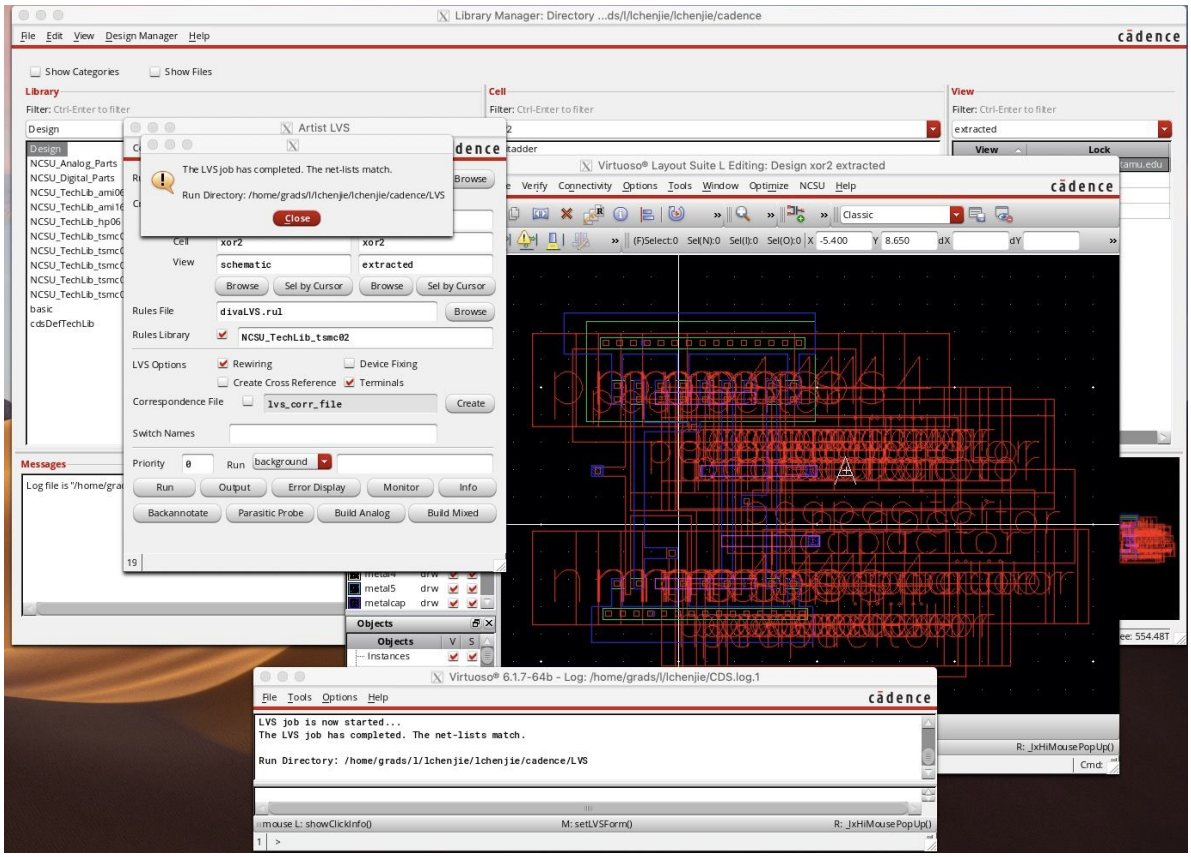

Fig.15 LVS result succeeds

Si.out for inverter:

@(#)$CDS: LVS version 6.1.7-64b 01/24/2017 19:46 (sjfhw310) $

Command line: /softwares/Linux/cadence/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir
/home/grads/l/lchenjie/lchenjie/cadence/LVS -l -s -t
/home/grads/l/lchenjie/lchenjie/cadence/LVS/layout
/home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

Net-list summary for
/home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic/netlist

count	
4	nets
4	terminals
1	pmos
1	nmos

Terminal correspondence points

N0	N2	GND
N3	N3	VDD
N2	N1	in
N1	N0	out

Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	2	2
total	2	2
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	4	4
total	4	4
	terminals	
un-matched	0	0
matched but different type	1	1
total	4	4

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal out's type in the schematic: output, in the layout: input

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal out's type in the layout: input, in the schematic: output

prunenet.out:

prunedev.out:

audit.out:

Si.out for NAND:

@(#)$CDS: LVS version 6.1.7-64b 01/24/2017 19:46 (sjfhw310) $

Command line: /softwares/Linux/cadence/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/l/lchenjie/lchenjie/cadence/LVS -l -s -t /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic/netlist

count	
6	nets
5	terminals
2	pmos
2	nmos

Terminal correspondence points

N3	N3	A
N2	N1	B
N1	N5	GND
N5	N0	VDD
N4	N2	out

Devices in the netlist but not in the rules:
pcapacitor
Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

layout schematic

	instances		
un-matched		0	0
rewired		0	0
size errors		0	0
pruned		0	0
active	4	4	
total	4	4	
	nets		
un-matched		0	0
merged		0	0
pruned		0	0
active	6	6	
total	6	6	
	terminals		
un-matched		0	0
matched but different type		0	0
total	5	5	

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Si.out for XOR:

@(#)$CDS: LVS version 6.1.7-64b 01/24/2017 19:46 (sjfhw310) $

Command line: /softwares/Linux/cadence/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/l/lchenjie/lchenjie/cadence/LVS -l -s -t /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout/netlist

count	
11	nets
5	terminals
6	pmos
6	nmos

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic/netlist

count	
11	nets
5	terminals
6	pmos
6	nmos

Terminal correspondence points

N9	N9	A
N8	N7	B
N6	N1	GND
N7	N6	OUT
N10	N8	VDD

Devices in the netlist but not in the rules:
    pcapacitor
Devices in the rules but not in the netlist:
    cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	

un-matched		0	0
rewired		0	0
size errors		0	0
pruned		0	0
active	12	12	
total	12	12	
	nets		
un-matched		0	0
merged		0	0
pruned		0	0
active	11	11	
total	11	11	
	terminals		
un-matched		0	0
matched but different type		0	0
total	5	5	

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:

prunenet.out:

prunedev.out:

audit.out: