ECEN714 Lab4 report
Chenjie Luo

1. 1-bit adder

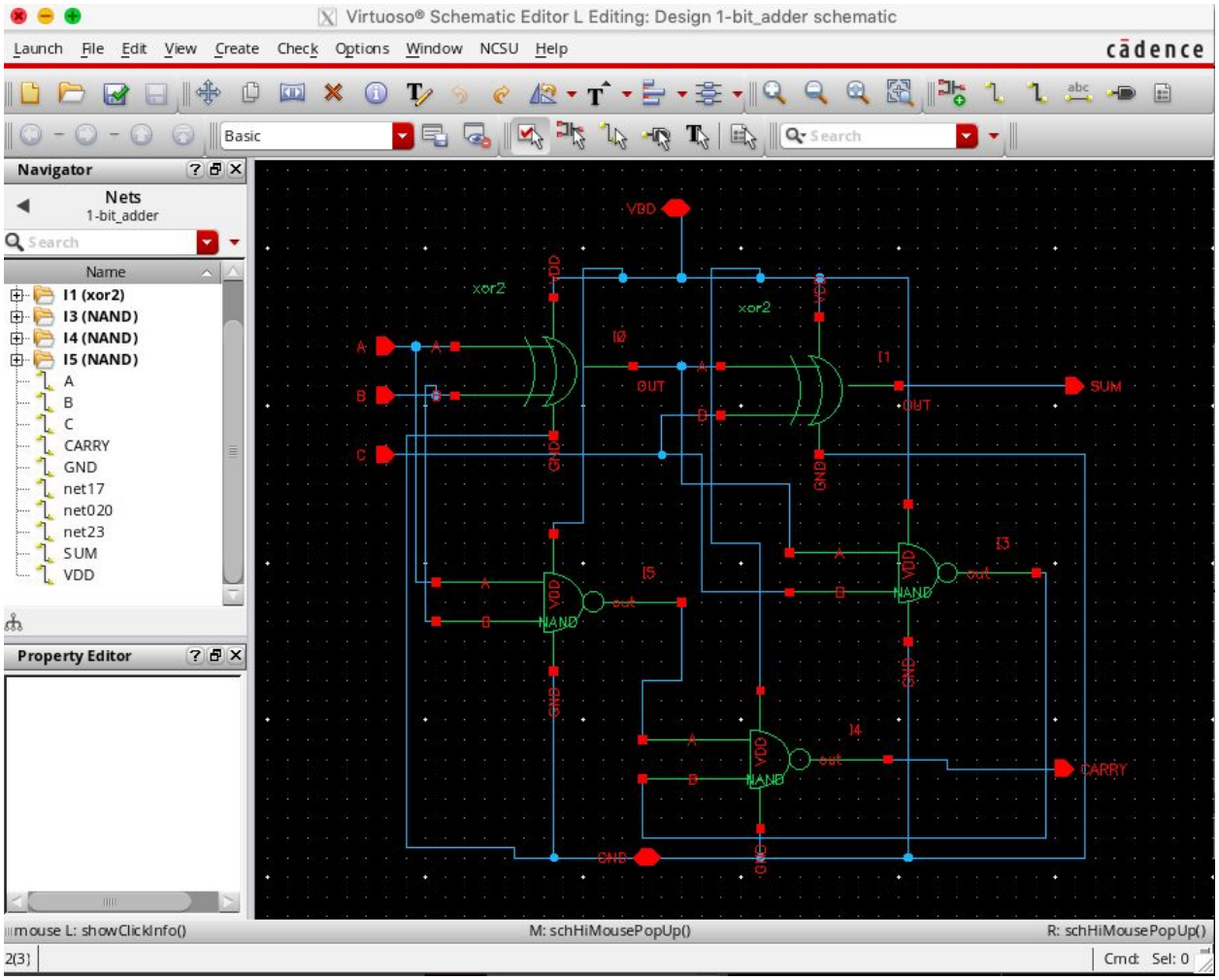


Fig.1 Schematics for 1 bit adder

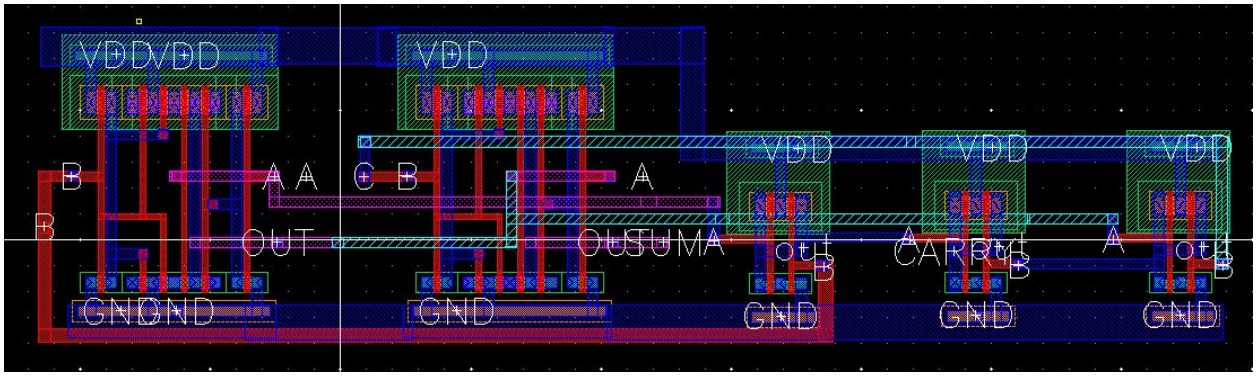


Fig.2 Layout of 1 bit adder

DRC output:

Running layout DRC analysis
Flat mode
Full checking.
DRC started.....Thu Feb 21 23:45:34 2019
completed ....Thu Feb 21 23:45:34 2019
CPU TIME = 00:00:00 TOTAL TIME = 00:00:00
********* Summary of rule violations for cell "1-bit_adder layout" *********
Total errors found: 0

LVS output:

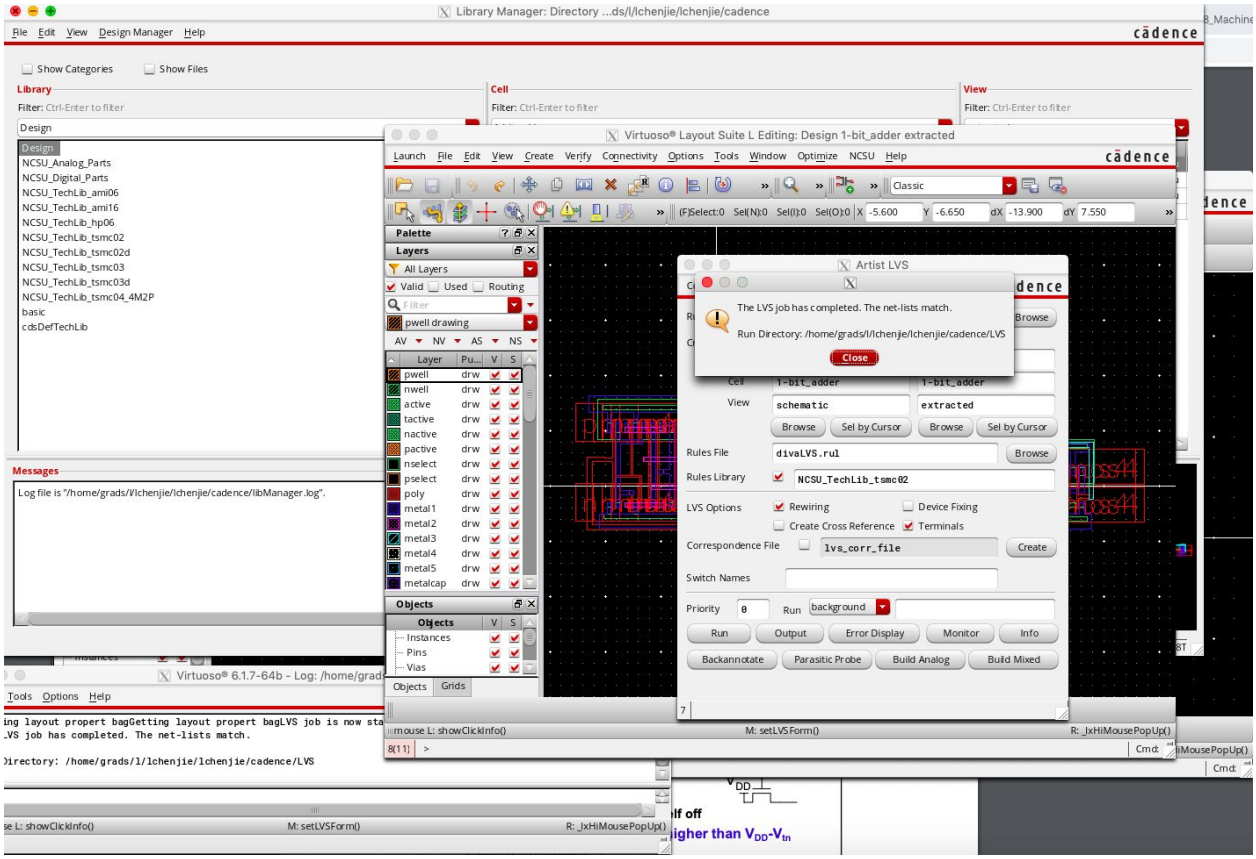


Fig.3 Screenshot of LVS check

Si.out of 1 bit adder:

Command line: /softwares/Linux/cadence/IC617/tools.lnx86/dfII/bin/64bit/LVS -dir /home/grads/l/lchenjie/lchenjie/cadence/LVS -l -s -t /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic
Like matching is enabled.
Net swapping is enabled.
Using terminal names as correspondence points.
Compiling Diva LVS rules...

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout/netlist

count	
25	nets
7	terminals
18	pmos
18	nmos

Net-list summary for /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic/netlist

count	
25	nets
7	terminals
18	pmos
18	nmos

Terminal correspondence points

N22	N9	A
N21	N6	B
N19	N4	C
N24	N2	CARRY
N18	N8	GND
N20	N0	SUM
N23	N7	VDD

Devices in the rules but not in the netlist:
cap nfet pfet nmos4 pmos4

The net-lists match.

	layout	schematic
	instances	
un-matched	0	0
rewired	0	0
size errors	0	0
pruned	0	0
active	36	36
total	36	36
	nets	
un-matched	0	0
merged	0	0
pruned	0	0
active	25	25
total	25	25
	terminals	
un-matched	0	0
matched but different type	1	1
total	7	7

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/schematic

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal C's type in the schematic: input, in the layout: inputOutput

prunenet.out:

prunedev.out:

audit.out:

Probe files from /home/grads/l/lchenjie/lchenjie/cadence/LVS/layout

devbad.out:

netbad.out:

mergenet.out:

termbad.out:
? Terminal C's type in the layout: inputOutput, in the schematic: input

prunenet.out:

prunedev.out:

audit.out:

2. Inverter

Rising delay: 264.7E-12s

Falling delay: 265.5E-12s

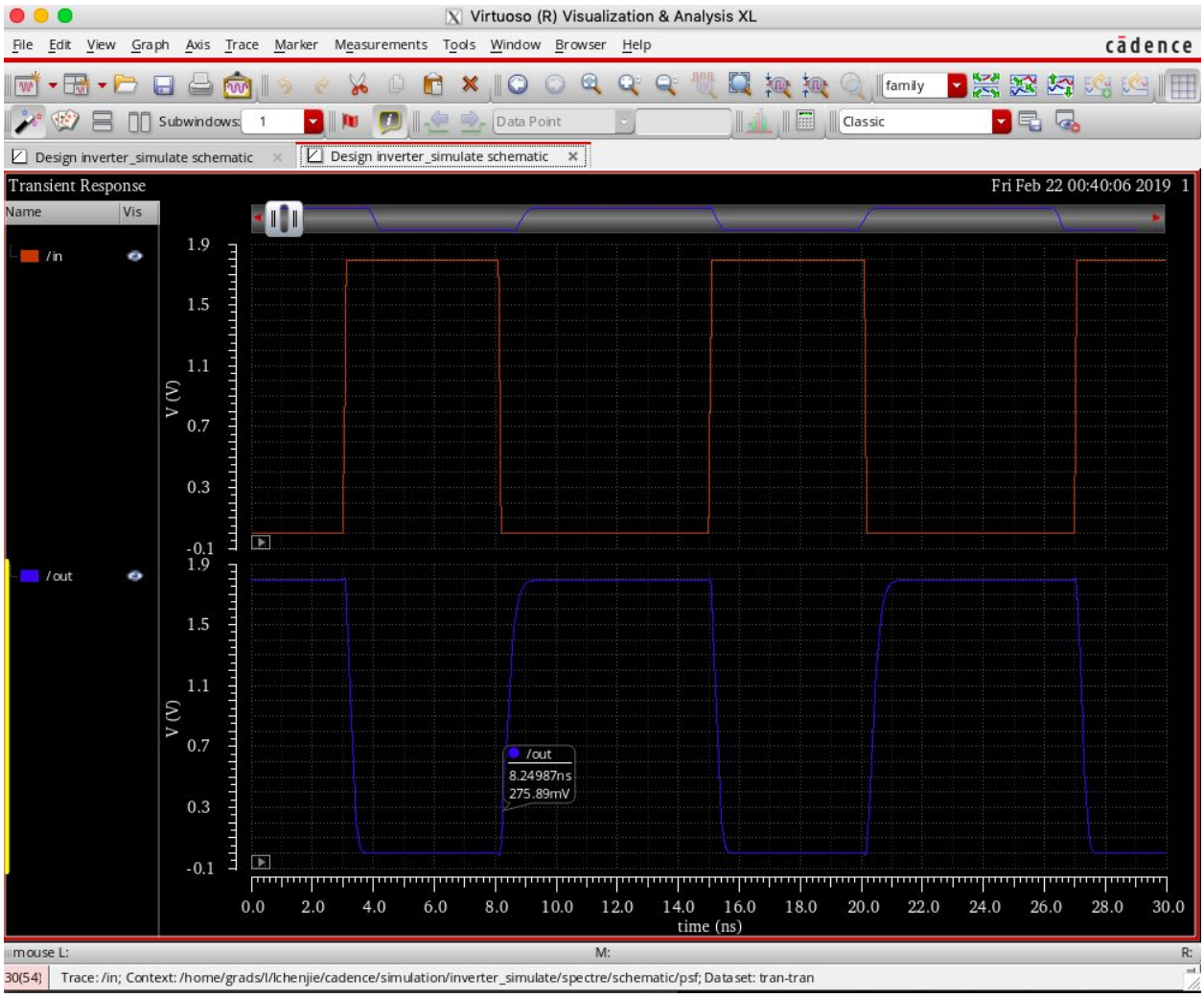


Fig.4 Inverter waveform

3. NAND

Rising delay: 310.1E-12s

Falling delay: 281.8E-12s

Error ratio = 10.01%

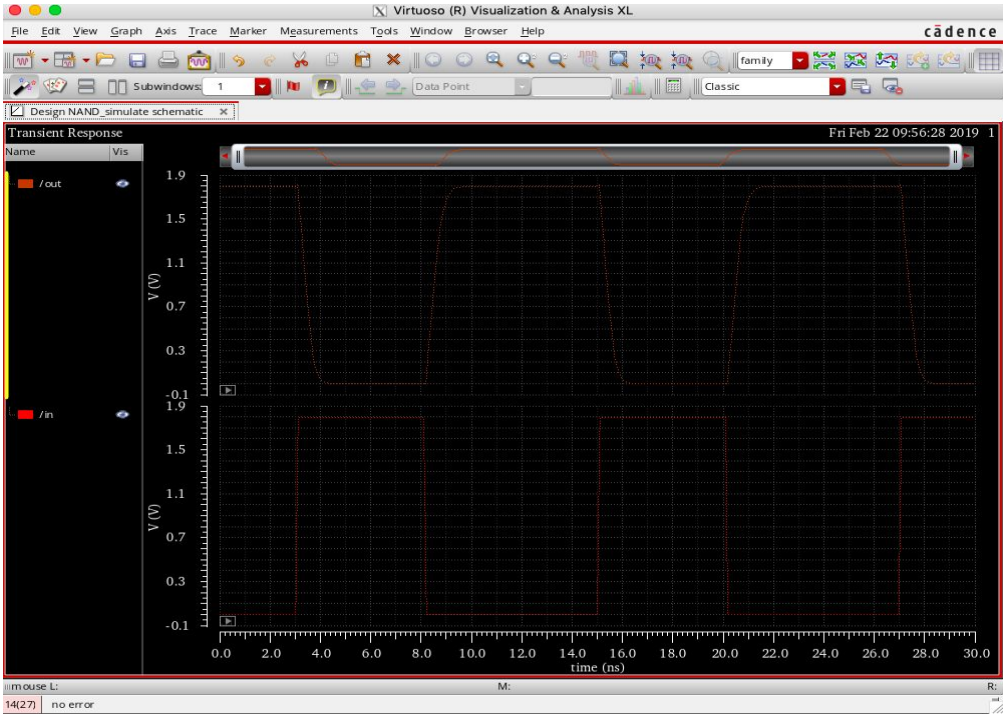


FIg.5 Waveform of NAND with 1 bit always on

4. XOR

Rising delay: 450.1E-12s Falling delay: 394.1E-12s

Error ratio = 14.1%

Power of VDC = 7.509E-6 W Power of Vpulse = 416.6E-9 W

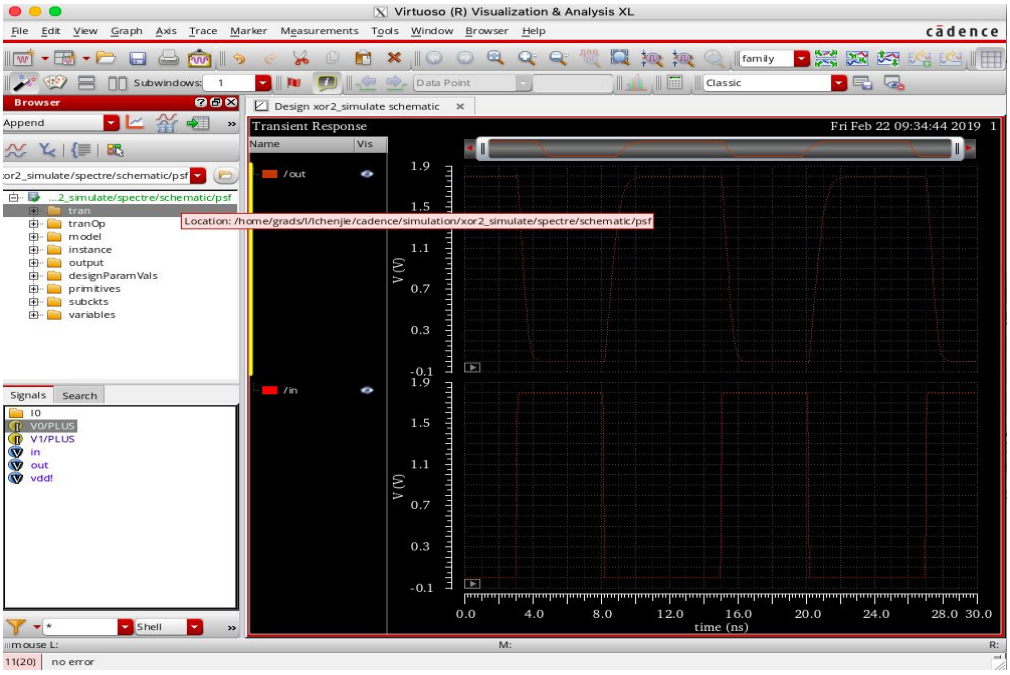


Fig. 5 Waveform of XOR with 1 bit always on

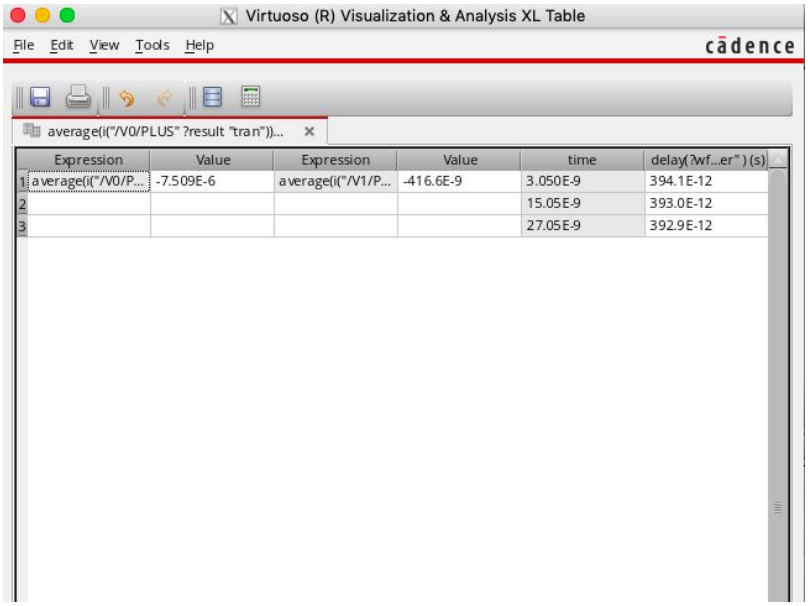
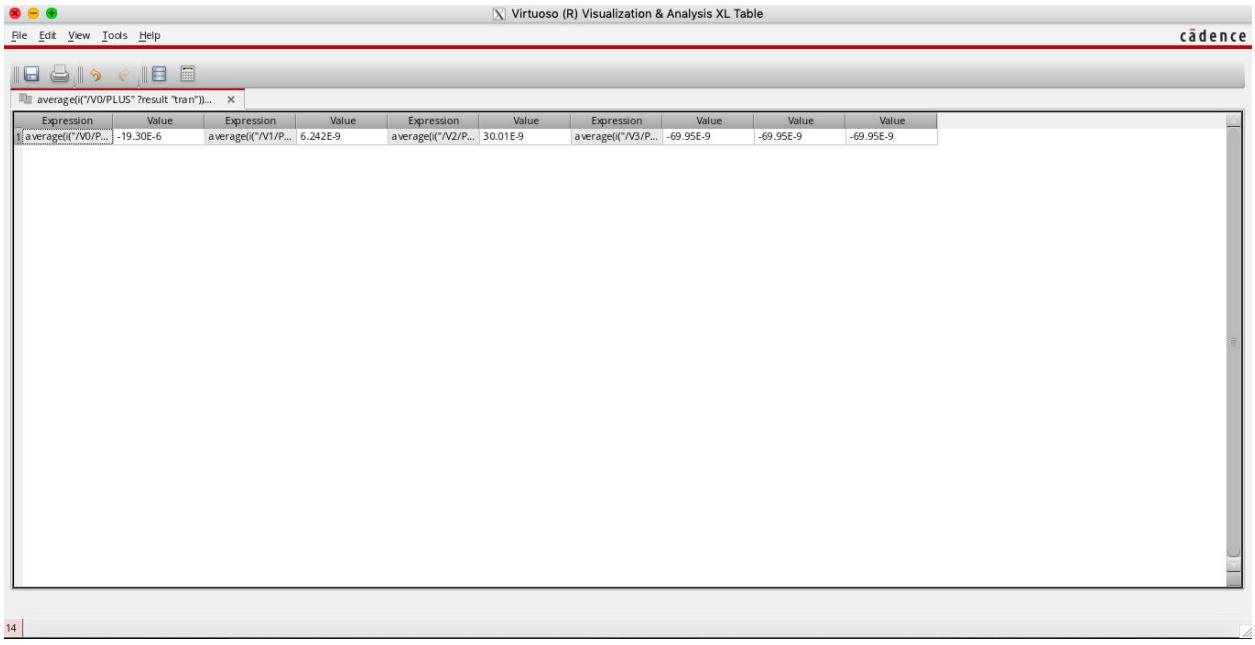


Fig.6 Delay and power dissipation output

5. 1 bit adder:

Power dissipation is attached as below:



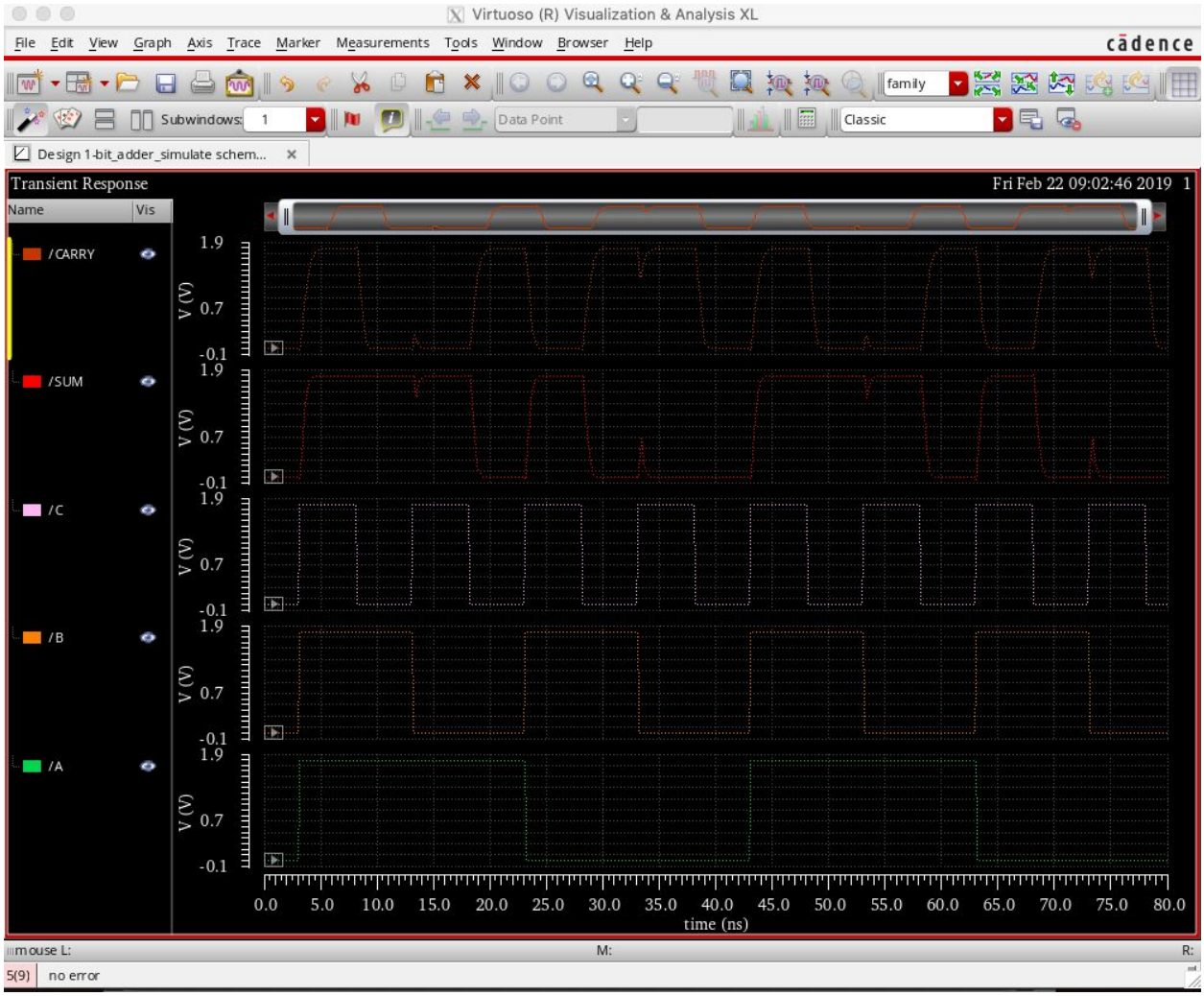
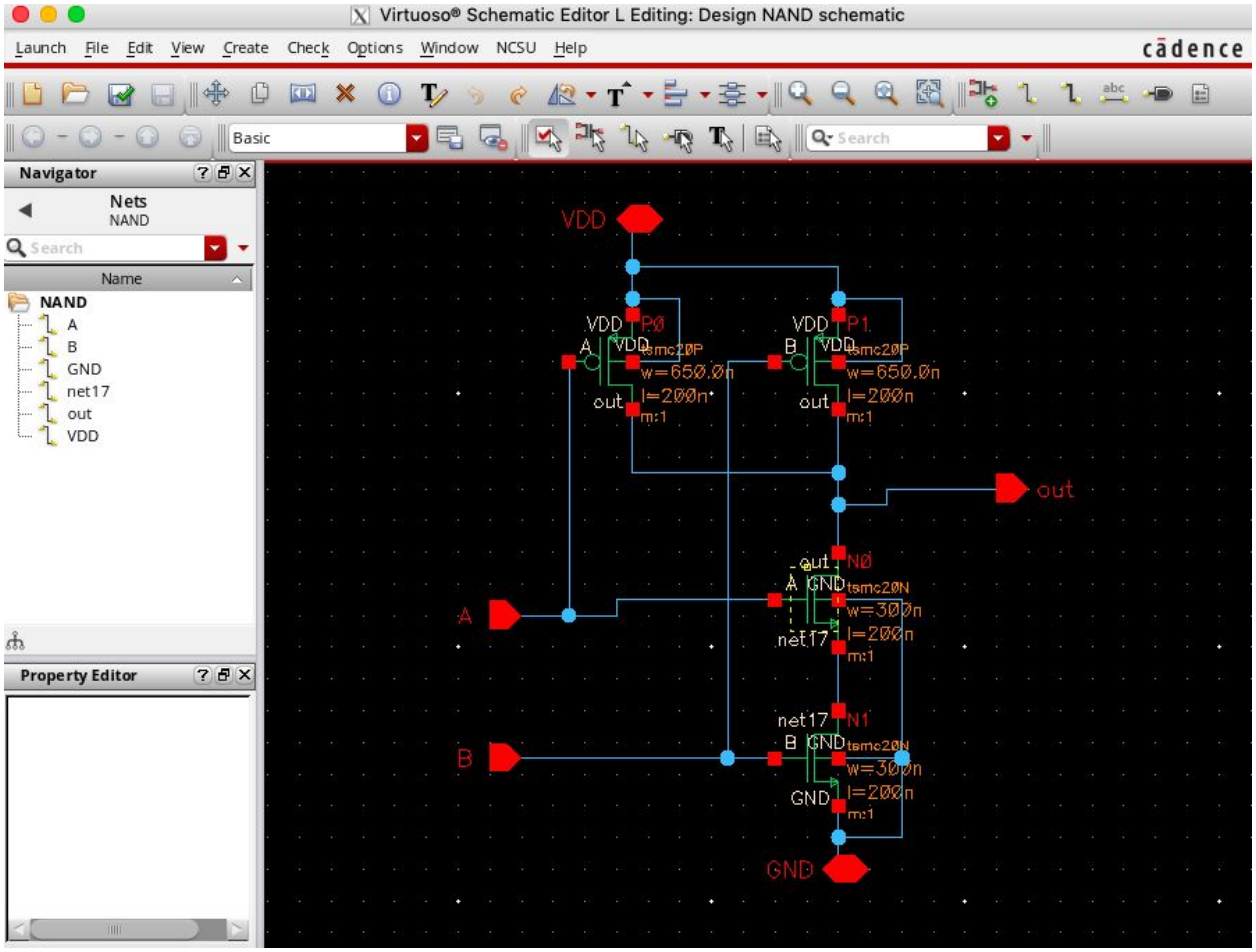


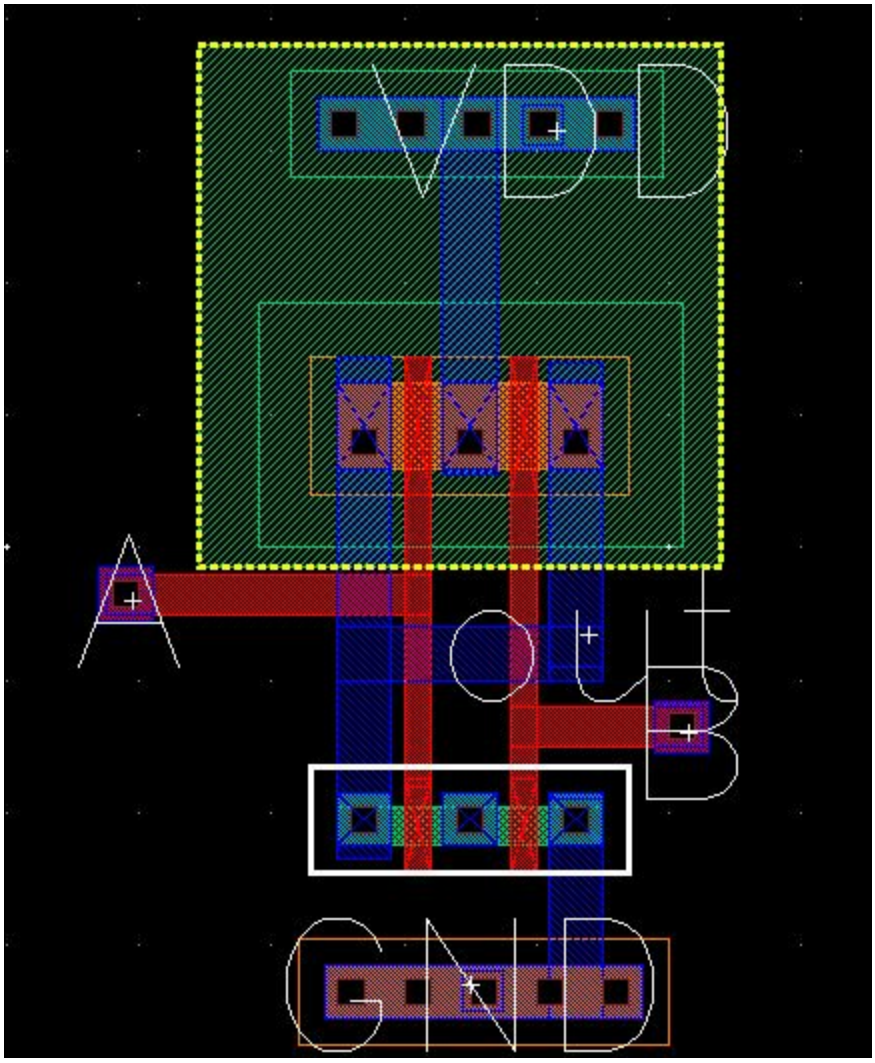
Fig.5 Waveforms of 1 bit adder

Update: During the lab I have asked TA Sara about the delay and I modified my cmos parameters and the error ratio now is within 10%. I have attached my updated output below. Thanks!

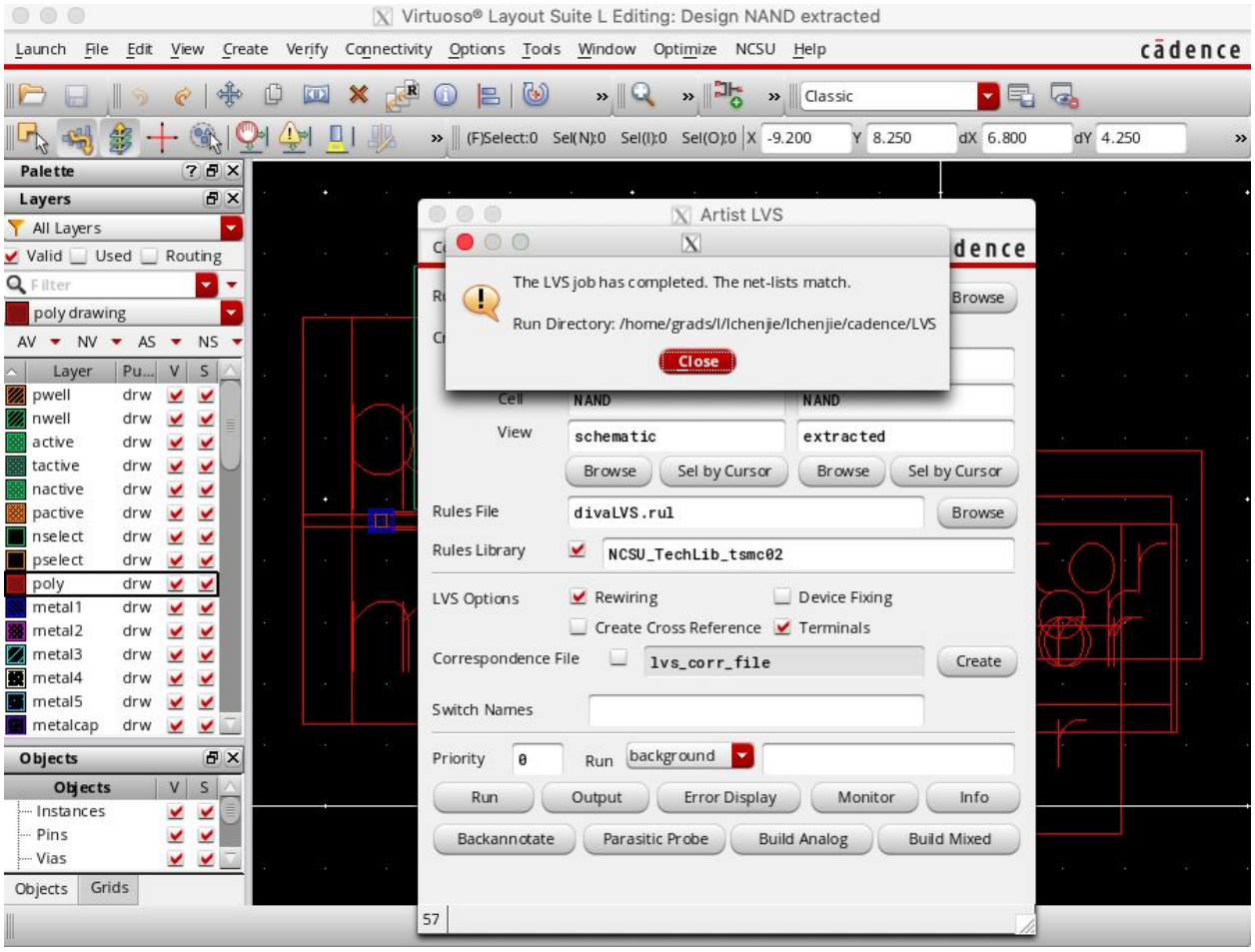
NAND:



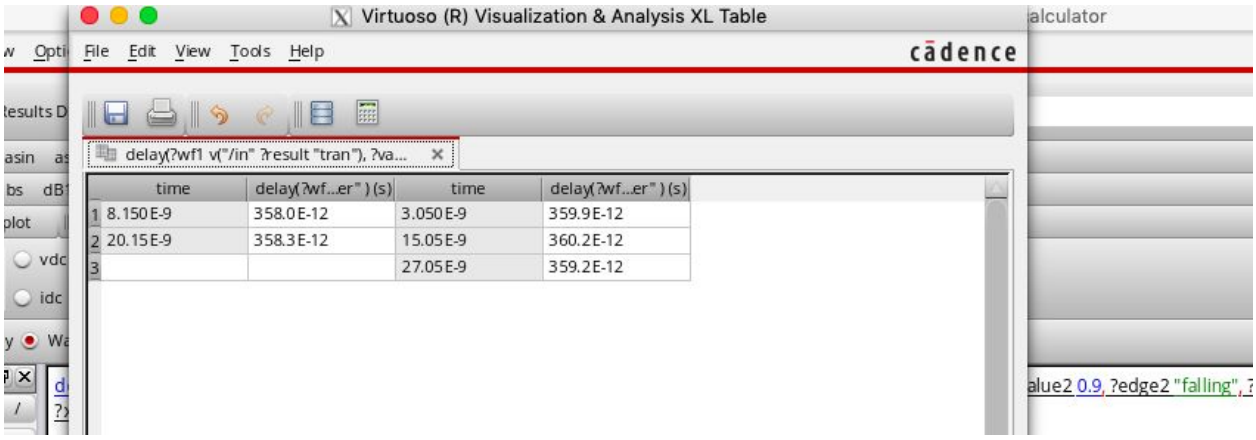
Updated Schematic of NAND



Updated Layout of NAND



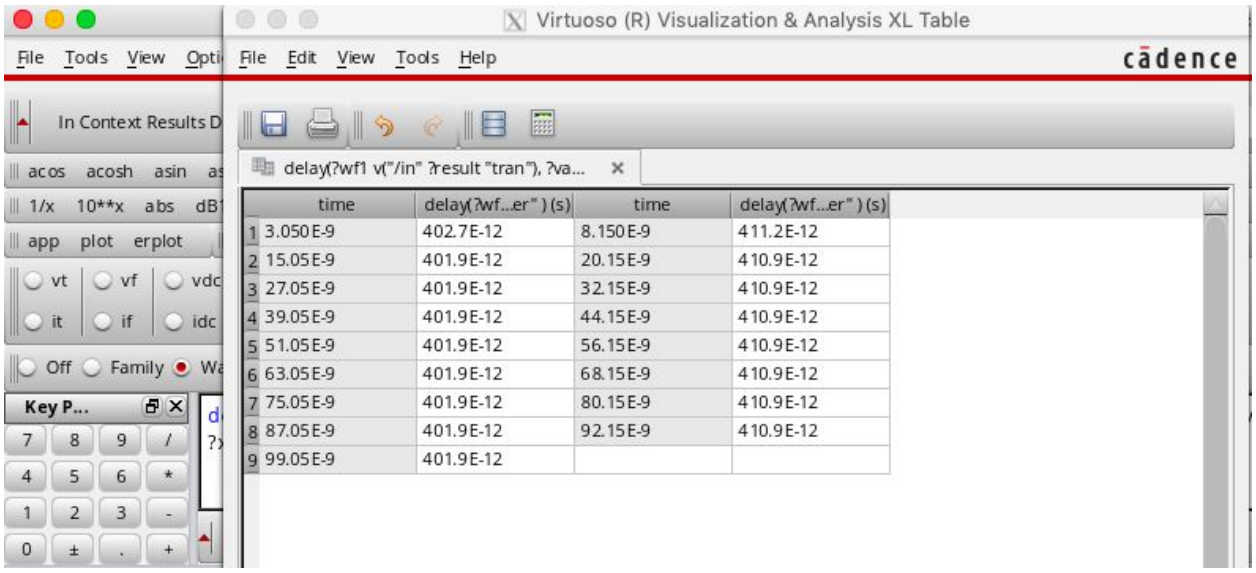
LVS output of updated NAND



Falling delay and Rising delay of Updated NAND simulate

Rising delay: 358.0E-12s
Falling delay: 360.2E-12s
Maximum error ratio = 0.725%

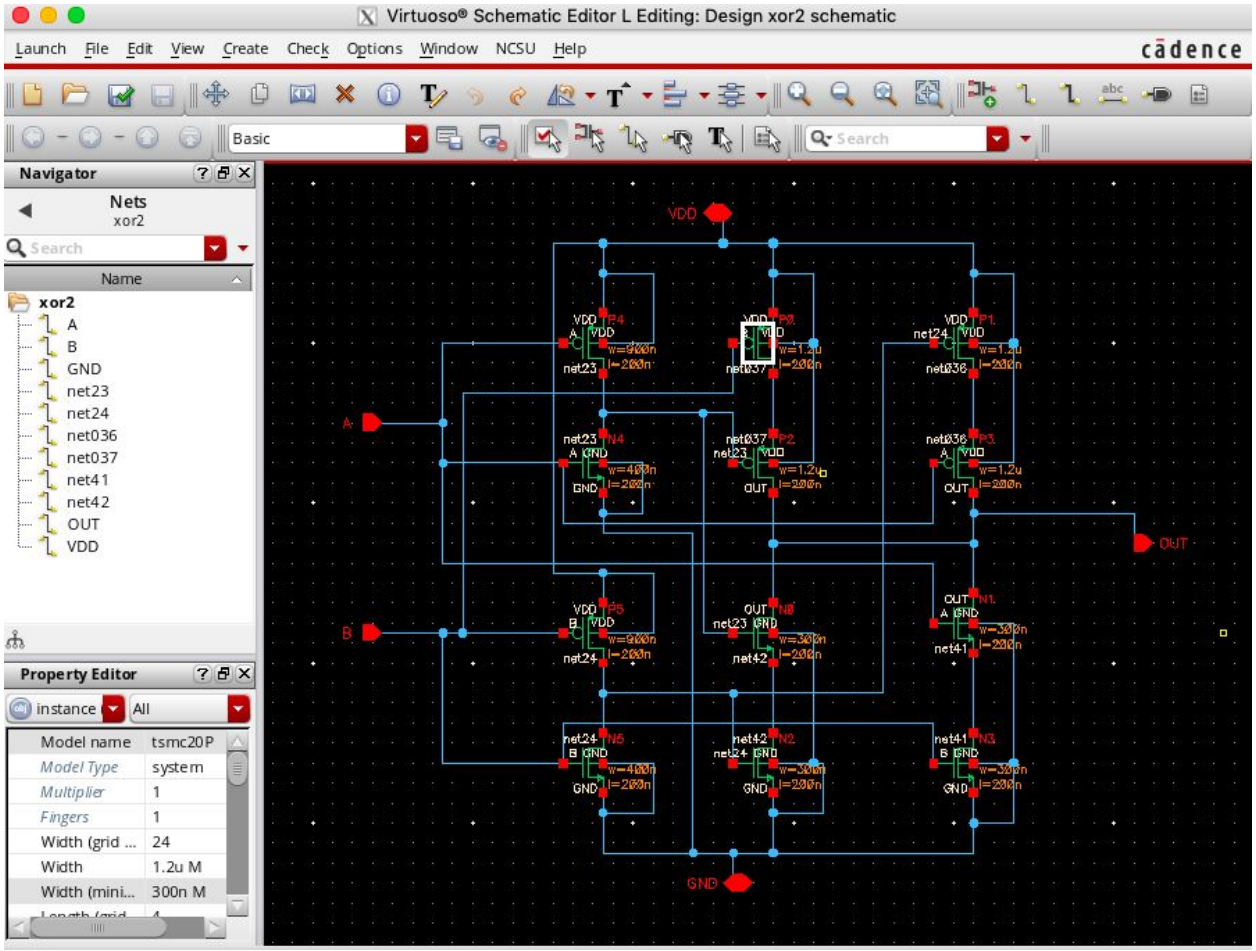
XOR:



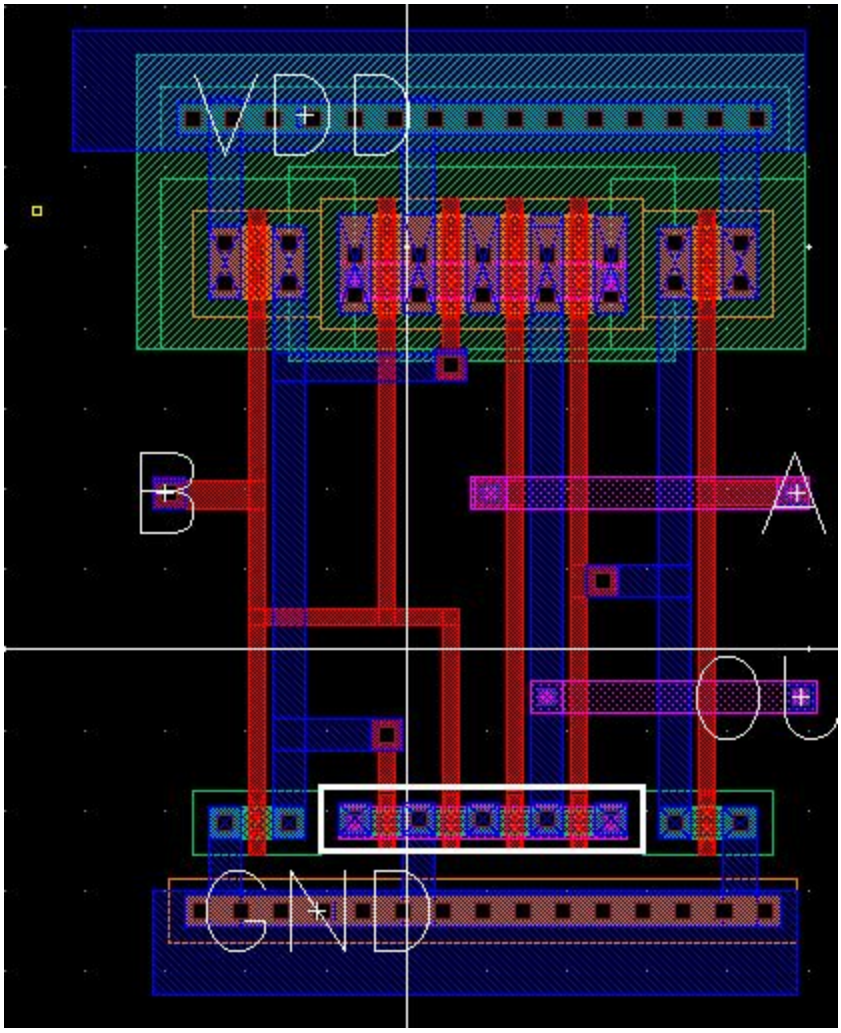
	time	delay(?wf...er") (s)	time	delay(?wf...er") (s)
1	3.050E-9	402.7E-12	8.150E-9	411.2E-12
2	15.05E-9	401.9E-12	20.15E-9	410.9E-12
3	27.05E-9	401.9E-12	32.15E-9	410.9E-12
4	39.05E-9	401.9E-12	44.15E-9	410.9E-12
5	51.05E-9	401.9E-12	56.15E-9	410.9E-12
6	63.05E-9	401.9E-12	68.15E-9	410.9E-12
7	75.05E-9	401.9E-12	80.15E-9	410.9E-12
8	87.05E-9	401.9E-12	92.15E-9	410.9E-12
9	99.05E-9	401.9E-12		

Falling delay and rising delay of XOR

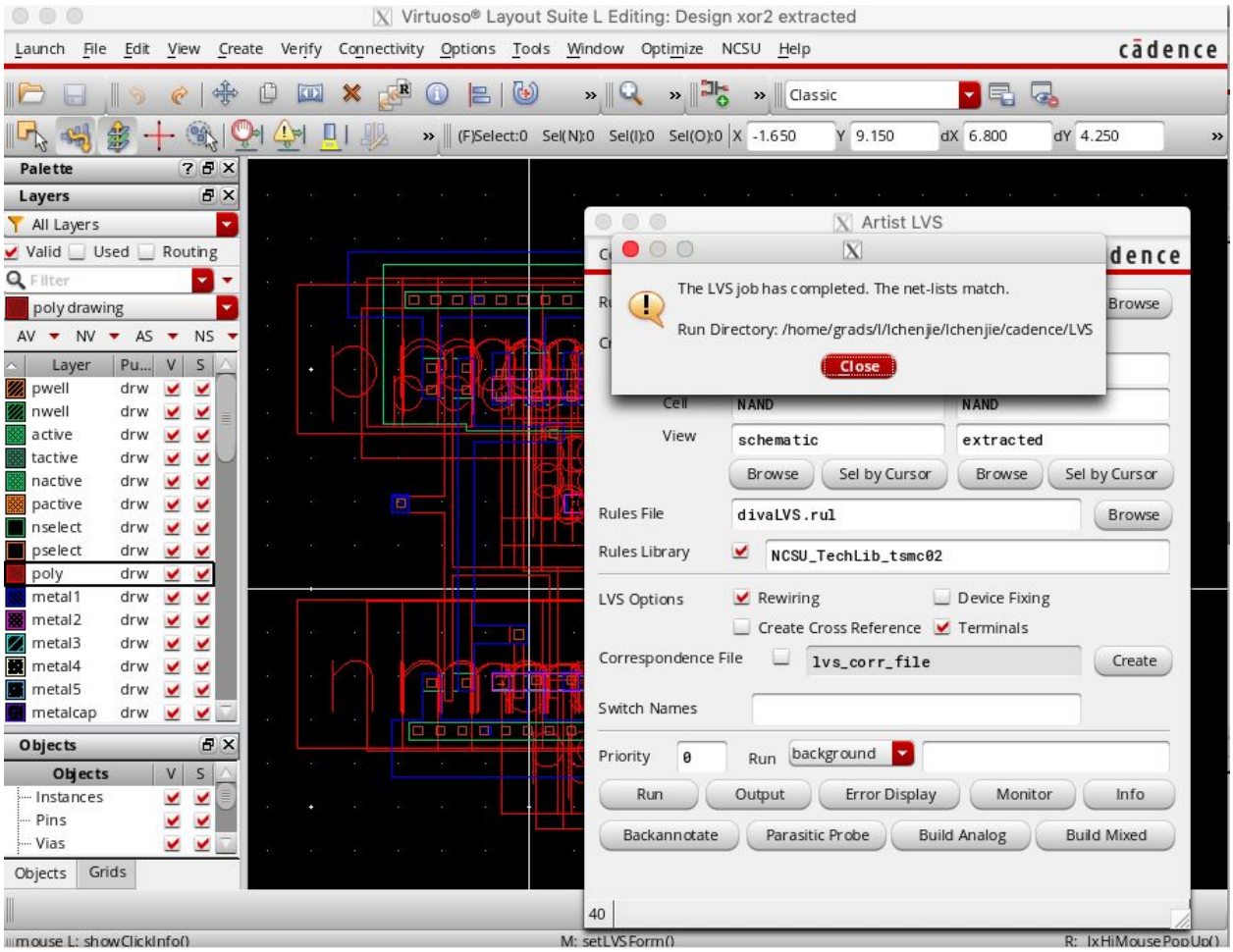
Rising delay: 410.9E-12s
Falling delay: 401.9E-12s
Maximum Error ratio = 2.24%



Updated Schematic for XOR



Updated Layout of XOR



LVS output of updated XOR