# Quantum Instruction Set Design for Performance

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A quantum instruction set is where quantum hardware and software meet. We develop characterization and compilation techniques for non-Clifford gates to accurately evaluate its designs. Applying these techniques to our fluxonium processor, we show that replacing the iSWAP gate by its square root SQiSW leads to a significant performance boost at almost no cost. More precisely, on SQiSW we measure a gate fidelity of up to 99.72% and averaging at 99.31%, and realize Haar random two-qubit gates with an average fidelity of 96.38%. This is an average error reduction of 41% for the former and a 50% reduction for the latter compared to using iSWAP on the same processor.

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A quantum instruction set is the interface that quantum hardware vendors provide to software. This has a subtle difference from a native gate set although they are often used interchangeably. A native gate set contains quantum operations that are physically realizable on a quantum computing platform. In contrast, a quantum instruction set is a carefully chosen set of gates with consideration for cost or performance of the processor. Although one can always include more quantum gates to an instruction set to more efficiently implement algorithms, there are additional considerations. First of all, the added instruction must be of sufficient accuracy. In addition, since we need to calibrate each instruction, it is preferable to limit the number of gates [1]. This is reminiscent of the debate between RISC (Reduced Instruction Set Computer) and CISC (Complex Instruction Set Computer) in classical computing [2].

Any universal quantum instruction set must contain at least one entangling two-qubit gate. Given that errors of single-qubit gates are usually much less than that of two-qubit gates, the design of a quantum instruction set is mainly about the selection of two-qubit gates. However, evaluating quantum instruction sets with different two-qubit gates has the following challenges. (1) The set of native two-qubit gates and how accurately each gate can be realized is highly dependent on hardware implementation. Therefore, it is difficult to make a direct comparison between quantum instruction sets at a software level; (2) It is a nontrivial task to faithfully characterize a general quantum gate. In particular, the conventional approach of using Clifford-based randomized benchmarking (RB) [3] cannot be used to benchmark non-Clifford gates. (3) The compilation of quantum algorithms into quantum instructions is only extensively studied for CNOT [4–6]. Although there are studies of compiling into general gates [1,7], these approaches use heuristics and so cannot give reliable data for designing an instruction set.

With these challenges in mind, in this Letter we reevaluate the design of the mainstream quantum instruction set for superconducting circuits that is based on CNOT, iSWAP, or gates that differ from either only by single-qubit gates [8]. Given all the focus on maximizing the fidelities of these two specific types of gates [9,10], it is worthwhile to critically analyze these particular choices of quantum instruction sets. In particular, we consider the instruction set with iSWAP and single-qubit gates. We numerically compute and experimentally demonstrate that for a quantum processor with such an instruction set, designing an instruction by replacing iSWAP with its matrix square root SQiSW can both reduce the gate error and improve compilation capabilities substantially. This new design can therefore significantly improve the quantum instruction set.

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More specifically, the gate

$$\mathrm{SQiSW} \equiv \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & \frac{i}{\sqrt{2}} & 0 \\ 0 & \frac{i}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix},$$

is in the iSWAP family and has been proposed and experimentally realized in earlier works [11–18]. The most common technique to realize iSWAP is to bring two transversally coupled qubits into resonance, and SQiSW is realized by halving the gate time for iSWAP. Thus, SQiSW is expected to be less susceptible to errors from decoherence and stray interactions. Despite hints of promise, few works have systematically studied the SQiSW from a holistic perspective, which we aim to accomplish in this Letter. In particular, we establish its control accuracy and compilation efficiency as follows. (i) Control accuracy: Taking into account decoherence, stray coupling between qubits, and instrumental limitations on experimental control parameters, we conduct a numerical simulation with experimentally achievable circuit parameters and decoherence times and estimate that we can realize SQiSW with an error of about $5 \times 10^{-4}$, which is only half of the error of iSWAP on the same system. (ii) Compilation efficiency: We give an analytical scheme to compile an arbitrary two-qubit gate with the optimal number of SQiSW gates and arbitrary single qubit gates. Moreover, we prove that 79% of two-qubit gates (under the Haar measure) can be generated with only two uses of the SQiSW gate, whereas the rest can be generated with three uses. As a result, using SQiSW to compile two-qubit Haar random or random Clifford gates leads to error reductions of about 63% or 35% compared to using iSWAP [19], assuming that the gate error of SQiSW is half of that of iSWAP and that single-qubit gate errors are negligible.

Furthermore, we experimentally demonstrate these advantages of SQiSW on a superconducting quantum processor consisting of two capacitively coupled fluxonium qubits. In order to characterize SQiSW, we develop a variant of interleaved randomized benchmarking (iRB) called interleaved fully randomized benchmarking (iFRB). iFRB can be used to characterize the fidelity of any fixed gate whenever an efficient implementation for arbitrary gates is available, which we establish through our explicit compilation scheme using SQiSW. We experimentally benchmark SQiSW using iFRB and compare the results to iSWAP in the same experimental run. We observe a SQiSW fidelity of up to 99.72% with average 99.31%. The latter is a 41% error reduction compared to the corresponding iSWAP fidelity. We also realize Haar random two-qubit gates using SQiSW and measure an average fidelity of 96.38%, the error reduction being 50% compared to that of iSWAP. This additional reduction demonstrates the superior compilation capabilities of SQiSW.

*The SQiSW gate scheme.*—Two-qubit gates in the iSWAP family can be implemented by turning on a transverse coupling between qubits for a given time $t$ [9]. In the weak coupling limit where the coupling energy is much smaller than the qubit energy, the interaction Hamiltonian takes the well-known form of the $XY$ spin interaction $g(\sigma_{XX} + \sigma_{YY})$ under the rotating wave approximation (RWA), where $g$ is the $XY$ coupling strength between the two qubits. The iSWAP family gate can be implemented by tuning the interaction time $t$: $t = \pi/g$ for $\mathrm{SQiSW}^\dagger$, $t = 2\pi/g$ for $\mathrm{iSWAP}^\dagger$, and $t = -\pi/g$ for SQiSW when $g < 0$. In the subsequent sections we consider the SQiSW gate even though $\mathrm{SQiSW}^\dagger$ is more common in physical implementations, as they are locally equivalent and therefore share all the compilation properties mentioned in the rest of the Letter.

In realistic systems, this gate scheme is complicated by possible stray longitudinal coupling ($ZZ$ interaction), inaccurate flux tuning (to bring qubits into resonance) and decoherence [20–22]. Since SQiSW takes roughly half of the gate time of iSWAP, the corresponding contributions from the major error sources are approximately halved as well. A more detailed analysis of the error contributions, together with numerical simulations, can be found in Sec. III of the Supplemental Material [23]. Considering recent progress on fluxonium fabrication [43] and the precision of the arbitrary wave generator, according to our simulation we can expect an infidelity as small as $5 \times 10^{-4}$ for the SQiSW gate.

Since $\mathrm{SQiSW}^2 = \mathrm{iSWAP}$, replacing iSWAP in a quantum instruction set with SQiSW in principle results in negligible fidelity loss, although possibly nonzero due to imprecise control on real devices. Assuming this, we next show that replacing iSWAP with SQiSW yields strict performance gain by proving that SQiSW is superior at certain compilation tasks.

*Compilation capabilities of SQiSW.*—We study how effective SQiSW can compile quantum circuits, in particular arbitrary two-qubit gates, and compare this with those of other widely used two-qubit gates. Assuming single-qubit gates are implemented perfectly, we use the two-qubit gate count as a quantitative measure of the circuit complexity. We give a more detailed analysis of the ability of SQiSW to compile multiqubit quantum circuits, such as $W$ state preparation, in Sec. II of the Supplemental Material [23].

Every two-qubit gate $U$ is equivalent to a gate of the form $\exp\{i(x \cdot \sigma_{XX} + y \cdot \sigma_{YY} + z \cdot \sigma_{ZZ})\}$ up to single-qubit gates, where $(x, y, z)$ lies in the *Weyl chamber* [45,46]

$$W \equiv \left\{ \frac{\pi}{4} \geq x \geq y \geq |z| \text{ and } z \geq 0 \text{ if } x = \frac{\pi}{4} \right\} \subset \mathbb{R}^3.$$

The vector $(x, y, z)$ associated to $U$ is called the *interaction coefficients*.

We prove the following result regarding the compilation capabilities of SQiSW: A two-qubit gate can be realized with two SQiSW gates and single-qubit gates if and only if its interaction coefficients $(x, y, z)$ lie in the region $S_2 \coloneqq \{(x, y, z) \in W || z| \leq x - y\}$. Moreover, all two-qubit gates outside of $S_2$ can be realized with one SQiSW gate and one gate from $S_2$, thus requiring at most three SQiSW gates.

The above result allows the decomposition of an arbitrary two-qubit gate into an optimal number of SQiSW gates. We can, in principle, find the required single-qubit gates using numerical optimization. To realize efficient compilation, we provide an analytical solution that directly computes the single-qubit gates. Section I of the Supplemental Material shows the proof of the above result and the analytical compilation scheme [23].

We also compare the ability of SQiSW to compile two-qubit gates with that of other two-qubit gates. The region $S_2$ contains all two-qubit Clifford gates not locally equivalent to SWAP, as well as 79% of all two-qubit gates under the Haar measure. The average two-qubit gate count required to generate Haar random two-qubit gates $\mathcal{L}_H$ and random Clifford gates $\mathcal{L}_C$ are summarized in Table I. It can be seen that, although only being half of the iSWAP gate, the SQiSW gate is actually much more efficient in compiling Haar random two-qubit gates than the iSWAP gate, while not being much worse in terms of compiling random Clifford gates. If we assume that SQiSW has half the error of that of iSWAP, by using SQiSW we expect a 63% reduction in the average infidelity for Haar random gates and a 35% reduction for random Clifford gates. Note that other two-qubit gates have been proposed in the literature, such as the $B$ gate [49] and the $\mathrm{iSWAP}^{\frac{3}{4}}$ gate [16]. However, the former does not have a high-fidelity experimental gate scheme while the latter does not have an explicit compilation scheme. SQiSW is the first gate to our knowledge that outperforms iSWAP and CNOT in compilation abilities *while still admitting a high-fidelity gate scheme and an explicit compilation scheme.* This reduction of error in two-qubit gate compilation leads to an appreciable increase in quantum volume under multiple circuit topologies and noise levels, as indicated by numerical experiments conducted in Sec. VI of the Supplemental Material [23].

*Experiment.*—We experimentally realize SQiSW and iSWAP on a fluxonium quantum processor. The experiment setup and quantum processor used in this experiment are the same as that of [50], but this experiment is performed in a different cool-down cycle. For individual single-qubit gates, the two qubits $Q_A$ and $Q_B$ are fixed at their sweet spots corresponding to 1.09 and 1.33 GHz, respectively, and a resonant microwave pulse generated by an arbitrary waveform generator (AWG) is applied to each qubit through their own charge line.

TABLE I. Comparison between SQiSW and conventional CNOT and iSWAP in terms of compiling Haar random two-qubit gates and random Clifford gates.

| | SQiSW | CNOT [19] | iSWAP [19] |
|---|---|---|---|
| $\mathcal{L}_H$ | 2.21 | 3 | 3 |
| $\mathcal{L}_C$ | 1.95 | 1.5 | 1.5 |

The two fluxonium qubits in our processor are capacitively coupled. To realize an iSWAP-like gate, we modulate the external flux of $Q_A$ to bring it in resonance with $Q_B$. The flux modulation pulse has a simple error-function shape and is also generated by an AWG and applied to $Q_A$ through its individual flux line. We use the same method as in Ref. [50] to calibrate the flux amplitude $\Phi_{\mathrm{amp}}$ that brings the two qubits in resonance. With a coupling strength of $g/2\pi \approx 11.2$ MHz, the gate times of iSWAP and SQiSW are 48.5 and 24.6 ns, respectively. The detailed calibration of the SQiSW gate is summarized in Sec. IV of the Supplemental Material [23].

We apply a variant of *interleaved randomized benchmarking* (iRB) [51] to characterize the fidelity of SQiSW and compare it with iSWAP. The iRB protocol characterizes the fidelity of a particular Clifford *target* gate by the

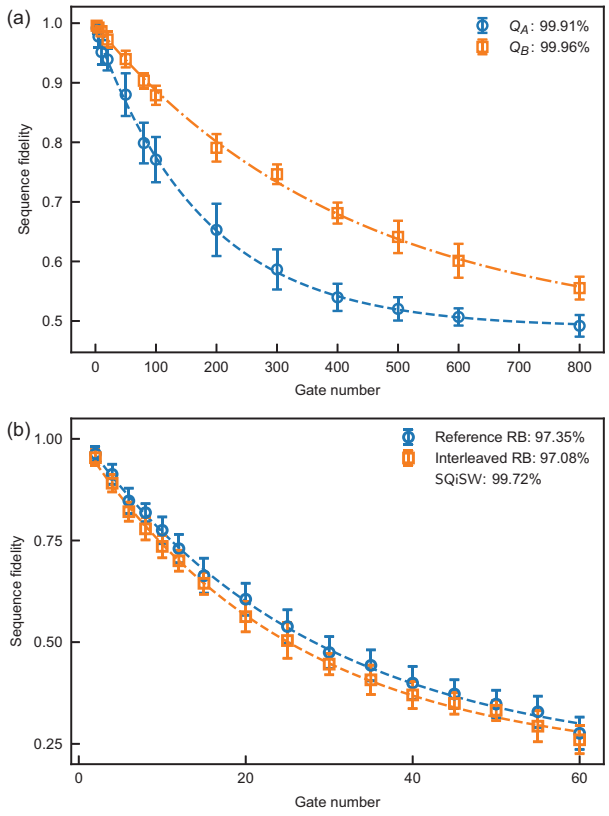


FIG. 1. (a) Simultaneous single-qubit FRB. The legend presents the average fidelity of a single microwave pulse. (b) Sequence fidelity of FRB and iFRB for SQiSW for the run with the highest fidelity. Each data point is averaged from 20 random sequences.

difference between the fidelity of a random Clifford gate, and a random Clifford gate appended by the target gate, both through the standard RB protocol [3]. To extend the applicability of iRB to non-Clifford target gates, in our experiments we choose the random gates from the Haar distribution on all two-qubit rotations SU(4). We call randomized benchmarking based on the whole (special) unitary group *fully randomized benchmarking* (FRB), and the corresponding interleaved version *interleaved fully randomized benchmarking* (iFRB). FRB and iFRB are applicable for SQiSW because we have an explicit compilation scheme and the required gates are all realized with high fidelities. FRB was first proposed in [52]; our Letter combines this idea with interleaved randomized benchmarking in order to characterize SQiSW, a non-Clifford gate.

In order to compile arbitrary two-qubit gates, we first need to compile arbitrary single-qubit gates. To do this, we employ the results in [53] to compile an arbitrary single-qubit gate using 3 phase-shifted microwave pulses (PMW-3). In Fig. 1(a), we show the results of simultaneous single-qubit FRB using the PMW-3 scheme. The extracted average fidelity of a single microwave pulse on $Q_A$ ($Q_B$) is 99.91% (99.96%). Note that since an arbitrary single-qubit gate is composed of three pulses, the infidelity per pulse is defined as a third of the infidelity per gate. This in particular demonstrates that the PMW-3 scheme can achieve state-of-the-art fidelities. Each microwave pulse is 10 ns long and is calibrated using known techniques developed, for example, in [54–56] and detailed in [50].

We run multiple FRB and iFRB experiments for SQiSW and iSWAP and compare the results in Fig. 2. The gate fidelities are obtained by running FRB and iFRB in an alternating fashion and computing a simple function of the measured decay rates. See Sec. V of the Supplemental Material for details [23]. We show the sequence fidelity

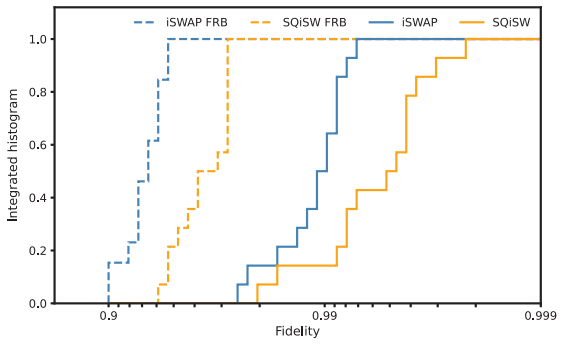


FIG. 2. Cumulative histogram of two-qubit FRB fidelities using iSWAP and SQiSW, in addition to the respective gate fidelities from 14 experiments. The gate fidelities are inferred using the corresponding iFRB experiments. Although we measure a SQiSW iFRB of 99.80% in one of the runs, a closer look into the data reveals a poor fitting due to highly fluctuating data. We include this data point here for completeness, but do not report the corresponding fidelity value as our highest.

TABLE II. Average values and standard deviations of different benchmarking metrics for SQiSW and iSWAP over 14 experiments. FRB is the fidelity of arbitrary two-qubit gates, while the target gate fidelities are inferred using the corresponding iFRB experiments. For iSWAP we also give the fidelity inferred using RB and iRB. In the last column we give the corresponding infidelities to make the error reductions more transparent.

| | | Fidelity | Infidelity |
|---|---|---|---|
| SQiSW | Gate | $99.31 \pm 0.50\%$ | $6.851 \times 10^{-3}$ |
| | FRB | $96.38 \pm 0.98\%$ | $3.615 \times 10^{-2}$ |
| iSWAP | Gate | $98.84 \pm 0.51\%$ | $11.63 \times 10^{-3}$ |
| | Gate (RB + iRB) | $98.88 \pm 0.44\%$ | $11.15 \times 10^{-3}$ |
| | FRB | $92.74 \pm 2.17\%$ | $7.265 \times 10^{-2}$ |

exponential decays for the highest measured SQiSW fidelity in Fig. 1(b). We also give average values and the standard deviation for each metric in Table II. We include in the table our measurements of iSWAP's gate fidelity inferred using RB and iRB, which, as expected, we find very similar to the fidelity according to FRB and iFRB [57]. We also find that the infidelity of SQiSW is reduced by 41% compared to iSWAP, while the FRB fidelity is reduced by 50%. This is similar to what is expected from the theoretical predictions (50% and 63% reduction, respectively). In particular, the additional reduction for FRB is testament to SQiSW's superior compilation abilities. More details on our benchmarking schemes are provided in Sec. V of the Supplemental Material; in Sec. IV of the Supplemental Material [23], we also discuss a fluctuation we observed in coherence times of our qubits, which we can possibly attribute to undesired coupling with a drifting two-level system.

*Conclusions.*—In this Letter we reevaluate the design of the quantum instruction set for superconducting qubits or any quantum computing platform that offers iSWAP as a native gate. By taking only roughly half of the time of iSWAP, the SQiSW gate is expected to be implemented with much higher fidelity. Moreover, it has superior compilation capabilities than iSWAP in the task of compiling arbitrary two-qubit gates. An iFRB experiment, which can benchmark non-Clifford gates, on our capacitively coupled fluxonium quantum processor shows the gate error is reduced by 41% and the Haar random two-qubit gate error is reduced by 50% compared to iSWAP on the same chip.

Our Letter indicates that while two-qubit gates such as CNOT and iSWAP are usually chosen to be the two-qubit gates in quantum instruction sets, it is actually beneficial to investigate other gates that are natively supported on the platform. A series of works [1,15,58] have studied how one can make full use of alternative two-qubit gates for compiling quantum circuits. We therefore advocate for a systematic study of hardware native gates as possible candidates to include as quantum instructions.

Additionally, the FRB and iFRB schemes are general schemes for benchmarking arbitrary gates, assuming that a Haar random unitary can be implemented efficiently. Although realizing Haar random gates is inefficient for a large number of qubits, they are still useful for characterizing one- or two-qubit hardware native gates. Our work is the first to demonstrate the applicability of the iFRB scheme as a general solution for benchmarking a non-Clifford gate. A recent work [59] established a framework for analyzing RB schemes that involve a continuous gate set under gate-dependent noise. We leave the theoretical interpretation of the iFRB decay exponent in terms of the target gate fidelity for future work.

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