Wafer-Scale Growth and Transfer of Aligned Single-Walled Carbon Nanotubes

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***Abstract*—Experimental demonstration of wafer-scale growth of well-aligned, dense, single-walled carbon nanotubes on 4″ ST-cut quartz wafers is presented. We developed a new carbon nanotube (CNT) wafer-scale growth process. This process allows quartz wafers to be heated to the CNT growth temperature of 865 °C through the alpha–beta phase transformation temperature of quartz (573 °C) without wafer fracture. We also demonstrate wafer-scale CNT transfer to transfer these aligned CNTs from quartz wafers to silicon wafers. The CNT transfer process preserves CNT density and alignment. Carbon nanotube FETs fabricated using these transferred CNTs exhibit high yield. Wafer-scale growth and wafer-scale transfer of aligned CNTs enable carbon nanotube very large-scale integration circuits and their large-scale integration with silicon CMOS.**

***Index Terms*—Carbon nanotube FETs, wafer-scale carbon nanotube growth, wafer-scale carbon nanotube transfer.**

I. Introduction

CARBON nanotube FETs fabricated from horizontally aligned single-walled carbon nanotubes (SWNTs[1]) grown on single-crystal quartz substrates have promising applications as extensions to silicon transistors in high-performance digital and analog circuits [1], [2]. At the 32 nm technology node, CNFETs circuits show 13× energy delay product improvement [2]–[4] over 32 nm silicon CMOS due to near-ballistic CNT transport [5]–[7].

Major progress has been made in demonstrating digital circuits using CNTs, e.g., ring oscillator using a single CNT [1]. However, for very large-scale integration (VLSI) CNFET circuits, multiple CNTs are needed per CNFET to provide the current density necessary for high-performance digital circuits [2]–[4]. Significant research is needed for design and integration of multiple-CNT CNFET circuits. For practical VLSI CNFET circuits, CNFETs must be fabricated on a wafer scale. We present two techniques that enable wafer-scale fabrication of CNFETs. We present wafer-scale growth of aligned CNTs on single-crystal quartz wafers and also demonstrate wafer-scale CNT transfer of aligned CNTs grown on quartz wafers to silicon wafers for VLSI integration with silicon. This low-temperature CNT transfer technique preserves CNT alignment and density. We present distributions of wafer-scale electrical characteristics of CNFETs fabricated from the aligned CNTs. CNFETs fabricated using these transferred aligned CNTs have very high yield ($\sim$99%) since they are made from multiple parallel CNTs. For VLSI CNFET integration, it is necessary to quantify CNFET variation [2]. We present statistical data from electrical and physical measurements to quantify the variations of the CNTs and CNFETs across the wafers.

We reported preliminary results of wafer-scale CNT growth and transfer techniques in [8]. In this paper, we provide a detailed description and analysis of the techniques. This paper also presents improved CNT growth and transfer processes that are compatible with patterned CNT growth for significantly enhanced CNT alignment with $\sim$99.5% of all CNTs being aligned. Design techniques described in [9] can be used to fabricate VLSI CNFET circuits that function correctly in the presence of the small fraction of misaligned and mispositioned CNTs.

The paper is organized as follows. Section II describes the wafer-scale-aligned CNT growth process, followed by Section III that describes the wafer-scale CNT transfer technique. Section IV details the characterization of CNTs using atomic force microscopy (AFM) and wafer-scale electrical measurements to quantify CNFET variations.

II. Wafer-Scale-Aligned CNT Growth

CNTs grown on substrates such as sapphire or single-crystal quartz grow aligned to a particular orientation of the crystal lattice [10], [11]. Pioneering work has been done in demonstrating aligned CNTs with remarkable CNT alignment on single-crystal quartz substrates. Patterning CNT catalyst in lithographically defined regions dramatically improves CNT alignment as it reduces the probability that a CNT encounters a catalyst particle during growth and becomes misaligned [11], [12].

For VLSI integration of CNFETs, we must scale this aligned CNT growth to the wafer scale. Published processes for aligned growth on quartz only allow growth on small quartz pieces. This is because single-crystal quartz undergoes a phase transformation from alpha quartz to beta quartz at 573 °C. This phase transformation at 573 °C results in a high probability of fracture of single-crystal wafers that are heated through this temperature [13], [14]. Aligned CNT growth requires

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[1]In this paper, all CNTs are SWNTs.

temperatures higher than 573 °C, and it has also been shown that high temperature (900 °C) annealing of quartz improves CNT alignment [11]. The probability of fracture increases with the size of the quartz substrate. Four-inch quartz wafers shatter when previously published CNT growth processes are used.

We have developed a new CNT growth process that enables full-wafer-scale growth on 4″ ST-cut quartz wafers. The key elements necessary for full-wafer-aligned CNT growth on quartz are

1) Uniform thermal gradient across the quartz wafer: This is achieved by using a three-zone chemical vapor deposition furnace. The thermal uniformity is further improved by using low pressure[2] while heating the wafers through the critical phase transformation temperature.
2) Slow thermal ramp rate through the alpha–beta phase transformation of single-crystal quartz: This reduces the probability of wafer fracture. This is consistent with prior work done, which determined that the fracture probability of bulk single-crystal quartz is inversely related to the thermal ramp rate as it is heated through the alpha–beta phase transformation temperature [14].

ST-cut quartz wafers (Hoffman Inc.) were first annealed in a three-zone, six-inch oxidation furnace. To avoid wafer fracture, the wafers were heated up slowly to 900 °C. The reduced thermal ramp rate is critical for the quartz wafers to remain intact through the alpha–beta phase transformation. The wafers were annealed in oxygen at 900 °C for 8 h. The presence of oxygen was critical for CNT alignment.[3] The wafers were brought back to room temperature after annealing using a similar slow ramp-down through the alpha–beta phase transformation of the quartz. After the annealing step, catalyst was deposited on the wafer. We used either unpatterned ferritin (Sigma Aldrich) solution (diluted 1:150 solution in DI water) or patterned iron catalyst deposited using electron beam evaporation.

After annealing, CNTs were grown in a low-pressure furnace.[4] Fig. 1 illustrates the detailed process for wafer-scale-aligned CNT growth. The wafer was calcinated in air at 550 °C for 10 min to yield catalyst nanoparticles for CNT growth. Note that the calcination temperature is less than the phase transformation temperature; hence a reduced thermal ramp rate to this calcination temperature is not required. After the calcination step, the quartz wafer, with the calcined catalyst, was heated to the CNT growth temperature of 865 °C. For the critical ramp through the phase transition temperature of quartz, the pressure was maintained at 3 Torr with 100 sccm of oxygen flow. The low pressure improves the thermal uniformity of the CNT growth furnace and reduces the thermal gradient across the wafer. The temperature ramp rate from 550 °C to 620 °C was kept at 0.8 °C/min. This ramp rate is consistent with prior studies done on the thermal fracture of bulk single-crystal quartz [14]. A faster ramp rate may be used if thermal uniformity across the wafers is within 1 °C. Beyond this critical temperature range,

[2]Low pressure reduces convective heat loss, improving thermal uniformity of the furnace.

[3]Annealing in nitrogen for the same duration gave significantly degraded CNT alignment.

[4]Base pressure of furnace was 10 mTorr.

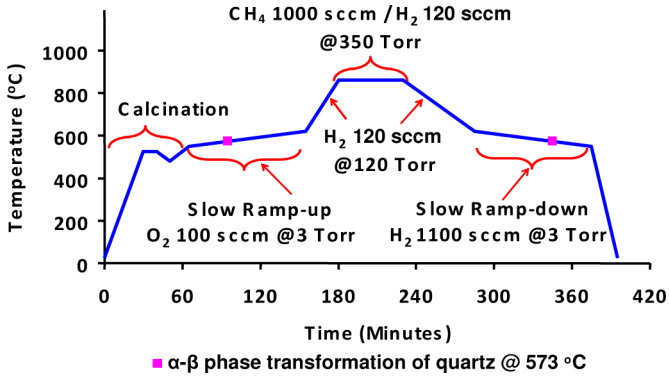

Fig. 1. Wafer-scale-aligned CNT growth process.

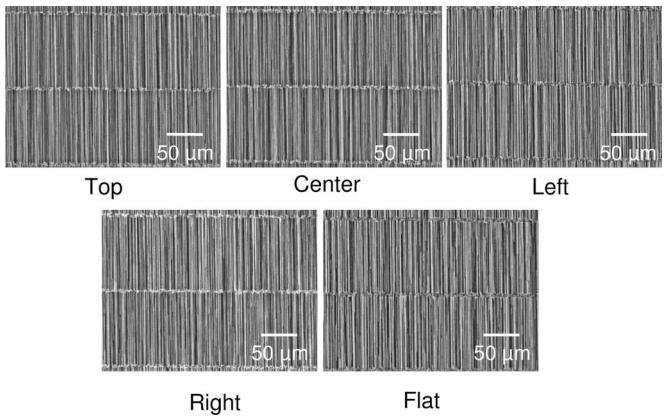

Fig. 2. Wafer-scale-aligned CNT growth using stripped Fe catalyst.

the wafer was heated in hydrogen at 120 Torr to the CNT growth temperature of 865 °C at a thermal ramp rate of ∼10 °C/min. CNT growth was carried out at 865 °C by coflowing methane and hydrogen (1000 sccm CH_4/120 sccm H_2) at a pressure of 350 Torr. After growth, the wafer was cooled to room temperature using a similar process employing a slow thermal ramp during the critical phase transformation of the single-crystal quartz wafers. The reproducibility of this wafer-scale growth technique is confirmed by multiple full-wafer-scale-aligned CNT growth runs for the various experiments presented in this paper.

CNT alignment and density can be significantly improved with patterned catalyst with ∼99.5% of CNTs being aligned. As mentioned in Section I, design principles described in [9] can be used to fabricate VLSI CNFET circuits that function correctly in the presence of the small fraction of misaligned CNTs. We show that full-wafer-aligned CNT growth on quartz is possible with patterned catalyst (Fig. 2). CNT growth was carried out using the process illustrated in Fig. 1. We used 0.2 nm of evaporated Iron (Fe) catalyst in photolithographically defined stripes. It is desirable to maximize the ratio of aligned CNT area to the catalyst area so that a large fraction of devices have aligned CNTs. We used different catalyst stripe widths (W) ranging from 0.5 to 10 μm and catalyst stripe spacing (S) between 50 and 1200 μm (Fig. 3). The CNTs have an average length of ∼400 μm and an average density of 5–10 CNTs/μm. The longest CNTs are approximately 675 μm in length [Fig. 3(a)]. The maximum

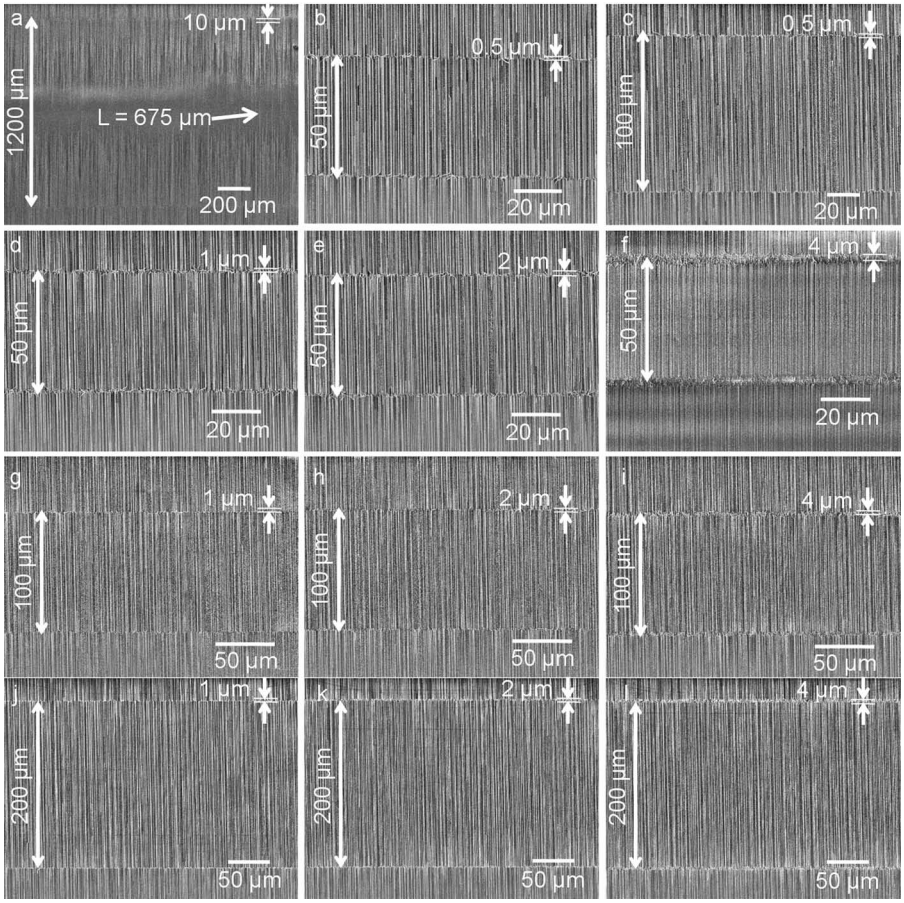

Fig. 3. Effect of catalyst width (W) and spacing (S) on CNT density and CNT coverage. (a) $W = 10\ \mu$m, $S = 1200\ \mu$m. (Length of longest CNT in image = 675 μm). (b) $W = 0.5\ \mu$m, $S = 50\ \mu$m. (c) $W = 0.5\ \mu$m, $S = 100\ \mu$m. (d) $W = 1\ \mu$m, $S = 50\ \mu$m. (e) $W = 2\ \mu$m, $S = 50\ \mu$m. (f) $W = 4\ \mu$m, $S = 50\ \mu$m. (g) $W = 1\ \mu$m, $S = 100\ \mu$m. (h) $W = 2\ \mu$m, $S = 100\ \mu$m. (i) $W = 4\ \mu$m, $S = 100\ \mu$m. (j) $W = 1\ \mu$m, $S = 200\ \mu$m. (k) $W = 2\ \mu$m, $S = 200\ \mu$m. (l) $W = 4\ \mu$m, $S = 200\ \mu$m.

catalyst spacing, for which CNT density is uniform between stripes, is approximately equal to the CNT length ($\sim 400\ \mu$m). Experimental results show that the catalyst strip can be as narrow as 0.5 μm. It may be possible to further reduce the width of the catalyst strip, while retaining high CNT density between the stripes.

III. Wafer-Scale CNT Transfer

For VLSI integration of CNFETs on silicon, aligned CNTs need to be transferred from quartz to silicon on a wafer scale. Transfer of aligned CNTs grown on quartz wafer pieces to silicon substrates using gold and polyimide was first demonstrated in [11]. Here, we demonstrate a new CNT transfer technique that can be used to transfer CNTs from quartz to silicon on a wafer scale. This low temperature (90 °C–120 °C) transfer procedure uses thermal release adhesive tape (Nitto Denko, Part Number: #3198MS) and preserves CNT density and alignment (Fig. 4). Unlike aligned CNT growth that requires high temperatures, CNT transfer is a low temperature process and enables the integration of CNTs on already fabricated silicon CMOS wafers, dies, and flexible substrates.

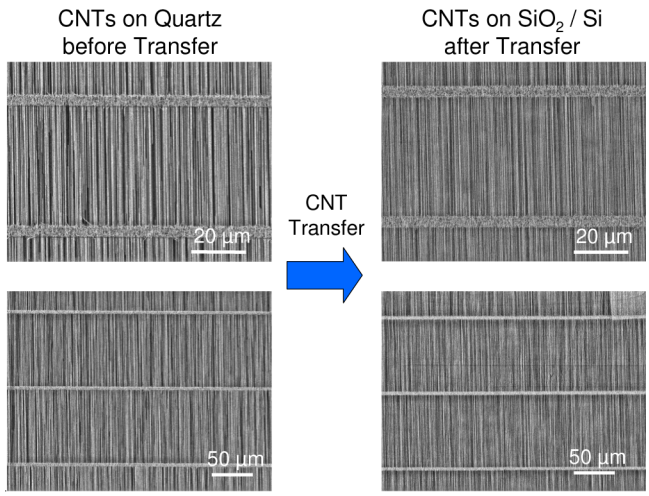

Fig. 4. SEM images of transferred CNTs.

Fig. 5 illustrates the CNT transfer technique. Aligned CNTs are grown on a quartz wafer [Fig. 5(a)]. A gold film (100 nm) is evaporated on the quartz wafer using e-beam evaporation [Fig. 5(b)]. Thermal release tape is applied to the gold film and the tape/gold bilayer is peeled off from the quartz substrate

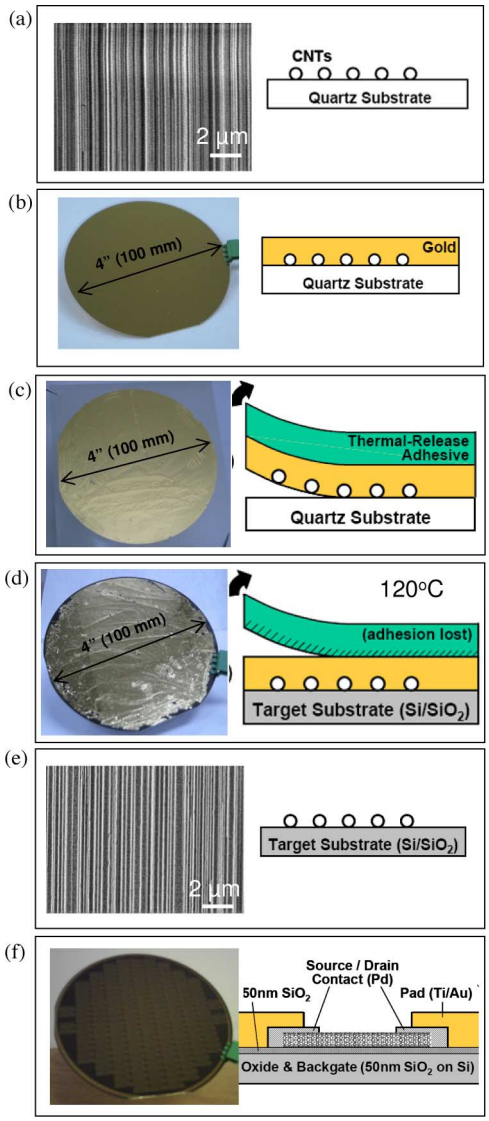

Fig. 5. CNT transfer technique.

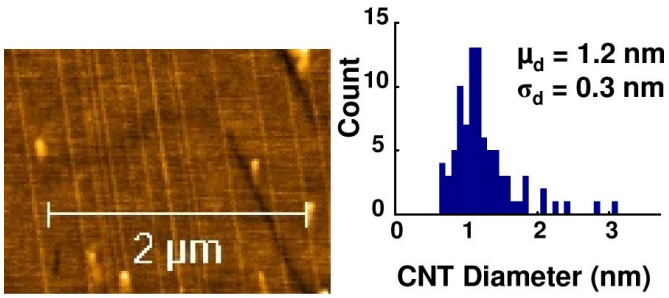

Fig. 6. (a) AFM image of aligned CNTs on quartz. (b) CNT diameter distribution.

[Fig. 5(c)]. The CNTs remain embedded in the gold layer. This tape/gold bilayer is then applied to the target wafer. The target wafer is then heated to the release temperature of the tape (90 °C or 120 °C, depending upon the type of thermal release tape). At this temperature, the tape loses adhesion and peels off, while the gold, along with the embedded CNTs, sticks to the target substrate (Fig. 5(d)). Oxygen plasma descum (55 W, 25 mTorr, 20 sccm O_2) for 3 min is then used to remove organic residues from the gold surface after transfer. The gold is then removed using gold etchant (Transcene Corp. KI/I_2), which leaves the CNTs on the target wafer. Fig. 5(e) shows an SEM image of the transferred CNTs on a silicon wafer. CNT density and alignment is preserved as can be seen from Figs. 4 and 5(e).

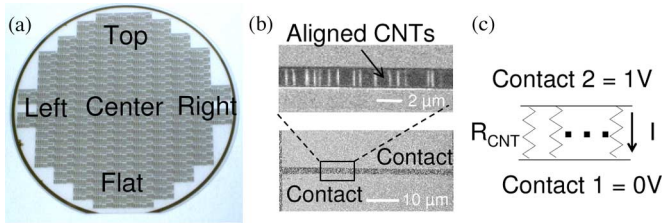

Fig. 7. (a) Optical micrograph of $4''$ ST-cut quartz wafer after aligned CNT growth and subsequent patterning of contacts. (b) SEM image of aligned CNTs bridging two contacts. (c) Two terminal measurement parameters.

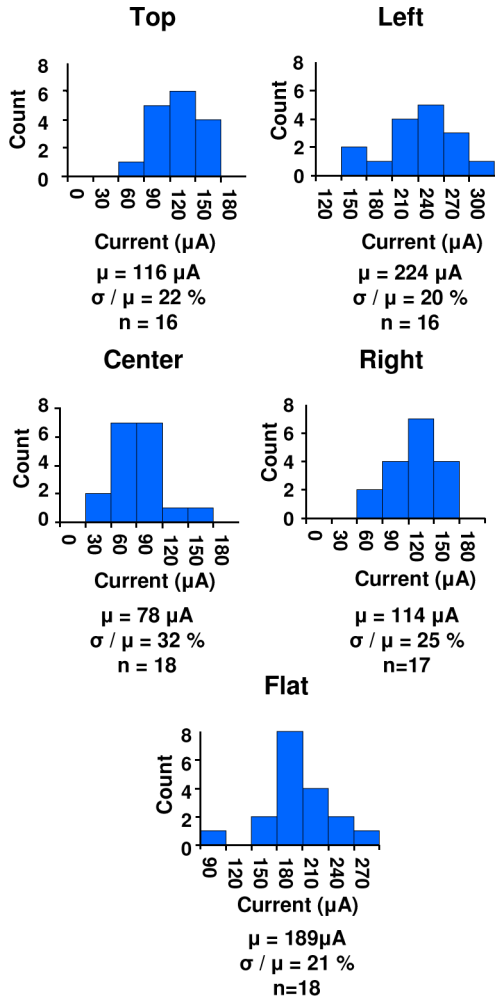

Fig. 8. Two terminal current distributions at 1V bias for n functional devices (out of 18) (Width $=$ 50 μm, Length $=$ 1 μm) in 5 arbitrary dies (out of 197 dies on the wafer) over 5 regions of the quartz wafer.

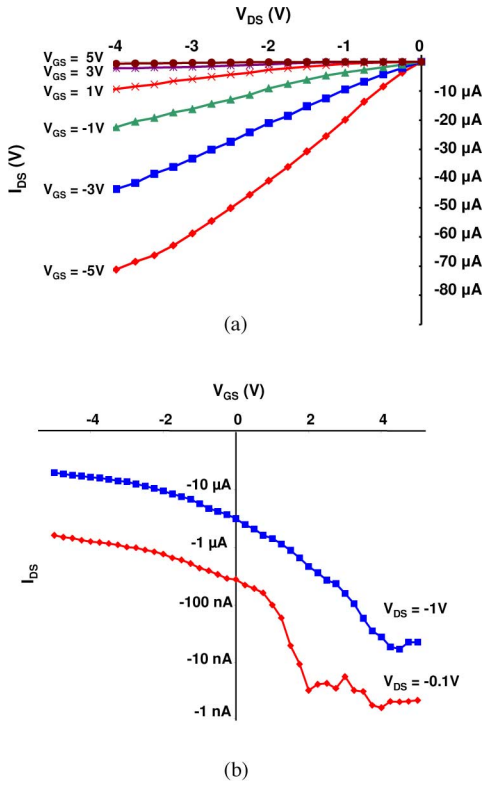

Fig. 9. CNFET current-voltage characteristics (width = 50 μm, length = 1 μm, $t_{\mathrm{SiO2}} = 50$ nm) after metallic-CNT breakdown. (a) I_{ds} vs. V_{ds}. (b) I_{ds} vs. V_{gs}.

IV. Characterization of CNTs

Using wafer-scale-aligned CNT growth described in Section II and wafer-scale-aligned CNT transfer described in Section III, we can now characterize CNT and CNFET variations. The CNTs have a mean diameter (μ_d) of 1.2 nm with a standard deviation (σ_d) of 0.3 nm [Fig. 6(b)] as measured from AFM images [Fig. 6(a)]. Fig. 7(a) shows an optical micrograph of a quartz wafer after CNT growth. The wafer was patterned with contacts [Ti (5 nm)/Au (40 nm)] using photolithography and e-beam evaporation of metals. We conducted two-terminal measurements of 18 devices with width = 50 μm/length = 1 μm [Fig. 7(b)] in a randomly selected die in each region (top, left, center, right, and flat) of the wafer. The measured current is due to the CNTs bridging the contacts and provides a measure of the electrical uniformity of the CNTs across the wafer. Fig. 8 shows the mean current and the standard deviation of these two terminal measurements at a bias of 1V. The standard deviation of CNT current equals to ~25% of the mean current in all regions. The variation in CNFET current is likely due to variation in the CNT density and CNT contact resistance.

We also fabricated back-gated CNFETs on silicon wafers using transferred CNTs. Fabricated CNFETs had a low $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio due to the presence of metallic CNTs. Metallic CNTs can be removed by using electrical breakdown [15] or selective etching [16]. CNFETs retain well-behaved I–V characteristics after electrical burning. Fig. 9 shows the current-voltage (I_{ds} vs. V_{ds} and I_{ds} vs. V_{gs}) measurements of a CNFET with Ti (1 nm)/Au (40 nm) source and drain contacts. We used electrical breakdown of metallic CNTs to achieve a high $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio [15], [16].

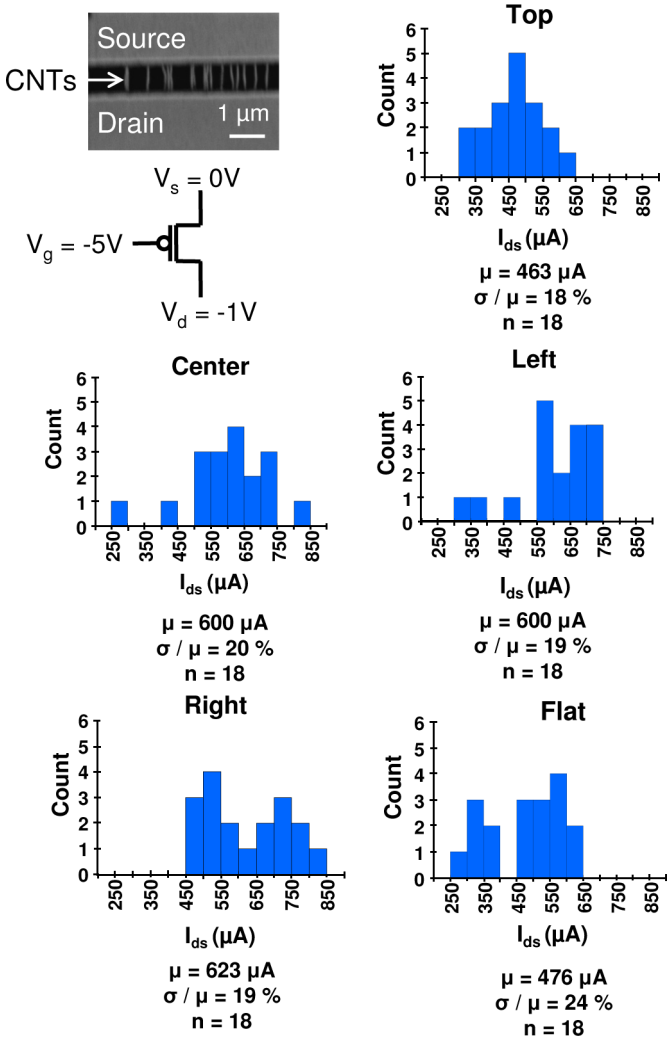

Fig. 10. CNFET current distributions ($V_{\mathrm{ds}} = 1$ V $V_{\mathrm{gs}} = -5$ V) of 18 back-gated CNFETs ($W = 50$ μm, $L = 1$ μm, $t_{\mathrm{SiO2}} = 50$ nm, Ti(5 nm)/Au(50 nm) contacts) in five regions of the silicon wafer.

To assess the electrical uniformity of the transferred CNTs across the wafer, we measured the I_{ON} ($V_{\mathrm{gs}} = -5$ V, $V_{\mathrm{ds}} = -1$ V) distributions of CNFETs (prior to electrical breakdown). For this electrical characterization, we measured 18 identically sized (width = 50 μm, length = 1 μm) randomly chosen CNFETs in each of the five regions (top center, left, right, and flat) of the wafer (out of a total of ~100 000 CNFETs fabricated) (Fig. 10).

SEM images indicate an average CNT density of approximately 4 CNTs/μm. For the 50 μm wide CNFETs, there are, on average, 200 CNTs per CNFET. The average CNFET ON-current across the wafer is 552 μA corresponding to CNFET average current density of 11 μA/μm. For the performance gains over CMOS projected in [2], CNT density must be improved to 250 CNTs/μm. One potential technique to attain high CNT density is to perform wafer-scale CNT transfer (Fig. 5) multiple times from multiple quartz wafers to the same target silicon wafer.

V. Conclusion

We have presented wafer-scale-aligned growth on single-crystal quartz and wafer-scale CNT transfer from quartz wafers to silicon wafers. Full-wafer-scale CNT growth on quartz and full-wafer-scale CNT transfer from quartz to silicon enable wafer-scale characterization of CNFETs and fabrication of VLSI circuits. The low-temperature CNT transfer technique potentially enables integration of aligned CNTs with already fabricated silicon CMOS dies, wafers, and flexible substrates, while preserving CNT density and alignment. Compatibility of wafer-scale aligned growth and transfer techniques with scalable metallic-CNT removal techniques, such as selective etching of metallic CNTs [17], and metallic CNT tolerant circuit design [18] must be investigated.

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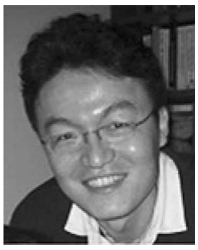

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