MOSFET Channel Length: Extraction and Interpretation

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***Abstract*—This paper focuses on MOSFET channel length: its definition, extraction, and physical interpretation. After a brief review of the objectives of channel length extraction and previous extraction methods, the principle and the algorithm of the latest "shift and ratio" (S&R) method are described. The S&R method allows the channel mobility to be an arbitrary function of gate voltage and, at the same time, provides a way to determine the threshold voltage of short-channel devices independent of their parasitic resistances. Accurate and consistent results are obtained from nMOSFET and pMOSFET data down to 0.05 μm channel length. By applying the S&R method to model generated current–voltage (I–V) curves, it is shown that the extracted channel length should be interpreted in terms of the injection points where the MOSFET current spreads from the surface layer into the bulk source-drain region. This implies significant degradation of short-channel effects (SCE's) if the lateral source-drain doping gradient is not abrupt enough. Several remaining issues, including errors due to channel-length-dependent mobilities, difficulties with lightly-doped drain (LDD) MOSFET's, and interpretation of capacitance–voltage (C–V) extracted channel lengths, are discussed in** Section VIII

***Index Terms*—Integrated circuits, MOSFET's, semiconductor devices, transistors.**

I. Introduction

CHANNEL length is a key parameter in CMOS technology used for performance projection (circuit models), short-channel design, and process monitoring. It usually differs from the mask gate length by an amount depending on the gate lithography and the etch bias, as well as on the lateral source-drain diffusion. In general, channel length is determined from a series of linear (low-drain-bias) I_{ds}–V_g curves of devices with different mask lengths. Extraction and physical interpretation of MOSFET channel lengths are becoming increasingly difficult in the deep submicron region due to strong variation of mobility with gate voltage, more pronounced effects of graded source-drain doping profiles, and linewidth-dependent lithography bias near the optical resolution limit.

This paper focuses on MOSFET channel length: its definition, extraction, and physical interpretation. Section II examines various definitions of channel length and the objectives of channel length extraction. Section III reviews several commonly used channel length extraction methods and their limitations. Section IV describes the principle and the algorithm of the "shift and ratio" (S&R) method. Section V shows the application of the S&R method to 0.1–μm nMOSFET and pMOSFET device data. Section VI examines the physical meaning of the extracted $L_{\rm eff}$ by applying the S&R method to model generated I_{ds}–V_g curves. Section VII addresses the implications on short-channel effects. (SCE's) Section VIII discusses possible errors due to channel-length-dependent mobilities, $L_{\rm eff}$ of lightly-doped drain (LDD) MOSFET's, and extraction of channel length from capacitance–voltage (C–V) measurements. Section IX concludes the paper.

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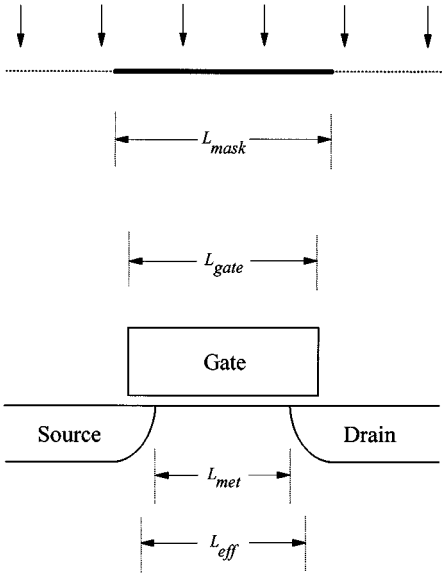

Fig. 1. Schematic diagram showing the definition and relationship among the various terms of channel length. The physical interpretation of $L_{\rm eff}$ is examined in Section VI.

II. Various Definitions of Channel Length

A number of terms, e.g., *mask length* ($L_{\rm mask}$), *gate length* ($L_{\rm gate}$), *metallurgical channel length* ($L_{\rm met}$), and *effective channel length* ($L_{\rm eff}$), have been used to describe the length of a MOSFET. Even though they are all related to each other, their relationships are strongly process dependent.

Fig. 1 shows schematically how various channel lengths are defined. $L_{\rm mask}$ is the design length on the polysilicon etch mask. It is reproduced on the wafer as $L_{\rm gate}$ through lithography and etching processes. Depending on the lithography and etching biases, $L_{\rm gate}$ can be either longer or shorter than $L_{\rm mask}$. There are also process tolerances associated with $L_{\rm gate}$. For the same $L_{\rm mask}$ design, $L_{\rm gate}$ may vary from chip to chip, wafer to wafer, and run to run. Although $L_{\rm gate}$ is an important parameter for process monitoring and control, there

is no simple way of making a large quantity of measurements. Typically, $L_{\rm gate}$ is measured by scanning electron microscope (SEM) only sporadically across some wafers. The exact $L_{\rm gate}$ of the device being measured electrically is usually unknown. There is also an uncertainty in the precise definition of $L_{\rm gate}$ when the polysilicon etch profile is not vertical. It is ambiguous as to whether $L_{\rm gate}$ refers to the top or to the bottom dimension of the gate.

$L_{\rm met}$ is defined as the distance between the metallurgical junctions of the source and drain diffusions at the silicon surface. Since the source and drain regions are self-aligned to the polysilicon gate in a standard process, there is a close correlation between $L_{\rm met}$ and $L_{\rm gate}$. Usually, $L_{\rm met}$ is shorter than $L_{\rm gate}$ by a certain amount due to the lateral straggle of ion implantation and the lateral source-drain diffusion in the process. Accurate, physical measurement of $L_{\rm met}$ in actual hardware is very difficult. Normally, $L_{\rm met}$ is used only in two–dimensional (2-D) models for short-channel device design. Even for that purpose, difficulties arise in defining $L_{\rm met}$ when dealing with a buried-channel device or a retrograde channel profile with zero surface doping, where there are no metallurgical junctions at the silicon surface.

The parameter $L_{\rm eff}$ is different from all other channel lengths discussed above in that it is defined through some electrical characteristics of the MOSFET device and as such is not strictly a physical parameter (a source of much confusion in the literature). It should be pointed out at the outset that $L_{\rm eff}$ extraction, based on just measured terminal currents, cannot generate a detailed model with all the physics taken into account since the 2-D doping profile of the device is not known. This necessitates the use of simplified, effective models for which $L_{\rm eff}$ has no precisely defined physical meaning. Qualitatively, $L_{\rm eff}$ is a measure of how much gate-controlled current a MOSFET delivers in reference to the long-channel device.

Despite the deficiency stated above, there are two main objectives for channel length extraction.

1) Process monitoring, for which one wants a parameter that tracks (for a given process) $L_{\rm gate}$ which varies statistically for a given $L_{\rm mask}$ due to process tolerances, and yet can be easily determined by automated electrical measurements.
2) Circuit modeling, for which one needs a parameter for current calculations. Since all circuit models assume a one–dimensional (1-D) long-channel expression for linear currents, it is natural to use that equation for defining $L_{\rm eff}$.

A key point to realize here is that one cannot expect to find the metallurgical channel length by channel length extraction. The conventional association of $L_{\rm eff}$ with $L_{\rm met}$ originates from the over-simplified notion that the source-drain junctions are infinitely abrupt. In reality, source-drain doping gradients are always finite (but unknown) and the metallurgical channel length as defined has no direct bearing on device current. A good example is the buried-channel device in which the surface doping is of the same type as the source and drain. There is no metallurgical p-n junction along the surface so $L_{\rm met} = 0$, but the current remains finite. In fact, application of $L_{\rm eff}$ extraction algorithm to buried-channel devices yields no anomalous results that differ from those of surface-channel devices. The correct physical interpretation of $L_{\rm eff}$ is discussed in Section VI.

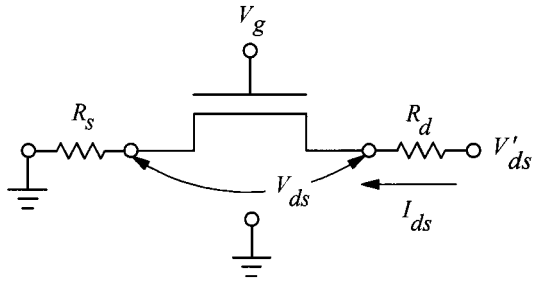

Fig. 2. Equivalent circuit of MOSFET with source and drain series resistance.

III. A Brief Review of $L_{\rm eff}$ Extraction Methods

The basis of $L_{\rm eff}$ definition lies in the fact that the channel resistance of a MOSFET in the linear or low-drain bias region is proportional to the channel length. That is

$$R_{ch} \equiv \frac{V_{ds}}{I_{ds}} = \frac{L_{\rm eff}}{\mu_{\rm eff} C_{ox} W (V_g - V_t)} \tag{1}$$

where

I_{ds} and V_{ds}	source-drain current and voltage (usually kept below 100 mV);
W	device width;
C_{ox}	gate oxide capacitance per unit area;
V_g	gate voltage;
V_t	linearly extrapolated threshold voltage;
$\mu_{\rm eff}$	effective mobility which contains the inversion-layer capacitance and the polysilicon-gate depletion effects [1].

$\mu_{\rm eff}$ is a weak function of V_g. (Sometimes a second-order term $-V_{ds}/2$ is included in the $(V_g - V_t)$ factor in (1), which makes no difference in the discussions of this paper.) For different $L_{\rm mask}$, $L_{\rm eff}$ differs but is assumed to relate to $L_{\rm mask}$ by a constant (independent of bias voltages) *channel length bias* ΔL

$$L_{\rm eff} = L_{\rm mask} - \Delta L. \tag{2}$$

All the lithography and etch biases as well as the lateral source-drain implant straggle and diffusion are lumped into ΔL.

In the simplest scheme of channel length extraction [2], R_{ch} is measured for a set of devices with different $L_{\rm mask}$. Based on (1) and (2), a plot of R_{ch} for a given V_g versus $L_{\rm mask}$ should yield a straight line whose intercept with the x-axis gives ΔL and therefore $L_{\rm eff}$. In practice, however, two issues must be addressed for short-channel devices. The first one is the source-drain series resistance. The second one is the SCE which causes V_t in (1) to vary with $L_{\rm mask}$.

The effect of source-drain resistance is examined using the equivalent circuit in Fig. 2. A source resistance R_s and a drain resistance R_d are assumed to connect an *intrinsic* MOSFET to the external terminals where a voltage V'_{ds} is applied between

the source and drain. If one defines the total source-drain parasitic resistance as $R_{sd} = R_s + R_d$, the externally measured total resistance can be written as

$$\begin{aligned} R_{tot} &\equiv \frac{V'_{ds}}{I_{ds}} \\ &= R_{sd} + R_{ch} \\ &= R_{sd} + \frac{L_{\text{mask}} - \Delta L}{\mu_{\text{eff}} C_{ox} W (V_g - V_t)}. \end{aligned} \tag{3}$$

(Here, we do not distinguish between the intrinsic and the external V_g since the difference, $R_s I_{ds}$, is a second-order term and can be dropped without loss of generality [1].) Note that V_t is defined in terms of the intrinsic device, i.e., one that would be obtained from linear extrapolation if there were no parasitic resistances. A key assumption in almost all L_{eff}-extraction algorithms is that, in contrast to R_{ch}, R_{sd} is independent of gate voltage. In fact, one should regard L_{eff} as defined by (3) with R_{sd} independent of gate voltage. In other words, R_{sd} is defined as the constant part of the measured device resistance, consistent with existing circuit models.

A good survey of various existing methods for channel length extraction can be found in [3]. In one class of extraction methods [4], [5], the mobility dependence on vertical field is assumed to take the following explicit form:

$$\mu_{\text{eff}} = \frac{\mu_0}{1 + \theta (V_g - V_t)} \tag{4}$$

where μ_0 and θ are constants, independent of V_g. If one substitutes (4) into (3) and takes a derivative with respect to V_g, it is straightforward to show that

$$\frac{I_{ds}}{\sqrt{dI_{ds}/dV_g}} = \sqrt{\frac{\mu_0 C_{ox} V'_{ds} W}{L_{\text{eff}}}} (V_g - V_t) \tag{5}$$

regardless of R_{sd} [6]. This has been used to determine the V_t of various devices and therefore L_{eff}. However, (5) is not supported by actual device data, as is clear from Fig. 3 which shows that when $I_{ds}/(dI_{ds}/dV_g)^{1/2}$ of a long-channel device is plotted as a function of V_g, the curve does not fit a straight line. This implies that the assumption (4) is too restrictive and is likely to lead to error in extraction results. For example, V_t extrapolation depends on which part of the curve in Fig. 3 is used. More sophisticated analytical forms of mobility may provide a better fit to the data, but they generally do not lead to a form like (5) for the linear extrapolation of V_t. Furthermore, the extraction results may depend on the specific function assumed.

There is actually no need to assume any explicit form of the $\mu_{\text{eff}}(V_g - V_t)$ function to carry out L_{eff} extraction. As a matter of fact, $\mu_{\text{eff}}(V_g - V_t)$ is exactly the information provided by the long-channel device. In the most commonly used method of channel length extraction [7], [8], called the *channel resistance method*, it is only necessary to assume that μ_{eff} does not change with channel length (this is examined later in Section VIII). For a set of devices with different L_{mask} but the same W, the parameters R_{sd}, ΔL, and C_{ox} are the same within process tolerances. The linear threshold voltage V_t, however, does depend on

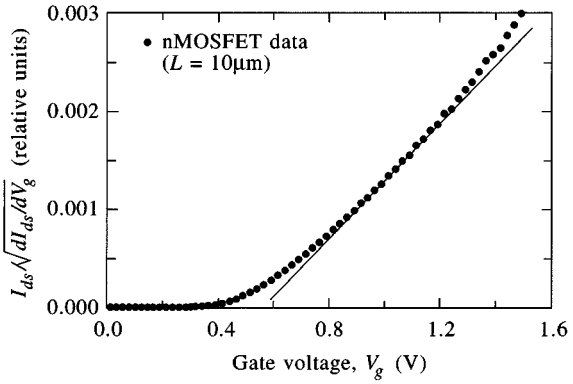

Fig. 3. $I_{ds}/(dI_{ds}/dV_g)^{1/2}$ versus V_g for a long-channel device. The straight line is an attempt to fit the high overdrive part of the curve.

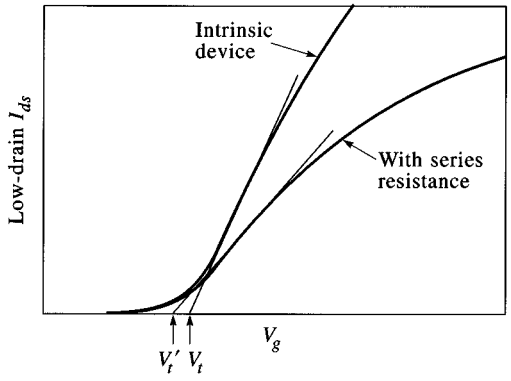

Fig. 4. Low-drain-bias (linear) I_{ds}–V_g curves of a short-channel device with and without series resistance, showing errors introduced on the linearly-extrapolated V_t.

channel length because of SCE's. When comparing R_{tot} of devices with different L_{mask}, therefore, it is important to measure V_t for each device and adjust V_g such that the gate overdrive $(V_g - V_t)$ is the same from device to device. A plot of R_{tot} (at small V'_{ds}) versus L_{mask} for a given $(V_g - V_t)$ would then yield a straight line that passes through the point $(\Delta L, R_{sd})$. The slope of the line depends on the specific value of the gate overdrive. ΔL and R_{sd} are determined by the common intercept of several lines, each for a different $(V_g - V_t)$ [8].

Despite the simplicity of the channel resistance method, two key issues remain. First, it is by no means straightforward to accurately determine the intrinsic V_t of short-channel devices. The presence of R_{sd} adds considerable difficulty in the usual linear extrapolation of V_t from the measured I_{ds}–V_g curve [9]. Typically, one tends to underestimate V_t in short-channel devices as the degradation of I_{ds} by R_{sd} is more severe at higher currents. This is illustrated in Fig. 4, where the "apparent" V_t-extrapolated from the measured I_{ds}–V_g curve is lower than the intrinsic device V_t because of series resistance effects. This introduces errors in channel length extraction. An iterative method has been used to correct the series resistance effect on V_t and obtain more accurate results [9]. However, several iterations are normally required, and a convergence problem may arise if the program is not robust enough. The problem is further aggravated by a strong dependence of mobility on gate voltage, for example, in low-temperature and/or 0.1 μm MOSFET's. The second problem with the resistance method is that the R_{tot}

versus $L_{\rm mask}$ lines for different gate overdrives may not intersect at a common point. Significant errors may result if only a limited number of $(V_g - V_t)$ are investigated.

IV. "Shift and Ratio" Method

An improved channel length extraction algorithm, called the "*shift and ratio*" method, is able to circumvent the above problems [10]. Shift and ratio (S&R) method is based on the same channel resistance concept described above. It starts with a generalization of (3) to the form

$$R^i_{tot}(V_g) = R_{sd} + L^i_{\rm eff} f(V_g - V^i_t) \tag{6}$$

where f is a general function of gate overdrive common to all the measured devices. The superscript i denotes the ith device with an unknown effective channel length $L^i_{\rm eff} = (L^i_{\rm mask} - \Delta L)$ and linear threshold voltage V^i_t. The key assumption behind (6) is that the effective mobility $\mu_{\rm eff}$ is a common function of $(V_g - V_t)$ for all the measured devices.

The task is to solve R_{sd}, $L^i_{\rm eff}$, and V^i_t in (6) from the measured data of $R^i_{tot}(V_g)$. The S&R algorithm simplifies the procedure by differentiating (6) with respect to V_g. Since the parasitic resistance R_{sd} is either independent or a weak function of V_g, its derivative can be neglected

$$S^i(V_g) \equiv \frac{dR^i_{tot}}{dV_g} = L^i_{\rm eff}\,\frac{df(V_g - V^i_t)}{dV_g}. \tag{7}$$

Here, df/dV_g is also a general function of gate overdrive common to all the devices measured. An important benefit of working with the derivatives is that R_{sd} drops completely out of the picture so it does not matter if R_{sd} varies from device to device as long as it is constant. S&R extraction is usually done with two devices: one long-channel and one short-channel. Equation (7) with superscript i represents the short-channel device, while superscript 0 refers to the long-channel device

$$S^0(V_g) \equiv \frac{dR^0_{tot}}{dV_g} = L^0_{\rm eff}\,\frac{df(V_g - V^0_t)}{dV_g}. \tag{8}$$

An example is shown in Fig. 5 for two devices: S^0 for $L^0_{\rm mask} = 10\ \mu$m, and S^i for $L^i_{\rm mask} = 0.25\ \mu$m.

It would have been easy if $V^i_t = V^0_t$, in which case S^i and S^0 are similar functions of V_g and $L^i_{\rm eff}$ is simply solved from the ratio $S^i/S^0 = L^i_{\rm eff}/L^0_{\rm eff} \approx L^i_{\rm eff}/L^0_{\rm mask}$. In general, however, $V^i_t \neq V^0_t$, and the two S-functions must be shifted with respect to each other before the ratio is taken. For example, in Fig. 5, we can shift one curve (S^i) horizontally to the right by a varying amount δ, and compute the ratio between the two curves

$$r(\delta, V_g) \equiv \frac{S^0(V_g)}{S^i(V_g - \delta)} \tag{9}$$

as a function of V_g. The purpose here is to find the δ value for which the ratio r is a constant, independent of V_g. If δ is zero or too small, r is a monotonically decreasing function of V_g. On the other hand, if δ is too large, r becomes a monotonically increasing function of V_g. These are shown in Fig. 6. Only when S^i is shifted by an amount δ equal to the threshold voltage difference between the two devices, $(V^0_t - V^i_t)$, does r become

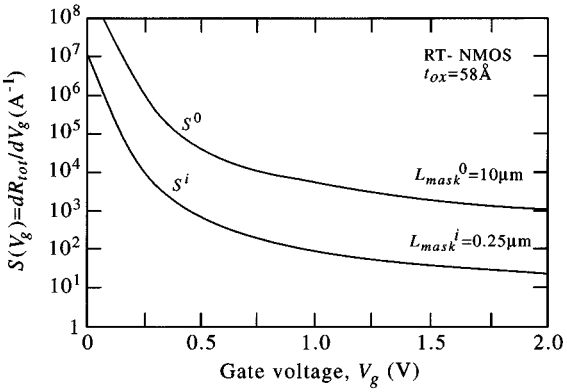

Fig. 5. Examples of $S(V_g) = dR_{tot}(V_g)/dV_g$ curves measured from long-($L_{\rm mask} = 10\ \mu$m) and short-channel ($L_{\rm mask} = 0.25\ \mu$m) devices.

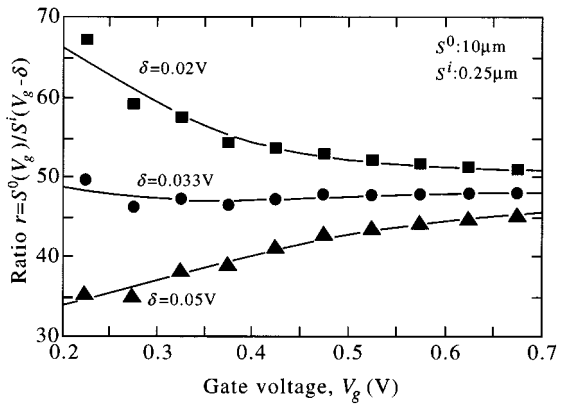

Fig. 6. $r(\delta, V_g)$ (ratio of S-functions after shift) versus V_g curves for three different amounts of shift (δ). The data are taken from the device examples in Fig. 5.

nearly independent of V_g. Once the correct shift is found, it is a simple matter to solve $L^i_{\rm eff}$ from the ratio r evaluated at that shift.

The above procedure can be automated by computing the average r and the mean square deviation of r from its average value, i.e.,

$$\langle r \rangle = \frac{\displaystyle\int_{\Delta V_g} r(\delta, V_g)\, dV_g}{\displaystyle\int_{\Delta V_g} dV_g} \tag{10}$$

and

$$\langle \sigma^2 \rangle = \langle r^2 \rangle - \langle r \rangle^2 \tag{11}$$

as functions of δ for a selected range of gate voltage, ΔV_g. Fig. 7 plots the example where the $\langle \sigma^2 \rangle$ versus δ curve exhibits a sharp minimum at the point of best match (constant S ratio)

$$\delta_{\rm min} = V^0_t - V^i_t. \tag{12}$$

The channel length $L^i_{\rm eff}$ (or ΔL) can be solved from the average ratio $\langle r \rangle$ at this point

$$\langle r \rangle_{\delta\,\rm min} = \frac{L^0_{\rm eff}}{L^i_{\rm eff}} = \frac{L^0_{\rm mask} - \Delta L}{L^i_{\rm mask} - \Delta L}. \tag{13}$$

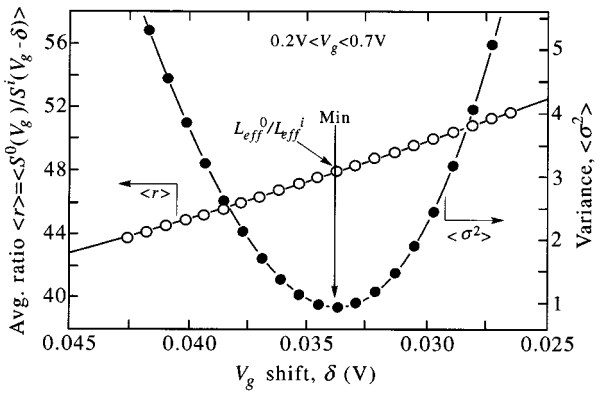

Fig. 7. Average ratio $\langle r\rangle$ (open circle) and variance $\langle\sigma^2\rangle$ (solid dot) versus shift δ. The data are taken from the device examples in Fig. 5 and 6.

Note that even if ΔL is different between the long-channel and the short-channel devices, very little error is introduced as $\Delta L \ll L^0_{\rm mask}$, hence $L^0_{\rm eff} \approx L^0_{\rm mask}$, insensitive to ΔL.

Once $\delta_{\rm min}$ and $\langle r\rangle_{\delta\,\rm min}$ are found, R_{sd} can be calculated from the measured resistances based on (6) and the corresponding equation for the long-channel device (superscript 0)

$$R_{sd} = \frac{\langle r\rangle_{\delta\,\rm min} R^i_{tot}(V_g - \delta_{\rm min}) - R^0_{tot}(V_g)}{\langle r\rangle_{\delta\,\rm min} - 1}. \qquad (14)$$

For a given long-channel reference, the above extraction procedure can be repeated for a number of short-channel devices with different $L^i_{\rm mask}$. A by-product of the process is the low-drain short-channel threshold voltage rolloff given by $\delta_{\rm min}$.

V. Application to 0.1-μm MOSFET

S&R algorithm has been applied to 0.1–μm nMOSFET's and pMOSFET's with e-beam patterned polysilicon gates and abrupt source-drain junctions [11]. The effective channel lengths extracted from nMOSFET currents are shown in Fig. 8(a) versus mask length. A straight line fit through the points shows that the channel length bias, $\Delta L = L_{\rm mask} - L_{\rm eff}$, is fairly constant for all the devices down to an $L_{\rm eff}$ of 0.05 μm. If the channel resistance extraction method [8] were applied to the same set of device data without series resistance corrections on V_t, the resulting $L_{\rm eff}$ would be significantly longer due to the underestimate of V_t in short-channel devices (Fig. 4).

Once the channel lengths are known, the series resistance R_{sd} of each device can be calculated using (14). The results are also plotted in Fig. 8(a). There is very little variation (±10%) of R_{sd} among the devices of different mask lengths. While it is not necessary to assume a constant ΔL and R_{sd} for the S&R algorithm to work, comparable ΔL and R_{sd} results among different devices are a good indication that the channel length extraction has been carried out consistently. Similar $L_{\rm eff}$ and R_{sd} results extracted from the 0.1–μm pMOSFET data are shown in Fig. 8(b). The R_{sd} extracted from pMOSFET's is typically a factor of two higher than that from nMOSFET's, more or less in agreement with the mobility difference between the two types of devices.

After $L_{\rm eff}$ is extracted, it is instructive to play back the decomposed R_{ch} and R_{sd} as a function of gate voltage. Typical examples for 0.08–μm nMOSFET's and pMOSFET's are shown in Fig. 9. In both cases, R_{sd} is nearly a constant, independent of V_g, self-consistent with the assumption made in (7).

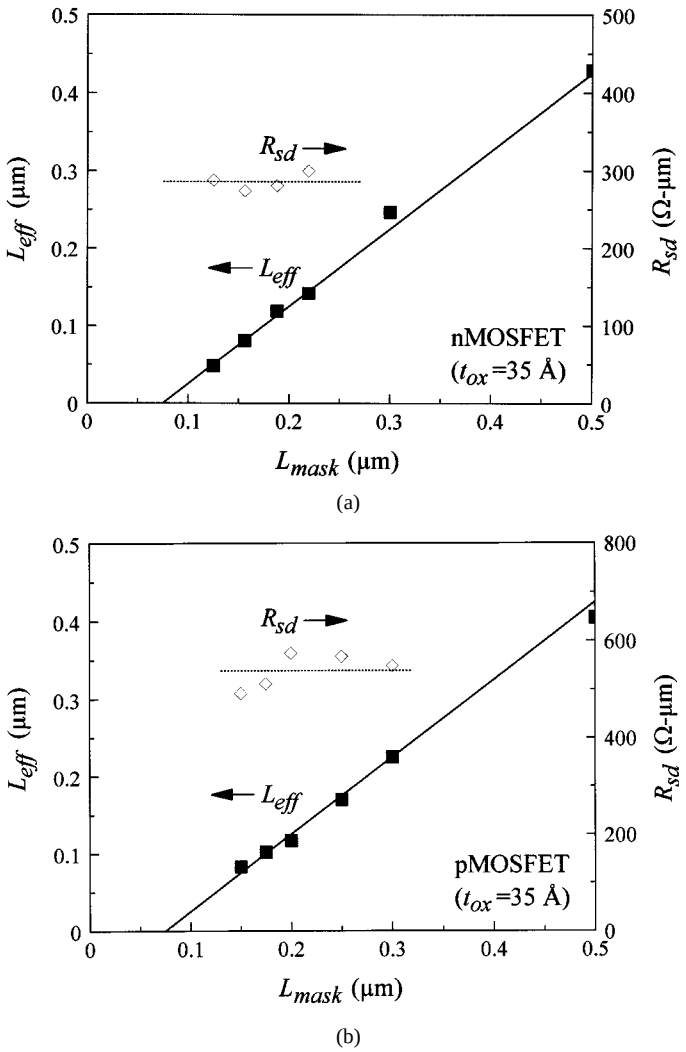

Fig. 8. S&R extracted effective channel length (solid square) and source-drain series resistance (open diamond) versus mask length for (a) nMOSFET's and (b) pMOSFET's.

It is important in the S&R algorithm to choose a proper gate voltage range ΔV_g for $\langle r\rangle$ and $\langle\sigma^2\rangle$ calculations. V_g range affects the extracted $L_{\rm eff}$ just like the intersection point (ΔL, R_{sd}) in the conventional channel resistance method depends on which two gate overdrives ($V_g - V_t$) are selected. S&R method allows us to take a whole range of $V_g - V_t$ into account, not just two discrete values. The V_g range for S&R extraction should not include the subthreshold region where the current conduction is controlled by diffusion over a maximum potential barrier, instead of by the average potential in the channel as in the linear region where (1) is based [12]. Fig. 10 shows the sensitivity of the extracted $L_{\rm eff}$ to the V_g range used for two nMOSFET's with $L_{\rm mask} = 0.188$ and 0.125 μm, respectively. The source and drain are abruptly doped. It can be seen that for both devices, $L_{\rm eff}$ is nearly independent of the V_g-range as long as the starting point is not too close to the linearly-extrapolated threshold voltage V_t. A good choice for ΔV_g is therefore from about ($V_t + 0.2$ V) all the way up to V_{dd}, which covers most regions of interest in the I_{ds}–V_g curve. In general, the sensitivity

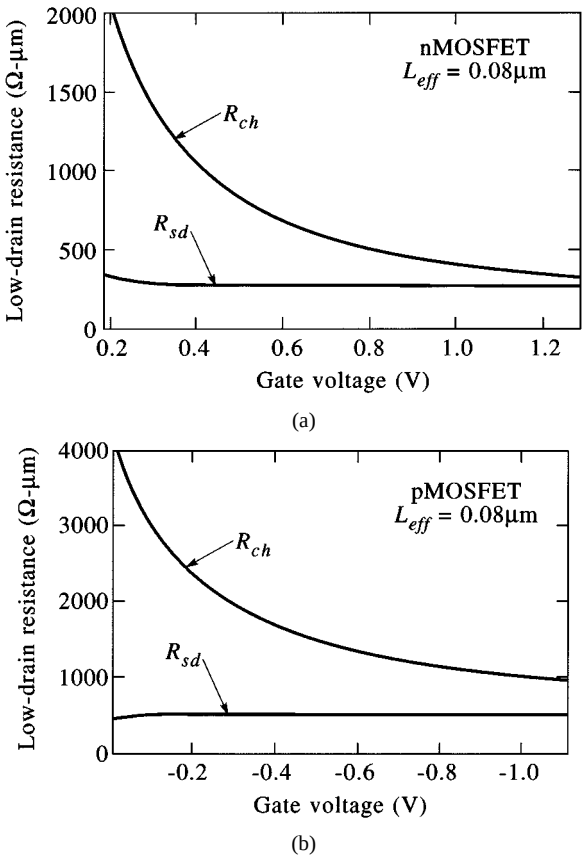

Fig. 9. Decomposition of the measured $R_{tot}(V_g)$ into $R_{ch}(V_g)$ and $R_{sd}(V_g)$ for (a) an 0.08–μm nMOSFET and (b) an 0.08–μm pMOSFET after S&R extraction.

of the extracted $L_{\rm eff}$ to ΔV_g depends on how abrupt the lateral source-drain profile is. This is discussed in more detail in the next subsection.

VI. Physical Meaning of $L_{\rm eff}$

While the S&R method yields consistent results down to sub-0.1–μm channel lengths, caution must be exercised not to interpret the extracted $L_{\rm eff}$ as the metallurgical channel length $L_{\rm met}$ under all circumstances. By its definition, $L_{\rm eff}$ represents a measure of the "effective" current carrying capability of the device and is not associated with any fixed physical quantity. When the channel profile is reasonably uniform and the source-drain doping is not too graded, $L_{\rm eff}$ is approximately equal to $L_{\rm met}$ [13]. In general, however, one cannot take $L_{\rm eff} = L_{\rm met}$ for granted, especially in very short-channel MOSFET's.

To find a proper physical interpretation for $L_{\rm eff}$, the same S&R algorithm is applied to I_{ds}–V_g curves generated from a 2-D device simulator. Fig. 11 plots the extracted $L_{\rm eff}$ versus $L_{\rm met}$ for a variety of source-drain and channel doping conditions [14]. A key parameter is the lateral straggle σ_L of an assumed 2-D Gaussian profile for the source and drain doping concentration near the gate edge

$$N_d(x, y) = N_0 e^{-(x-x_0)^2/2\sigma_V^2} e^{-(y-y_0)^2/2\sigma_L^2}. \qquad (15)$$

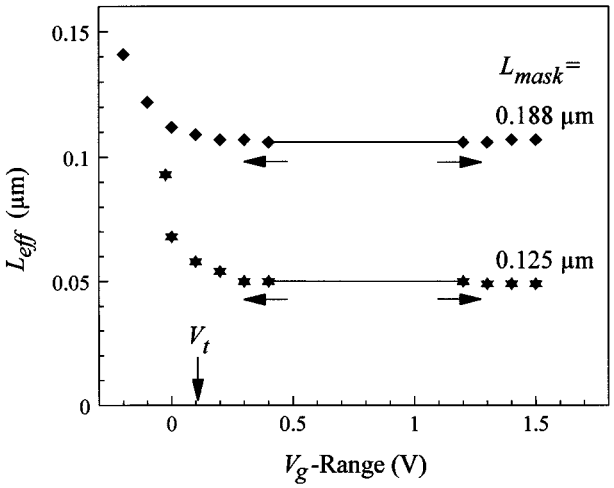

Fig. 10. Extracted $L_{\rm eff}$ versus V_g-range used in the S&R algorithm. For each of the two nMOSFET's shown, the base range is 0.4 V $\leq V_g \leq$ 1.2 V. The range is then stretched in either direction with the other end fixed. For example, the $L_{\rm eff}$ value plotted at $V_g = 1.5$ V is obtained with a range of 0.4 V $\leq V_g \leq$ 1.5 V, and that at $V_g = 0.1$ V is obtained with 0.1 V $\leq V_g \leq$ 1.2 V.

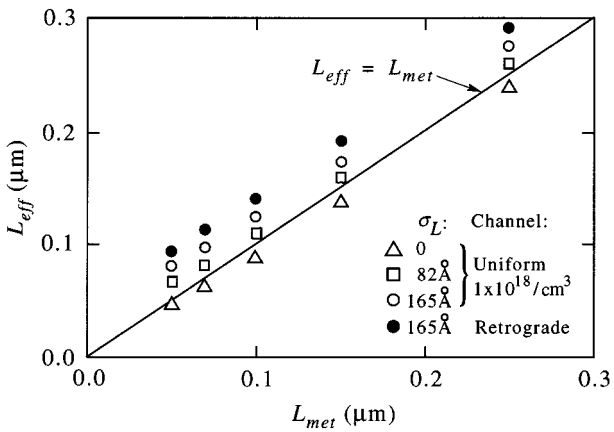

Fig. 11. $L_{\rm eff}$ extracted from simulated currents versus $L_{\rm met}$ for four doping cases. Open symbols are for a uniformly-doped channel with different lateral source-drain gradients. Solid dots are for a retrograde-doped channel.

Here, $N_0 = 10^{20}$ cm^{-3}, x is in the vertical direction and y is in the lateral direction. The vertical straggle σ_V is chosen such that the junction depth $x_j = 500$ Å. For each of the doping cases in Fig. 11, $L_{\rm eff}$ varies linearly with $L_{\rm met}$ with a slope of unity. This confirms that $L_{\rm eff}$ tracks $L_{\rm gate}$ for a given process, thus validating the use of $L_{\rm eff}$ for process monitoring purposes. However, ($L_{\rm eff} - L_{\rm met}$) varies considerably with the doping profile. For an infinitely abrupt source-drain profile, $\sigma_L = 0$, ($L_{\rm eff} - L_{\rm met}$) is slightly negative. As the lateral straggle σ_L increases, ($L_{\rm eff} - L_{\rm met}$) becomes increasingly more positive. The difference grows even larger in the retrograde channel case where $L_{\rm eff}$ is significantly longer than $L_{\rm met}$.

Such a deviation can be understood by examining the laterally-varying channel sheet resistivity defined by [1]

$$\rho_{ch}(y) = \frac{dV/dy}{I_{ds}/W} = \frac{1}{\mu_{\rm eff}|Q_i(y)|} \qquad (16)$$

where $V(y)$ is the quasi-Fermi level and $Q_i(y)$ is the inversion charge density per unit area at a point y along the channel length

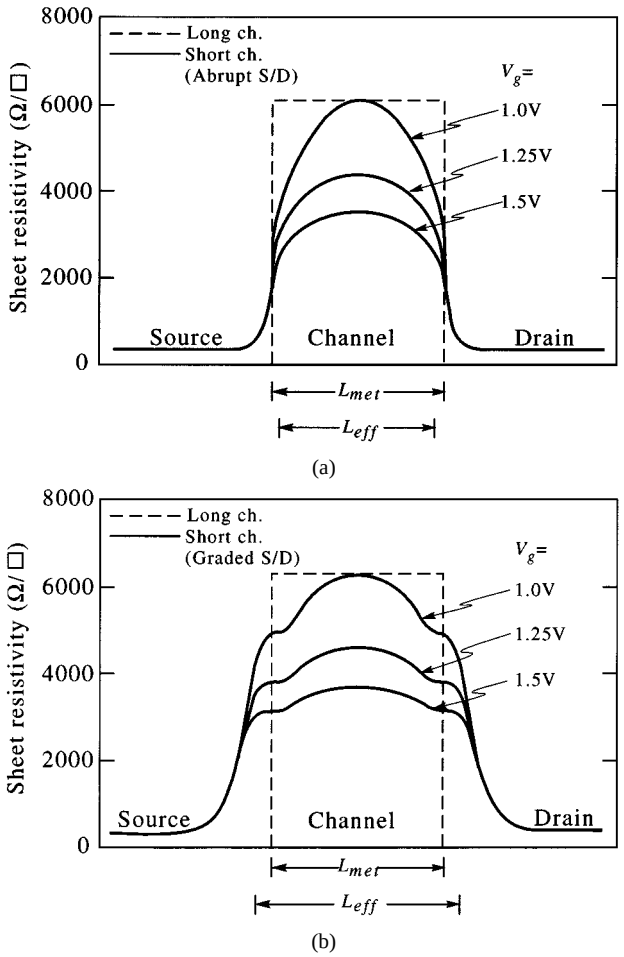

Fig. 12. Simulated channel sheet resistivity at three different gate voltages versus distance from source to drain of a $L_{\rm met} = 0.10$ μm nMOSFET. The curves in (a) are for an infinitely abrupt (laterally) source-drain case in which $L_{\rm eff} = 0.091$ μm. The curves in (b) are for a graded ($\sigma_L = 165$ Å) source-drain case in which $L_{\rm eff} = 0.124$ μm. In both cases, the dashed lines represent the ideal, uniform sheet resistivity of a scaled long-channel device.

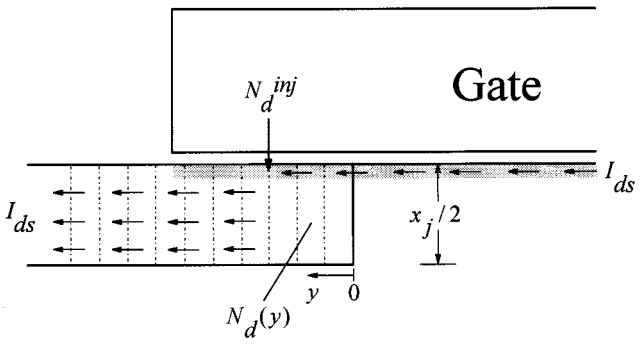

Fig. 13. Schematic diagram of a simple 1-D model for estimating the source-drain doping concentration at the point of current injection from the surface into the bulk. As far as the resistance is concerned, the source or drain region is modeled as uniform stripes of doping concentration $N_d(y)$ and width $x_j/2$.

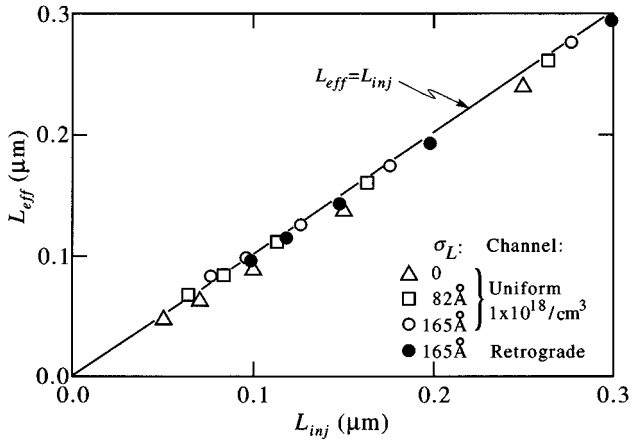

Fig. 14. Same $L_{\rm eff}$ data as in Fig. 11, but plotted versus L_{inj} in terms of the current injection points. Open symbols are for a uniformly-doped channel with different lateral source-drain gradients. Solid dots are for a retrograde-doped channel.

direction. The terminal current I_{ds} is a constant independent of y as required by current continuity. This expression is valid as long as the current flow is largely parallel to the y-direction and the equipotential contours are perpendicular to the silicon surface.

Fig. 12 plots $\rho_{ch}(y)$ calculated from the 2-D device simulator versus distance from the source to the drain for $L_{\rm met} = 0.10$ μm at three different gate voltages [14]. The area under each curve gives the total source-drain resistance for that particular gate voltage. It is first noted that, in contrast to a long-channel device for which $R_{ch} = (L_{\rm eff}/W)\rho_{ch}$ as implied by (1), $\rho_{ch}(y)$ is nonuniform with a peak near the middle of the channel while decreasing toward the edges, especially at low gate voltages near threshold. This is due to SCE's from the source-drain fields which help lower the potential barrier near the junctions and raise the local inversion charge density [15]. Sheet resistivity is more uniform within the channel at higher gate voltages, which makes such ranges more suitable for channel length extraction as discussed above (Fig. 10).

In Fig. 12(a) for an infinitely abrupt (laterally) source-drain junction, the sheet resistivity is modulated by the gate voltage only inside the metallurgical channel and the extracted $L_{\rm eff}$ is slightly shorter than $L_{\rm met}$ (triangles in Fig. 11). On the other hand, in Fig. 12(b) for the same $L_{\rm met} = 0.10$ μm, but with a finite lateral source-drain gradient, a nonnegligible portion of the sheet resistivity outside the metallurgical channel is also gate-voltage-dependent. This is because of accumulation or gate modulation of the series resistance arising from the finite source-drain doping gradient. Since, according to the $L_{\rm eff}$ definition in (6), any part of the sheet resistivity that is gate voltage-dependent contributes to the effective channel length, the extracted $L_{\rm eff}$ is substantially longer than $L_{\rm met}$ (circles in Fig. 11).

To further illustrate the point and to quantify the relationship between $L_{\rm eff}$ and source-drain doping gradient, a simple 1-D current model is constructed in Fig. 13. When the gate voltage is high enough to turn on the nMOSFET channel, an n^+ surface accumulation layer is also formed in the gate-to-source or -drain overlap region [16]. Current flow out of the inversion channel stays in the accumulation layer near the surface until the local source-drain doping becomes high enough that the bulk conductance exceeds that of the accumulation layer. For an n^+ polysilicon gated nMOSFET, the sheet resistivity of the accumulation layer is approximately given by [1]

$$\rho_{ac} = \frac{1}{\mu_{ac}|Q_{ac}|} = \frac{1}{\mu_{ac}C_{ox}V_g} \tag{17}$$

where Q_{ac} is the charge density and μ_{ac} is the average electron mobility in the accumulation layer [17]. The only difference between the V_g-dependence of ρ_{ac} in (17) and of ρ_{ch} in (1) is the term V_t. In reality, there is no abrupt, distinct transition from the channel to the accumulation region, as the local V_t and therefore the sheet resistivity always change smoothly over the graded region (see Fig. 12). Without knowing the exact 2-D doping profile, there is no consistent way of separating the accumulation layer resistance from the channel resistance. The region where the current flows predominantly in the accumulation layer is therefore considered, in some effective way, as a part of L_{eff}.

To estimate the source-drain doping concentration at which current injection into the bulk takes place, we assume the surface donor concentration in Fig. 13 to be $N_d(y)$ which varies along the direction of current flow as dictated by the lateral doping gradient. If the bulk resistivity corresponding to N_d is $\rho(N_d)$ and the source-drain junction depth is x_j, the average sheet resistivity of a thin stripe perpendicular to the current flow is approximately $\rho(N_d)/(x_j/2)$. Current injection into the bulk takes place at $N_d = N_d^{inj}$ where the sheet resistivity $\rho(N_d^{inj})/(x_j/2)$ equals ρ_{ac} of (17). Since ρ_{ac} depends on the gate voltage, so does the point of injection [18], [22]. For reasonably abrupt source-drain doping profiles, $N_d(y)$ is a strong (exponential) function of y and the injection points do not spread too far apart. Setting $\rho(N_d^{inj})/(x_j/2)$ equal to ρ_{ac} of (17) with $V_g = V_{dd}/2$ corresponding to the middle of the V_g-range for the S&R algorithm, one can solve N_d^{inj} from

$$\rho\left(N_d^{inj}\right) = \frac{x_j}{\mu_{ac} C_{ox} V_{dd}} \tag{18}$$

where μ_{ac} can be looked up from the universal mobility curve at an average normal field of $\mathcal{E}_{\text{eff}} = C_{ox}V_{dd}/4\varepsilon_{si}$ [19].

In general, N_d^{inj} increases as the device dimensions are scaled down. For a 1 μm CMOS technology, $N_d^{inj} \approx 10^{17}$ cm^{-3}. For the 0.1 μm devices in Fig. 11, $V_{dd} = 1.5$ V, $t_{ox} = 30$ Å, $x_j = 500$ Å, one obtains $\mathcal{E}_{\text{eff}} = 4.2 \times 10^5$ V/cm, $\mu_{ac} = 420$ cm^2/V-s [19], and $\rho(N_d^{inj}) = 0.007$ Ω-cm. The last number corresponds to $N_d^{inj} \approx 8 \times 10^{18}$ cm^{-3} from the n-type silicon resistivity curve. Fig. 14 replots the simulated L_{eff} data in Fig. 11 against L_{inj} defined as the distance between the points where the source-drain doping equals N_d^{inj}. All the points lie within 100 Å of the $L_{\text{eff}} = L_{inj}$ line, independent of the lateral doping gradient and channel profile. This supports the physical interpretation of L_{eff} in terms of the current injection points from the accumulation layer.

VII. Implications on Short-Channel Effect

The fact that L_{eff} can be much longer than L_{met} has significant implications on short-channel V_t roll-off curves. Fig. 15 shows the low-drain threshold voltage roll-off versus L_{eff} for several different source-drain doping gradients. The abrupt doping profile has the best SCE. As the lateral straggle increases, SCE becomes progressively worse. This is best illustrated in Fig. 16, where the net doping concentration ($N_d - N_a$) at the surface is plotted along the channel length direction for

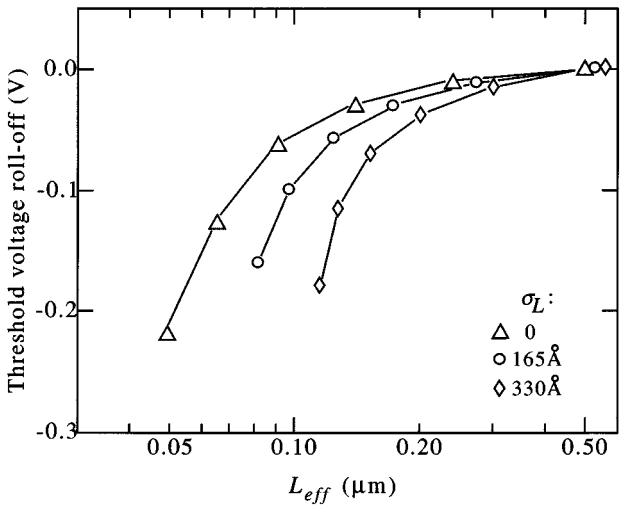

Fig. 15. Simulated short-channel threshold roll-off versus L_{eff} for three different lateral source-drain doping gradients. In each curve, the points are for $L_{\text{met}} = 0.05$, 0.07, 0.10, 0.15, 0.25, and 0.50 μm.

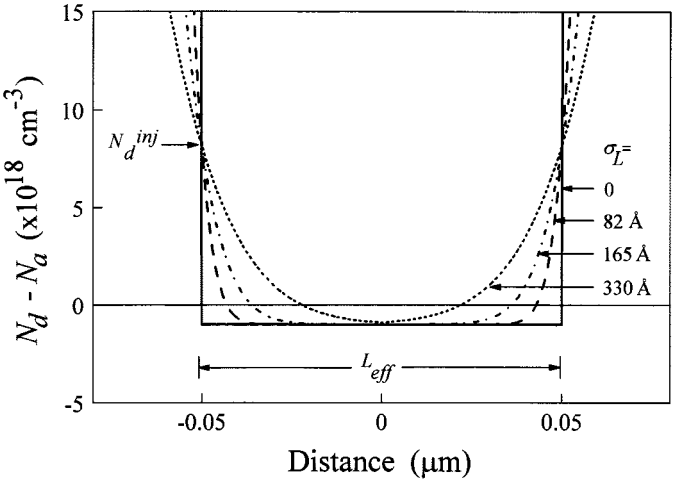

Fig. 16. Net n-type concentration along the surface of a 0.1 μm (L_{inj} or L_{eff}) nMOSFET versus lateral distance from the source to the drain. The injection points (N_d^{inj}) are kept the same for all four cases of different lateral doping gradients.

the various source-drain profiles studied. For a given L_{eff} or L_{inj} (=0.1 μm), the distance between the points where the doping concentration falls to N_d^{inj} (=8×10^{18} cm^{-3} in this case) is fixed. It is clear that the more graded the source-drain profile is, the deeper the n-type doping tail penetrates into the channel and compensates or reverses the p-type doping inside the channel. This is detrimental to the SCE as the edge regions become more easily depleted and inverted by the source and drain fields (opposite to the *halo* effect [11]). It is therefore very important to reduce the lateral width of the graded source-drain region as the channel length is scaled down.

VIII. Discussions

The cornerstones of nearly every channel length extraction method are: channel-length independent mobility and gate-voltage independent series resistance (considered in Section III as the definition of R_{sd}). In earlier works such as [20], inconsistent extraction results led to the speculation that

the mobility might be degraded in 0.1 μm devices due to stress. This would of course render the $L_{\rm eff}$ solution to (1) ambiguous. While channel-length independent mobility is an assertion rather than a conclusion of the S&R extraction method, consistent $L_{\rm eff}$'s such as those in Fig. 8 lend confidence in its validity down to sub-0.1–μm channel lengths. There is, however, a known mechanism that causes the mobility to vary slightly with channel length through the V_t-dependence. This is discussed below, followed by discussions on gate-voltage-dependent series resistance in LDD MOSFET's, and interpretation of channel lengths extracted from C–V measurements.

A. Errors Due to Vertical-Field Dependent Mobility

Strictly speaking, short-channel devices have a slightly higher mobility $\mu_{\rm eff}$ because of the lower threshold voltage and therefore lower vertical field ($\mathcal{E}_{\rm eff}$) for the same ($V_g - V_t$). Assuming a long-channel V_t of 0.5 V and a power supply voltage V_{dd} of 2.0 V, one can estimate the effect of V_t rolloff on $\mathcal{E}_{\rm eff}$ based on [1]

$$\mathcal{E}_{\rm eff} = \frac{V_t + 0.2}{3t_{ox}} + \frac{V_g - V_t}{6t_{ox}}. \tag{19}$$

For a V_t (low drain) rolloff of 100 mV, the vertical field is 14% lower at $(V_g - V_t) = 0$ and 7% lower at $(V_g - V_t) = 1.5$ V (maximum). Since $\mu_{\rm eff} \propto \mathcal{E}_{\rm eff}^{-0.3}$ from, say, [19], an average of (14% + 7%)/2 = 10.5% lower $\mathcal{E}_{\rm eff}$ translates into a mobility increase of only 3%. Such a small error is deemed acceptable for most practical purposes of the channel length extraction.

In fact, the vertical-field dependence of mobility is built-in in the 2-D model simulation that led to Fig. 11. The observed trend that the extracted ($L_{\rm eff} - L_{\rm met}$) becomes slightly longer (more positive) at very short channel lengths, instead of slightly shorter as suggested by the above mobility effect, implies that it is more than compensated by other 2-D effects.

Recently, heavy *halo* implants have been employed to create a laterally nonuniform channel doping for counteracting short-channel effects at or below 0.1 μm [27]. This often leads to a strong *reverse short-channel effect* such that short-channel V_t's can be 100 mV or more higher than that of the long-channel reference. When coupled with a strongly field dependent mobility at $\mathcal{E}_{\rm eff} \geq 1$ MV/cm, this effect results in extracted $L_{\rm eff}$'s significantly longer than what would be otherwise. A possible solution is to apply a reverse substrate bias to the long-channel reference device until its V_t matches that of the short-channel device. In other words, instead of shift and ratio, the long-channel substrate bias is varied until the ratio of the S-functions (without shift) between the long and the short devices becomes nearly independent of V_g. In effect, the vertical field in the long-channel device is raised to the same level as in the short device, thus equalizing their mobilities for the purpose of channel length extraction.

B. Effective Channel Length of LDD MOSFET's

LDD MOSFET's [21] are designed with an extended, moderately-doped (10^{17}–10^{18} cm^{-3} range) source-drain region to relieve high electric fields and related hot-electron effects. The presence of such a lightly-doped region poses great difficulties in the extraction and interpretation of effective channel length. Current injection from the surface accumulation layer into the bulk region takes place over an extended distance with the location dependent on gate voltage. No matter what kind of $L_{\rm eff}$ extraction method is used, $L_{\rm eff}$ is significantly longer than $L_{\rm met}$, especially at high gate overdrives [9]. In some cases, especially when a wide spacer is employed, the extracted $L_{\rm eff}$ may even be slightly longer than $L_{\rm gate}$, as the sheet resistivity of the lightly-doped source-drain region immediately outside the gate edge can still be modulated by the fringe field from the gate.

In one attempt to deal with V_g-dependent R_{sd} of LDD devices, a substrate bias is used to alter V_t in (3) [22]. This generates multiple values of ($V_g - V_t$) for a given V_g, thus allowing a common intercept (ΔL, R_{sd}) to be determined from several R_{tot} versus $L_{\rm mask}$ lines, as in the channel resistance method described in Section III. However, due to geometry effects, V_t variation with substrate bias is channel length-dependent. One cannot maintain the same ($V_g - V_t$) among different $L_{\rm mask}$'s by applying the same substrate bias to all the devices. As a result, this method usually leads to erroneously short $L_{\rm eff}$'s with a part of the V_g-dependent (but insensitive to the substrate bias) channel resistance lumped into R_{sd} [15].

In another approach, channel resistance extraction is carried out for a pair of closely spaced V_g [18]. The procedure is repeated throughout the entire voltage range, allowing both $L_{\rm eff}$ and R_{sd} to be gate-voltage-dependent. Similar methods can be implemented in the S&R algorithm as well by breaking up the full voltage range used in (10) into small intervals of 0.5 or 0.25 V each. A set of ($L_{\rm eff}$, R_{sd}) can be extracted from the current data in each interval by repeating the S&R algorithm. However, most circuit models do not accommodate gate-voltage- dependent channel lengths. Furthermore, once $L_{\rm eff}$ and R_{sd} are allowed to be gate-voltage-dependent, there is no unique way of breaking up R_{ch} and R_{sd} from the measured R_{tot}, and the solutions to (3) or (6) become ambiguous and method-dependent.

There is no set method in defining the $L_{\rm eff}$ of an LDD MOSFET. If the entire I_{ds}–V_g characteristics can be fitted within acceptable tolerances (e.g., 5–10%) by a constant $L_{\rm eff}$ and a constant R_{sd}based on (6), a circuit model can be formulated with these parameters. Otherwise, one needs to define a constant $L_{\rm eff}$, perhaps using the figure extracted from the current data at low gate overdrives [9], and leave the rest of the resistance as a gate-voltage-dependent series resistance. For process monitoring purposes, as long as one adheres to a consistent approach, there should be a constant relationship between the extracted $L_{\rm eff}$ and $L_{\rm gate}$. It is not necessary to look for a unique, precisely defined $L_{\rm eff}$ which does not exist in LDD devices.

C. Extraction of Channel Length by C–V Measurements

In an entirely different approach, another type of channel length has been extracted from the measured C–V data of a series of MOSFET's with different $L_{\rm mask}$ [23]. It is based on the fact that, when a MOSFET is turned on, the intrinsic gate-to-channel capacitance is proportional to the channel length

$$C_{gc} = C_{ox} W L_{cap}. \tag{20}$$

Here, L_{cap} is the capacitively defined channel length which may or may not be the same as $L_{\rm eff}$ or $L_{\rm met}$. However, just like in the resistance extraction methods, the total measured capacitance also contains a parasitic gate to source-drain overlap component in addition to the intrinsic capacitance

$$C_{tot} = C_{gc} + 2C_{ov} = C_{ox}WL_{cap} + 2C_{ov}. \qquad (21)$$

Here, C_{ov} is the overlap capacitance per gate edge, which is independent of channel length. Typical examples of C_{tot}–V_g curves can be found in [24]. Using a large-area MOS capacitor, one can easily calibrate C_{ox}, taking all the polysilicon depletion and inversion layer quantum effects into account. To find out L_{cap}, it is critical to determine what $2C_{ov}$ to subtract from the measured C_{tot}. [Plotting C_{tot} versus $L_{\rm mask}$ only yields an x-intercept made up of two unknowns: $\Delta L_{cap} \equiv (L_{\rm mask} - L_{cap})$ and $2C_{ov}/C_{ox}W$.] In principle, $2C_{ov}$ in (21) is the parasitic capacitance at a gate voltage when the MOSFET is on and C_{gc} is given by (20). In practice, $2C_{ov}$ cannot be separated from C_{gc} since, unlike channel resistance, channel capacitance does not vary significantly with gate voltage once the device is turned on. What is usually done is to take $2C_{ov}$ as the measured capacitance when the MOSFET is off. However, $2C_{ov}$ varies with the gate voltage [24], [25]. There is no guarantee that $2C_{ov}$ in the off state is the same as $2C_{ov}$ in the on state. If $2C_{ov}$ is taken as the capacitance right below the threshold voltage, it will contain an unwanted inner fringe term that is absent when the conducting channel is formed. If $2C_{ov}$ is taken at a negative gate voltage (for nMOSFET's) to accumulate the substrate and eliminate the inner fringe component, the directly overlapped source-drain region could be depleted [23]. Any such error in $2C_{ov}$ translates into a large error in L_{cap} when dealing with short-channel devices having small intrinsic capacitances.

A better interpretation of the capacitively extracted channel length is in terms of the gate length, $L_{\rm gate}$ (Fig. 1). As the gate voltage is varied, the same amount of charge per unit area is induced at the silicon surface whether it is in the inversion channel or in the source-drain overlap region under the gate. In other words, as far as the capacitance is concerned, the direct overlap length should be lumped into the channel length. This circumvents the problem with the inner fringe component mentioned above. One still needs to estimate the outer fringe capacitance and subtract it from the measured capacitance. But this can be done using a simple formula [26] (typically ~0.1 fF/μm per edge) and should have much less error associated with it.

IX. Conclusions

In conclusion, the extraction and physical interpretation of MOSFET channel length have been thoroughly investigated using 0.1–μm CMOS device data together with 2-D model simulations. The S&R extraction method is shown to circumvent the limitations of previous methods and yield accurate and consistent results down to 0.05 μm. A proper physical interpretation of the extracted $L_{\rm eff}$ is in terms of the injection points where the MOSFET current spreads from the surface layer into the bulk source-drain region. A key implication is that the SCE could become significantly worse if the lateral spread of the source and drain junctions is not properly scaled together with the channel length. Finally, it is pointed out that the channel lengths extracted from C–V methods are best interpreted in terms of $L_{\rm gate}$, which complements $L_{\rm eff}$ obtained from current–voltage (I–V) methods.

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