ZA7783 Display Interface Converter

Datasheet

Version 1.1

Revision History

Ver.	Date	Author	Content
0.5	2013-5-14	Dai Jin	1. Initial release
0.6	2013-9-29	Jiang Bo	1. Add typical application circuit 2. Add package information 3. Add functional block diagram
0.7	2014-2-12	Jiang Bo	1. Change LVDS_ATO to DVDD18
1.0	2014-4-28	Jiang Bo	1. Add software register description 2. Add more details for typical application circuit 3. Add software guideline 4. Add electrical parameters
1.1	2014-9-3	Jiang Bo	1. Change DVDD12 cap to 0.47uF 2. Modify power-up sequence

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1 Overview

ZA7783 is a bridge chip which supports three kinds of display interfaces:

- MIPI DSI RX Interface (1 Clock Lane + 4 Data Lanes)
- LVDS TX Interface (1 Clock Lane + 4 Data Lanes)
- MIPI DPI TX/RX Interface (PCLK + RGB888 + VSYNC + HSYNC + DATAEN)

The chip bridges these display interfaces in three working modes:

- MODE1: MIPI DSI RX => LVDS TX
- MODE2: MIPI DSI RX => DPI TX
- MODE3: DPI RX => LVDS TX

Besides, there is also an I2C control interface (XCLK + I2C_SCL + I2C_SDA) for the host chip (AP or BB) to access ZA7783's software registers.

Analog IPs of ZA7783 are supplied by 3.3V voltage (typical). For Digital IOs, the host interface (XCLK + I2C_SCL + I2C_SDA) is supplied by DVDD18 (PIN32), while the DPI interface (PCLK + RGB888 + VSYNC + HSYNC + DATAEN) is supplied by DVDD33 (PIN45 and PIN59). Thus, ZA7783 is able to bridge AP or BB with 1.8V IO to RGB Panel with 3.3V IO. Besides, an embedded LDO converts 3.3V to 1.2V to supply the chip's internal digital logic. In addition, an embedded POR implements a power on reset to the whole chip.

2 Target Applications

Tablet PC

3 Feature Description

MIPI DSI RX Interface

- Compliant to MIPI DSI V1.01 and MIPI D-PHY V1.00
- 1 Clock Lane + 4 Data Lanes
- Data rate up to 600Mbps per data lane (300MHz high-speed clock on clock lane)
- 2.4Gbps bandwidth on four data lanes in total, giving a display resolution up to 1366x768 24bpp @ 60fps
- Only support MIPI DSI Video Mode (Non-Burst Mode with Sync Pulses) and all lanes are unidirectional from the host chip to the bridge chip

- The host chip is required to provide continuous high-speed clock
- Only support using all of the four data lanes, in other words, using part of them is not supported
- Support multiple packets within a single high-speed transmission
- Ignore received virtual channel field
- Only the following packet data types are supported:
  - 6'h01=Sync Event, V Sync Start (Short)
  - 6'h11=Sync Event, V Sync End (Short)
  - 6'h21=Sync Event, H Sync Start (Short)
  - 6'h31=Sync Event, H Sync End (Short)
  - 6'h08=End of Transimission packet (EoTp) (Short)
  - 6'h09=Null Packet, no data (Long)
  - 6'h19=Blanking Packet, no data (Long)
  - 6'h2E=Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format (Long)
  - 6'h3E=Packed Pixel Stream, 24-bit RGB, 8-8-8 Format (Long)

  The other packet data types cannot be handled and must not be sent to ZA7783!
- Ignore received ecc field
- Ignore received checksum field
- RGB565 Packed Pixel Stream and RGB666 Packed Pixel Stream are not supported
- For a data lane, the connection of Dp/Dn can be exchanged
- The order of the four data lanes can be configured
- Dither function for converting RGB888 to RGB666

LVDS TX Interface

- Compliant to LVDS Spec
- 1 Clock Lane + 4 Data Lanes
- Support RGB888 and RGB666
  - RGB888: 1 Clock Lane + 4 Data Lanes
  - RGB666: 1 Clock Lane + 3 Data Lanes
- Support NS Mode and JEIDA Mode
- The polarity of VSYNC/HSYNC/DATAEN can be configured
- For a data lane, the connection of Dp/Dn can be exchanged
- The order of the four data lanes can be configured
- Dither function for converting RGB888 to RGB666

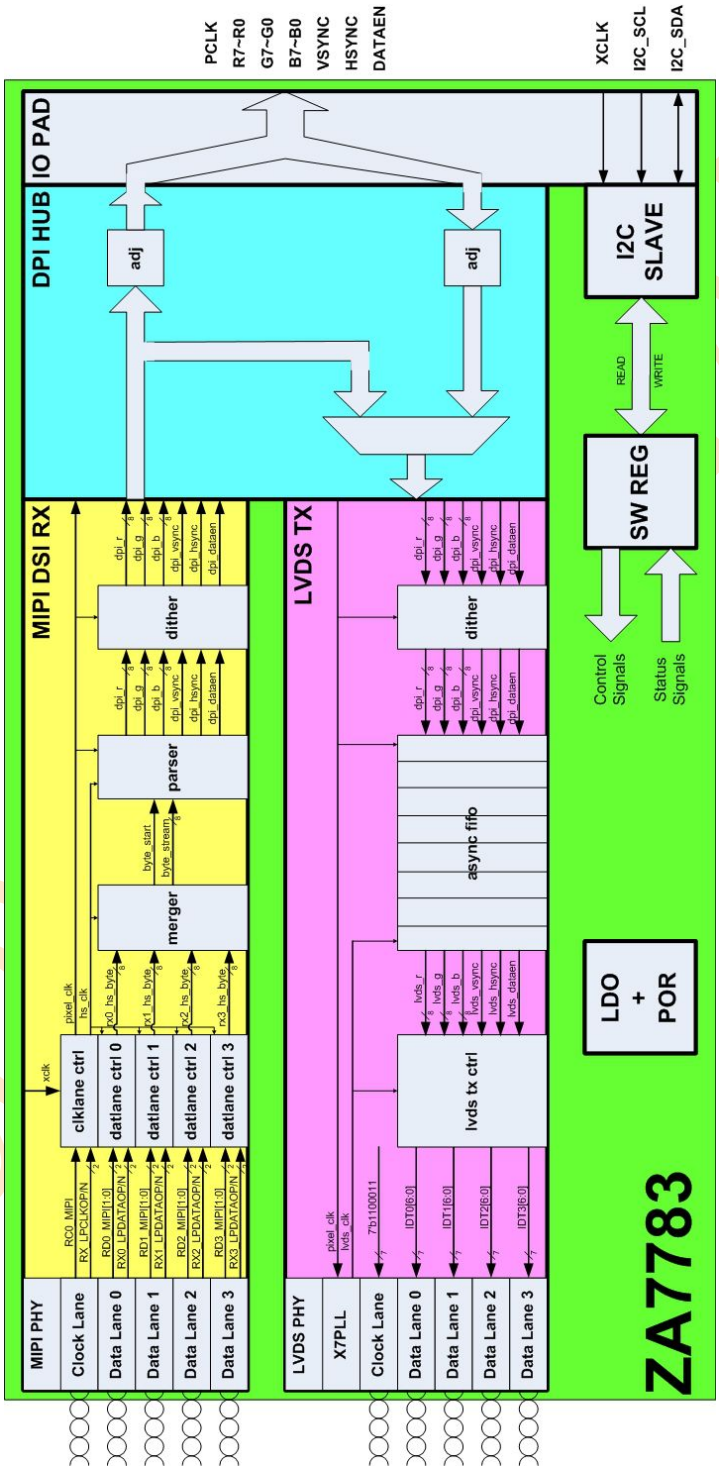
DPI TX/RX Interface

- PCLK + RGB888 + VSYNC + HSYNC + DATAEN
- The edge of PCLK can be configured
- The polarity of VSYNC/HSYNC/DATAEN can be configured

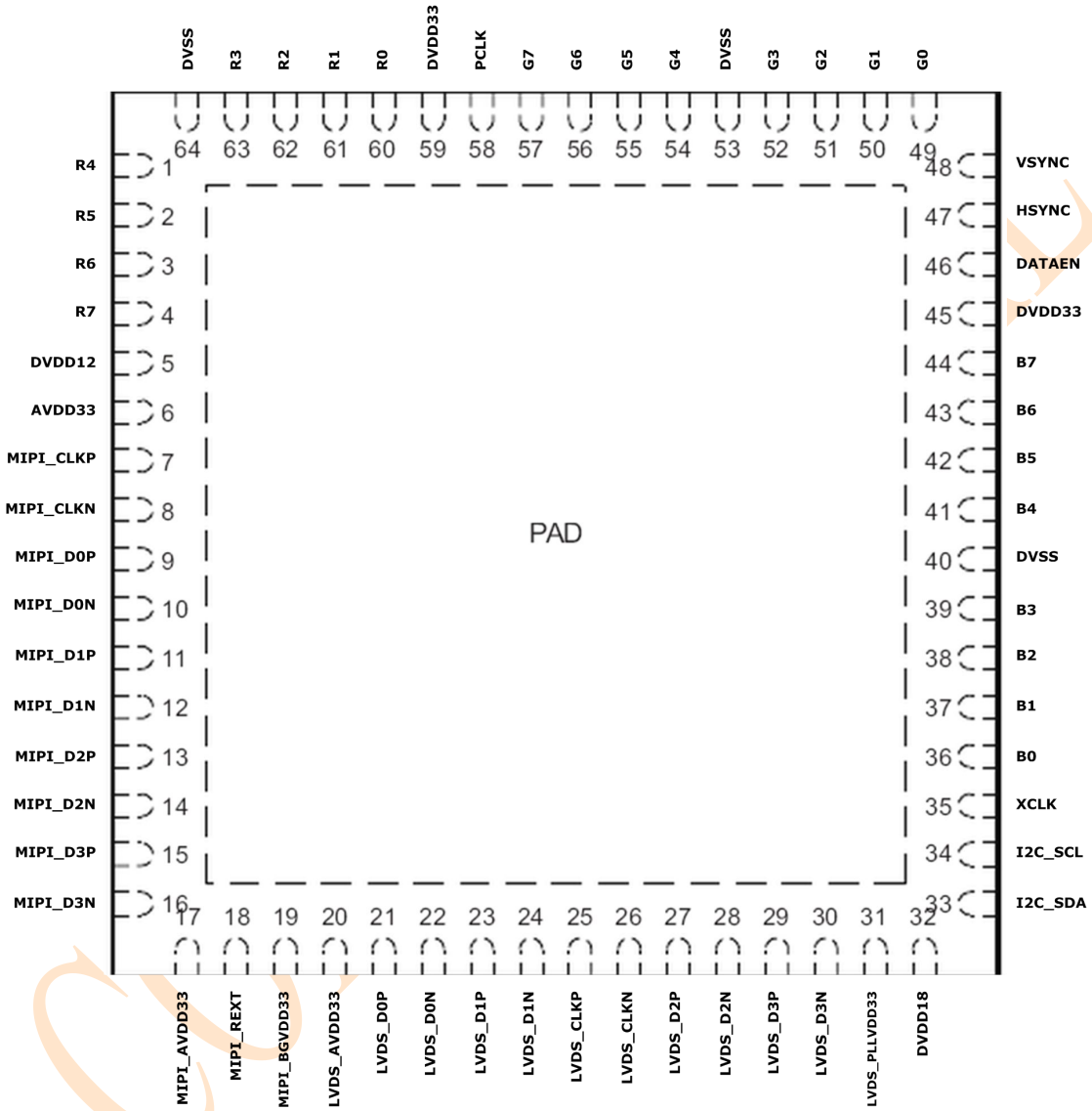
I2C Interface

- An external clock XCLK should be provided (e.g. 26MHz)
- Up to 400Kbps
- I2C Slave ID is 0x37

4 Functional Block Diagram



5 Pin Configuration



No.	Name	Description
1	R4	DPI R[7:4]
2	R5	
3	R6	
4	R7	
5	DVDD12	LDO 1.2V Output (connected to **0.47uF** ceramic cap) Digital Core 1.2V Power Supply
6	AVDD33	LDO 3.3V Power Supply
7	MIPI_CLKP	MIPI DSI RX Clock Lane

8	MIPI_CLKN	
9	MIPI_D0P	MIPI DSI RX Data Lane 0~3
10	MIPI_D0N	
11	MIPI_D1P	
12	MIPI_D1N	
13	MIPI_D2P	
14	MIPI_D2N	
15	MIPI_D3P	
16	MIPI_D3N	
17	MIPI_AVDD33	MIPI PHY 3.3V Power Supply
18	MIPI_REXT	Tie a 24KOhm resistor (1% accuracy) to analog ground
19	MIPI_BGVDD33	MIPI PHY 3.3V BandGap Supply
20	LVDS_AVDD33	LVDS TX 3.3V Power Supply
21	LVDS_D0P	LVDS TX Data Lane 0
22	LVDS_D0N	
23	LVDS_D1P	LVDS TX Data Lane 1
24	LVDS_D1N	
25	LVDS_CLKP	LVDS TX Clock Lane
26	LVDS_CLKN	
27	LVDS_D2P	LVDS TX Data Lane 2
28	LVDS_D2N	
29	LVDS_D3P	LVDS TX Data Lane 3
30	LVDS_D3N	
31	LVDS_PLLVDD33	LVDS TX 3.3V PLL Supply
32	DVDD18	Digital IO 1.8V Power Supply This power supply is for XCLK/I2C_SCL/I2C_SDA.
33	I2C_SDA	I2C Serial Data Line
34	I2C_SCL	I2C Serial Clock Line
35	XCLK	XCLK Input (e.g. 26MHz)
36	B0	DPI B[3:0]
37	B1	
38	B2	
39	B3	
40	DVSS	Digital Ground
41	B4	DPI B[7:4]
42	B5	
43	B6	
44	B7	
45	DVDD33	Digital IO 3.3V Power Supply This power supply is for DPI IF, including PCLK, R7~0, G7~0, B7~0, VSYNC, HSYNC, and DATAEN.
46	DATAEN	DPI Data Enable
47	HSYNC	DPI HSYNC
48	VSYNC	DPI VSYNC
49	G0	DPI G[3:0]
50	G1	
51	G2	
52	G3	
53	DVSS	Digital Ground
54	G4	DPI G[7:4]
55	G5	

56	G6	
57	G7	
58	PCLK	DPI Pixel Clock
59	DVDD33	Digital IO 3.3V Power Supply This power supply is for DPI IF, including PCLK, R7~0, G7~0, B7~0, VSYNC, HSYNC, and DATAEN.
60	R0	DPI R[3:0]
61	R1	
62	R2	
63	R3	
64	DVSS	Digital Ground
EP(65)	AVSS	Analog Ground for LDO, MIPI PHY, and LVDS TX

6 Electrical Parameters

ABSOLUTE MAXIMUM RATINGS

		MIN	MAX	UNIT
Supply Voltage Range	AVDD33	-0.3	+4	V
	MIPI_AVDD33	-0.3	+4	V
	MIPI_BGVDD33	-0.3	+4	V
	LVDS_AVDD33	-0.3	+4	V
	LVDS_PLLVDD33	-0.3	+4	V
	DVDD33	-0.3	+4	V
	DVDD18	-0.3	+4	V
Input Voltage Range	CMOS Input Terminals	-0.3	DVDD+0.3(1)	V
	DSI Input Terminals	-0.4	+1.4	V
Storage Temperature	Ts	-65	105	℃
Electrostatic Discharge	Human Body Model		+/-3	KV
	Charged-Device Model		+/-500	V

(1) For XCLK, I2C_SCL, and I2C_SDA, DVDD means the voltage level of DVDD18. For the other digital IO, DVDD means the voltage level of DVDD33.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
AVDD33	LDO 3.3V Power Supply	3.0	3.3	3.6	V
MIPI_AVDD33	MIPI 3.3V Power Supply	3.0	3.3	3.6	V
MIPI_BGVDD33	MIPI BandGap 3.3V Power Supply	3.0	3.3	3.6	V
LVDS_AVDD33	LVDS 3.3V Power Supply	3.0	3.3	3.6	V
LVDS_PLLVDD33	LVDS PLL 3.3V Power Supply	3.0	3.3	3.6	V
DVDD33	Digital IO Power Supply	3.0	3.3	3.6	V
		1.62	1.8	1.98	V
DVDD18	Digital IO Power Supply	3.0	3.3	3.6	V
		1.62	1.8	1.98	V
V_{PSN}	Supply Noise on Any Power Pin			0.05	V
T_A	Operating Temperature	-40		85	℃
T_{CASE}	Case Temperature			85	℃
V_{DSI_PIN}	DSI Input Pin Voltage Range	-50		1350	mV
F_{I2C}	I2C Input Frequency			400	KHz
F_{HS_CLK}	DSI HS Clock Input Frequency			300	MHz
T_{setup}	DSI HS Data to Clock Setup Time	0.15			UI(1)
T_{hold}	DSI HS Data to Clock Hold Time	0.15			UI
Z_L	LVDS Output Differential Impedance	90		132	Ohm

(1) The unit interval (UI) is one half of the period of the HS clock.

ELECTRICAL CHARACTERISTICS

		MIN	TYP	MAX	UNIT
V_{IL}	Low-level Control Signal Input Voltage			0.3*DVDD	V
V_{IH}	High-level Control Signal Input Voltage	0.7*DVDD			V
V_{OH}	High-level Output Voltage	0.8*DVDD			V
V_{OL}	Low-level Output Voltage			0.3	V
I_{OZ}	High-impedance Output Current			+/-10	uA
I_{CC}	Device Active Current		67(1)		mA

I_{STDBY}	Device Standby Current			500(2)	uA

(1) Test Condition:
1024x768 24-bit LCD Panel @ PCLK=65MHz
Enable MIPI DSI RX with 1 Clock Lane and 4 Data Lanes, DSI HS Clock=195MHz
Enable LVDS TX with 1 Clock Lane and 4 Data Lanes, LVDS Clock=65MHz
Enable DPI TX, PCLK=65MHz

(2) Test Condition:
ZA7783 is powered but all functions are disabled by I2C configuration.

XCLK

		MIN	TYP	MAX	UNIT
F_{XCLK}	XCLK Frequency	10		30	MHz
T_{rise}/T_{fall}	XCLK Rise/Fall Time			5	ns
Duty	XCLK Duty Cycle	30	50	70	%

MIPI DSI RX

		MIN	TYP	MAX	UNIT
V_{IH-LP}	LP Receiver Input High Threshold	880			mV
V_{IL-LP}	LP Receiver Input Low Threshold			550	mV
$\|V_{ID}\|$	HS Differential Input Voltage	70		270	mV
$\|V_{IDT}\|$	HS Differential Input Voltage Threshold			50	mV
V_{CM-HS}	HS Common Mode Voltage: Steady-State	70		330	mV
$\triangle V_{CM-HS}$	HS Common Mode Peak-to-Peak Variation			100	mV
V_{IH-HS}	HS Single-Ended Input High Voltage			460	mV
V_{IL-HS}	HS Single-Ended Input Low Voltage	-40			mV
$R_{DIFF-HS}$	HS Mode Differential Input Impedance	80		125	Ohm

ULPS (Ultra-Low Power State) is not supported.

LVDS TX

		MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Steady-State Differential Output Voltage	220	310	350	mV
$\triangle\|V_{OD}\|$	Change in Steady-State Differential Output Voltage between Opposite Binary States	10	15	20	mV
$V_{OC(SS)}$	Steady State Common Mode Output Voltage	1.15	1.25	1.35	V
$V_{OC(PP)}$	Peak-to-Peak Common Mode Output Voltage	50	60	80	mV
R_{LVDS_DIS}	Pull-Down Resistance for Disabled LVDS Outputs	---	---	---	KOhm

DPI TX/RX

		MIN	TYP	MAX	UNIT
F_{PCLK}	PCLK Frequency	20		100	MHz
T_{PCLK}	PCLK Period	10		50	ns
T_{setup}	VSYNC, HSYNC, DATAEN, RGB Setup Time in DPI RX Mode	2			ns
T_{hold}	VSYNC, HSYNC, DATAEN, RGB Hold Time in DPI RX Mode	2			ns

SWITCHING CHARACTERISTICS

		MIN	TYP	MAX	UNIT
	MIPI DSI RX				
t_{GS}	DSI LP Glitch Suppression Pulse Width			300	ps
	LVDS TX				
t_c	Output Clock Period	10		50	ns
t_w	High-level Output Clock Pulse Duration	$4/7*t_c$ - 0.1	$4/7*t_c$	$4/7*t_c$ + 0.1	ns
t_0	Delay Time, CLK ↑ to 1st serial bit position	-0.2	0	+0.2	ns
t_1	Delay Time, CLK ↑ to 2nd serial bit position	$1/7*t_c$ - 0.2	$1/7*t_c$	$1/7*t_c$ + 0.2	ns
t_2	Delay Time, CLK ↑ to 3rd serial bit position	$2/7*t_c$ - 0.2	$2/7*t_c$	$2/7*t_c$ + 0.2	ns
t_3	Delay Time, CLK ↑ to 4th serial bit position	$3/7*t_c$ - 0.2	$3/7*t_c$	$3/7*t_c$ + 0.2	ns
t_4	Delay Time, CLK ↑ to 5th serial bit position	$4/7*t_c$ - 0.2	$4/7*t_c$	$4/7*t_c$ + 0.2	ns

t_5	Delay Time, CLK ↑ to 6th serial bit position	5/7*t_c - 0.2	5/7*t_c	5/7*t_c + 0.2	ns
t_6	Delay Time, CLK ↑ to 7th serial bit position	6/7*t_c - 0.2	6/7*t_c	6/7*t_c + 0.2	ns
t_r	Differential Output Rise Time	189	199	209	ps
t_f	Differential Output Fall Time	186	196	208	ps
LDO + POR					
$T_{LDO-SETUP}$	LDO Setup Time to Output 1.2V			100	us
$T_{POR-DELAY}$	POR Delay Time to Release Internal Reset after 1.2V Setup		2		ms

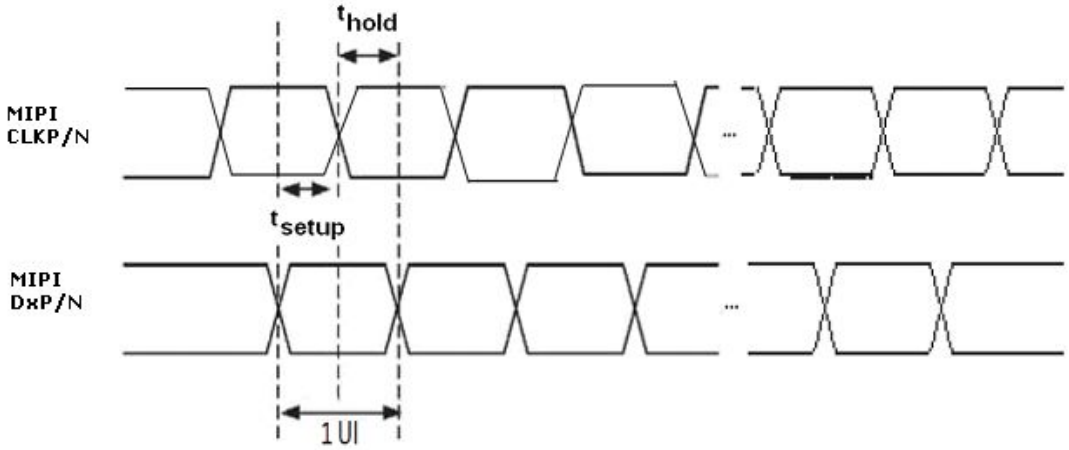


Figure 6-1 MIPI DSI HS Mode Receiver Timing Definitions

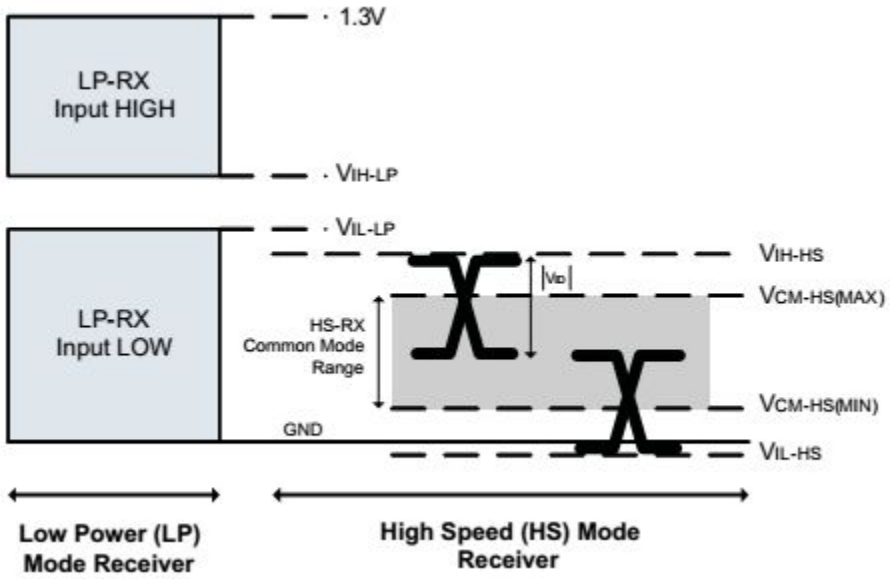


Figure 6-2 MIPI DSI Receiver Voltage Definitions

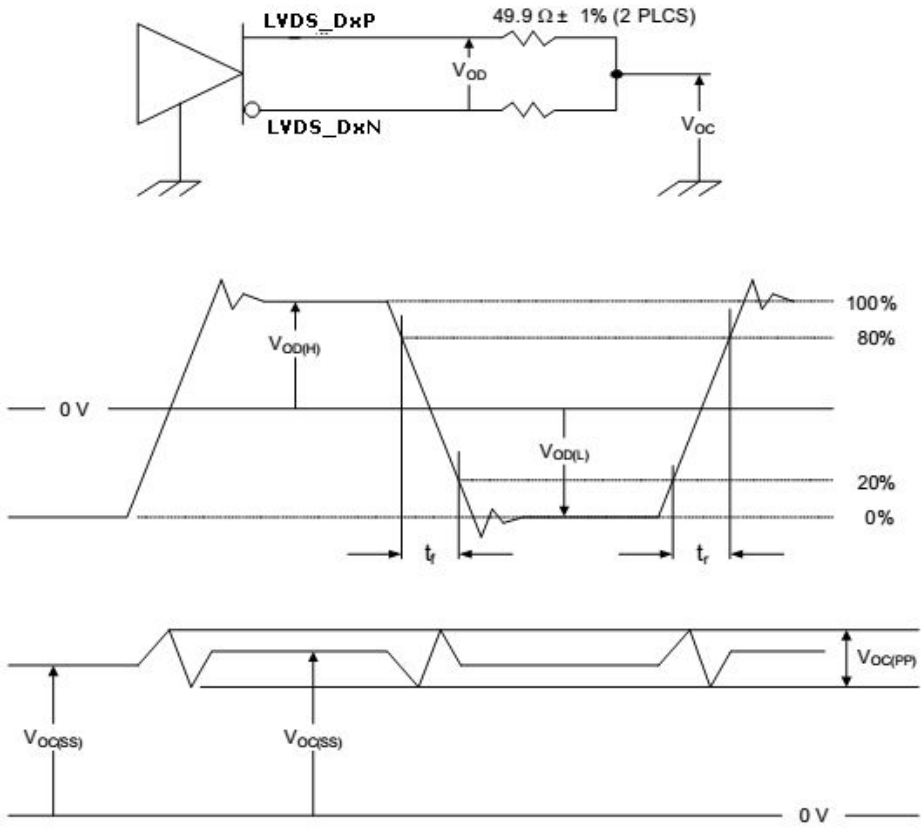


Figure 6-3 Test Load and Voltage Definitions for LVDS Outputs

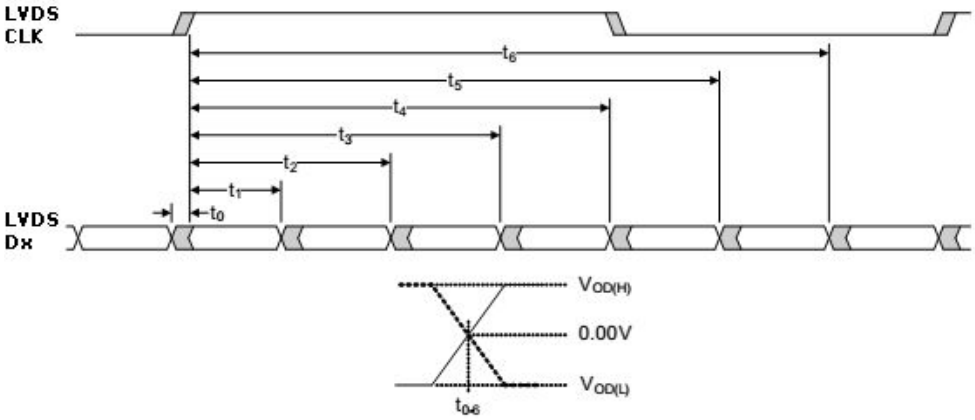


Figure 6-4 LVDS Timing Definitions

7 Typical Application Circuit

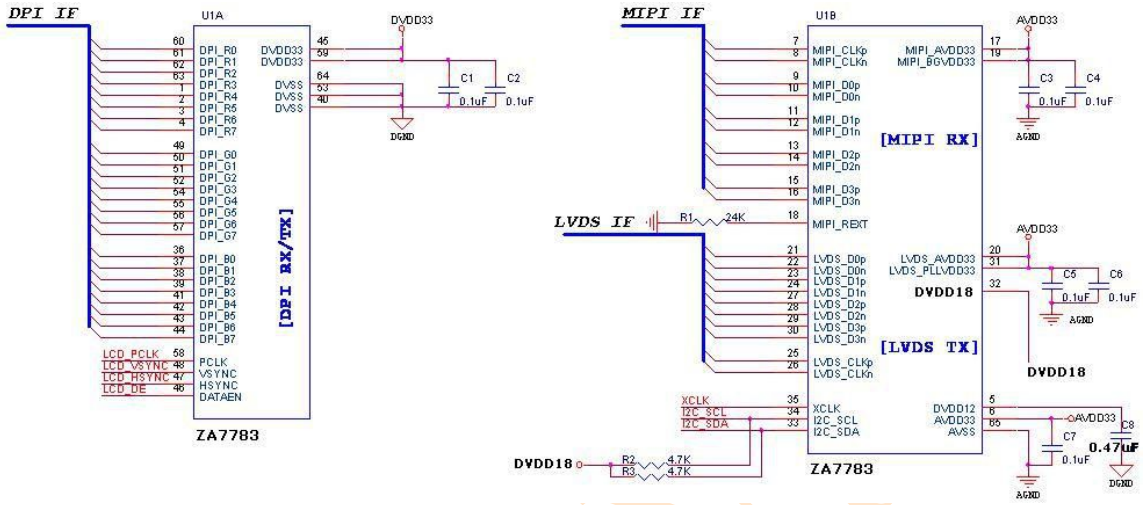


Figure 7-1 Typical Application Circuit

7.1 MIPI => LVDS Reference Design

MIPI => LVDS Reference Design derives from Typical Application Circuit:

1. ZA7783 DPI IF is not used in this scenario. Leave the related pins not connected. That is, PCLK, VSYNC, HSYNC, DATAEN, R[7:0], G[7:0], and B[7:0] are left open.

2. Connect MIPI IF of the host chip and ZA7783 in a straight way. The MIPI IF includes 1 clock lane and 4 data lanes. Just route MIPI_CLKp to MIPI_CLKp, MIPI_CLKn to MIPI_CLKn, MIPI_D0p to MIPI_D0p, MIPI_D0n to MIPI_D0n, and so on.

3. Connect LVDS IF of ZA7783 and LVDS Panel in a straight way. The LVDS IF includes 1 clock lane and 4 data lanes for 24-bit LVDS Panel, or 3 data lanes for 18-bit LVDS Panel. Just route LVDS_CLKp to LVDS_CLKp, LVDS_CLKn to LVDS_CLKn, LVDS_D0p to LVDS_D0p, LVDS_D0n to LVDS_D0n, and so on. For 18-bit LVDS Panel, LVDS_D3p and LVDS_D3n are not used and left open.

4. The host chip should provide a 10~30MHz clock to ZA7783's XCLK pin. This clock is required during I2C configuration and normal display. When the host chip shuts down LVDS Panel and switches to sleep mode, this clock may be stopped, so as to minimize power consumption.

5. The host chip uses its I2C Master IF to connect ZA7783's I2C Slave IF to do configuration.

6. XCLK, I2C_SCL, and I2C_SDA of ZA7783 are powered by DVDD18 (PIN32). The IO voltage level of these pins on both sides (the host chip and ZA7783) should be consistent.

7. LVDS Panel may have some control pins, such as LCD_EN, LCD_RSTN, LCD_PWM, etc. These pins should be controlled directly by the host chip. ZA7783 does nothing to these control pins.

7.2 MIPI => RGB Reference Design

MIPI => RGB Reference Design derives from Typical Application Circuit:

1. ZA7783 LVDS IF is not used in this scenario. Leave these pins open.

2. Connect MIPI IF of the host chip and ZA7783 in a straight way. The MIPI IF includes 1 clock lane and 4 data lanes. Just route MIPI_CLKp to MIPI_CLKp, MIPI_CLKn to MIPI_CLKn, MIPI_D0p to MIPI_D0p, MIPI_D0n to MIPI_D0n, and so on.

3. Connect DPI IF of ZA7783 and RGB Panel in a straight way. For 18-bit RGB Panel, route R[7:2], G[7:2], and B[7:2] to the panel, while leave R[1:0], G[1:0], and B[1:0] open.

4. The host chip should provide a 10~30MHz clock to ZA7783's XCLK pin. This clock is required during I2C configuration and normal display. When the host chip shuts down RGB Panel and switches to sleep mode, this clock may be stopped, so as to minimize power consumption.

5. The host chip uses its I2C Master IF to connect ZA7783's I2C Slave IF to do configuration.

6. XCLK, I2C_SCL, and I2C_SDA of ZA7783 are powered by DVDD18 (PIN32). The IO voltage level of these pins on both sides (the host chip and ZA7783) should be consistent.

7. RGB Panel may have some control pins, such as LCD_EN, LCD_RSTN, LCD_PWM, etc. These pins should be controlled directly by the host chip. ZA7783 does nothing to these control pins.

7.3 RGB => LVDS Reference Design

RGB => LVDS Reference Design derives from Typical Application Circuit:

1. ZA7783 MIPI IF is not used in this scenario. Leave these pins open.

2. Connect DPI IF of the host chip and ZA7783 in a straight way. If the host chip only outputs 18-bit DPI IF, route them to R[7:2], G[7:2], and B[7:2] of ZA7783, while R[1:0], G[1:0], and B[1:0] of ZA7783 are left open.

3. Connect LVDS IF of ZA7783 and LVDS Panel in a straight way. The LVDS IF includes 1 clock lane and 4 data lanes for 24-bit LVDS Panel, or 3 data lanes for 18-bit LVDS Panel. Just route LVDS_CLKp to LVDS_CLKp, LVDS_CLKn to LVDS_CLKn, LVDS_D0p to LVDS_D0p, LVDS_D0n to LVDS_D0n, and so on. For 18-bit LVDS Panel, LVDS_D3p and LVDS_D3n are not used and left open.

4. The host chip should provide a 10~30MHz clock to ZA7783's XCLK pin. This clock is required during I2C configuration and normal display. When the host chip shuts down LVDS Panel and switches to sleep mode, this clock may be stopped, so as to minimize power consumption.

5. The host chip uses its I2C Master IF to connect ZA7783's I2C Slave IF to do configuration.

6. XCLK, I2C_SCL, and I2C_SDA of ZA7783 are powered by DVDD18 (PIN32). The IO voltage level of these pins on both sides (the host chip and ZA7783) should be consistent.

7. LVDS Panel may have some control pins, such as LCD_EN, LCD_RSTN, LCD_PWM, etc. These pins should be controlled directly by the host chip. ZA7783 does nothing to these control pins.

7.4 FAQ

7.4.1 AVDD33 and DVDD33

AVDD33 and DVDD33 can be supplied with a single 3.3V LDO. Place decoupling capacitance close to each power supply pin to decrease noise, as Typical Application Circuit shows.

7.4.2 DVDD33 and DVDD18

PCLK, VSYNC, HSYNC, DATAEN, and RGB888 are powered by DVDD33

(PIN45 and PIN59), while XCLK, I2C_SCL, and I2C_SDA are powered by DVDD18 (PIN32). Although DVDD33 and DVDD18 are named with the voltage level, in fact both of them can be supplied with 1.8V~3.3V power. For example, users can supply 1.8V to DVDD33, or 3.3V to DVDD18.

7.4.3 Power-Up Sequence

DVDD18 should be supplied first, and then AVDD33 and DVDD33.

7.4.4 Power-Down Sequence

The sequence of removing AVDD33, DVDD33, and DVDD18 is unconstrained.

7.4.5 PCB Layout of MIPI/LVDS

MIPI and LVDS include high-speed differential pairs. When routing these signals, users should follow the general and common rules for differential pairs. Besides, there is no more special requirement.

7.4.6 XCLK Requirement

ZA7783 XCLK is supplied by the host chip. The frequency should be 10~30MHz. **If DVDD18 is 1.8V, the amplitude of XCLK should also be 1.8V (waveform with low-level voltage 0V and high-level voltage 1.8V).**

Please carefully check this amplitude requirement. Make sure that you have selected a correct clock output from the host chip. Especially note that some host chip clock pins only output 500mV Vpp waveform or so, thus such clock outputs cannot be used as the source of ZA7783 XCLK.

8 Software Register Description

8.1 Software Register Overview

The host chip (AP or BB) may access ZA7783's software registers through I2C interface. The 7-bit I2C Slave ID is 0x37, and the following table lists all the software registers.

Table 8-1 Software Register Overview

Addr.	Name	Attr.	Default	Description
0x00	GLOBAL_SW_RSTN	RW	0x00	Global Software Reset
0x08	PADO_DPI_OEN	RW	0x01	DPI Related PAD Output Enable
0x10	MIPI_PD	RW	0x3F	MIPI PHY Power Down Control
0x11	MIPI_DATLANE_RSTN	RW	0x00	MIPI PHY Data Lane Reset Control
0x12	MIPI_DATLANE_PN_EXCH	RW	0x00	MIPI PHY Data Lane Dp/Dn Swap
0x13	MIPI_DATLANE_ORDER	RW	0xE4	MIPI PHY Data Lane Reorder
0x14	TIME_CLK_SETTLE	RW	0x02	MIPI PHY Clock Lane Timing
0x15	TIME_D_TERM_EN	RW	0x02	MIPI PHY Data Lane Timing 1
0x16	TIME_HS_SETTLE	RW	0x24	MIPI PHY Data Lane Timing 2
0x17	MIPI_DITHER_EN	RW	0x00	MIPI DSI RX Dither Enable
0x18	MIPI_DLY_TRIM	RW	0x21	MIPI DSI RX Delay Trim
0x20	LVDS_PD	RW	0x3F	LVDS PHY Power Down Control
0x21	X7PLL_PD	RW	0xFF	X7PLL Power Down Control
0x22	LVDS_RSTN	RW	0x00	LVDS PHY Reset Control
0x23	LVDS_FIFO_EN	RW	0x00	LVDS TX Enable
0x24	LVDS_FORMAT	RW	0x00	LVDS TX Format
0x25	LVDS_DATLANE_PN_EXCH	RW	0x00	LVDS PHY Data Lane Dp/Dn Swap
0x26	LVDS_DATLANE_ORDER	RW	0xE4	LVDS PHY Data Lane Reorder
0x27	LVDS_DITHER_EN	RW	0x00	LVDS TX Dither Enable
0x28	LVDS_SSC	RW	0x28	LVDS PHY SSC Control
0x29	LVDS_PHY	RW	0x01	LVDS PHY Trim
0x2A	X7PLL_ADJ1	RW	0x00	X7PLL Adjustment 1
0x2B	X7PLL_ADJ2	RW	0x01	X7PLL Adjustment 2
0x2C	X7PLL_ADJ3	RW	0x0E	X7PLL Adjustment 3
0x2D	X7PLL_ADJ4	RW	0x00	X7PLL Adjustment 4
0x2E	X7PLL_ADJ5	RW	0x18	X7PLL Adjustment 5
0x2F	X7PLL_ADJ6	RW	0x02	X7PLL Adjustment 6
0x30	X7PLL_ADJ7	RW	0x02	X7PLL Adjustment 7
0x31	LVDS_TEST	RW	0x00	LVDS PHY Test Control
0x32	LVDS_TDI	RW	0x63	LVDS PHY Test Data In
0x33	LVDS_TDO	RO	--	LVDS PHY Test Data Out
0x34	LVDS_TSO	RO	--	LVDS PHY Test Result
0x35	X7PLL_LOCK	RO	0x00	X7PLL Lock Status
0x40	PADI_DPI_ADJ	RW	0x00	Adjust DPI from PAD inputs
0x41	PADO_DPI_ADJ	RW	0x00	Adjust DPI to PAD outputs
0x42	LVDS_SOURCE	RW	0x00	LVDS TX Source DPI Selection

8.2 Software Register Description

8.2.1 GLOBAL_SW_RSTN

Global Software Reset

ADDR=0x00 (RW)

Bits	Field	Default	Description
[7:1]	Reserved		
[0]	sw_rstn	1'b0	reset all digital logic except i2c slave and software register, low active

8.2.2 PADO_DPI_OEN

DPI Related PAD Output Enable
DPI Related PAD: PCLK, R7~R0, G7~G0, B7~B0, VSYNC, HSYNC, DATAEN

ADDR=0x08 (RW)

Bits	Field	Default	Description
[7:3]	Reserved		
[2]	debug_mode2	1'b0	switch to debug mode2: R0=CK_FIFO from LVDS PHY G0=LOCK from LVDS PHY B0=TPSO from LVDS PHY
[1]	debug_mode	1'b0	switch to debug mode: PCLK = RC0_MIPI from MIPI D-PHY VSYNC = RX_LPCLKOP from MIPI D-PHY HSYNC = RX_LPCLKON from MIPI D-PHY G[3:0] = {RX0_LPDATAOP, RX0_LPDATAON, RD0_MIPI[1:0]} from MIPI D-PHY G[7:4] = {RX1_LPDATAOP, RX1_LPDATAON, RD1_MIPI[1:0]} from MIPI D-PHY B[3:0] = {RX2_LPDATAOP, RX2_LPDATAON, RD2_MIPI[1:0]} from MIPI D-PHY B[7:4] = {RX3_LPDATAOP, RX3_LPDATAON, RD3_MIPI[1:0]} from MIPI D-PHY R[7:0] = byte_stream[7:0] after mipi dsi rx merger DATAEN = byte_start indicator after mipi dsi rx merger
[0]	pado_dpi_oen	1'b1	low active

8.2.3 MIPI_PD

MIPI D-PHY Power Down Control

ADDR=0x10 (RW)

Bits	Field	Default	Description
[7:6]	Reserved		
[5]	pd_bias	1'b1	power down bias, high active
[4]	rx_clkpd	1'b1	power down clock lane, high active
[3]	rx3_datapd	1'b1	power down data lane 3, high active
[2]	rx2_datapd	1'b1	power down data lane 2, high active
[1]	rx1_datapd	1'b1	power down data lane 1, high active
[0]	rx0_datapd	1'b1	power down data lane 0, high active

8.2.4 MIPI_DATLANE_RSTN

MIPI D-PHY Data Lane Reset Control

ADDR=0x11 (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3]	rx3_resetn	1'b0	reset data lane 3, low active
[2]	rx2_resetn	1'b0	reset data lane 2, low active
[1]	rx1_resetn	1'b0	reset data lane 1, low active
[0]	rx0_resetn	1'b0	reset data lane 0, low active

8.2.5 MIPI_DATLANE_PN_EXCH

MIPI D-PHY Data Lane Dp/Dn Exchange

ADDR=0x12 (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3]	rx3_pn_exch	1'b0	exchange data lane 3 Dp/Dn, high active
[2]	rx2_pn_exch	1'b0	exchange data lane 2 Dp/Dn, high active
[1]	rx1_pn_exch	1'b0	exchange data lane 1 Dp/Dn, high active
[0]	rx0_pn_exch	1'b0	exchange data lane 0 Dp/Dn, high active

8.2.6 MIPI_DATLANE_ORDER

MIPI D-PHY Data Lane Reorder

ADDR=0x13 (RW)

Bits	Field	Default	Description
[7:6]	sel_4th_datlane	2'h3	the 4th data lane is from 2'h0: data lane 0 2'h1: data lane 1 2'h2: data lane 2 2'h3: data lane 3
[5:4]	sel_3rd_datlane	2'h2	the 3rd data lane is from 2'h0: data lane 0 2'h1: data lane 1 2'h2: data lane 2 2'h3: data lane 3
[3:2]	sel_2nd_datlane	2'h1	the 2nd data lane is from 2'h0: data lane 0 2'h1: data lane 1 2'h2: data lane 2 2'h3: data lane 3
[1:0]	sel_1st_datlane	2'h0	the 1st data lane is from 2'h0: data lane 0 2'h1: data lane 1 2'h2: data lane 2 2'h3: data lane 3

8.2.7 TIME_CLK_SETTLE

MIPI D-PHY Clock Lane Timing Parameter: TIME_CLK_SETTLE

ADDR=0x14 (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3:0]	time_clk_settle	4'h2	time interval during which the HS receiver shall ignore any Clock Lane HS transitions, starting from the beginning of LP-00 state. this time interval is counted based on xclk, and should be within [95ns, 300ns]

8.2.8 TIME_D_TERM_EN

MIPI D-PHY Data Lane Timing Parameter: TIME_D_TERM_EN

ADDR=0x15 (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3:0]	time_d_term_en	4'h2	time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses Vil,max. this time interval is counted based on hs_clk (high-speed clock received from Clock Lane), and should be within [time for Dn to reach Vterm-en, 35ns+4*UI] (UI=hs_clk/2).

8.2.9 TIME_HS_SETTLE

MIPI D-PHY Data Lane Timing Parameter: TIME_HS_SETTLE

ADDR=0x16 (RW)

Bits	Field	Default	Description
[7:6]	Reserved		
[5:0]	time_hs_settle	6'h24	time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of LP-00 state. this time interval is counted based on hs_clk (high-speed clock received from Clock Lane), and should be within [85ns+6*UI, 145ns+10*UI] (UI=hs_clk/2).

8.2.10 MIPI_DITHER_EN

MIPI DSI RX RGB888->RGB666 Dither Enable

ADDR=0x17 (RW)

Bits	Field	Default	Description
[7:1]	Reserved		
[0]	mipi_dither_en	1'b0	high active

8.2.11 MIPI_DLY_TRIM

MIPI DSI RX HSA and HBP Delay Trim

ADDR=0x18 (RW)

Bits	Field	Default	Description
[7:4]	hbp_delay	4'b0010	please refer to timing diagram. one and only one bit should be 1'b1. hbp_delay[0]=1'b1: no delay hbp_delay[1]=1'b1: 3-byte delay

			hbp_delay[2]=1'b1: 6-byte delay hbp_delay[3]=1'b1: 9-byte delay
[3:0]	hsa_delay	4'b0001	please refer to timing diagram. one and only one bit should be 1'b1. hsa_delay[0]=1'b1: no delay hsa_delay[1]=1'b1: 3-byte delay hsa_delay[2]=1'b1: 6-byte delay hsa_delay[3]=1'b1: 9-byte delay

8.2.12 LVDS_PD

LVDS PHY Power Down Control

ADDR=0x20 (RW)

Bits	Field	Default	Description
[7:6]	Reserved		
[5]	pd_bg	1'b1	power down bandgap, high active
[4:0]	pd	5'b11111	pd[4]: power down clock lane, high active pd[3]: power down data lane 3, high active pd[2]: power down data lane 2, high active pd[1]: power down data lane 1, high active pd[0]: power down data lane 0, high active

8.2.13 X7PLL_PD

X7PLL Power Down Control
power down X7PLL submodules, high active

ADDR=0x21 (RW)

Bits	Field	Default	Description
[7]	pd_dt	1'b1	high active
[6]	pd_vco	1'b1	high active
[5]	pd_ib	1'b1	high active
[4]	pd_capmul	1'b1	high active
[3]	pd_chp_op	1'b1	high active
[2]	pd_chp	1'b1	high active
[1]	pd_pfd	1'b1	high active
[0]	pd_reg	1'b1	high active

8.2.14 LVDS_RSTN

LVDS PHY Reset Control

ADDR=0x22 (RW)

Bits	Field	Default	Description
[7:2]	Reserved		
[1]	rb_lock	1'b0	reset lock detector, low active
[0]	rb	1'b0	reset digital logic, low active

8.2.15 LVDS_FIFO_EN

LVDS TX Enable

ADDR=0x23 (RW)

Bits	Field	Default	Description
[7:1]	Reserved		
[0]	fifo_en	1'b0	enable the internal fifo to deliver DPI interface to LVDS transmitter, that is, start LVDS transmission, high active

8.2.16 LVDS_FORMAT

LVDS TX Format

ADDR=0x24 (RW)

Bits	Field	Default	Description
[7:5]	Reserved		
[4]	dataen_polarity	1'b0	LVDS TX sends DATAEN as 1'b0: high active 1'b1: low active
[3]	hsync_polarity	1'b0	LVDS TX sends HSYNC as 1'b0: high active 1'b1: low active
[2]	vsync_polarity	1'b0	LVDS TX sends VSYNC as 1'b0: high active 1'b1: low active
[1]	lvds_mode	1'b0	LVDS TX sends DPI interface as 1'b0: NS Mode 1'b1: JEIDA Mode
[0]	dpi_format	1'b0	LVDS TX sends DPI interface as 1'b0: RGB888, using 1 clock lane and 4 data lanes 1'b1: RGB666, using 1 clock lane and 3 data lanes

8.2.17 LVDS_DATLANE_PN_EXCH

LVDS PHY Data Lane Dp/Dn Exchange

ADDR=0x25 (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3]	tx3_pn_exch	1'b0	exchange data lane 3 Dp/Dn, high active
[2]	tx2_pn_exch	1'b0	exchange data lane 2 Dp/Dn, high active
[1]	tx1_pn_exch	1'b0	exchange data lane 1 Dp/Dn, high active
[0]	tx0_pn_exch	1'b0	exchange data lane 0 Dp/Dn, high active

8.2.18 LVDS_DATLANE_ORDER

LVDS PHY Data Lane Reorder

ADDR=0x26 (RW)

Bits	Field	Default	Description
[7:6]	sel_tx3	2'h3	data lane 3 is used as 2'h0: the 1st data lane 2'h1: the 2nd data lane 2'h2: the 3rd data lane 2'h3: the 4th data lane
[5:4]	sel_tx2	2'h2	data lane 2 is used as 2'h0: the 1st data lane

			2'h1: the 2nd data lane 2'h2: the 3rd data lane 2'h3: the 4th data lane
[3:2]	sel_tx1	2'h1	data lane 1 is used as 2'h0: the 1st data lane 2'h1: the 2nd data lane 2'h2: the 3rd data lane 2'h3: the 4th data lane
[1:0]	sel_tx0	2'h0	data lane 0 is used as 2'h0: the 1st data lane 2'h1: the 2nd data lane 2'h2: the 3rd data lane 2'h3: the 4th data lane

8.2.19 LVDS_DITHER_EN

LVDS TX RGB888->RGB666 Dither Enable

ADDR=0x27 (RW)

Bits	Field	Default	Description
[7:1]	Reserved		
[0]	lvds_dither_en	1'b0	high active

8.2.20 LVDS_SSC

LVDS PHY Spread Spectrum Enable

ADDR=0x28 (RW)

Bits	Field	Default	Description
[7:5]	sel_depth	3'h1	spread ratio selection
[4:3]	sel_freq	2'h1	modulation frequency selection
[2]	mod34	1'b0	sigma-delta modulator order selection
[1]	spr_mod	1'b0	spread mode selection 1'b0: down spread 1'b1: center spread
[0]	ssc_en	1'b0	spread spectrum enable, high active

8.2.21 LVDS_PHY

LVDS PHY Trim

ADDR=0x29 (RW)

Bits	Field	Default	Description
[7:5]	Reserved		
[4:3]	iset	2'h0	LVDS PHY Swing Selection 2'h0: 250mV 2'h1: 350mV 2'h2: 400mV 2'h3: 250mV (with 100 ohm terminal resistance)
[2:1]	vcm	2'h0	LVDS PHY Common-Mode Voltage Trim
[0]	frq	1'b1	LVDS PHY Clock Range 1'b0: 20~50MHz 1'b1: 50~100MHz

8.2.22 X7PLL_ADJ1

X7PLL Adjustment 1
reserved for debug

ADDR=0x2A (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3]	phasesel	1'b0	debug only
[2]	dv_sel	1'b0	debug only
[1]	forcelock	1'b0	debug only
[0]	pl_bps	1'b0	debug only

8.2.23 X7PLL_ADJ2

X7PLL Adjustment 2
reserved for debug

ADDR=0x2B (RW)

Bits	Field	Default	Description
[7:2]	Reserved		
[1:0]	chp	2'h1	debug only

8.2.24 X7PLL_ADJ3

X7PLL Adjustment 3
reserved for debug

ADDR=0x2C (RW)

Bits	Field	Default	Description
[7:5]	Reserved		
[4:0]	dvt	5'b01110	debug only

8.2.25 X7PLL_ADJ4

X7PLL Adjustment 4
reserved for debug

ADDR=0x2D (RW)

Bits	Field	Default	Description
[7:2]	Reserved		
[1:0]	dly	2'h0	debug only

8.2.26 X7PLL_ADJ5

X7PLL Adjustment 5
reserved for debug

ADDR=0x2E (RW)

Bits	Field	Default	Description

[7:6]	Reserved		
[5:3]	c2trm	3'h3	debug only
[2:0]	c1trm	3'h0	debug only

8.2.27 X7PLL_ADJ6

X7PLL Adjustment 6
reserved for debug

ADDR=0x2F (RW)

Bits	Field	Default	Description
[7:3]	Reserved		
[2:0]	rtrm	3'h2	debug only

8.2.28 X7PLL_ADJ7

X7PLL Adjustment 7
reserved for debug

ADDR=0x30 (RW)

Bits	Field	Default	Description
[7:2]	Reserved		
[1:0]	frq_trm	2'h2	debug only

8.2.29 LVDS_TEST

LVDS PHY Test Control

ADDR=0x31 (RW)

Bits	Field	Default	Description
[7:6]	Reserved		
[5:4]	ts	2'h0	analog test mux selection
[3:2]	tm	2'h0	built in test mode selection 2'h0: PRBS mode 2'h1: 1100011 (clock mode) 2'h2: high 2'h3: low
[1]	test_pl_en	1'b0	pll vc test enable
[0]	tst_en	1'b0	built in test mode enable

8.2.30 LVDS_TDI

LVDS PHY Test Data In

ADDR=0x32 (RW)

Bits	Field	Default	Description
[7]	Reserved		
[6:0]	tdi	7'b1100011	test data input

8.2.31 LVDS_TDO

LVDS PHY Test Data Out

ADDR=0x33 (RO)

Bits	Field	Default	Description
[7]	Reserved		
[6:0]	tdo	--	test data output

8.2.32 LVDS_TSO

LVDS PHY Test Result

ADDR=0x34 (RO)

Bits	Field	Default	Description
[7:2]	Reserved		
[1]	tpso	--	test result
[0]	tso	--	test result

8.2.33 X7PLL_LOCK

X7PLL Lock Status

ADDR=0x35 (RO)

Bits	Field	Default	Description
[7:1]	Reserved		
[0]	lock	1'b0	1'b1 means locked

8.2.34 PADI_DPI_ADJ

Adjust DPI interface from PAD inputs

ADDR=0x40 (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3]	padi_dataen_inv	1'b0	inverse DATAEN from PAD input, high active
[2]	padi_hsync_inv	1'b0	inverse HSYNC from PAD input, high active
[1]	padi_vsync_inv	1'b0	inverse VSYNC from PAD input, high active
[0]	padi_pclk_inv	1'b0	inverse PCLK from PAD input, high active

8.2.35 PADO_DPI_ADJ

Adjust DPI interface to PAD outputs

ADDR=0x41 (RW)

Bits	Field	Default	Description
[7:4]	Reserved		
[3]	pado_dataen_inv	1'b0	inverse DATAEN to PAD output, high active
[2]	pado_hsync_inv	1'b0	inverse HSYNC to PAD output, high active
[1]	pado_vsync_inv	1'b0	inverse VSYNC to PAD output, high active
[0]	pado_pclk_inv	1'b0	inverse PCLK to PAD output, high active

8.2.36 LVDS_SOURCE

LVDS TX Source DPI Selection

ADDR=0x42 (RW)

Bits	Field	Default	Description
[7:2]	Reserved		
[1]	lvds_pixel_clk_en	1'b0	pixel clk to LVDS TX enabled or gated 1'b0: gated 1'b1: enabled
[0]	lvds_dpi_sel	1'b0	LVDS TX Source DPI Selection 1'b0: from MIPI DSI RX 1'b1: from PAD inputs

9 Software Guideline

To ease the use of ZA7783 as a display bridge chip, we provide an excel tool ZA7783_APPTOOL_Vx.x.xls. Users may select the desired working mode, and fill in the timing parameters of the target RGB/LVDS Panel. Then, the tool will give out the following results:

1. ZA7783 initialization configuration
2. ZA7783 sleep configuration
3. ZA7783 wake-up configuration

To implement a successful bridge solution, besides ZA7783, the host chip should also be properly configured. The following sections detail this.

9.1 Host Chip in MIPI => LVDS Scenario

In MIPI => LVDS scenario, the host chip must configure MIPI DSI TX according to the following rules:

1. MIPI DSI TX must work in Video Mode, and must select Non-Burst Mode with Sync Pulses.

2. MIPI DSI TX must use all of its four data lanes.

3. MIPI DSI TX must provide continuous high-speed clock in clock lane. During normal display, the clock lane must keep in high-speed state with active clock, and must not switch to low-power state.

4. The frequency of high-speed clock in clock lane must be 3 times of the target pixel clock frequency.

5. MIPI DSI TX must use RGB888 format or Loosely Packed RGB666 format.

6. Timing information carried by MIPI DSI TX, such as HSA, HBP, HFP, HACT, VSA, VBP, VFP, and VACT, must match the timing requirements of the target LVDS Panel.

9.2 Host Chip in MIPI => RGB Scenario

It is the same as MIPI => LVDS scenario.

9.3 Host Chip in RGB => LVDS Scenario

In RGB => LVDS scenario, the host chip must configure DPI IF according to the following rules:

1. The frequency of pixel clock outputted by the host chip must match the target pixel clock frequency.

2. Timing parameters of DPI IF outputted by the host chip, such as HSA, HBP, HFP, HACT, VSA, VBP, VFP, and VACT, must match the requirements of the target LVDS Panel.

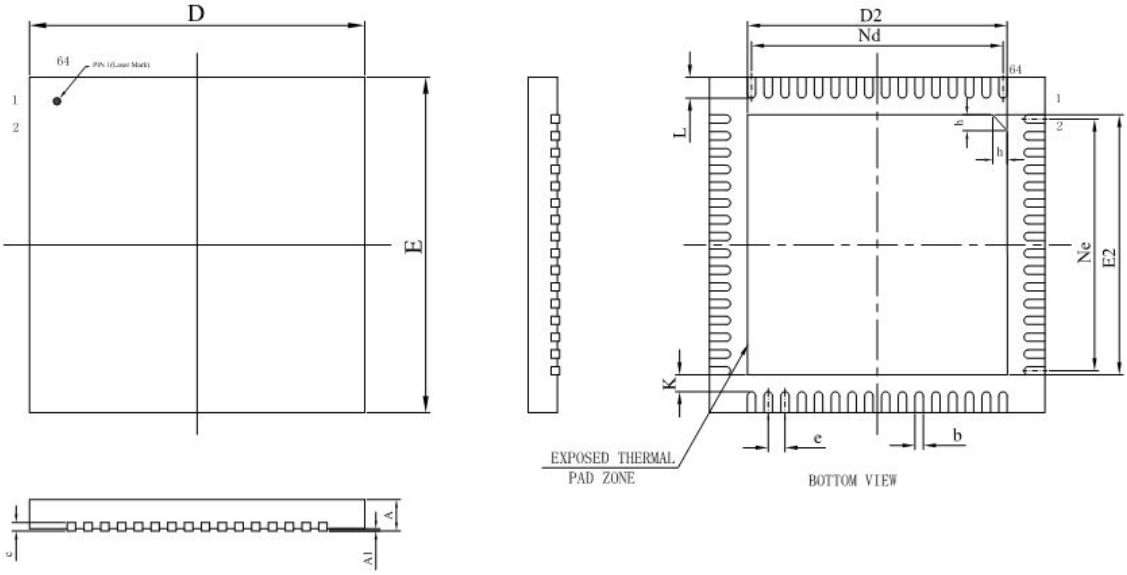
9.4 Start-Up Sequence

Normally, it is recommended that firstly do the initialization of ZA7783, and then start the host chip to display.

However, it is also allowed that the host chip starts display firstly, and initializes ZA7783 later on. The design of ZA7783 is robust to handle the case of starting in the middle of a frame.

10 Package Information

ZA7783 is provided in 8x8 QFN64 package, 0.4 pitch.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 70	0. 75	0. 80
A1	—	0. 02	0. 05
b	0. 15	0. 20	0. 25
c	0. 18	0. 20	0. 25
D	7. 90	8. 00	8. 10
D2	6. 10	6. 20	6. 30
e	0. 40BSC		
Nd	6. 00BSC		
E	7. 90	8. 00	8. 10
E2	6. 10	6. 20	6. 30
Ne	6. 00BSC		
L	0. 45	0. 50	0. 55
K	0. 20	—	—
h	0. 30	0. 35	0. 40

包装规格

封装形式	卷盘规格	载带宽度	只/卷	卷/盒	只/盒	盒/箱	只/箱
QFN064 (0808*0.75-0.40)	13”	16	3000	1	3000	8	24000