Piecewise Compensated High PSRR Bandgap Voltage Reference

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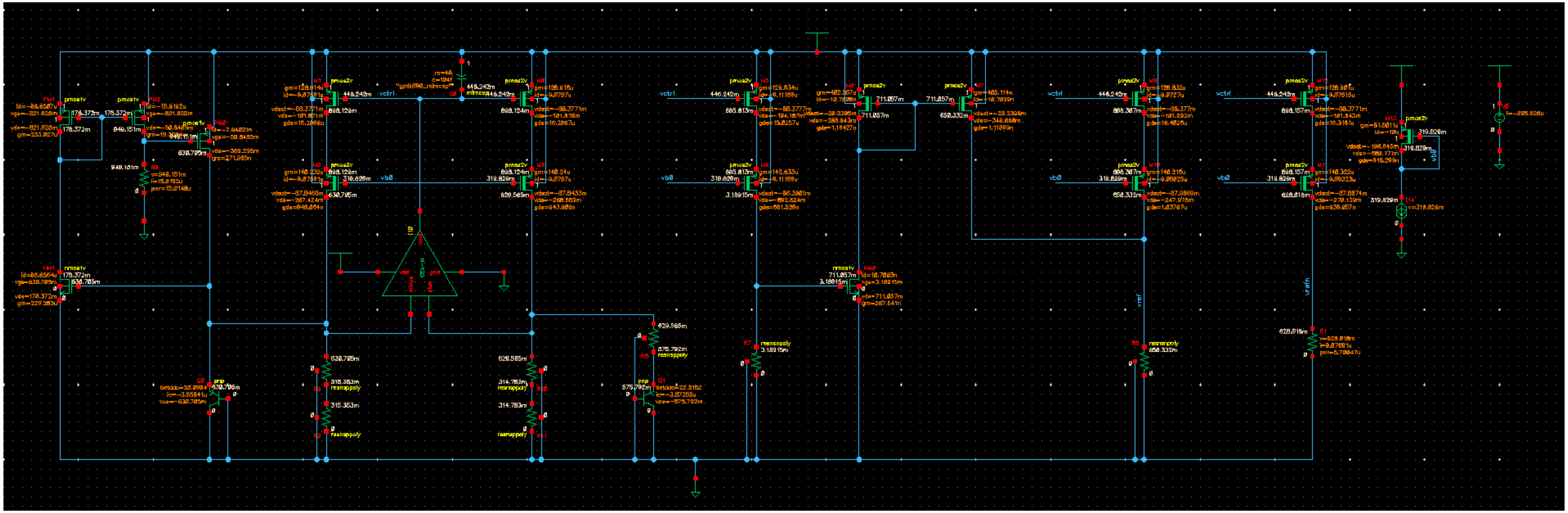
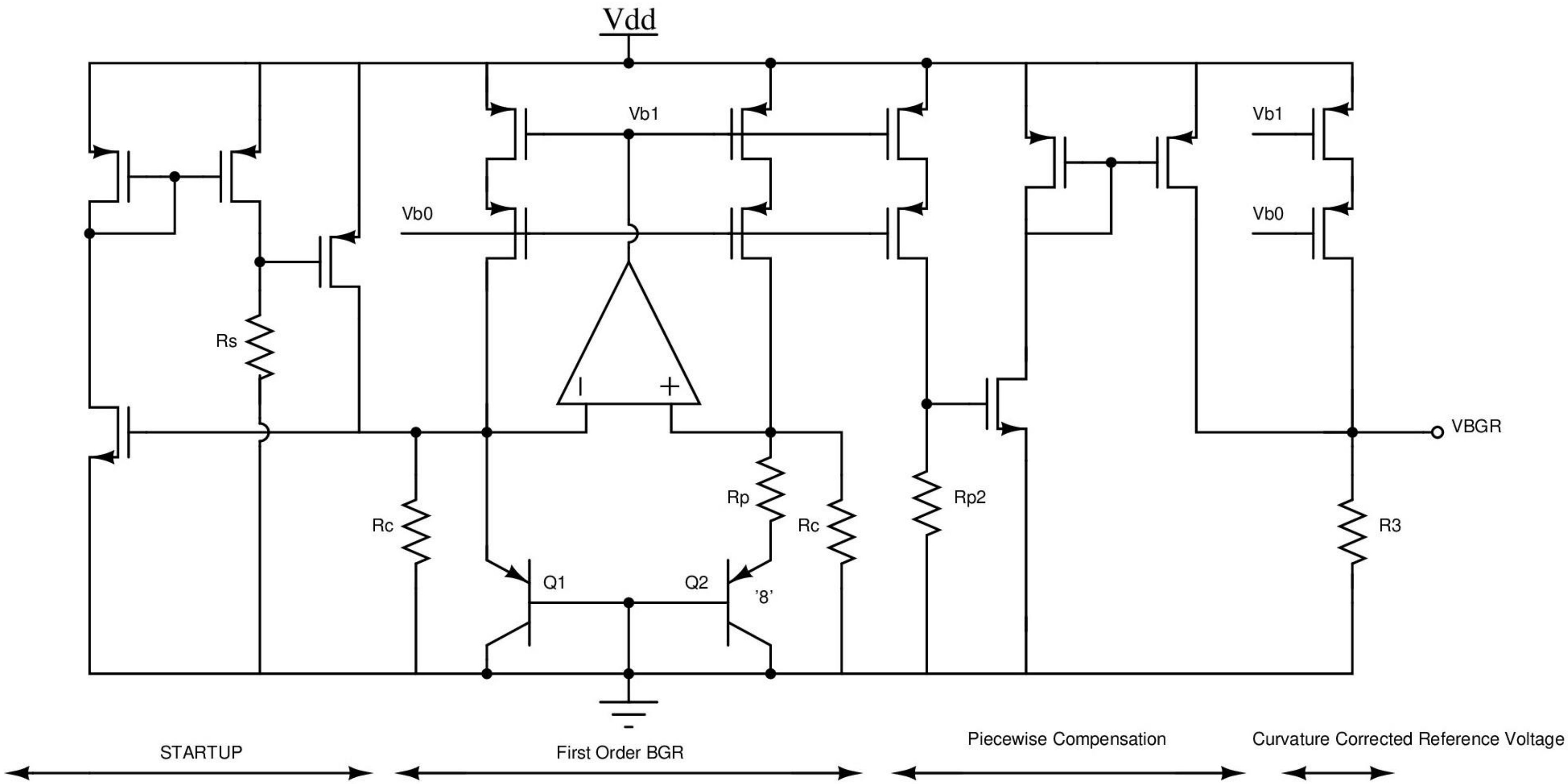
- **Second Order Curvature Corrected Bandgap Reference Schematic**



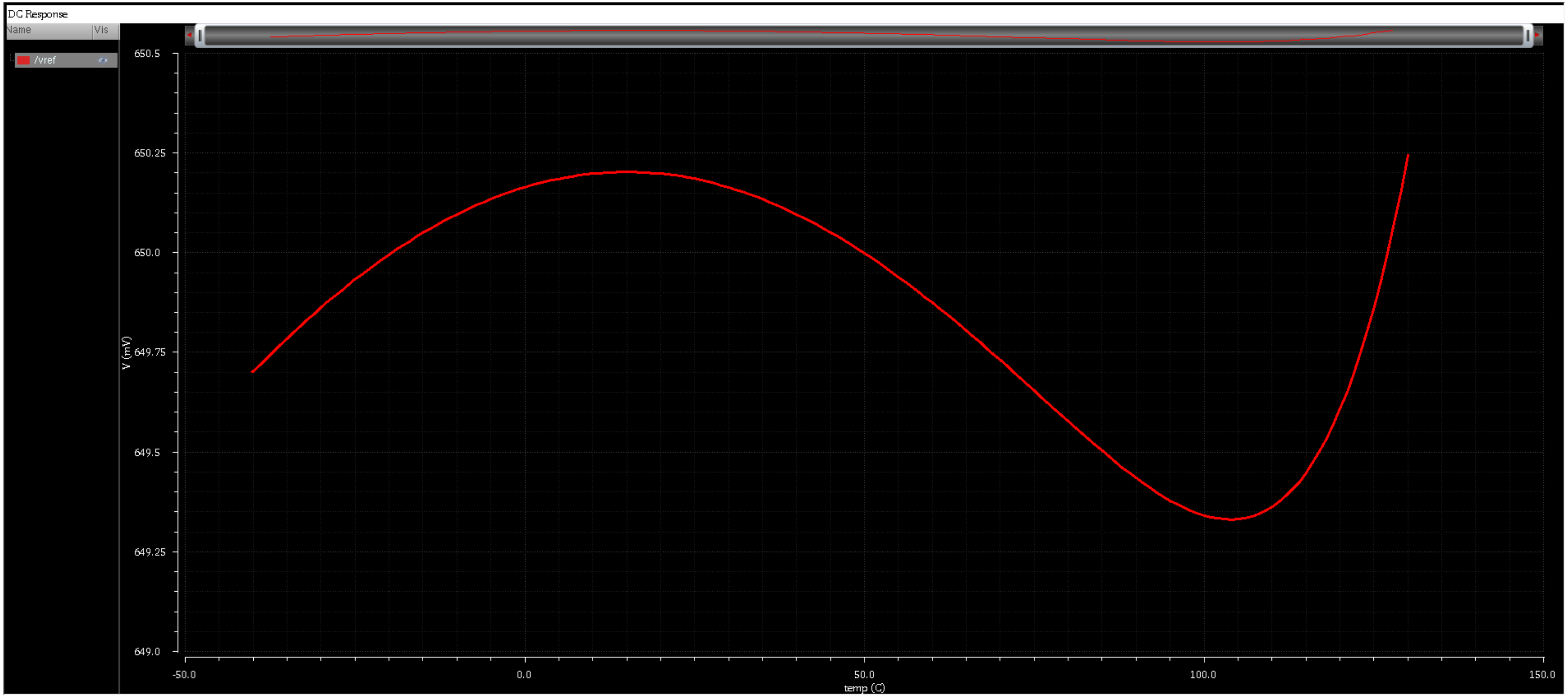
- M1, M2, M3, M4: gm/id=15 | R8, R10, R11, R2: 62.6K | R6=13.2867K | R7=500 | NM0: gm/id=25.

Circuit Diagram

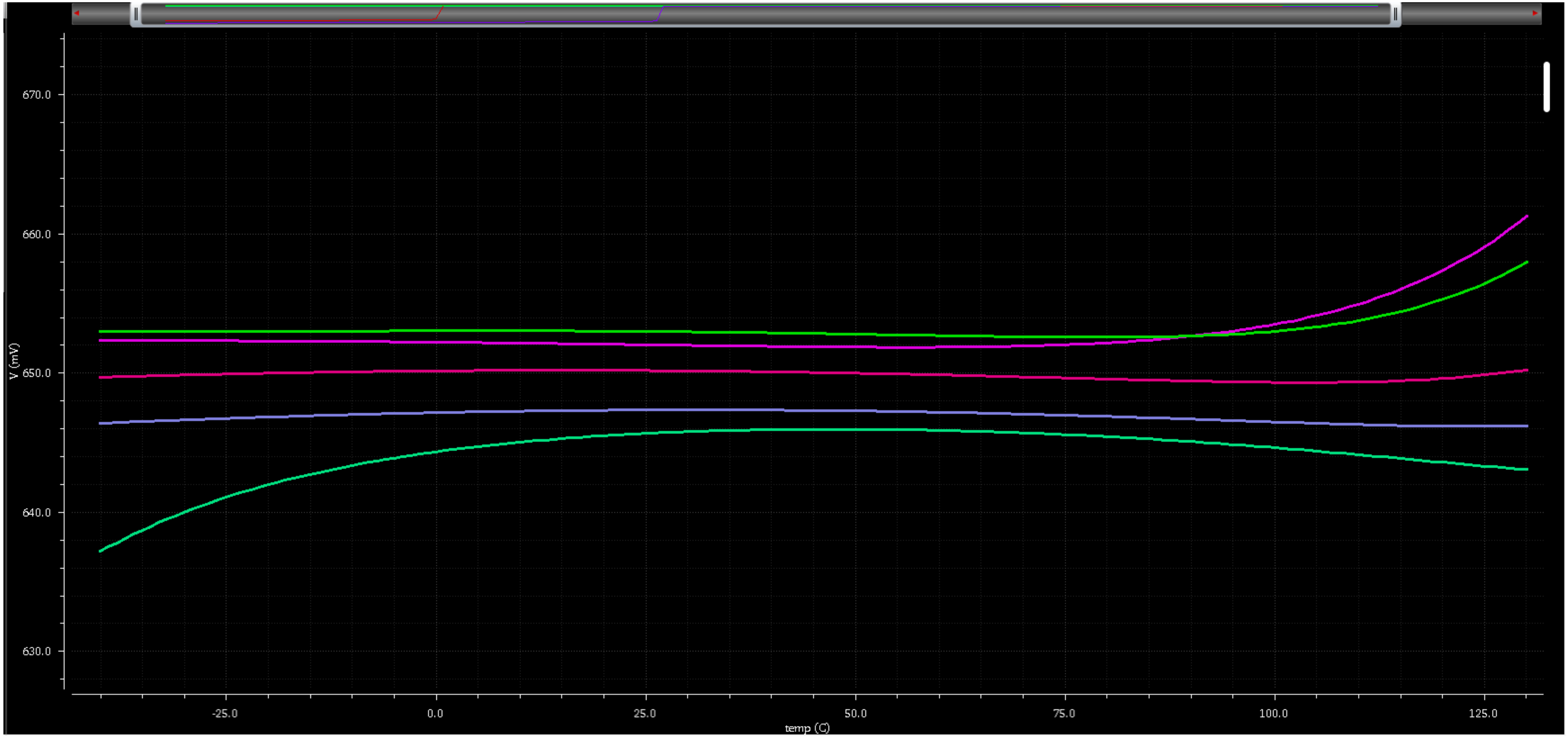


Second Order Curvature Corrected Reference Voltage wrt to Temperature

- I have added an extra exponential current to I_{ref} to cancel higher order terms in I_{ref} (Especially ones from V_{BE}).
- This has been realized by pushing I_{ref} current to a resistor and this is sensed by a Mosfet in subthreshold region and this exponential current is pushed along with I_{ref} to cancel higher order terms in I_{ref}.
- The Accuracy of this BGR is within 0.8mV
- As you can see this Bandgap Reference has a very small Temperature coefficient across temperature making it very accurate.
- **Temperature Coefficient = 4.4ppm/°C**

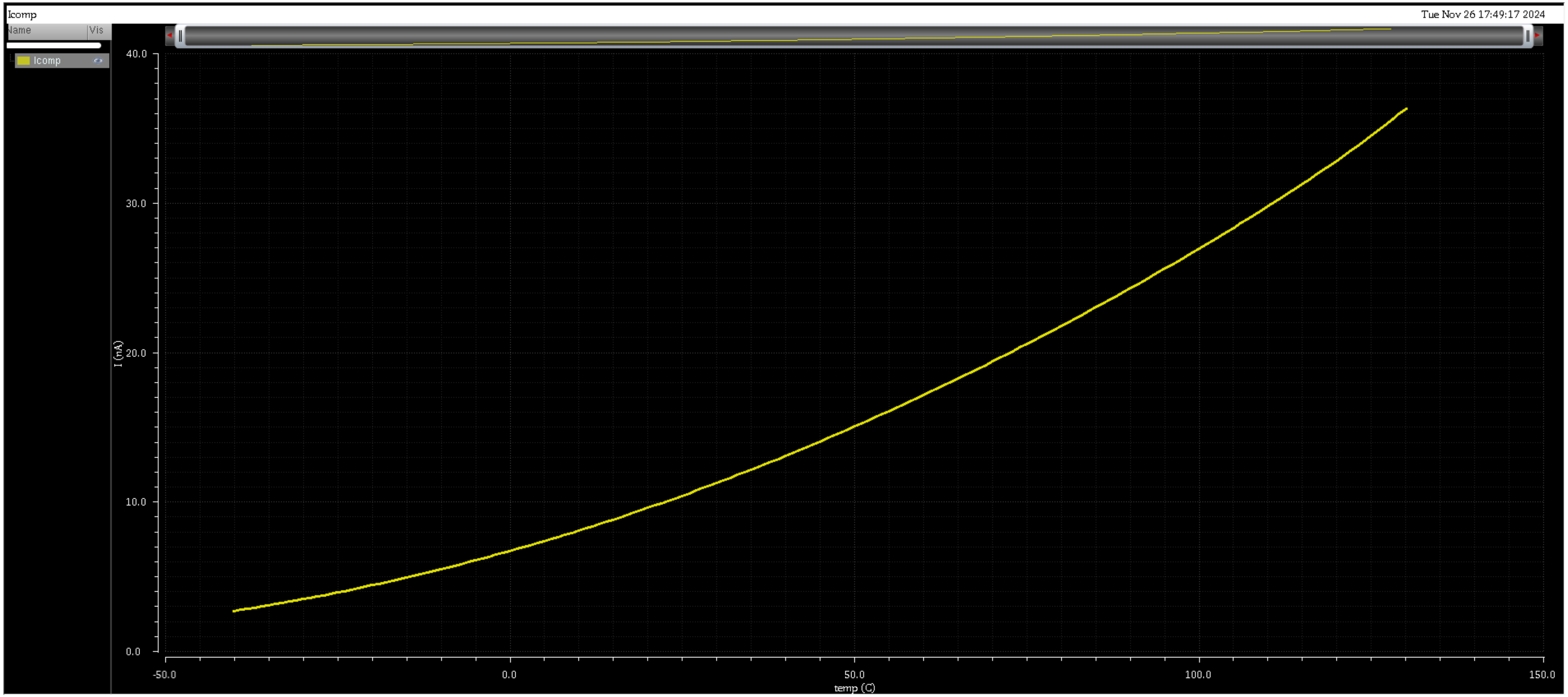


Second Order Curvature Corrected Reference Voltage across Different Process Corners (FF, FS, TT, SF, SS) and Temperature



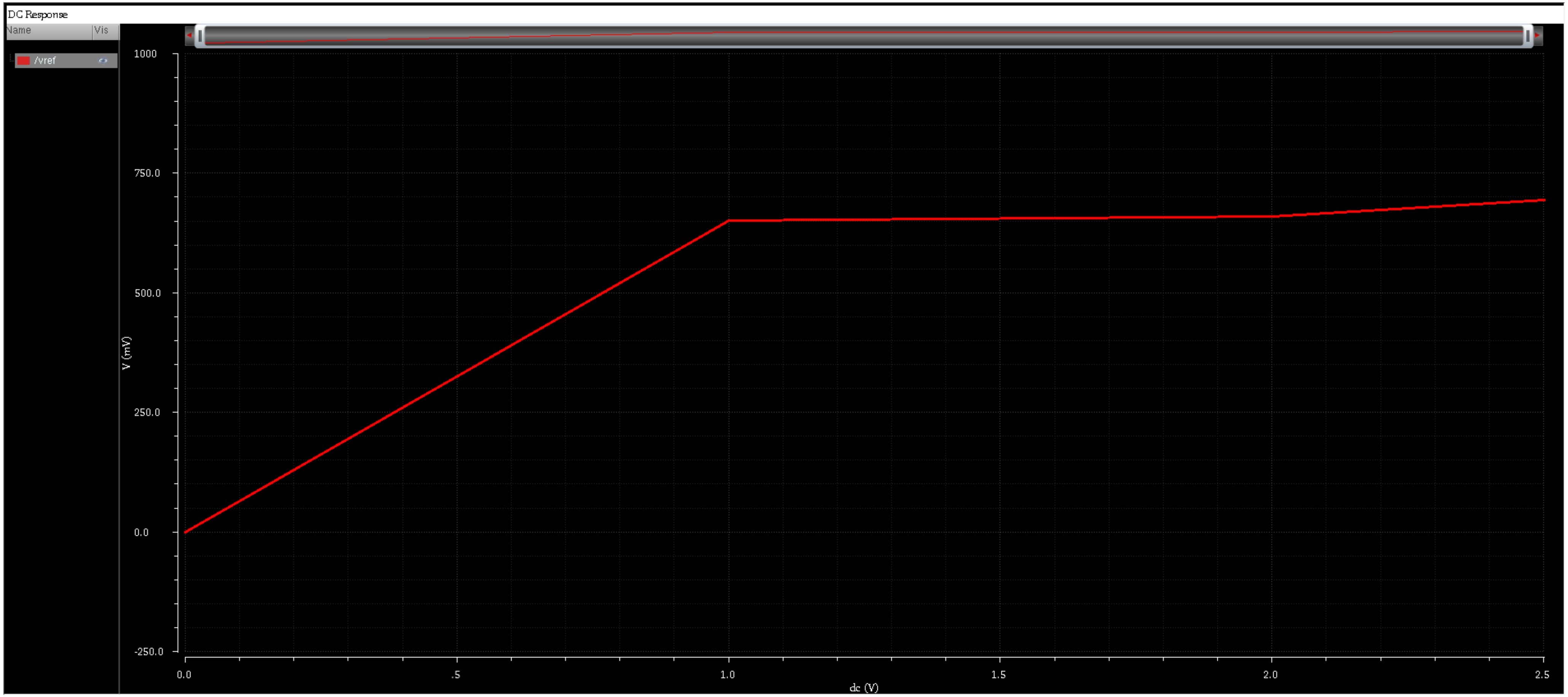
- The Reference Voltage across Different Process corners (SS, SF, FF, FS, TT) and temperature (-40 °C, 27 °C, 125 °C).

Second Order Compensation Current



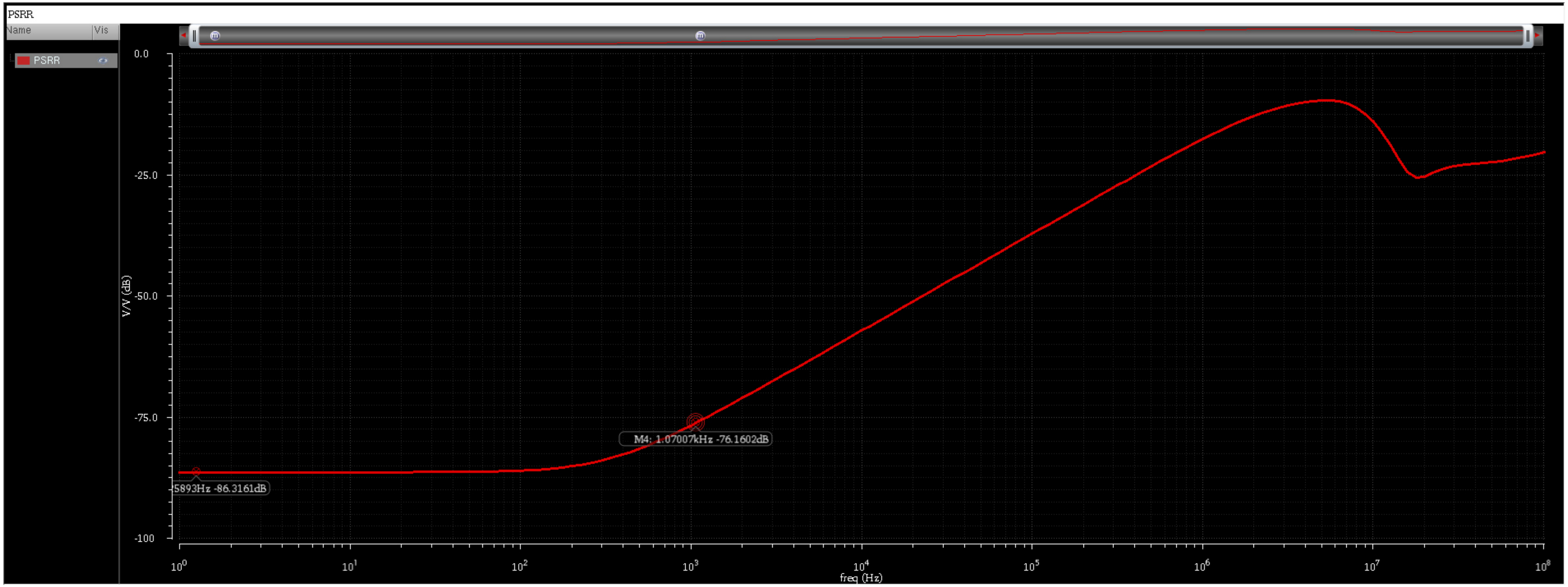
- This Compensation current has been added to compensate for higher order terms within Bandgap Reference. This is a function of both PTAT and CTAT higher order terms.
- The curve is kind of exponential in nature, but it is much more complex and contains higher order dependencies of Vbe especially Is (Saturation Current) which has higher order dependencies on temperature.

Second Order Curvature Corrected Reference Voltage wrt Supply Voltage sweep



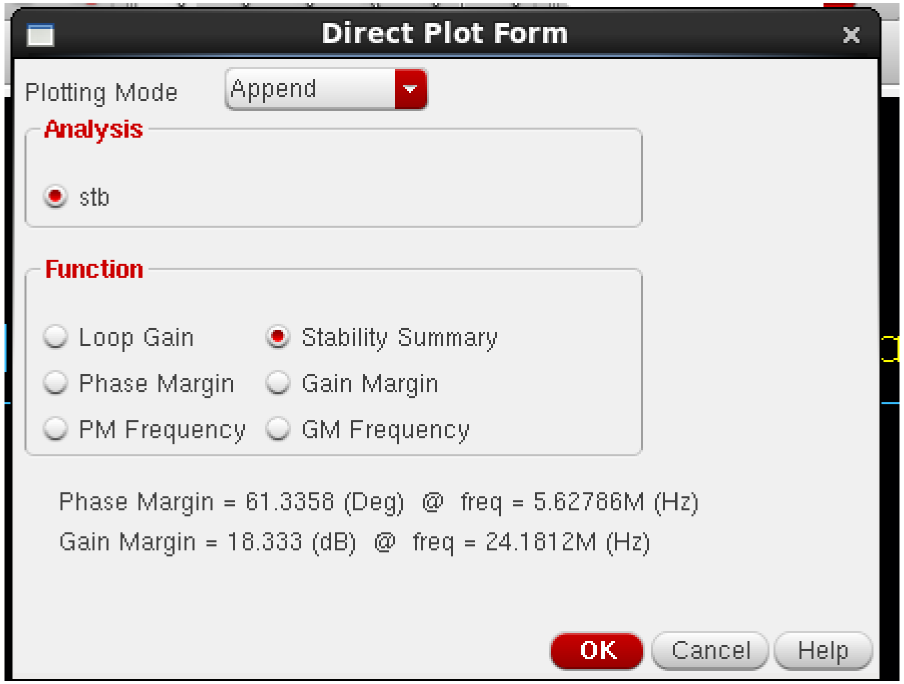
- Supply Voltage is swept from 0 to 2.5V. The BGR and OTA wake up and start working properly around 1V. Later the Reference Voltage mostly remains constant.

Power Supply Rejection Ratio of the Piecewise Compensated Bandgap Voltage Reference



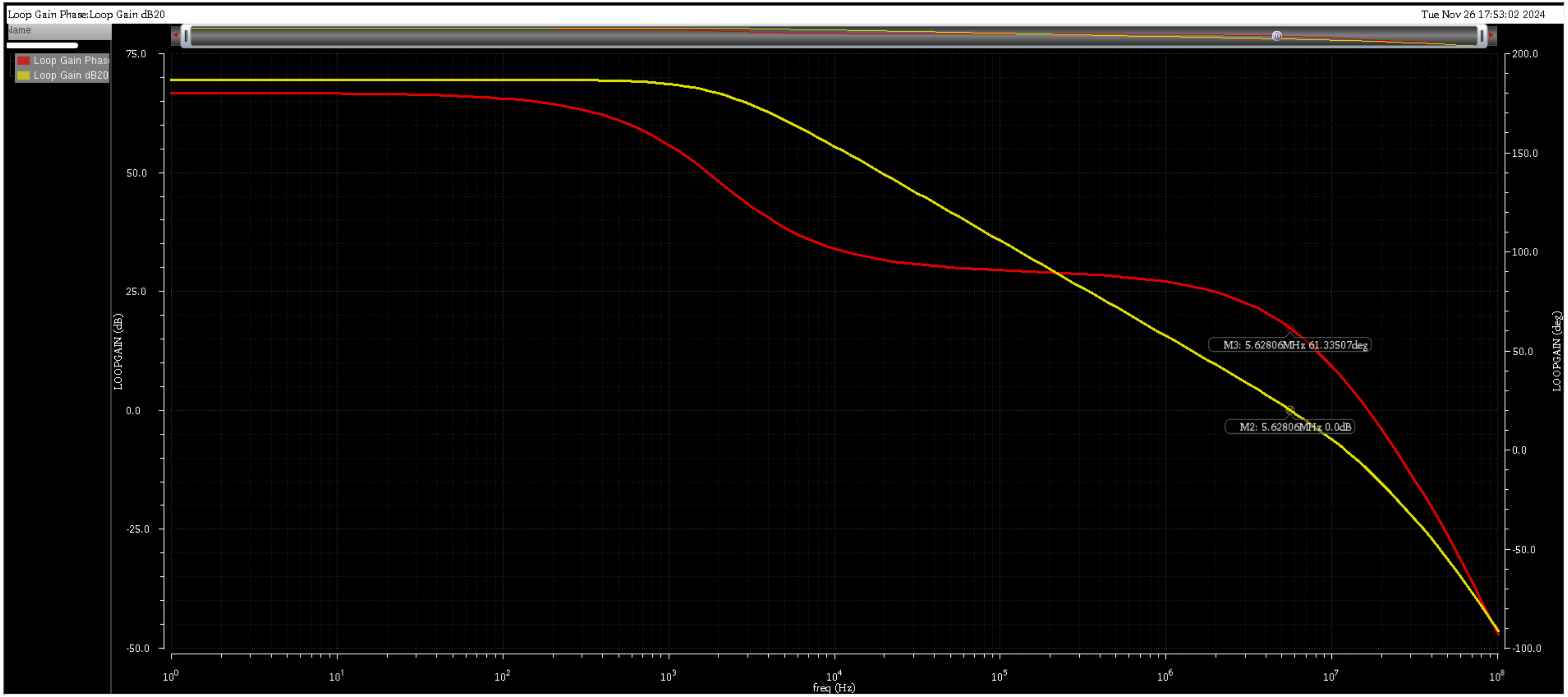
- The PSRR of the BGR at DC is -86dB and -76dB at 1kHz. This due to the use of high swing cascode current mirror in the BGR and bias network that also track the supply ripple essentially attenuating it.

Stability of the combined Feedback Loop



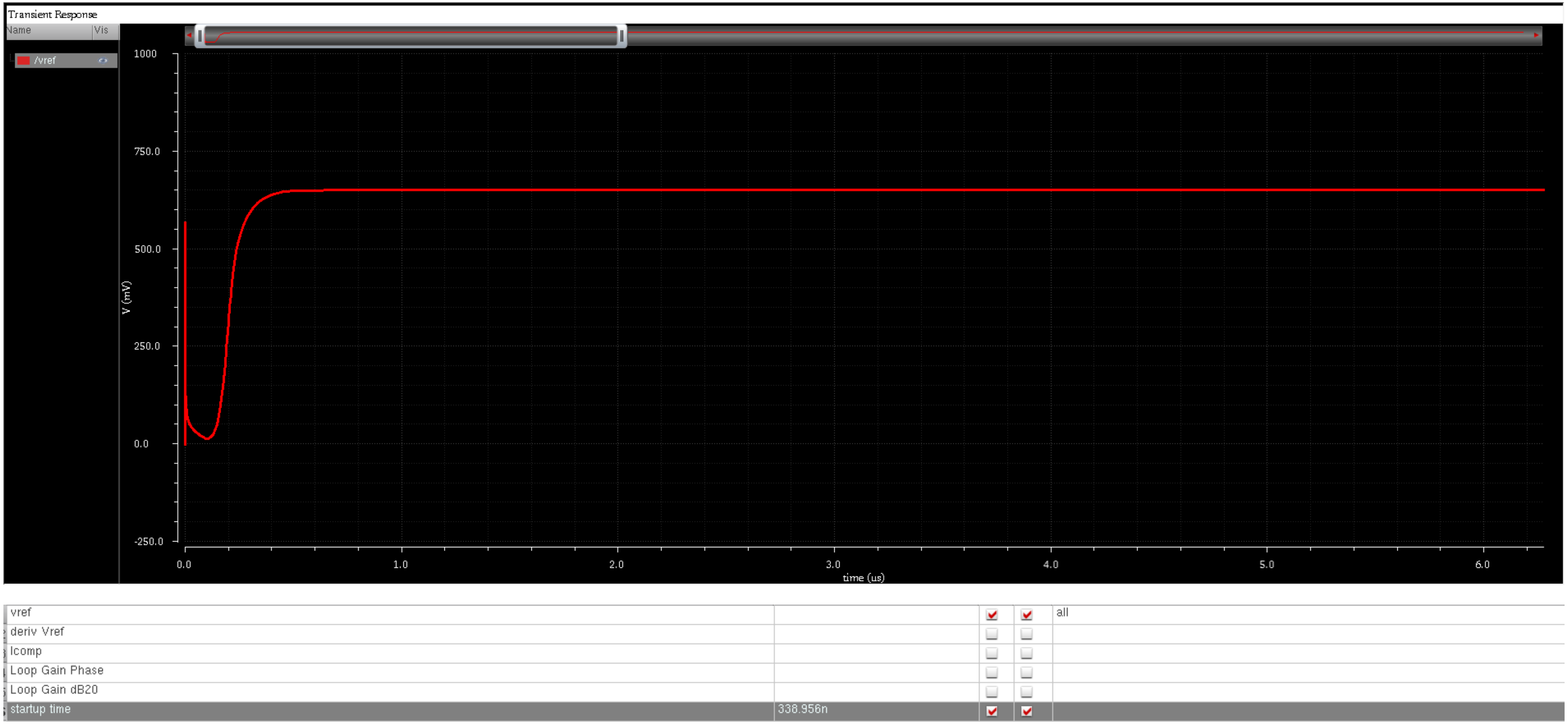
- The Phase margin of the combined feedback Loop of the BGR is 61.3359° and Unity Gain Bandwidth of 5MHz.
- The Gain margin of the feedback Loop is 18.33dB.
- The Negative feedback Loop is stable and is capable of settling transients within 1µsec.

Loop Gain and Phase of BGR Feedback Loop



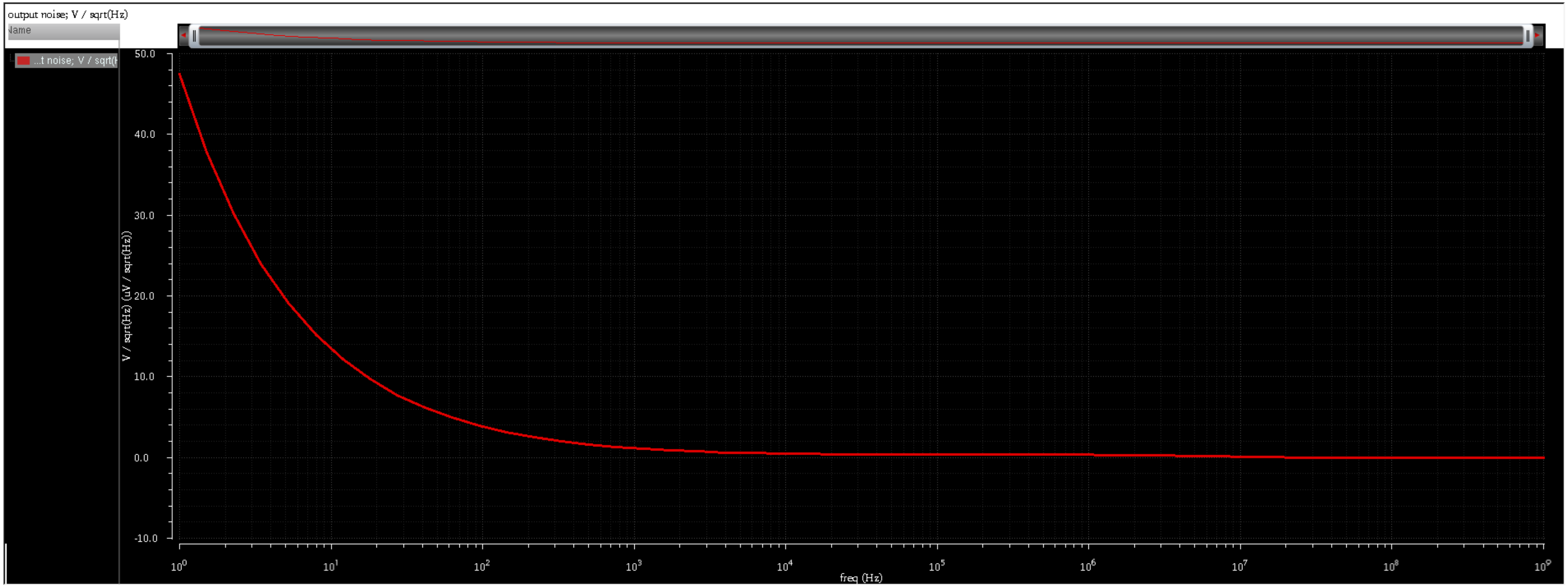
- The Phase margin of the combined feedback Loop of the BGR is 61.3359° and Unity Gain Bandwidth of 5MHz.

Startup time of the Piecewise Compensated Bandgap Voltage Reference



- The startup time of the Bandgap Reference (BGR) is approximately 338 ns. The startup circuit quickly transitions the BGR from a zero-current state to its stable operating point, ensuring rapid stabilization.

Noise Analysis of the Piecewise Compensated Bandgap Voltage Reference



Noise Analysis of the Piecewise Compensated Bandgap Voltage Reference

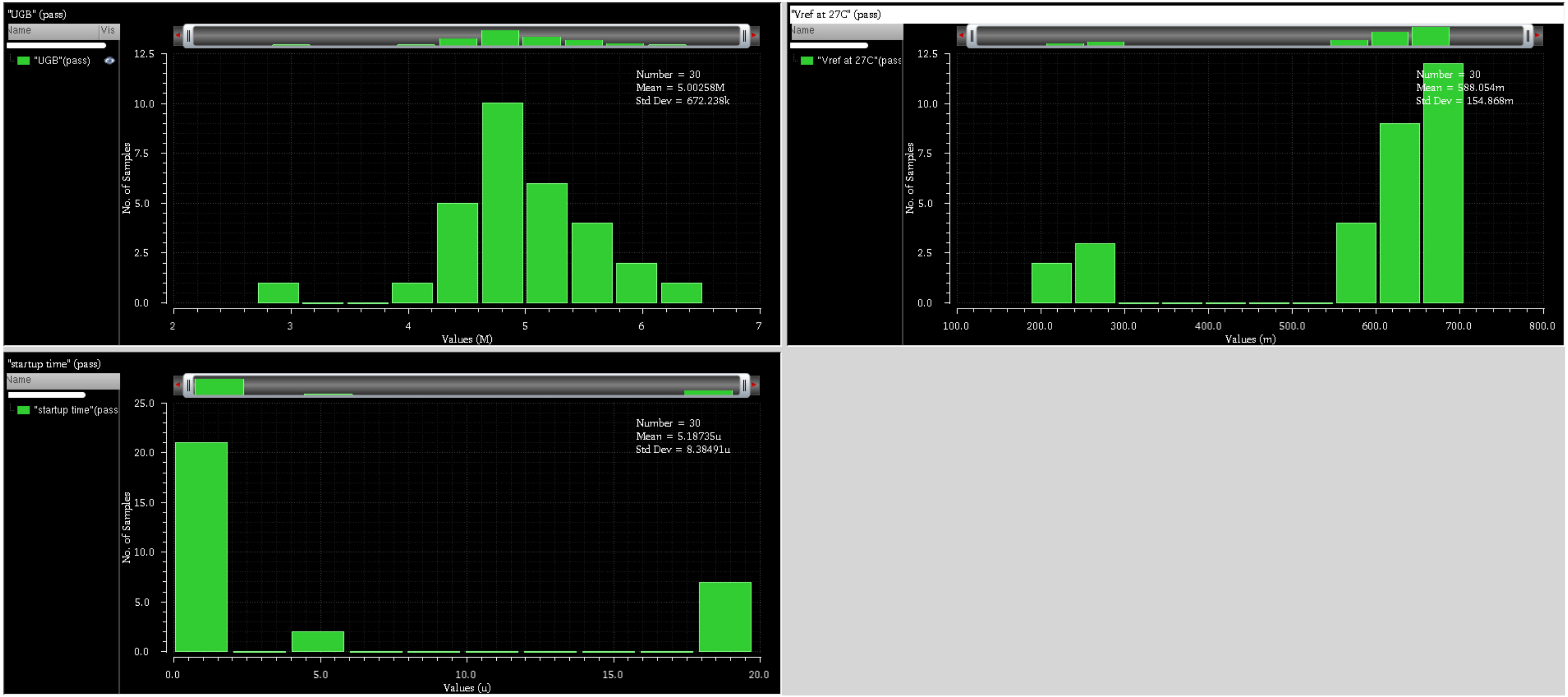
Device	Param	Noise Contribution	% Of Total
/M0	id	1.85049e-07	24.38
/M9	id	1.23298e-07	16.25
/I10/NM0	id	8.99705e-08	11.85
/I10/NM5	id	8.98908e-08	11.84
/M10	id	3.19899e-08	4.22
/I10/PM3	id	2.96141e-08	3.90
/R6/R0	rs	2.77217e-08	3.65
/I10/PM1	id	2.69555e-08	3.55
/M1	id	2.61503e-08	3.45
/I10/NM9	id	2.04612e-08	2.70
/R8/R0	rs	1.86573e-08	2.46
/Q0	ic	8.48255e-09	1.12
/R8/R1	rs	8.22986e-09	1.08
/I10/PM2	id	7.37711e-09	0.97
/Q0	rb	6.92098e-09	0.91
/Q1	ic	6.5466e-09	0.86
/I10/NM6	id	4.43338e-09	0.58
/R8/R2	rs	4.21385e-09	0.56
/M7	id	3.79361e-09	0.50
/R8/R3	rs	2.45116e-09	0.32
/I10/PM3	fn	2.11443e-09	0.28
/I10/PM1	fn	1.95593e-09	0.26
/M3	id	1.67195e-09	0.22
/R8/R4	rs	1.57617e-09	0.21
/I10/NM0	fn	1.37214e-09	0.18
/I10/NM5	fn	1.36615e-09	0.18
/R8/R5	rs	1.09326e-09	0.14
/I10/R3/R8	rs	9.34857e-10	0.12
/M13	id	8.95059e-10	0.12
/I10/NM9	fn	8.17839e-10	0.11
/R8/R6	rs	8.02956e-10	0.11
/Q1	rb	7.23013e-10	0.10
/R8/R7	rs	6.16438e-10	0.08
/I10/R3/R7	rs	6.10442e-10	0.08
/R8/R8	rs	4.9035e-10	0.06
/PM0	id	4.77584e-10	0.06
/M0	fn	4.66944e-10	0.06
/I10/R3/R6	rs	4.1613e-10	0.05
/I10/R0/R8	rs	4.14528e-10	0.05
/I10/R0/R7	rs	4.14527e-10	0.05
/I10/R0/R6	rs	4.14525e-10	0.05
/I10/R0/R5	rs	4.14523e-10	0.05
/I10/R0/R4	rs	4.14522e-10	0.05
/I10/R0/R3	rs	4.1452e-10	0.05
/I10/R0/R2	rs	4.14519e-10	0.05
/I10/R0/R1	rs	4.14517e-10	0.05
/I10/R0/R0	rs	4.14516e-10	0.05
/R8/R9	rs	4.01753e-10	0.05
/R8/R10	rs	3.37652e-10	0.04
/R10/R9	rs	3.30737e-10	0.04

Integrated Noise Summary (in V^2) Sorted By Noise Contributors
Total Summarized Noise = 7.58953e-07
Total Input Referred Noise = 0.00178593
The above noise summary info is for noise data

Monte Carlo Simulations

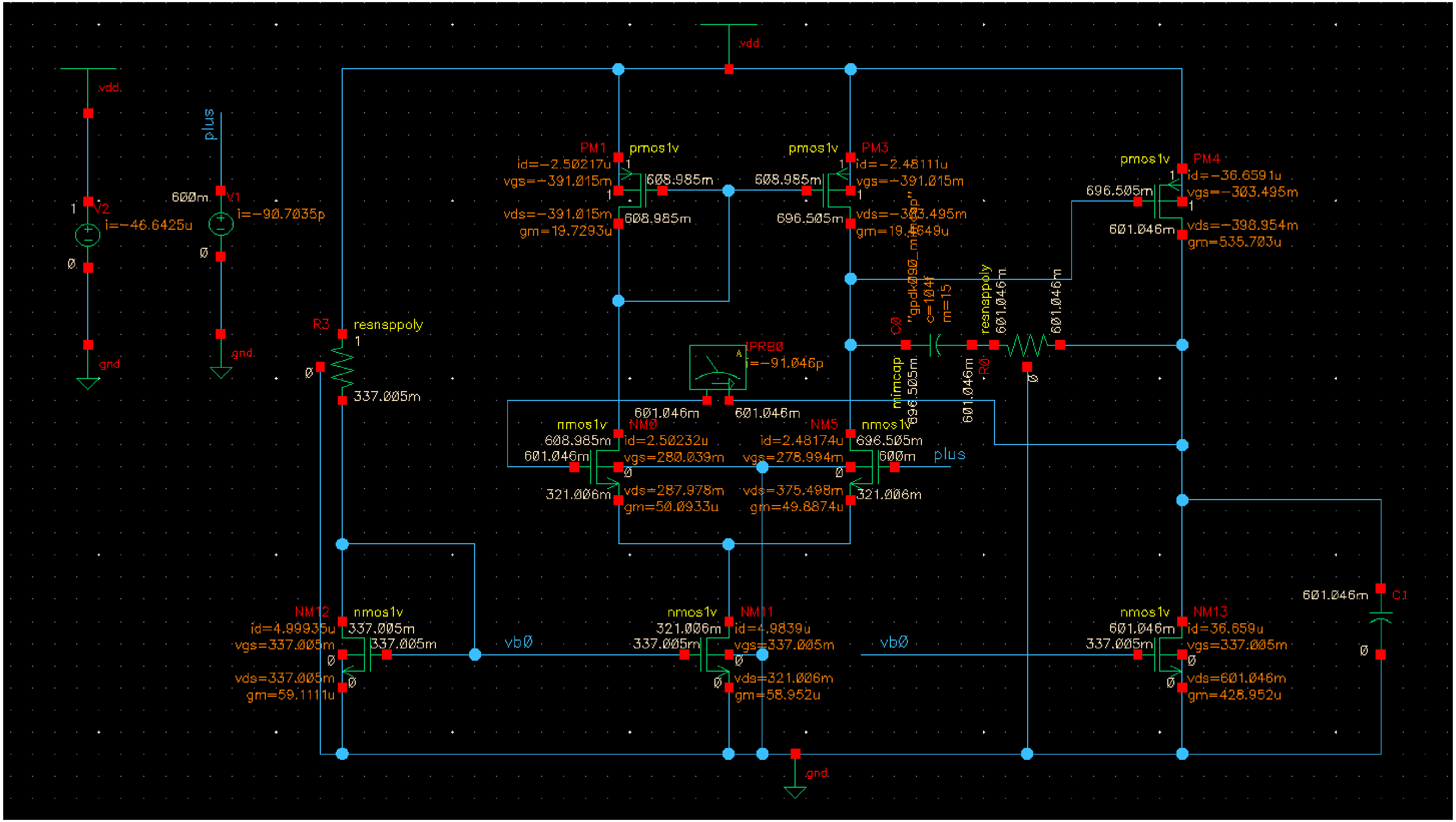
- The 200mV and 300mV are due to startup convergence issue, other than that most of the time Vref is close to 650mV.

Monte Carlo Simulations



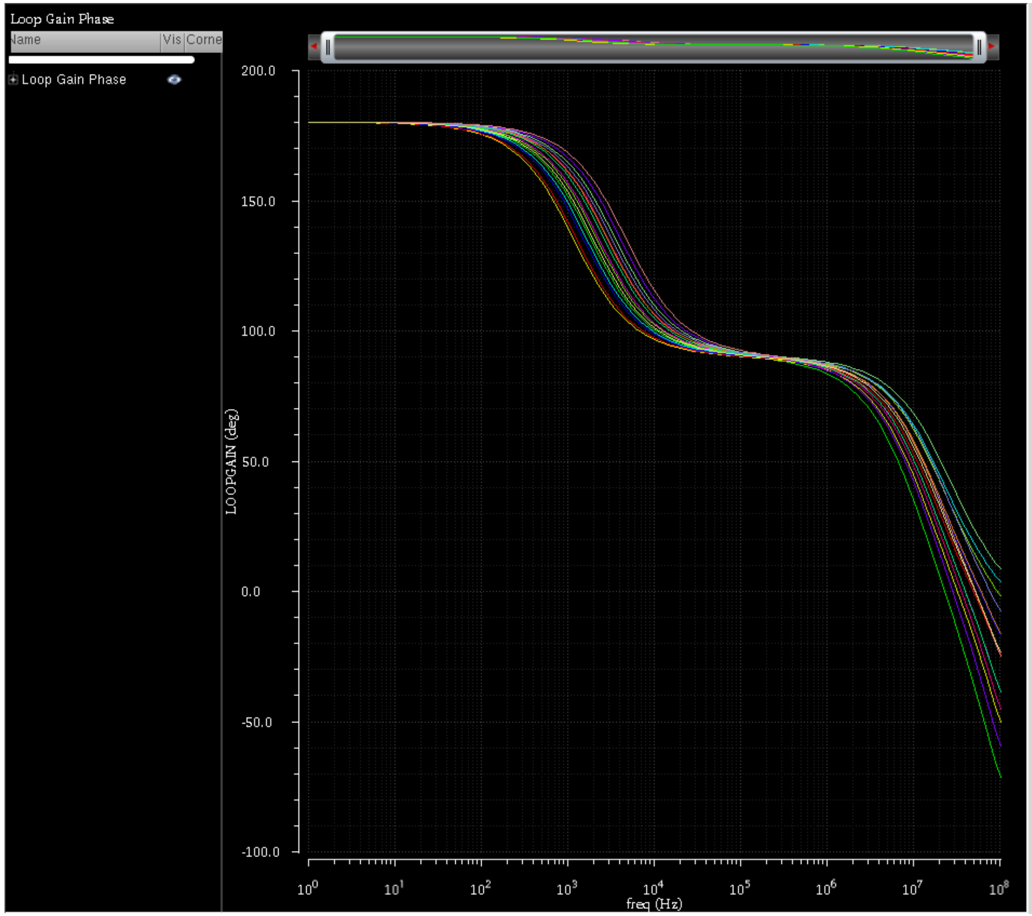
- Monte Carlo Sims of UGB, V_{ref} and Startup time of the BGR.

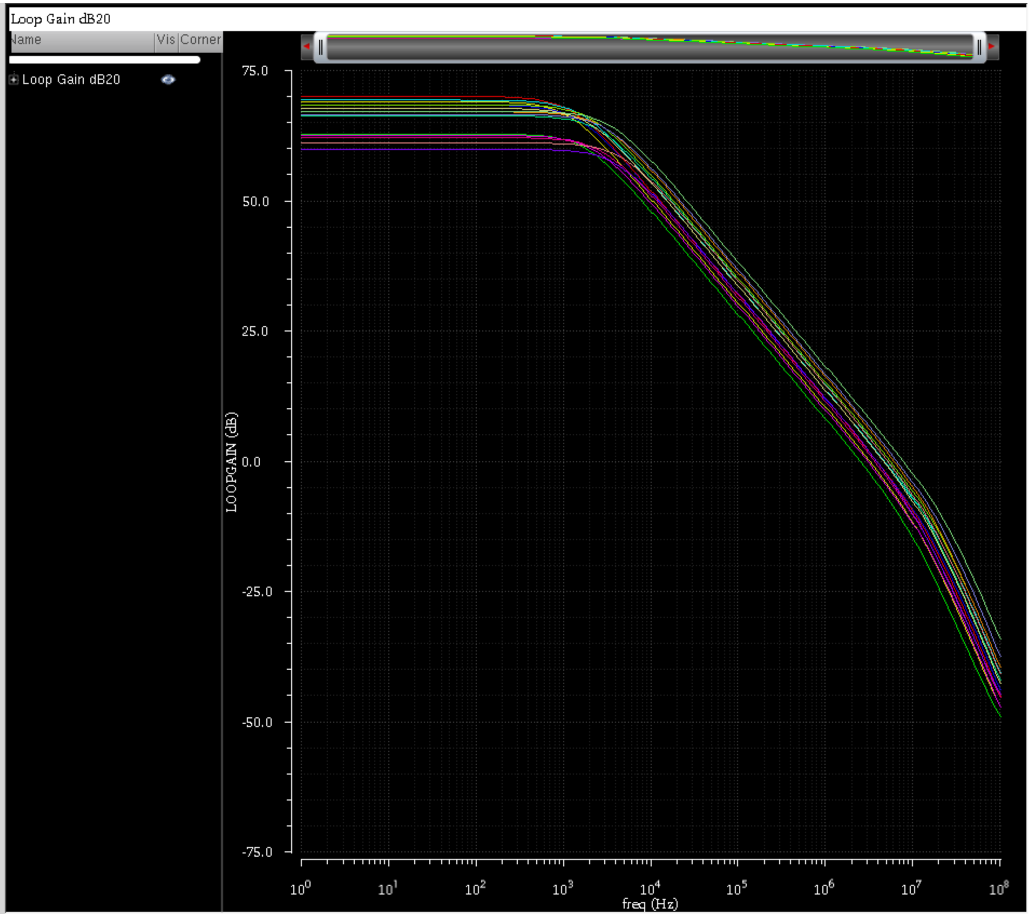
OTA used in the Bandgap Voltage Reference



- NM0, NM5: gm/id=20, NM1, NM12, NM13: gm/id=12, PM1, PM3: gm/id=8, PM4: gm/id= 15

Loop Gain and Phase of the OTA across different corners and Operating Temperature of the BGR





- Across Different Process corners (SS, SF, FF, FS, TT) and temperature (-40 °C, 27 °C, 125 °C) the Gain the OTA remains sufficiently high and the GBW is between 3.5MHz to 7MHz.

Acknowledgement

- **I'm Thankful to Soumya Kanta Rana and Diarmuid Collins for all their Guidance and Suggestions.**

References:

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5. Ka Nang Leung and P. K. T. Mok, "A sub-1-V 15-ppm//spl deg/C CMOS bandgap voltage reference without requiring low threshold voltage device," in *IEEE Journal of Solid-State Circuits*, vol. 37, no. 4, pp. 526-530, April 2002, doi: 10.1109/4.991391.

THANK YOU