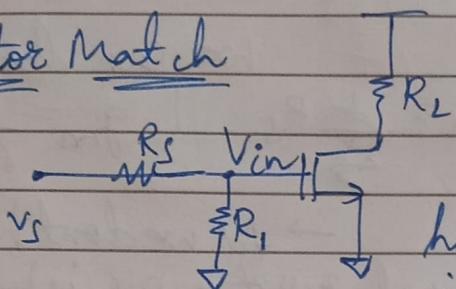


LNA design :-

Input Match

- 1) For a signal source coming in at 50Ω , but the input to the mosfet is a capacitor, so we need to transform it to a resistor.

Resistor Match

CS Amp. Match

→ Broadband

→ $R_1 \approx R_s$ [Power Matching]

For every high frequency the MOSFET is O.C due to very high impedance so impedance will be R_1 . It is also Broadband

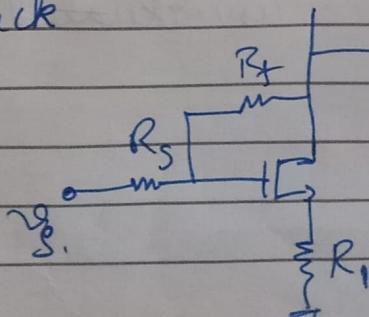
$\rightarrow V_{in} = \frac{V_s}{2}$ [So this is attenuation before amplification, so bad]

$\rightarrow R_1 \rightarrow$ Thermal Noise [which is adding directly at the ip]

$\rightarrow f = 2 + 4r \frac{1}{g_m R_s}$ [for CS Amplifier]

So NF $\geq 3dB$ [This a problem]

2) Feedback

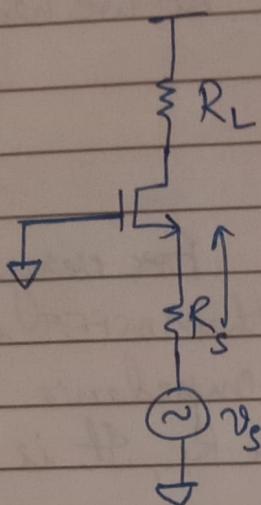


\rightarrow So R_f (feedback resistor is added) we can match input Res to 50Ω

\rightarrow Also added advantage is there is no attenuation before amp. lifier stage

- But we have noise from R_f
- Noise figure of this ckt is greater than CS Amplifier

3) G-Gate Amplifier



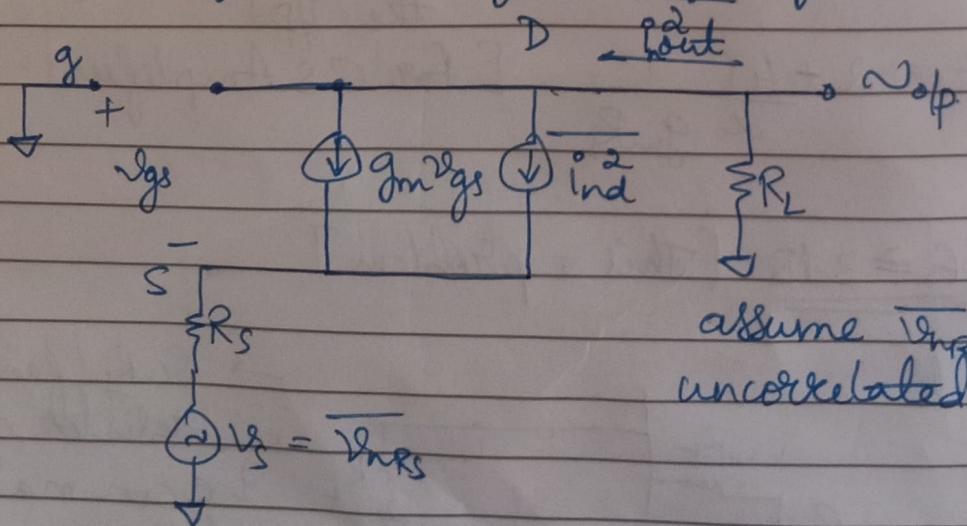
Input impedance is a function $R_L \& g_m$

$$R_{in} = \frac{1}{g_m} R_s \quad [g_m = \frac{1}{R_s}]$$

→ As we don't have any physical resistor NF is better here

For Calculation we are going to ignore Gate noise for now. But for high frequency gate noise will be added on top of the Drain noise. But here we calculate for long channel case.

→ Signal coming in are mostly voltages but in mixers it's easier if current signal is going in.



assume i_{D1}, i_{D2} are uncorrelated

a) $\overline{V_{RS}}$ [$i_{nd} = 0$]

$$\overline{i_{inout}} = g_m \overline{v_{gs}} = -g_m \overline{v_s}$$

$$\overline{v_s} = -\overline{v_{nRS}} + \overline{i_{inout}} \cdot R_s$$

$$\Rightarrow -\frac{\overline{i_{inout}}}{g_m} = \overline{v_{nRS}} + \overline{i_{inout}} \cdot R_s$$

$$\overline{i_{inout}} = -\frac{g_m \overline{v_{nRS}}}{1+g_m R_s}$$

b) $\overline{i_{nd}}$ [$v_s = 0$]

$$\overline{v_s} = \overline{i_{inout}} \cdot R_s$$

$$\overline{i_{inout}} = -g_m v_s + \overline{i_{nd}}$$

$$\overline{i_{inout}} = -g_m (R_s \overline{i_{inout}} + -\overline{v_{nRS}}) + \overline{i_{nd}}$$

$$\overline{i_{inout}} = -g_m R_s \overline{i_{inout}} + \overline{i_{nd}}$$

$$\overline{i_{inout}} = \frac{\overline{i_{nd}}}{1+g_m R_s}$$

$$\left\{ g_m = \frac{1}{R_s} \right. \\ \text{for matching} \left. \right]$$

$$\boxed{\overline{i_{inout}} = \frac{\overline{i_{nd}}}{1+g_m R_s}}$$

$$\text{For } g_m = \frac{1}{R_s}$$

$$\overline{i_{inout}}_1 = \frac{-\overline{v_{nRS}}}{2R_s} ; \quad \overline{i_{inout}}_2 = \frac{\overline{i_{nd}}}{2}$$

So the total noise is $\overline{i_{inout}}_{total}^2 = \overline{i_{inout}}_1^2 + \overline{i_{inout}}_2^2$

$$\overline{i_{inout}}_{total}^2 = \frac{\overline{i_{nd}}^2}{4} + \frac{\overline{v_{nRS}}^2}{4R_s^2}$$

$$\Rightarrow \overline{i_{\text{inout,tot}}^2} = \frac{\overline{i_{\text{ind}}^2}}{4} + \frac{\overline{v_{nR_s}^2}}{4R_s^2}$$

Total N.F. = $\frac{\overline{i_{\text{inout,tot}}^2}}{\overline{i_{\text{inout,RS}}^2}} = 1 + \frac{\overline{i_{\text{ind}}^2}/4}{\overline{v_{nR_s}^2}/4R_s^2}$

Noise Fig = $1 + \frac{4KTR_g d_o \Delta f}{4KTR_s \Delta f}$

Noise Fig = $1 + \frac{r_{gdo} R_s}{g_m} = 1 + \frac{r_{gdo}}{g_m}$

$$\left\{ \frac{g_m n}{g_d} = \alpha \right.$$

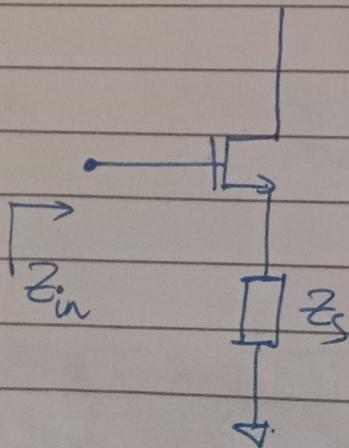
Noise Fig = $1 + \frac{r}{\alpha}$

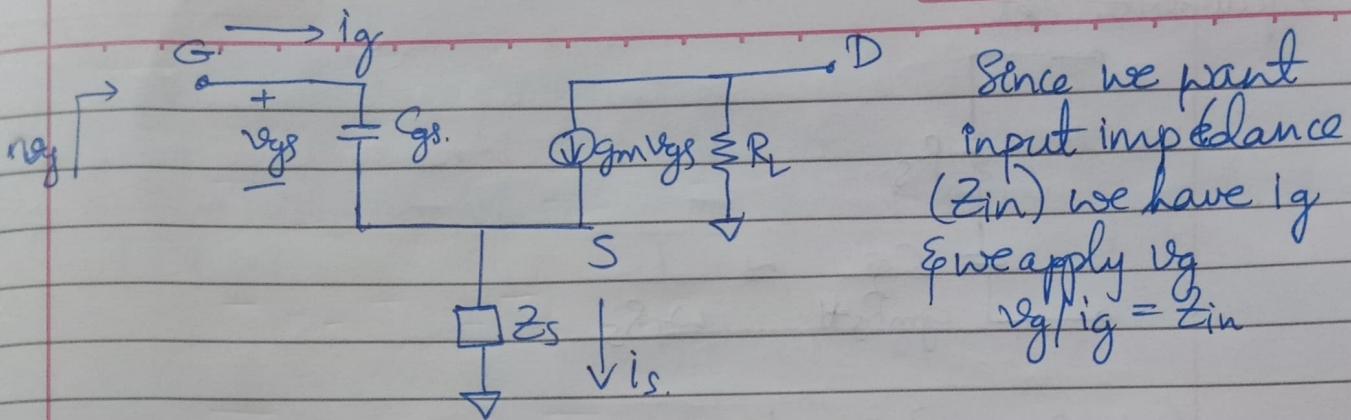
For Long Channel Mosfet
 $r = 2/3, \alpha = 1$

Noise Fig = $1 + 2/3 = 1.67 \Rightarrow \underline{2.2 \text{dB}}$

For short Channel $r \uparrow, \alpha \downarrow$ so Noise Fig \uparrow

4).





Since we want input impedance (Z_{in}) we have i_g & we apply v_g
 $v_g / i_g = Z_{in}$

$$\Rightarrow \frac{v_g - v_{gs}}{Z_s} = g_m v_{gs} + i_g = \frac{v_g}{Z_s} = i_s$$

$$\Rightarrow v_g = i_g Z_s + v_{gs}(g_m Z_s + 1)$$

Now

$$v_{gs} = \frac{i_g}{s C_{gs}}$$

put v_{gs} in previous eqn

$$v_g = i_g Z_s + \frac{(g_m Z_s + 1) i_g}{s C_{gs}}$$

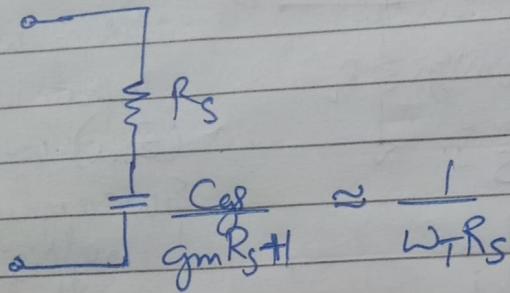
$$\Rightarrow Z_{in} = \frac{v_g}{i_g} = Z_s + \frac{(g_m Z_s + 1)}{s C_{gs}}$$

$$Z_{in} = Z_s + \frac{1}{s C_{gs}} + \frac{g_m Z_s}{s C_{gs}}$$

(Case-1) $Z_s = R_s$

$$Z_{in} = R_s + \frac{1}{s C_{gs}} + \frac{g_m R_s}{s C_{gs}}$$

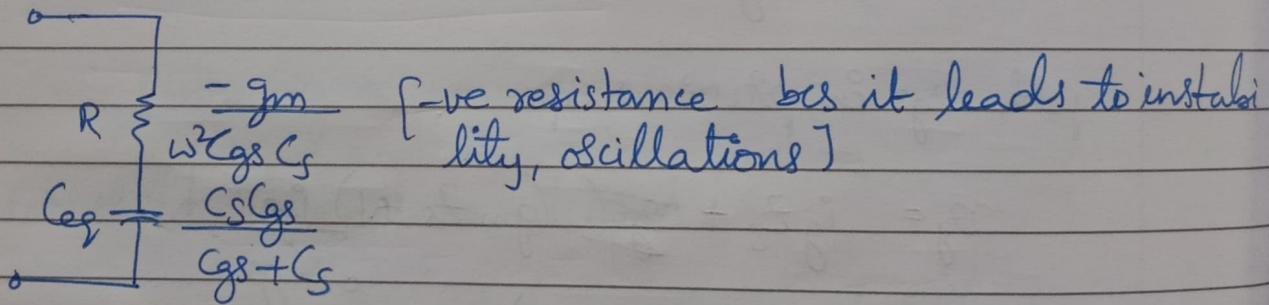
Equivalent ckt



Case-2 $Z_s = \frac{1}{sC_s}$

$$Z_{in} = \frac{1}{sC_s} + \frac{1}{sC_{gs}} + \frac{g_m}{s^2 C_g s C_s}$$

$$Z_{in}(j\omega) = \frac{1}{j\omega} \left[\frac{C_{gs} + C_s}{C_s C_{gs}} \right] + -\frac{g_m}{\omega^2 C_g s C_s}$$

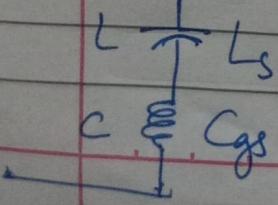


Case-3: $Z_s = sL_s$

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{sC_{gs}}$$

$$Z_{in} = sL_s + \frac{1}{sC_{gs}} + \frac{g_m L_s}{C_{gs}}$$

$R = g_m L_s / C_{gs} \approx \omega_T L_s$ (no noise)



Here we get a Resistor component without adding resistor which is good.

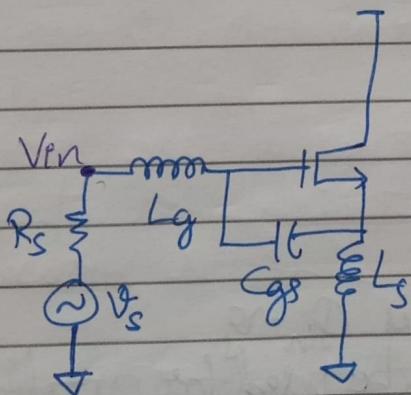
Power Match $w_T L_S = 50\Omega$

But we need to get rid of L_S & C_{gs} so we operate them at resonance

$$f_0 = \frac{1}{2\pi \sqrt{L_S C_{gs}}}$$

So when we design w_T is fixed because it's mosfet behaviour, we design it for Gain Noise, but we can choose L_S such that Z_{in} is matched to 50Ω , Also when we design transistor w_T , C_{gs} are known

so f_0 will become fixed and will not be equal to our desired frequency, so we need another degree of freedom, so we add another inductor at the gate



$$Z_{in} = w_T L_S + jw$$

$$Z_{in} = sL_S + \frac{1}{sC_{gs}} + \frac{w_T L_S}{C_{gs}}$$

here L_S changes to $L_g + L_S$

$$Z_{in} = s(L_g + L_S) + \frac{1}{sC_{gs}} + w_T L_S$$

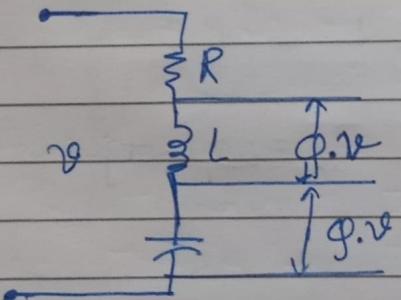
So Now to keep resonant frequency equal to f_0 we set L_g , but obvious resonant frequency will be lower than $\frac{1}{2\pi\sqrt{L_s C_g}}$

$$\Rightarrow f_0 = \frac{1}{2\pi\sqrt{C_g(L_s + L_g)}}$$

Q of a series resonant ntk

$$Q = \frac{\omega L}{R} = \frac{\omega L_{eq}}{R_{eq}}$$

$$Q_{in} = \frac{\omega(L_s + L_g)}{R + \omega L_s}$$



- Here v_{gs} of transistor is $Q_{in} \cdot v_s$
- Series resonant ntk can be used for parallel amplification
- Other advantage of doing this matching is that we get some extra amplification through Q

$$|V_L| = |V_o| = Q |V_{in}| = Q_{in} v_s$$

so

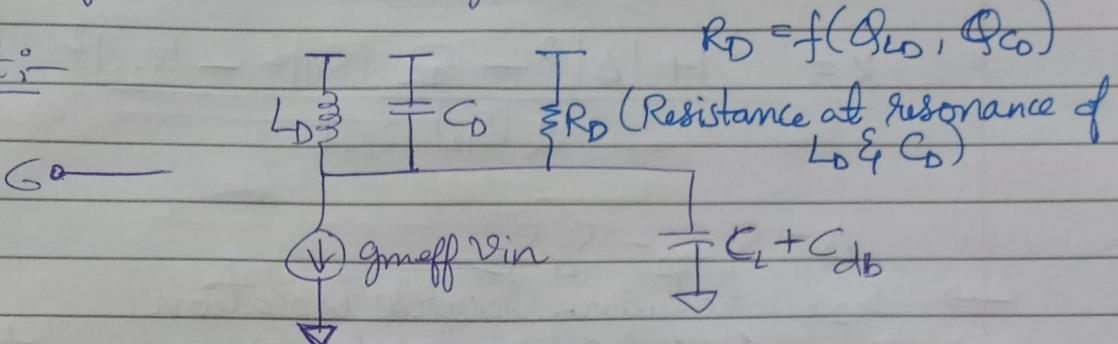
$$\frac{v_{in}}{2} \Rightarrow v_{gs} = 2 Q_{in} v_{in}$$

→ We also choose L_D , C_D such that R_D is max bcs overall gain is $g_{m\text{eff}} R_D$

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$$\Rightarrow g_{m\text{eff}} = (2Q_{in} \cancel{R_D}) gm$$

Output:-



Here we add L_D , C_D because we want narrow band amplifier, if we use R_D it will simply add noise, But when we add resonant circuit we get high impedance at resonance without adding Physical resistor & get narrow band noise & reject wideband Noise

C_L → input capacitor of the next stage

C_{db} → depletion capacitors between the drain and bulk

Here we are neglecting g_{ds} bcs R_D will be less compared to g_{ds}

$$f_0 = \frac{1}{2\pi \sqrt{L_D(C_D + C_L + C_{db})}}$$

Here so that resonant frequency is not susceptible to parasitic capacitance we make

$$C_D \gg C_{db}, C_L \quad [C_D \gg C_{db} + C_L]$$

so that C The parasitic are dependent on your mosfet size
 \rightarrow because you donot want to be dependant on that bcs off is mixer, if mixer changes you dont want to redo LNA design

Stability:-

→ Stern stability factor

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|}$$

$$\Delta = S_{11}S_{22} - S_{21}S_{12}$$

- $S_{21} \downarrow$ reducing reverse isolation
- $K > 1, \Delta < 1$ for stability \Rightarrow unconditionally stable
- S_{11} for ip match very small, S_{22} for dp match very small, S_{21} is power gain
- C_{gd} is related to S_{12} [This is ip impedance, this has negative resistor component proportional to C_{gd}]
 - $C_{gd} \uparrow$ bad the -ve Resistor

$S_{11}, S_{22} \rightarrow$ Return Loss

$$S_{11} = 20 \log \left| \frac{Z_{in} - R_s}{Z_{in} + R_s} \right|$$

Stability

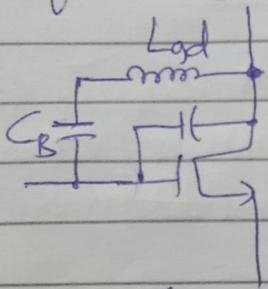
- Input and output matches in case LNA, where we need to do both matching, but there will be some dependence bcs we gm the forward way & C_{gd} the reversed way
- We match opamp, I/p it is discrete LNA or at the o/p of LNA ~~as~~ it might need filtering, usually that filter will be an offchip/moschip filter then we have to SOT matching again
- If we don't do the above then we don't do matching at the output, we would include the load of the mixer as part of the tuned ckt

See C_{gd} is a problem

$$C_{gd} \leftrightarrow S_{12}$$

Bonito force Method [Tune out your C_{gd}]

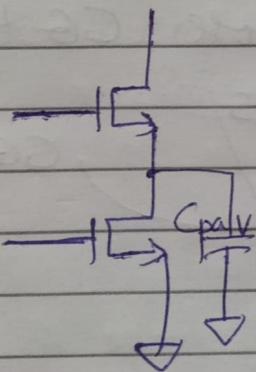
1)



To get rid of C_{gd} we use resonance so we use an inductor but we cannot connect inductor directly so we put a capacitor. we can tune L_{sd} to tune out the C_{gd}

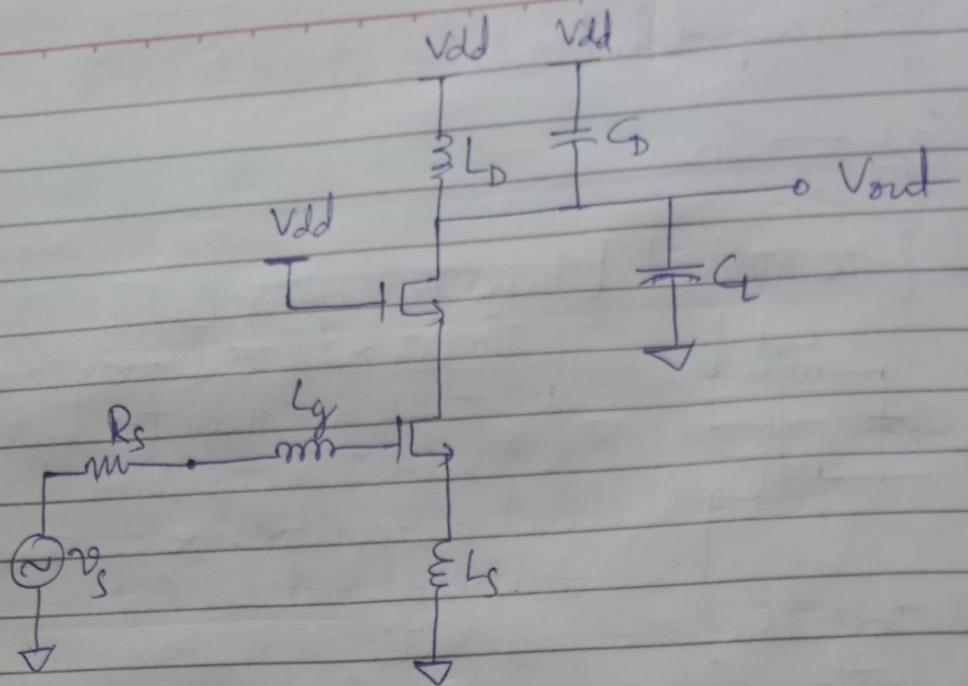
Inductors also have parasitic capacitors, capacitors with bottom plane capacitance & parasitic capacitance all of this will load your input Node. Also size Inductor is large so cannot add Inductor anywhere we want

2) Cascode

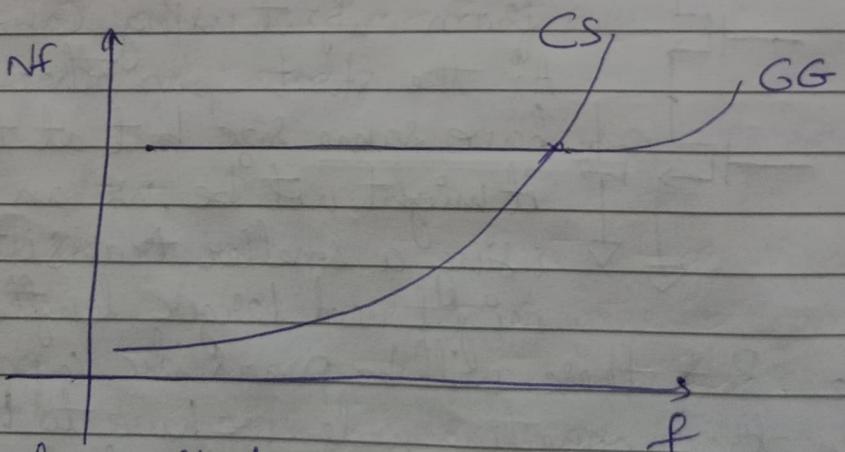


We effectively isolate our input from output using Cascode
At the start your other mosfet will have same size but at the end it might not be, we can make it using a smaller transistor or might need larger length to the cascode.

But there will be parasitic capacitance between the connecting node. we have to limit this C_{pkv} because signal is going to get diverted through that & gate of the cascode is typically connected to Vdd (because we want to give importance to main amplifier)



- we know the CS Amplifier less NF_{min}, we get it like 0.6, 0.7 even for a long channel
- we also know CS Amplifier has higher gain but we are doing narrow band match at i/p & it is opposed to CG structure which has wide band
- For some cases we can choose GG topology



- we know that NF of CS is directly proportional to w/w_T ~~& not~~ & not 3dB [that is only if you are using resistance at the input], for this f_{min} is smaller. So there will be point where GG works better but for pretty high frequency to achieve that [H + R_A]

4) Voltage Gain (A_v)

$$A_v = \frac{V_{out}}{V_{in}} = G_m R_p$$

$[G_m = \text{eff gm}]$

$$A_v = 2Q_{in} g_m R_p$$

$(R_p = \text{parallel resistance of the tank})$

→ Here we are neglecting output resistance of the tank now that we use cascode the output impedance of the amplifier gets even better

5) Transducer Power Gain (G_T):

For a port we can define G_T

$$G_T = \frac{\text{Power delivered to the load}}{\text{max Power available from source}} = \frac{P_{load}}{P_{ark}}$$

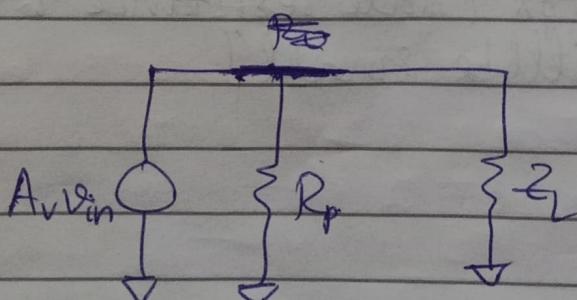
$$P_{ark} = \frac{|V_{in}|^2}{2R_s}$$

Load [max Power available from source when z_L is matched]

$$Y_L = \frac{1}{Z_L} \quad \text{so we don't have constraint over load so load can be anything}$$

Let's take Real part

$$G_L = \text{Re}\left(\frac{1}{Z_L}\right)$$



$$P_{load} = \frac{|V_{out}|^2}{2} \cdot G_L$$

$$= \frac{|V_{out}|^2}{2} \text{Re}\left(\frac{1}{Z_L}\right)$$

$$|V_{out}|^2 = G_m (R_p || Z_L) |V_{in}|^2$$

$[A_v \text{ won't change}]$

$$P_{load} = \frac{1}{2} \operatorname{Re} \left(\frac{1}{Z_L} \right) \cdot \frac{1}{2} \cdot |G_m(R_p || Z_L)|^2 |v_{in}|^2$$

$$G_f = |G_m(R_p || Z_L)|^2 \operatorname{Re} \left(\frac{1}{Z_L} \right) \cdot R_s \text{ [Transducer Gain]}$$

This is true for any 2-port

- a) Let's say the LNA is driving some offchip or something [output is Matched]
Matched Load:

$$[R_p = Z_L]$$

$$G_f = |G_m \frac{(R_p)}{2}|^2 \cdot \frac{R_s}{R_p}$$

$$\boxed{G_f = \frac{G_m^2 R_s R_p}{4}}$$

→ This also happens to be available power at load under Max condn and power available from source under max condn

- b) Let's say we are driving a mixer [Capacitive load]
 [Capacitive load]

$$G_f \rightarrow 0$$

because if the i/p of the next stage is capacitive (MOSFET) is purely or some gate resistance is present along with capacitor [gate resistance will be tried to be minimized so it'll be small]

Power Consumption:-

To achieve min Noise figure the amt of power we need to burn is huge to get NF so we need to do Power Constraint Noise optimization [Power upper limit] and we need to calculate NF based on that [derivation is complicated so just take the Result] [Book T. Lee . Page no 380-384]

$$F = F_{\min} + \frac{R_n}{G_s} [(G_s - G_{\text{opt}})^2 + (B_s - B_{\text{opt}})^2]$$

We assume imaginary part $B_s - B_{\text{opt}}$ is very small Then we define

$$\Phi_{\text{opt}} = \frac{G_{\text{opt}}}{w G_s} = \alpha \sqrt{\frac{s}{5r} (1 - |c|^2)}$$

$$\Phi_s = \frac{1}{w G_s R_s}$$

so we want to arrive at it an optimum width of the transistor given a power dissipation bound so G_s depends on the width of the transistor so we want to find optimum Φ_s

$$f = f_{\min} + \frac{r}{2 g_m R_s} \left[1 - \frac{\Phi_{\text{opt}}^2}{\Phi_s^2} \right]$$

so optimum $\Phi_{s,\text{opt}} \approx 4.5$

$$\text{So } W_{\text{opt},P} = \frac{3}{2} \frac{1}{L C_o R_s \Phi_{s,P}}$$

$$\text{So } C_{gs} = \frac{2}{3} WL Cox \quad [C_{gs} = \frac{2}{3} WL Cox]$$

Put $Q_{sp} = 4.5$

$$W_{opt, p} = \frac{1}{3WL Cox R_s}$$

so Q_{sp} is the power constraint Q_s , optimized Q_s after you've applied Power Constraint, so for $Q_s = 4.5$ we can get good NF with for a given power and it is fairly broad band w.r.t to many parameters like W, L, S, R, W also Power consumption

So Finally

$$* F_{min, p} = 1 + 2.4 \frac{r}{\omega} \left[\frac{\omega}{\omega_T} \right]$$

put r, α

$$F_{min} = 1 + 2.3 \left[\frac{\omega}{\omega_T} \right]$$

ω_T/ω	F_{min}	$F_{min, P}$
20	0.5	1.1
15	0.6	1.4
10	0.9	1.9
5	1.6	3.3

Power comes in through ω_T , so you burn more power we get better ω_T

$$r = 2, S = 4, \alpha = 0.85$$

$$\omega_T = \frac{g_m}{C_{gs}} = \frac{g_m}{\frac{2}{3} WL Cox}$$

ω_T will be fixed if you fix size and current

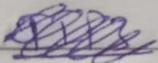
→ Assuming that we use min length to get max W_T and also to get min Noise figure

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If you burn more current I_{bias} gm increases so W_T increases

Design Procedure:

- 1) Determine $W_{opt,p}$ as above
- 2) Choose I_{bias} based on Power dissipation
- 3) Determine L_s [$\omega_L L_s = 50 \pi^2 = R_s$]
- 4) Calculate Nf_{min}
- 5) L_g based on f_0 [such that i_p is matched at desired frequency]
- 6) ~~to R_C~~ Use cascode [cascode will be same as main transistor in beginning]
- 7) Choose load L_o, C_o so that you maximize R_p [Achieve more gain at lower current]



In differential topology it'll give better linearity but NF is same

Ways to maximize R_p

→ Here it is coming through L_o (assume ideal capacitor) so i_{cap} is much larger. Let's say we choose L of $1mH$, for G of 10 we get particular parallel resistance, if we don't get good gain we have to use $2/3$ times higher inductor, but when we do that C_o comes down, which means we cannot tune out the load [it becomes sensitive]

II P3

W_T MOSFET is not a short channel & doesn't behave in square law, so it is very difficult to calculate II P3. bcs it'll be far off from our measurements

So after we go through design procedure and simulate TIP3 see if it looks good, if it doesn't look good only way is to increase $V_{GS} - V_T$ because TIP3 is related to $V_{GS} - V_T$ & B . So if we increase V_{DSAT} then TIP3

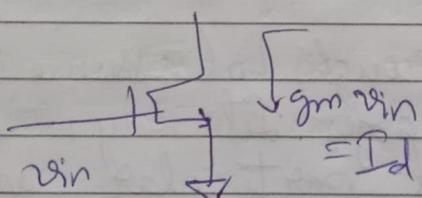
$$I_{bias} \uparrow \Rightarrow (V_{GS} - V_T) \uparrow = TIP3 \text{ improve}$$

Short Channel effects depends on $V_{GS} - V_T$, so if we increase $V_{GS} - V_T$ we are going deeper into short channel regime [$\lambda = \frac{g_m}{g_{d0}}$, for long channel mosfet it is 1, for short it'll decrease from 1 (0.85), so $NF \downarrow$] so λ reduces NF increases. also I_{bias} increases W/L will increase, so $NF \downarrow$

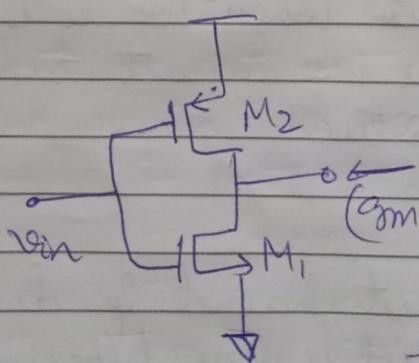
$NF \propto \frac{1}{f_T}$, but λ also depends

Look at

1) Current Reuse



If we take a single mosfet its transconductance is $g_m v_{in}$



Instead of single mosfet we can make nmos pmos amplifiers. This to get more gain for given current. However we match the output impedance needs to be small.

Let's say the output is capacitor, obviously this will be low output impedance node so we might need an inductor to tune out the capacitor.

2) Feedback :-

$$* R_{in} = 50\Omega$$

* Improve IIP3

cons are

- NF ↑ & Gain will decrease & increase in Power,
- stability changes

Rules of thumb:

→ Same $\frac{W}{L}$ for calculate E_g gate = Vdd

→ f_T , we need a starting point for W, larger W we start with, the more headroom we'll have for main transistor & better IIP3.

→ W_{opt} has to be chosen such way that we get some f_T

$$f_T \geq 10f$$

If this condition is taken into consideration our NF will be something like 2dB or 1.9dB

→ Model noise accurately (take care of r_s & s)

→ Simulation :-

1) Hand Calculation

2) Characterise it so that what happens when things

- change [like g_m , input impedance dependence as a function of current] such as Noise

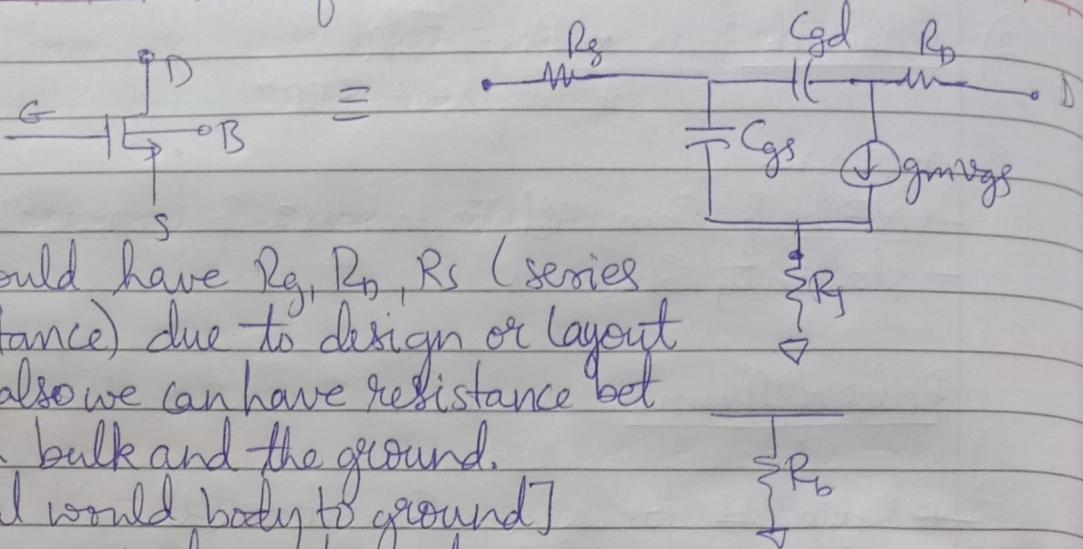
→ Our hand calculation is for square law devices
plot f_T , g_m , Γ as a function of I_{bias} & Width
also Noise of the transistor, instead of starting with W_{opt} we can do it start with given current density & move on

NF v/s I-density

→ $NF_{opt} \neq Gain_{opt} \neq IIP_{opt}$

so optimum point for each pt will be diff. so choose such way it meets overall spec

Extrinsic Sources of Noise [MOSFET]



→ we could have R_g , R_s , R_b (series Resistance) due to design or layout and also we can have resistance between bulk and the ground.

[ideal would body to ground]

Here majorly we have to worry about R_g

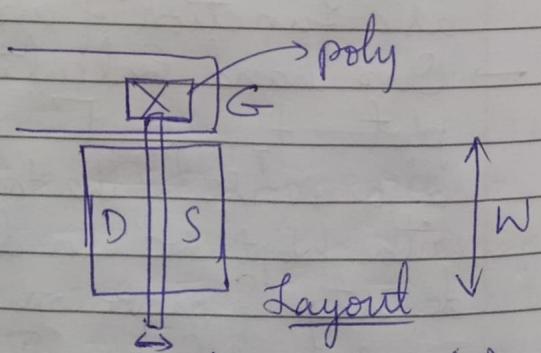
i) R_g :- Resistance of gate, Normally gate, drain resistance will be small, in a normal design and good layout we have to worry about R_g and R_s . Drain Source series resistances will be due to metal [metal] lines. But R_g relates to your transistor width and length. Drain and source contact through metal directly to the diffusion. Problem of the gate is it contacts from the metal to down to poly [which is relatively high resistivity and poly itself is the gate].

$$\frac{R_g}{L} = \frac{10\mu}{0.13\mu}$$

but we put contacts on the drain & source and take it out as metal

Gate Resistance

Transistor is a distributive structure, the gate signal is coming in from here & travelling down so we are lumping it as lumped Resistor R_g but we'll have poly Resistance



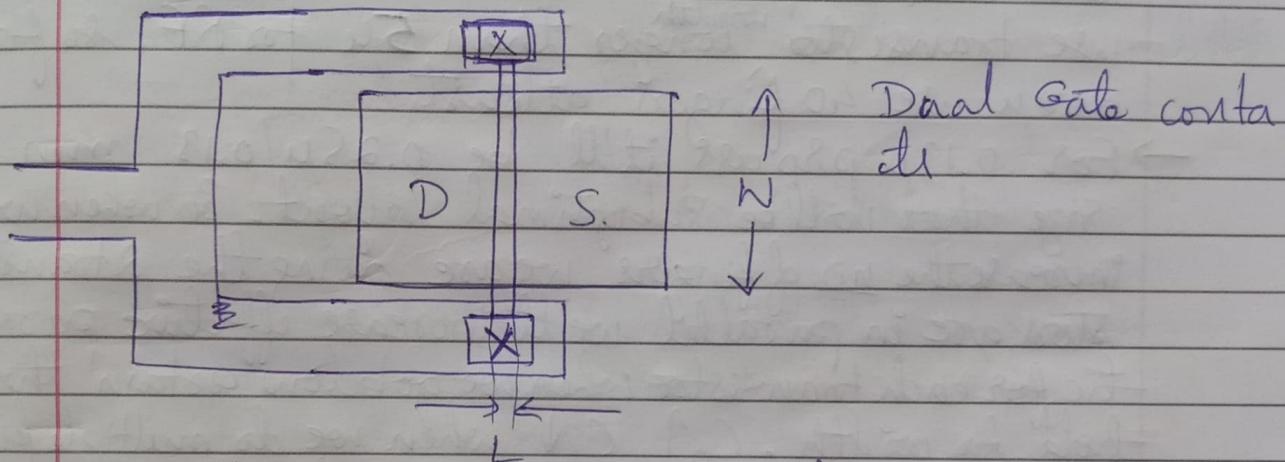
length of transistor (L)

assume

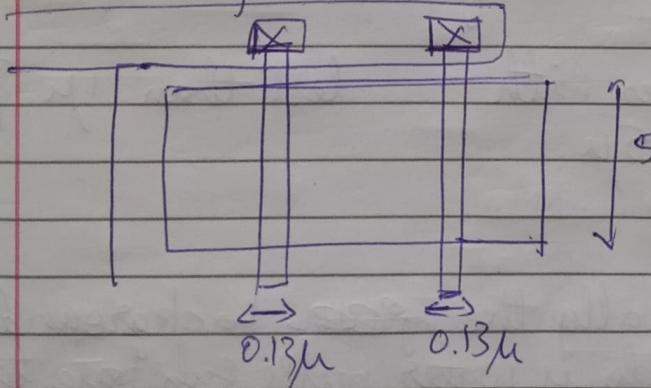
Rmetal \ll Rpoly

We can do is we are contacting it from one side, we can put similar gate contact on the other side. But this will half the existing Resistor which is good.

→ Dual-gate contacts [in fact if we pickup RF process the transistors (RF transistors) will have dual gate contact already]

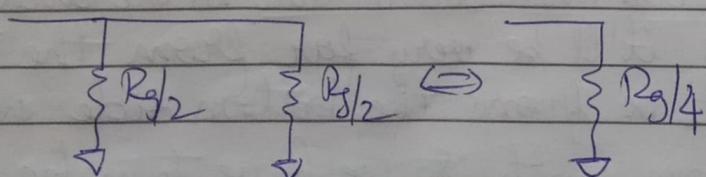


→ The other thing we can do is fold the transistor vertically down



Here we can do dual gate contact also and trade off R_g , R_{ds} is called Multi Fingered contact. Here gate Resistance will be half

So it'll be like, so the actual Resistance will be $R_g/4$



In a way we have half the poly length and $R_g/2 \parallel R_g/2$ so we have $R_g/4$

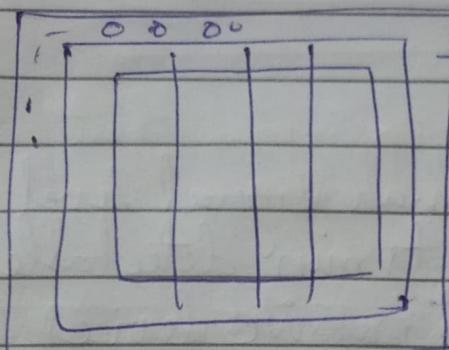
The General eqn be like

- This is given bcs, let's say we've 200 μ transistor and don't use single finger with 200 μ long, this will be problematic. So in a sense do not use transistors ^{width} longer than 5 μ for RF, so for 200 μ use 40 fingers atleast
- For 0.13 μ process it'll be 0.25 μ /0.13 min size that will be suboptimal layout. So when we increase the no. of fingers we are doing the 2 transistors are in parallel we'll increase effective parasitic for each transistor when we go below certain threshold fix width. $C_o \uparrow, C_s \downarrow$ when we do multiple fingers. But problem is also from layout, when we do layout we will know that a lot of noise comes from gate terminal
- Don't have finger with less than 1 μ & not larger than 5 μ

2) R_b

The Bulk is actually the ~~poly~~ background, normally what we do is water pulse substrate taps or bulk contacts around transistors, Effectively there will be a common connection to the bulk for the overall chip but it'll be very far from the transistor and it'll be from the bottom side which will be at a 500 μ depth, so we have to make sure that this transistor has good bulk contact

To do that in normal RF layout, we see



→ Substrate Ring [Ring around the substrate full of substrate contact] bcs we've to make sure the RF transistors are especially sensitive to substrate effect, so we make sure it has very good

substrate may be far away, what we try to do is we'll connect it here & connect it on metal to a good ground. This won't affect schematics we've to model this effect separately

$R_b \rightarrow 4KTR_b \Delta f$ (at the bulk node)

$$\overline{i_{d,sub}^2} = 4KTR_b g_{mbs}^2 \Delta f$$