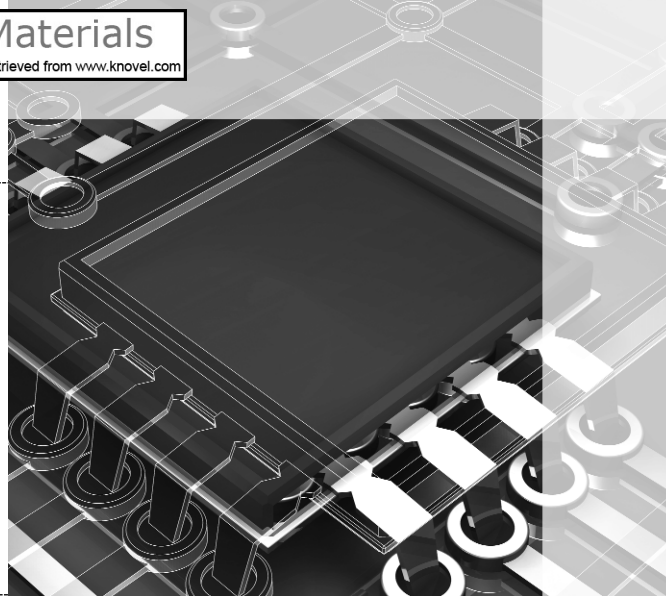

CHAPTER 6

CMOS Operational Amplifiers

The operational amplifier, which has become one of the most versatile and important building blocks in analog circuit design, is introduced in this chapter. The operational amplifier (op amp) fits into the scheme of Table 1.1-2 as an example of a complex circuit. The unbuffered operational amplifiers developed in this chapter might be better described as operational-transconductance amplifiers since the output resistance typically will be very high (hence the term "unbuffered"). The term "op amp" has become accepted for such circuits, so it will be used throughout this text. The terms "unbuffered" and "buffered" will be used to distinguish between high output resistance (operational-transconductance amplifiers or OTAs) and low output resistance amplifiers (voltage operational amplifiers). Chapter 7 will examine op amps that have low output resistance (buffered op amps).

Operational amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer function is practically independent of the gain of the op amp. This principle has been exploited to develop many useful analog circuits and systems. The primary requirement of an op amp is to have an open-loop gain that is sufficiently large to implement the negative feedback concept. Most of the amplifiers in Chapter 5 do not have a large enough gain. Consequently, most CMOS op amps use two or more stages of gain. One of the most popular op amps is a two-stage op amp. We will carefully examine the performance of this type of op amp for several reasons. The first is because it is a simple yet robust implementation of an op amp and second, it can be used as the starting point for the development of other types of op amps.

The two-stage op amp will be used to introduce the important concept of compensation. The goal of compensation is to maintain stability when negative feedback is applied around the op amp. An understanding of compensation, along with the previous concepts, provides the necessary design relationships to formulate a design approach for the two-stage op amp. In addition to the two-stage op amp, this chapter will examine the folded-cascode op amp. This amplifier was developed in order to improve the power-supply rejection ratio performance of the two-stage op amp. The folded-cascode op amp is also an example of a self-compensated op amp.

Simulation and measurement of op amp performance will be the final subjects of this chapter. Simulation is necessary to verify and refine the design. Experimental measurements

are necessary to verify the performance of the op amp with the original design specifications. Typically, the techniques applicable to simulation are also suitable for experimental measurement.

6.1 Design of CMOS Op Amps

Figure 6.1-1 shows a block diagram that represents the important aspects of an op amp. CMOS op amps are very similar in architecture to their bipolar counterparts. The differential-transconductance stage introduced in Section 5.2 forms the input of the op amp and sometimes provides the differential to single-ended conversion. Normally, a good portion of the overall gain is provided by the differential-input stage, which improves noise and offset performance. The second stage is typically an inverter similar to that introduced in Section 5.1. If the differential-input stage does not perform the differential-to-single-ended conversion, then it is accomplished in the second-stage inverter. If the op amp must drive a low-resistance load, the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing. Bias circuits are provided to establish the proper operating point for each transistor in its quiescent state. As noted in the introduction, compensation is required to achieve stable closed-loop performance. Section 6.2 will address this important topic.

Ideal Op Amp

Ideally, an op amp has infinite differential-voltage gain, infinite input resistance, and zero output resistance. In reality, an op amp only approaches these values. For most applications where unbuffered CMOS op amps are used, an open-loop gain of 2000 or more is usually sufficient. The symbol for an op amp is shown in Fig. 6.1-2, where, in the nonideal case, the output voltage v_{OUT} can be expressed as

$$v_{OUT} = A_v (v_1 - v_2) \tag{6.1-1}$$

A_v is used to designate the open-loop differential-voltage gain. v_1 and v_2 are the input voltages applied to the noninverting and inverting terminals, respectively. The symbol in Fig. 6.1-2 also shows the power-supply connections of V_{DD} and V_{SS}. Generally, these connections are not shown but the designer must remember that they are an integral part of the op amp.

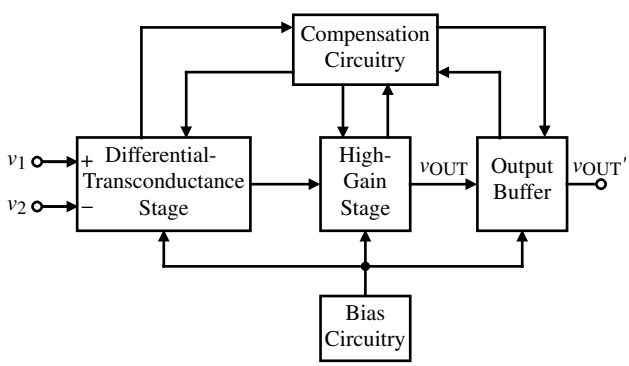

Figure 6.1-1 Block diagram of a general two-stage op amp.

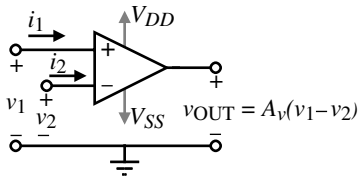

Figure 6.1-2 Symbol for an operational amplifier.

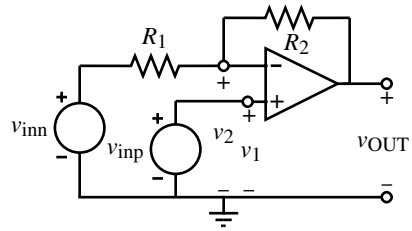

Figure 6.1-3 General configuration of the op amp as a voltage amplifier.

If the gain of the op amp is large enough, the input port of the op amp becomes a *null port* when negative feedback is applied. A null port (or *nullor*) is a pair of terminals to a network where the voltage across the terminals is zero and the current flowing into or out of the terminals is also zero [1]. In terms of Fig. 6.1-2, if we define

$$v_i = v_1 - v_2 \tag{6.1-2}$$

and

$$i_i = i_1 = -i_2 \tag{6.1-3}$$

then

$$v_i = i_i = 0 \tag{6.1-4}$$

This concept permits the analysis of op amp circuits with negative feedback to be very simple. This will be illustrated shortly.

Figure 6.1-3 shows the typical implementation of a voltage amplifier using an op amp. Returning the output through R_2 to the inverting input provides the negative feedback path. The input may be applied at the positive or negative inputs. If only v_{inp} is applied ($v_{inn} = 0$), the voltage amplifier is called *noninverting*. If only v_{inn} is applied ($v_{inp} = 0$), the voltage amplifier is called *inverting*.

Example 6.1-1

Simplified Analysis of an Op Amp Circuit

The circuit shown in Fig. 6.1-4 is an inverting voltage amplifier using an op amp. Find the voltage-transfer function, v_{out}/v_{in}.

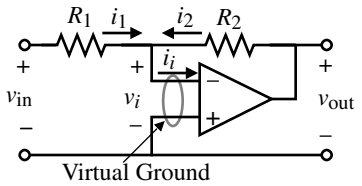

Figure 6.1-4 Inverting voltage amplifier using an op amp.

SOLUTION

If the differential-voltage gain, A_v, is large enough, then the negative feedback path through R_2 will cause the voltage v_i and the current i_i shown on Fig. 6.1-4 to both be zero. Note that the null port becomes the familiar *virtual ground* if one of the op amp input terminals is on ground. If this is the case, then we can write that

$$i_1 = \frac{v_{\text{in}}}{R_1}$$

and

$$i_2 = \frac{v_{\text{out}}}{R_2}$$

Since $i_i = 0$, then $i_1 + i_2 = 0$, giving the desired result as

$$\frac{v_{\text{out}}}{v_{\text{in}}} = -\frac{R_2}{R_1}$$

Characterization of Op Amps

In practice, the operational amplifier only approaches the ideal infinite-gain voltage amplifier. Some of its other nonideal characteristics are illustrated in Fig. 6.1-5. The *finite differential-input impedance* is modeled by R_{id} and C_{id}. The *output resistance* is modeled by R_{out}. The *common-mode input resistances* are given as resistors of R_{icm} connected from each of the inputs to ground. V_{OS} is the *input-offset voltage* necessary to make the output voltage zero if both of the inputs of the op amp are grounded. I_{OS} (not shown) is the *input-offset current,* which is necessary to make the output voltage zero if the op amp is driven from two identical current sources. Therefore, I_{OS} is defined as the magnitude of the difference between the two *input-bias currents* I_{B1} and I_{B2}. Since the bias currents for a CMOS op amp are approximately zero, the offset current is also zero. The *common-mode rejection ratio* (CMRR) is modeled by the voltage-controlled voltage source indicated as v_1/CMRR. This

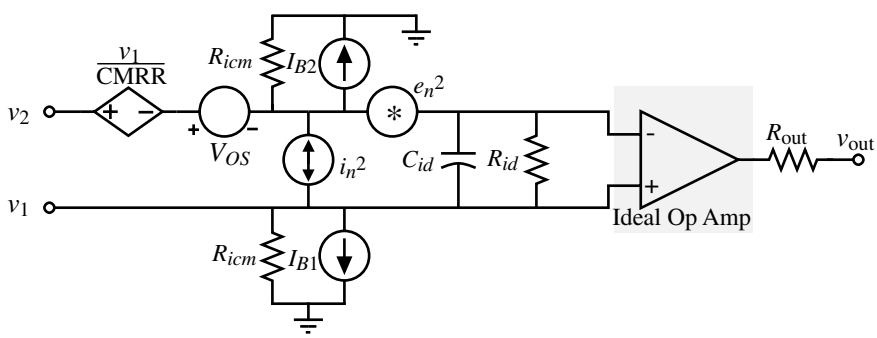

Figure 6.1-5 A model for a nonideal op amp showing some of the nonideal linear characteristics.

source approximately models the effects of the common-mode input signal on the op amp. The two sources designated as e_n^2 and i_n^2 are used to model the op amp noise. These are *rms voltage- and current-noise sources* with units of mean-square volts and mean-square amperes, respectively. These noise sources have no polarity and are always assumed to add.

Not all of the nonideal characteristics of the op amp are shown in Fig. 6.1-5. Other pertinent characteristics of the op amp will now be defined. The output voltage of Fig. 6.1-2 can be defined as

$$V_{\text{out}}(s) = A_v(s)\,[V_1(s) - V_2(s)] \pm A_c(s)\left(\frac{V_1(s) + V_2(s)}{2}\right) \tag{6.1-5}$$

where the first term on the right is the differential portion of $V_{\text{out}}(s)$ and the second term is the common-mode portion of $V_{\text{out}}(s)$. The *differential-frequency response* is given as $A_v(s)$ while the *common-mode frequency response* is given as $A_c(s)$. A typical differential-frequency response of an op amp is given as

$$A_v(s) = \frac{A_{v0}}{\left(\frac{s}{p_1} - 1\right)\left(\frac{s}{p_2} - 1\right)\left(\frac{s}{p_3} - 1\right)\cdots} \tag{6.1-6}$$

where $p_1, p_2, \ldots$ are poles of the operational amplifier open-loop transfer function. In general, a pole designated as p_i can be expressed as

$$p_i = -\omega_i \tag{6.1-7}$$

where ω_i is the reciprocal time constant or break-frequency of the pole p_i. While the operational amplifier may have zeros, they will be ignored at the present time. A_{v0} or $A_v(0)$ is the gain of the op amp as the frequency approaches zero. Figure 6.1-6 shows a typical frequency response of the magnitude of $A_v(s)$. In this case we see that ω_1 is much lower than the rest of the break-frequencies, causing ω_1 to be the dominant influence in the frequency response. The frequency where the -6 dB/oct. slope from the dominant pole intersects with the 0 dB axis

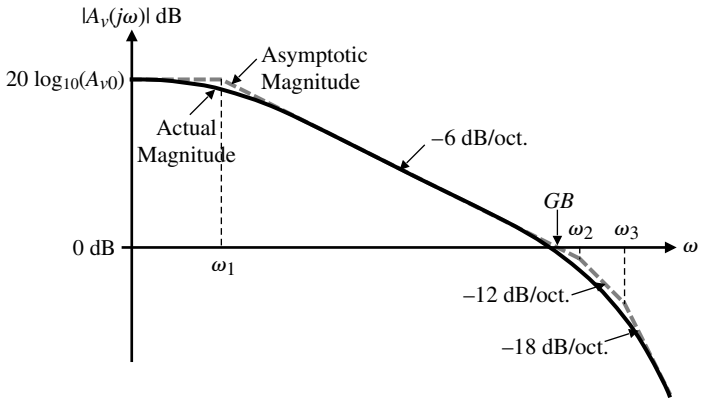

Figure 6.1-6 Typical frequency response of the magnitude of $A_v(j\omega)$ for an op amp.

is designated as the *unity-gain bandwidth,* abbreviated *GB,* of the op amp. Even if the next higher order poles are smaller than *GB,* we shall still continue to use the unity-gain bandwidth as defined above.

Other nonideal characteristics of the op amp not defined by Fig. 6.1-5 include the *power-supply rejection ratio,* PSRR. The PSRR is defined as the product of the ratio of the change in supply voltage to the change in output voltage of the op amp caused by the change in the power supply and the open-loop gain of the op amp. Thus,

$$\text{PSRR} = \frac{\Delta V_{DD}}{\Delta V_{\text{OUT}}} A_v(s) = \frac{V_o/V_{\text{in}}(V_{dd} = 0)}{V_o/V_{dd}(V_{\text{in}} = 0)} \tag{6.1-8}$$

An ideal op amp would have an infinite PSRR. The reader is advised that both this definition for PSRR and its inverse will be found in the literature. The *common-mode input range* is the voltage range over which the input common-mode signal can vary. Typically, this range is 1–2 V less than V_{DD} and 1–2 V more than V_{SS}.

The output of the op amp has several important limits, one of which is the maximum output current sourcing and sinking capability. There is a limited range over which the output voltage can swing while still maintaining high-gain characteristics. The output also has a voltage rate limit called *slew rate.* The slew rate is generally determined by the maximum current available to charge or discharge a capacitance. Normally, slew rate is not limited by the output, but by the current sourcing/sinking capability of the first stage. The last characteristic of importance in analog sampled-data circuit applications is the *settling time.* This is the time needed for the output of the op amp to reach a final value (to within a predetermined tolerance) when excited by a small signal. This is not to be confused with slew rate, which is a large-signal phenomenon. Many times, the output response of an op amp is a combination of both large- and small-signal characteristics. Small-signal settling time can be completely determined from the location of the poles and zeros in the small-signal equivalent circuit, whereas slew rate is determined from the large-signal conditions of the circuit.

The importance of the settling time to analog sampled-data circuits is illustrated by Fig. 6.1-7. It is necessary to wait until the amplifier has settled to within a few tenths of a percent of its final value in order to avoid errors in the accuracy of processing analog signals. A longer settling time implies that the rate of processing analog signals must be reduced.

Fortunately, the CMOS op amp does not suffer from all of the nonideal characteristics previously discussed. Because of the extremely high input resistance of the MOS devices, both R_{id} and I_{OS} (or I_{B1} and I_{B2}) are of no importance. A typical value of R_{id} is in the range of 10^{14} Ω. Also, R_{icm} is extremely large and can be ignored. If an op amp is used in the configuration of Fig. 6.1-3 with the noninverting terminal on ac ground, then all common-mode characteristics are unimportant.

Classification of Op Amps

In order to understand the design of CMOS op amps it is worthwhile to examine their classification and categorization. It is encouraging that op amps that we are totally unfamiliar with at this point can be implemented using the blocks of the previous two chapters. Table 6.1-1 gives a hierarchy of CMOS op amps that is applicable to nearly all CMOS op amps that will be presented in this chapter and the next. We see that the differential amplifier is almost ubiquitous

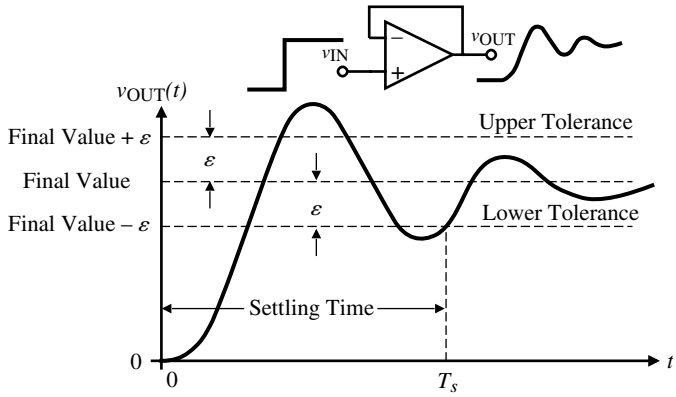

Figure 6.1-7 Transient response of an op amp with negative feedback illustrating settling time T_S. ε is the tolerance to the final value used to define the settling time.

in its use as the input stage. We will study several op amps in the next chapter that use a modified form of the differential amplifier of Section 5.2 but by and large the differential amplifier is the input stage of choice for most op amps.

As we have shown previously, amplifiers generally consist of a cascade of voltage-to-current or current-to-voltage converting stages. A voltage-to-current stage is called a *transconductance stage* and a current-to-voltage stage is called the *load stage.* In some cases, it is easier to think of a current-to-current stage, but eventually current will be converted back to voltage.

Based on the categorization in Table 6.1-1, there are two major op amp architectures that we will study in this chapter. The first is the two-stage op amp. It consists of a cascade of $V \rightarrow I$ and $I \rightarrow V$ stages and is shown in Fig. 6.1-8. The first stage consists of a differential amplifier converting the differential input voltage to differential currents. These differential currents are applied to a current-mirror load recovering the differential voltage. This of course is nothing more than the differential voltage amplifier of Fig. 5.2-5 or 5.2-7. The second stage consists of a common-source MOSFET converting the second-stage input voltage to current. This transistor is loaded by a current-sink load, which converts the current to voltage at the output.

Table 6.1-1 Categorization of CMOS Op Amps

Conversion	Hierarchy			
Voltage to current	Classic differential amplifier	Modified differential amplifier		First voltage stage
Current to voltage	Differential-to-single-ended load (current mirror)	Source/sink current loads	MOS diode load	
Voltage to current	Transconductance grounded gate	Transconductance grounded source		Current stage
Current to voltage	Class A (source or sink load)	Class B (push–pull)		Second voltage stage

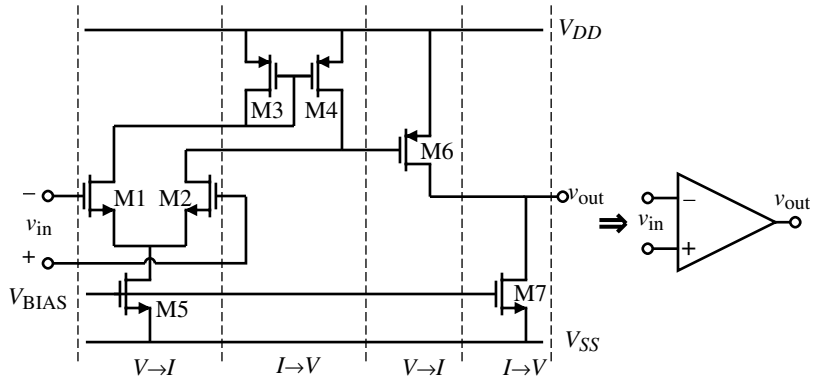

Figure 6.1-8 Classical two-stage CMOS op amp broken into voltage-to-current and current-to-voltage stages.

The second stage is also nothing more than the current-sink inverter of Fig. 5.1-7. This two-stage op amp is so widely used that we will call it the *classical two-stage op amp;* it has both MOSFET and BJT versions.

A second architecture that results is shown in Fig. 6.1-9. This architecture is commonly called the *folded-cascode op amp.* This architecture was developed in part to improve the input common-mode range and the power-supply rejection of the two-stage op amp. In this particular op amp, it is probably more efficient to consider it as the cascade of a differential-transconductance stage with a current stage followed by a cascode current-mirror load. One of the advantages of the folded-cascode op amp is that it has a push–pull output. That is, the op amp can actively sink or source current from the load. The output stage of the previous two-stage op amp is Class A, which means that either its sinking or sourcing capability is fixed.

Slight modifications in the two op amps of Figs. 6.1-8 and 6.1-9 result in many possible other forms (see Problems 6.1-5 and 6.1-6). However, for the purposes of space and simplicity we will restrict our present considerations to these two CMOS op amps.

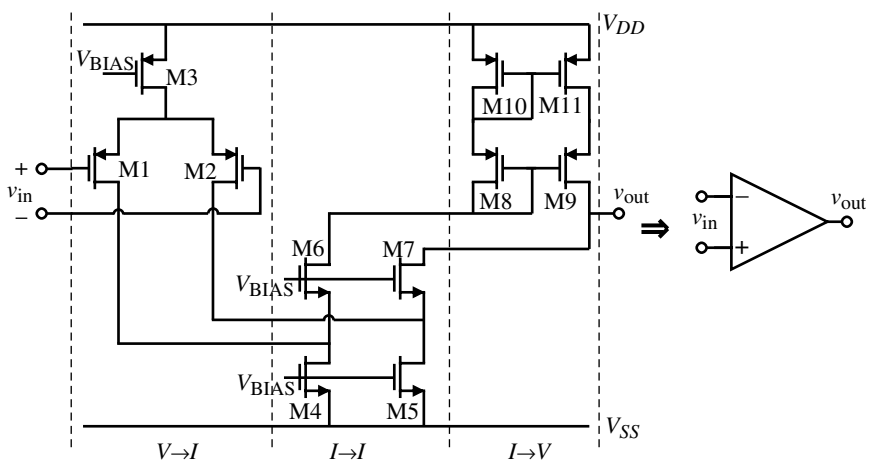

Figure 6.1-9 Folded-cascode op amp broken into stages.

Design of Op Amps

The design of an op amp can be divided into two distinct design-related activities that are for the most part independent of one another. The first of these activities involves choosing or creating the basic structure of the op amp. A diagram that describes the interconnection of all of the transistors results. In most cases, this structure does not change throughout the remaining portion of the design, but sometimes certain characteristics of the chosen design must be changed by modifying the structure.

Once the structure has been selected, the designer must select dc currents and begin to size the transistors and design the compensation circuit. Most of the work involved in completing a design is associated with this, the second activity of the design process. Devices must be properly scaled in order to meet all of the ac and dc requirements imposed on the op amp. Computer circuit simulations, based on hand calculations, are used extensively to aid the designer in this phase.

Before the actual design of an op amp can begin, though, one must set out all of the requirements and boundary conditions that will be used to guide the design. The following list describes many of the items that must be considered.

Boundary conditions:

1. Process specification (V_T, K', C_{ox}, etc.)
2. Supply voltage and range
3. Supply current and range
4. Operating temperature and range

Requirements:

1. Gain
2. Gain bandwidth
3. Settling time
4. Slew rate
5. Input common-mode range, ICMR
6. Common-mode rejection ratio, CMRR
7. Power-supply rejection ratio, PSRR
8. Output-voltage swing
9. Output resistance
10. Offset
11. Noise
12. Layout area

The typical specifications for an unbuffered CMOS op amp are listed in Table 6.1-2.

The block diagram of Fig. 6.1-1 is useful for guiding the CMOS op amp design process. The compensation method has a large influence on the design of each block. Two basic methods of compensation are suggested by the opposite parallel paths into the compensation block

Table 6.1-2 Specifications for a Typical Unbuffered CMOS Op Amp

Boundary Conditions	Requirement
Process specification	See Tables 3.1-1, 3.1-2, and 3.2-1
Supply voltage	± 2.5 V $\pm 10\%$
Supply current	100 μA
Temperature range	0–70 °C
Specifications	
Gain	$\geq$ 70 dB
Gain bandwidth	$\geq$ 5 MHz
Settling time	$\leq$ 1 μs
Slew rate	$\geq$ 5 V/μs
ICMR	$\geq \pm 1.5$ V
CMRR	$\geq$ 60 dB
PSRR	$\geq$ 60 dB
Output swing	$\geq \pm 1.5$ V
Output resistance	N/A, capacitive load only
Offset	$\leq \pm 10$ mV
Noise	$\leq 100\ \text{nV}/\sqrt{\text{Hz}}$ at 1 kHz
Layout area	$\leq 5000 \times$ (minimum channel length)^2

of Fig. 6.1-1. These two methods, feedback and feedforward, are developed in the following section. The method of compensation is greatly dependent on the number of stages present (differential, second, or buffer stages).

In designing an op amp, one can begin at many points. The design procedure must be iterative, since it is almost impossible to relate all specifications simultaneously. For a typical CMOS op amp design, the following steps may be appropriate.

1. Decide on a Suitable Configuration

After examining the specifications in detail, determine the type of configuration required. For example, if extremely low noise and offset are a must, then a configuration that affords high gain in the input stage is required. If there are low-power requirements, then a Class AB-type output stage may be necessary. This in turn will govern the type of input stage that must be used. Often, one must create a configuration that meets a specific application.

2. Determine the Type of Compensation Needed to Meet the Specifications

There are many ways to compensate amplifiers. Some have unique aspects that make them suitable for particular configurations or specifications. For example, an op amp that must drive very large load capacitances might be compensated at the output. If this is the case, then this requirement also dictates the types of input and output stages needed. As this example shows, iteration might be necessary between steps 1 and 2 of the design process.

3. Design Device Sizes for Proper dc, ac, and Transient Performance

This begins with hand calculations based on approximate design equations. Compensation components are also sized in this step of the procedure. After each device is sized by hand, a circuit simulator is used to fine-tune the design.

One may find during the design process that some specification may be difficult or impossible to meet with a given configuration. At this point the designer has to modify the configuration or search the literature for ideas particularly suited to the requirement. This literature search takes the place of creating a new configuration from scratch. For very critical designs, the hand calculations can achieve about 80% of the complete job in roughly 20% of the total job time. The remaining 20% of the job requires 80% of the time for completion. Sometimes hand calculations can be misleading due to their approximate nature. Nonetheless, they are necessary to give the designer a feel for the sensitivity of the design to parameter variation. There is no other way for the designer to understand how the various design parameters influence performance. Iteration by computer simulation gives the designer very little feeling for the design and is generally not a wise use of computer resources.*

In summary, the design process consists of two major steps. The first is the conception of the design and the second is the optimization of the design. The conception of the design is accomplished by proposing an architecture to meet the given specifications. This step is normally accomplished using hand calculations in order to maintain the intuitive viewpoint necessary for choices that must be made. The second step is to take the "first-cut" design and verify and optimize it. This is normally done by using computer simulation and can include such influences as environmental or process variations.

6.2 Compensation of Op Amps

Operational amplifiers are generally used in a negative-feedback configuration. In this way, the relatively high, inaccurate forward gain can be used with feedback to achieve a very accurate transfer function that is a function of the feedback elements only. Figure 6.2-1 illustrates a general negative-feedback configuration. $A(s)$ is the amplifier gain and will normally be the open-loop, differential-voltage gain of the op amp, and $F(s)$ is the transfer function for external feedback from the output of the op amp back to the input. The loop gain of this system will be defined as

$$\text{Loop gain} = L(s) = -A(s)F(s) \tag{6.2-1}$$

Consider a case where the forward gain from V_{in} to V_{out} is to be unity. It is easily shown that if the open-loop gain at dc $A(0)$ is between 1000 and 2000, and F is equal to 1, the forward gain varies from 0.999 to 0.9995. For very high loop gain (due primarily to a high amplifier gain), the forward transfer function V_{out}/V_{in} is accurately controlled by the feedback network. This is the principle applied in using operational amplifiers.

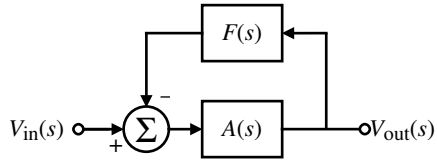

Figure 6.2-1 A single-loop, negative-feedback system.

*A useful relationship in analog design is: (use of a simulator) × (common sense) = (a constant).

Small-Signal Dynamics of a Two-Stage Op Amp

It is of primary importance that the signal fed back to the input of the op amp be of such amplitude and phase that it does not continue to regenerate itself around the loop. Should this occur, the result will be either clamping of the output of the amplifier at one of the supply potentials (regeneration at dc), or oscillation (regeneration at some frequency other than dc). The requirement for avoiding this situation can be succinctly stated by the following equation:

$$|A(j\omega_{0^\circ})F(j\omega_{0^\circ})| = |L(j\omega_{0^\circ})| < 1 \tag{6.2-2}$$

where ω_{0° is defined as

$$\text{Arg}[-A(j\omega_{0^\circ})F(j\omega_{0^\circ})] = \text{Arg}[L(j\omega_{0^\circ})] = 0^\circ \tag{6.2-3}$$

Another convenient way to express this requirement is

$$\text{Arg}[-A(j\omega_{0\,\text{dB}})F(j\omega_{0\,\text{dB}})] = \text{Arg}[L(j\omega_{0\,\text{dB}})] > 0^\circ \tag{6.2-4}$$

where $\omega_{0\,\text{dB}}$ is defined as

$$|A(j\omega_{0\,\text{dB}})F(j\omega_{0\,\text{dB}})| = |L(j\omega_{0\,\text{dB}})| = 1 \tag{6.2-5}$$

If these conditions are met, the feedback system is said to be stable (i.e., sustained oscillation cannot occur).

This second relationship given in Eq. (6.2-4) is best illustrated with the use of Bode diagrams. Figure 6.2-2 shows the response of $|A(j\omega)F(j\omega)|$ and $\text{Arg}[-A(j\omega)F(j\omega)]$ as a function of frequency. The requirement for stability is that the $|A(j\omega)F(j\omega)|$ curve cross the 0 dB point before the $\text{Arg}[-A(j\omega)F(j\omega)]$ reaches 0°. A measure of stability is given by the value of the phase when $|A(j\omega)F(j\omega)|$ is unity, 0 dB. This measure is called *phase margin* and is described by the following relationship:

$$\text{Phase margin} = \Phi_M = \text{Arg}[-A(j\omega_{0\,\text{dB}})F(j\omega_{0\,\text{dB}})] = \text{Arg}[L(j\omega_{0\,\text{dB}})] \tag{6.2-6}$$

The importance of "good stability" obtained with adequate phase margin is best understood by considering the response of the closed-loop system in the time domain. Figure 6.2-3 shows the time response of a second-order closed-loop system with various phase margins.

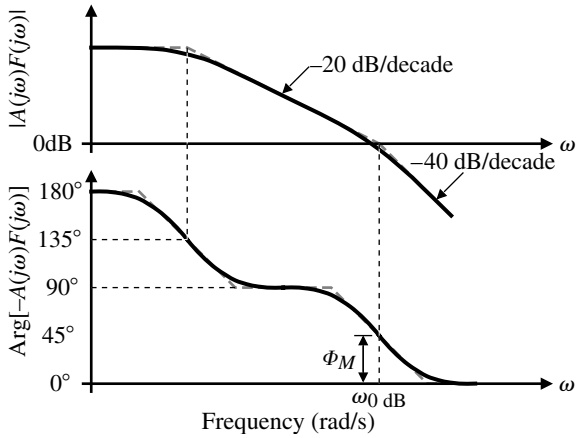

Figure 6.2-2 Frequency and phase response of a second-order system.

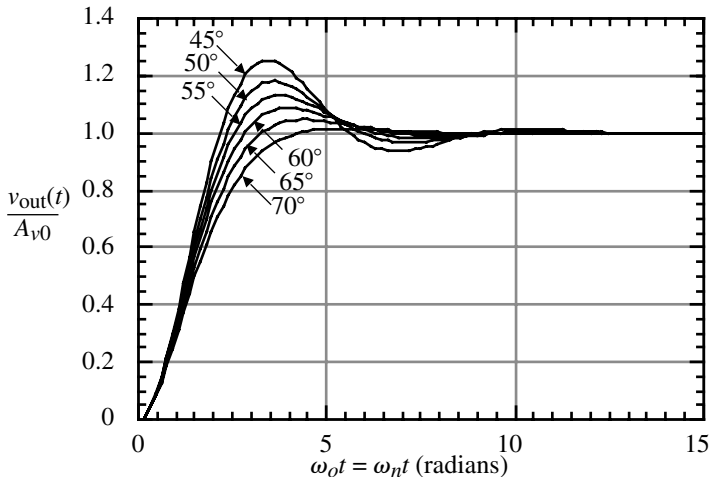

Figure 6.2-3 Response of a second-order system with various phase margins.

One can see that larger phase margins result in less "ringing" of the output signal. Too much ringing can be undesirable, so it is important to have adequate phase margin keeping the ringing to an acceptable level. It is desirable to have a phase margin of at least 45°, with 60° preferable in most situations. Appendix D develops the relationship between phase margin and time domain response for second-order systems.

Now consider the second-order, small-signal model for an uncompensated op amp shown in Fig. 6.2-4. In order to generalize the results, the components associated with the first stage have the subscript *I* and those associated with the second stage have the subscript *II*. The locations for the two poles are given by the following equations:

$$p_1' = \frac{-1}{R_I C_I} \tag{6.2-7}$$

and

$$p_2' = \frac{-1}{R_{II} C_{II}} \tag{6.2-8}$$

where R_I (R_{II}) is the resistance to ground seen from the output of the first (second) stage and C_I (C_{II}) is the capacitance to ground seen from the output of the first (second) stage. In a typical case, these poles are far away from the origin of the complex frequency plane and are relatively close together. Figure 6.2-5 illustrates the open-loop frequency response of a negative-feedback loop using the op amp modeled by Fig. 6.2-4 and a feedback factor of $F(s) = 1$.

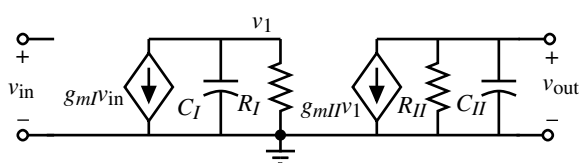

Figure 6.2-4 Second-order, small-signal equivalent circuit for a two-stage op amp.

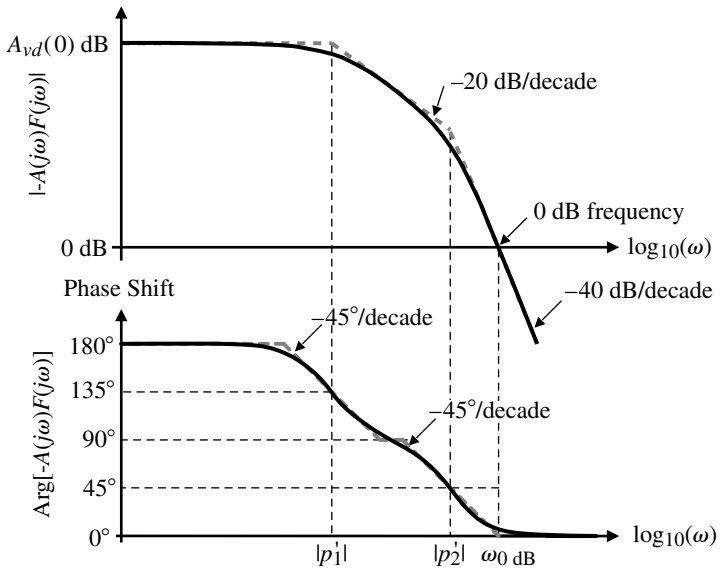

Figure 6.2-5 The open-loop frequency response of a negative-feedback loop using an uncompensated op amp and a feedback factor of $F(s) = 1$.

Note that $F(s) = 1$ is the worst case for stability considerations. In Fig. 6.2-5, the phase margin is significantly less than 45°, which means that the op amp should be compensated before using it in a closed-loop configuration.

Miller Compensation of the Two-Stage Op Amp

The first compensation method discussed here will be the "Miller" compensation technique [2]. This technique is applied by connecting a capacitor from the output to the input of the second transconductance stage g_{mII}. The resulting small-signal model is illustrated in Fig. 6.2-6. Two results come from adding the compensation capacitor C_c. First, the effective capacitance shunting R_I is increased by the additive amount of approximately $g_{mII}(R_{II})(C_c)$. This moves p_1 (the new location of p_1') closer to the origin of complex frequency plane by a significant amount (assuming that the second-stage gain is large). Second, p_2 (the new location of p_2') is moved away from the origin of the complex frequency plane, resulting from the negative feedback reducing the output resistance of the second stage.

The following derivation illustrates this in a rigorous way. The overall transfer function that results from the addition of C_c is

$$\frac{V_O(s)}{V_{\text{in}}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})(1 - sC_c/g_{mII})}{1 + s[R_I(C_I + C_c) + R_{II}(C_{II} + C_c) + g_{mII}R_IR_{II}C_c] + s^2R_IR_{II}[C_IC_{II} + C_cC_I + C_cC_{II}]} \tag{6.2-9}$$

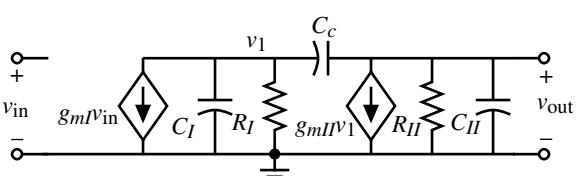

Figure 6.2-6 Miller capacitance applied to the two-stage op amp.

Using the approach developed in Section 5.3 for two widely spaced poles gives the following compensated poles:

$$p_1 \cong \frac{-1}{g_{mII}R_IR_{II}C_c} \tag{6.2-10}$$

and

$$p_2 \cong \frac{-g_{mII}C_c}{C_IC_{II} + C_{II}C_c + C_IC_c} \tag{6.2-11}$$

If C_{II} is much greater than C_I and C_c is greater than C_I, then Eq. (6.2-11) can be approximated by

$$p_2 \cong \frac{-g_{mII}}{C_{II}} \tag{6.2-12}$$

It is of interest to note that a zero occurs on the positive-real axis of the complex frequency plane and is due to the feedforward path through C_c. The right half-plane zero is located at

$$z_1 = \frac{g_{mII}}{C_c} \tag{6.2-13}$$

Figure 6.2-7(a) illustrates the movement of the poles from their uncompensated to their compensated positions on the complex frequency plane. Figure 6.2-7(b) shows results of compensation illustrated by an asymptotic magnitude and phase plot. Note that the second pole does not begin to affect the magnitude until after $|A(j\omega)F(j\omega)|$ is less than unity. The right half-plane (RHP) zero increases the phase shift [acts like a left half-plane (LHP) pole] but increases the magnitude (acts like an LHP zero). Consequently, the RHP zero causes the two worst things possible with regard to stability considerations. If either the zero (z_1) or the pole (p_2) moves toward the origin of the complex frequency plane, the phase margin will be degraded. The task in compensating an amplifier for closed-loop applications is to move all poles and zeros, except for the dominant pole (p_1), sufficiently away from the origin of the complex frequency plane (beyond the unity-gain bandwidth frequency) to result in a phase shift similar to Fig. 6.2-7(b).

Only a second-order (two-pole) system has been considered thus far. In practice, there are more than two poles in the transfer function of a CMOS op amp. The rest of this treatment will concentrate on the two most dominant (smaller) poles and the RHP zero. Figure 6.2-8 illustrates a typical CMOS op amp with various parasitic and circuit capacitances shown. The approximate pole and zero locations resulting from these capacitances are given below:

$$p_1 \cong \frac{-G_IG_{II}}{g_{mII}C_c} = \frac{-(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}C_c} \tag{6.2-14}$$

$$p_2 \cong \frac{-g_{mII}}{C_{II}} = \frac{-g_{m6}}{C_2} \tag{6.2-15}$$

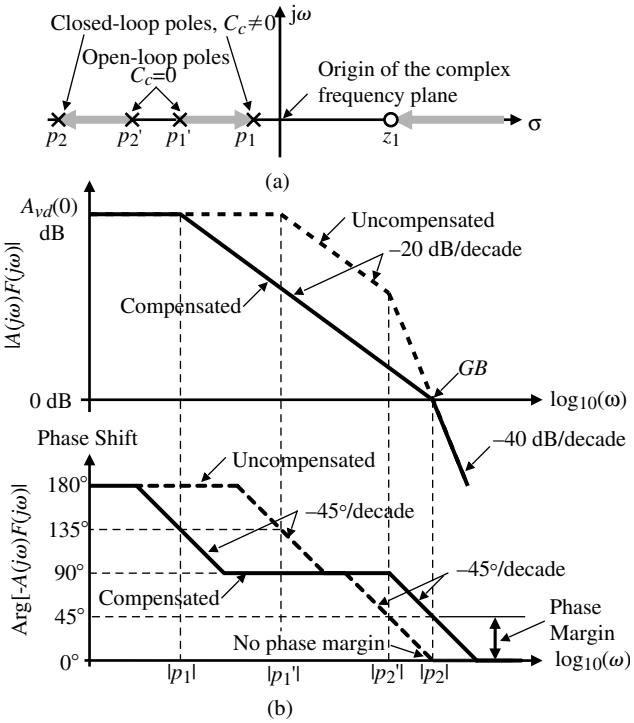

Figure 6.2-7 (a) Root locus plot of the loop gain $[F(s) = 1]$ resulting from the Miller compensation as C_C is varied from 0 to the value used to achieve the unprimed roots. (b) The asymptotic magnitude and phase plots of the loop gain $[F(s) = 1]$ before and after compensation.

and

$$z_1 \cong \frac{g_{mII}}{C_c} = \frac{g_{m6}}{C_c} \tag{6.2-16}$$

The unity-gain bandwidth as defined in Section 6.1 is easily derived (see Problem 6.2-3) and is shown to be approximately

$$GB \cong \frac{g_{mI}}{C_c} = \frac{g_{m2}}{C_c} \tag{6.2-17}$$

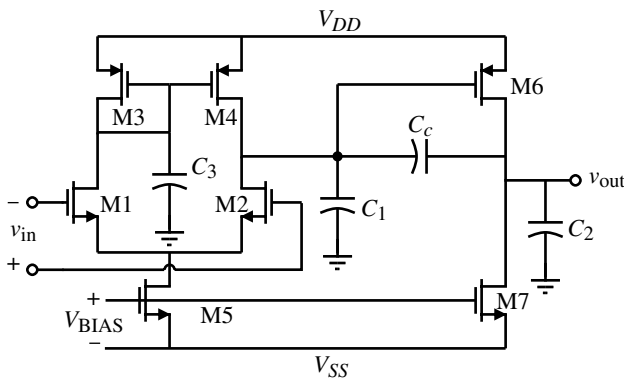

Figure 6.2-8 A two-stage op amp with various parasitic and circuit capacitances shown.

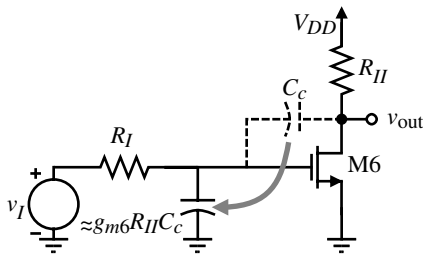

Figure 6.2-9 Illustration of the implementation of the dominant pole through the Miller effect on C_C. M6 is treated as an NMOS for this illustration.

The above three roots are very important to the dynamic performance of the two-stage op amp. The dominant left-half plane pole, p_1, is called the *Miller pole* and accomplishes the desired compensation. Intuitively, it is created by the Miller effect on the capacitance, C_c, as illustrated in Fig. 6.2-9, where M6 is assumed to be an NMOS transistor. The capacitor C_c is multiplied by approximately the gain of the second stage, $g_{II}R_{II}$, to give a capacitor in parallel with R_I of $g_{II}R_{II}C_c$. Multiplying this capacitance times R_I and inverting gives Eq. (6.2-14).

The second root of importance is p_2. The magnitude of this root must be at least equal to GB and is due to the capacitance at the output of the op amp. It is often called the *output pole.* Generally, C_{II} is equal to the load capacitance, C_L, which makes the output pole strongly dependent on the load capacitance. Figure 6.2-10 shows intuitively how this root develops. Since $|p_2|$ is near or greater than GB, the reactance of C_c is approximately $1/(GB \cdot C_c)$ and is very small. For all practical purposes the drain of M6 is connected to the gate of M6, forming an MOS diode. We know that the small-signal resistance of an MOS diode is $1/g_m$. Multiplying $1/g_{mII}$ by C_{II} (or C_L) and inverting gives Eq. (6.2-15).

The third root is the RHP zero. This is a very undesirable root because it boosts the loop gain magnitude while causing the loop phase shift to become more negative. Both of these results worsen the stability of the op amp. In BJT op amps, the RHP zero was not serious because of the large values of transconductance. However, in CMOS op amps, the RHP zero cannot be ignored. This zero comes from the fact that there are two signal paths from the input to the output as illustrated in Fig. 6.2-11. One path is from the gate of M6 through the compensation capacitor, C_c, to the output (V'' to V_{out}). The other path is through the transistor, M6, to the output (V' to V_{out}). At some complex frequency, the signals through these two paths will be equal and opposite and cancel, creating the zero. The RHP zero is developed by using superposition on these two paths as shown below:

$$V_{out}(s) = \left(\frac{-g_{m6}R_{II}(1/sC_c)}{R_{II} + 1/sC_c}\right)V' + \left(\frac{R_{II}}{R_{II} + 1/sC_c}\right)V'' = \frac{-R_{II}(g_{m6}/sC_c - 1)}{R_{II} + 1/sC_c}V \quad (6.2\text{-}18)$$

where $V = V' = V''$.

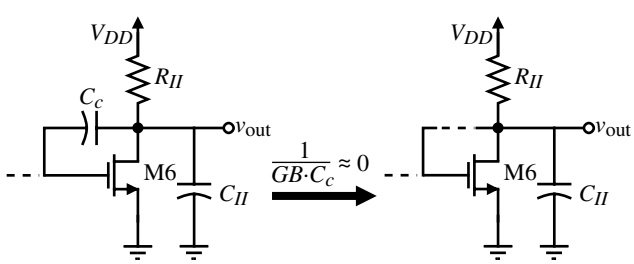

Figure 6.2-10 Illustration of how the output pole in a two-stage op amp is created. M6 is treated as an NMOS for this illustration.

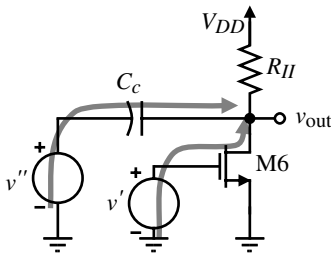

Figure 6.2-11 Illustration of how the RHP zero is developed. M6 is treated as an NMOS for this illustration.

As stated before, the goal of the compensation task is to achieve a phase margin greater than 45°. It can be shown (see Problem 6.2-4) that if the zero is placed at least ten times higher than the *GB,* then in order to achieve a 45° phase margin, the second pole (p_2) must be placed at least 1.22 times higher than *GB.* In order to obtain 60° of phase margin, p_2 must be placed about 2.2 times higher than *GB* as shown in the following example.

Example 6.2-1

Location of the Output Pole for a Phase Margin of 60°

For an op amp model with two poles and one RHP zero, prove that if the zero is ten times higher than *GB,* then in order to achieve a 60° phase margin, the second pole must be placed at least 2.2 times higher than *GB.*

SOLUTION

The requirement for a 60° phase margin is given as

$$\Phi_M = \pm 180° - \text{Arg}[A(j\omega)F(j\omega)] = \pm 180° - \tan^{-1}\left(\frac{\omega}{|p_1|}\right) - \tan^{-1}\left(\frac{\omega}{|p_2|}\right) - \tan^{-1}\left(\frac{\omega}{z_1}\right) = 60°$$

Assuming that the unity-gain frequency is *GB,* we replace ω by *GB* to get

$$120° = \tan^{-1}\left(\frac{GB}{|p_1|}\right) + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}\left(\frac{GB}{z_1}\right) = \tan^{-1}[A_v(0)] + \tan^{-1}\left(\frac{GB}{|p_2|}\right) + \tan^{-1}(0.1)$$

Assuming that $A_v(0)$ is large, then the above equation can be reduced to

$$24.3° \approx \tan^{-1}\left(\frac{GB}{|p_2|}\right)$$

which gives $|p_2| \geq 2.2GB$.

Assuming that a 60° phase margin is required, the following relationships apply:

$$\frac{g_{m6}}{C_c} > 10\left(\frac{g_{m2}}{C_c}\right) \tag{6.2-19}$$

Therefore,

$$g_{m6} > 10g_{m2} \tag{6.2-20}$$

Furthermore,

$$\left(\frac{g_{m6}}{C_2}\right) > 2.2\left(\frac{g_{m2}}{C_c}\right) \tag{6.2-21}$$

Combining Eqs. (6.2-20) and (6.2-21) gives the following requirement:

$$C_c > \frac{2.2\ C_2}{10} = 0.22\ C_2 \tag{6.2-22}$$

Up to this point, we have neglected the influence of the capacitor, C_3, associated with the current-mirror load of the input stage in Fig. 6.2-8. A small-signal model for the input stage of Fig. 6.2-8 that includes C_3 is shown in Fig. 6.2-12(a). The transfer function from the input to the output voltage of the first stage, $V_{o1}(s)$, can be written as

$$\begin{aligned}\frac{V_{o1}(s)}{V_{in}(s)} &= \frac{-g_{m1}}{2(g_{ds2} + g_{ds4})}\left[\frac{g_{m3} + g_{ds1} + g_{ds3}}{g_{m3} + g_{ds1} + g_{ds3} + sC_3} + 1\right] \\ &\approx \frac{-g_{m1}}{2(g_{ds2} + g_{ds4})}\left[\frac{sC_3 + 2g_{m3}}{sC_3 + g_{m3}}\right]\end{aligned} \tag{6.2-23}$$

We see that there is a pole and a zero given as

$$p_3 = -\frac{g_{m3}}{C_3} \qquad \text{and} \qquad z_3 = -\frac{2g_{m3}}{C_3} \tag{6.2-24}$$

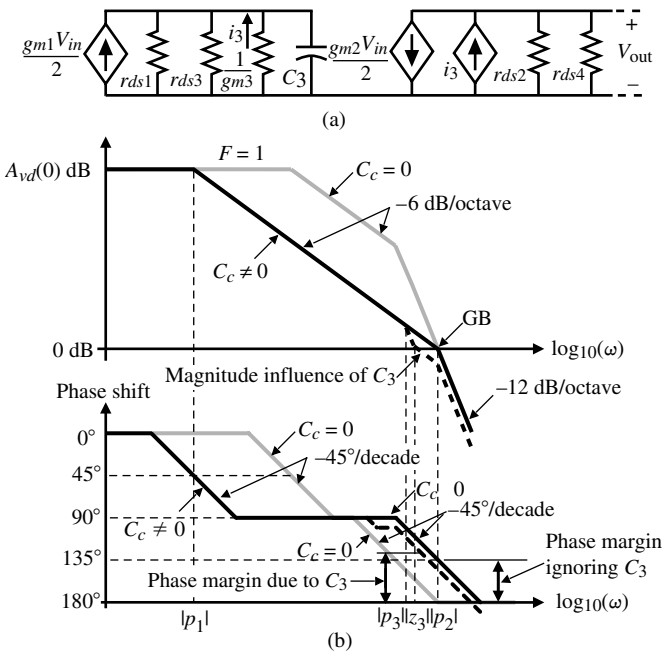

Figure 6.2-12 (a) Influence of the mirror pole, p_3, on the Miller compensation of a two-stage op amp. (b) The location of the open-loop and closed-loop roots.

Fortunately, the presence of the zero tends to negate the effect of the pole. Generally, the pole and zero due to C_3 is greater than *GB* and will have very little influence on the stability of the two-stage op amp. Figure 6.2-12(b) illustrates the case where these roots are less than *GB* and even then they have little effect on stability. In fact, they actually increase the phase margin slightly because *GB* is decreased.

Controlling the Right Half-Plane Zero

The RHP zero resulting from the feedforward path through the compensation capacitor tends to limit the *GB* that might otherwise be achievable if the zero were not present. There are several ways of eliminating the effect of this zero. One approach is to eliminate the feedforward path by placing a unity-gain buffer in the feedback path of the compensation capacitor [3]. This technique is shown in Fig. 6.2-13. Assuming that the output resistance of the unity-gain buffer is small ($R_o \rightarrow 0$), then the transfer function is given by the following equation:

$$\frac{V_o(s)}{V_{\text{in}}(s)} = \frac{(g_{mI})(g_{mII})(R_I)(R_{II})}{1 + s[R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c] + s^2[R_IR_{II}C_{II}(C_I + C_c)]} \tag{6.2-25}$$

Using the technique as before to approximate p_1 and p_2 results in the following:

$$p_1 \cong \frac{-1}{R_IC_I + R_{II}C_{II} + R_IC_c + g_{mII}R_IR_{II}C_c} \cong \frac{-1}{g_{mII}R_IR_{II}C_c} \tag{6.2-26}$$

and

$$p_2 \cong \frac{-g_{mII}C_c}{C_{II}(C_I + C_c)} \tag{6.2-27}$$

Note that the poles of the circuit in Fig. 6.2-13 are approximately the same as before, but the zero has been removed. With the zero removed, the pole p_2 can be placed higher than the *GB* in order to achieve a phase margin of 45°. For a 60° phase margin, p_2 must be placed 1.73 times greater than the *GB*. Using the type of compensation scheme shown in Fig. 6.2-13 results in greater bandwidth capabilities as a result of eliminating the zero.

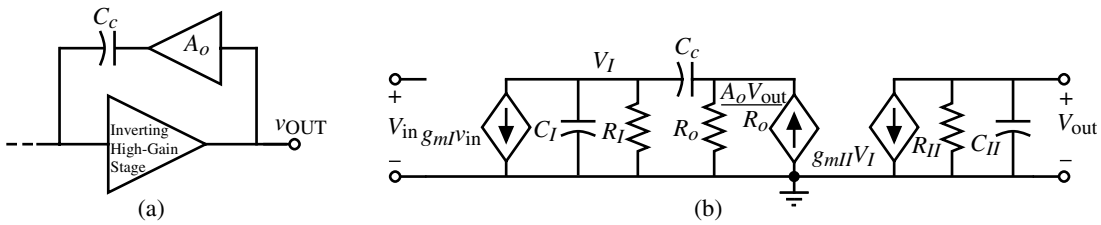

Figure 6.2-13 (a) Elimination of the feedforward path by a voltage amplifier. (b) Small-signal model for the two-stage op amp using the technique of (a).

The above analysis neglects the output resistance of the buffer amplifier R_o, which can be significant. Taking the output resistance into account, and assuming that it is less than R_I or R_{II}, results in an additional pole p_4 and an LHP zero z_2 given by

$$p_4 \cong \frac{-1}{R_o[C_I C_c/(C_I + C_c)]} \tag{6.2-28}$$

$$z_2 \cong \frac{-1}{R_o C_c} \tag{6.2-29}$$

Although the LHP zero can be used for compensation, the additional pole makes this method less desirable than the following method. The most important aspect of this result is that it leads naturally to the next scheme for controlling the RHP zero.

Another means of eliminating the effect of the RHP zero resulting from feedforward through the compensation capacitor C_c is to insert a nulling resistor in series with C_c [4]. Figure 6.2-14 shows the application of this technique. This circuit has the following node-voltage equations:

$$g_{mI}V_{\text{in}} + \frac{V_I}{R_I} + sC_I V_I + \left(\frac{sC_c}{1 + sC_c R_z}\right)(V_I - V_{\text{out}}) = 0 \tag{6.2-30}$$

$$g_{mII}V_I + \frac{V_o}{R_{II}} + sC_{II}V_{\text{out}} + \left(\frac{sC_c}{1 + sC_c R_z}\right)(V_{\text{out}} - V_I) = 0 \tag{6.2-31}$$

These equations can be solved to give

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = \frac{a\{1 - s[(C_c/g_{mII}) - R_z C_c]\}}{1 + bs + cs^2 + ds^3} \tag{6.2-32}$$

where

$$a = g_{mI}g_{mII}R_I R_{II} \tag{6.2-33}$$

$$b = (C_{II} + C_c)R_{II} + (C_I + C_c)R_I + g_{mII}R_I R_{II}C_c + R_z C_c \tag{6.2-34}$$

$$c = [R_I R_{II}(C_I C_{II} + C_c C_I + C_c C_{II}) + R_z C_c(R_I C_I + R_{II}C_{II})] \tag{6.2-35}$$

$$d = R_I R_{II} R_z C_I C_{II} C_c \tag{6.2-36}$$

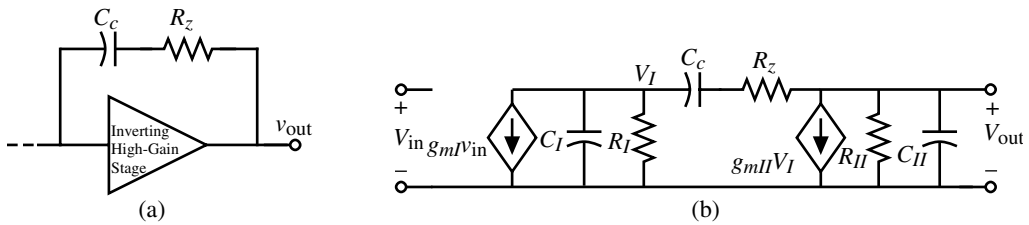

Figure 6.2-14 (a) Use of a nulling resistor, R_z, to control the RHP zero. (b) Small-signal model of the nulling resistor applied to a two-stage op amp.

If R_z is assumed to be less than R_I or R_{II} and the poles are widely spaced, then the roots of Eq. (6.2-32) can be approximated as

$$p_1 \cong \frac{-1}{(1 + g_{mII}R_{II})R_I C_c} \cong \frac{-1}{g_{mII}R_{II}R_I C_c} \tag{6.2-37}$$

$$p_2 \cong \frac{-g_{mII}C_c}{C_I C_{II} + C_c C_I + C_c C_{II}} \cong \frac{-g_{mII}}{C_{II}} \tag{6.2-38}$$

$$p_4 = \frac{-1}{R_z C_I} \tag{6.2-39}$$

and

$$z_1 = \frac{1}{C_c(1/g_{mII} - R_z)} \tag{6.2-40}$$

It is easy to see how the nulling resistor accomplishes the control over the RHP zero. Figure 6.2-15 shows the output stage broken into two parts, similar to what was done in Fig. 6.2-11. The output voltage, V_{out}, can be written as

$$V_{\text{out}} = \frac{-g_{m6}R_{II}\left(R_z + \dfrac{1}{sC_c}\right)}{R_{II} + R_z + \dfrac{1}{sC_c}} V' + \frac{R_{II}}{R_{II} + R_z + \dfrac{1}{sC_c}} V'' = \frac{-R_{II}\left(g_{m6}R_z + \dfrac{g_{m6}}{sC_c} - 1\right)}{R_{II} + R_z + \dfrac{1}{sC_c}} \tag{6.2-41}$$

Setting the numerator equal to zero gives Eq. (6.2-40), assuming $g_{m6} = g_{mII}$.

The resistor R_z allows independent control over the placement of the zero. In order to remove the RHP zero, R_z must be set equal to $1/g_{mII}$. Another option is to move the zero from the RHP to the LHP and place it on top of p_2. As a result, the pole associated with the output loading capacitance is canceled. To accomplish this, the following condition must be satisfied:

$$z_1 = p_2 \tag{6.2-42}$$

which results in

$$\frac{1}{C_c(1/g_{mII} - R_z)} = \frac{-g_{mII}}{C_{II}} \tag{6.2-43}$$

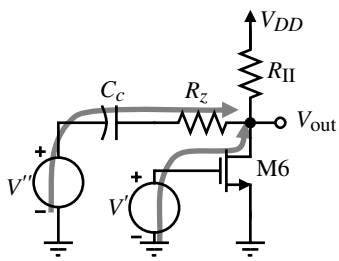

Figure 6.2-15 Illustration of how the nulling resistor accomplishes the control of the RHP zero.

The value of R_z can be found as

$$R_z = \left(\frac{C_c + C_{II}}{C_c}\right)\left(\frac{1}{g_{mII}}\right) \tag{6.2-44}$$

With p_2 canceled, the remaining roots are p_1 and p_3. For unity-gain stability, all that is required is that the magnitudes of p_3 and p_4 be sufficiently greater than GB. Therefore

$$|p_3| > A_v(0)|p_1| = \frac{A_v(0)}{g_{mII}R_{II}R_IC_c} = GB \tag{6.2-45}$$

$$|p_4| = (1/R_zC_I) > (g_{mI}/C_c) \tag{6.2-46}$$

Substituting Eq. (6.2-44) into Eq. (6.2-46) and assuming $C_{II} \gg C_c$ results in

$$C_c > \sqrt{\frac{g_{mI}}{g_{mII}}C_IC_{II}} \tag{6.2-47}$$

The nulling resistor approach has been used in the two-stage op amp with excellent results. The op amp can have good stability properties even with a large load capacitor. The only drawback is that the output pole, p_2, cannot change after the compensation has been designed (as it will if C_L changes).

The magnitude of the output pole, p_2, can be increased by introducing gain in the Miller capacitor feedback path as done by M8 in Fig. 6.2-16(a) [5]. The small-signal model of Fig. 6.2-16(a) is shown in Fig. 6.2-16(b). The resistors R_1 and R_2 are defined as

$$R_1 = \frac{1}{g_{ds2} + g_{ds4} + g_{ds9}} \tag{6.2-48}$$

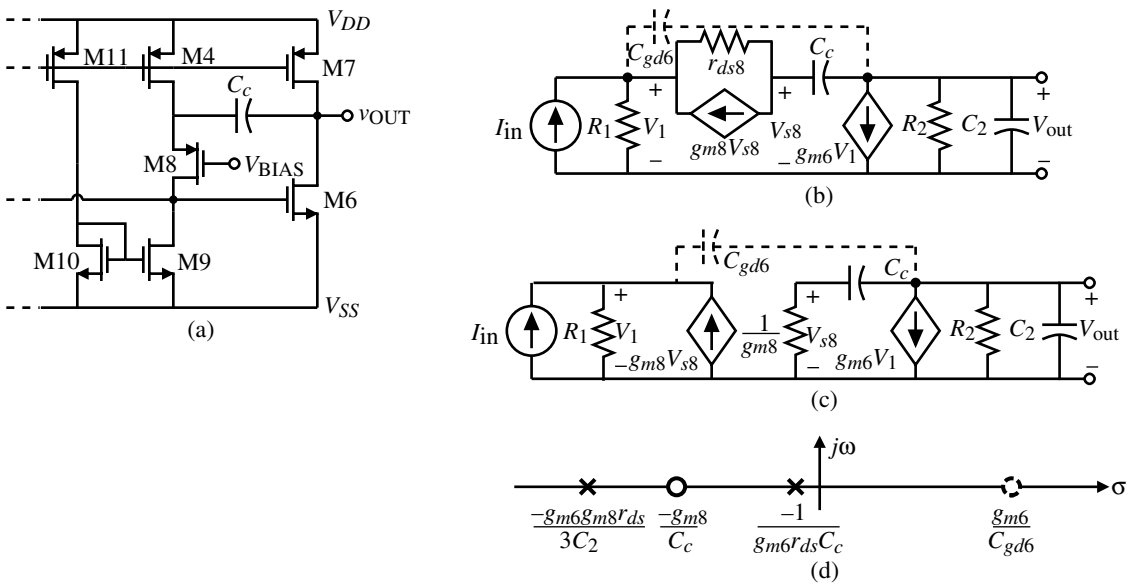

Figure 6.2-16 (a) Circuit to increase the magnitude of the output pole. (b) Small-signal model of (a). (c) Simplified version of (b). (d) Resulting poles and zeros of (a).

and

$$R_2 = \frac{1}{g_{ds6} + g_{ds7}} \tag{6.2-49}$$

where transistors M2 and M4 are the output transistors of the first stage. In order to simplify the analysis, we have rearranged the controlled source, $g_{m8}V_{s8}$, and have ignored r_{ds8}. The simplified small-signal model of Fig. 6.2-16(a) is given in Fig. 6.2-16(c). The nodal equations of this circuit are

$$I_{\text{in}} = G_1V_1 - g_{m8}V_{s8} = G_1V_1 - \left(\frac{g_{m8}sC_c}{g_{m8} + sC_c}\right)V_{\text{out}} \tag{6.2-50}$$

and

$$0 = g_{m6}V_1 + \left(G_2 + sC_2 + \frac{g_{m8}sC_c}{g_{m8} + sC_c}\right)V_{\text{out}} \tag{6.2-51}$$

Solving for the transfer function $V_{\text{out}}/I_{\text{in}}$ gives

$$\frac{V_{\text{out}}}{I_{\text{in}}} = \left(\frac{-g_{m6}}{G_1G_2}\right)\left[\frac{\left(1 + \dfrac{sC_c}{g_{m8}}\right)}{1 + s\left(\dfrac{C_c}{g_{m8}} + \dfrac{C_2}{G_2} + \dfrac{C_c}{G_2} + \dfrac{g_{m6}C_c}{G_1G_2}\right) + s^2\left(\dfrac{C_cC_2}{g_{m8}G_2}\right)}\right] \tag{6.2-52}$$

Using the approximate method of solving for the roots of the denominator illustrated earlier gives

$$p_1 = \frac{-1}{\dfrac{C_c}{g_{m8}} + \dfrac{C_c}{G_2} + \dfrac{C_2}{G_2} + \dfrac{g_{m6}C_c}{G_1G_2}} \approx \frac{-6}{g_{m6}r_{ds}^2C_c} \tag{6.2-53}$$

and

$$p_2 \approx \frac{\dfrac{g_{m6}r_{ds}^2C_c}{6}}{\dfrac{C_cC_2}{g_{m8}G_2}} = \frac{g_{m8}r_{ds}^2G_2}{6}\left(\frac{g_{m6}}{C_2}\right) = \left(\frac{g_{m8}r_{ds}}{3}\right)|p_2'| \tag{6.2-54}$$

where all the various channel resistances have been assumed to equal r_{ds} and p_2' is the output pole for normal Miller compensation. The result of Fig. 6.2-16(a) is to keep the dominant pole approximately the same and to multiply the output pole by roughly the gain of a single stage (g_mr_{ds}). In addition to the poles, there is an LHP zero at g_{m8}/sC_c, which can be used to enhance the compensation. Note in Fig. 6.2-16(d) that there is still an RHP zero in the compensation scheme of Fig. 6.2-16 because of the feedforward path through C_{gd6} shown as the dashed path on Figs. 6.2-16(b) and 6.2-16(c).

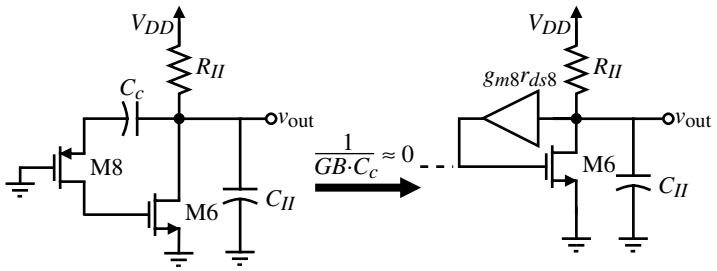

Figure 6.2-17 Illustration of how the output pole is increased by Fig. 6.2-16(a).

Figure 6.2-17 shows intuitively how the output pole is increased by the addition of M8 in the feedback path around M6. At frequencies near *GB,* the reactance of C_c can be considered small. Under these assumptions, M6 approximates an MOS diode with a gain of $g_{m8}r_{ds8}$ in the feedback path. This makes the output resistance seen by C_2 (C_{II}) to be approximately

$$R_{\text{out}} = R_{II} \| \left(\frac{1}{g_{m6}g_{m8}r_{ds8}} \right) \approx \frac{1}{g_{m6}g_{m8}r_{ds8}} \tag{6.2-55}$$

Multiplying this resistance by C_2 and inverting gives Eq. (6.2-54), ignoring the influence of the channel resistances of other transistors, which leads to the 3 in the denominator.

Feedforward Compensation

Another compensation technique used in CMOS op amps is the feedforward scheme shown in Fig. 6.2-18(a). In this circuit, the buffer is used to break the bidirectional path through the compensation capacitor. Unfortunately, this circuit will result in a zero that is in the right half-plane. If either the polarity of the buffer or the high-gain amplifier is reversed, the zero will be in the left half-plane. Figure 6.2-18(b) shows a feedforward compensation technique

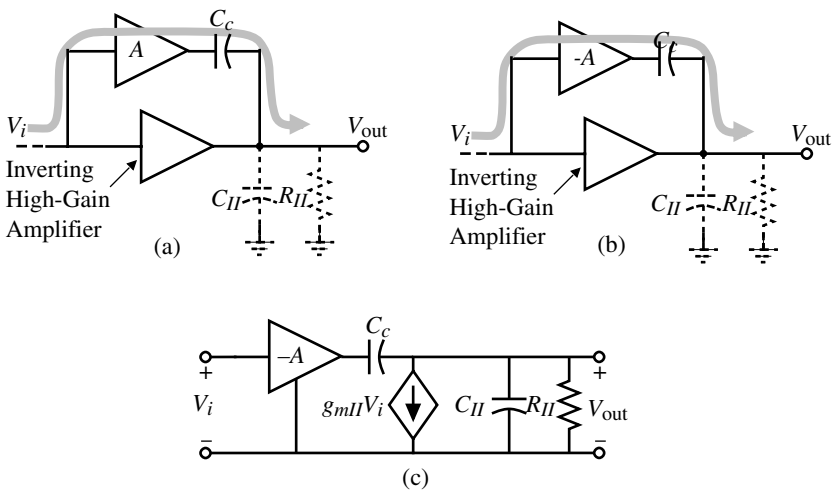

Figure 6.2-18 (a) Feedforward resulting in an RHP zero. (b) Feedforward resulting in an LHP zero. (c) Small-signal model for (b).

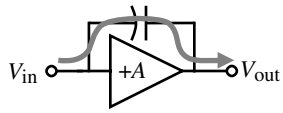

Figure 6.2-19 Feedforward compensation around a noninverting amplifier.

that has a zero in the left half-plane because the gain of the buffer is inverted. Figure 6.2-18(c) can be used as a model for this circuit. The voltage-transfer function $V_{out}(s)/V_{in}(s)$ can be found to be

$$\frac{V_{out}(s)}{V(s)} = \frac{-AC_c}{C_c + C_{II}}\left(\frac{s + g_{mII}/AC_c}{s + 1/[R_{II}(C_c + C_{II})]}\right) \tag{6.2-56}$$

In order to use the circuit in Fig. 6.2-18(b) to achieve compensation, it is necessary to place the zero located at g_{mII}/AC_c above the value of GB so that the boosting of the magnitude will not negate the desired effect of positive phase shift caused by the zero. Fortunately, the phase effects extend over a much broader frequency range than the magnitude effects so that this method will contribute additional phase margin to that provided by the feedback compensation technique. It is quite possible that several zeros can be generated in the transfer function of the op amp. These zeros should all be placed above GB and should be well controlled to avoid large settling times caused by poles and zeros that are close together in the transient response [6].

Another form of feedforward compensation is to provide a feedforward path around a noninverting amplifier. This is shown in Fig. 6.2-19. This type of compensation is often used in source followers, where a capacitor is connected from the gate to source of the source follower. The capacitor will provide a path that bypasses the transistor at high frequencies.

6.3 Design of the Two-Stage Op Amp

The previous two sections described the general approach to op amp design and compensation. In this section, a procedure will be developed that will enable a first-cut design of the two-stage op amp shown in Fig. 6.3-1. In order to simplify the notation, it is convenient to define the notation $S_i = W_i/L_i = (W/L)_i$, where S_i is the ratio of W and L of the ith transistor.

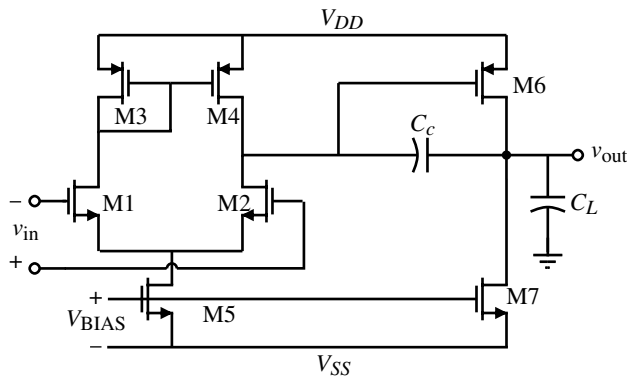

Figure 6.3-1 Schematic of an unbuffered, two-stage CMOS op amp with an n-channel input pair.

Design Procedure for the Two-Stage CMOS Op Amp

Before beginning this task, important relationships describing op amp performance will be summarized from Section 6.2, assuming that $g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$. These relationships are based on the circuit shown in Fig. 6.3-1.

$$\text{Slew rate } SR = \frac{I_5}{C_c} \tag{6.3-1}$$

$$\text{First-stage gain } A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5(\lambda_2 + \lambda_4)} \tag{6.3-2}$$

$$\text{Second-stage gain } A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6(\lambda_6 + \lambda_7)} \tag{6.3-3}$$

$$\text{Gain bandwidth } GB = \frac{g_{m1}}{C_c} \tag{6.3-4}$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L} \tag{6.3-5}$$

$$\text{RHP zero } z_1 = \frac{g_{m6}}{C_c} \tag{6.3-6}$$

$$\text{Positive CMR } V_{\text{in}}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{T03}|(\max) + V_{T1}(\min) \tag{6.3-7}$$

$$\text{Negative CMR } V_{\text{in}}(\min) = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max) + V_{DS5}(\text{sat}) \tag{6.3-8}$$

$$\text{Saturation voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \tag{6.3-9}$$

It is assumed that all transistors are in saturation for the above relationships.

The following design procedure assumes that specifications for the following parameters are given:

1. Gain at dc, $A_v(0)$
2. Gain bandwidth, GB
3. Input common-mode range, ICMR
4. Load capacitance, C_L
5. Slew rate, SR
6. Output voltage swing
7. Power dissipation, P_{diss}

The design procedure begins by choosing a device length to be used throughout the circuit. This value will determine the value of the channel length modulation parameter λ, which

will be a necessary parameter in the calculation of amplifier gain. Because transistor modeling varies strongly with channel length, the selection of a device length to be used in the design (where possible) allows for more accurate simulation models. Having chosen the nominal transistor device length, one next establishes the minimum value for the compensation capacitor C_c. It was shown in Section 6.2 that placing the output pole p_2 2.2 times higher than the *GB* permitted a 60° phase margin (assuming that the RHP zero z_1 is placed at or beyond ten times *GB*). It was shown in Eq. (6.2-22) that such pole and zero placements result in the following requirement for the minimum value for C_c:

$$C_c > (2.2/10)C_L \tag{6.3-10}$$

Next, determine the minimum value for the tail current I_5, based on slew-rate requirements. Using Eq. (6.3-1), the value for I_5 is determined to be

$$I_5 = SR\,(C_c) \tag{6.3-11}$$

If the slew-rate specification is not given, then one can choose a value based on settling-time requirements. Determine a value that is roughly ten times faster than the settling-time specification, assuming that the output slews approximately one-half of the supply rail. The value of I_5 resulting from this calculation can be changed later if need be. The aspect ratio of M3 can now be determined by using the requirement for positive input common-mode range. The following design equation for $(W/L)_3$ was derived from Eq. (6.3-7):

$$S_3 = (W/L)_3 = \frac{I_5}{(K_3')\,[V_{DD} - V_{\text{in}}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \tag{6.3-12}$$

If the value determined for $(W/L)_3$ is less than one, then it should be increased to a value that minimizes the product of *W* and *L*. This minimizes the area of the gate region, which in turn reduces the gate capacitance. This gate capacitance contributes to the mirror pole, which may cause a degradation in phase margin.

Requirements for the transconductance of the input transistors can be determined from knowledge of C_c and *GB*. The transconductance g_{m1} can be calculated using the following equation:

$$g_{m1} = GB(C_c) \tag{6.3-13}$$

The aspect ratio $(W/L)_1$ is directly obtainable from g_{m1} as shown below:

$$S_1 = (W/L)_1 = \frac{g_{m1}^2}{(K_1')(I_5)} \tag{6.3-14}$$

Enough information is now available to calculate the saturation voltage of transistor M5. Using the negative ICMR equation, calculate V_{DS5} using the following relationship derived from Eq. (6.3-8):

$$V_{DS5} = V_{\text{in}}(\min) - V_{SS} - \left(\frac{I_5}{\beta_1}\right)^{1/2} - V_{T1}(\max) \tag{6.3-15}$$

If the value for V_{DS5} is less than about 100 mV, then the possibility of a rather large $(W/L)_5$ may result. This may not be acceptable. If the value for V_{DS5} is less than zero, then the ICMR specification may be too stringent. To solve this problem, I_5 can be reduced or $(W/L)_1$ increased. The effects of these changes must be accounted for in previous design steps. One must iterate until the desired result is achieved. With V_{DS5} determined, $(W/L)_5$ can be extracted using Eq. (6.3-9) in the following way:

$$S_5 = (W/L)_5 = \frac{2(I_5)}{K_5'(V_{DS5})^2} \tag{6.3-16}$$

At this point, the design of the first stage of the op amp is complete. We next consider the output stage.

For a phase margin of 60°, the location of the output pole was assumed to be placed at 2.2 times *GB*. Based on this assumption and the relationship for $|p_2|$ in Eq. (6.3-5), the transconductance g_{m6} can be determined using the following relationship:

$$g_{m6} = 2.2(g_{m2})(C_L/C_c) \tag{6.3-17}$$

Generally, for reasonable phase margin, the value of g_{m6} is approximately ten times the input stage transconductance g_{m1}. At this point, there are two possible approaches to completing the design of M6 (i.e., W_6/L_6 and I_6). The first is to achieve proper mirroring of the first-stage current-mirror load of Fig. 6.3-1 (M3 and M4). This requires that $V_{SG4} = V_{SG6}$. Using the formula for g_m, which is $K'S(V_{GS} - V_T)$, we can write that if $V_{SG4} = V_{SG6}$, then

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} \tag{6.3-18}$$

Knowing g_{m6} and S_6 will define the dc current I_6 using the following equation:

$$I_6 = \frac{g_{m6}^2}{(2)(K_6')(W/L)_6} = \frac{g_{m6}^2}{2K_6'\,S_6} \tag{6.3-19}$$

One must now check to make sure that the maximum output voltage specification is satisfied. If this is not true, then the current or *W/L* ratio can be increased to achieve a smaller V_{DS}(sat). If these changes are made to satisfy the maximum output voltage specification, then the proper current mirroring of M3 and M4 is no longer guaranteed.

The second approach to designing the output stage is to use the value of g_{m6} and the required V_{DS}(sat) of M6 to find the current. Combining the defining equation for g_m and V_{DS}(sat) results in an equation relating (W/L), V_{DS}(sat), g_m, and process parameters. Using this relationship, given below, with the V_{DS}(sat) requirement taken from the output range specification one can determine $(W/L)_6$.

$$S_6 = (W/L)_6 = \frac{g_{m6}}{K_6'V_{DS6}(\text{sat})} \tag{6.3-20}$$

Equation (6.3-19) is used as before to determine a value for I_6. In either approach to finding I_6, one also should check the power dissipation requirements since I_6 will most likely determine the majority of the power dissipation.

The device size of M7 can be determined from the balance equation given below:

$$S_7 = (W/L)_7 = (W/L)_5\left(\frac{I_6}{I_5}\right) = S_5\left(\frac{I_6}{I_5}\right) \tag{6.3-21}$$

The first-cut design of all *W/L* ratios is now complete. Figure 6.3-2 illustrates the above design procedure showing the various design relationships and where they apply in the two-stage CMOS op amp.

At this point in the design procedure, the total amplifier gain must be checked against the specifications.

$$A_v = \frac{(2)(g_{m2})(g_{m6})}{I_5(\lambda_2 + \lambda_4)I_6(\lambda_6 + \lambda_7)} \tag{6.3-22}$$

If the gain is too low, a number of things can be adjusted. The best way to do this is to use Table 6.3-1, which shows the effects of various device sizes and currents on the different parameters generally specified. Each adjustment may require another pass through this design procedure in order to ensure that all specifications have been met. Table 6.3-2 summarizes the above design procedure.

No attempt has been made to account for noise or PSRR thus far in the design procedure. Now that the preliminary design is complete, these two specifications can be addressed. The input-referred noise voltage results primarily from the load and input transistors of the first stage. Each of these contributes both thermal and 1/*f* noise. The 1/*f* noise contributed by any transistor can be reduced by increasing device area (e.g., increase *WL*). Thermal noise contributed by any transistor can be reduced by increasing its g_m. This is accomplished by an increase in *W/L,* an increase in current, or both. Effective input-noise voltage attributed to the load transistors can be reduced by reducing the g_{m3}/g_{m1} (g_{m4}/g_{m2}) ratio. One must be careful that these adjustments to improve noise performance do not adversely affect some other important performance parameter of the op amp.

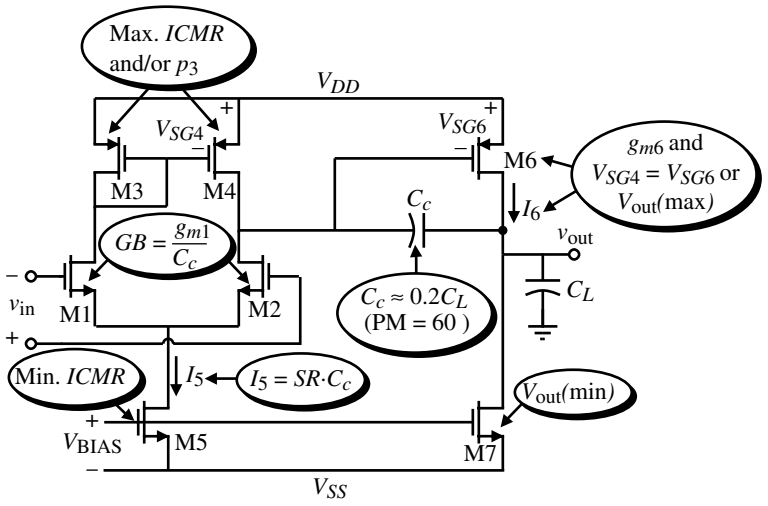

Figure 6.3-2 Illustration of the design relationship and the circuit for a two-stage CMOS op amp.

Table 6.3-1 Dependence of the Performance of Fig. 6.3-1 on dc Current, *W/L* Ratios, and the Compensating Capacitor

	Drain Current		M1 and M2		M3 and M4		Inverter	Inverter Load		Compensation Capacitor
	I_5	I_7	W/L	L	W	L	W_6/L_6	W_7	L_7	C_c
Increase dc Gain	$(\downarrow)^{1/2}$	$(\downarrow)^{1/2}$	$(\uparrow)^{1/2}$	$\uparrow$		$\uparrow$	$(\uparrow)^{1/2}$		$\uparrow$	
Increase *GB*	$(\uparrow)^{1/2}$		$(\uparrow)^{1/2}$							$\downarrow$
Increase RHP Zero		$(\uparrow)^{1/2}$					$(\uparrow)^{1/2}$			$\downarrow$
Increase Slew Rate	$\uparrow$									$\downarrow$
Increase C_L										$\uparrow$

Table 6.3-2 Unbuffered Op Amp Design Procedure

This design procedure assumes that the gain at dc (A_v), unity-gain bandwidth (*GB*), input common-mode range [V_{in}(min) and V_{in}(max)], load capacitance (C_L), slew rate (*SR*), settling time (T_s), output voltage swing [V_{out}(max) and V_{out}(min)], and power dissipation (P_{diss}) are given.

1. Choose the smallest device length that will keep the channel modulation parameter constant and give good matching for current mirrors.
2. From the desired phase margin, choose the minimum value for C_c; that is, for a 60° phase margin we use the following relationship. This assumes that $z \geq 10\ GB$.

$$C_c > 0.22C_L$$

3. Determine the minimum value for the "tail current" (I_5) from the largest of the two values.

$$I_5 = SR \cdot C_c$$

4. Design for S_3 from the maximum input voltage specification.

$$S_3 = \frac{2I_3}{K_3'[V_{DD} - V_{\text{in}}(\max) - |V_{T03}|(\max) + V_{T1}(\min)]^2} \geq 1$$

5. Verify that the pole and zero due to C_{gs3} and C_{gs4} ($= 0.67W_3L_3C_{\text{ox}}$) will not be dominant by assuming p_3 to be greater than $10GB$. Note that a zero exists at $2p_3$ and will diminish the influence of p_3 on the op amp.

$$\frac{g_{m3}}{2C_{gs3}} > 10\ GB$$

6. Design for S_1 (S_2) to achieve the desired *GB*.

$$g_{m1} = GB \cdot C_c \Rightarrow S_1 = S_2 = \frac{g_{m2}^2}{K_2' I_5}$$

Table 6.3-2 (continued)

7. Design for S_5 from the minimum input voltage. First calculate $V_{DS5}(\text{sat})$ and then find S_5.

$$V_{DS5}(\text{sat}) = V_{\text{in}}(\text{min}) - V_{SS} - \sqrt{\frac{I_5}{\beta_1}} - V_{T1}\,(\text{max}) \geq 100\ \text{mV}$$

$$S_5 = \frac{2I_5}{K_5'[V_{DS5}(\text{sat})]^2}$$

8. Find S_6 and I_6 by letting the second pole (p_2) be equal to 2.2 times *GB*.

$$g_{m6} = 2.2g_{m2}(C_L/C_c)$$

Let $V_{SG4} = V_{SG6}$, which gives

$$S_6 = S_4\frac{g_{m6}}{g_{m4}}$$

Knowing g_{m6} and S_6 allows us to solve for I_6 as

$$I_6 = \frac{g_{m6}^2}{2K_6'S_6}$$

9. Alternately, I_6 can be calculated by solving for S_6 using

$$S_6 = \frac{g_{m6}}{K_6'V_{DS6}(\text{sat})}$$

and then using the previous relationship to find I_6. Of course, the proper mirror between M3 and M4 is no longer guaranteed.

10. Design S_7 to achieve the desired current ratios between I_5 and I_6.

$$S_7 = (I_6/I_5)S_5$$

11. Check gain and power dissipation specifications.

$$A_v = \frac{2g_{m2}g_{m6}}{I_5(\lambda_2 + \lambda_3)(\lambda_6 + \lambda_7)}$$

$$P_{\text{diss}} = (I_5 + I_6)(V_{DD} + |V_{SS}|)$$

12. If the gain specification is not met, then the currents I_5 and I_6 can be decreased or the *W*/*L* ratios of M2 and/or M6 increased. The previous calculations must be rechecked to ensure that they have been satisfied. If the power dissipation is too high, then one can only reduce the currents I_5 and I_6. Reduction of currents will probably necessitate an increase of some of the *W*/*L* ratios to satisfy input and output swings.

13. Simulate the circuit to check to see that all specifications are met.

The power-supply rejection ratio is to a large degree determined by the configuration used. Some improvement in negative PSRR can be achieved by increasing the output resistance of M5. This is usually accomplished by increasing both W_5 and L_5 proportionately without seriously affecting any other performance. Transistor M7 should be adjusted accordingly for proper matching. A more detailed analysis of the PSRR of the two-stage op amp will be considered in the next section.

The following example illustrates the steps in designing the op amp described.

Example 6.3-1

Design of a Two-Stage Op Amp

Using the material and device parameters given in Tables 3.1-1 and 3.1-2, design an amplifier similar to that shown in Fig. 6.3-1 that meets the following specifications with a phase margin of 60°. Assume the channel length is to be 1 μm.

$A_v > 5000$ V/V	$V_{DD} = 2.5$ V	$V_{SS} = -2.5$ V
$GB = 5$ MHz	$C_L = 10$ pF	$SR > 10$ V/μs
V_{out} range $= \pm 2$ V	ICMR $= -1$ to 2 V	$P_{\text{diss}} \leq 2$ mW

SOLUTION

The first step is to calculate the minimum value of the compensation capacitor C_c, which is

$$C_c > (2.2/10)(10 \text{ pF}) = 2.2 \text{ pF}$$

Choose C_c as 3 pF. Using the slew-rate specification and C_c calculate I_5.

$$I_5 = (3 \times 10^{-12})(10 \times 10^6) = 30 \text{ μA}$$

Next calculate $(W/L)_3$ using ICMR requirements. Using Eq. (6.3-12) we have

$$(W/L)_3 = \frac{30 \times 10^{-6}}{(50 \times 10^{-6})[2.5 - 2 - 0.85 + 0.55]^2} = 15$$

Therefore,

$$(W/L)_3 = (W/L)_4 = 15$$

Now we can check the value of the mirror pole, p_3, to make sure that it is in fact greater than $10GB$. Assume the $C_{\text{ox}} = 2.47$ fF/μm^2. The mirror pole can be found as

$$p_3 \approx \frac{-g_{m3}}{2C_{gs3}} = \frac{-\sqrt{2K_p' S_3 I_3}}{2(0.667)\, W_3 L_3 C_{\text{ox}}} = 2.81 \times 10^9 \text{ rad/s}$$

or 448 MHz. Thus, p_3 and z_3 are not of concern in this design because $p_3 >> 10GB$.

The next step in the design is to calculate g_{m1} using Eq. (6.3-13).

$$g_{m1} = (5 \times 10^6)(2\pi)(3 \times 10^{-12}) = 94.25\ \mu\text{S}$$

Therefore, $(W/L)_1$ is

$$(W/L)_1 = (W/L)_2 = \frac{g_{m1}^2}{2K_N' I_1} = \frac{(94.25)^2}{2 \cdot 110 \cdot 15} = 2.79 \approx 3.0$$

Next, calculate V_{DS5} using Eq. (6.3-15).

$$V_{DS5} = (-1) - (-2.5) - \sqrt{\frac{30 \times 10^{-6}}{110 \times 10^{-6} \cdot 3}} - 0.85 = 0.35\ \text{V}$$

Using V_{DS5} calculate $(W/L)_5$ from Eq. (6.3-16).

$$(W/L)_5 = \frac{2(30 \times 10^{-6})}{(110 \times 10^{-6})(0.35)^2} = 4.49 \approx 4.5$$

From Eq. (6.2-20), we know that

$$g_{m6} \geq 10 g_{m1} \geq 942.5\ \mu\text{S}$$

Assuming that $g_{m6} = 942.5\ \mu\text{S}$ and calculating g_{m4} as 150 μS, we use Eq. (6.3-18) to get

$$S_6 = S_4 \frac{g_{m6}}{g_{m4}} = 15 \cdot \frac{942.5}{150} = 94.25 \approx 94$$

Calculate I_6 using Eq. (6.3-19).

$$I_6 = \frac{(942.5 \times 10^{-6})^2}{(2)(50 \times 10^{-6})(94)} = 94.5\ \mu\text{A} \approx 95\ \mu\text{A}$$

Designing S_6 by using Eq. (6.3-20) gives $S_6 \approx 15$. Since the W/L ratio of 94 from above is greater, the maximum output voltage specification will be met.

Finally, calculate $(W/L)_7$ using Eq. (6.3-21).

$$(W/L)_7 = 4.5 \left(\frac{95 \times 10^{-6}}{30 \times 10^{-6}} \right) = 14.25 \approx 14$$

Let us check the $V_{\text{out}}(\text{min})$ specification although the W/L of M7 is large enough that this is probably not necessary. The value of $V_{\text{out}}(\text{min})$ is

$$V_{\text{min}}(\text{out}) = V_{DS7}(\text{sat}) = \sqrt{\frac{2 \cdot 95}{110 \cdot 14}} = 0.351\ \text{V}$$

which is less than required. At this point, the first-cut design is complete.

The power dissipation can be calculated as

$$P_{\text{diss}} = 5\text{ V} \cdot (30\ \mu\text{A} + 95\ \mu\text{A}) = 0.625\text{ mW}$$

Now check to see that the gain specification has been met.

$$A_v = \frac{(2)(92.45 \times 10^{-6})(942.5 \times 10^{-6})}{30 \times 10^{-6}(0.04 + 0.05)95 \times 10^{-6}(0.04 + 0.05)} = 7696\text{ V/V}$$

which meets specifications. If more gain were desired, an easy way to achieve it would be to increase the W and L values by a factor of 2, which because of the decreased value of λ would increase the gain by a factor of 20. Figure 6.3-3 shows the results of the first-cut design. The next phase requires simulation.

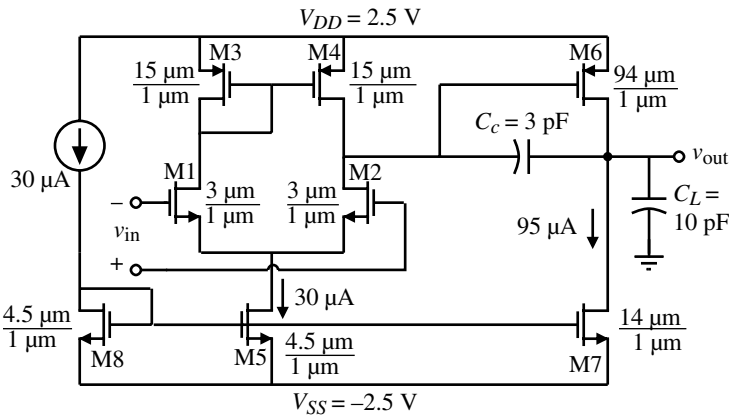

Figure 6.3-3 Result of Example 6.3-1.

Nulling Resistor, Miller Compensation

It may likely occur that the undesired RHP zero may not be negligible in the above design procedure. This would occur if the *GB* specification was large or if the output stage transconductance (g_{m6}) was not large. In this case, it becomes necessary to employ the nulling resistor compensation method. We shall use the results of Section 6.2 to illustrate how to apply this solution.

Section 6.2 described a technique whereby the RHP zero can be moved to the left half-plane and placed on the highest nondominant pole. To accomplish this, a resistor is placed in series with the compensation capacitor. Figure 6.3-4 shows a compensation scheme using transistor M8 as a resistor. This transistor is controlled by a control voltage V_c that adjusts the resistor so that it maintains the proper value over process variations [6].

With the addition of the resistor in the compensation scheme, the resulting poles and zeros are [see Eqs. (6.2-37) to (6.2-40)]

$$p_1 = -\frac{g_{m2}}{A_v C_c} = -\frac{g_{m1}}{A_v C_c} \tag{6.3-23}$$

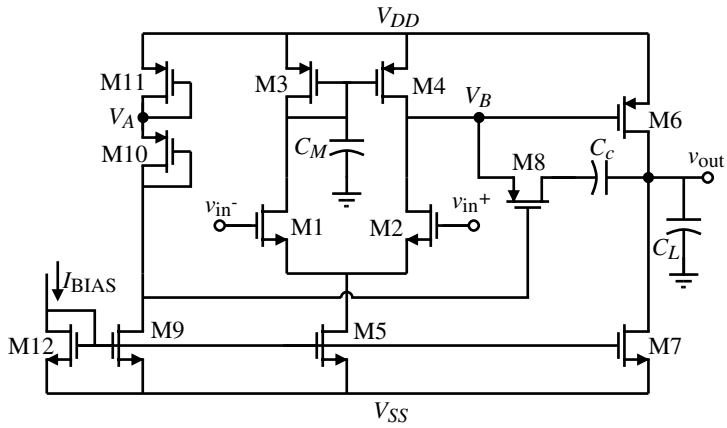

Figure 6.3-4 CMOS two-stage op amp using nulling resistor compensation.

$$p_2 = -\frac{g_{m6}}{C_L} \tag{6.3-24}$$

$$p_4 = -\frac{1}{R_z C_I} \tag{6.3-25}$$

$$z_1 = \frac{-1}{R_z C_c - C_c/g_{m6}} \tag{6.3-26}$$

where $A_v = g_{m1}g_{m6}R_I R_{II}$. In order to place the zero on top of the second pole (p_2), the following relationship must hold:

$$R_z = \frac{1}{g_{m6}}\left(\frac{C_L + C_c}{C_c}\right) = \left(\frac{C_c + C_L}{C_c}\right)\frac{1}{\sqrt{2K_P' S_6 I_6}} \tag{6.3-27}$$

The resistor R_z is realized by the transistor M8, which is operating in the active region because the dc current through it is zero. Therefore, R_z can be written as

$$R_z = \left.\frac{\partial v_{DS8}}{\partial i_{D8}}\right|_{V_{DS8}=0} = \frac{1}{K_P' S_8 (V_{SG8} - |V_{TP}|)} \tag{6.3-28}$$

The bias circuit is designed so that voltage V_A is equal to V_B. As a result,

$$|V_{GS10}| - |V_T| = |V_{GS8}| - |V_T| \tag{6.3-29}$$

In the saturation region

$$|V_{GS10}| - |V_T| = \sqrt{\frac{2(I_{10})}{K_P'(W_{10}/L_{10})}} = |V_{GS8}| - |V_T| \tag{6.3-30}$$

Substituting into Eq. (6.3-28) yields

$$R_z = \frac{1}{K_P' S_8}\sqrt{\frac{K_P' S_{10}}{2I_{10}}} = \frac{1}{S_8}\sqrt{\frac{S_{10}}{2K_P' I_{10}}} \tag{6.3-31}$$

Equating Eq. (6.3-27) to Eq. (6.3-31) gives

$$\left(\frac{W_8}{L_8}\right) = \left(\frac{C_c}{C_L + C_c}\right)\sqrt{\frac{S_{10}S_6 I_6}{I_{10}}} \tag{6.3-32}$$

This relationship must be met in order for Eq. (6.3-27) to hold. To complete the design of this compensation circuit, M11 must be designed to meet the criteria set forth in Eq. (6.3-29). To accomplish this V_{SG11} must be equal to V_{SG6}. Therefore,

$$\left(\frac{W_{11}}{L_{11}}\right) = \left(\frac{I_{10}}{I_6}\right)\left(\frac{W_6}{L_6}\right) \tag{6.3-33}$$

The example that follows illustrates the design of this compensation scheme.

Example 6.3-2

RHP Zero Compensation

Use results of Example 6.3-1 and design compensation circuitry so that the RHP zero is moved from the RHP to the LHP and placed on top of the output pole p_2. Use device data given in Example 6.3-1.

SOLUTION

The task at hand is the design of transistors M8, M9, M10, M11, and bias current I_{10}. The first step in this design is to establish the bias components. In order to set V_A equal to V_B, V_{SG10} must be equal to V_{SG6}. Therefore,

$$S_{11} = (I_{11}/I_6)S_6$$

Choose $I_{11} = I_{10} = I_9 = 15\ \mu\text{A}$, which gives $S_{11} = (15\ \mu\text{A}/95\ \mu\text{A}) \cdot 94 = 14.8 \approx 15$.

The aspect ratio of M10 is essentially a free parameter and will be set equal to 1. There must be sufficient supply voltage to support the sum of V_{SG11}, V_{SG10}, and V_{DS9}. The ratio of I_{10}/I_5 determines the (W/L) of M9. This ratio is

$$(W/L)_9 = (I_{10}/I_5)(W/L)_5 = (15/30)(4.5) = 2.25 \approx 2$$

Now using design Eq. (6.3-32), $(W/L)_8$ is determined to be

$$(W/L)_8 = \left(\frac{3\ \text{pF}}{3\ \text{pF} + 10\ \text{pF}}\right)\sqrt{\frac{1 \cdot 94 \cdot 95\ \mu\text{A}}{15\ \mu\text{A}}} = 5.63 \approx 6$$

It is worthwhile to check that the RHP zero has been moved on top of p_2. To do this, first calculate the value of R_z. V_{SG8} must first be determined. It is equal to V_{SG10}, which is

$$V_{SG10} = \sqrt{\frac{2I_{10}}{K'_p S_{10}}} + |V_{TP}| = \sqrt{\frac{2 \cdot 15}{50 \cdot 1}} + 0.7 = 1.474 \text{ V}$$

Next, determine R_z.

$$R_z = \frac{1}{K'_P S_8 (V_{SG10} - |V_{TP}|)} = \frac{10^6}{50 \cdot 5.63(1.474 - 0.7)} = 4.590 \text{ k}\Omega$$

Using Eq. (6.3-26), the location of z_1 is calculated to be

$$z_1 = \frac{-1}{(4.590 \times 10^3)(3 \times 10^{-12}) - \dfrac{3 \times 10^{-12}}{942.5 \times 10^{-6}}} = -94.46 \times 10^6 \text{ rad/s}$$

The output pole, p_2, is found from Eq. (6.3-24) and is

$$p_2 = \frac{942.5 \times 10^{-6}}{10 \times 10^{-12}} = -94.25 \times 10^6 \text{ rad/s}$$

Thus, we see that, for all practical purposes, the output pole is canceled by the zero that has been moved from the RHP to the LHP.

The results of this design are summarized below.

$$W_8 = 6 \text{ μm}$$
$$W_9 = 2 \text{ μm}$$
$$W_{10} = 1 \text{ μm}$$
$$W_{11} = 15 \text{ μm}$$

Because we are trying to cancel a pole with a zero, let us examine the dependence of the nulling resistor technique on temperature and the process variations. The key relationship is given in Eq. (6.3-26), where R_z is canceling $1/g_{m6}$. If we think of the technique as g_{m6} canceling $1/R_z$, the answer is clear. One of the forms for the small-signal transconductance is

$$g_{m6} = K'_P (W_6/L_6)(V_{SG6} - |V_{TP}|) \tag{6.3-34}$$

From Eq. (6.3-28), we see that $1/R_z$ has exactly the same form. As long as we keep M6, M8, and M10 the same type of transistor, the temperature and process tracking should be good. One could replace the resistor by an MOS diode and also achieve good temperature and process tracking (see Problem 6.3-13).

Simulation of the Electrical Design

After the design has been developed using the above procedures, the next step is to simulate the circuit using more accurate models of the transistor. In most cases, the BSIM2 [7] or BSIM3 [8] model is sufficient. The designer should be sure the computer simulation makes sense with the hand design. The computer simulation will take into account many of the details that have been neglected such as the bulk effect. While the designer can make minor modifications in the design, one should resist the temptation to use the computer to make major design changes, such as an architecture change. The function of simulation is to verify and to explore the influence of things like matching, process variations, temperature changes, and power-supply changes. If one does not have information on how the process parameters vary, a good substitute is to examine the circuit at high and low temperatures. These simulations will give some idea of the circuit's dependence on process parameter changes. Also, simulators can be used with Monte Carlo methods to investigate the influence of statistical variations in the values of components.

Although the circuit has not yet been designed physically, it is a good practice to include some of the parasitics that will be due to the physical layout. This will minimize the differences between the simulation performance before layout and after layout. At this point, the designer only knows the *W*/*L* values and the dc currents. The area and shape of the source and drain are not yet determined. Unfortunately, the parasitic capacitances due to the reverse-biased bulk–source and bulk–drain cannot be modeled until the area and periphery of the source and drain are known.

A technique that will allow the designer to include the bulk–source and drain–source capacitance parasitics is outlined below. In Fig. 6.3-5, a simple rectangular MOSFET layout is shown. The minimum possible source or drain area would be that indicated by the sum of the lengths L1, L2, and L3 times *W*. The lengths L1, L2, and L3 are related to the design rules for a given process and are as follows:

L1 = Minimum allowable distance between the contact in S/D and the poly

L2 = Width of a minimum size contact to diffusion

L3 = Minimum allowable distance from the contact in S/D to the edge of the S/D

These rules are easily found from the technology information. Thus, the minimum area of the drain and source is (L1 + L2 + L3) × *W* and the corresponding periphery is 2(L1 + L2 + L3) + 2*W*. A conservative approach might be to double this area to account for connection parasitics between the source (drain) and their respective destinations.

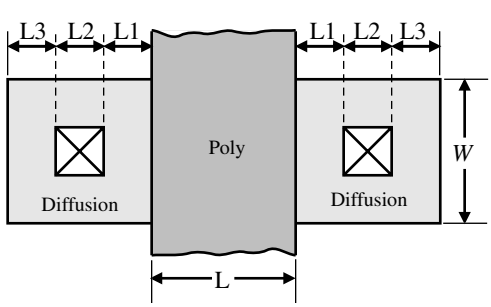

Figure 6.3-5 Method of estimating the source and drain areas and peripheries.

Example 6.3-3

Estimation of Bulk–Source and Bulk–Drain Capacitive Parasitics

Use the above method to estimate the area and periphery of a transistor that has a width of 10 μm and a length of 1 μm if L1 = L2 = L3 = 2 μm.

SOLUTION

The area of the source and drain is 6 μm times the width of 10 μm, resulting in an area of 60 μm^2. The periphery is 2 × 10 μm plus 2 × 6 μm or 32 μm. If this information is entered into the simulator (see Section 3.6), it will calculate the value of depletion capacitance corresponding to the value of reverse-bias voltage.

Physical Design of Analog Circuits

The next phase in the design process after satisfactory simulation results have been achieved is the physical design. One of the unmistakable trends in CMOS analog IC design is that the physical aspects of the design have a strong influence on the electrical performance. It is not possible to assume that the design is complete without carefully considering the physical implementation. A good electrical design can be ruined by a poor physical design or layout.

The goals of physical design go beyond simply minimizing the area required. The primary goal is to enhance the electrical performance. Because IC design depends on matching, physical design that enables better matching is extremely important. Good matching depends on how similar are the two items to be matched. The *unit-matching* principle is very useful in achieving good matching. The replication principle starts with a unit value of a device to be matched (transistor, resistor, capacitor, etc.). Next, the unit value is stepped-and-repeated using the same orientation. The unit value must be designed so that the influence of its connections is identical for both devices. Figure 6.3-6 shows two layouts for a 5-to-1 current mirror. In Fig. 6.3-6(a), a single transistor shown between the two vertical dashed lines has been repeated five times but the diffusion area has been combined to save area. In Fig. 6.3-6(b), the transistor on the left between the vertical dashed lines has been repeated five times to form the transistor on the right. While the layout in Fig. 6.3-6(a) is minimum area, the layout in Fig. 6.3-6(b) has better matching because the drain/source areas are identical. In Fig. 6.3-6(a), the drains and sources of the inner transistors are shared. This causes the depletion capacitance

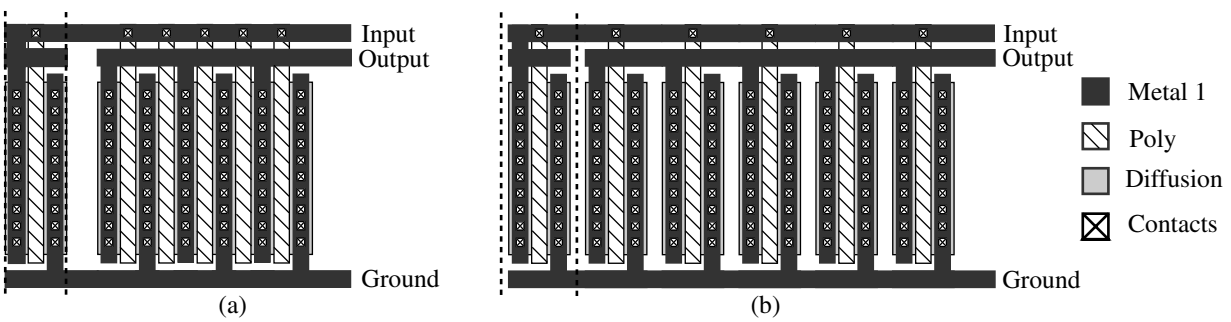

Figure 6.3-6 The layout of a 5-to-1 current mirror. (a) Layout that minimizes area at the sacrifice of matching. (b) Layout that optimizes matching.

of the bulk–drain and bulk–source junctions to be different from the unit transistor on the left. Not only are the capacitances different, but also the bulk resistances that account for the resistivity in the drains and sources are different.

If noninteger ratios are required, more than one unit can be used for the smaller. For example, 2 units compared with 3 give a 1.5 ratio. In this case, one can use a common-centroid geometry approach to get less dependence on the location at which the transistor is built. Figure 6.3-7 shows a good method of getting a 1.5 ratio using five individual transistors. The transistors labeled "2" and "1" are interleaved. If all three terminals of each transistor are to be available, then it is necessary to use a second layer of metal to provide external connections.

One can also use the geometry to improve the electrical performance of the circuit. A good example of this is shown in Fig. 6.3-8. In this figure, a transistor has been laid out as a square "donut." The objective is to reduce the value of C_{gd} at the sacrifice of the value of C_{gs}. Since the capacitor C_{gd} is often multiplied by the Miller effect, it is important to be able to keep it small. The donut transistor structure also has the advantage of being very area efficient. The approximate W is the length of the dotted centerline of the polysilicon modified by the influence of the corners.

In addition to matching between components, the designer must avoid unnecessary voltage drops. Unsilicided polysilicon should never be used for connections because of its high resistivity compared with metal. Even when the polysilicon is used to connect to gates and no dc current flows, one still needs to be careful of transient currents that must flow to charge and discharge parasitic capacitances. Even the low resistivity (50 mΩ/□) of metal can cause problems when the current flow is large. Consider an aluminum conductor 1000 μm long and 2 μm wide. This conductor has 500□ between ends and thus has a resistance of 500□ times 0.05 Ω/□ or 25 Ω. If 1 mA is flowing through this conductor, a voltage drop of 25 mV is experienced. A 25 mV drop between ends is sufficient to cause serious problems in a sensitive circuit. For example, suppose an analog signal is being converted to an 8 bit digital signal and the reference voltage is 1 V (see Chapter 9). This means the least-significant bit (LSB) has a value of 1 V/256 or 4 mV. Therefore, the 25 mV voltage drop on

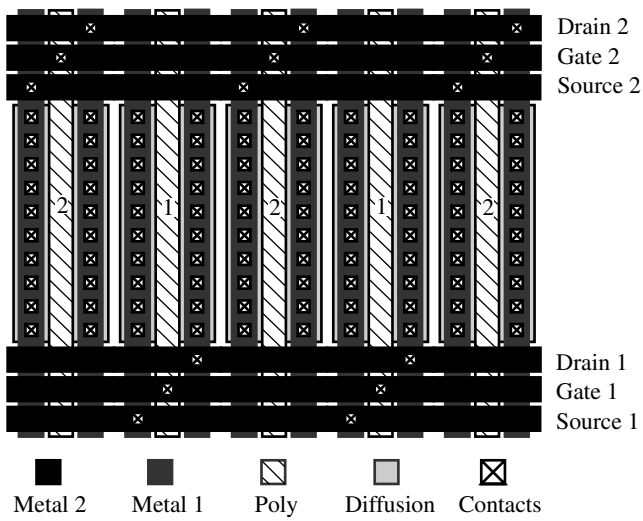

Figure 6.3-7 The layout of two transistors with a 1.5-to-1 matching using centroid geometry to improve matching.

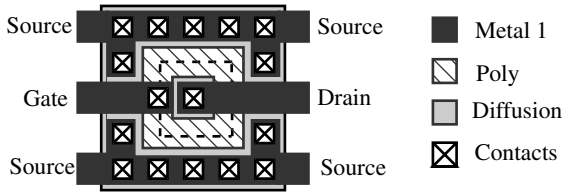

Figure 6.3-8 Reduction of C_{gs} by a donut-shaped transistor.

the conductor could have a deteriorating influence on the analog–digital converter. The ohmic drops in power-supply buses can be avoided by converting the bias voltage to current and routing the current across the chip. The bias voltage is recreated at the physical location where it is to be applied, avoiding the voltage drops in the buses. Figure 6.3-9 shows an implementation of this concept. The bandgap voltage, V_{BG}, is generated and distributed via M13–M14 to the slave bias circuits consisting of all transistors with an "A." The slave bias circuit generates the necessary bias voltages at a portion of the chip remote from the reference voltage.

In addition to the voltage drop caused by conductors, there is also a thermal noise generated by resistances. This is particularly important where polysilicon is used to connect the MOSFET gates to the signal source. Even though no dc current flows, a significant resistance results and will cause the noise to be increased. Most modern processes allow the siliciding of polysilicon to reduce its resistivity to much lower levels than normal polysilicon.

The influence of the physical layout on the electrical performance is becoming greater as more and more circuits are placed on a single integrated-circuit chip. The presence of noise in the substrate and on the connections at the surface can no longer be neglected [9,10]. This

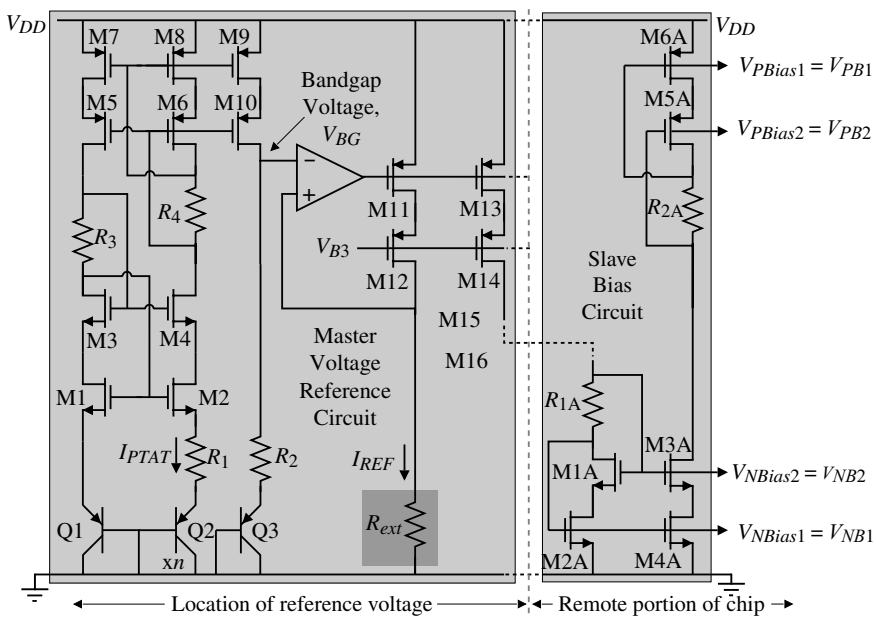

Figure 6.3-9 Generation of a reference voltage that is distributed on the chip as a current to slave bias circuits.

is a problem that must be approached from both the electrical and physical design viewpoints. Electrically, the designer can use differential circuits and design circuits with large values of power-supply rejection and common-mode rejection. From the physical viewpoint, the designer must try to keep the power supplies and grounds as free from noise as possible. This can be achieved by separating digital and analog power supplies and by routing all power supplies to a circuit back to a common point. One should never power digital and analog circuits from the same power-supply buses.

Physical separation of noisy circuits from sensitive circuits does not offer any significant improvement in processes that have a lightly doped epitaxial layer on top of a heavily doped substrate. What appears to be the best approach is to use multiple (parallel) bond wires off the chip to reduce the lead inductance from off-chip power supplies to on-chip grounds such as the substrate or well. When guard rings are used, they are most effective if they have their own off-chip bond wire and do not share the off-chip bond wires of another area with the same dc potential. As frequencies increase and more circuitry is put on a single chip, the interference problem will get worse. This factor certainly seems to be the biggest impediment to a single-chip solution of many mixed-signal applications.

Once the op amp (or other circuitry) is physically designed, it is then necessary to do two important steps. The first is to make sure that the physical design represents the electrical design. This is done by using a CAD tool called the *layout versus schematic* (LVS) checker. This tool checks to make sure the electrical schematic and the physical layout are in agreement. This step avoids making misconnections or leaving something out of the physical design. The second important step is to extract the parasitics of the circuit now that the physical implementation is known. Once the parasitics (typically capacitive and resistive) have been extracted, the simulation is performed again. If the simulation performance meets the specifications, then the circuit is ready for fabrication. This concludes the first two steps of an analog design, namely, the electrical and physical design. A third important step will be discussed later in this chapter and that is testing and debugging. A successful product must successfully pass all three steps.

Several aspects of the performance of the two-stage op amp will be considered in later sections. These performance considerations include PSRR (Section 6.4) and noise (Section 7.5). This section has introduced a procedure for the electrical design of a two-stage, unbuffered CMOS op amp. In addition, some important considerations of the physical design of analog integrated circuits have been presented. More information on the influence of the layout on analog design can be found in a book on the subject [11].

6.4 Power-Supply Rejection Ratio of Two-Stage Op Amps

The two-stage, unbuffered op amp of the last section has been used in many commercial products, particularly in the telecommunications area. After the initial successes, it was noted that this op amp suffers from a poor power-supply rejection ratio (PSRR). The ripple on the power supplies contributed too much noise at the output of the op amp. In order to illustrate this problem consider the op amp of Fig. 6.2-8. The definition of PSRR given in Eq. (6.1-8) is stated as the ratio of the differential gain A_v to the gain from the power-supply ripple to the output with the differential input set to zero (A_{dd}). Thus, PSRR can be written as

$$\text{PSRR} = \frac{A_v(V_{dd} = 0)}{A_{dd}(V_{\text{in}} = 0)} \tag{6.4-1}$$

While one can calculate A_v and A_{dd} and combine the results, it is easier to use the unity-gain configuration of Fig. 6.4-1(a). Using the model of the op amp shown in Fig. 6.4-1(b) to represent the two gains of Eq. (6.4-1), we can show that

$$V_{\text{out}} = \frac{A_{dd}}{1 + A_v} V_{dd} \cong \frac{A_{dd}}{A_v} V_{dd} = \frac{1}{\text{PSRR}^+} V_{dd} \tag{6.4-2}$$

where V_{dd} is the power-supply ripple of V_{DD} and PSRR^+ is the PSRR for V_{DD}. Therefore, if we connect the op amp in the unity-gain mode and input an ac signal of V_{dd} in series with the V_{DD} power supply, V_o/V_{dd} will be equal to the inverse of PSRR^+. This approach will be taken to calculate the PSRR of the two-stage op amp.

Positive PSRR

The two-stage op amp of Fig. 6.2-8 is shown in Fig. 6.4-2(a) connected in the unity-gain mode with an ac ripple of V_{dd} on the positive power supply. The two possible connections for the negative terminal of V_{BIAS} will become important later in the calculation for the negative power-supply rejection ratio. As before, C_I and C_{II} are the parasitic capacitances to ground at the output of the first and second stages, respectively. The unsimplified, small-signal model corresponding to the PSRR^+ calculation is shown in Fig. 6.4-2(b). This model has been simplified as shown in Fig. 6.4-2(c), where V_5 is assumed to be zero and the current I_3 flowing through $1/g_{m3}$ is replaced by

$$I_3 = g_{m1}V_{\text{out}} + g_{ds1}\left(V_{dd} - \frac{I_3}{g_{m3}}\right) \cong g_{m1}V_{\text{out}} + g_{ds1}V_{dd} \tag{6.4-3}$$

Equation (6.4-3) assumes that $g_{m3}r_{ds1} > 1$. The dotted line represents the portion of Fig. 6.4-2(b) in parallel with V_{dd} and thus is not important to the model.

The nodal equations for the voltages V_1 and V_{out} of Fig. 6.4-2(c) can be written as follows. For the node at V_1 we have

$$(g_{ds1} + g_{ds4})V_{dd} = (g_{ds2} + g_{ds4} + sC_c + sC_I)V_1 - (g_{m1} + sC_c)V_{\text{out}} \tag{6.4-4}$$

and for the output node we have

$$(g_{m6} + g_{ds6})V_{dd} = (g_{m6} - sC_c)V_1 + (g_{ds6} + g_{ds7} + sC_c + sC_{II})V_{\text{out}} \tag{6.4-5}$$

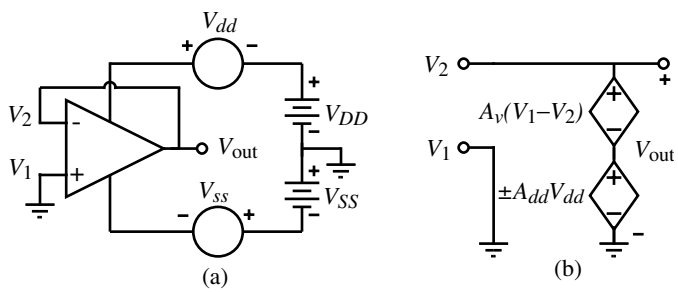

Figure 6.4-1 (a) Method for calculating PSRR. (b) Model (a).

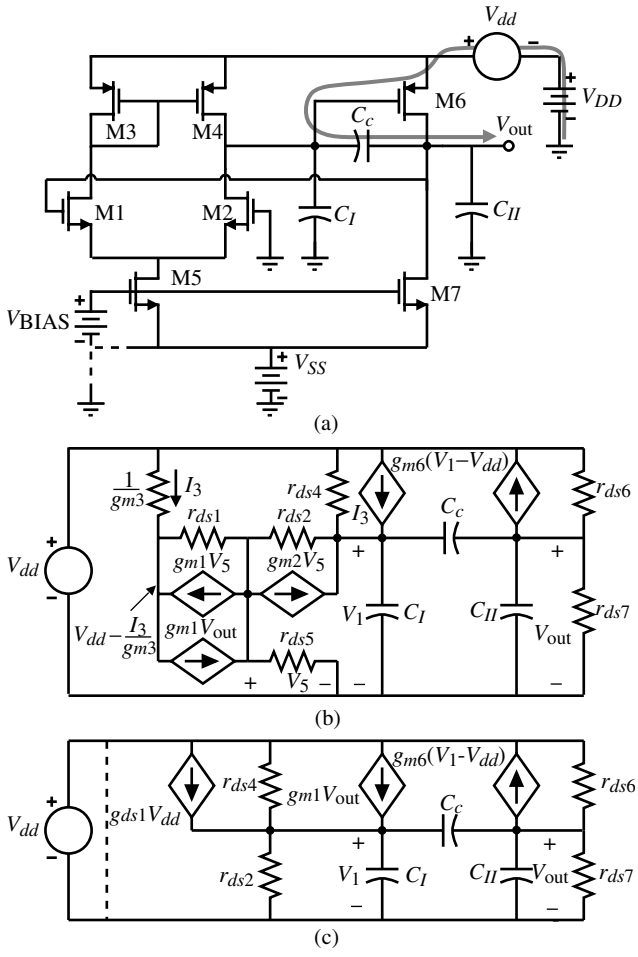

Figure 6.4-2 (a) Method for calculating the $PSRR^+$ of the two-stage op amp. (b) Model of (a). (c) Simplified equivalent of (b) assuming that $V_5 \approx 0$.

Using the generic notation for the two-stage op amp allows Eqs. (6.4-4) and (6.4-5) to be rewritten as

$$G_I V_{dd} = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_{\text{out}} \tag{6.4-6}$$

and

$$(g_{mII} + g_{ds6})V_{dd} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_{\text{out}} \tag{6.4-7}$$

where

$$G_I = g_{ds1} + g_{ds4} = g_{ds2} + g_{ds4} \tag{6.4-8}$$

$$G_{II} = g_{ds6} + g_{ds7} \tag{6.4-9}$$

$$g_{mI} = g_{m1} = g_{m2} \tag{6.4-10}$$

and

$$g_{mII} = g_{m6} \tag{6.4-11}$$

Solving for the transfer function, V_{out}/V_{dd}, and inverting the transfer function gives the following result:

$$\frac{V_{dd}}{V_{\text{out}}} = \frac{\begin{array}{c} s^2[C_cC_I + C_IC_{II} + C_{II}C_c] + s[G_I(C_c + C_{II}) + G_{II}(C_c + C_I) \\ + C_c(g_{mII} - g_{mI})] + G_IG_{II} + g_{mI}g_{mII} \end{array}}{s[C_c(g_{mII} + G_I + g_{ds6}) + C_I(g_{mII} + g_{ds6})] + G_Ig_{ds6}} \tag{6.4-12}$$

Using the technique described in Section 6.3, we may solve for the approximate roots of Eq. (6.4-12) as

$$\text{PSRR}^+ = \frac{V_{dd}}{V_{\text{out}}} \cong \left(\frac{g_{mI}g_{mII}}{G_Ig_{ds6}}\right)\left[\frac{\left(\dfrac{sC_c}{g_{mI}} + 1\right)\left(\dfrac{s(C_cC_I + C_IC_{II} + C_cC_{II})}{g_{mII}C_c} + 1\right)}{\left(\dfrac{sg_{mII}C_c}{G_Ig_{ds6}} + 1\right)}\right] \tag{6.4-13}$$

where we have assumed that g_{mII} is greater than g_{mI} and that all transconductances are larger than the channel conductances. For all practical purposes, Eq. (6.4-13) reduces to

$$\text{PSRR}^+ = \frac{V_{dd}}{V_{\text{out}}} = \left(\frac{g_{mI}g_{mII}}{G_Ig_{ds6}}\right)\left[\frac{\left(\dfrac{sC_c}{g_{mI}} + 1\right)\left(\dfrac{sC_{II}}{g_{mII}} + 1\right)}{\dfrac{sg_{mII}C_c}{G_Ig_{ds6}} + 1}\right] \tag{6.4-14}$$

$$= \left(\frac{G_{II}A_v(0)}{g_{ds6}}\right)\frac{\left(\dfrac{s}{GB} + 1\right)\left(\dfrac{s}{|p_2|} + 1\right)}{\left(\dfrac{sG_{II}A_v(0)}{g_{ds6}GB} + 1\right)}$$

Figure 6.4-3 illustrates the results of this analysis. It is seen that at a frequency of $GB/A_v(0)$ the PSRR^+ begins to roll off with a -20 dB/decade slope. Consequently, the PSRR^+ becomes degraded at high frequencies, which is a disadvantage of the two-stage, unbuffered op amp.

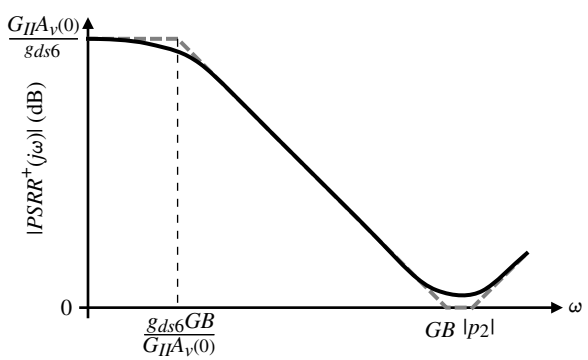

Figure 6.4-3 Magnitude of the PSRR^+ for a two-stage op amp.

The above calculation probably represents the most difficult encountered yet in this text. Unfortunately, while the results are clear, what causes the poor PSRR^+ is not. Because M6 is biased by the M7 current source, the gate–source voltage of M6 must remain constant. This requirement forces the gate of M6 to track the changes in V_{DD}, which are in turn transmitted by C_c to the output of the amplifier. This path from the power-supply ripple, V_{dd}, to the output is shown by the shaded arrow on Fig. 6.4-2(a). As the frequency increases, the impedance of the compensation capacitor, C_c, becomes low and the gate and drain of M6 begin to track one another and the gain from V_{dd} to V_{out} becomes approximately unity. Thus, the PSRR^+ has the approximate frequency response of $A_v(s)$ until the zeros at $-GB$ and $-p_2$ influence the frequency response. For the value of Example 6.3-1, the dc value of PSRR^+ is 68.8 dB and the roots are $z_1 = -5$ MHz, $z_2 = -15$ MHz, and $p_1 = -906.6$ Hz. Figures 6.6-18(a) and 6.6-18(b) are the simulated response of the PSRR^+ of Example 6.3-1 and compare very closely with these results.

Negative PSRR

Figure 6.4-4(a) shows the two-stage op amp in the configuration for calculating the negative PSRR (PSRR^-). The analysis of the PSRR^- depends on where the voltage V_{BIAS} is connected. Normally, V_{BIAS} would be a voltage generated by a current derived from V_{DD} flowing into an MOS diode. If this is the case, then the gate–source voltage of M5 and M7 would remain constant if the current is independent of V_{ss}. For this reason it is a good practice to use the current sources of Section 4.5 that are independent of power supply (or Fig. 6.3-9) to provide bias currents that are not influenced by power-supply changes. If for some reason V_{BIAS} was connected to ground, then as the power-supply changes, V_{ss} would cause a change in the gate–source voltage of M5 and M7 and this change would result in a change of currents in

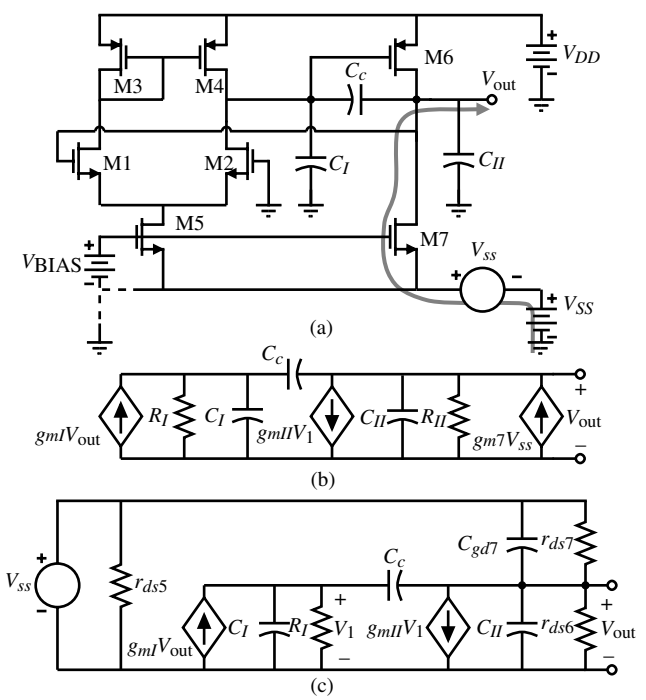

Figure 6.4-4 (a) Circuit for calculating the PSRR^- of the two-stage op amp. (b) Model of (a) when V_{BIAS} is grounded. (c) Model of (a) when V_{BIAS} is independent of V_{SS}.

the drains. While the common-mode rejection of the first stage would diminish the ac current in the drain of M5, the ac current in M7 would be multiplied by R_{II} and appear at the output as a change due to V_{ss}. The small-signal model for this case is shown in Fig. 6.4-4(b). The nodal equations corresponding to Fig. 6.4-4(b) are

$$0 = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_o \tag{6.4-15}$$

and

$$g_{m7}V_{ss} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II})V_o \tag{6.4-16}$$

Solving for V_{out}/V_{ss} and inverting gives

$$\frac{V_{ss}}{V_{\text{out}}} = \frac{\begin{array}{c}s^2[C_cC_I + C_IC_{II} + C_{II}C_c] + s[G_I(C_c + C_{II}) + G_{II}(C_c + C_I) \\ + C_c(g_{mII} - g_{mI})] + G_IG_{II} + g_{mI}g_{mII}\end{array}}{[s(C_c + C_I) + G_I]g_{m7}} \tag{6.4-17}$$

Again, using the technique described in Section 6.3, we may solve for the approximate roots of Eq. (6.4-17) as

$$\text{PSRR}^- = \frac{V_{ss}}{V_{\text{out}}} \cong \left(\frac{g_{mI}g_{mII}}{G_Ig_{m7}}\right)\left[\frac{\left(\dfrac{sC_c}{g_{mI}} + 1\right)\left(\dfrac{s(C_cC_I + C_IC_{II} + C_cC_{II})}{g_{mII}C_c} + 1\right)}{\left(\dfrac{s(C_c + C_I)}{G_I} + 1\right)}\right] \tag{6.4-18}$$

Equation (6.4-18) can be rewritten as approximately

$$\text{PSRR}^- = \frac{V_{ss}}{V_{\text{out}}} \cong \left(\frac{g_{mI}g_{mII}}{G_Ig_{m7}}\right)\left[\frac{\left(\dfrac{sC_c}{g_{mI}} + 1\right)\left(\dfrac{sC_{II}}{g_{mII}} + 1\right)}{\left(\dfrac{sC_c}{G_I} + 1\right)}\right] = \left(\frac{G_{II}A_v(0)}{g_{m7}}\right)\left[\frac{\left(\dfrac{s}{GB} + 1\right)\left(\dfrac{s}{|p_2|} + 1\right)}{\left(\dfrac{s}{GB}\dfrac{g_{mI}}{G_I} + 1\right)}\right] \tag{6.4-19}$$

Comparing this result with the PSRR^+ shows that the zeros are identical but the dc gain is smaller by nearly the amount of the second-stage gain and the pole is lower by the amount of the first-stage gain. Assuming the values of Example 6.3-1 gives a gain of 23.7 dB and a pole at -147 kHz. The dc value of PSRR^- is very poor for this case; however, this case can be avoided by correctly implementing V_{Bias}, which we consider next.

If the value of V_{Bias} is independent of V_{ss}, then the model of Fig. 6.4-4(c) results. The nodal equations for this model are

$$0 = (G_I + sC_c + sC_I)V_1 - (g_{mI} + sC_c)V_{\text{out}} \tag{6.4-20}$$

and

$$(g_{ds7} + sC_{gd7})V_{ss} = (g_{mII} - sC_c)V_1 + (G_{II} + sC_c + sC_{II} + sC_{gd7})V_{\text{out}} \tag{6.4-21}$$

Again, solving for V_{out}/V_{ss} and inverting gives

$$\frac{V_{ss}}{V_{\text{out}}} = \frac{\begin{array}{c}s^2[C_cC_I + C_IC_{II} + C_{II}C_c + C_IC_{gd7} + C_cC_{gd7}] + s[G_I(C_c + C_{II} + C_{gd7}) \\ + G_{II}(C_c + C_I) + C_c(g_{mII} - g_{mI})] + G_IG_{II} + g_{mI}g_{mII}\end{array}}{(sC_{gd7} + g_{ds7})(s(C_I + C_c) + G_I)} \tag{6.4-22}$$

Solving for the approximate roots of both the numerator and denominator gives

$$\text{PSRR}^- = \frac{V_{ss}}{V_{\text{out}}} \cong \left(\frac{g_{mI}g_{mII}}{G_Ig_{ds7}}\right)\left[\frac{\left(\dfrac{sC_c}{g_{mI}} + 1\right)\left(\dfrac{s(C_cC_I + C_IC_{II} + C_cC_{II})}{g_{mII}C_c} + 1\right)}{\left(\dfrac{sC_{gd7}}{g_{ds7}} + 1\right)\left(\dfrac{s(C_I + C_c)}{G_I} + 1\right)}\right] \tag{6.4-23}$$

Equation (6.4-23) can be rewritten as

$$\text{PSRR}^- = \frac{V_{ss}}{V_{\text{out}}} \approx \left(\frac{G_{II}A_v(0)}{g_{ds7}}\right)\left[\frac{\left(\dfrac{s}{GB} + 1\right)\left(\dfrac{s}{|p_2|} + 1\right)}{\left(\dfrac{sC_{gd7}}{g_{ds7}} + 1\right)\left(\dfrac{sC_c}{G_I} + 1\right)}\right] \tag{6.4-24}$$

This time the dc gain has been increased by the ratio of G_{II} to g_{ds7} and instead of one pole there are two. However, the pole at $-g_{ds7}/C_{gd7}$ is very large and can be ignored. The general frequency response of the negative PSRR is shown in Fig. 6.4-5. Again, assuming the values of Example 6.3-1, we find the dc gain as 76.7 dB. To find the poles we must assume a value of C_{gd7}. Let us assume a value of 10 fF for C_{gd7}. This gives the pole locations as -71.2 kHz and -149 kHz. The higher poles allow the PSRR to be much larger as the frequency increases compared to the positive PSRR. The result is that PSRR^- for the n-channel input, two-stage op amp is always greater than PSRR^+. Of course, this is reversed if a p-channel input op amp is used. Alternate methods of calculating the PSRR can be found in the literature [5,12].

The power-supply rejection ratio of the two-stage op amp has been shown to be poor because of the path from the power-supply ripple through the compensating capacitor to the output. We shall next examine the use of cascoding to improve the performance of the two-stage op amp. Cascoding will also allow a much better power-supply rejection ratio to be achieved.

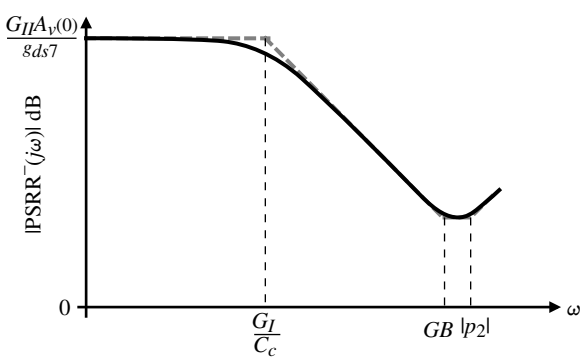

Figure 6.4-5 Magnitude of the PSRR^- for a two-stage op amp.

6.5 Cascode Op Amps

Previously, we introduced the design of a two-stage CMOS op amp. This op amp is probably one of the most widely used CMOS amplifiers to date. Its performance is well understood and experimental results compare closely to the design results. However, there are a number of unbuffered applications in which the performance of the two-stage op amp is not sufficient. Performance limitations of the two-stage op amp include insufficient gain, limited stable bandwidth caused by the inability to control the higher-order poles of the op amp, and a poor power-supply rejection ratio.

In this section we introduce several versions of the cascode CMOS op amp that offer improved performance in the above three areas. Three cascode op amp topologies will be discussed. The primary difference between these three topologies is where the cascode stage is applied in the block diagram of a general op amp shown in Fig. 6.1-1. First we will apply cascoding to the first stage followed by applying it to the second stage. Finally, we will examine a very useful version of the cascode op amp called the folded-cascode op amp. Throughout our presentation, we will illustrate how the gain of the cascode op amp can be enhanced using feedback.

Use of Cascoding in the First Stage

The motivation for using the cascode configuration to increase the gain can be seen by examining how the gain of the two-stage op amp could be increased. There are three ways in which the gain could be increased: (1) add additional gain stages, (2) increase the transconductance of the first or second stage, and (3) increase the output resistance seen by the first or second stage. Due to possible instability, the first approach is not attractive. Of the latter two approaches, the third is the more attractive because the output resistance increases in proportion to a decrease in bias current whereas the transconductance increases as the square root of the increase in bias current. Thus, it is generally more power efficient to increase r_{out} rather than g_m. Also, r_{out} can be dramatically increased by using special circuit techniques such as the cascode structure introduced in Sections 4.3 and 5.3 and the regulated cascode structure of Section 4.4.

Let us start by considering cascoding only the first stage of the two-stage op amp. Figure 6.5-1(a) shows the replacement of the transistors M1–M4 of Fig. 5.2-6 with the cascode configuration. Note that the bias for the cascode transistors, MC1 and MC2, is referenced to the common source node. If this were not the case, then the input common mode range would be severely limited. Using intuitive analysis to find the gain of this circuit, we see that v_{in} causes a current in M1 flowing downward of $0.5g_{m1}v_{in}$ and a current in M2 flowing upward of $0.5g_{m2}v_{in}$. These two currents flow toward the output of the amplifier creating the output voltage of $g_{m1}R_{out}v_{in}$ (where $g_{m1} = g_{m2}$). Thus, we can write the gain as

$$A_v = \frac{v_{out}}{v_{in}} = g_{m1}R_{out} \approx g_{m1}(g_{mC2}r_{dsC2}r_{ds2}) \| (g_{mC4}r_{dsC4}r_{ds4}) \tag{6.5-1}$$

If $g_{mN} = g_{mP}$ and $r_{dsN} = 2r_{dsP}$, then an estimate for the open-loop voltage gain, A_v, is

$$A_v \approx 0.2g_{mN}^2 r_{dsN}^2 \tag{6.5-2}$$

which is approximately equal to that of a two-stage op amp. The dominant pole of Fig. 6.5-1(a) is given by the output resistance and the capacitance. If C_L is the capacitance connected to the output, the magnitude of the dominant pole is

$$|p_1| \approx \frac{1}{R_{out}C_L} \tag{6.5-3}$$

If all higher-order poles are greater than the gain bandwidth, *GB*, then the gain bandwidth can be written as

$$GB = A_v|p_1| = \frac{g_{m1}}{C_L} \tag{6.5-4}$$

It is seen that Fig. 6.5-1(a) is self-compensated and should have good stability characteristics as long as the output is connected to a capacitor. With very little capacitance at the output, the nondominant poles may cause the phase margin of 90° to decrease. Also, because the amplifier is self-compensated, there is no Miller capacitor to deteriorate the PSRR. Consequently, Fig. 6.5-1 should have much better PSRR than the two-stage op amp using Miller compensation.

The floating battery, V_{Bias}, is used to bias MC1 and MC2 and to set the dc values of the drain–source voltages of M1 and M2. Typically, these voltage are close to V_{ds}(sat). In fact, if one wants to linearize the differential output current as a function of the differential input voltage, the transistors M1 and M2 can be operated in the linear or active region where the transconductance characteristics of the MOSFET are linear. The floating battery is implemented by the shaded area in Fig. 6.5-1(b) consisting of transistors MB1 through MB5. The common mode voltage is taken from the drains of MB1 and MB2 and applied to the input of a p-channel current mirror, MB3. MB4 provides the bias current for the MOS diode MB5, which implements the floating battery. The dc currents through MB1 and MB2 are determined by the *W/L* ratios between M1 and M2 and MB1 and MB2. $I_{MB1} + I_{MB2}$ will flow through MB5 creating V_{Bias}. The sinking current of M5 should be increased to accommodate I_{MB1} and I_{MB2}.

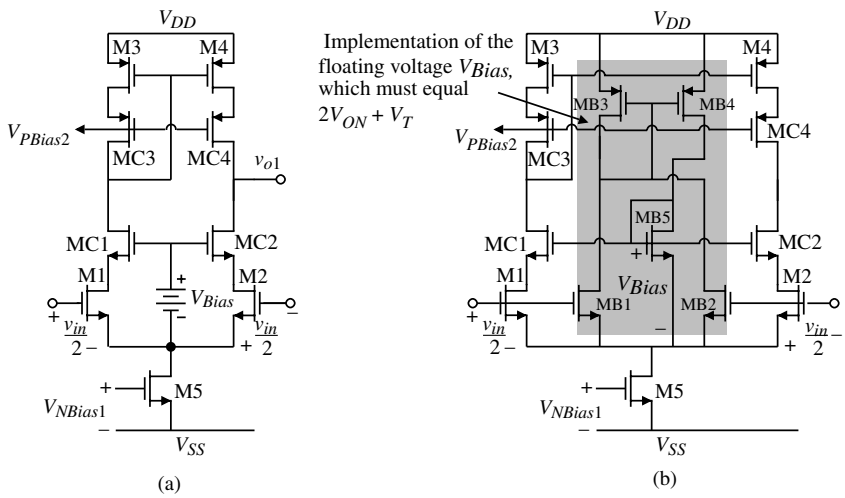

Figure 6.5-1 (a) Cascoding of the first stage of the two-stage op amp. (b) Implementation of the floating voltage, V_{Bias}.

Example 6.5-1

Single-Stage Cascode Op Amp Performance

Assume that all *W/L* ratios are 10 μm/1 μm, and that $I_{DS1} = I_{DS2} = 50$ μA of Fig. 6.5-1(a). Find the voltage gain of this op amp and the value of C_I if $GB = 10$ MHz. Use the model parameters of Table 3.1-2.

SOLUTION

The device transconductances are $g_{m1} = g_{m2} = g_{mI} = 331.7$ μS, $g_{mC2} = 331.7$ μS, and $g_{mC4} = 223.6$ μS. The output resistance of the NMOS and PMOS devices is 0.5 MΩ and 0.4 MΩ, respectively, giving an output resistance, R_{out}, of 25 MΩ. Therefore, the voltage gain is 8290 V/V. For a unity-gain bandwidth of 10 MHz, the value of C_I is 5.28 pF.

If higher gain or lower output resistance is required, then Fig. 6.5-1 needs to be cascaded with a second stage. However, we note that the output dc voltage of Fig. 6.5-1 is farther away from V_{DD} than that of the two-stage op amp. Driving a common-source PMOS output transistor from this stage would result in a large V_{DS}(sat), which would degrade the output-swing performance. To optimize the output swing of the second stage, it is better to perform a voltage translation before driving the gate of the output PMOS transistor. This is accomplished very easily using Fig. 6.5-2. MT1 and MT2 serve the function of level translation between the first and second stage. MT2 is a current source that biases the source follower, MT1. The current-voltage plot in Fig. 6.5-2 shows that without the level translation, the *W/L* of M6 would have to be reduced, lowering the output transconductance and increasing the saturation voltage. The small-signal gain from the output of the differential stage to the output of the voltage translator is close to unity with a small amount of phase shift. Compensation of Fig. 6.5-2 can be performed using Miller compensation techniques on the second stage as was illustrated in Section 6.2. One must be careful that the level shifter (MT1 and MT2) does not cause problems by introducing a pole at the gate of M6. Generally, the value of this pole is high enough not to cause problems. The typical voltage gain of this op amp could easily be 100,000 V/V.

An alternate approach to increasing the voltage gain of Fig. 6.5-1 is to use gain enhancement. Figure 6.5-3(a) shows the gain enhancement in Fig. 6.5-1 through the use of

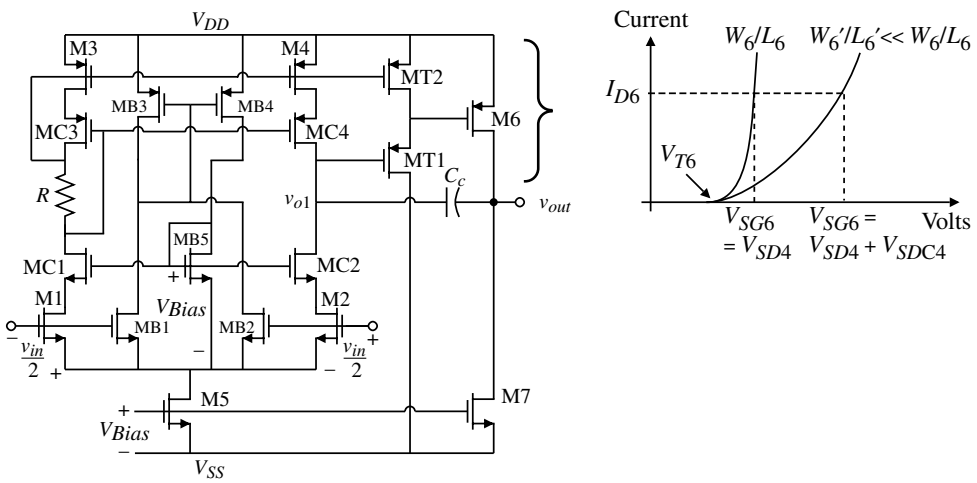

Figure 6.5-2 Two-stage op amp with a cascoded first stage.

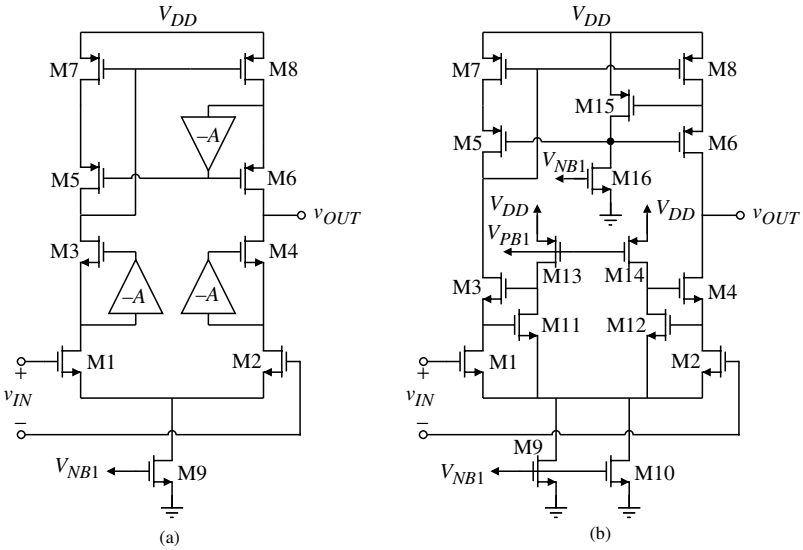

Figure 6.5-3 (a) Application of gain-enhancement amplifiers to increase the gain of Fig. 6.5-1. (b) Implementation of the gain-enhancement amplifiers in Fig. 6.5-3(a).

inverting amplifiers having a gain of $-A$. In Fig. 6.5-3(b) the gain amplifiers are simple inverters. Note that it is no longer necessary to implement the V_{Bias} voltage in Fig. 6.5-1. Through negative feedback, the current flowing in M13, M14, and M16 is forced through M11, M12, and M15, respectively. This sets the drain–source voltage of M1 and M2 and the source–drain voltage of M8. These voltages are not optimized for maximum output swing although it is possible to do so using a different version of the inverting amplifiers, illustrated later.

The gain of Fig. 6.5-3(a) can be written by inspection or intuitive analysis methods. The input voltage v_{in} causes a current in M1 flowing downward of $0.5g_{m1}v_{in}$ and a current flowing upward in M2 of $0.5g_{m2}v_{in}$. In contrast to Fig. 6.5-1, the output resistance is boosted by the magnitude of the gain-enhancement amplifiers. An approximation for the output resistance of Fig. 6.5-3 is

$$R_{out} \approx (Ar_{ds6}g_{m6}r_{ds8})\|(Ar_{ds2}g_{m4}r_{ds4}) \tag{6.5-5}$$

If $A \approx 0.5g_m r_{ds}$, $g_{mN} = g_{mP}$, and $r_{dsN} = 2r_{dsP}$, then the output resistance becomes approximately

$$R_{out} \approx 0.5g_m r_{ds}(0.2g_m r_{ds}^2) = 0.1g_m^2 r_{ds}^3 \tag{6.5-6}$$

Therefore, an estimate of the open-loop voltage gain of Fig. 6.5-3 is

$$A_v = \frac{v_{out}}{v_{in}} = g_{m1}R_{out} \approx 0.1g_m^3 r_m^3 \tag{6.5-7}$$

If $g_m r_{ds} \approx 100$, then the voltage gain is 100,000 V/V. The magnitude of the dominant pole is given by Eq. (6.5-3), but for Fig. 6.5-3 the output resistance is larger, causing the dominant pole to be smaller. Figure 6.5-4 illustrates the relationship between the frequency response of Fig. 6.5-1 and Fig. 6.5-3. As with Fig. 6.5-1, the op amp of Fig. 6.5-3 should have good PSRR characteristics.

Use of Cascoding in the Second Stage

Figure 6.5-5 shows the two-stage op amp with a cascaded second stage. The gain of the second stage will be increased, which enhances the Miller compensation. The approximate differential voltage gain will be $x(g_m r_{ds})^3$, where x is a constant between 0 and 1 and depends on the relative values of the p- and n-channel transconductances and conductances. Typically, x is close to 0.5. The increased gain is due to the increased output resistance of the second stage. The output pole, RHP zero, and *GB* of this op amp are the same as the two-stage op amp if C_c is the same. Lastly, the PSRR will be poor because of the Miller compensation. The relationship of the frequency response of Fig. 6.5-5 to a two-stage op amp is given by Fig. 6.5-4 where A would be the increased gain due to the cascoded second stage.

A balanced, two-stage op amp using a cascoded second stage is shown in Fig. 6.5-6. In this op amp, the first stage has been replaced with an MOS diode-loaded differential amplifier. The identical loads in the first stage create a balanced op amp (the resistance seen looking into the sources of M1 and M2 are identical). The currents in M3 and M4 are mirrored into M8 and M6, respectively, and then combined at the output to create the voltage gain. The small-signal differential voltage gain can written by inspection. The input differential voltage, v_{in}, causes a current of $0.5 g_{mN} v_{in}$ flowing downward in M1 and a current $0.5 g_{mN} v_{in}$ flowing upward in M2. Assuming a current mirror gain of k ($k = g_{m8}/g_{m3} = g_{m6}/g_{m4}$), the output voltage is found by summing the two currents flowing into the output resistance, R_{out}. Therefore, the voltage gain by inspection is

$$A_v = \frac{v_{out}}{v_{in}} = g_{mN} k R_{out} \tag{6.5-8}$$

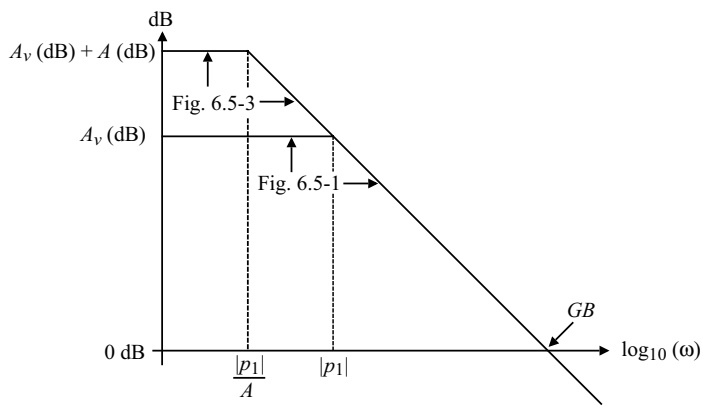

Figure 6.5-4 Comparison of the frequency response of Figs. 6.5-1 and 6.5-3.

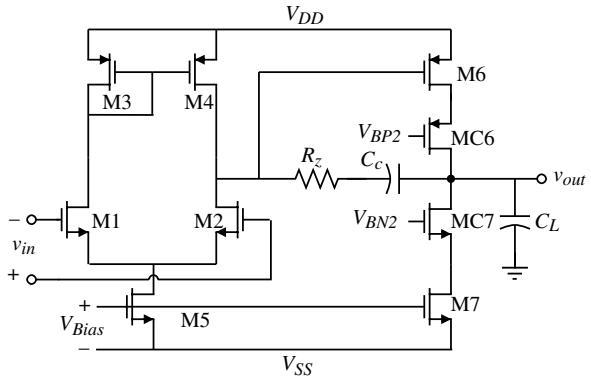

Figure 6.5-5 Two-stage op amp with a cascode second stage.

where

$$R_{out} \approx (g_{mN}r_{dsN^2})\|(g_{mP}r_{dsP^2}) \tag{6.5-9}$$

The actual value of the voltage gain depends on the value of k and the relative values of the p and n channel transconductances and conductances.

This op amp is self-compensated as the poles in the first stage are now much larger because of the lower-resistance loads of the first stage. The noise performance of this op amp may not be good unless some gain is realized in the first stage. This implies that $g_{mN} > g_{mP}$ in the first stage. The *GB* of this op amp is larger than the normal op amp by the factor of the current mirror gain, k.

Example 6.5-2

Balanced Two-Stage Op Amp Performance

Assume that all the n-channel transistors of Fig. 6.5-6 have the small-signal parameters of g_{mN} and r_{dsN} where $g_{mN}r_{dsN} = 100$ V/V. Furthermore, assume that $g_{mP} = 0.5g_{mN}$ and $r_{dsP} = 0.5r_{dsN}$. Find the small-signal differential voltage gain of the op amp and the first-stage gain if $k = 10$.

SOLUTION

From Eq. (6.5-9) we see that

$$R_{out} \approx (g_{mN}r_{dsN^2})\|(0.125g_{mN}r_{dsN^2}) = 0.11g_{mN}r_{dsN^2}$$

From Eq. (6.5-8) we see that the small-signal differential voltage gain is $1.1\ g_{mN^2}r_{dsN^2}$ or 11,000 V/V.

If $k = 10$, then the transconductance and conductances of M3 and M4 are $0.1g_{mP} = 0.05g_{mN}$. The voltage gain of the first stage is

$$A_{v1} = -0.5(g_{mN}/0.05g_{mN}) = -10 \text{ V/V}$$

This amount of first-stage voltage gain should be sufficient to maintain reasonable noise performance for Fig. 6.5-6.

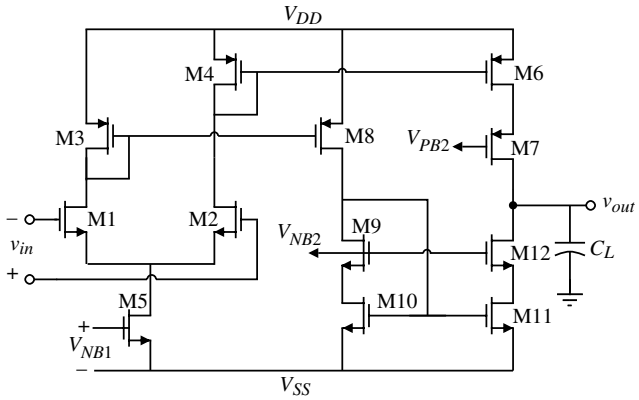

Figure 6.5-6 Op amp using cascode output stage.

The parasitic capacitance of op amps with a cascaded stage can be improved if a double polysilicon process is available [13]. Because the source and drain of a cascode pair are not connected externally, it is possible to treat the cascode pair as a dual-gate MOSFET. This is illustrated by considering the cascode pair shown in Fig. 6.5-7(a). The parasitic capacitance associated with the common drain/source connection can be virtually eliminated, as shown in Fig. 6.5-7(b), if a double polysilicon process is available. Obviously, one wants to minimize the overlap of the polysilicon layers in order to reduce the shunt input capacitance to the cascode pair. If the technology only has single polysilicon, then the layout should try to minimize the active area between the polysilicon of the cascoding transistor and the polysilicon of the cascoded transistor as shown in Fig. 6.5-7(c).

Folded-Cascode Op Amp

Figure 6.1-9 showed the architecture of an op amp called the folded-cascode op amp. This op amp uses cascoding in the output stage combined with an unusual implementation of the differential amplifier to achieve good input common-mode range. Thus, the folded-cascode op amp offers self-compensation, good input common-mode range, and the gain of a two-stage op amp. Let us examine this op amp in more detail and develop a design procedure that can be used as a starting point in its design.

To understand how the folded-cascode op amp optimizes the input common-mode range, consider Fig. 6.5-8. This figure shows the input common-mode range for an n-channel differential amplifier with a current mirror load and current source loads. From this figure and our previous considerations in Section 5.2, we know that Fig. 6.5-8(b) has a higher positive

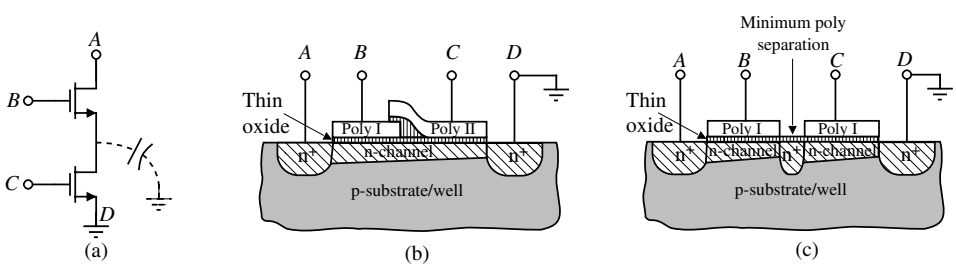

Figure 6.5-7 (a) Cascode amplifier with parasitic capacitance. Method of reducing source/drain-to-bulk capacitance for (b) a double poly technology and (c) a single poly technology.

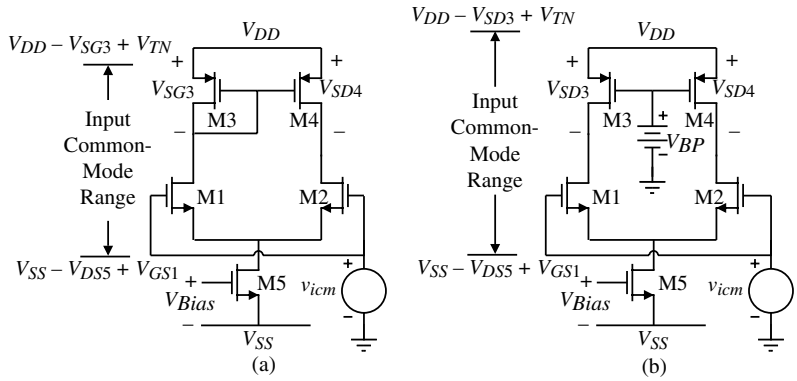

Figure 6.5-8 Input common-mode range for an n-channel input differential amplifier with (a) a current mirror load and (b) current source loads.

input common-mode voltage. In fact, if V_{SD3} is less than V_{TN}, then the positive input common-mode voltage of Fig. 6.5-8(b) can exceed V_{DD}. Figure 5.2-14 is one possible practical implementation of Fig. 6.5-8(b).

The problem with the differential amplifier of Fig. 6.5-8(b) is that it is difficult to get the single-ended output voltage without losing half the gain. One could follow Fig. 6.5-8(b) with another differential amplifier such as Fig. 6.5-8(a), which would achieve the desired result; however, compensation becomes more complex. A better approach is found in the folded topology op amps where the signal current is steered in the opposite direction of dc polarity. Problem 5.2-18 is an example of this architecture using a simple current mirror. However, the gain of this configuration is just that of a single stage. A better approach is to use a cascode mirror that achieves the gain of a two-stage op amp and allows for self-compensation. The basic form of an n-channel input, folded-cascode op amp is shown in Fig. 6.5-9 [12].

Note that the folded cascode does not require perfect balance of currents in the differential amp because excess dc current can flow into or out of the current mirror. Because the

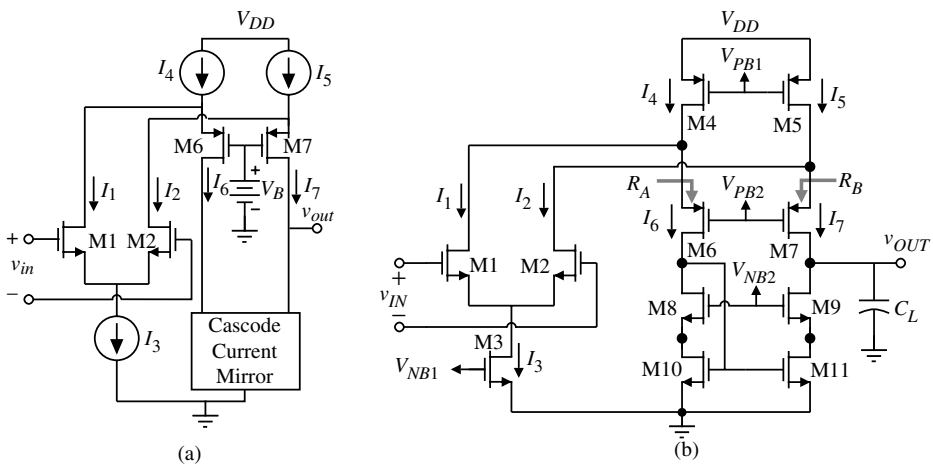

Figure 6.5-9 (a) Simplified version of an n-channel input, folded-cascode op amp. (b) Practical version (a).

drains of M1 and M2 are connected to the drains of M4 and M5, the extended positive input common-mode voltage of Fig. 6.5-8(b) is achieved. The bias currents I_3, I_4, and I_5 of the folded-cascode op amp should be designed so that the dc current in the cascode mirror never goes to zero. If the current should go to zero, this requires a delay in turning the mirror back on because of the parasitic capacitances that must be charged. For example, suppose v_{in} is large enough so that M2 is on and M1 is off. Then, all of I_3 flows through M1 and none through M2, resulting in $I_1 = I_3$ and $I_2 = 0$. If I_4 and I_5 are not greater than I_3, then the current I_6 will be zero. To avoid this, the values of I_4 and I_5 are normally between the value of I_3 and $2I_3$.

First, we will find the small-signal voltage gain by inspection and then repeat the small-signal circuit analysis. Figure 6.5-10 shows how a small voltage of ΔV applied at the differential input will create the small-signal currents in the folded-cascode amplifier of Fig. 6.5-9(b). Note that it has been assumed that the current flowing upward in M2 sees the same resistance in the drain of M5 as in the source of M7. This is because a cascode circuit (M9 and M11) is connected from the drain of M7 to ground. In Section 5.3, we learned that the resistance looking into the sources of the cascode transistors, M6 and M7, is

$$R_A(\text{M6}) \approx 1/g_{m6} \tag{6.5-10}$$

and

$$R_B(\text{M7}) \approx r_{ds} \tag{6.5-11}$$

We see that the current flowing into the output resistance, R_{out}, is $0.5(g_{m1} + 0.5\ g_{m2})\ v_{in}$. The approximate value of the output resistance is given as

$$R_{out} \approx (g_{m9}r_{ds9}r_{ds11}) \| [g_{m7}r_{ds7}(r_{ds2} \| r_{ds5})] \ \approx x(g_{mN}r_{dsN^2}) \tag{6.5-12}$$

where x is a constant between 0 and 1 depending on the relative values of the n- and p-transistor transconductances and conductances. $x = 0.0769$ if $g_{mP} = 0.5g_{mN}$ and $r_{dsP} = 0.5r_{dsN}$. Note the term $r_{ds2} \| r_{ds5}$ in the expression for the output resistance. This term comes about because M7 cascodes the parallel combination of M2 and M5. Finally, the small-signal differential voltage gain is written as

$$A_v = \frac{v_{out}}{v_{in}} = 0.5(g_{mN} + 0.5g_{mN})R_{out} \approx \frac{3}{4}g_{mN}R_{out} \approx \frac{3}{4}x(g_{mN}r_{dsN})^2 \tag{6.5-13}$$

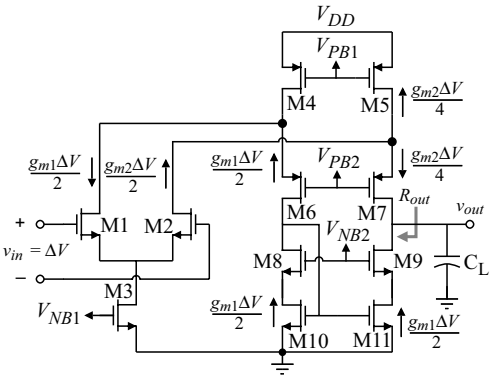

Figure 6.5-10 Intuitive analysis of the folded-cascode op amp of Fig. 6.5-9(b).

If $x = 0.0769$, the differential voltage gain is 769 V/V assuming that $g_{mN}r_{dsN} = 100$. We see that the gain of the folded-cascode op amp is similar to that of the two-stage op amp.

Unfortunately, we do not know exactly how the current flowing upward in M2 splits into M5 and M7. To examine this further, we will use small-signal circuit analysis methods to find the exact voltage gain of Fig. 6.5-9 approximated in Eq. (6.5-13). Figure 6.5-11 shows a model for the exact small-signal analysis. The resistances designated as R_A and R_B are the resistances looking into the sources of M6 and M7, respectively. R_A and R_B can be found using Eq. (5.3-15) of Section 5.3:

$$R_A = \frac{r_{ds6} + 1/g_{m10}}{1 + g_{m6}r_{ds6}} \approx \frac{1}{g_{m6}} \tag{6.5-14}$$

and

$$R_B = \frac{r_{ds7} + R_9}{1 + g_{m7}r_{ds7}} \approx \frac{R_9}{g_{m7}r_{ds7}} \approx r_{ds} \tag{6.5-15}$$

where

$$R_9 \approx g_{m9}r_{ds9}r_{ds11} \tag{6.5-16}$$

The small-signal voltage transfer function of Fig. 6.5-11 can be found as follows. The current i_{10} is written as

$$i_{10} = \frac{-g_{m1}(r_{ds1} \| r_{ds4})v_{in}}{2[R_A + (r_{ds1} \| r_{ds4})]} \approx \frac{-g_{m1}v_{in}}{2} \tag{6.5-17}$$

and the current i_7 can be expressed as

$$i_7 = \frac{g_{m2}(r_{ds2} \| r_{ds5})v_{in}}{2\left[\dfrac{R_9}{g_{m7}\, r_{ds7}} + (r_{ds2} \| r_{ds5})\right]} = \frac{g_{m2}v_{in}}{\left(1 + \dfrac{R_9(g_{ds2} + g_{ds5})}{g_{m7}r_{ds7}}\right)} = \frac{g_{m2}v_{in}}{2(1 + k)} \tag{6.5-18}$$

where a low-frequency unbalance factor, k, is defined as

$$k = \frac{R_9(g_{ds2} + g_{ds5})}{g_{m7}r_{ds7}} \tag{6.5-19}$$

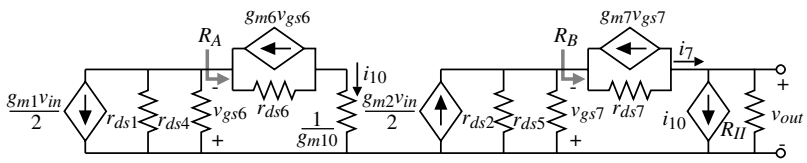

Figure 6.5-11 Small-signal model of Fig. 6.5-9(b).

Typical values of k are greater than one. The output voltage, v_{out}, is equal to the sum of i_7 and i_{10} flowing through R_{out}. Thus,

$$\frac{v_{out}}{v_{in}} = \left(\frac{g_{m1}}{2} + \frac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\frac{2+k}{2+2k}\right)g_{m1}R_{out} \tag{6.5-20}$$

where the output resistance, R_{out}, was given in Eq. (6.5-12). Comparing Eq. (6.5-20) with Eq. (6.5-13), we see that the intuitive approach assumes that $k = 1$.

The poles of the folded-cascode op amp occur at the nodes in Fig. 6.5-9(b) indicated by black dots. It can be seen that there are six poles. The dominant pole is the one at the output and is given as

$$p_{out} = \frac{-1}{R_{out}C_{out}} \tag{6.5-21}$$

The nondominant poles are given below.

Pole at node A:

$$p_A \approx \frac{-g_{m6}}{C_{gs} + 2C_{bd}} \tag{6.5-22}$$

Pole at node B:

$$p_B \approx \frac{-g_{m7}}{C_{gs} + 2C_{bd}} \tag{6.5-23}$$

Pole at drain of M6:

$$p_6 \approx \frac{-g_{m10}}{2C_{gs} + 2C_{bd}} \tag{6.5-24}$$

Pole at source of M8:

$$p_8 \approx \frac{-g_{m8}r_{ds8}g_{m10}}{C_{gs} + C_{bd}} \tag{6.5-25}$$

Pole at source of M9:

$$p_9 \approx \frac{-g_{m9}}{C_{gs} + C_{bd}} \tag{6.5-26}$$

It is interesting to note that the shunt feedback loop of M10 around M8 causes the resistance at the source of M8 to be extremely small. Consequently, p_8 is much larger than the other four nondominant poles.

Example 6.5-3

Folded-Cascode Op Amp Performance

Assume that all the n-channel transistors of Fig. 6.5-9(b) have the small-signal parameters of $g_{mN} = 100\ \mu S$, $r_{dsN} = 2\ M\Omega$, $g_{mP} = 50\ \mu S$, $r_{dsP} = 1\ M\Omega$, and $C_L = 10$ pF. Find the small-signal differential voltage gain, the output resistance, the dominant pole, and the *GB* of the folded-cascode op amp.

SOLUTION

From Eq. (6.5-12) we get

$$R_{out} \approx (g_{m9}r_{ds9}r_{ds11})\|[g_{m7}r_{ds7}(r_{ds2}\|r_{ds5})]$$

$$= 400\ M\Omega\|33.33\ M\Omega = 30.77\ M\Omega$$

From Eq. (6.5-19), k is equal to

$$k = \frac{R_9(g_{ds2} + g_{ds5})}{g_{m7}r_{ds7}} = \frac{400\ M\Omega\ (0.5\ \mu S + 1\ \mu S)}{50} = 12$$

From Eq. (6.5-20) we get

$$\frac{v_{out}}{v_{in}} = \left(\frac{2 + k}{2 + 2k}\right)g_{mN}R_{out} = \frac{7}{13}(100\ \mu S)(30.77\ M\Omega) = 1657\ V/V$$

The dominant pole is given as

$$p_{out} = \frac{-1}{R_{out}C_L} = \frac{-1}{(30.77\ M\Omega)(10\ pF)} = 3250\ rads/s\ (517\ Hz)$$

Therefore, the $GB = (1657)(3250) = 5.385$ Mrads/s (0.857 MHz)

The power-supply rejection ratio of the folded-cascode op amp of Fig. 6.5-9(b) has been greatly improved over the two-stage op amp. To examine the power-supply rejection properties consider the partial circuit of Fig. 6.5-9(b) shown in Fig. 6.5-12(a). The negative power-supply ripple is transferred directly to the gates M3, M8, M9, M10, and M11. Figure 6.5-12(a) ignores the coupling through the input differential amplifier. We note that the ripple also appears at the source of M9, preventing feedthrough of V_{ss} through C_{gd11} or r_{ds11}. Therefore, the only path for the ripple on V_{SS} is through C_{gd9} as indicated on Fig. 6.5-12.

Let us take a slightly different approach to calculate the PSRR. In this case, we will find the transfer function from the ripple to the output rather than the PSRR. We know that for good PSRR, this transfer function should be small. Figure 6.5-12(b) gives a

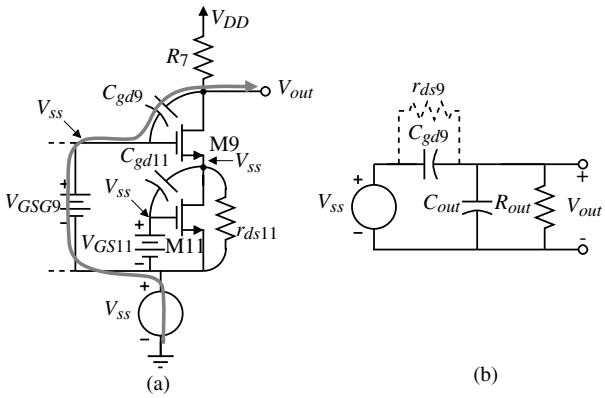

Figure 6.5-12 (a) Portion of Fig. 6.5-9(b) used to examine PSRR$^-$. (b) Model of (a).

small-signal model equivalent of Fig. 6.5-12(a). The transfer function of V_{out}/V_{ss} can be found as

$$\frac{V_{out}}{V_{ss}} \approx \frac{sC_{gd9}R_{out}}{sC_{out}R_{out} + 1} \tag{6.5-27}$$

Assuming the $C_{gd9}R_{out}$ is less than $C_{out}R_{out}$ allows us to sketch the response of Eq. (6.5-27) and the dominant pole differential frequency response as shown on Fig. 6.5-13. At low frequencies, we are assuming that other sources of V_{ss} injection become significant. Therefore, depending on the magnitude of other sources of V_{ss} injection, the magnitude of V_{out}/V_{ss} starts flat and then increases up to the dominant pole frequency and then remains flat. We see that this leads to a negative PSRR, which is at least as large as the magnitude of the differential voltage gain.

The positive power-supply injection is similar to the negative power-supply injection. The ripple appears at the gates of M4, M5, M6, and M7. The primary source of injection is through the gate–drain capacitor of M7, which is the same situation as for the negative power-supply injection.

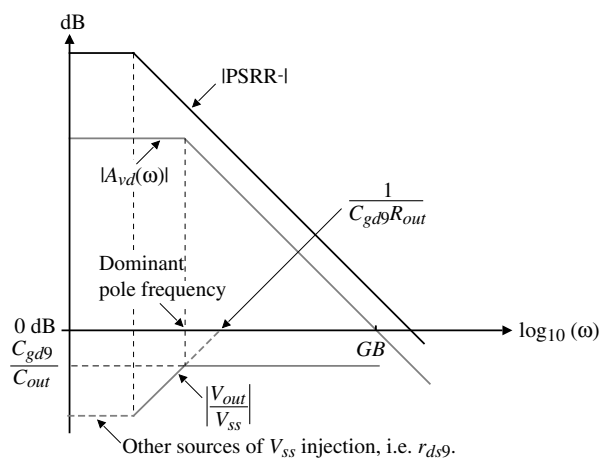

Figure 6.5-13 Approximate graphical illustration of the PSRR$^-$ for the folded-cascode op amp.

A typical approach to designing the folded-cascode op amp is illustrated below.

Example 6.5-4

Design of a Folded-Cascode Op Amp

Follow the procedure of Table 6.5-1 to design the folded-cascode op amp of Fig. 6.5-9(b) when the slew rate is 10 V/μs, the load capacitor is 10 pF, the maximum and minimum output voltages are 2 V and 0.5 V for a 2.5 V power supply, the *GB* is 10 MHz, the minimum input common-mode voltage is +1 V, and the maximum input common-mode voltage is 2.5 V. The differential voltage gain should be greater than 3000 V/V and the power dissipation should be less than 5 mW. Use $K_N' = 120\ \mu A/V^2$, $K_P' = 25\ \mu A/V^2$, $V_{TN} = |V_{TP}| = 0.5$ V, $\lambda_N = 0.06\ V^{-1}$, and $\lambda_P = 0.08\ V^{-1}$. Let $L = 0.5\ \mu m$.

Table 6.5-1 Design Approach for the Folded-Cascode Op Amp

Step	Relationship	Design Equation/Constraint	Comments
1	Slew rate	$I_3 = SR \cdot C_L$	
2	Bias currents in output cascodes	$I_4 = I_5 = 1.2I_3$ to $1.5I_3$	Avoid zero current in cascodes
3	Maximum output voltage, v_{out}(max)	$S_5 = \dfrac{2I_5}{K_P' V_{SD5}^2}$, $S_7 = \dfrac{2I_7}{K_P' V_{SD7}^2}$, ($S_4 = S_5$ and $S_6 = S_7$)	$V_{SD5}(\text{sat}) = V_{SD7}(\text{sat}) = 0.5[V_{DD} - V_{out}(\text{max})]$
4	Minimum output voltage, v_{out}(min)	$S_{11} = \dfrac{2I_{11}}{K_N' V_{DS11}^2}$, $S_9 = \dfrac{2I_9}{K_N' V_{DS9}^2}$, ($S_{10} = S_{11}$ and $S_8 = S_9$)	$V_{DS9}(\text{sat}) = V_{DS11}(\text{sat}) = 0.5[V_{out}(\text{min}) - V_{SS}]$
5	$GB = \dfrac{g_{m1}}{C_L}$	$S_1 = S_2 = \dfrac{g_{m1}^2}{K_N' I_3} = \dfrac{GB^2 C_L^2}{K_N' I_3}$	
6	Minimum input CM	$S_3 = \dfrac{2I_3}{K_N'(V_{in}(\text{min}) - V_{SS} - \sqrt{(I_3 K_N' S_1)} - V_{T1})^2}$	
7	Maximum input CM	$S_4 = S_5 = \dfrac{2I_4}{K_P'(V_{DD} - V_{in}(\text{max}) + V_{T1})}2$	S_4 and S_5 must meet or exceed value in step 3
8	Differential-voltage gain	$\dfrac{v_{out}}{v_{in}} = \left(\dfrac{g_{m1}}{2} + \dfrac{g_{m2}}{2(1+k)}\right)R_{out} = \left(\dfrac{2+k}{2+2k}\right)g_{m1}R_{out}$	$k = \dfrac{R_{II}(g_{ds2} + g_{ds4})}{g_{m7} r_{ds7}}$
9	Power dissipation	$P_{diss} = (V_{DD} - V_{SS})(I_3 + I_{10} + I_{11})$	

SOLUTION

Following the approach outlined in Table 6.5-1 we obtain the following results:

$$I_3 = SR \cdot C_L = 10 \times 10^6 \cdot 10^{-11} = 100\ \mu A$$

Select $I_4 = I_5 = 125\ \mu A$.

Next, we see that the value of $0.5[V_{DD} - V_{out}(\text{min})]$ is 0.5 V/2 or 0.25 V. Thus,

$$S_4 = S_5 = \frac{2 \cdot 125\ \mu A}{25\ \mu A/V^2 \cdot (0.25V)^2} = \frac{2 \cdot 125 \cdot 16}{225} = 160$$

and assuming worst-case currents in M6 and M7 gives

$$S_6 = S_7 = \frac{2 \cdot 125\ \mu\text{A}}{25\ \mu\text{A/V}^2(0.25\ \text{V})^2} = \frac{2 \cdot 125 \cdot 16}{25} = 160$$

The value of $0.5[V_{out}(\text{min}) - |V_{SS}|]$ is also 0.25 V, which gives the value of S_8, S_9, S_{10}, and S_{11} as

$$S_8 = S_9 = S_{10} = S_{11} = \frac{2 \cdot I_8}{K_N' V_{DS8}{}^2} = \frac{2 \cdot 125}{120 \cdot (0.25)^2} = 20$$

In step 5, the value of GB gives S_1 and S_2 as

$$S_1 = S_2 = \frac{GB^2 \cdot C_L^2}{K_N' I_3} = \frac{(20\pi \times 10^6)^2 (10^{-11})^2}{120 \times 10^{-6} \cdot 100 \times 10^{-6}} = 32.9 \approx 33$$

The minimum input common-mode voltage defines S_3 as

$$S_3 = \frac{2I_3}{K_N' \left(V_{in}(\text{min}) - V_{SS} - \sqrt{\dfrac{I_3}{K_N' S_1}} - V_{T1} \right)^2}$$

$$= \frac{200 \times 10^{-6}}{110 \times 10^{-6} \left(-1.5 + 2.5 - \sqrt{\dfrac{100}{120 \cdot 35.9}} - 0.75 \right)^2} = 14.3 \approx 15$$

We need to check that the values of S_4 and S_5 are large enough to satisfy the maximum input common-mode voltage. The maximum input common-mode voltage of 2.5 requires

$$S_4 = S_5 \geq \frac{2I_4}{K_P'[V_{DD} - V_{in}(\text{max}) + V_{T1}]} = \frac{2 \cdot 125\ \mu\text{A}}{25 \times 10^{-6}\ \mu\text{A/V}^2[0.5\ \text{V}]^2} = 40$$

which is much less than 160. In fact, with $S_4 = S_5 = 160$, the maximum input common-mode voltage is 2.75 V.

The power dissipation is found to be

$$P_{diss} = 2.5\ \text{V}(125\ \mu\text{A} + 125\ \mu\text{A} + 125\ \mu\text{A}) = 0.625\ \text{mW}$$

The small-signal voltage gain requires the following values to evaluate:

$$S_4, S_5\text{: } g_m = \sqrt{2 \cdot 125 \cdot 25 \cdot 160} = 1000\ \mu\text{S} \text{ and } g_{ds} = 125 \times 10^{-6} \cdot 0.08 = 10\ \mu\text{S}$$

S_6, S_7: $g_m = \sqrt{2 \cdot 75 \cdot 25 \cdot 160} = 774.6\ \mu S$ and $g_{ds} = 75 \times 10^{-6} \cdot 0.08 = 6\ \mu S$

S_8, S_8, S_{10}, S_{11}: $g_m = \sqrt{2 \cdot 75 \cdot 120 \cdot 20} = 600\ \mu S$ and $g_{ds} = 75 \times 10^{-6} \cdot 0.06 = 4.5\ \mu S$

S_1, S_2: $g_{mI} = \sqrt{2 \cdot 50 \cdot 120 \cdot 33} = 629\ \mu S$ and $g_{ds} = 50 \times 10^{-6}(0.06) = 3\ \mu S$

Thus,

$$R_9 \approx g_{m9}\, r_{ds9}\, r_{ds11} = (600\ \mu S)\left(\frac{1}{4.5\ \mu S}\right)\left(\frac{1}{4.5\ \mu S}\right) = 29.63\ M\Omega$$

$$R_{out} \approx (29.63\ M\Omega) \parallel (774.6\ \mu S)\left(\frac{1}{6\ \mu S}\right)\left(\frac{1}{10\ \mu S + 3\ \mu S}\right) = 7.44\ M\Omega$$

$$k = \frac{R_9(g_{ds2} + g_{ds5})}{g_{m7}\, r_{ds7}} = \frac{7.44\ M\Omega(3\ \mu S + 10\ \mu S)(6\ \mu S)}{774.6\ \mu S} = 0.75$$

The small-signal differential-input voltage gain is

$$A_{vd} = \left(\frac{2+k}{2+2k}\right) g_{mI} R_{out} = \left(\frac{2+0.75}{2+1.5}\right) 0.629 \times 10^{-3} \cdot 7.44 \times 10^{6} = (0.786)(4680) = 3678\ V/V$$

The gain is slightly larger than required by the specifications but this should be okay.

As before, we can enhance the gain of the folded-cascode op amp using inverting amplifiers with a gain of $-A$ in Fig. 6.5-14. A p-channel differential input has been used just to remind the reader that either type of input stage can be used. In the case of Fig. 6.5-14, the lower ICMR could include the lower rail. The output resistance and the voltage gain of the folded cascode are all increased by the magnitude of A.

The enhancement amplifiers used to increase the gain are examined in more detail. Figure 6.5-15 shows one implementation of the lower and upper enhancement amplifiers in

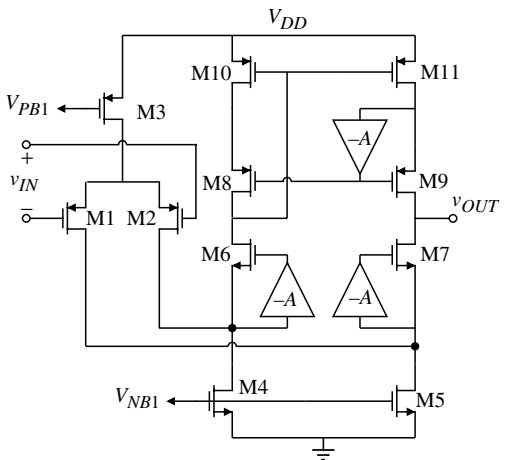

Figure 6.5-14 Enhanced-gain folded-cascode op amp.

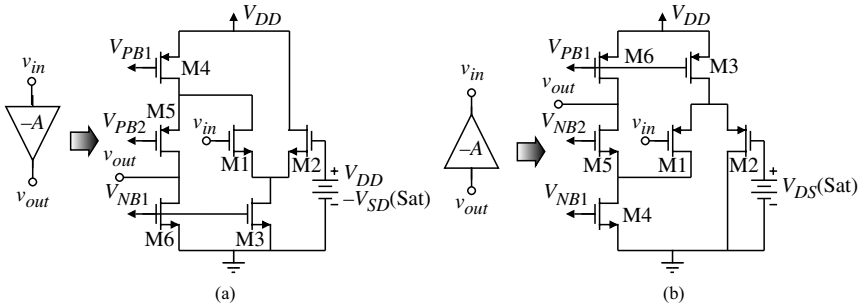

Figure 6.5-15 Enhancement amplifier realizations for (a) the upper amplifier and (b) the lower amplifier.

Fig. 6.5-14. These amplifiers could be used in any of the previous op amps that used enhancement amplifiers. The gain of the upper enhancement amplifier of Fig. 6.5-15(a) is

$$A_v(\text{upper}) \approx -0.5 g_{m1}\, r_{ds6} = -0.5 g_{mN}\, r_{dsN} \tag{6.5-28}$$

and the gain of the lower enhancement amplifier of Fig. 6.5-15(b) is

$$A_v(\text{lower}) \approx -0.5 g_{m1}\, r_{ds6} = -0.5 g_{mP}\, r_{dsP} \tag{6.5-29}$$

We see that the enhancement amplifiers use a folded-cascode architecture with a uncascoded load.

We can see that through negative feedback, the voltage at the input of the enhancement amplifier is equal to the voltage connected to the gate of M2. It helps to remember that the output of the enhancement amplifier is connected back to the input through a source follower. Typically, the gate voltage of M2 of lower enhancement amplifiers in Fig. 6.5-15(b) is selected to make the drain–source voltage of M4 and M5 in Fig. 6.5-14 equal to V_{DS}(sat). Similarly, the gate voltage of M2 in the upper enhancement amplifier of Fig. 6.5-15(a) is selected to make the source–drain voltage of M11 in Fig. 6.5-14 equal to V_{SD}(sat).

The total transistor realization of Fig. 6.5-14 is shown in Fig. 6.5-16. The shaded areas are the enhancement amplifiers. We examine the performance of this amplifier in the following example.

Example 6.5-5

Performance of the Enhanced Gain Folded-Cascode Op Amp

Assume that all the n-channel transistors of Fig. 6.5-16 have the small-signal parameters of $g_{mN} = 100\ \mu\text{S}$, $r_{dsN} = 2\ \text{M}\Omega$, $g_{mP} = 50\ \mu\text{S}$, $r_{\text{dsP}} = 1\ \text{M}\Omega$, and $C_L = 10$ pF. Find the small-signal differential voltage gain, the output resistance, the dominant pole, and the *GB* of the folded-cascode op amp.

SOLUTION

The output resistance of Fig. 6.5-16 can be approximated as

$$R_{out} \approx [A_v(\text{upper})\, g_{m9} r_{d9} r_{ds11}\,] \| [A_v(\text{lower})\, g_{m7} r_{ds7}\, (r_{ds2} \| r_{ds5})]$$

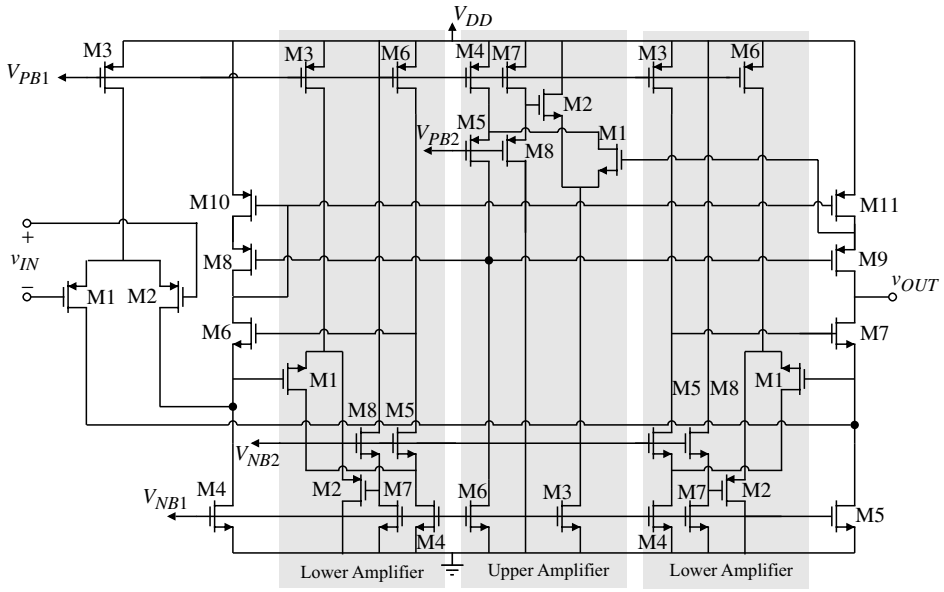

Figure 6.5-16 Complete transistor realization of the enhanced gain folded-cascode op amp.

$$= [(g_{mN}r_{dsN})\, g_{mP}r_{dsP^2}] \| [(g_{mP}r_{dsP})\, g_{mN}r_{dsN}\, (r_{dsP} \| r_{dsN})]$$

$$= (10\ \text{G}\Omega) \| (6.67\ \text{G}\Omega\ ) = 4\ \text{G}\Omega$$

If we assume the current flowing from M1 divides evenly between M5 and the upper path (M7), then the output voltage can be written as

$$A_v = \frac{V_{out}}{v_{in}} = 0.5(g_{mP} + 0.5g_{mP})R_{out} = 0.75g_{mP}R_{out} = 150{,}000\ \text{V/V}$$

The dominant pole of this op amp is

$$p_{\text{dominant}} \approx \frac{1}{R_{out}C_L} = 25\ \text{rads/s}\ (4\ \text{Hz})$$

Within all inverting enhancement amplifiers with any appreciable gain, there is a dominant pole. We can see from Fig. 6.5-15 that the enhancement amplifier pole is approximately

$$p_{\text{enhancement}} \approx \frac{1}{r_{ds}(C_{gs} + 2C_{db} + 2C_{gd})} \tag{6.5-30}$$

As the frequency increases, the magnitude of A will decrease. This will cause the output resistance to decrease. However, since the magnitude of the pole of the enhancement amplifier is normally much larger than the magnitude of the dominant pole, the load capacitor has shorted out any influence a change in R_{out} might have.

The higher-order poles of the enhanced gain folded-cascode op amp of Fig. 6.5-16 are listed below.

1. Pole at the source of M6:

$$p_6 \approx \frac{-Ag_{m6}}{2C_{gs} + 2C_{bd}} \tag{6.5-31}$$

2. Pole at the source of M7:

$$p_7 \approx \frac{-Ag_{m7}}{2C_{gs} + 2C_{bd}} \tag{6.5-32}$$

3. Pole at the drain of M8:

$$p_8 \approx \frac{-Ag_{m10}}{2C_{gs} + 2C_{bd}} \tag{6.5-33}$$

4. Pole at the source of M9:

$$p_9 \approx \frac{-Ag_{m9}}{2C_{gs} + C_{bd}} \tag{6.5-34}$$

5. Pole at the drain of M10:

$$p_{10} \approx \frac{-g_{m8}\, r_{ds8}\, g_{m10}}{C_{gs} + C_{bd}} \tag{6.5-35}$$

Although it looks like most of the nondominant poles of Fig. 6.5-16 are increased by the magnitude of A, the fact that the enhancement amplifier gain will decrease because of the pole of the enhancement amplifier will cause the nondominant poles of the enhanced gain folded-cascode op amp to approach those of the folded-cascode op amp.

Op amps using the cascode configuration enable the designer to optimize some of the second-order performance specifications not possible with the classical two-stage op amp. In particular, the cascode technique is useful for increasing the gain and increasing the value of PSRR, and it allows self-compensation when used at the output. This flexibility has allowed the development of high-performance unbuffered op amps suitable for CMOS technology. Such amplifiers are widely used in present-day integrated circuits for telecommunications applications.

6.6 Simulation and Measurement of Op Amps

In designing a CMOS op amp, the designer starts with building blocks whose performance can be analyzed to a first-order approximation by hand/calculator methods of analysis. The advantage of this step is the insight it provides to the designer as the design of the circuit develops. However, at some point the designer must turn to a better means of simulation. For the CMOS op amp this is generally a computer-analysis program such as SPICE. With the insight of the first-order analysis and the modeling capability of SPICE, the circuit design

can be optimized and many other questions (such as tolerances, stability, and noise) can be examined.

Fabrication follows the simulation and layout of the MOS op amp. After fabrication the MOS op amp must be tested and evaluated. The techniques for testing various parameters of the op amp can be as complex as the design of the op amp itself. Each specification must be verified over a large number of op amps to ensure a working op amp in case of process variations.

Simulation and Measurement Techniques

The objective of this section is to provide the background for simulating and testing a CMOS op amp. We shall consider methods of simulating an op amp that are appropriate to SPICE but the concepts are applicable to other types of computer-simulation programs. Because the simulation and measurement of the CMOS op amp are almost identical, they are presented simultaneously. The only differences found are in the parasitics that the actual measurement introduces in the op amp circuit and the limited bandwidths of the instrumentation.

The categories of op amp measurements and simulations discussed include open-loop gain, open-loop frequency response (including the phase margin), input-offset voltage, common-mode gain, power-supply rejection ratio, common-mode input- and output-voltage ranges, open-loop output resistance, and transient response including slew rate. Configurations and techniques for each of these measurements will be presented in this section.

Simulating or measuring the op amp in an open-loop configuration is one of the most difficult steps to perform successfully. The reason is the high differential gain of the op amp. Figure 6.6-1 shows how this step might be performed. The op amp under test or simulation is shaded to differentiate it from other op amps that may be used to implement the test or simulation. V_{OS} is an external voltage whose value is adjusted to keep the dc value of v_{OUT} between the power-supply limits. Without V_{OS} the op amp will be driven to the positive or negative power supply for either the measurement or simulation cases. The resolution necessary to find the correct value of V_{OS} usually escapes the novice designer. It is necessary to be able to find V_{OS} to the accuracy of the magnitude of the power supply divided by the low-frequency differential gain (typically in the range of millivolts). Although this method works well for simulation, the practical characteristics of the op amp make the method almost impossible to use for measurement.

A method more suitable for measuring the open-loop gain is shown in the circuit of Fig. 6.6-2. In this circuit it is necessary to select the reciprocal *RC* time constant a factor of $A_v(0)$ less than the anticipated dominant pole of the op amp. Under these conditions, the op amp has total dc feedback, which stabilizes the bias. The dc value of v_{OUT} will be exactly the dc value of v_{IN}. The true open-loop frequency characteristics will not be observed until the frequency is approximately $A_v(0)$ times $1/RC$. Above this frequency, the ratio of v_{OUT} to v_{IN} is

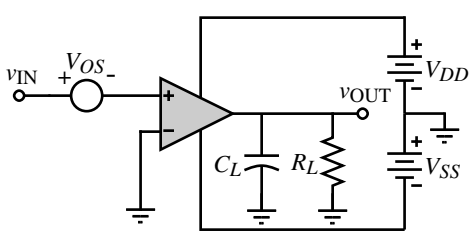

Figure 6.6-1 Open-loop mode with offset compensation.

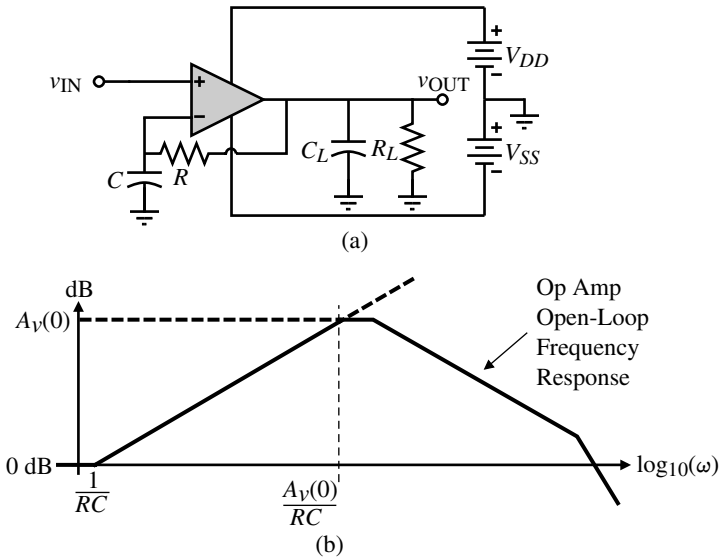

Figure 6.6-2 (a) A method of measuring the open-loop characteristics with dc bias stability. (b) Asymptotic magnitude plot of the voltage-transfer function.

essentially the open-loop gain of the op amp. This method works well for both simulation and measurement.

Simulation or measurement of the open-loop gain of the op amp will characterize the open-loop transfer curve, the open-loop output-swing limits, the phase margin, the dominant pole, the unity-gain bandwidth, and other open-loop characteristics. The designer should connect the anticipated loading at the output in order to get meaningful results. In some cases, where the open-loop gain is not too large, the open-loop gain can be measured by applying v_{IN} in Fig. 6.6-3 and measuring v_{OUT} and v_I. In this configuration, one must be careful that R is large enough not to cause a dc current load on the output of the op amp.

The dc input-offset voltage can be measured using the circuit of Fig. 6.6-4. If the dc input-offset voltage is too small, it can be amplified by using a resistor divider in the negative-feedback path. One must remember that V_{OS} will vary with time and temperature and is very difficult to precisely measure experimentally. Interestingly enough, V_{OS} cannot be simulated. The reason is that the input-offset voltage is not only due to the bias mismatches as discussed for the two-stage op amp (systematic offset) but is due to device and component mismatches. Presently, most simulators do not have the ability to predict device and component mismatches.

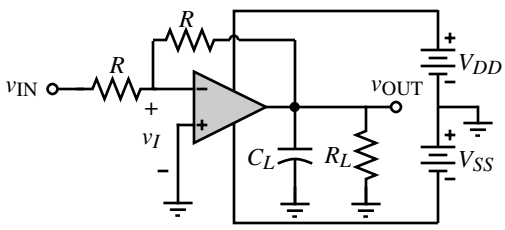

Figure 6.6-3 Configuration for simulating or measuring the open-loop frequency response for moderate-gain op amps.

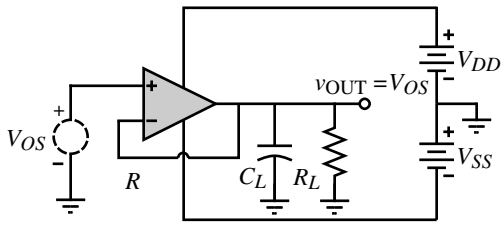

Figure 6.6-4 Configuration for measuring the input-offset voltage and the simulation of the systematic offset voltage of an op amp.

The common-mode gain is most easily simulated or measured using Fig. 6.6-5. It is seen that if V_{OS} fails to keep the op amp in the linear region, this configuration will fail, which is often the case in experimental measurements. More often than not, the designer wishes to measure or simulate the CMRR. The common-mode gain could be derived from the CMRR and the open-loop gain if necessary.

A method of measuring the CMRR of an op amp, which is more robust, is given in Fig. 6.6-6 [14]. While the method can be used for dynamic characterization, we will explain the operation from a static viewpoint. Assume that first all v_{SET} voltage sources are increased by some amount, say, 1 V. This causes the output and the power supplies to the op amp under test to be increased by 1 V. As a result of this a voltage, v_I, will appear at the input of the op amp under test. v_I will be equal to the common-mode output voltage of 1 V divided by the differential voltage gain of the op amp under test. This change in v_I can be measured at v_{OS} as approximately 1000 v_I. Let this value of v_{OS} be designated as V_{OS1}. Next, all v_{SET} voltage sources are decreased by the same amount (in order to cancel any positive or negative signal differences). This measure of v_{OS} is designated as V_{OS2}. The CMRR can be found as

$$\text{CMRR} = \frac{2000}{|V_{OS1} - V_{OS2}|} \tag{6.6-1}$$

If the v_{SET} sources are replaced by a small-signal voltage called v_{icm}, then it can be shown (in Problem 6.6-4) that the CMRR can be given as

$$\text{CMRR} = \frac{1000\, v_{icm}}{v_{os}} \tag{6.6-2}$$

Using this approach, one could apply v_{icm} and sweep the frequency to measure v_{os} and the CMRR as a function of frequency.

Another way to measure the CMRR would be to measure first the differential voltage gain in dB and then the common-mode voltage gain in dB by applying a common-mode signal to the input. The CMRR in dB could be found by subtracting the common-mode voltage

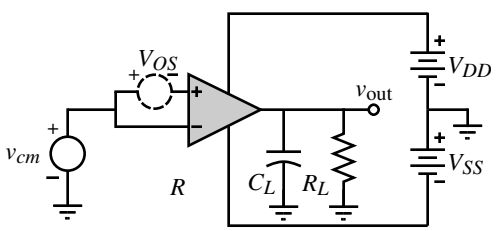

Figure 6.6-5 Configuration for simulating the common-mode gain.

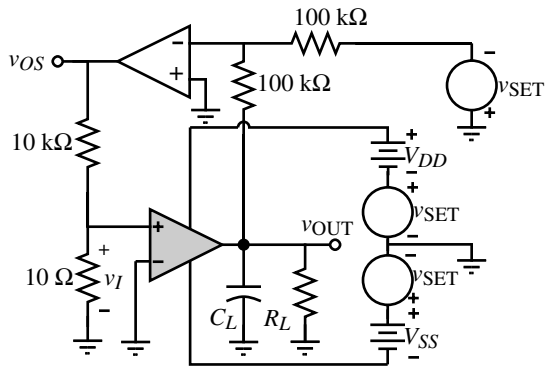

Figure 6.6-6 Circuit used to measure CMMR and PSRR.

gain in dB from the differential-mode voltage gain in dB. If the measurement system is associated with a controller or computer, this could be done automatically.

While the above methods could be used for simulation of the CMRR, there are easier methods if simulation of CMRR is the goal. The objective of simulation is to get an output that is equal to CMRR or can be related to CMRR. Figure 6.6-7(a) shows a method that can accomplish this objective. Two identical voltage sources designated as V_{cm} are placed in series with both op amp inputs where the op amp is connected in the unity-gain configuration. A model of this circuit is shown in Fig. 6.6-7(b). It can be shown that

$$\frac{V_{\text{out}}}{V_{cm}} = \frac{\pm A_c}{1 + A_v - (\pm A_c/2)} \cong \frac{|A_c|}{A_v} = \frac{1}{\text{CMRR}} \tag{6.6-3}$$

Computer simulation can be used to calculate Eq. (6.6-3) directly. If the simulator has a postprocessing capability, then it is usually possible to plot the reciprocal of the transfer function so that CMRR can be plotted directly. Figure 6.6-8(a) shows the simulation results of the magnitude of the CMRR for the op amp of Example 6.3-1 and Fig. 6.6-8(b) gives the phase response of the CMRR. It is seen that the CMRR is quite large for frequencies up to 100 kHz.

The configuration of Fig. 6.6-6 can also be used to measure the power-supply rejection ratio, PSRR. The procedure sets all v_{SET} voltage sources to zero except for the one in series with V_{DD}. Set this source equal to +1 V. In this case, v_I is the input-offset voltage for V_{DD} + 1 V.

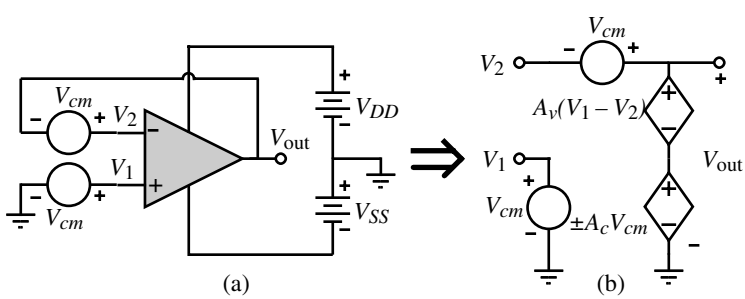

Figure 6.6-7 (a) Configuration for the direct simulation of CMRR. (b) Model for (a).

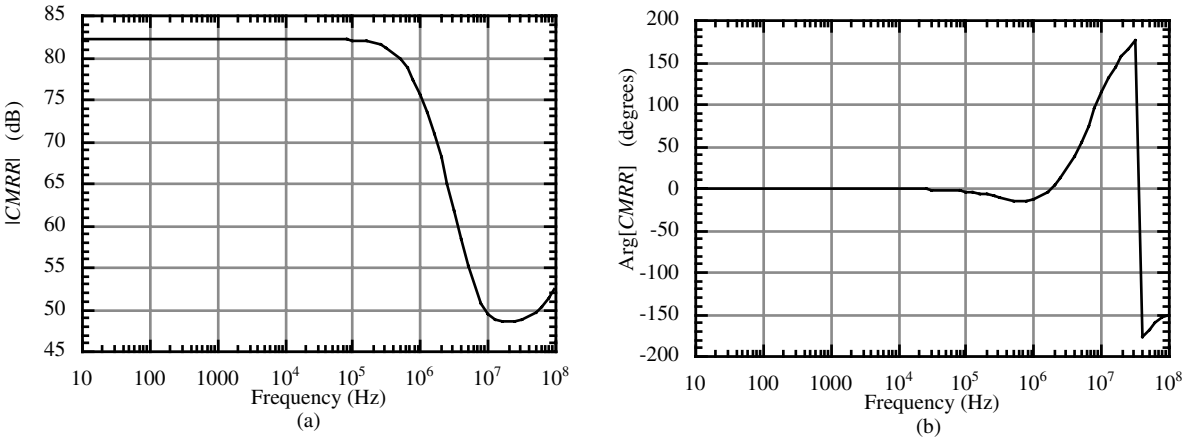

Figure 6.6-8 CMRR frequency response of Example 6.3-1 with $C_c = 10$ pF. (a) Magnitude response. (b) Phase response.

Measure V_{OS} under these conditions and designate it as V_{OS3}. Next, set V_{DD} to $V_{DD} - 1$ V using the v_{SET} source in series with V_{DD}; measure V_{OS} and designate it as V_{OS4}. The PSRR of the V_{DD} supply is given as

$$\text{PSRR of } V_{DD} = \frac{2000}{|V_{OS3} - V_{OS4}|} \tag{6.6-4}$$

Similarly for the V_{SS} rejection ratio, change V_{SS} and keep V_{DD} constant while V_{OUT} is at 0 V. The above formula can be applied in the same manner to find the negative power-supply rejection ratio. This approach is also suitable for measuring PSRR as a function of frequency if the appropriate v_{SET} voltage sources are replaced with a sinusoid.

Figure 6.6-9 shows a configuration similar to Fig. 6.4-1 that is suitable for measuring the PSRR as a function of frequency. A small sinusoidal voltage is inserted in series with V_{DD} (V_{SS}) to measure PSRR^+ (PSRR^-). From Eq. (6.4-2) it was shown that

$$\frac{V_{\text{out}}}{V_{dd}} \cong \frac{1}{\text{PSRR}^+} \qquad \text{or} \qquad \frac{V_{\text{out}}}{V_{ss}} \cong \frac{1}{\text{PSSR}^-} \tag{6.6-5}$$

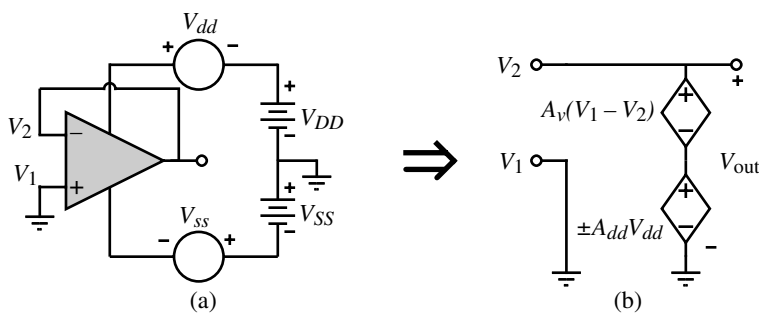

Figure 6.6-9 (a) Configuration for the direct simulation or measurement of PSRR. (b) Model of (a) with $V_{SS} = 0$.

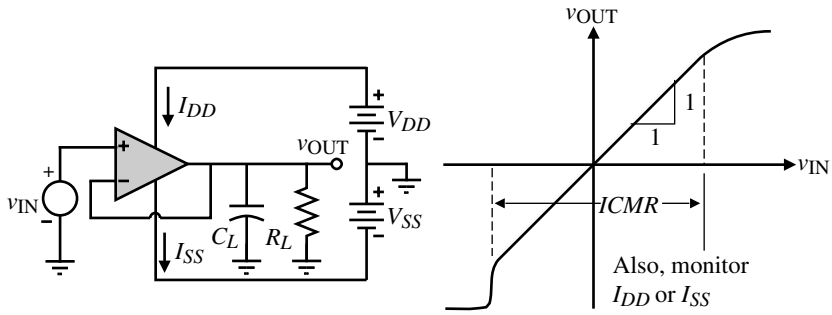

Figure 6.6-10 Measurement of the input common-mode voltage range of an op amp.

This procedure was the method by which PSRR was calculated for the two-stage op amp in Section 6.4. This method works well as long as the CMRR is much greater than 1.

The input and output common-mode voltage range can be defined for both the open-loop and closed-loop modes of the op amp. For the open-loop case, only the output CMR makes sense. One of the configurations of Fig. 6.6-1 or 6.6-3 can be used to measure the output CMR. Typically, the open-loop, output CMR is about half the power-supply range. Because the op amp is normally used in a closed-loop mode, it makes more sense to measure or simulate the input and output CMR for this case. The unity-gain configuration is useful for measuring or simulating the input CMR. Figure 6.6-10 shows the configuration and the anticipated results. The linear part of the transfer curve where the slope is unity corresponds to the input common-mode voltage range. The initial jump in the voltage sweep from negative values of v_{IN} to positive values is due to the turn-on of M5. In the simulation of the input CMR of Fig. 6.6-10, it is also useful to plot the current in M1 because there may be a small range of v_{IN} before M1 begins to conduct after M5 is turned on (e.g., see Fig. 6.6-17).

In the unity-gain configuration, the linearity of the transfer curve is limited by the ICMR. Using a configuration of higher gain, the linear part of the transfer curve corresponds to the output-voltage swing of the amplifier. This is illustrated in Fig. 6.6-11 for an inverting gain of 10 configuration. The amount of current flowing in R_L will have a strong influence on the output-voltage swing and should be selected to represent the actual circumstance.

The output resistance can be measured by connecting a load resistance R_L to the op amp output in the open-loop configuration. The measurement configuration is shown in Fig. 6.6-12.

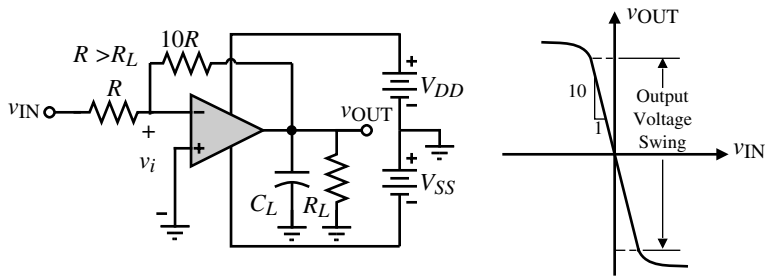

Figure 6.6-11 Measurement of the output-voltage swing.

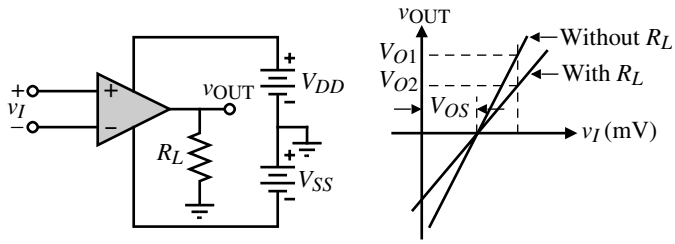

Figure 6.6-12 Measurement of the open-loop output resistance.

The voltage drop caused by R_L at a constant value of v_{IN} can be used to calculate the output resistance as

$$R_{\text{out}} = R_L\left(\frac{V_{O1}}{V_{O2}} - 1\right) \tag{6.6-6}$$

An alternate approach is to vary R_L until $V_{O2} = V_{O1}/2$. Under this condition $R_{\text{out}} = R_L$. If the op amp must be operated in the closed-loop mode, then the effects of the feedback on the measured output resistance must be considered. The best alternative is to use Fig. 6.6-13, where the value of the open-loop gain A_v is already known. In this case, the output resistance is

$$R_{\text{out}} = \left(\frac{1}{R_o} + \frac{1}{100R} + \frac{A_v}{100R_o}\right)^{-1} \cong \frac{100R_o}{A_v} \tag{6.6-7}$$

It is assumed that A_v is in the range of 1000 and that R is greater than R_o. Measuring R_{out} and knowing A_v allows one to calculate the output resistance of the op amp R_o from Eq. (6.6-7). Other schemes for measuring the output impedance of op amps can be found in the literature [15,16].

The configuration of Fig. 6.6-14 is useful for measuring the slew rate and the settling time. Figure 6.6-14 gives the details of the measurement. For best accuracy, the slew rate and settling time should be measured separately. If the input step is sufficiently small (<0.5 V), the output should not slew and the transient response will be a linear response. The settling time can easily be measured. (Appendix D shows how the unity-gain step response can be related to the phase margin, making this configuration a quick method of measuring the phase margin.) If the input step magnitude is sufficiently large, the op amp will slew by virtue of not having enough current to charge or discharge the compensating and/or load capacitances. The slew rate is determined from the slope of the output waveform during the rise or fall of the output. The output loading of the op amp should be present during the settling-time and slew-rate measurements. The unity-gain configuration places the severest requirements on stability and slew rate because its feedback is the largest, resulting in the largest values of loop gain, and should always be used as a worst-case measurement.

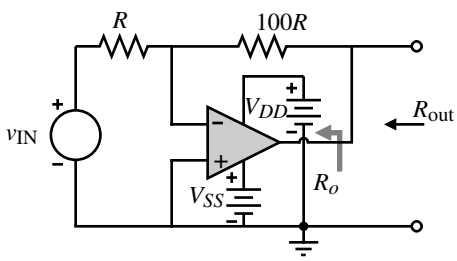

Figure 6.6-13 An alternative method of measuring the open-loop output resistance R_o.

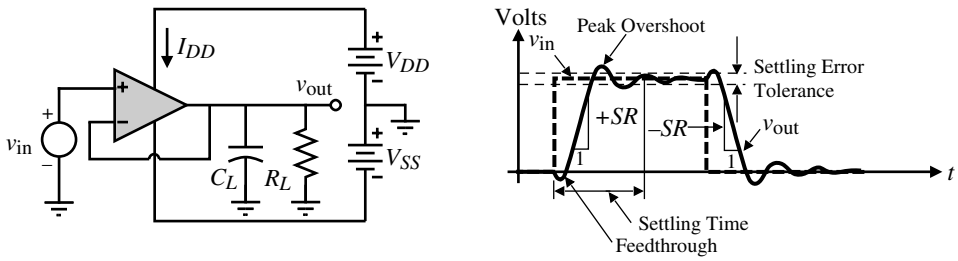

Figure 6.6-14 Measurement of slew rate (*SR*) and settling time.

Other simulations (such as noise, tolerances, process-parameter variations, and temperature) can also be performed. At this point, one could breadboard the op amp. However, if the accuracy of the simulation models is sufficient this step is questionable. An example of using SPICE to simulate a CMOS op amp is given in the following.

Example 6.6-1

Simulation of the CMOS Op Amp of Example 6.3-1

The op amp designed in Example 6.3-1 and shown in Fig. 6.3-3 is to be analyzed by SPICE to determine if the specifications are met. The device parameters to be used are those of Tables 3.1-2 and 3.2-1. In addition to verifying the specifications of Example 6.3-1, we will simulate PSRR^+ and PSRR^-.

SOLUTION

The op amp will be treated as a subcircuit in order to simplify the repeated analyses. Table 6.6-1 gives the SPICE subcircuit description of Fig. 6.3-3. While the values of *AD, AS, PD,* and *PS* could be calculated if the physical layout was complete, we will make an educated estimate of these values by using the following approximations.

$$AS = AD \cong W[L1 + L2 + L3]$$

$$PS = PD \cong 2W + 2[L1 + L2 + L3]$$

where $L1$ is the minimum allowable distance between the polysilicon and a contact in the moat (Rule 5C of Table B-1), $L2$ is the length of a minimum-size square contact to moat (Rule 5A of Table B-1), and $L3$ is the minimum allowable distance between a contact to moat and the edge of the moat (Rule 5D of Table B-1).

The first analysis to be made involves the open-loop configuration of Fig. 6.6-1. A coarse sweep of v_{IN} is made from -5 to $+5$ V to find the value of v_{IN} where the output makes the transition from V_{SS} to V_{DD}. Once the transition range is found, v_{IN} is swept over values that include only the transition region. The result is shown in Fig. 6.6-15. From this data, the value of V_{OS} in Fig. 6.6-1 can be determined. While V_{OS} need not make v_{OUT} exactly zero, it should keep the output in the linear range so that when SPICE calculates the bias point for small-signal analysis, reasonable results are obtained. Since when $v_{\text{IN}} = 0$ V the op amp is still in the linear region, no offset was used to obtain the following open-loop performances.

Table 6.6-1 SPICE Subcircuit Description of Fig. 6.3-3

```
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W = 3U L = 1U AD = 18P AS = 18P PD = 18U PS =
+ 18U
M2 5 1 3 3 NMOS1 W = 3U L = 1U AD = 18P AS = 18P PD = 18U PS =
+ 18U
M3 4 4 8 8 PMOS1 W = 15U L = 1U AD = 90P AS = 90P PD = 42U PS = 42U
M4 5 4 8 8 PMOS1 W = 15U L = 1U AD = 90P AS = 90P PD = 42U PS = 42U
M5 3 7 9 9 NMOS1 W = 4.5U L = 1U AD = 27P AS = 27P PD = 21U PS = 21U
M6 6 5 8 8 PMOS1 W = 94U L = 1U AD = 564P AS = 564P PD = 200U PS = 200U
M7 6 7 9 9 NMOS1 W = 14U L = 1U AD = 84P AS = 84P PD = 40U PS = 40U
M8 7 7 9 9 NMOS1 W = 4.5U L = 1U AD = 27P AS = 27P PD = 21U PS = 21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO = 0.70 KP = 110U GAMMA = 0.4 LAMBDA = 0.04 PHI =
+ 0.7 MJ = 0.5 MJSW = 0.38 CGBO = 700P CGSO = 220P CGDO = 220P CJ
+ = 770U CJSW = 380P LD = 0.016U TOX = 14N
.MODEL PMOS1 PMOS VTO = −0.7 KP = 50U GAMMA = 0.57 LAMBDA = 0.05 PHI
+ = 0.8 MJ = 0.5 MJSW = .35 CGBO = 700P CGSO = 220P CGDO = 220P CJ
+ = 560U CJSW = 350P LD = 0.014U TOX = 14N
IBIAS 8 7 30U
.ENDS
```

At this point, the designer is ready to begin the actual simulation of the op amp. In the open-loop configuration the voltage-transfer curve, the frequency response, the small-signal gain, and input and output resistances can be simulated. The SPICE input deck using the PC version of SPICE (PSPICE) is shown in Table 6.6-2. Figure 6.6-16 shows the results of this simulation. The open-loop voltage gain is 10,530 V/V (determined from the output file), *GB* is 5 MHz, output resistance is 122.5 kΩ (determined from the output file), power dissipation is 0.806 mW (determined from the output file), phase margin for a 10 pF load is 65°, and the open-loop output-voltage swing is +2.3 to −2.2 V. The simulation results compare well with the original specifications.

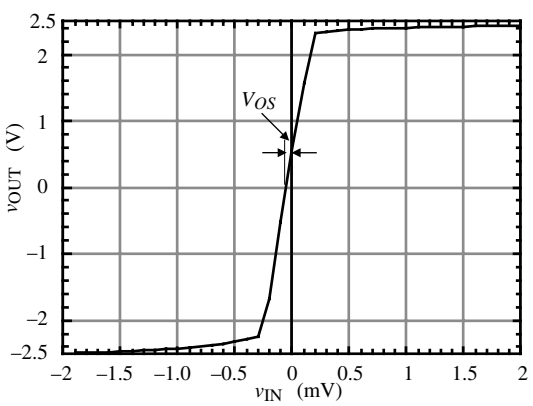

Figure 6.6-15 Open-loop transfer characteristic of Example 6.6-1 illustrating V_{OS}.

Table 6.6-2 PSPICE Input File for the Open-Loop Configuration

```
EXAMPLE 6.6-1 OPEN LOOP CONFIGURATION
.OPTION LIMPTS = 1000
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 2.5
VSS 0 5 DC 2.5
VIN − 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
        .
        .
        .
(Subcircuit of Table 6.6-1)
        .
        .
        .
.OP
.TF V(3) VIN+
.DC VIN+ −0.005 0.005 100U
.PRINT DC V(3)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE (This entry is unique to PSPICE)
.END
```

The next configuration is the unity-gain configuration of Fig. 6.6-10. From this configuration, the ICMR, $PSRR^+$, $PSRR^-$, slew rate, and settling time can be determined. Table 6.6-3 gives the SPICE input file to accomplish this ($PSRR^+$ and $PSRR^-$ must be done on separate runs). The results of this simulation are shown in the following figures. The ICMR is -1.2 to $+2.3$ V as seen on Fig. 6.6-17. Note that the lower limit of the ICMR is determined by when

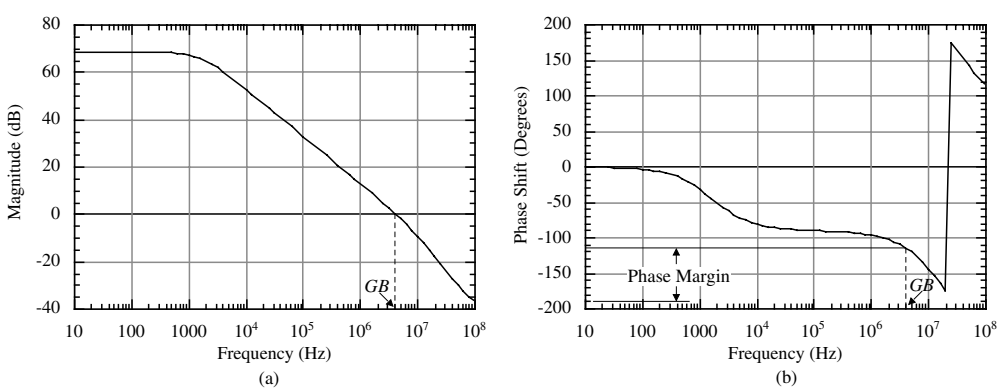

Figure 6.6-16 (a) Open-loop transfer function magnitude response of Example 6.6-1. (b) Open-loop transfer function phase response of Example 6.6-1.

TABLE 6.6-3 Input File for the Unity-Gain Configuration

```
EXAMPLE 6.6-1 UNITY GAIN CONFIGURATION.
.OPTION LIMPTS = 501
VIN+ 1 0 PWL(0 −2 10N −2 20N 2 2U 2 2.01U −2 4U −2
+4.01U −.1 6U −.1 6.01U .1 8U .1 8.01U −.1 10U −.1)
VDD 4 0 DC 2.5 AC 1.0
VSS 0 5 DC 2.5
CL 3 0 20P
X1 1 3 3 4 5 OPAMP
  .
  .
  .
(Subcircuit of Table 6.6-1)
  .
  .
  .
.DC VIN+ −2.5 2.5 0.1
.PRINT DC V(3)
.TRAN 0.05U 10U 0 10N
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE (This entry is unique to PSPICE)
.END
```

the current in M5 reaches its quiescent value. $PSRR^+$ is shown in Fig. 6.6-18 and $PSRR^-$ is shown in Fig. 6.6-19.

The large-signal and small-signal transient responses were made by applying a 4 V pulse and a 0.2 V pulse to the unity-gain configuration. The results are illustrated in Fig. 6.6-20. From these data the positive slew rate is seen to be 10 V/μs but the negative slew rate is closer to −6.7 V/μs and has a large negative overshoot. The reason for the poorer negative slew rate is due to the limited current available to discharge the 10 pF load capacitance. At a slew rate of −6.7 V/μs, the current through the compensating capacitor, C_c, is about 20 μA.

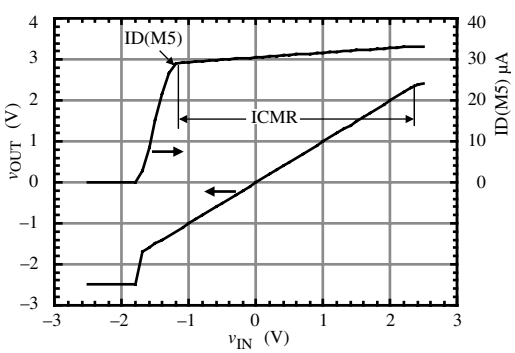

Figure 6.6-17 Input common-mode simulation of Example 6.6-1.

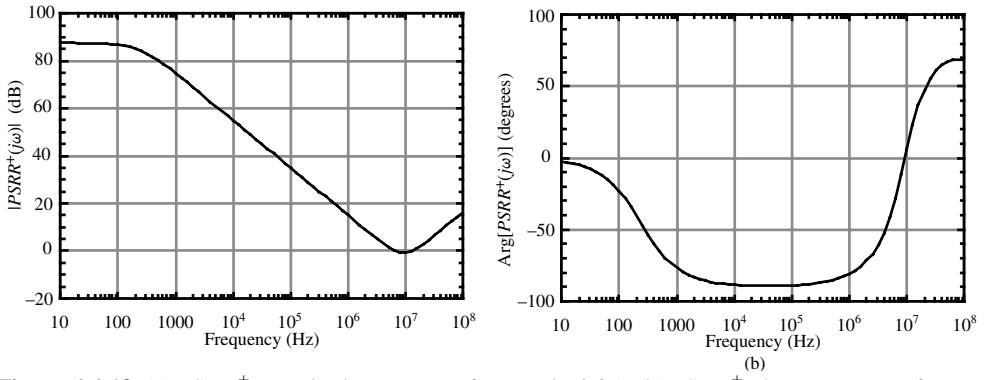

Figure 6.6-18 (a) PSRR$^+$ magnitude response of Example 6.6-1. (b) PSRR$^+$ phase response of Example 6.6-1.

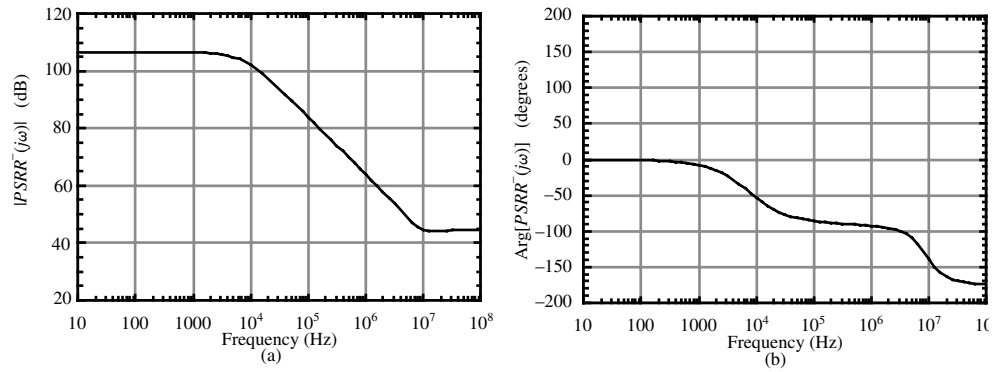

Figure 6.6-19 (a) PSRR$^-$ magnitude response of Example 6.6-1. (b) PSRR$^-$ phase response of Example 6.6-1.

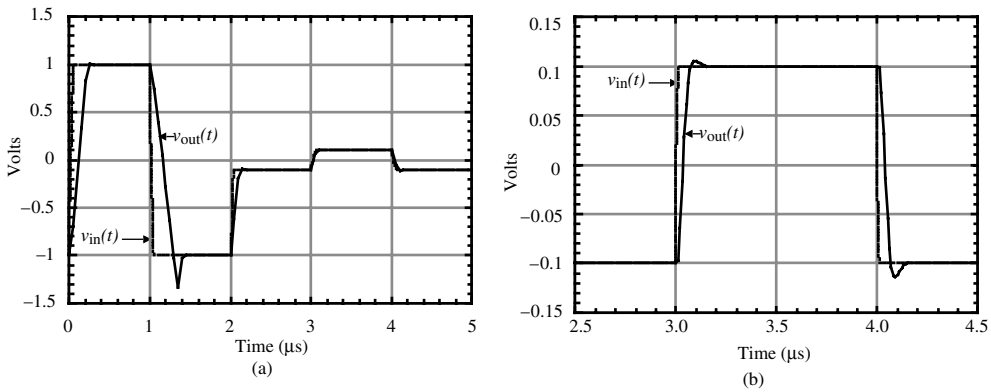

Figure 6.6-20 (a) Unity-gain transient response of Example 6.6-1. (b) Unity-gain, small-signal transient response of Example 6.6-1.

Therefore, the current remaining to discharge the load capacitor is 95 μA minus 20 μA or 70 μA. Thus, the slew rate of the negative transition is limited by the load capacitance rather than the compensation capacitance and is about −7 V/μs. This could easily be solved by increasing the bias current in the output stage from 95 μA to 130 μA (30 μA for C_c and 100 μA for C_L).

The large overshoot on the negative slew is due to the fact that there is no current in M6 because all of the 95 μA from M7 is being used to discharge capacitances C_c and C_L and none is left to flow through M6. On the positive slew, M6 can provide whatever current is needed so it can respond immediately to changes. However, the negative slew continues past the final point until the output stage can respond accordingly through the unity-gain feedback network.

The overshoot is seen to be very small. The settling time to within ±5% is approximately 0.5 μs as determined from the output file. The relatively large-value compensation capacitor is preventing the 10 pF load from causing significant ringing in the transient response. An interesting question that is pursued further in Problem 6.6-11 is why the negative overshoot is greater than the positive overshoot. Slewing is no longer a concern because the op amp is operating in the linear mode.

The specifications resulting from this simulation are compared to the design specifications in Table 6.6-4. It is seen that the design is almost satisfactory. Slight adjustments can be made in the *W/L* ratios or dc currents to bring the amplifier within the specified range. The next step in simulation would be to vary the values of the model parameters, typically K', V_T, γ, and λ, to ensure that the specifications are met even if the process varies.

TABLE 6.6-4 Comparison of the Simulation with Specifications of Example 6.3-1

Specification (Power supply = ±2.5 V)	Design (Example 6.3-1)	Simulation (Example 6.6-1)
Open-loop gain	>5000	10,000
GB (MHz)	5 MHz	5 MHz
ICMR (volts)	−1 to 2 V	+2.4 V, −1.2 V
Slew rate (V/μs)	>10 (V/μs)	+10, −7 (V/μs)
P_{diss} (mW)	<2 mW	0.625 mW
V_{out} range (V)	±2 V	+2.3 V, −2.2 V
$PSRR^+$ (0) (dB)	—	87
$PSRR^-$ (0) (dB)	—	106
Phase margin (degrees)	60°	65°
Output resistance (kΩ)	—	122.5 kΩ

The measurement schemes of this section will work reasonably well as long as the open-loop gain is not large. If the gain should be large, techniques applicable to bipolar op amps must be employed. A test circuit for the automatic measurement of integrated-circuit op amps in the frequency domain has been developed and described [17]. This method supplements the approaches given in this section. Data books, websites, and technical literature are also good sources of information on this topic.

6.7 Summary

This chapter has presented the design, simulation, and measurement considerations of unbuffered CMOS op amps. The general approach to designing op amps concentrates first on establishing dc conditions that are process insensitive. This results in defining some of the ratios of the devices and establishing constraints between the device ratios. Next, the ac performance is achieved by selecting dc current levels and the remaining device ratios. Constraints are then developed in order to achieve satisfactory frequency response. This procedure for designing simple CMOS op amps was seen to be reasonably straightforward, and a design procedure was developed for the two-stage CMOS op amp that ensures a first-cut design for most specifications.

One important aspect of the op amp is its stability characteristics, which are specified by the phase margin. Several compensation procedures that allow the designer to achieve reasonably good phase margins even with large capacitive loads were discussed. The stability of the op amp was also important in the settling time of the pulse response. The Miller compensation method of pole splitting, used together with a nulling resistor to eliminate the effects of the RHP zero, was found to be satisfactory.

The design of the CMOS op amp given in Sections 6.3 and 6.4 resulted in a first-cut design for a two-stage op amp or a cascode op amp. The two-stage op amp was seen to give satisfactory performance for most typical applications. The cascode configuration of Section 6.3 was used to improve the performance of the two-stage op amp in the areas of gain, stability, and PSRR. If all internal nodes of an op amp are low impedance, compensation can be accomplished by a shunt capacitance to ground at the output. This configuration is self-compensating for large capacitive loads. Although the output resistance of the cascode op amp was generally large, this is not a problem if the op amp is to drive capacitive loads.

Sections 6.3 and 6.4 show how the designer can obtain the approximate values for the performance of the op amp. However, it is necessary to simulate the performance of the CMOS op amp to refine the design and to check to make sure no errors were made in the design. Refining the design also means varying the process parameters in order to make sure the op amp still meets its specifications under given process variations. Finally, it is necessary to be able to measure the performance of the op amp when it is fabricated. So, techniques of simulation and measurement applicable to the CMOS op amp were presented.

This chapter has presented the principles and procedures by which the reader can design op amps for applications not requiring low output resistance. This information serves as the basis for improving the performance of op amps, the topic to be considered in the next chapter.

Problems

6.1-1. Use the null port concept to find the voltage-transfer function of the noninverting voltage amplifier shown in Fig. P6.1-1.

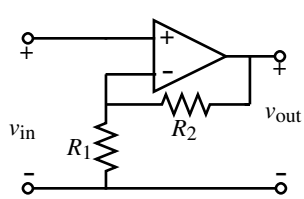

Figure P6.1-1

6.1-2. Show that if the voltage gain of an op amp approaches infinity, the differential input becomes a null port. Assume that the output is returned to the input by means of negative feedback.

6.1-3. Show that the controlled source of Fig. 6.1-5 designated as v_1/CMRR is in fact a suitable model for the common-mode behavior of the op amp.