Low Drop-out Voltage Regulators with SKY130PDK

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Acknowledgement:

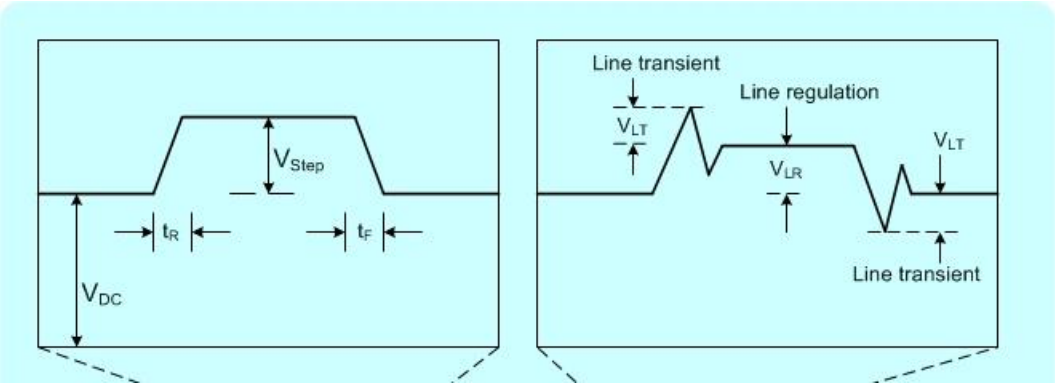
- I’m grateful to the constant mentoring and support of Manjunath Kareppagoudar and Soumya Kanta Rana.
- I’m thankful to Ahmed Tawfiq for the help on Ngspice and Xschem software, it simplified much of my work .
- This project wouldn’t have been possible without all the help I got.

Linear Regulators

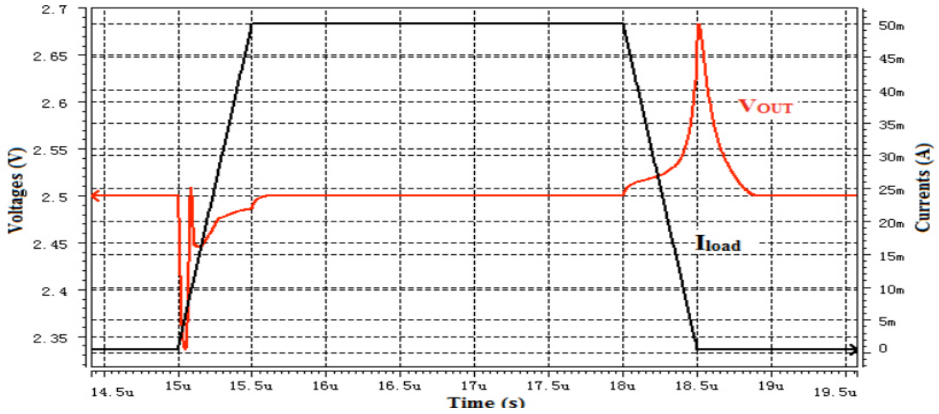
- Regulations is achieved by dropping voltage
- Switches are in saturation region.
- Higher losses and low efficiency when dropout is high.
- We select linear regulators when there is a need of small voltage drop.
- Efficiency is inversely proportional to Voltage drop.
- LDO have less noise , so they are preferred for RF sensors and others.

Important Concepts:

- Line transient and Load transient.
- Concept of negative feedback and why is it necessary ???
- Second order system.
- Why pole splitting is required???
- Why do we need a phase margin of 60degree or greater???
- How to stabilize a system ???
- How to analyze the stability ??
- How to get poles and decide which is significant and which is not (dominant and non dominant poles) ???
- Types of Compensation employed.



Line transient



Load transient

Specifications:

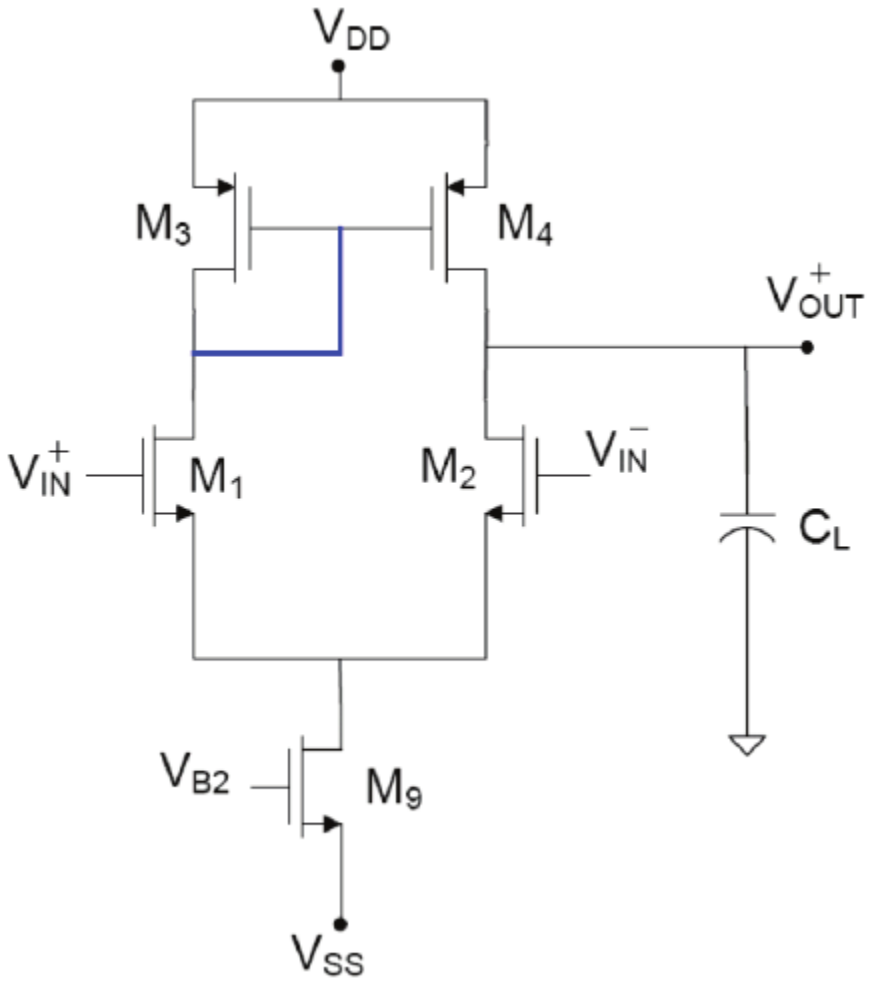
Specifications (V_{out} = 1.35V, Load capacitor=0.1nF, and Full load=40mA):

Specs	Description	Value
V_{IN}(max)	Maximum input voltage range	3V
V_{IN}(min)	Minimum input voltage range	1.5V
V_{DO}	Dropout voltage for 40mA load current (error loop gain = 20dB)	150mV
I_Q	Quiescent current (no load current) (V_{in} = 3V)	≤ 50 µA
t_{Set}(Load)	Average of settling time to ±1% of final value of 20mA to 40mA and 40mA to 20mA load changes (100ns rise and fall time)	≤ 1µs
t_{Set}(Line)	Average of settling time to ±1% of final value for ΔV_{IN} from 2V to 3V and 3V to 2V for 10mA load (100ns rise and fall time)	≤ 2µs
PSRR	Magnitude of power supply rejection (v_{out}/v_{in}) at 100Hz (10mA)	≥ 60dB
I_{SC}	Short circuit current with a 10Ω load resistor (V_{in} = 3V)	≤50mA
PM	Phase margin of main feedback loop (10mA)	≥ 60°
η	Efficiency for full load and V_{IN} =1. 5V	≥ 90%
WC^+ V_{out}	Max V_O with 10mA load (V_{in} = 1.5-3V, -40°C≤*T*≤125°C, Process)	≤ 1.36V
WC^- V_{out}	Min V_O with 10mA load (V_{in} = 1.5-3V, -40°C≤*T*≤125°C, Process)	≥ 1.34V

Credits: Soumya Kanta rana, Analog Engineer (Texas Instruments)

Error Amplifier

- Here I've used a simple differential amplifier because If we use a single stage Error Amplifier, We will handle less poles as a whole and the design will be easy for us.
- The design of the Error amplifier must be robust and good so that the regulated output voltage doesn't deviate more than 5% of the specified Vreg.
- Should provide a good gain and have a good PSRR.



Design

- This is a linear regulator so all the Mosfets operate in saturation region.

Design of Error Amplifier:

- The Aspect ratio of Differential Pair:
- gm1 is the one that contributes to the gain and bandwidth of the error amplifier so
- gm1,2 = 2pi(GBW*CL)

$$\frac{W}{L} \cdot 1,2 = \frac{g_{m1}^2}{\mu_n C_{ox} \cdot 2I_1}$$

- The Aspect ratio of the Current Mirror:
- Before finding the W/L3,4 we need to find the Vt max of current mirrors and Vtnmax , Vtnmin of Differential pairs
- For Simplicity I've used the mosfet nfet_01v8_lvt and pfet_01v8_lvt whose Vt doesn't change much unlike nfet_01v8 and pfet_01v8.
- Vsg3=Vdd-Icmr(+)+Vtn1min

$$W/L \cdot 3.4 = 2I_3/\mu_p C_{ox}(V_{sg3} - V_{tpmax})^2$$

- The aspect ratio of the biasing mosfets:

$$V_{dsat5} = I_{crm}^{-} - \sqrt{\frac{I_5}{\beta}} - V_{tnmin}$$

$$\frac{W}{L}_{5,6} = \frac{2I_5}{\mu_n C_{ox} \cdot V_{dsat5}^2}$$

- Aspect ratio of the Pass Transistor:
- Pass transistors are typically PowerFETs which are large in width.
- From the specifications we know that Vdrop=150mV, so Vsd of Mpass is 150mV, so I targeted an overdrive voltage of 100mV.
- (W/L)pass=2IL/upCoxVov^2
- From this for IL of 40mA I got a W/L ratio of 145454.5
- (W/L)pass = 145455
- Here I used pfet_01v8 because of all the parasitic capacitance the gate cap will be quite large and can have an effect on the stability and add over miller cap, So I designed the error amp for a CL=50pF, the Mosfet pfet_01v8 offers the least Cgg (approx 20pF).

Design Concessions I made

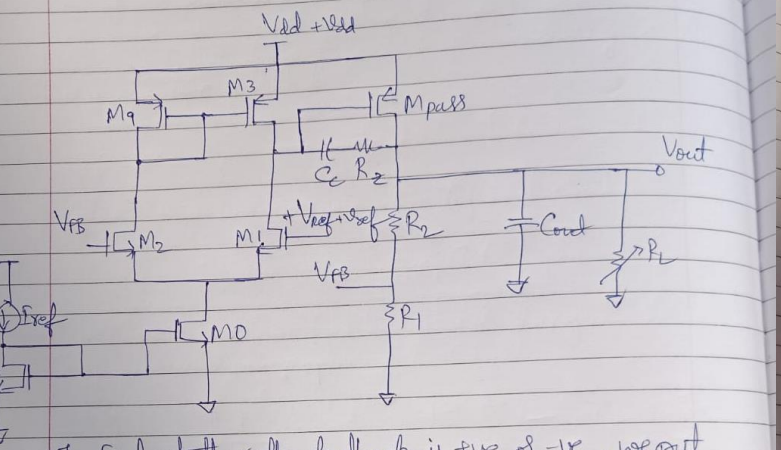
- I chose a bias current of 50uA because the specification needed a settling time of 1us which will be very much affected if we decrease Slew rate but the quiescent current (IQ) should be less than 50uA.
- Only way to not hamper the settling time was to choose a good Slew-Rate, the only solution to do that was burn more current as I cannot change the load cap.
- This has an affect of increasing the quiescent current (IQ) to more than 50uA, the final result showed a IQ of around 100uA, this cannot be avoided because of the PDK.

Intuitive Analysis of poles and Zeros

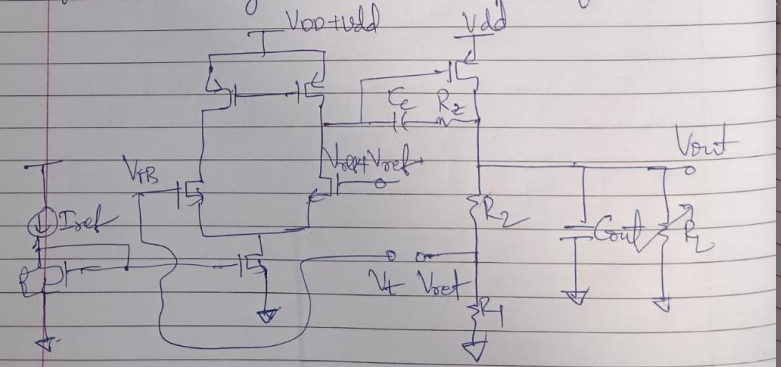
Credits: Anuit Sar

25/04/23

Finding Poles and Zero of LDO Intuitively



→ To find whether the feedback is +ve or -ve, we put a huge impedance node at the feedback and apply small signal Vtest and cover the loop and check what's coming back at the other part of node

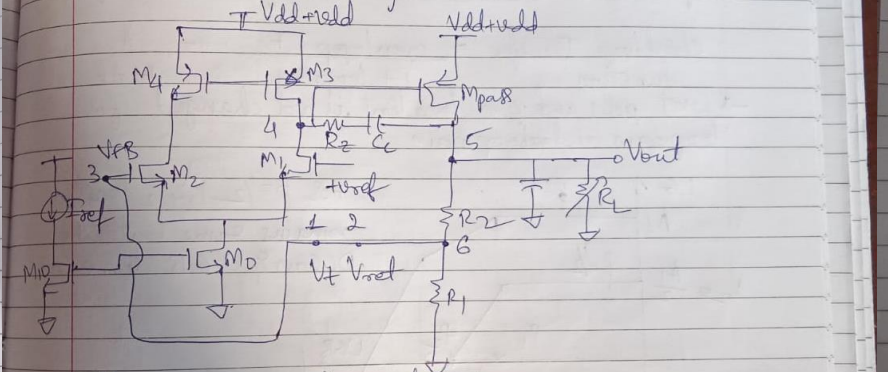


Find loop gain = $\frac{V_{ret}}{V_{test}}$ is negative

loop gain = $\frac{V_{ret}}{V_{test}} < 0$ [negative] so -ve feedback

~~loop gain~~ =

Now lets do it Intuitively.



If we increase voltage at V_t

→ For M_2, if we increase gate voltage, small signal source voltage will increase, so the source of M_1 voltage also Increases

→ If we increase source of M_1, drain of M_1 also increases bcs it becomes common gate config

→ So Voltage at Node 5 also increases

→ then gate voltage of PMOS Mpass increases the drain voltage decrease bcs its common source config of PMOS

→ then node 5 voltage decreases the combo of R_2 & R_1 becomes voltage divider, then voltage at node 6

U.G.B → Unity Gain Bandwidth.

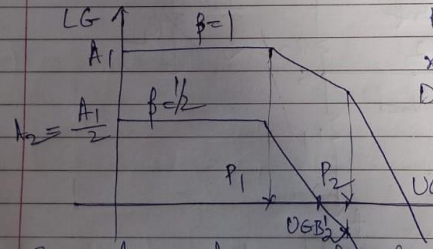
→ Voltage decreases then voltage at node 2 also decreases. So when we increase voltage at node 1 after travelling the nodes, the voltage at node 2 is decreasing. So this is a negative feedback

[LG] Loop Gain: [open loop gain x feedback factor] [Aβ]

→ If we know L.G we can directly find closed loop behavior

Closed loop Transfer function = $\frac{\text{open loop T.F}}{1 + \text{loop Gain}} = \frac{A}{1+A\beta}$

→ WKT poles and zero location is not changed for loop gain and ~~close~~ loop gain



For $\beta = 1/2$ P_1 & P_2 location remains same but the DC Gain & U.G.B decreases

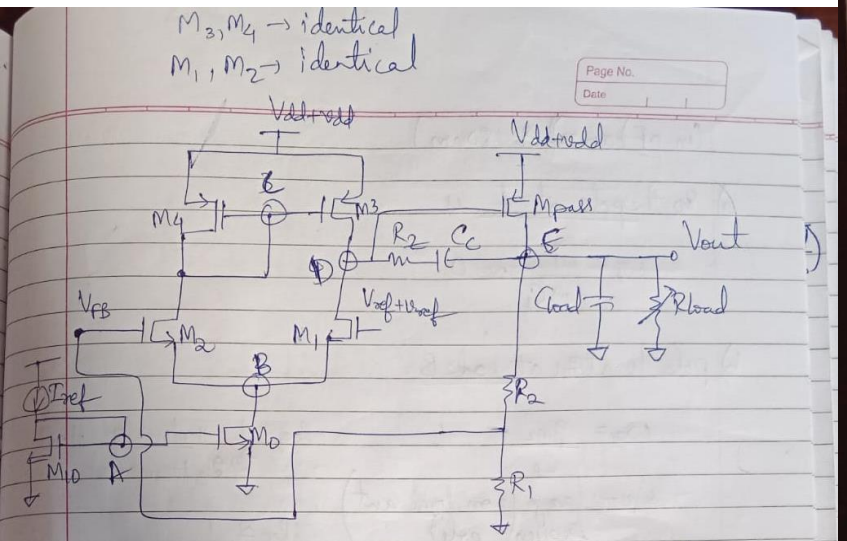
→ Even if we decrease β poles and zero locations are unchanged but DC Gain U.G.B is decreased

$A_2 = \frac{A_1}{2}$ & $UGB_2 = \frac{UGB_1}{2}$ [for $\beta = 1/2$]

→ WKT every ~~loop~~ node containing a pole

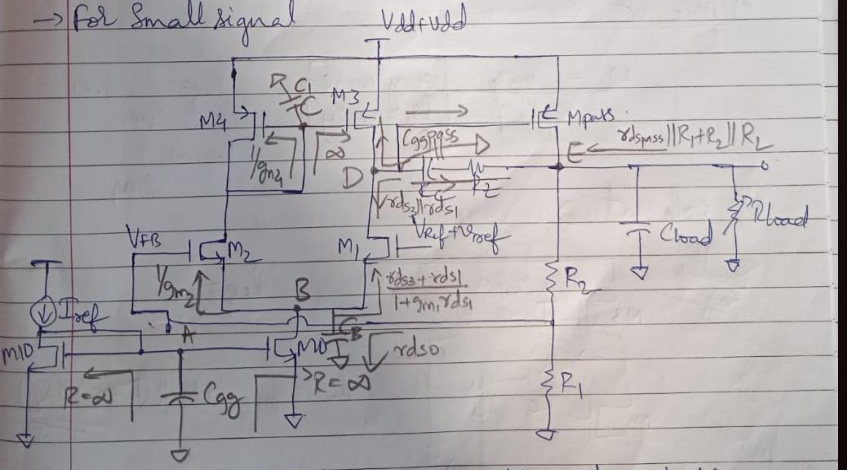
$M_3, M_4 \rightarrow$ identical

$M_1, M_2 \rightarrow$ identical



→ There are 5 nodes so there can be max 5 poles

→ For Small signal



→ For small signal I_{ref} = open ckt and R looking at M_{10} & M_0 are ∞ and also C_{gg} of M_{10} & M_0 is present (gate to ground capacitance) which is large.

(in pF range for 180nm)

a) So the pole at A is

$$\omega_A = \frac{1}{(\infty) C_A} \simeq 0$$

b) pole location at node B

$$\omega_B = \frac{g_{m2}}{C_B}$$

$\omega_B \rightarrow$ large frequency (non dominant pole)

C_B

$$R_{eq} = \frac{1}{g_{m2}} \| \frac{r_{ds3}+r_{ds1}}{1+g_m r_{ds1}} \| r_{ds0}$$ very high

$$R_{eq} \simeq \frac{1}{g_{m4}}$$

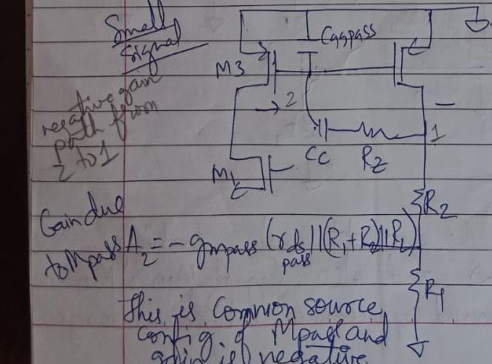
c) pole at C

$$\omega_c = \frac{g_{m4}}{C_1}$$ [very large frequency]

$$R_{eq} = \frac{1}{g_{m4}} \| \infty$$

$$R_{eq} \simeq \frac{1}{g_{m4}}$$

D) pole at D

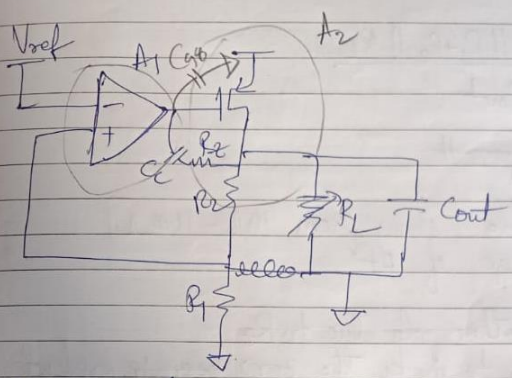


R_{eq} =

$A_2 = -g_{mpass}(r_{ds_{pass}} \| (R_1+R_2) \| R_L)$

Gain due to Mpass $A_2 = -g_{mpass}(r_{ds_{pass}} \| (R_1+R_2) \| R_L)$

This is common source config of Mpass and gain is negative



→ A_2 is negative gain so the C_c experience Miller effect, so C_c is miller cap

$$C_{eq_D} = C_{gg} + C_c(A_2+1)$$

$$\omega_D = \frac{1}{(r_{ds3} \| r_{ds1})(C_{gg} + C_c(A_2+1))}$$

large Impedance

large Capacitance

So ω_D becomes lower frequency

WKT

$$A_1 = g_{m1}(r_{ds3} \| r_{ds1})$$

$$A_2 = -g_{mpass}(r_{ds_{pass}} \| (R_1+R_2) \| R_L)$$

E) pole at node E

$$R_{eq_E} = r_{ds_{pass}} \| (R_1+R_2) \| R_L$$

$$C_{eq_E} = C_{out}$$

$$\omega_c = \frac{r_{dspass} \parallel R_1 + R_2 \parallel R_L}{C_{out}}$$

~~$R_{eq} = r_{dspass} \parallel$~~

R_L is variable [vary from 10Ω – 10MΩ]
C_{out} in range of pf

→ There is another pole due to R_2
→ we added R_2 to make the zero ~~because~~ present because of the ~~bypass~~ C_c. To nullify zero present in left we add R_2

pole due to R_2

$$R_{eq} = R_2, \quad C_{eq} = \left(\frac{1}{C_c} + \frac{1}{C_{gg}} + \frac{1}{C_{out}}\right)$$

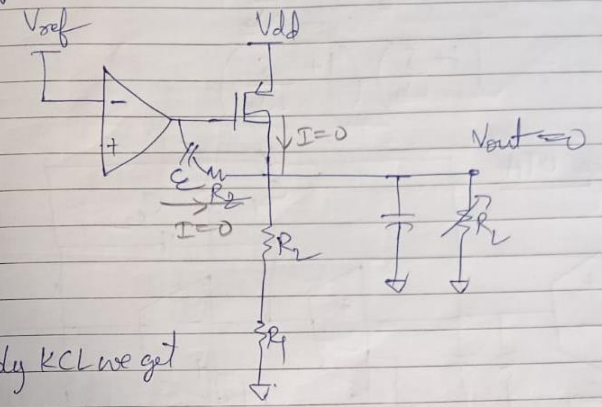
$$P_{R_2} = \frac{1}{R_2 \times \left(\frac{1}{C_c} + \frac{1}{C_{gg}} + \frac{1}{C_{out}}\right)}$$

This P_{R_2} is very high frequency.

So there are total 6 poles and 1 zero

→ To find zero, for input = zero, output = 0

To find zero



Apply KCL we get

$$\omega_z = \frac{1}{\left(\frac{1}{g_{mpass}} - R_2\right) C_c}$$

→ If we make $R_2 > \frac{1}{g_{mpass}}$ then ω_z comes in Left half plane

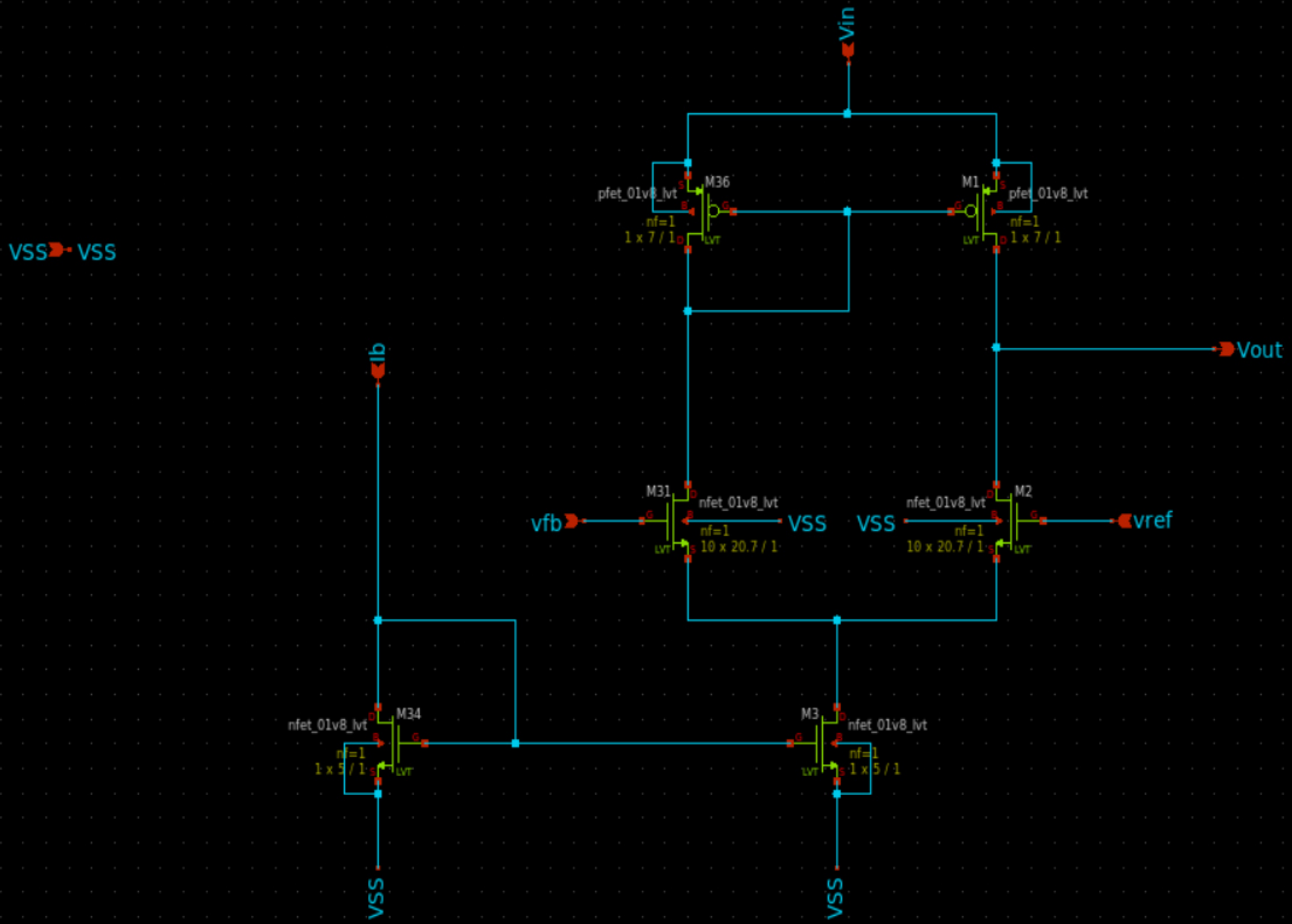
→ So we nullify the effect of RHP [because RHP zero is phase lagging]

→ pole at A the node will not be coming at signal path (V_{out} path) (bcs its bias path). So pole at A is not an important pole
→ So we get effective pole 2, one due to R_2 and other at the output
→ So 2 effective pole (ω_z, ω_c)
- ω_z → dominant pole
- ω_c → non dominant pole

one zero (ω_z)

$$\text{Loop Gain}(S) = \frac{(-A_1 A_2) \times \left(1 - \frac{S}{\omega_z}\right)}{\left(1 + \frac{S}{\omega_D}\right)\left(1 + \frac{S}{\omega_c}\right)}$$

Error Amplifier Schematics



Spec Achieved:
(W/L)1,2 = 207
(W/L)3,4 = 7
(W/L)5,8 = 5
Gain : 37dB
GBW: 7MHz
Ibias: 50uA
Slew Rate: 1V/usec
VDD: 1.5V
ICMR+: 1.2V
ICMR-: 0.9V
CL: 50pF

XSCHEM

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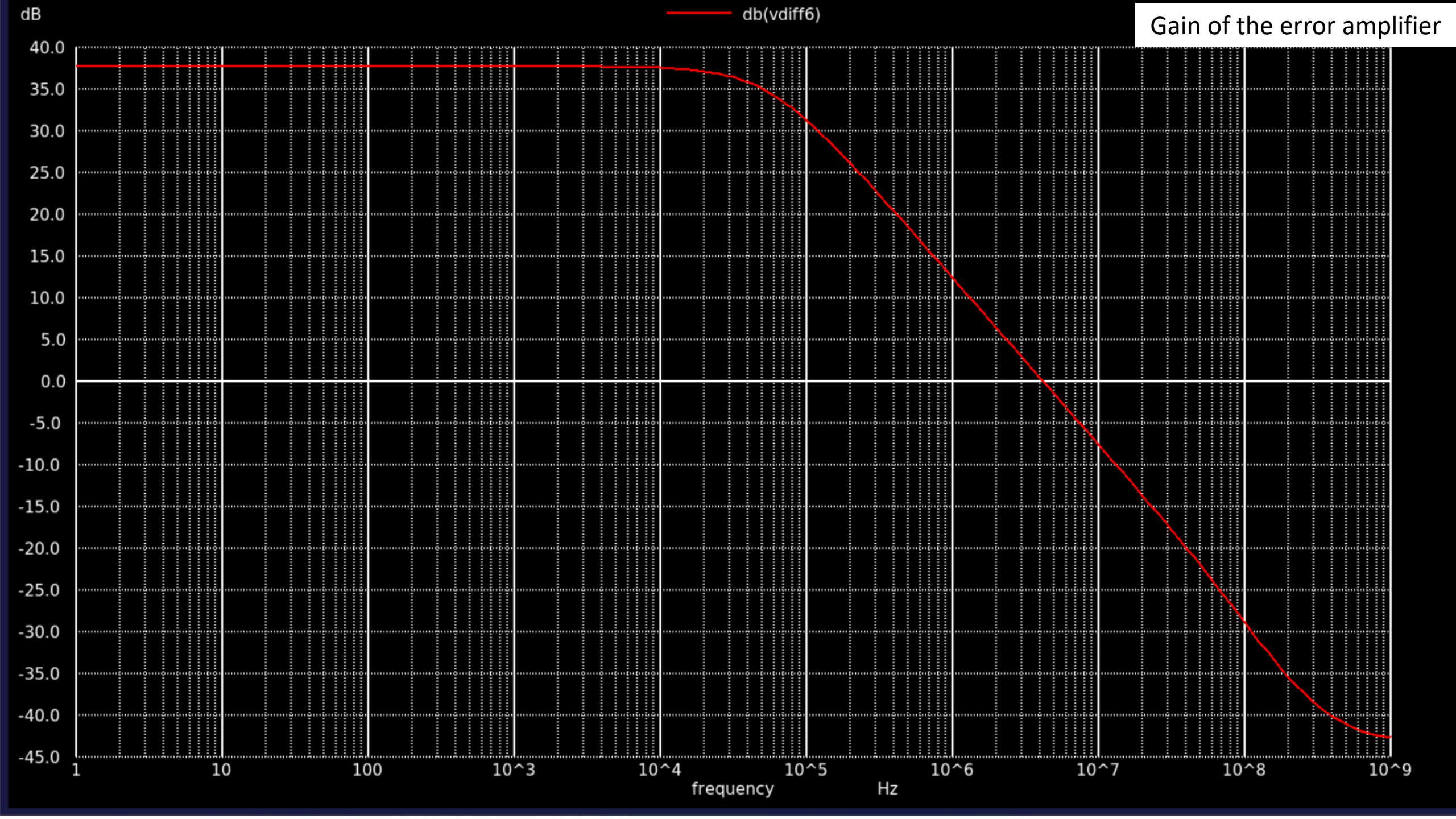
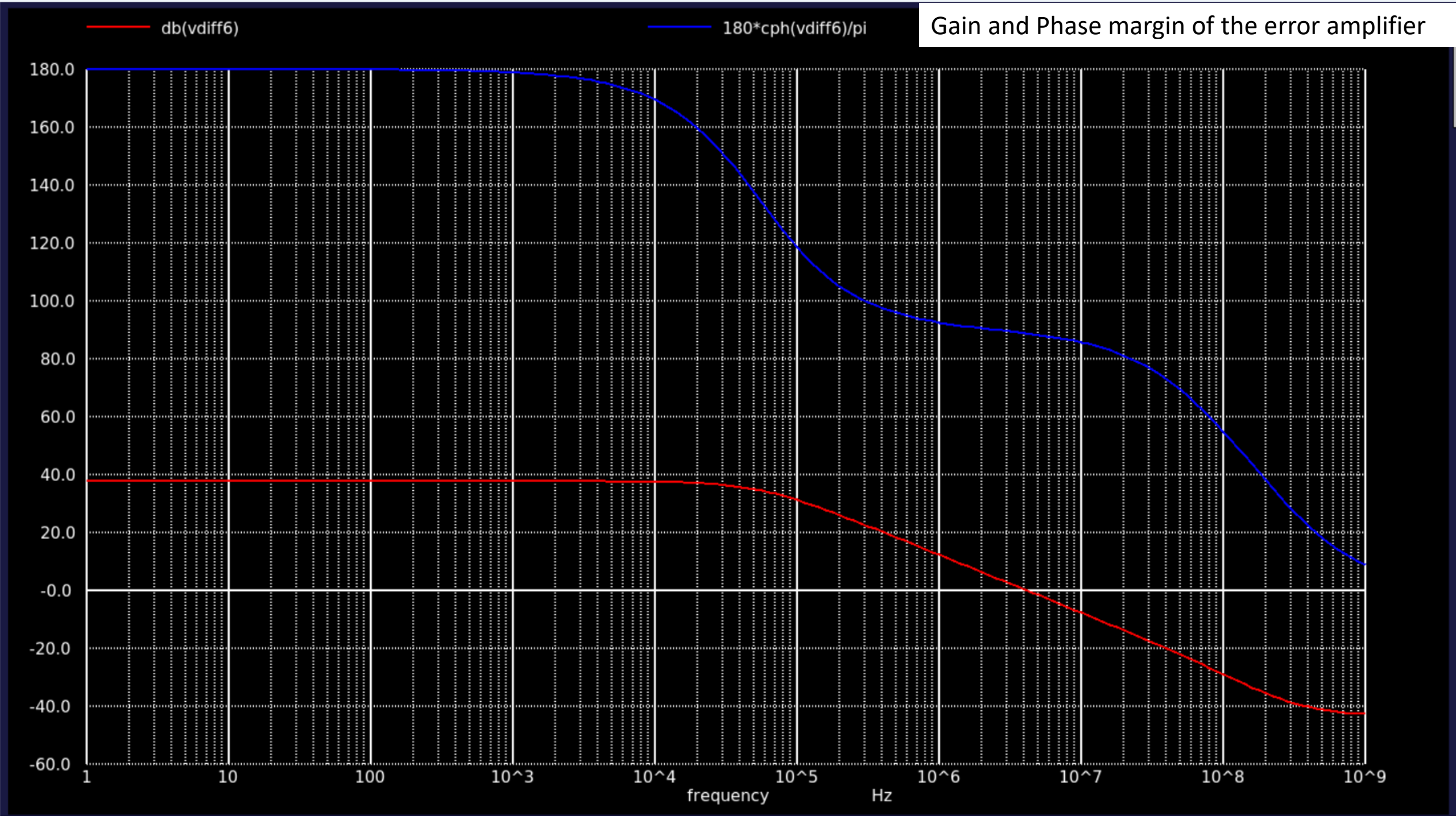
Gain of the error amplifier



Gain and Phase margin of the error amplifier



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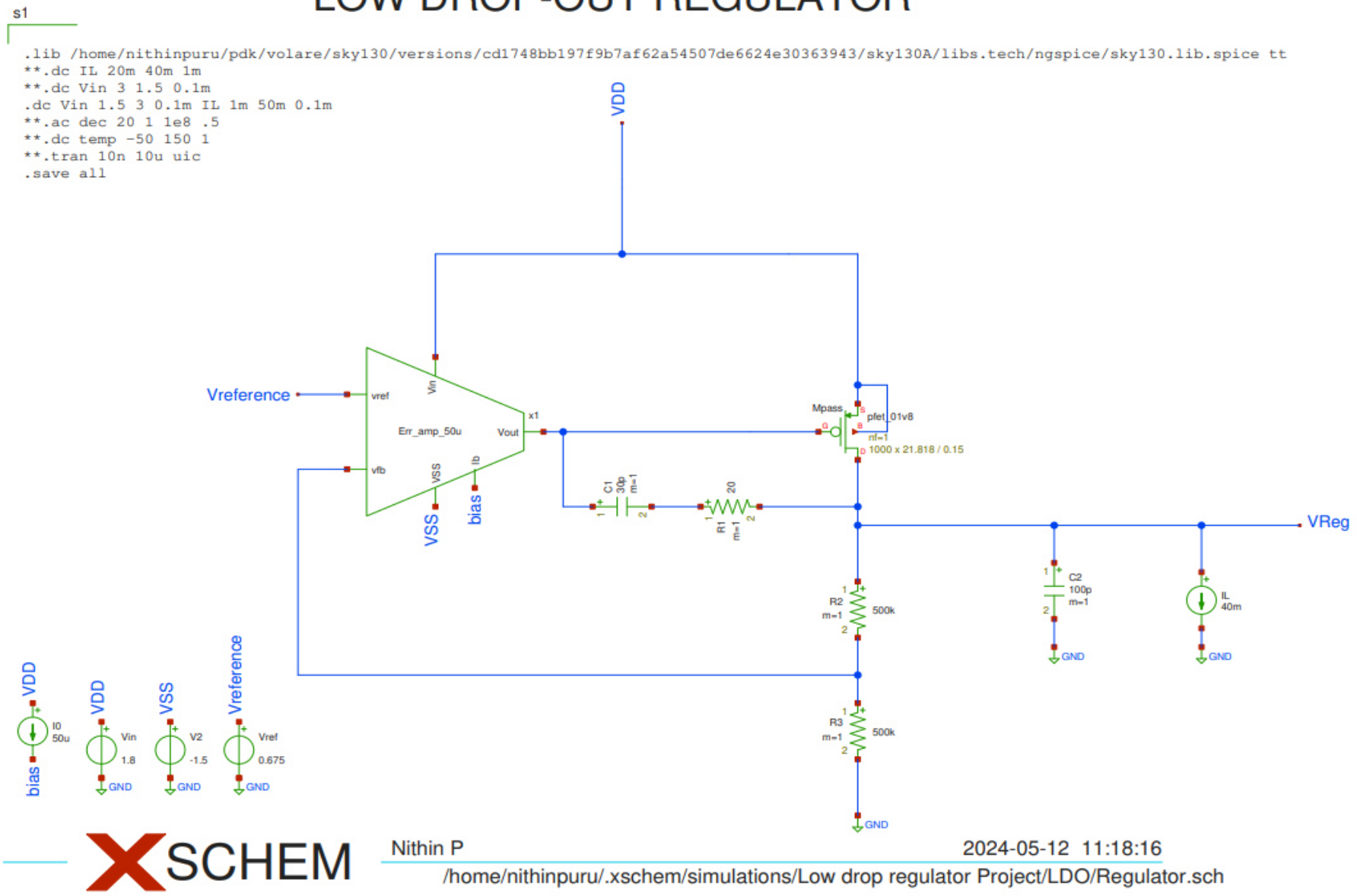
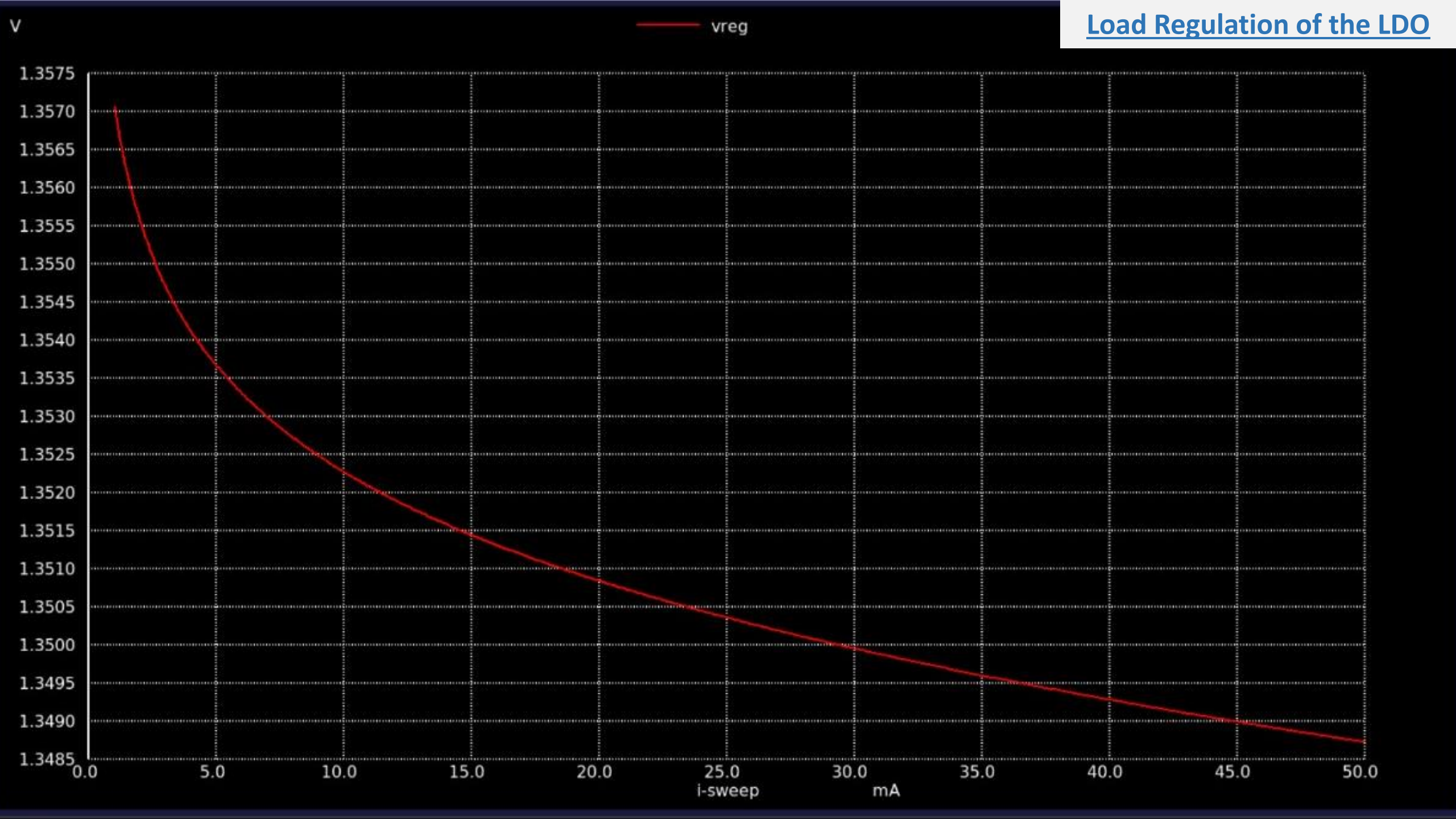
LOW DROP-OUT REGULATOR

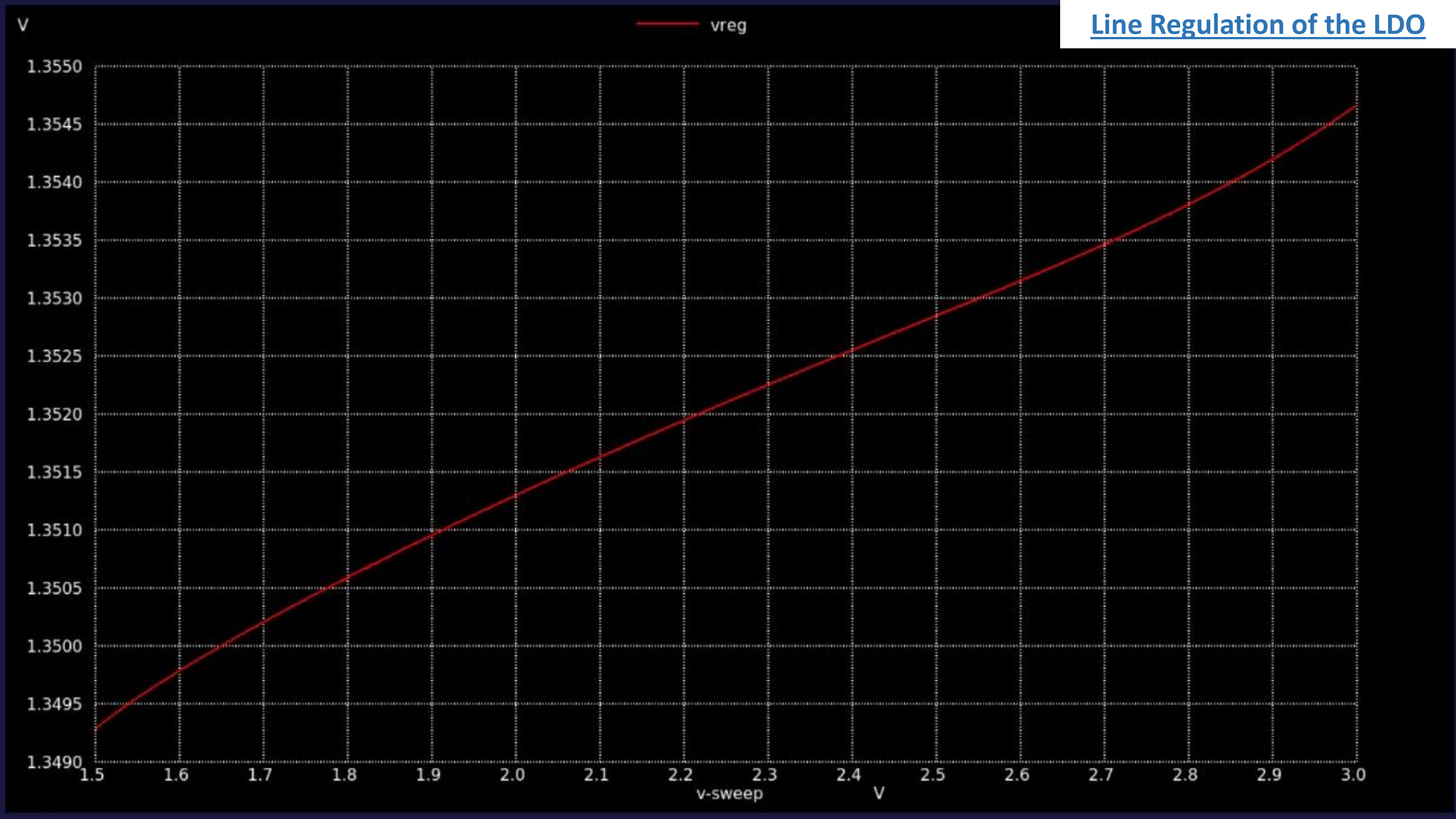


LDO Schematics

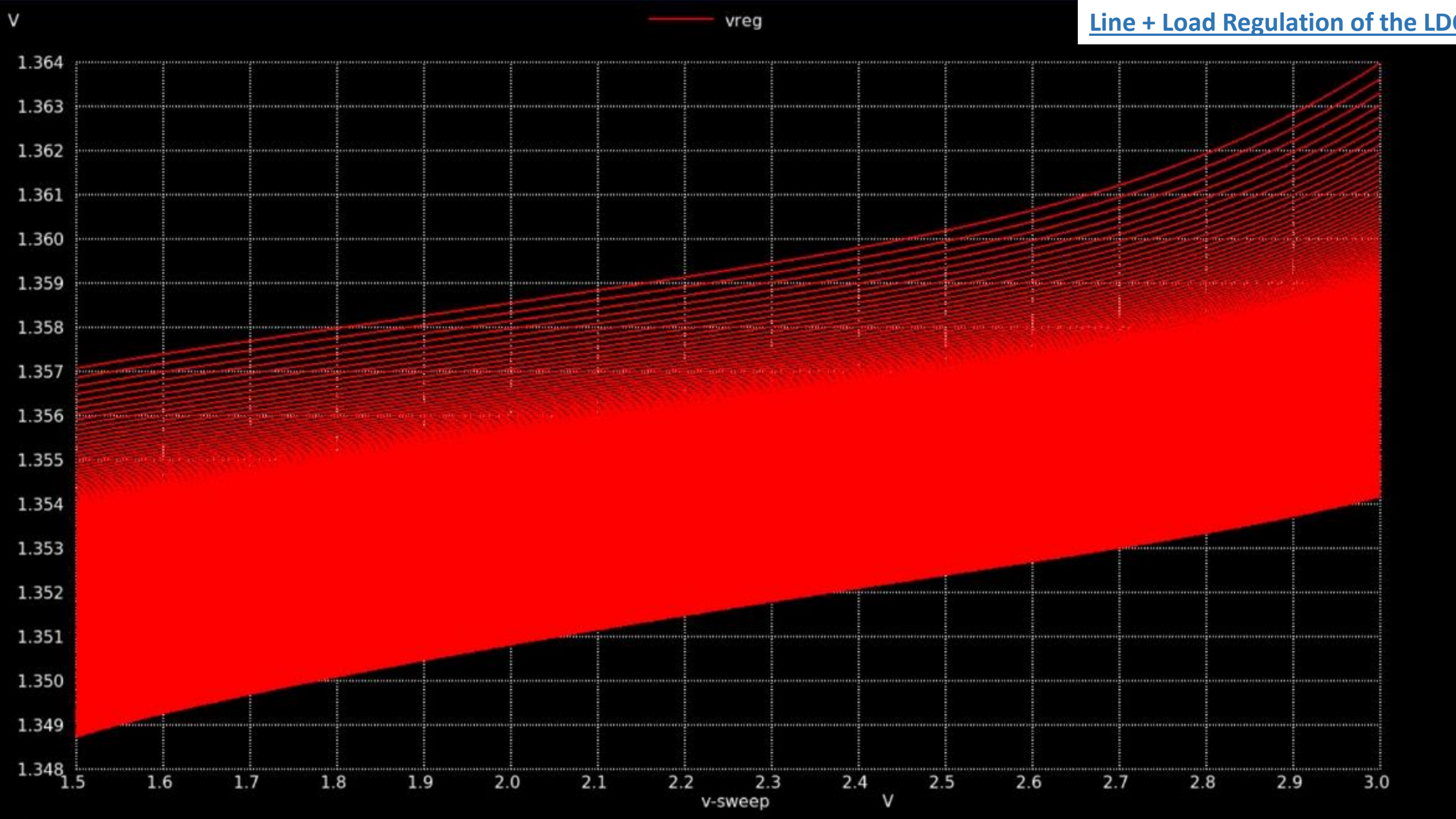
Load Regulation of the LDO



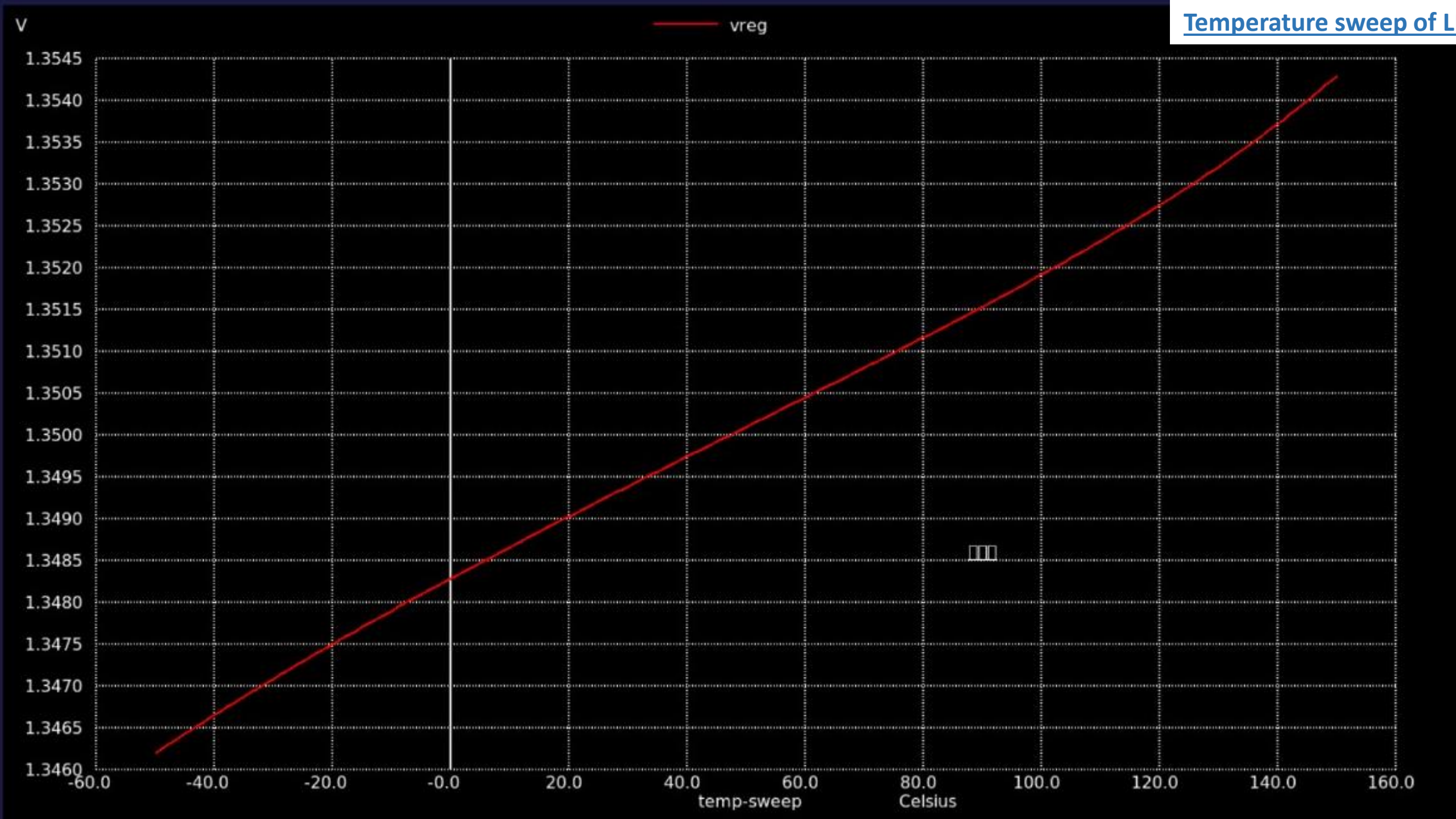
Line Regulation of the LDO



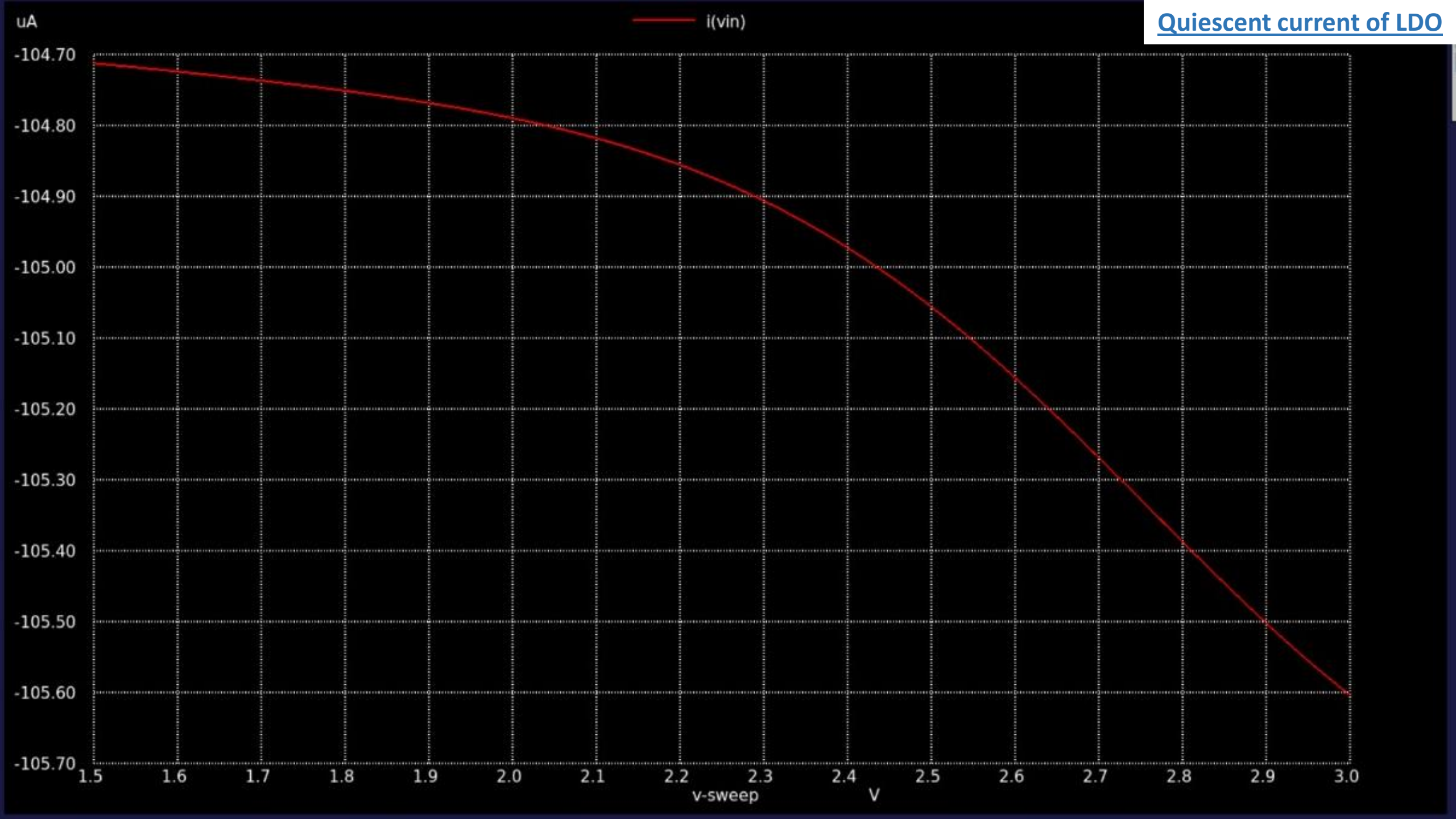
Line + Load Regulation of the LDO



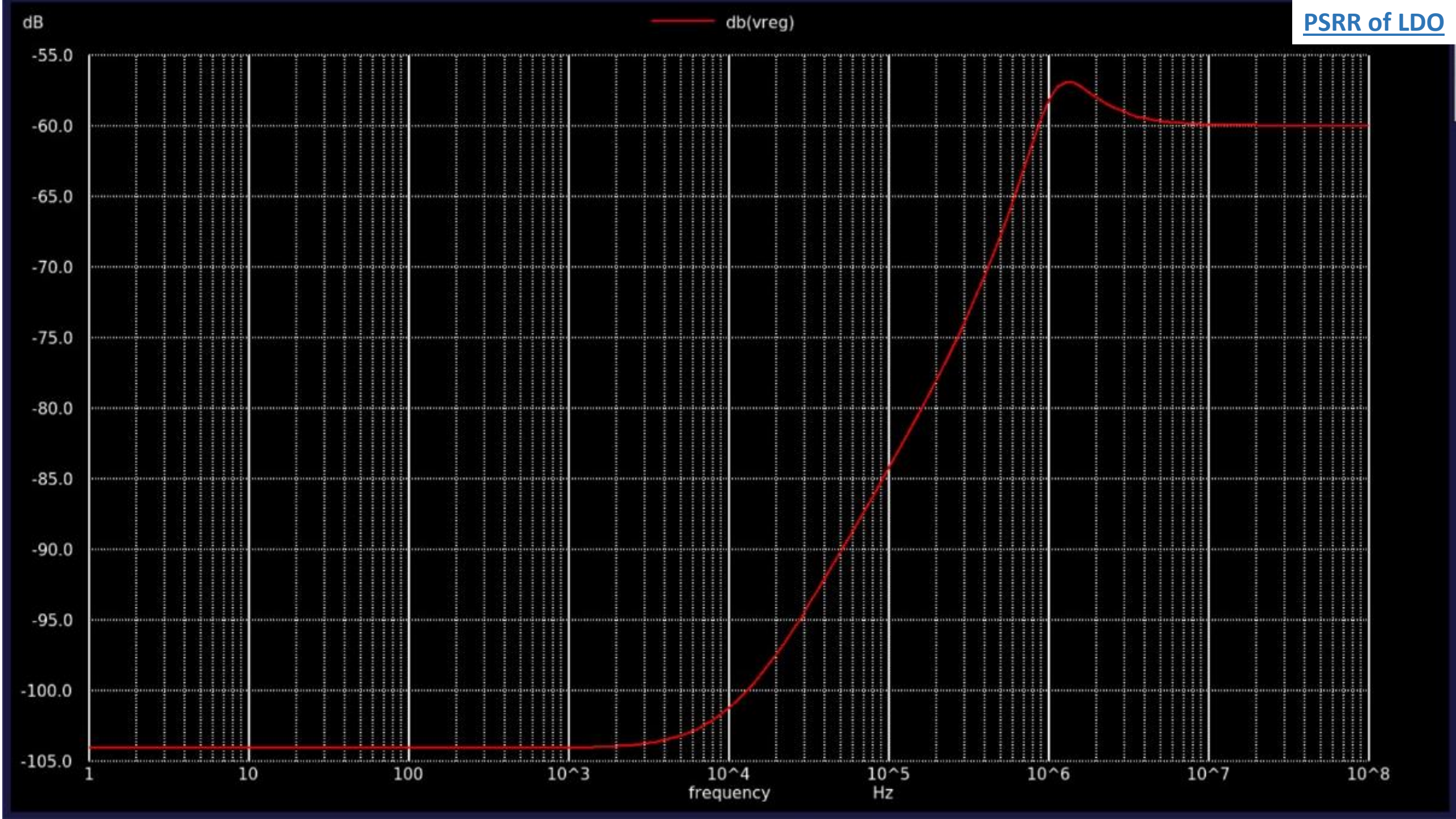
Temperature sweep of L



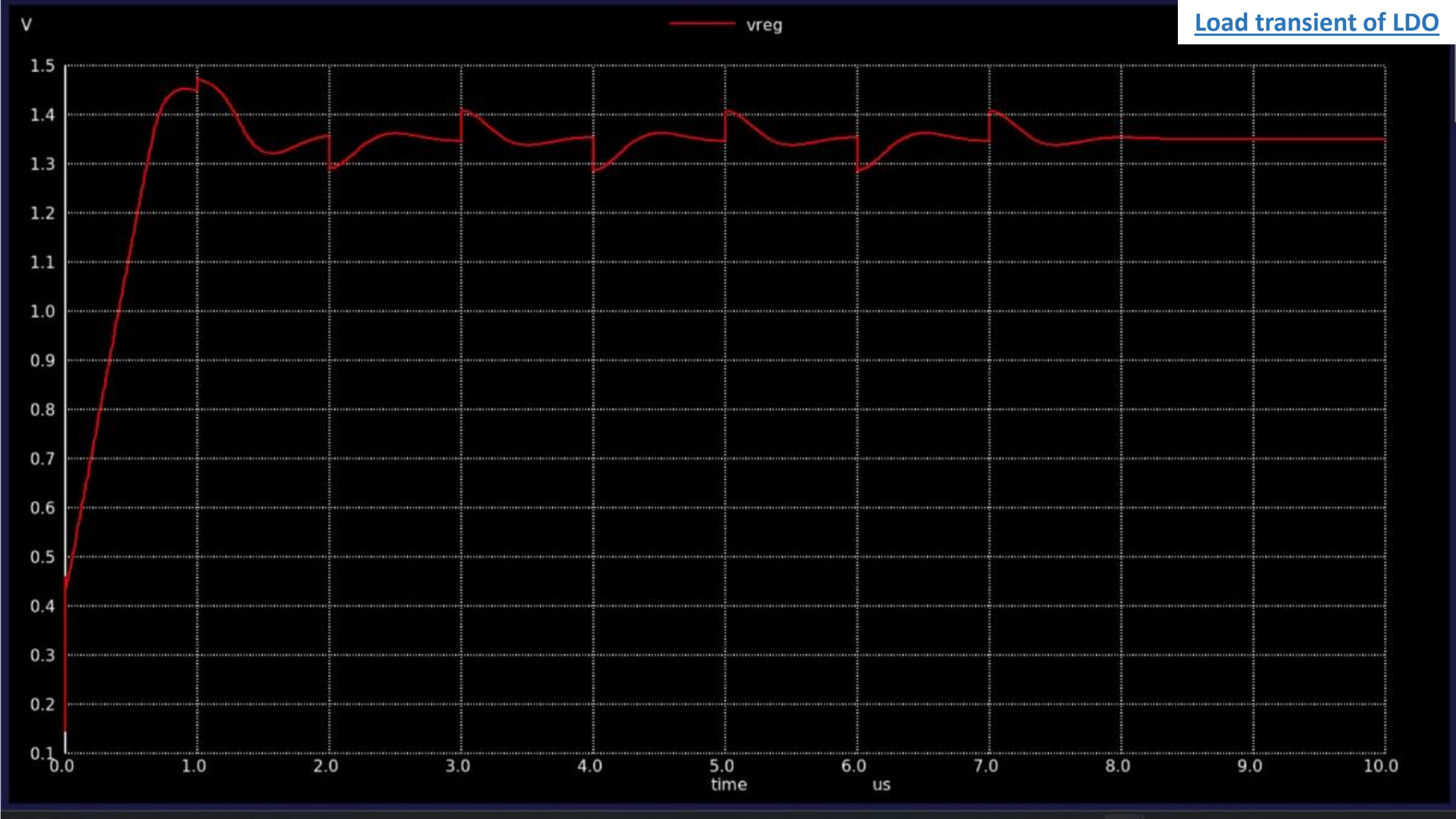
Quiescent current of LDO



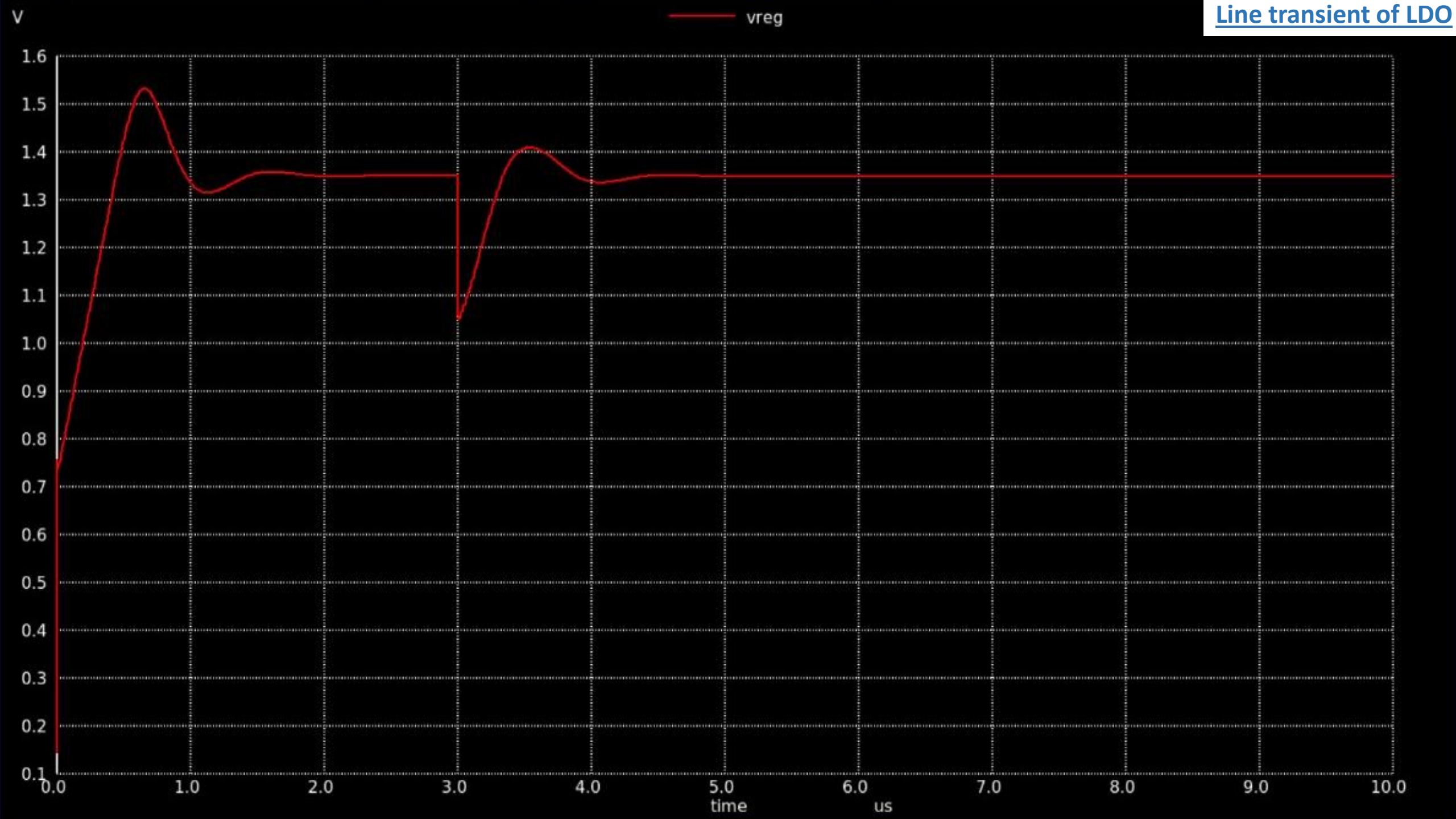
PSRR of LDO


dB
db(vreg)
-55.0
-60.0
-65.0
-70.0
-75.0
-80.0
-85.0
-90.0
-95.0
-100.0
-105.0
1
10
100
10^3
10^4
10^5
10^6
10^7
10^8
frequency
Hz

Load transient of LDO



Line transient of LDO



Final Results

- **Gain**: 62dB (hand calculated)
- **Pole1**(dominant): 4kHz, **Pole2**(non dominant): 100MHz (hand calculated)
- **GBW**: 4.8MHz(hand calculated)
- **Phase margin**: 82degree (hand calculated)
- **|PSRR|:** greater than 60dB
- **Iq**: 104uA
- **Efficiency:** 89.77%

Things I learnt from this Project

- This project helped me strengthen my concepts on Compensation, Pole zero Analysis and Stability.
- I learnt how to approach the design for the topology with Mosfets in saturation.
- Relearnt the concepts of small signal analysis and Transfer functions
- Improved my problem solving approach after many attempts.
- Learnt all the wrong approaches to do the design and learnt the correct way.
- Improved my concepts of Analog and avoid silly mistakes.

References

[1]. A Low Drop Regulator (LDO) in UMC 180 nm Technology by Mohammed Rizwan

[2]. Low Drop-Out Voltage Regulators: Capacitor-less Architecture Comparison by Joselyn Torres, Mohamed El-Nozahi, Ahmed Amer, Seenu Gopalraju, Reza Abdullah, Kamran Entesari, and Edgar Sánchez-Sinencio.

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Thank you