Low Drop-out Voltage Regulators with SKY130PDK

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Acknowledgement:

- I'm grateful to the constant mentoring and support of [Manjunath Kareppagoudar](#) and [Soumya Kanta Rana](#).

- I'm thankful to [Ahmed Tawfiq](#) for the help on Ngspice and Xschem software, it simplified much of my work .

- This project wouldn't have been possible without all the help I got.

Linear Regulators

- Regulations is achieved by dropping voltage

- Switches are in saturation region.

- Higher losses and low efficiency when dropout is high.

- We select linear regulators when there is a need of small voltage drop.

- Efficiency is inversely proportional to Voltage drop.

- LDO have less noise , so they are preferred for RF sensors and others.

Important Concepts:

- Line transient and Load transient.
- Concept of negative feedback and why is it necessary ???
- Second order system.
- Why pole splitting is required???
- Why do we need a phase margin of 60degree or greater???
- How to stabilize a system ???
- How to analyze the stability ??
- How to get poles and decide which is significant and which is not (dominant and non dominant poles) ???
- Types of Compensation employed.
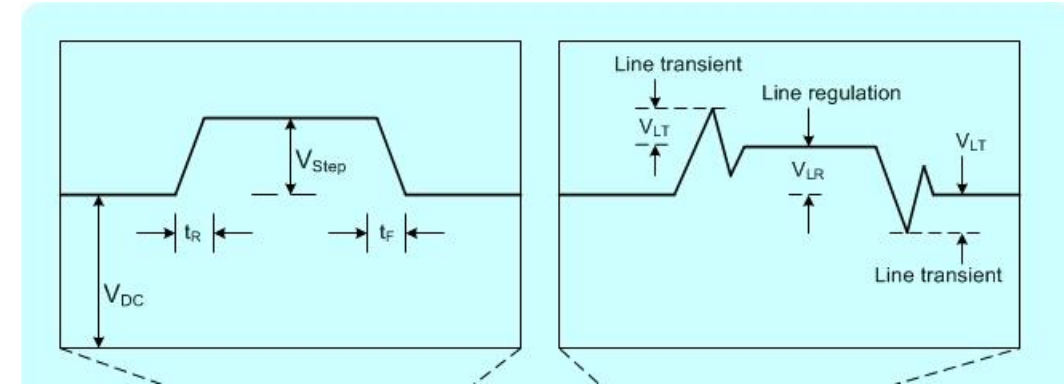

Line transient
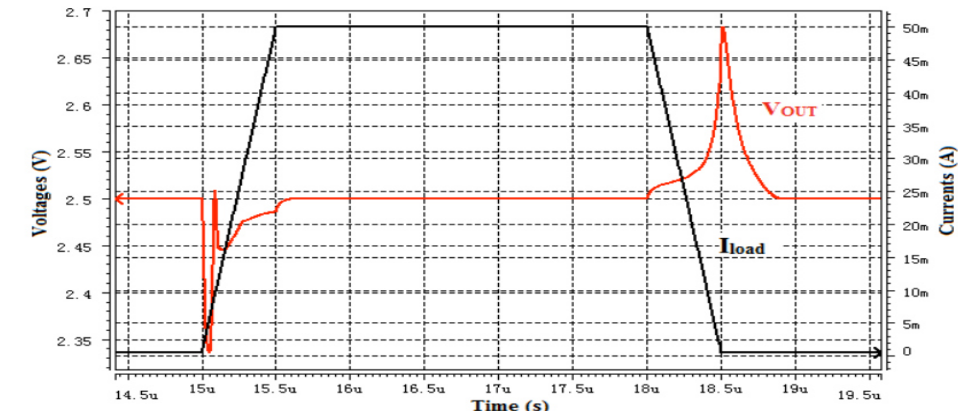
Load transient

Specifications:

Specifications (V_{out} = 1.35V, Load capacitor=0.1nF, and Full load=40mA):

Specs	Description	Value
V_{IN}(max)	Maximum input voltage range	3V
V_{IN}(min)	Minimum input voltage range	1.5V
V_{DO}	Dropout voltage for 40mA load current (error loop gain = 20dB)	150mV
I_Q	Quiescent current (no load current) (V_{in} = 3V)	$\leq$ 50 µA
t_{Set}(Load)	Average of settling time to ±1% of final value of 20mA to 40mA and 40mA to 20mA load changes (100ns rise and fall time)	$\leq$ 1µs
t_{Set}(Line)	Average of settling time to ±1% of final value for ΔV_{IN} from 2V to 3V and 3V to 2V for 10mA load (100ns rise and fall time)	$\leq$ 2µs
PSRR	Magnitude of power supply rejection (v_{out}/v_{in}) at 100Hz (10mA)	$\geq$ 60dB
I_{SC}	Short circuit current with a 10Ω load resistor (V_{in} = 3V)	$\leq$50mA
PM	Phase margin of main feedback loop (10mA)	$\geq$ 60°
η	Efficiency for full load and V_{IN} =1. 5V	$\geq$ 90%
$WC^+ V_{out}$	Max V_O with 10mA load (V_{in} = 1.5-3V, -40°C$\leq T \leq$125°C, Process)	$\leq$ 1.36V
$WC^- V_{out}$	Min V_O with 10mA load (V_{in} = 1.5-3V, -40°C$\leq T \leq$125°C, Process)	$\geq$ 1.34V

Credits: Soumya Kanta rana, Analog Engineer (Texas Instruments)

Error Amplifier

- Here I've used a simple differential amplifier because If we use a single stage Error Amplifier, We will handle less poles as a whole and the design will be easy for us.

- The design of the Error amplifier must be robust and good so that the regulated output voltage doesn't deviate more than 5% of the specified Vreg.

- Should provide a good gain and have a good PSRR.
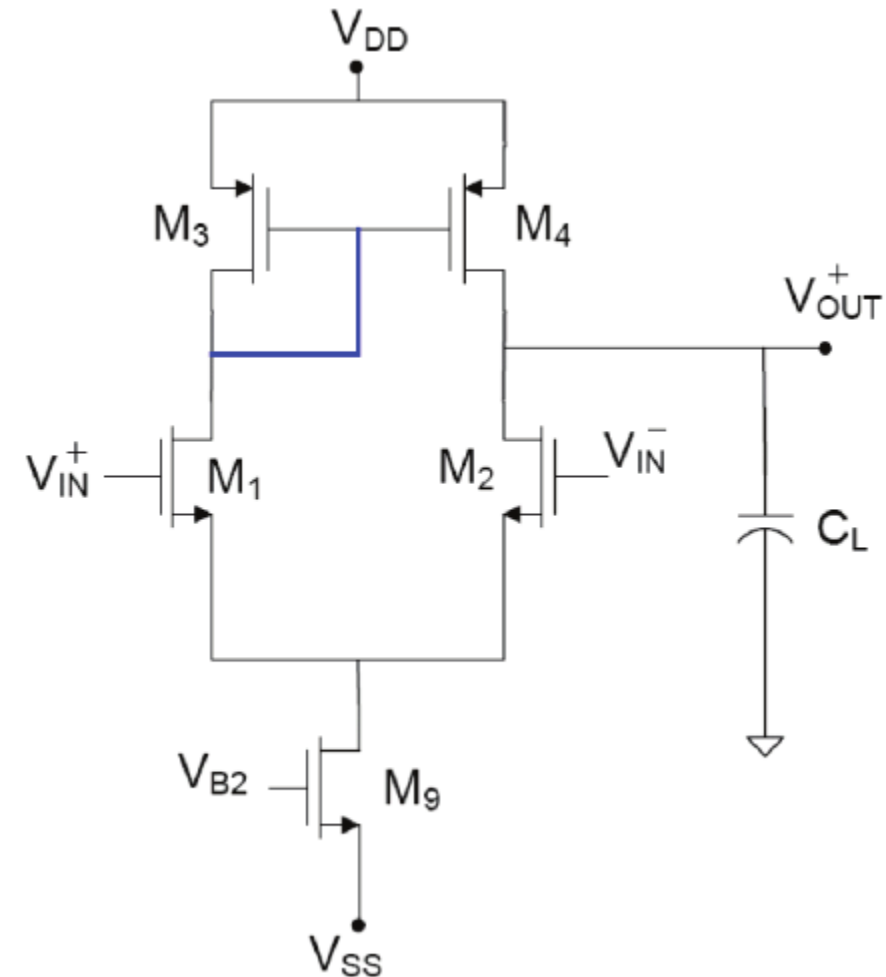
Design

- This is a linear regulator so all the Mosfets operate in saturation region.

Design of Error Amplifier:

- <u>The Aspect ratio of Differential Pair:</u>

- gm1 is the one that contributes to the gain and bandwidth of the error amplifier so

- gm1,2 = 2pi(GBW*CL)

$$\frac{W}{L} \cdot 1,2 = \frac{g_{m1}^2}{\mu_n C_{ox} \cdot 2I_1}$$

- <u>The Aspect ratio of the Current Mirror:</u>

- Before finding the W/L3,4 we need to find the Vt max of current mirrors and Vtnmax , Vtnmin of Differential pairs

- For Simplicity I've used the mosfet nfet_01v8_lvt and pfet_01v8_lvt whose Vt doesn't change much unlike nfet_01v8 and pfet_01v8.

- Vsg3=Vdd-Icmr(+)+Vtn1min

$$W/L \cdot 3.4 = 2I_3/\mu_p C_{ox}(V_{sg3} - V_{tpmax})^2$$

- The aspect ratio of the biasing mosfets:

$$V_{dsat5} = I_{crm}^- - \sqrt{\frac{I_5}{\beta}} - V_{tnmin}$$

$$\frac{W}{L}_{5,6} = \frac{2I_5}{\mu_n C_{ox} \cdot V_{dsat5}^2}$$

- Aspect ratio of the Pass Transistor:

- Pass transistors are typically PowerFETs which are large in width.

- From the specifications we know that Vdrop=150mV, so Vsd of Mpass is 150mV, so I targeted an overdrive voltage of 100mV.

- (W/L)pass=2IL/upCoxVov^2

- From this for IL of 40mA I got a W/L ratio of 145454.5

- (W/L)pass = 145455

- Here I used pfet_01v8 because of all the parasitic capacitance the gate cap will be quite large and can have an effect on the stability and add over miller cap, So I designed the error amp for a CL=50pF, the Mosfet pfet_01v8 offers the least Cgg (approx 20pF).

Design Concessions I made

- I chose a bias current of 50uA because the specification needed a settling time of 1us which will be very much affected if we decrease Slew rate but the quiescent current (IQ) should be less than 50uA.

- Only way to not hamper the settling time was to choose a good Slew-Rate, the only solution to do that was burn more current as I cannot change the load cap.

- This has an affect of increasing the quiescent current (IQ) to more than 50uA, the final result showed a IQ of around 100uA, this cannot be avoided because of the PDK.

Intuitive Analysis of poles and Zeros

Finding Poles and Zero of LDO Intuitively

$V_{dd} + V_{odd}$

M9 M3 Mpass

Ce R2 Vout

VFB M2 M1 Vref+Vref R2 Cout RL

VFB

Iref M0 R1

M10

→ To find whether the feedback is +ve or -ve, we put a huge impedance node at the feedback and apply small signal Vtest and cover the loop and check what's coming back at the other part of node

VDD+Vdd Vdd

Ce R2

VFB Vref+Vref Vout

Iref R2 Cout RL

V+ Vref R1

Find loop gain = $\dfrac{V_{ret}}{V_{test}}$ is negative

loop gain = $\dfrac{V_{ret}}{V_{test}} < 0$ [negative] so -ve feedback

loop gain -
Now let's do it Intuitively.

$V_{dd} + V_{dd}$ $V_{dd} + V_{dd}$

M4 M3 Mpass

4 R2 Ce 5

VFB M2 M1 Vout

3 +Vref

Iref 1 2 R2 RL

M10 M0 6

V+ Vref R1

If we increase voltage at V+
→ For M_2, if we increase gate voltage, small signal source voltage will increase, so the source of M_1 voltage also Increases
→ If we increase source of M_1 drain of M_1 also increases bcz it becomes common gate config.
→ So Voltage at Node 5 also increases
→ then gate voltage of PMOS Mpass increases the drain voltage decreases bcz its common source config of PMOS
→ then node 5 voltage decreases the combo of R_2 & R_1 becomes voltage divider, then voltage at node 6

U.G.B → Unity Gain Bandwidth.

Voltage decreases then voltage at node 2 also decreases
→ So when we increase voltage at node 1 after travelling the nodes the voltage at node 2 is decreasing. So this is a negative feedback

[LG] Loop Gain: [open loop gain x feedback factor] [Aβ]

→ If we know L.G we can directly find closed loop behaviour

Closed loop Transfer = $\dfrac{\text{open loop T.F}}{1 + \text{loop Gain}} = \dfrac{A}{1 + A\beta}$
function

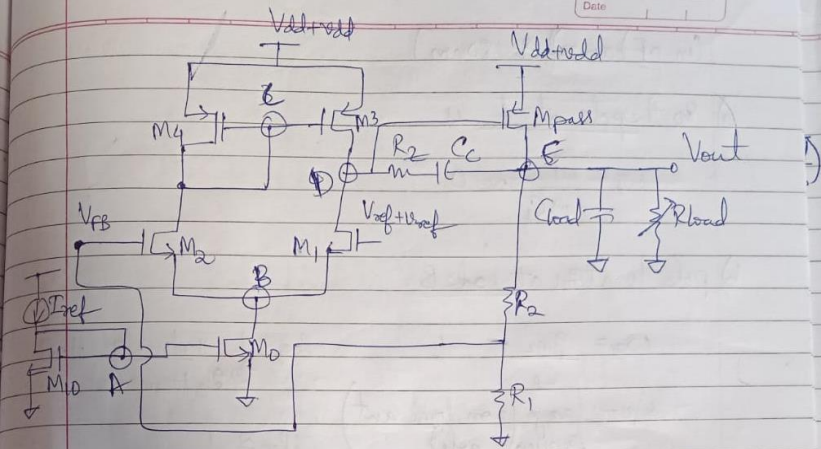→ WKT poles and zero location is not changed for loop gain and open loop gain

LG β=1 For β=½ P_1 & P_2 location
A remains same but the
$A_2 = \dfrac{A_1}{2}$ β=½ DC Gain & U.G.B decreases

P_1 P_2 UGB1
UGB2

→ Even if we decrease β poles and zero locations are unchanged but DC Gain & U.G.B is decreased

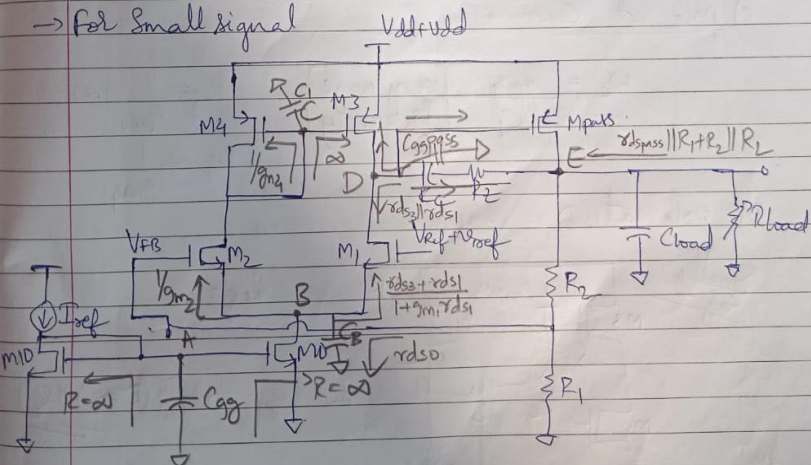$A_2 = \dfrac{A_1}{2}$ & $UGB_2 = \dfrac{UGB_1}{2}$ [for β=½]

→ WKT every node containing a pole

Panel 1 (left)

$M_3, M_4 \rightarrow$ identical

$M_1, M_2 \rightarrow$ identical

Vdd+vdd

Vdd+vdd

M_4 | M_3

R_2 C_c

Mpass

$V_{ref}+U_{ref}$

Vout

C_{load} | R_{load}

V_{FB} | M_2 | M_1

B

R_2

Iref

M_0 A

M_{10}

R_1

→ There are 5 nodes so there can be max 5 poles

→ For Small signal

Vdd+vdd

$\frac{R_{C1}}{C}$ M3

M_4 $\frac{1}{g_{m4}}$

C_{gspass} D

Mpass

$E \leftarrow rd_{spass}||R_1+R_2||R_L$

$\frac{1}{g_{m4}}$

$\frac{W}{R_2}$

$rd_{s3}||rd_{s1}$

$V_{ref}+U_{ref}$

C_{load}

R_{load}

V_{FB} | M_2 | M_1

$\frac{1}{g_{m2}}$ B

$\frac{rd_{s3}+rd_{s1}}{1+g_{m1}rd_{s1}}$

R_2

Iref

A

M_{10} | M_0 | (rd_{s0})

$R=\infty$

$R=\infty$

C_{gg}

R_1

→ For small signal Iref = open ckt and R looking at M_{10} & M_0 are ∞ and also C_{gg} of M_{10} & M_0 is present (gate to ground capacitance) which is large.

Panel 2 (middle)

(in pF range for 180nm)

a) So the pole at A is

$$w_A = \frac{1}{(\infty)C_A} \sim 0$$

b) pole location at node B.

$$w_B = \frac{g_{m2}}{C_B}$$

$w_B \rightarrow$ large (non dominant frequency pole) $-C_V$

$R_{eq} = \frac{1}{g_{m2}} \frac{1}{1+g_{m1}rd_{s1}} ||(rd_{s3}+rd_{s1})|| rd_{s0}$

very high

$R_{eq} \simeq \frac{1}{g_{m2}}$

c) pole at C

$$w_C = \frac{g_{m4}}{C} \begin{bmatrix} \text{very large} \\ \text{frequency} \end{bmatrix}$$

$R_{eq} = \frac{1}{g_{m4}} || \infty$

$R_{eq} \simeq \frac{1}{g_{m4}}$

D) pole at D

Small Signal

C_{gspass}

M3

$R_{eq} =$

negative gain from

$\S$ to 1

M3

C_c R_2

M_2

R_2
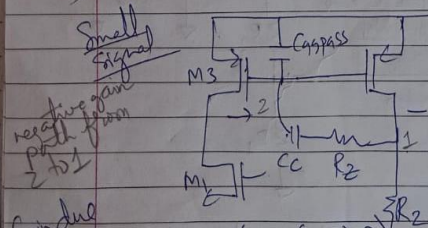
$A_2 = -g_{mpass}\left(rd_{s_{pass}} || (R_1+R_2)||R_L\right)$

Gain due to Mpass $A_2 = -g_{mpass}\left(rd_{s_{pass}} || (R_1+R_2)||R_L\right)$

R_1

This is Common source config of Mpass and gain is negative

Panel 3 (right)

Vref

A_1 C_{gg}

A_2

R_2

C_c

R_1

R_L C_{out}

R_1
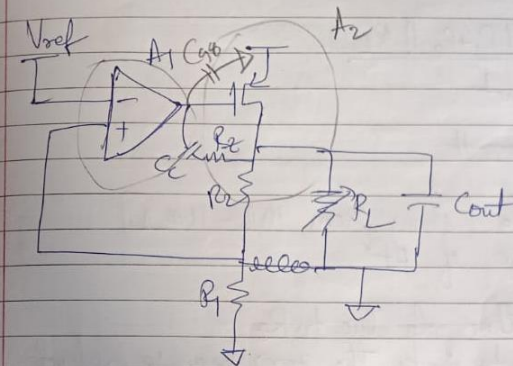
Miller

→ A_2 is negative gain so the C_c experience Miller effect, so C_c is miller cap

$$C_{eq_D} = C_{gg} + C_c(A_2+1)$$

$$w_p = \frac{1}{(rd_{s3}||rd_{s1})(C_{gg} + C_c(A_2+1))}$$

large Impedance / large Capacitance

So w_p becomes lower frequency

WKT

$$A_1 = g_{m1}(rd_{s3}||rd_{s1})$$

$$A_2 = -g_{mpass}(rd_{s_{pass}}||(R_1+R_2)||R_L)$$

E) pole at node E

$$R_{eq_E} = rd_{s_{pass}}||(R_1+R_2)||R_L$$

$$C_{eq_E} = C_{out}$$

$$W_6 = \frac{rdspass \,||\, R_1+R_2 \,||\, R_L}{C_{out}}$$

$$R_{eq} = rdspass \,||$$

R_L is variable [vary from $10\Omega - 10m\Omega$]
C_{out} in range of pf

→ There is another pole due to R_z
→ we added R_z to make the zero ~~because~~ present because of the ~~bypass~~ C_c. To nullify zero we add R_z (present in left)

pole due to R_z

$$R_{eq} = R_z \;,\; C_{eq} = \left(\frac{1}{C_c} + \frac{1}{C_{gg}} + \frac{1}{C_{out}}\right)$$

$$P_{R_z} = \frac{1}{R_z \times \left[\frac{1}{C_c} + \frac{1}{C_{gg}} + \frac{1}{C_{out}}\right]}$$

This P_{R_z} is very high frequency.

So there are total 6 poles and 1 zero

→ To find zero, for input = zero, output = 0

To find zero
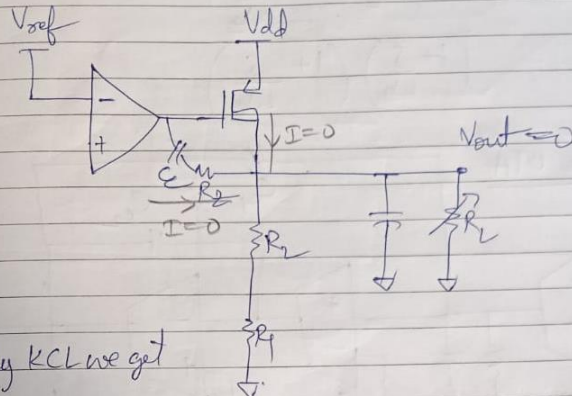
Apply KCL we get

$$W_z = \frac{1}{\left(\frac{1}{g_m pass} - R_z\right) C_c}$$

→ If we make $R_z > \frac{1}{g_m pass}$ then W_z comes in left half plane

→ So we nullify the effect of RH.P [because RHP zero is phase lagging]

→ pole at A the node will not be coming at signal path (bcs its bias path). So pole at A is not an important pole (Vref / V$_{th}$ path)

→ So we get effective pole 2, one due to R_z and other at the output

→ So 2 effective pole (W_z, W_e)

dominant pole ↙   ↘ non dominant pole

one zero (W_z)

$$Loop\ Gain\ (S) = (-A_1 A_2) \times \frac{\left(1 - \frac{S}{W_z}\right)}{\left(1 + \frac{S}{W_D}\right)\left(1 + \frac{S}{W_e}\right)}$$

Error Amplifier Schematics

Spec Achieved:
(W/L)1,2 = 207
(W/L)3,4 = 7
(W/L)5,8 = 5
Gain : 37dB
GBW: 7MHz
Ibias: 50uA
Slew Rate: 1V/usec
VDD: 1.5V
ICMR+: 1.2V
ICMR-: 0.9V
CL: 50pF

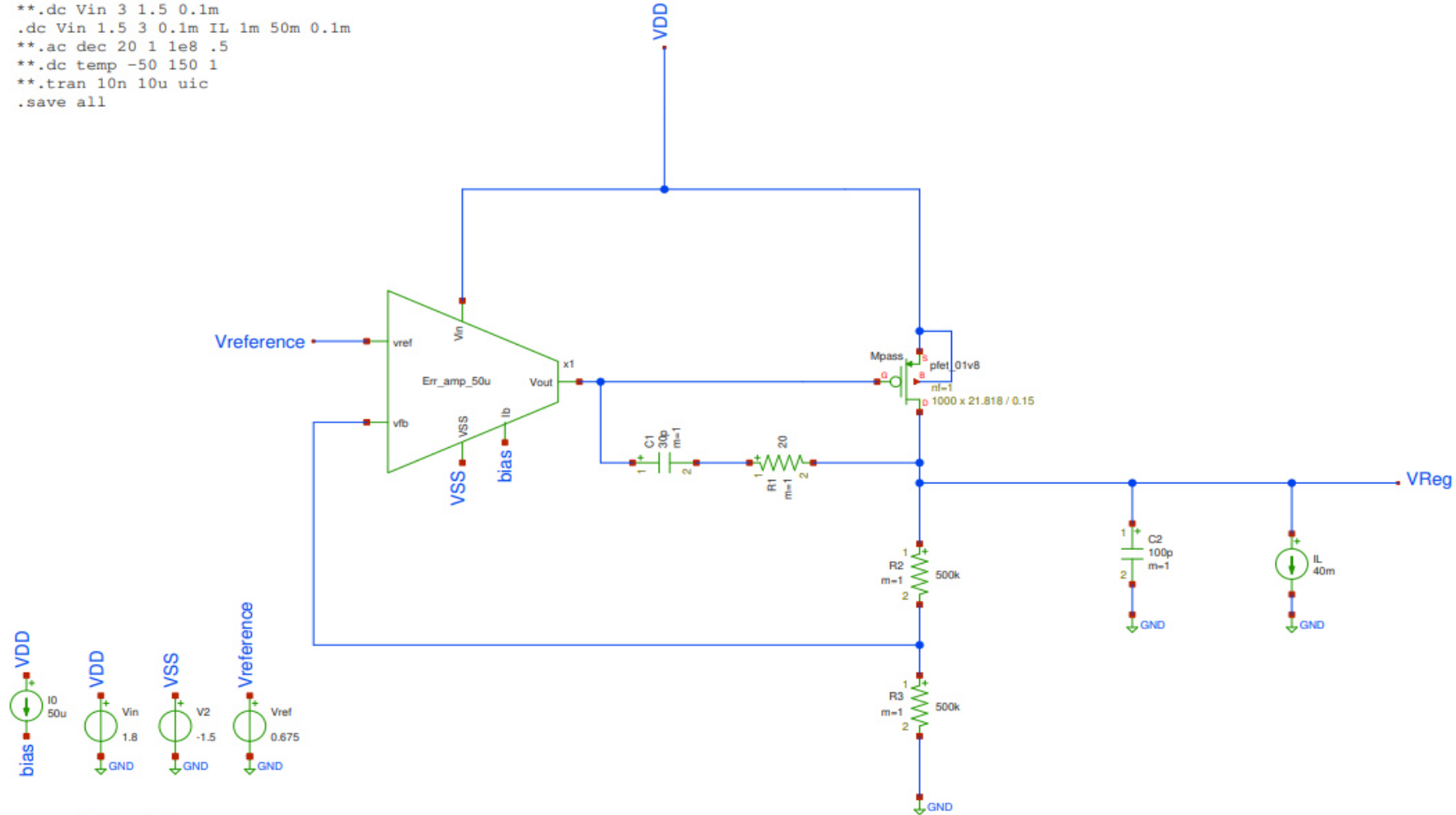Gain of the error amplifier
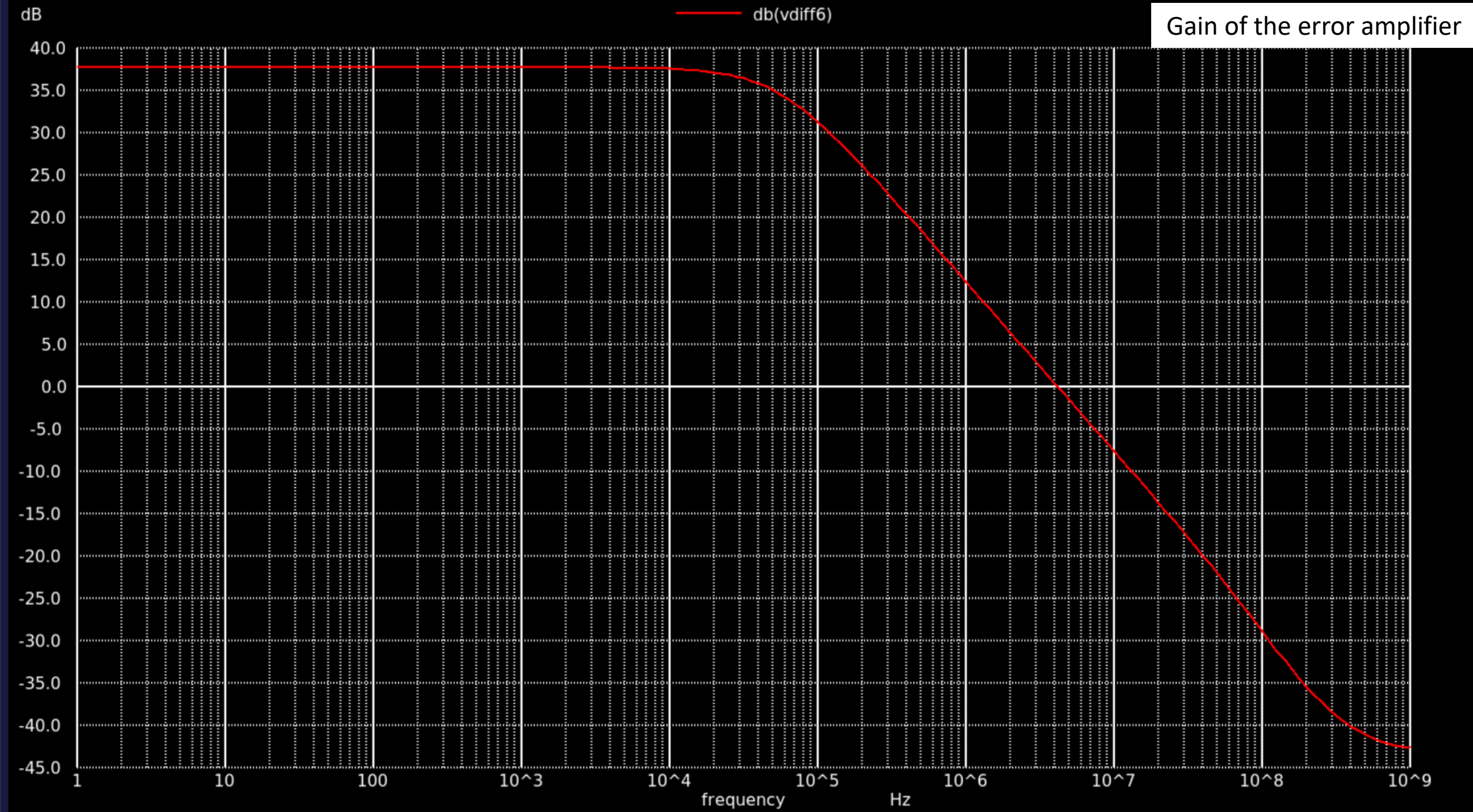
Gain and Phase margin of the error amplifier
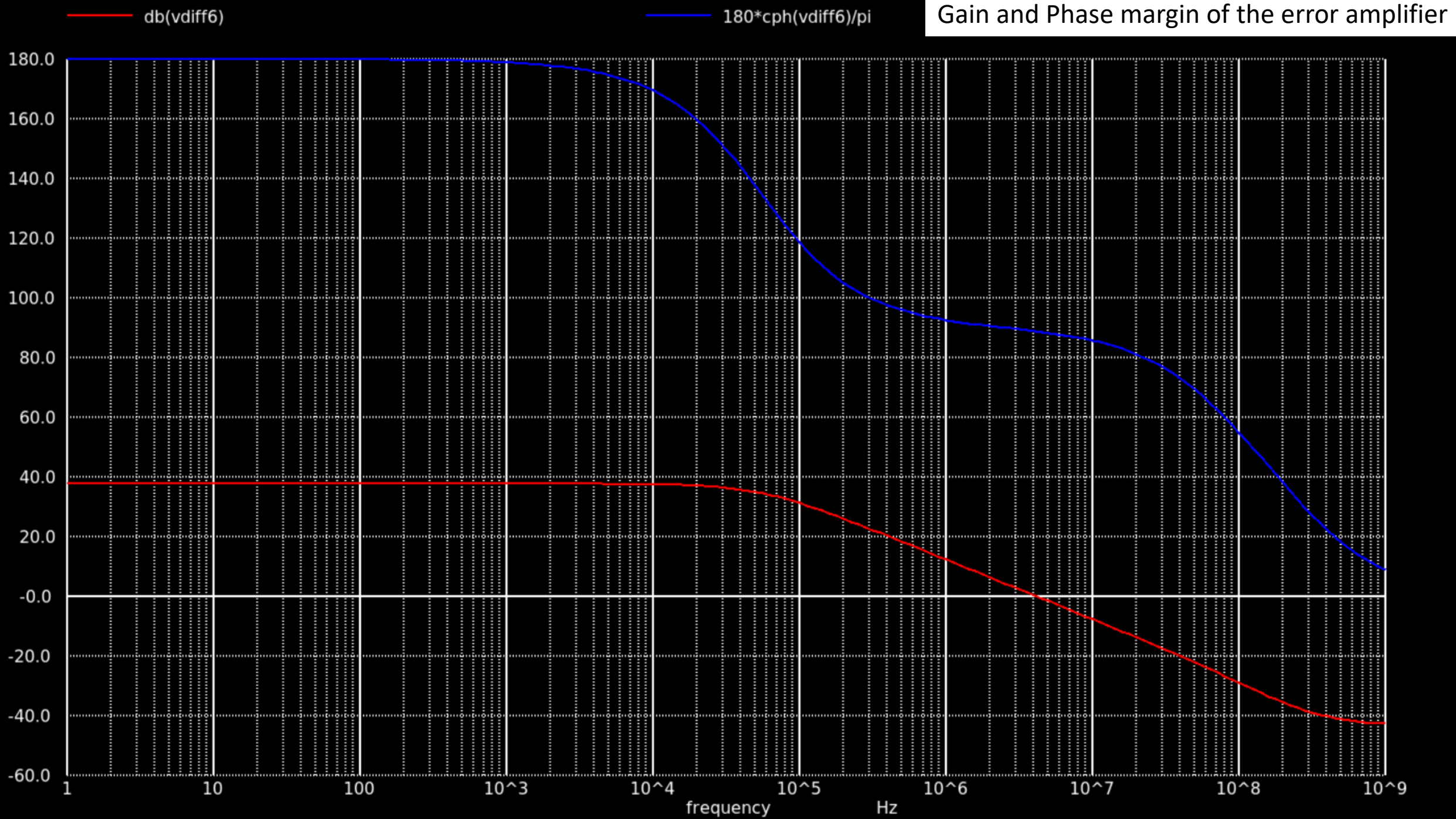
LDO Schematics
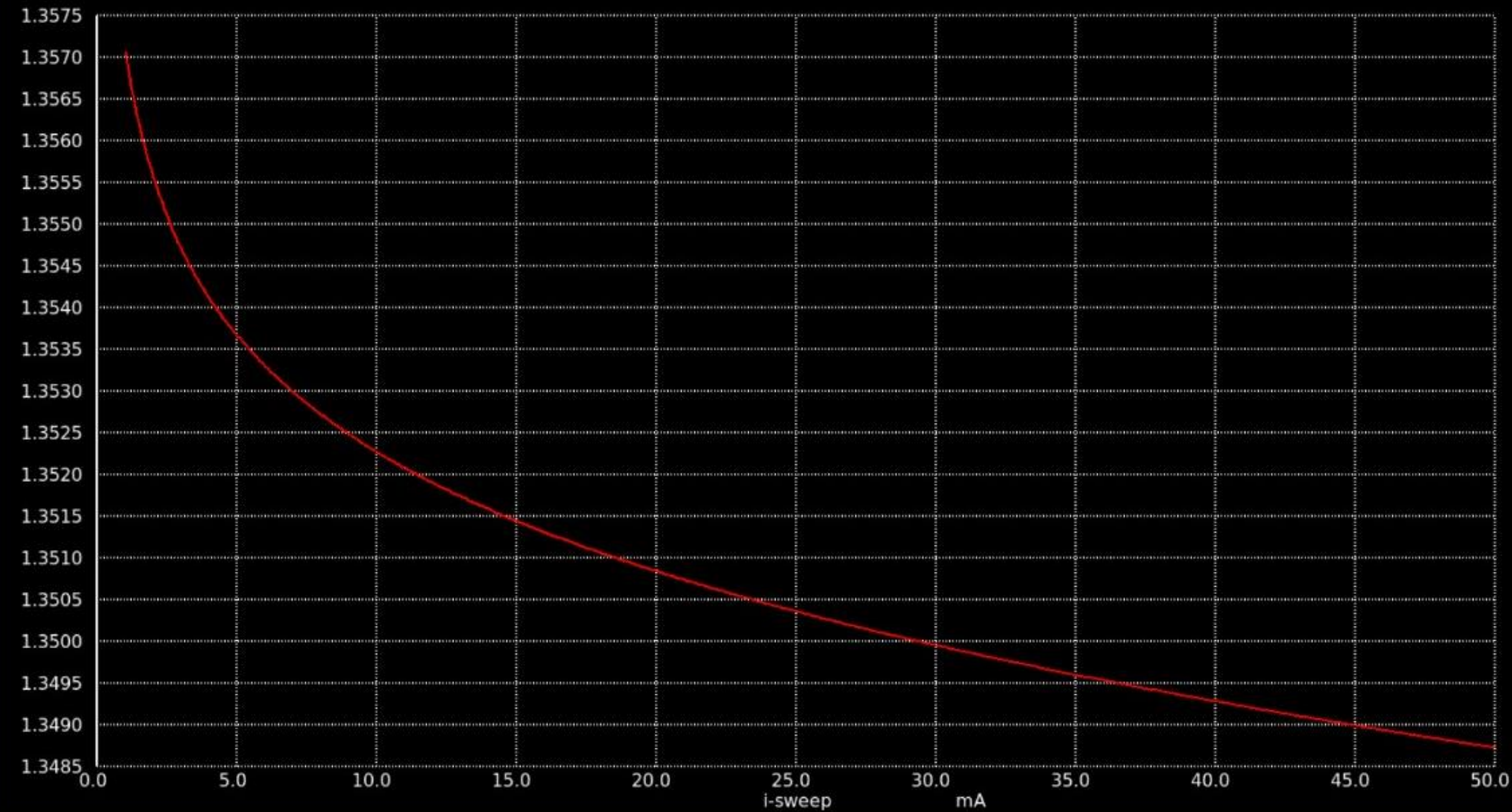
Load Regulation of the LDO
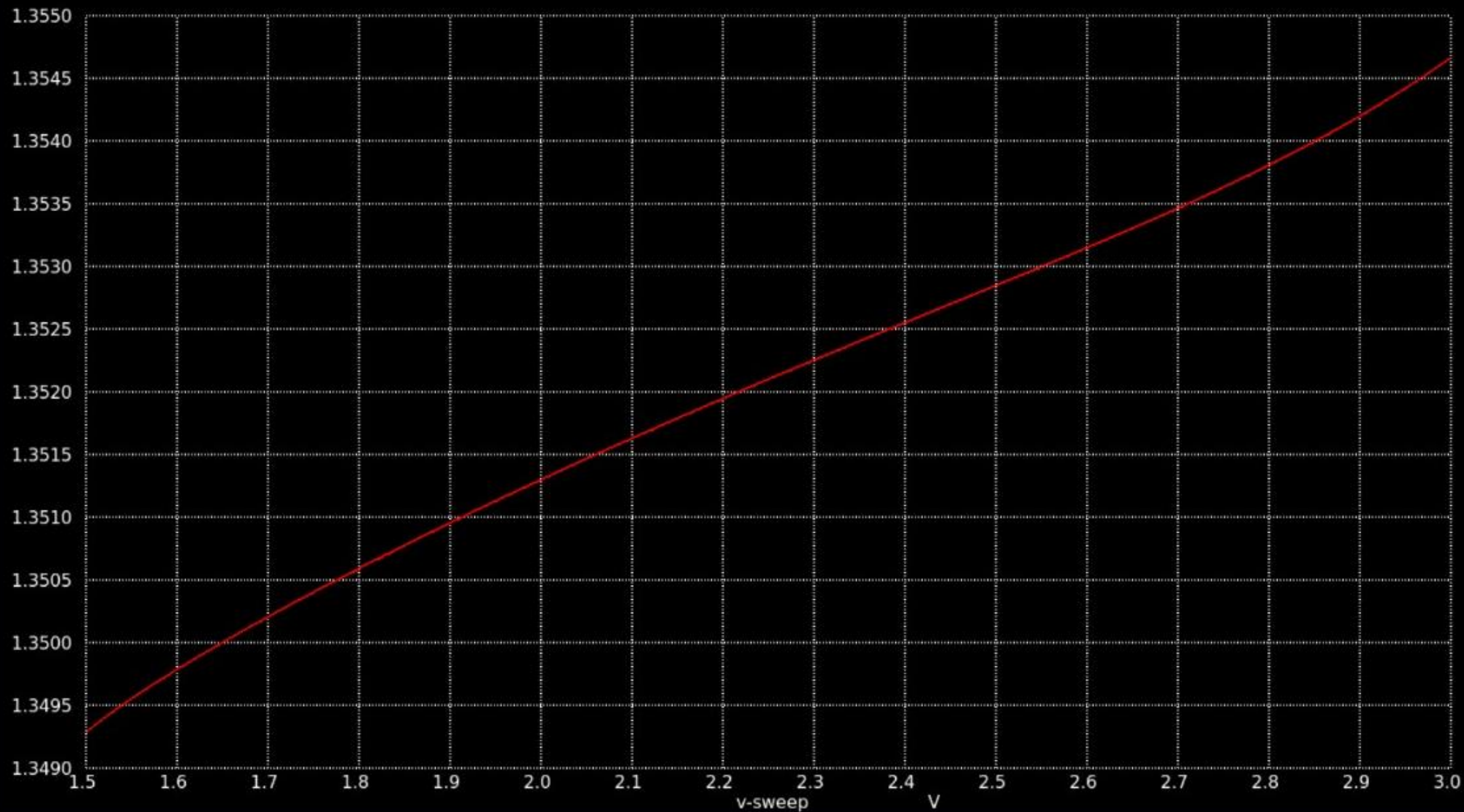
Line Regulation of the LDO
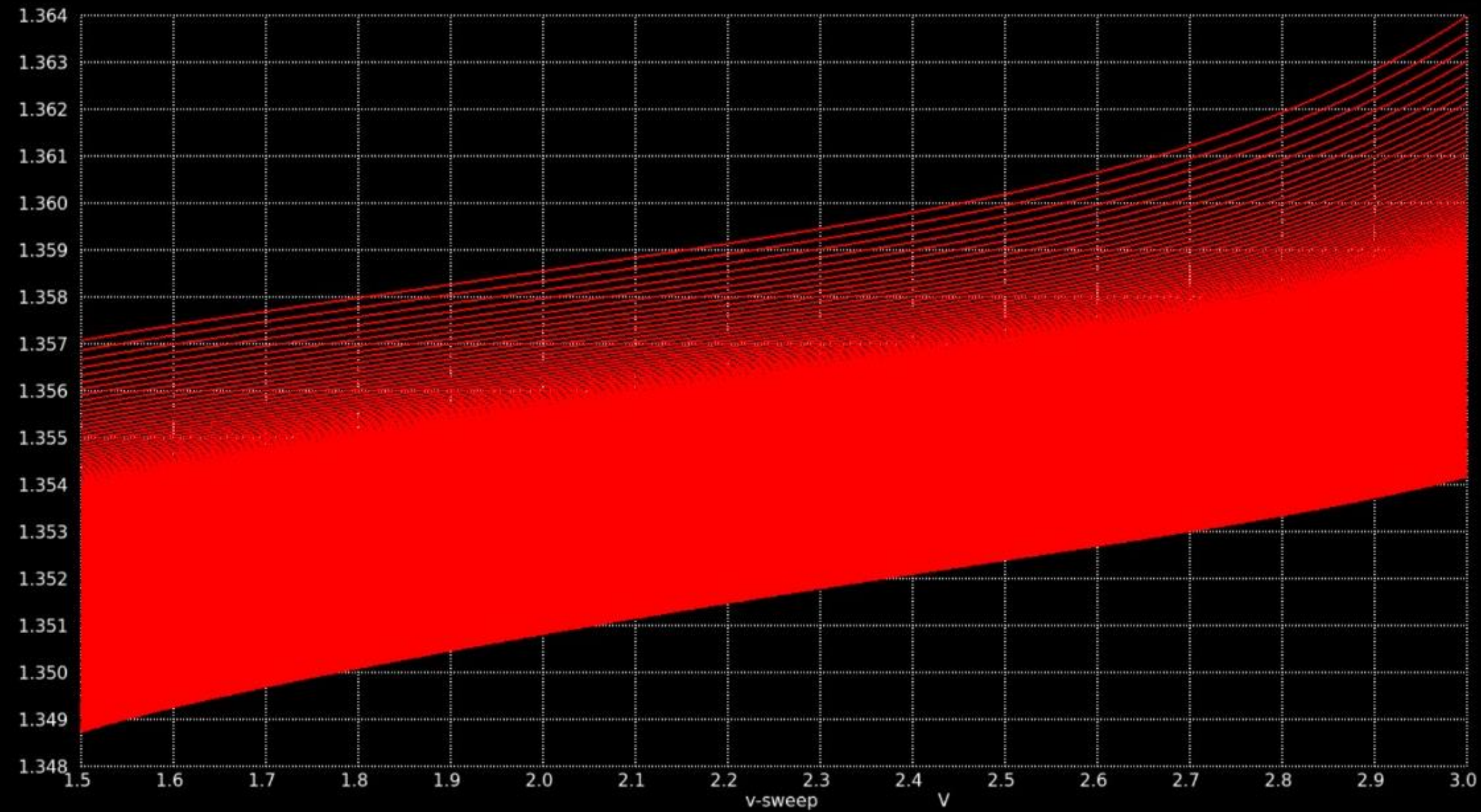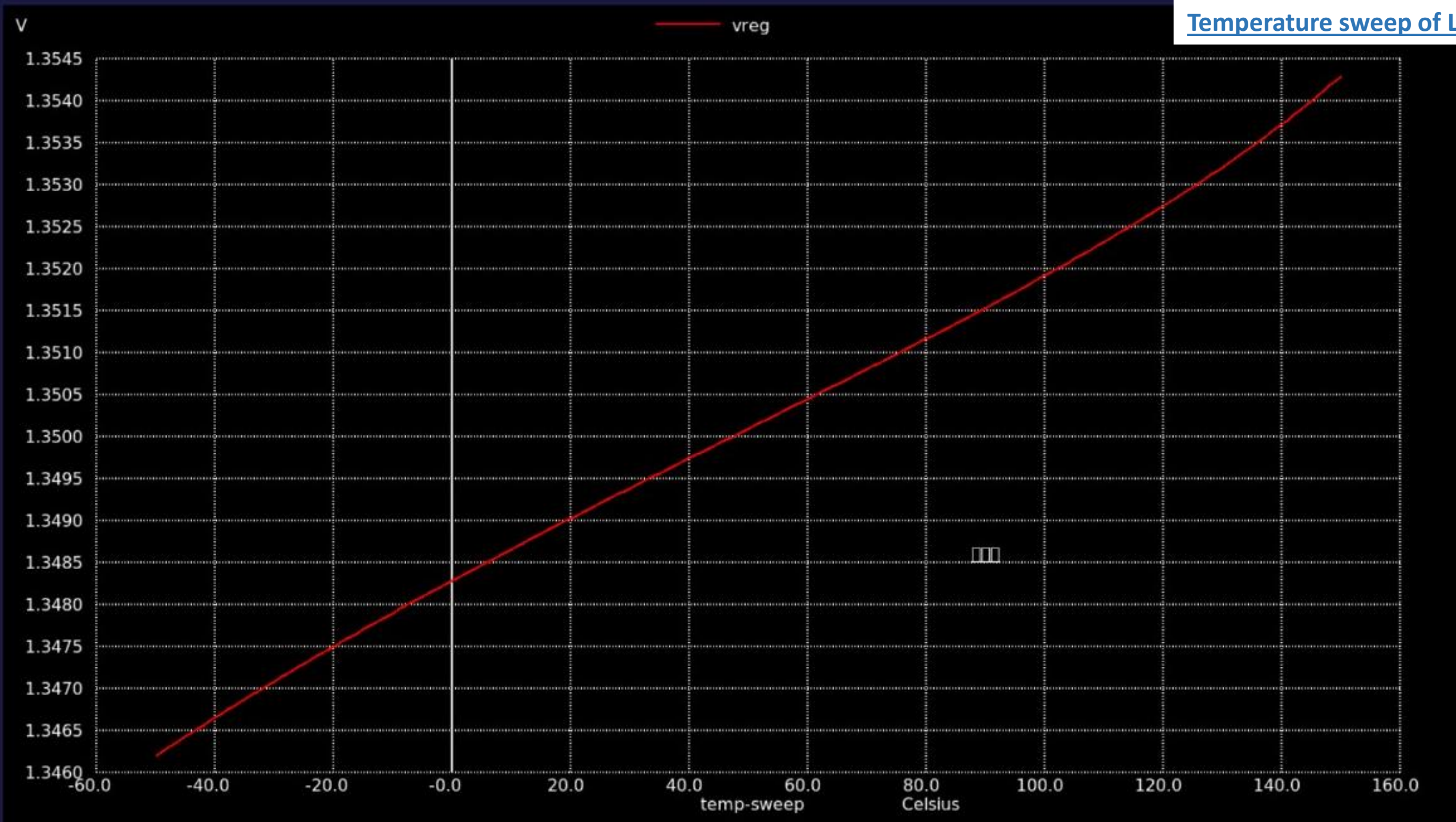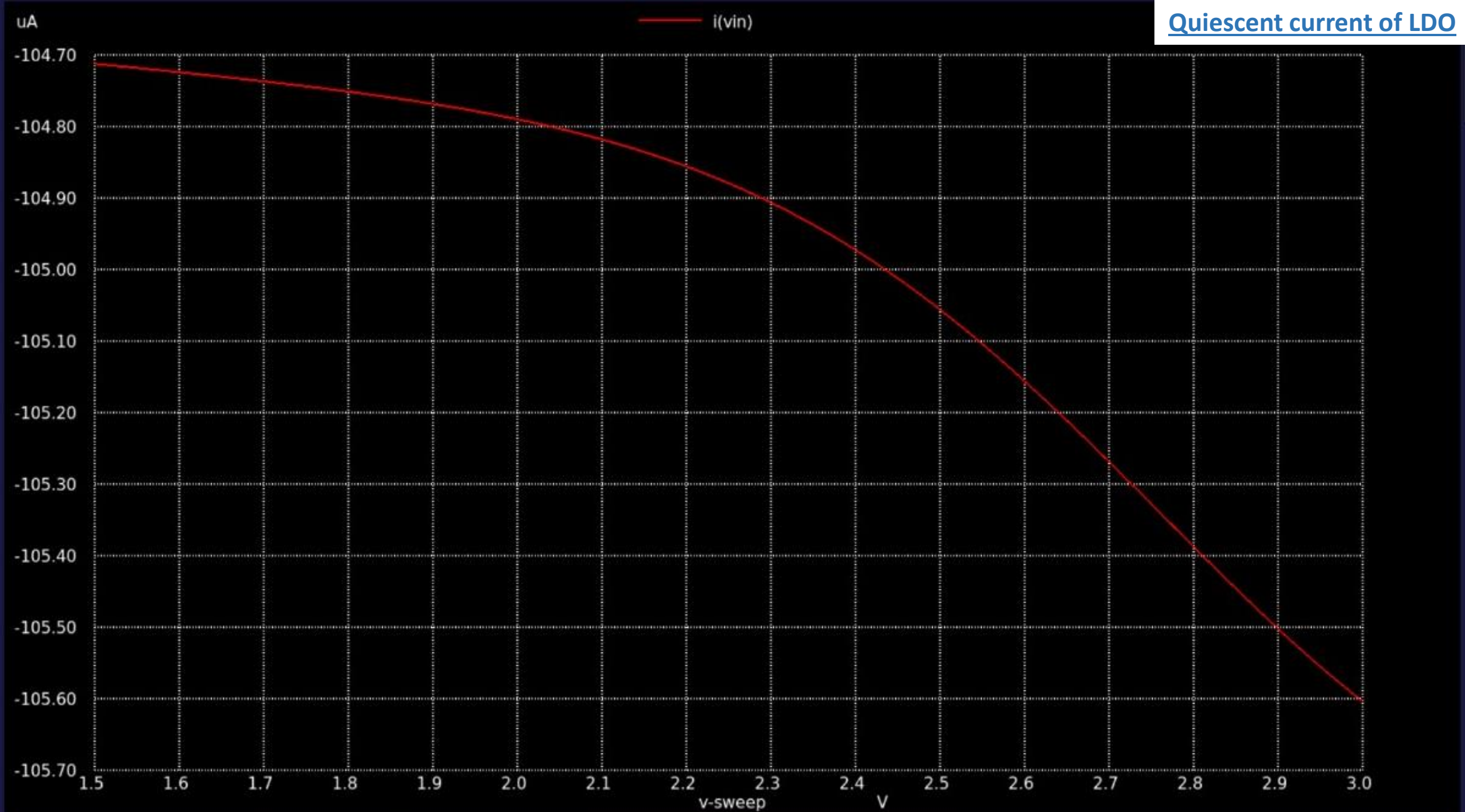
Quiescent current of LDO
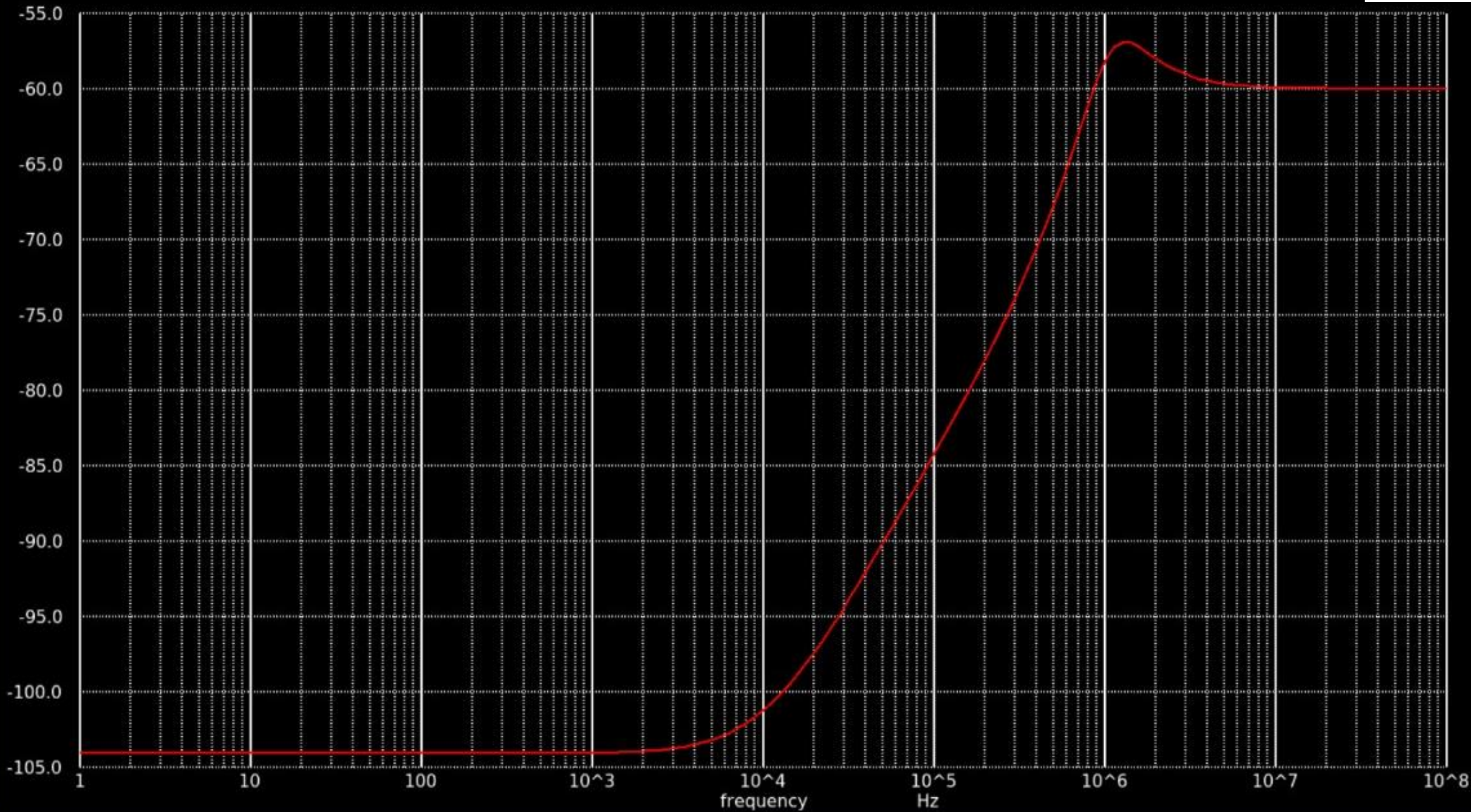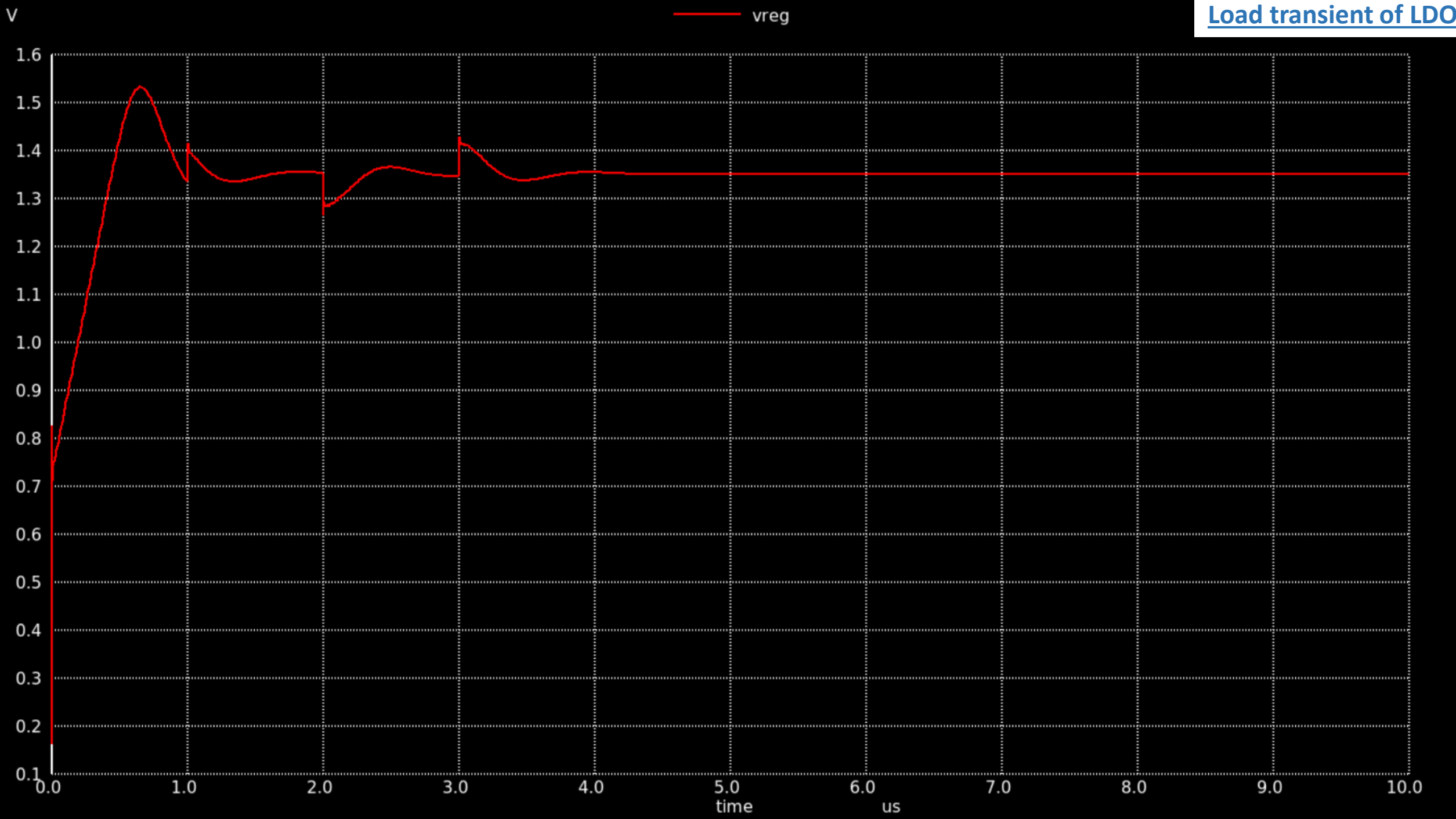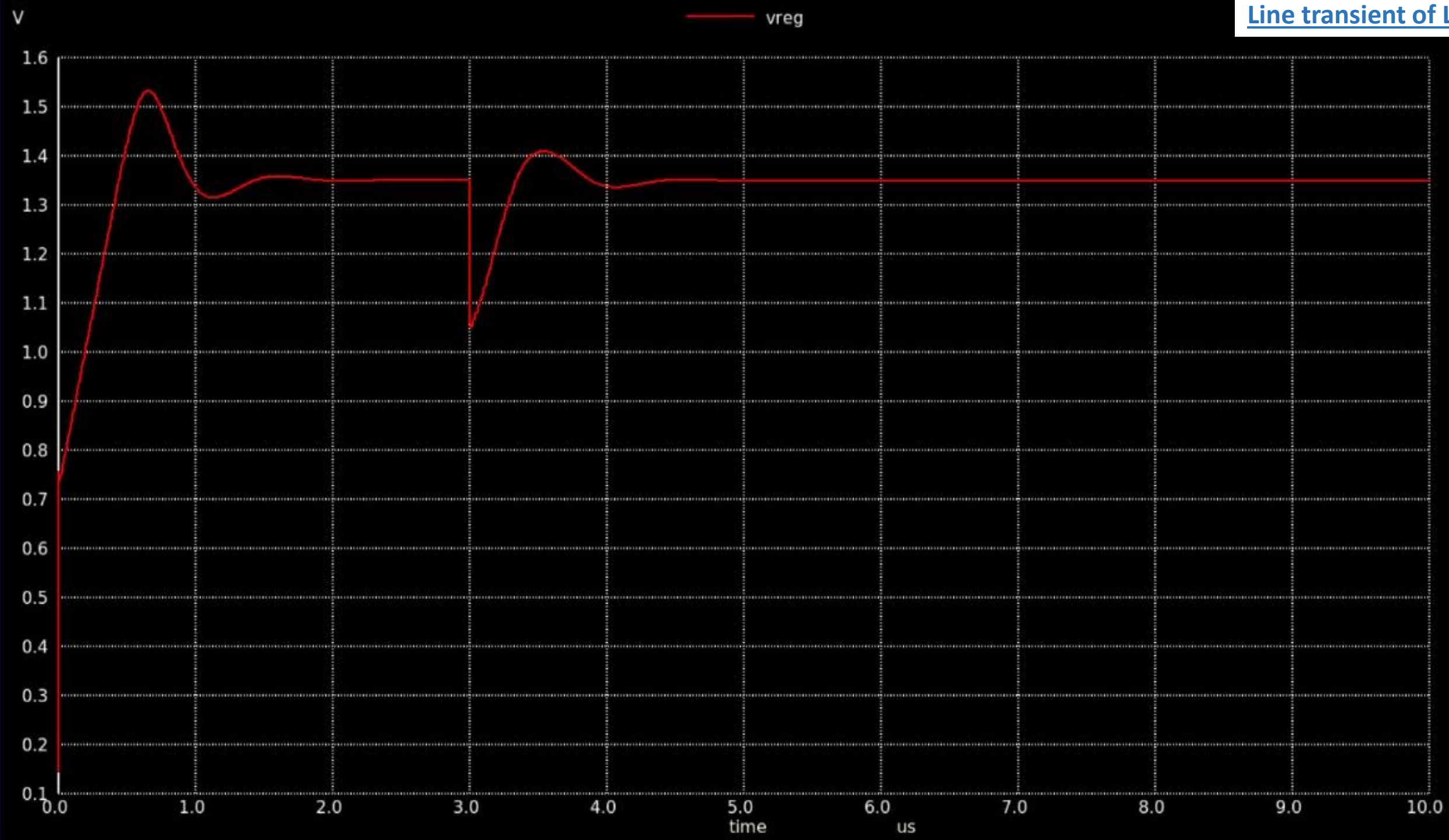
Final Results

- **Gain**: 62dB (hand calculated)

- **Pole1**(dominant): 4kHz, **Pole2**(non dominant): 100MHz (hand calculated)

- **GBW**: 4.8MHz(hand calculated)

- **Phase margin**: 82degree (hand calculated)

- **|PSRR|:** greater than 60dB

- **Iq**: 104uA

- **Efficiency:** 89.77%

Things I learnt from this Project

- This project helped me strengthen my concepts on Compensation, Pole zero Analysis and Stability.

- I learnt how to approach the design for the topology with Mosfets in saturation.

- Relearnt the concepts of small signal analysis and Transfer functions

- Improved my problem solving approach after many attempts.

- Learnt all the wrong approaches to do the design and learnt the correct way.

- Improved my concepts of Analog and avoid silly mistakes.

References

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Thank you