

# **Low Drop-Out Voltage Regulator using Open-Source SKY130PDK**

**Nithin P**

**3<sup>rd</sup> year, B.E (ECE)**

**June 9<sup>th</sup>, 2024**

Email: [nithinpurushothama@gmail.com](mailto:nithinpurushothama@gmail.com)

Linkedin: [Nithin Purushothama](#)

# Outline

---

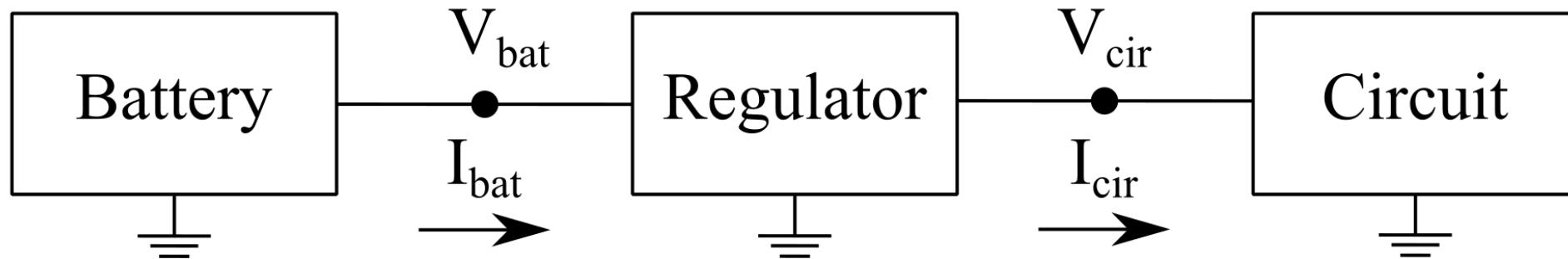
- Motivation
- Regulators and their Characters
- Feedback and Stability of a System
- Dominant Pole and Miller Compensation
- Design and Analysis
- Simulation Result
- Conclusion

# Motivation

---

- **Efficient Power Management:** Efficient power management is crucial in electronic devices, particularly those that are battery-operated.
- Design a robust Low drop out regulator that is stable and provides a constant output voltage for a variation in various parameters.
- Deepen my understanding of Analog IC design and Power management Integrated circuit.
- Design Industry standard PMICs

# Regulators



- Regulators provide regulated Output Voltage under varying  $V_{in}$  and  $I_{out}$ .
- There are 2 types of DC-DC Convertors:
  1. Switching Regulators
  2. Linear Regulators
- Here we mainly discuss about Linear Regulators.
- Linear Regulators achieve regulation by dropping Voltage.
- These have higher losses and their efficiency drops as Dropout( $V_{drop}$ ) increases.

# Regulator Characteristics

- Efficiency of LDO is dependent on Vdrop.

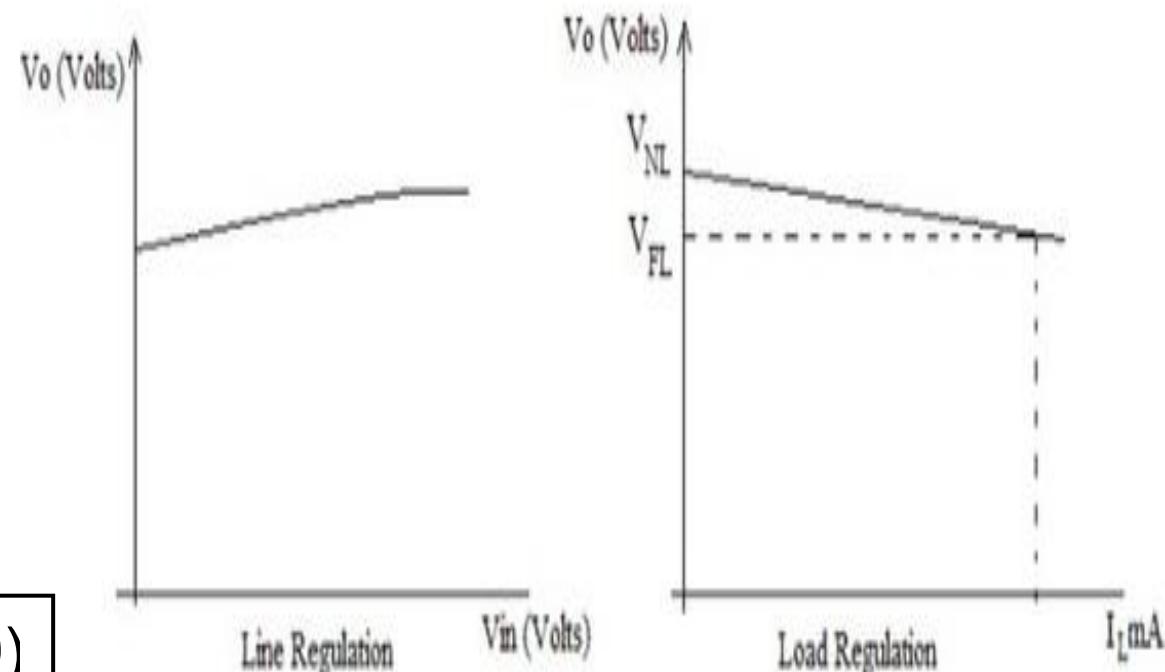
$$\eta = (V_{out} \cdot I_{out}) / (V_{in} (I_{out} + I_q)) * 100$$

- Load Regulation is change in Output Voltage wrt change in Load Current.

$$R_{out} = \Delta V_{out} / I_{out} \text{ (Ideally } R_{out}=0\text{)}$$

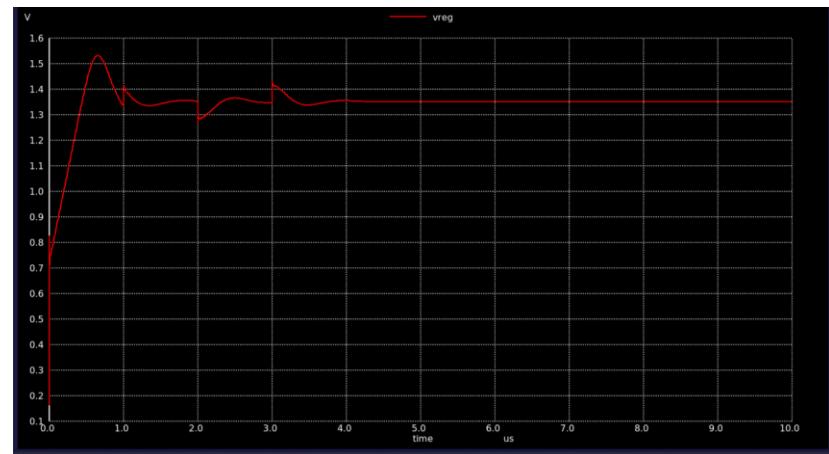
- Line regulation is change in Output Voltage wrt change in Input Voltage.

$$\text{Line Regulation} = \Delta V_{out} / V_{in} \text{ (Ideally L.R=0)}$$

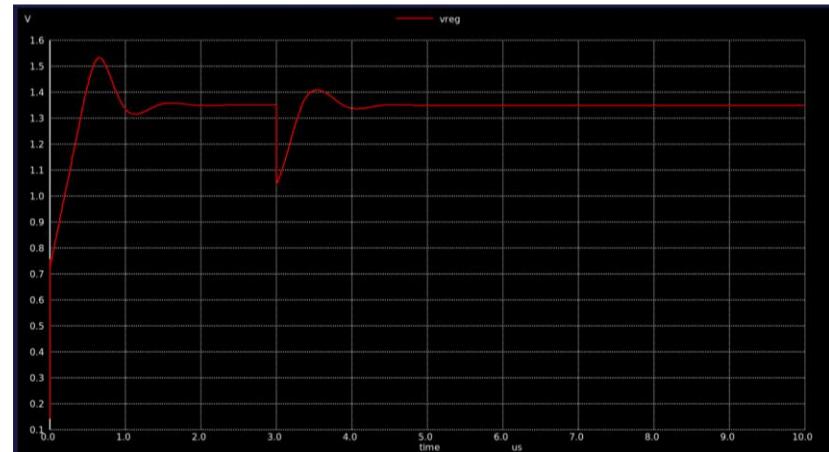


# Transient Character of LDO

- Line Transient of LDO, When there is an instantaneous change in  $V_{in}$ , the  $V_{out}$  also increases, but the negative feedback stabilizes it. So the settling time can be improved by improving the Bandwidth of the Loop.
- Load Transient of LDO, when there is an instantaneous change in  $I_{load}$ , the  $V_{out}$  decreases(because the Mpass is unable to provide instantaneous current so Current is drawn from  $C_L$  and the  $V_{reg}$  decreases), but the negative feedback stabilizes it.



Load Transient of LDO



Line Transient of LDO

# Feedback and Stability of a system

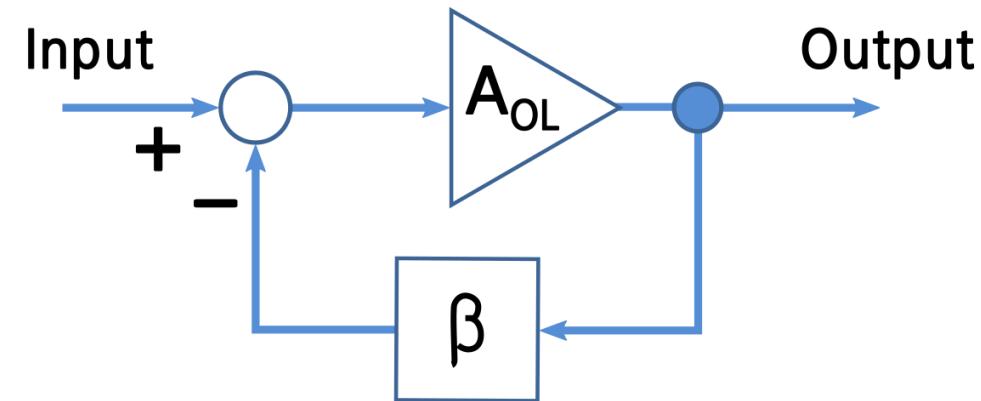
- **Negative Feedback:**

$$C.L.G = (L.G / (1 + L.G)) / \beta$$

C.L.G=Closed Loop gain

L.G= Loop gain

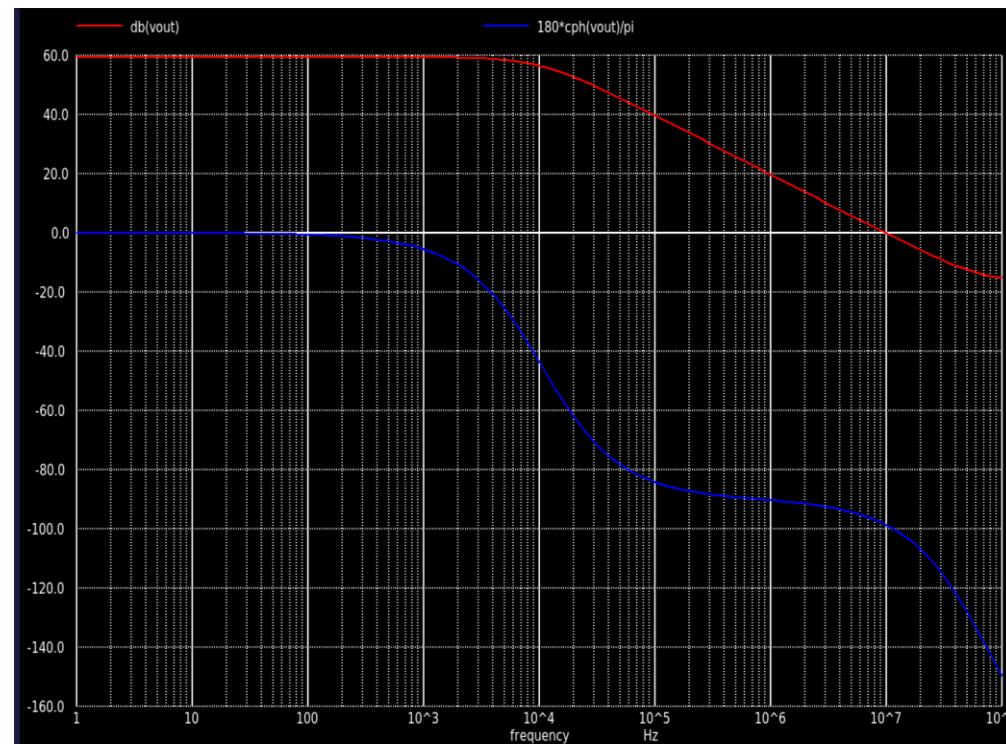
- For a system to be unstable  $L.G >= 1$  and phase has to be  $180^\circ$ .
- For a  $L.G <= 1$ , the signal will decay and It'll not oscillate.
- For 1<sup>st</sup> order system, it is always stable as long as pole in closed loop remains in Left half plain and the phase drop will never be more than  $90^\circ$ .



# Feedback and Stability of a system

- **2<sup>nd</sup> Order System**

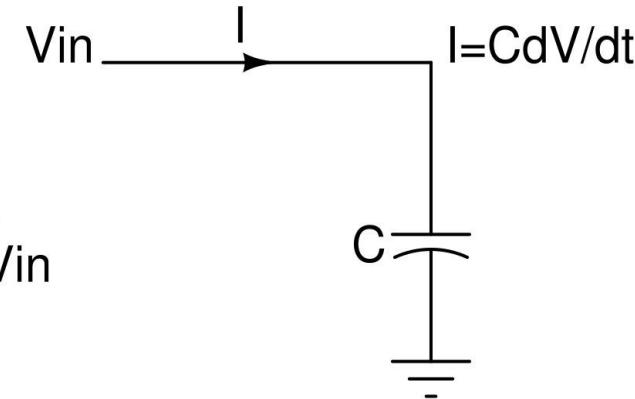
- In 2<sup>nd</sup> order system, there are 2 poles. -20dB/dec roll off of happens at the first pole and -40dB/dec roll off happens at the second pole.
- A good stable system requires a phase margin of  $\geq 60^\circ$ .
- This can be achieved by making the  $\omega_{p2}$  greater than  $\omega_{ugb}$ .
- We can achieve this by utilizing Dominant Pole compensation or Miller Compensation.
- Dominant pole can be achieved by putting a large capacitor at the node where we want dominant pole, this has its own advantages but for SoC application, its not that useful because of using large capacitors.



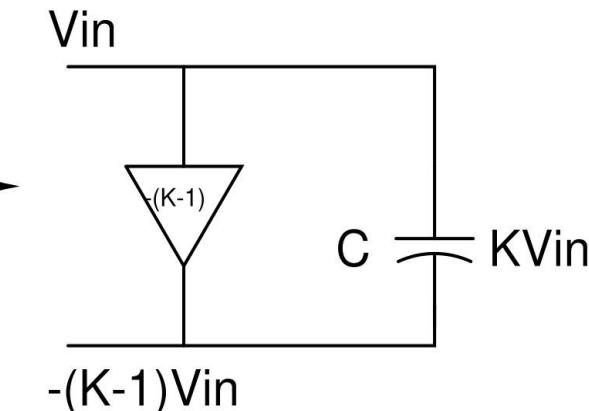
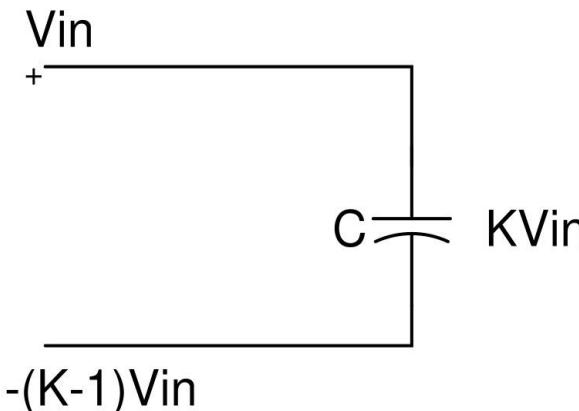
# Miller Compensation

- **Miller Compensation**
- Miller Compensation is very useful where we don't want to physically put a large capacitor.
- We can achieve the same thing by using the miller compensation.
- Miller Compensation ensures that we get a large capacitor without physically putting a large capacitor by placing a small capacitor in the feedback of the amplifier.

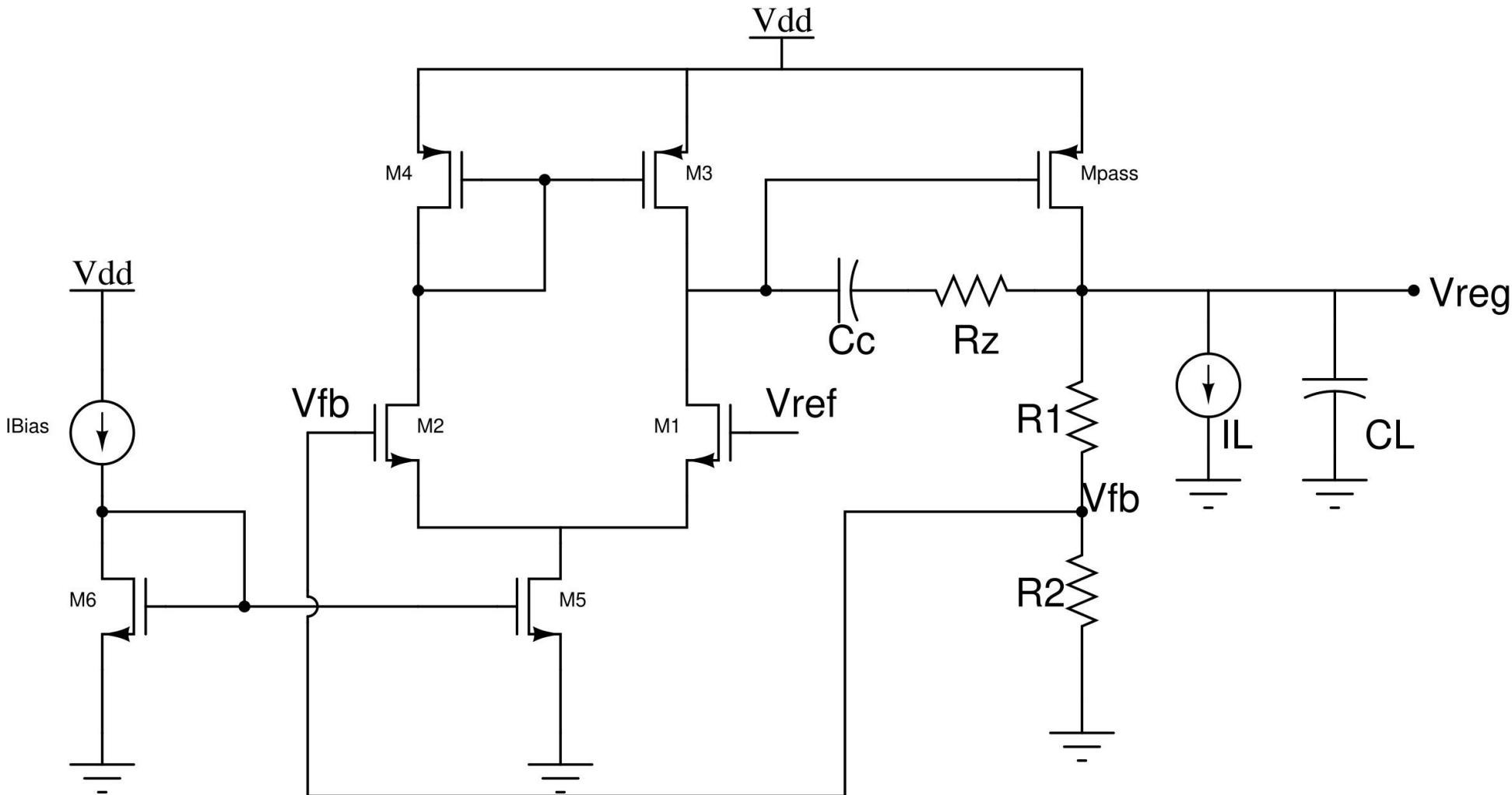
To Increase I to KI  
1. Increase C to KC  
2. Increase Vin to KVin



The above statement can be realised like this



# Intuitive Analysis of Poles and Zeros



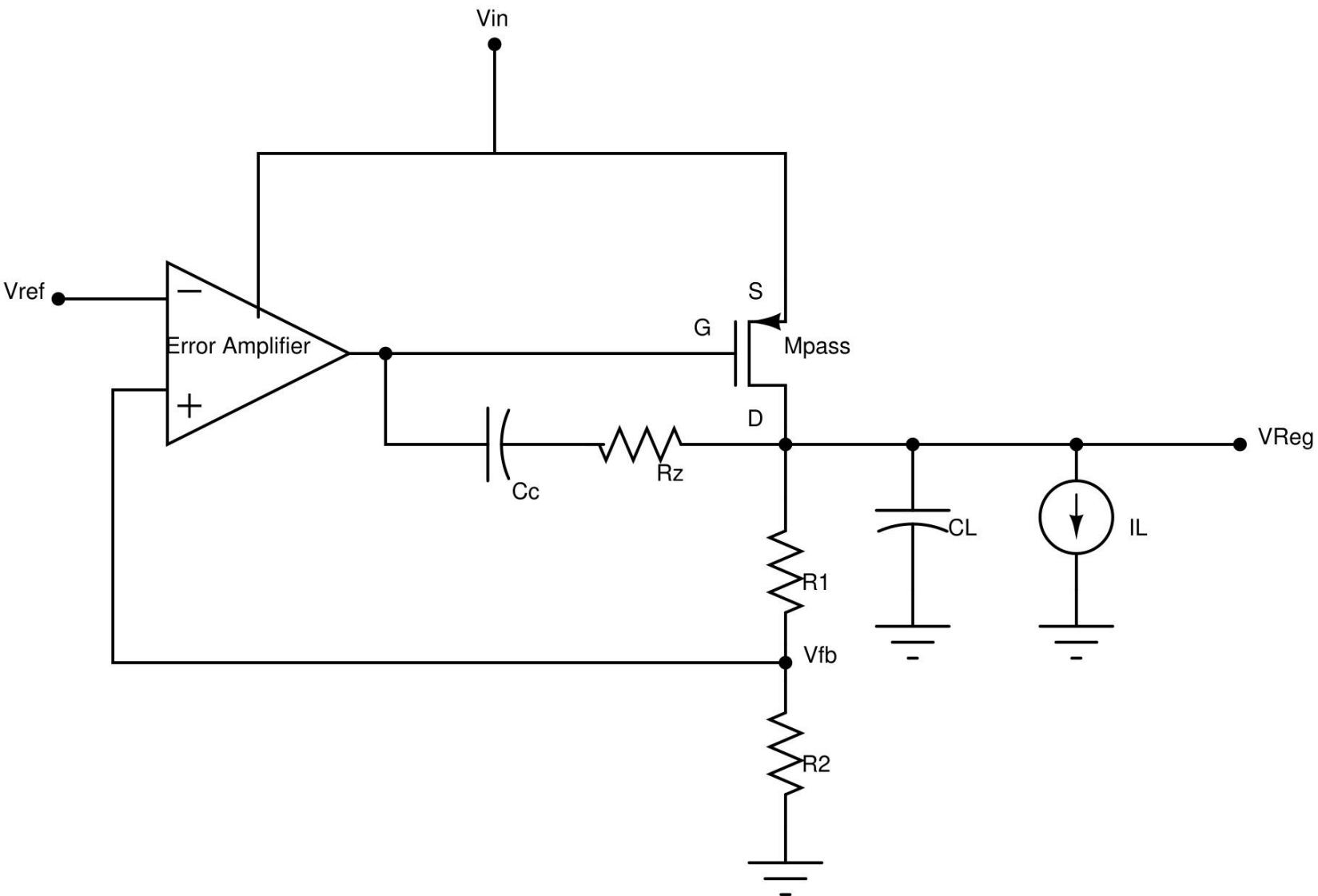
# Intuitive Analysis of Poles and Zeros

- **Poles and zeros of the proposed LDO**
- There are 2 major poles in this LDO
  1. Pole at the output of the Error amplifier.
  2. Pole at the output of the LDO.
- $\omega_{p1} = 1/((rds1||rd3)(C_{gg}+Cc(A2+1))) \rightarrow \text{Dominant Pole}$
- $\omega_{p2} = 1/((rdspass||R1+R2||RL)(C_{out})) \rightarrow \text{Non Dominant Pole}$
- Where  $A1 = gm1(rds1||rds3)$  and  $A2 = -gmpass(rdspass||R1+R2||RL)$ .
- $\omega_z = 1/((1/gmpass)-Rz)Cc$ , If we make  $Rz \gg 1/gmpass$  then  $\omega_z$  comes in Left half plane. So we nullify the effect of Right half Plane(because of R.H.P zero is phase lagging)
- Loop gain(s) =  $-A1*A2*(1-s/\omega_z)/(1-s/\omega_{p1})(1-s/\omega_{p2})$

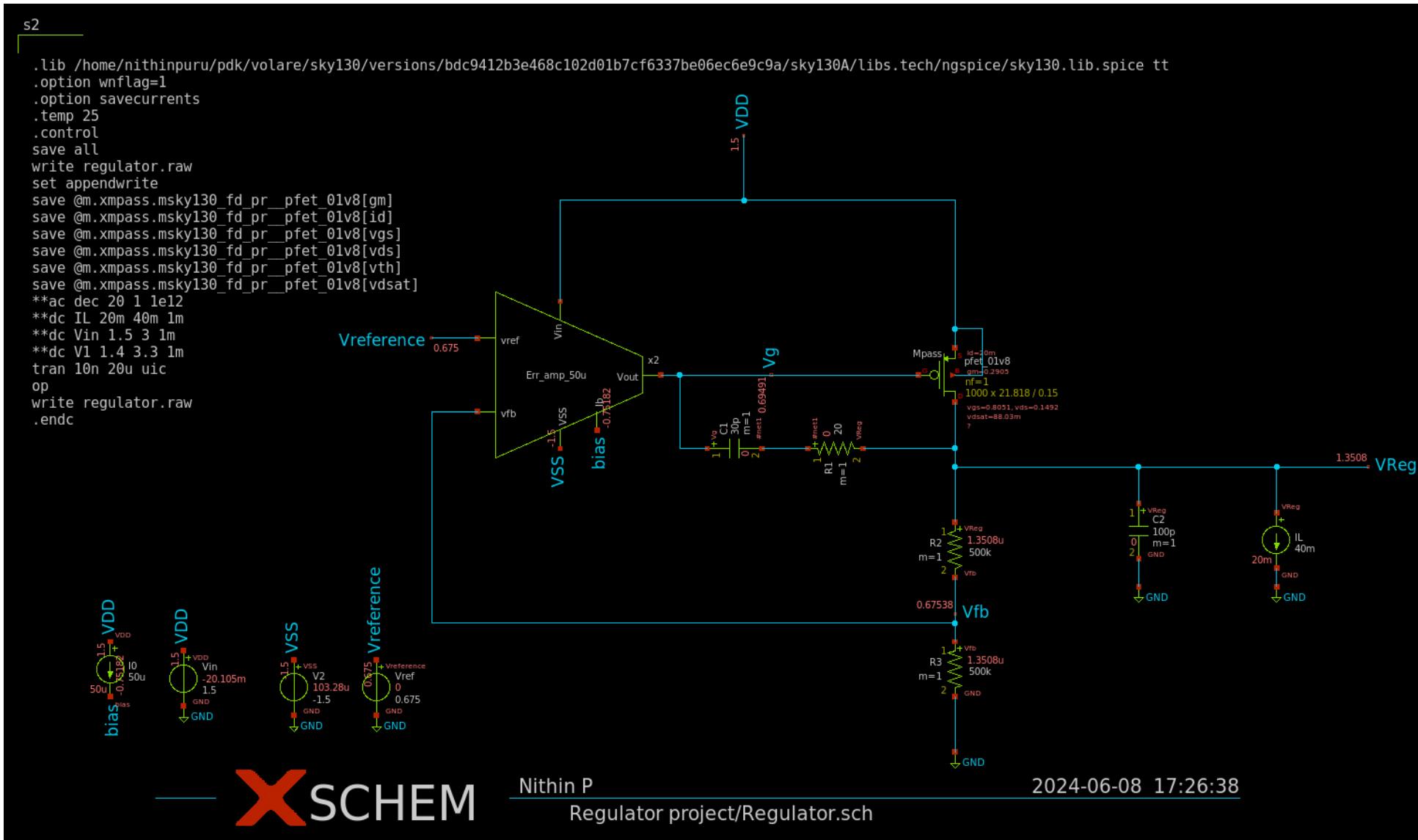
# Specification

Specs	Description	Value
Vin(max)	Maximum input voltage range	3V
Vin(min)	Minimum input voltage range	1.5V
VDO	Dropout voltage for 40mA load current	150mV
IQ	Quiescent current(no load current) (Vin=3V)	<=50uA
Tset(Load)	Average of settling time to +/-1% of final value of 20mA to 40mA and 40mA to 20mA load changes(100ns rise and fall time)	<=1us
Tset(Line)	Average of settling time to +/-1% of final value for $\Delta$ Vin from 2V to 3V and 3V to 2V for 10mA load(100ns rise and fall time)	<=2us
PSRR	Magnitude of power supply rejection (Vout/Vin) at 100Hz(10mA)	>=60dB
Isc	Short circuit current with 10ohm Load resistor (Vin=3V)	<=50mA
PM	Phase margin of main feedback loop(10mA)	>=60deg
Efficiency	Efficiency for full load and Vin=1.5V	>=90%
WC+ Vout	Max Vo variation with 10mA load(Vin=1.5-3V, -40C<=T<=125, Process	1.36V-1.34V

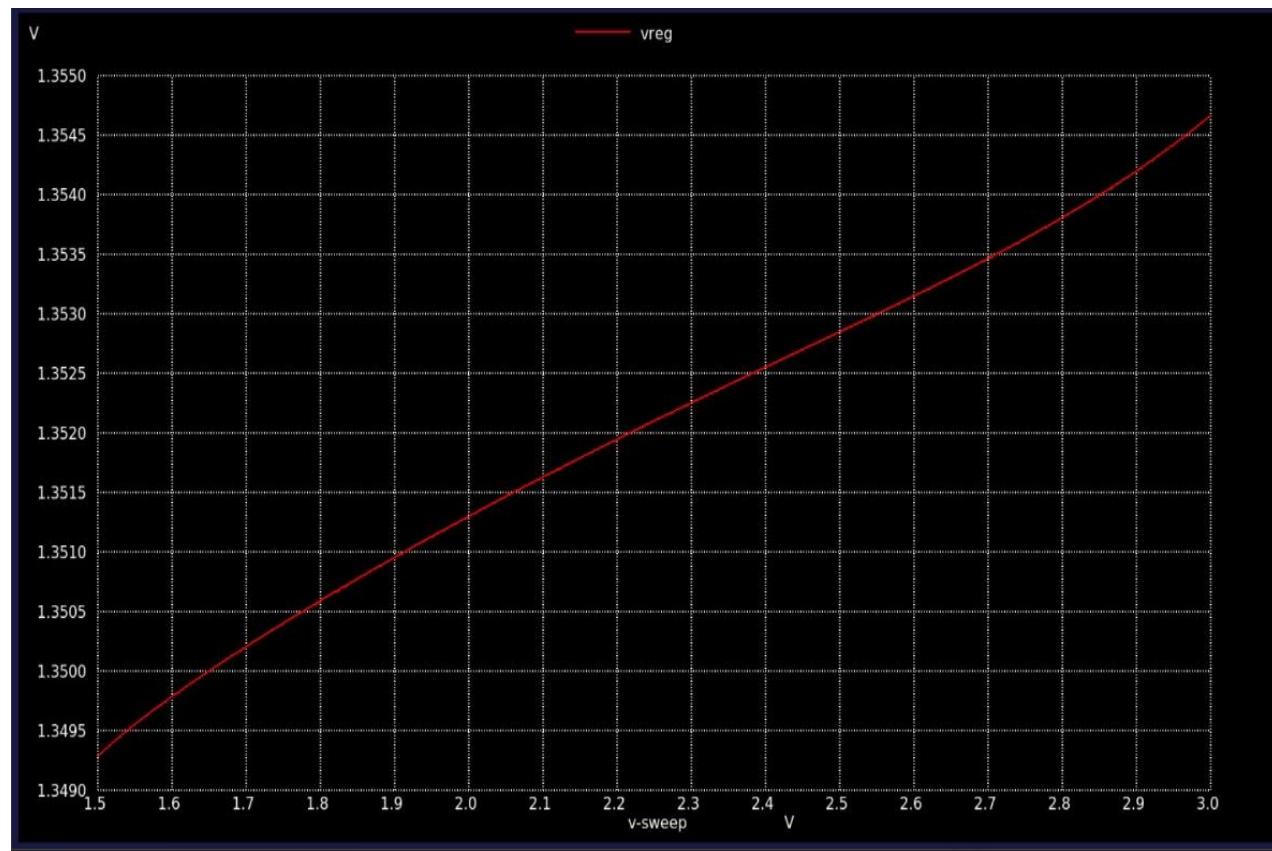
# Circuit Diagram



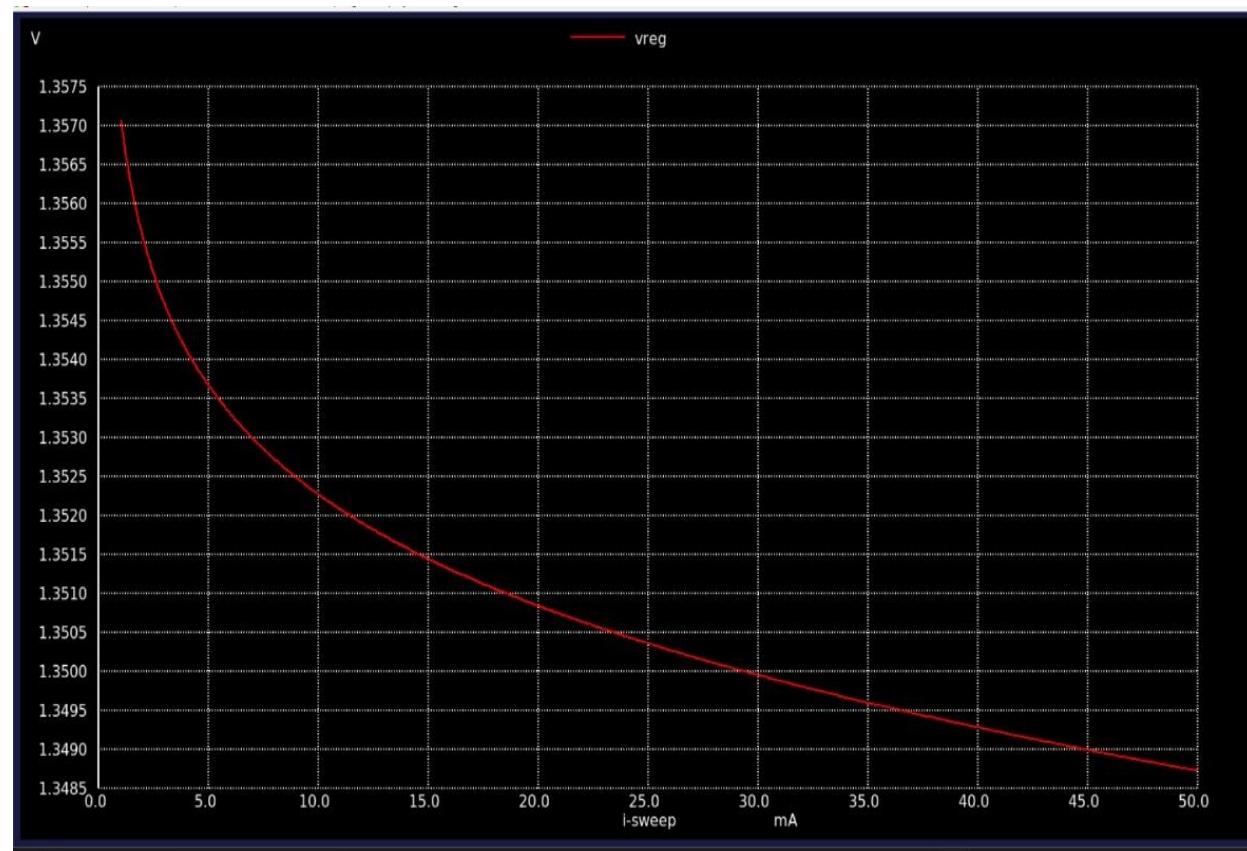
# Schematic



# Simulation Results

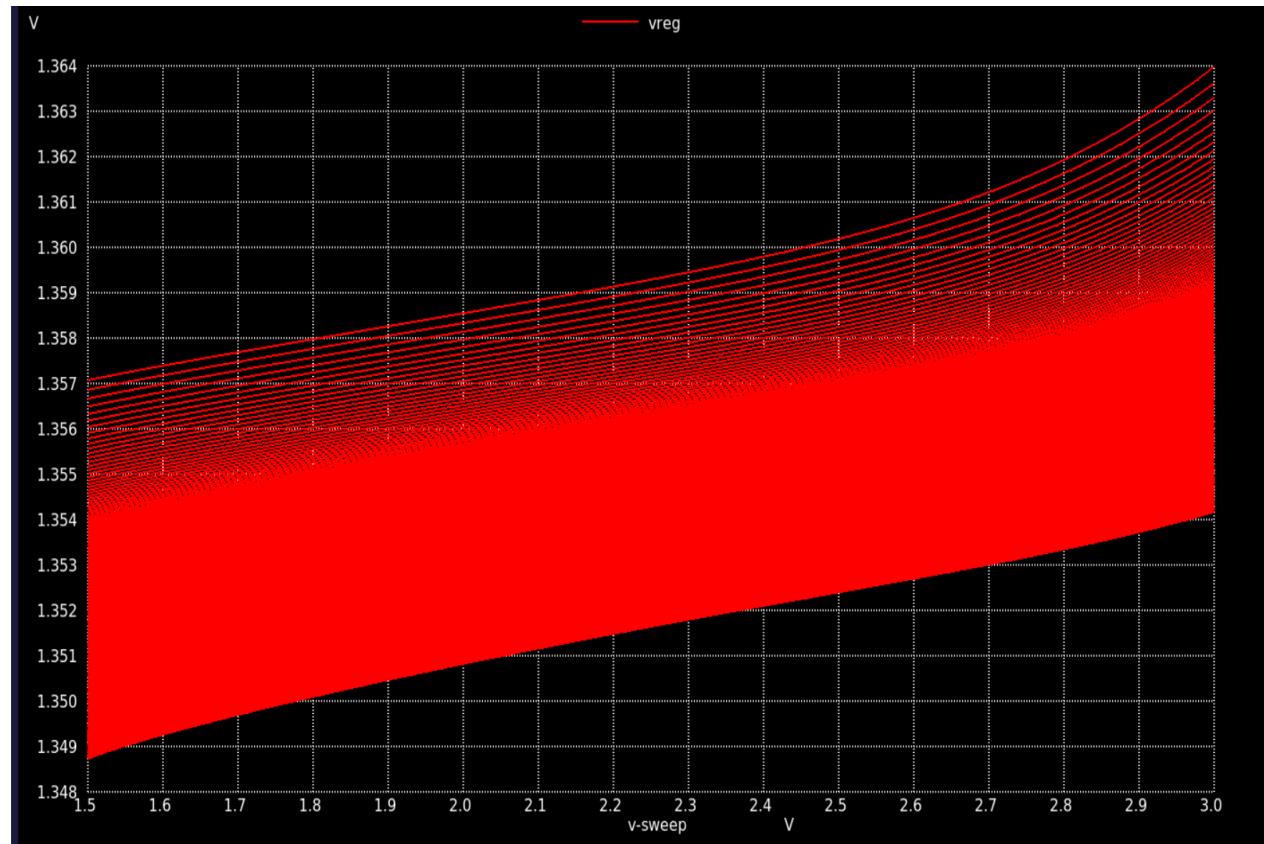


Line regulation of the LDO, max variation observed  
is 5mV

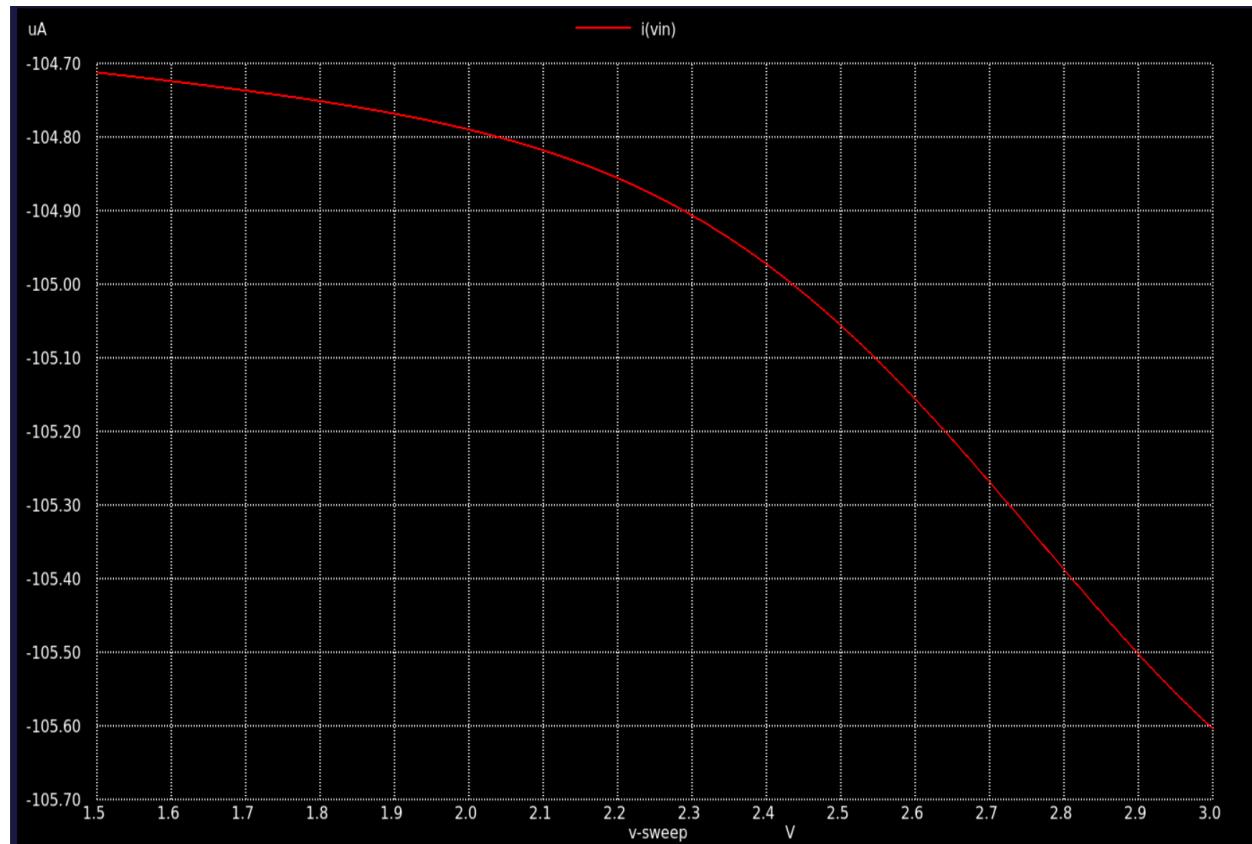


Load regulation of the LDO, max variation observed  
is 8mV

# Simulation Results

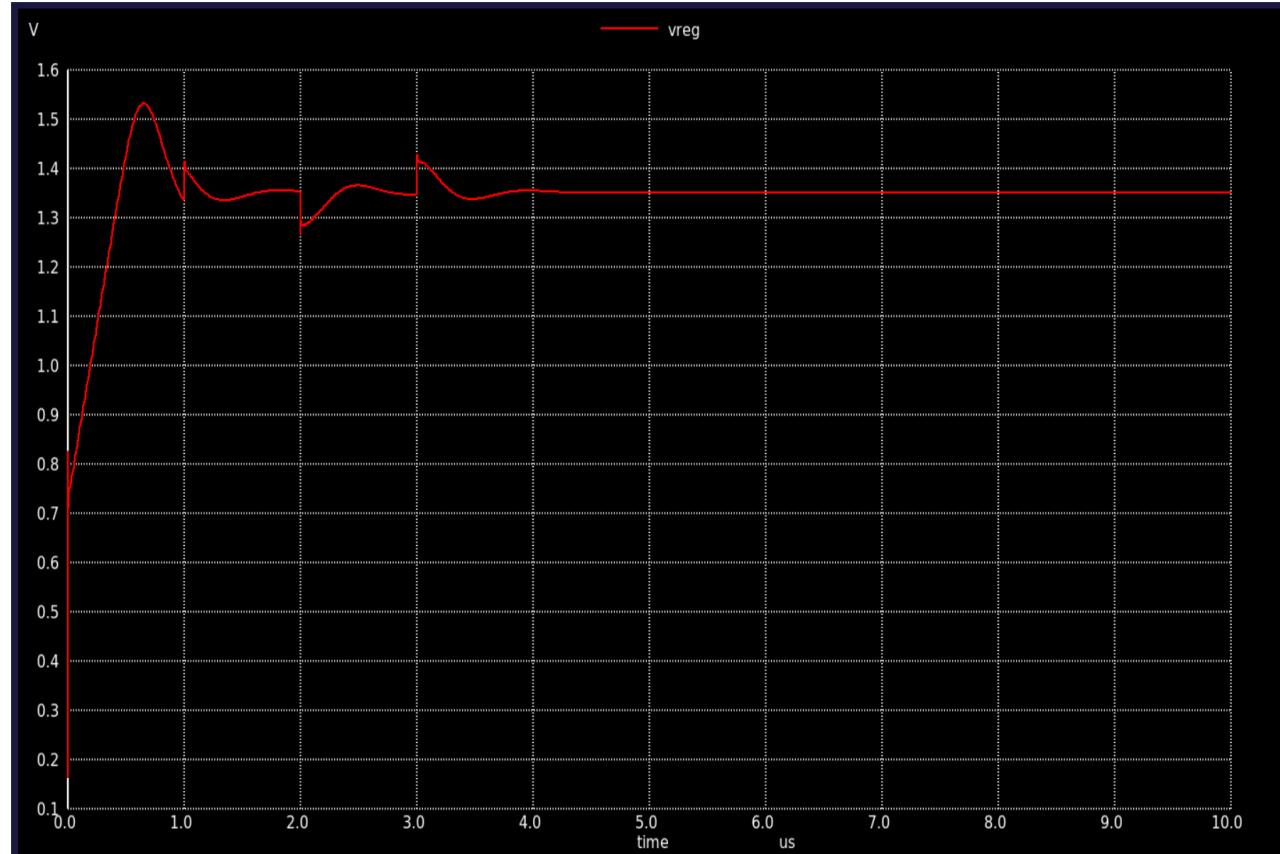


Line+Load regulation of the LDO, max variation observed is 15mV

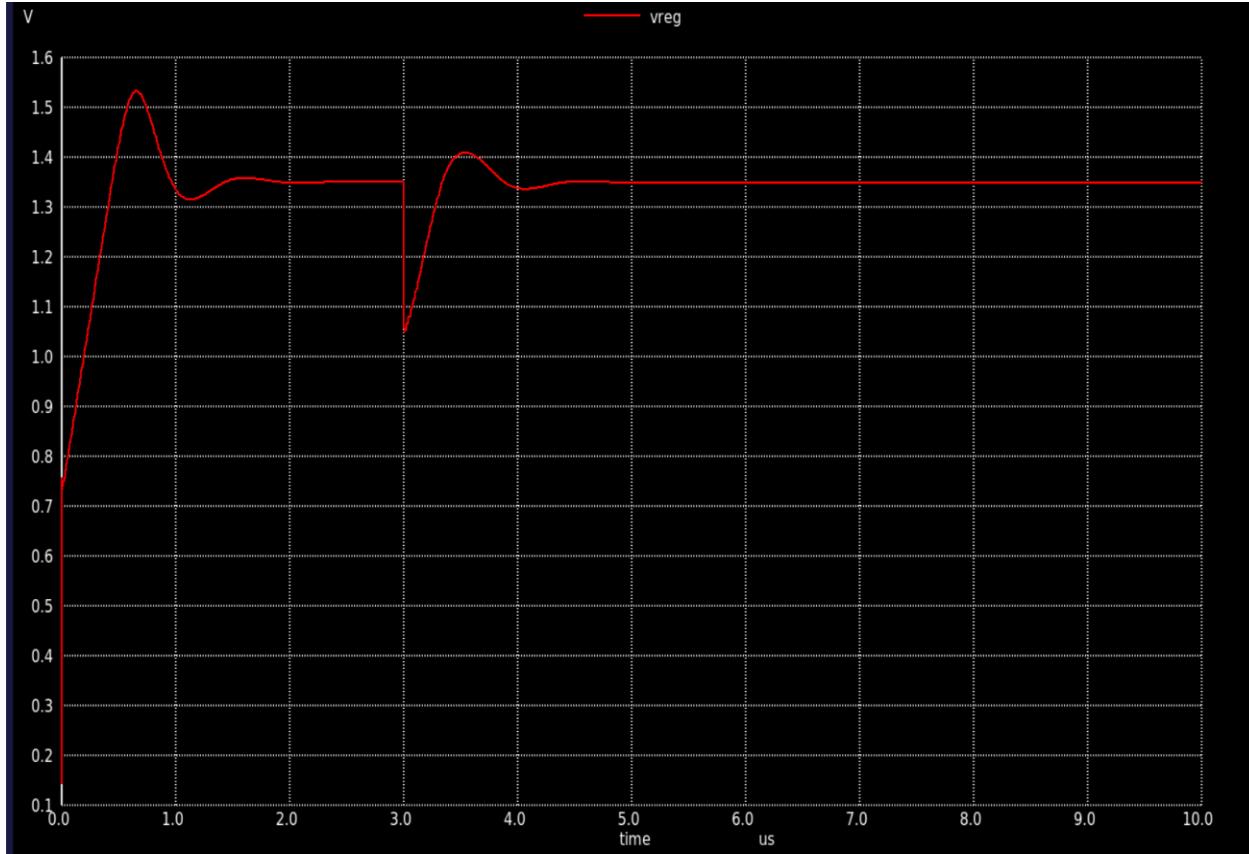


Quiscent Current of the LDO

# Simulation Results

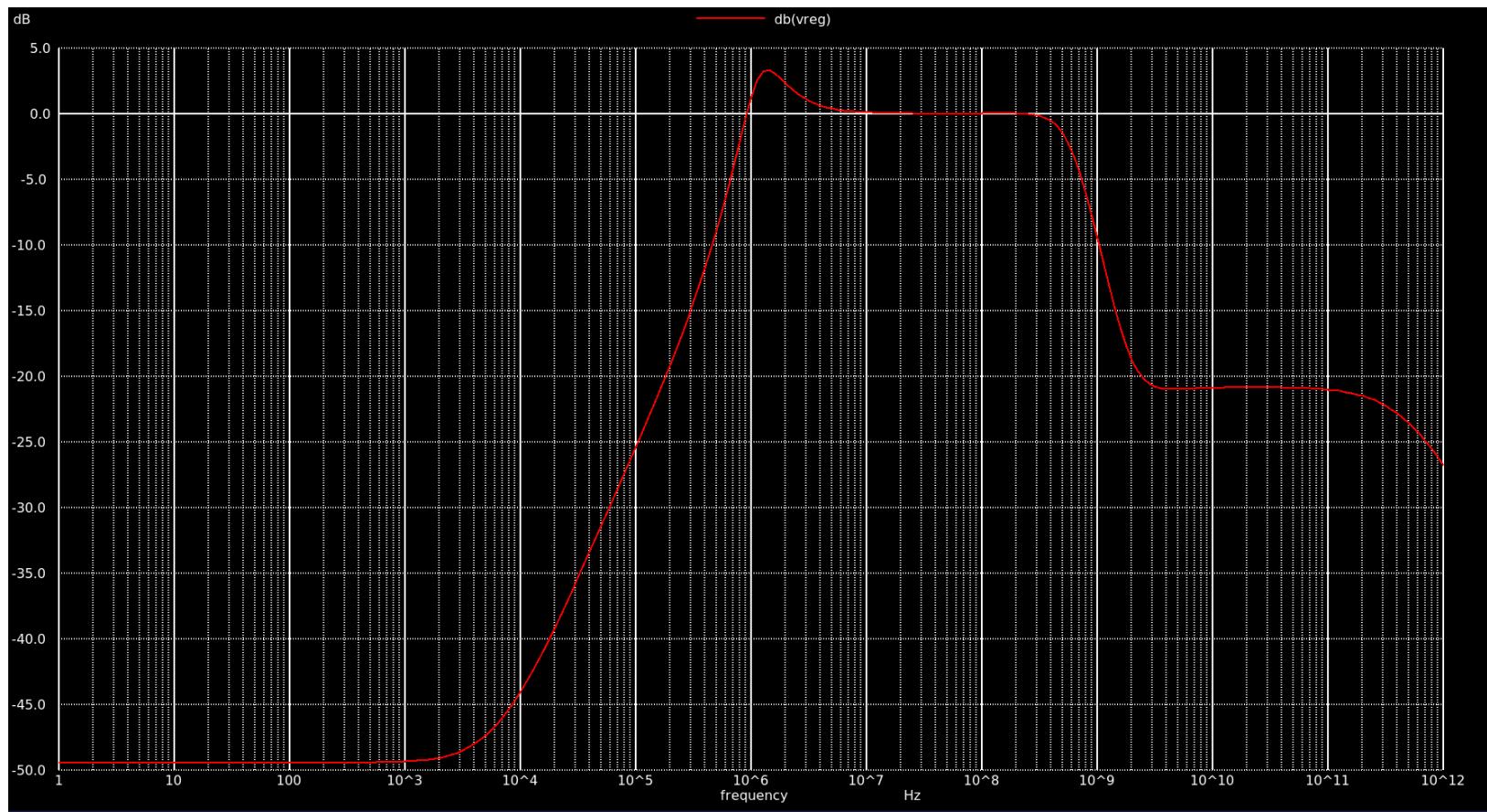


Load Transient of the LDO, the observed tset is  
2usec



Line Transient of the LDO, the observed tset is  
2usec

# Simulation Results



PSRR of the LDO is observed around 50dB

# Conclusion

---

- Gain: 57dB
- Pole1(dominant): 4kHz,
- Pole2(non dominant): 100MHz
- GBW: 4.8MHz
- Phase margin: 82degree
- |PSRR|: 50dB
- Iq: 104uA
- Efficiency: 89.77%

# Design Improvement

---

- Use a Folded cascode Error Amplifier to provide more gain and Improvement in PSRR
- Iq (Quiescent current) can be improved by choosing a better Error amp topology which have higher slewrate and lower Iq.
- The settling time can be improved by increasing the bandwidth of the loop.

# References

---

- [1]. A Low Drop Regulator (LDO) in UMC 180 nm Technology by Mohammed Rizwan
- [2]. Low Drop-Out Voltage Regulators: Capacitor-less Architecture Comparison by Joselyn Torres, Mohamed El- Nozahi, Ahmed Amer, Seenu Gopalraju, Reza Abdullah, Kamran Entesari, and Edgar Sánchez-Sinencio.
- [3]. Full On-Chip CMOS Low-Dropout Voltage Regulator Robert J. Milliken, Jose Silva-Martínez
- [4]. IC Design of Power Management Circuits (IV) Wing-Hung Ki Integrated Power Electronics Laboratory ECE Dept., HKUST Clear Water Bay, Hong Kong.
- [5]. Design of low-dropout voltage regulator Miroslav Čermák.
- [6]. LDO Linear Regulator to Charge Battery by Ahmed tawfiq.

Thank you

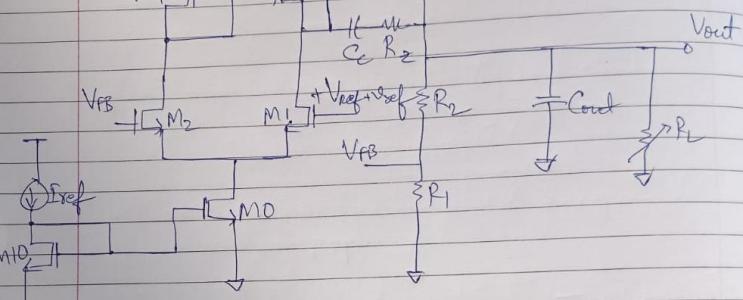
# **Back up Slides**

Credits: Amit Bar

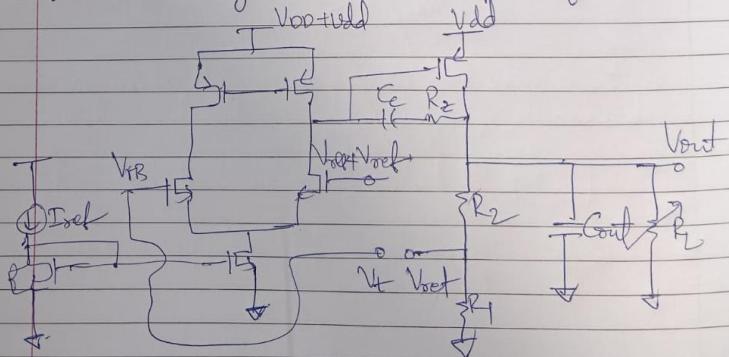
### Finding Poles and Zeros of LDO Intuitively

$V_{dd} + V_{dd}$

$M_3$



To find whether the feedback is +ve or -ve, we put a huge impedance node at the feedback and apply small signal  $V_{test}$  and cover the loop and check what's coming back at the other part of node



25/04/23

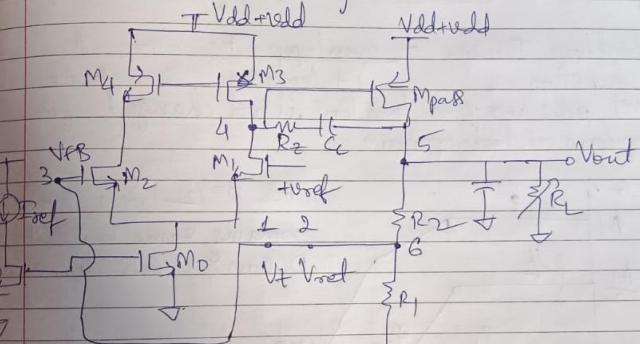
Page No.

Date

Find loop gain =  $\frac{V_{out}}{V_{test}}$  is negative

$$\text{loop gain} = \frac{V_{out}}{V_{test}} < 0 \quad [\text{negative}] \text{ so -ve feedback}$$

Now let's do it intuitively.



If we increase voltage at  $V_1$

→ For  $M_2$ , if we increase gate voltage, small signal source voltage will increase, so the source of  $M_1$  voltage also increases

→ If we increase source of  $M_1$ , drain of  $M_1$  also increases. b/c it becomes common gate config.

→ So voltage at Node 5 also increases

→ Then gate voltage of PMOS Mpass increases the drain voltage decreases b/c its common source config of PMOS

→ Then node 5 voltage decreases the combo of  $R_2$  &  $R_1$  becomes voltage divider, then voltage at node 6

### U.G.B → Unity Gain Bandwidth

Page No.

Date

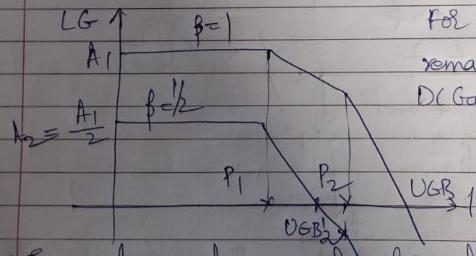
Voltage decreased then voltage at node 2 also decreases  
→ So when we increase voltage at node 1 after travelling the nodes the voltage at node 2 is decreasing, so this is a negative feedback.

[LG] Loop Gain: [open loop gain x feedback factor]  $[A_f]$

→ If we know E.G we can directly find closed loop behaviour

$$\text{closed loop Transfer function} = \frac{\text{open loop T.F.}}{1 + \text{loop Gain}} = \frac{A}{1 + A_f}$$

→ W.L.K poles and zeros location is not changed for loop gain and open loop gain



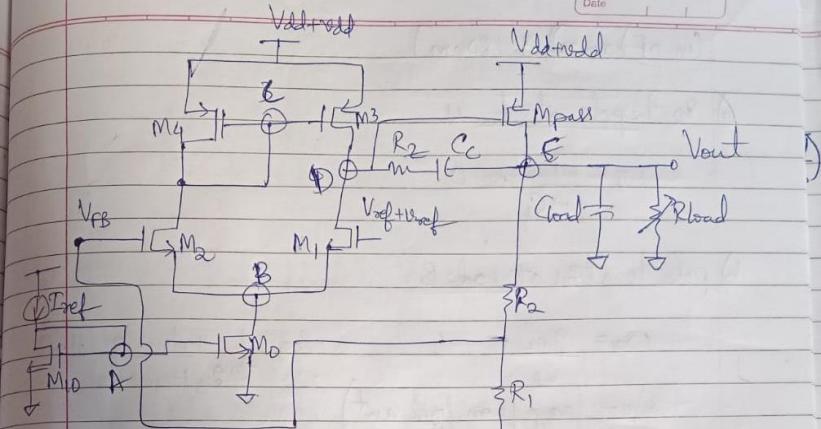
for  $\beta = 1/2$  P<sub>1</sub> & P<sub>2</sub> location remains same but the DC Gain & U.G.B is decreased

→ Even if we decrease  $\beta$  poles and zeros locations are unchanged but DC Gain & U.G.B is decreased

$$A_2 = \frac{A_1}{2} \quad \& \quad UGB_2 = \frac{UGB_1}{2} \quad [\text{for } \beta = 1/2]$$

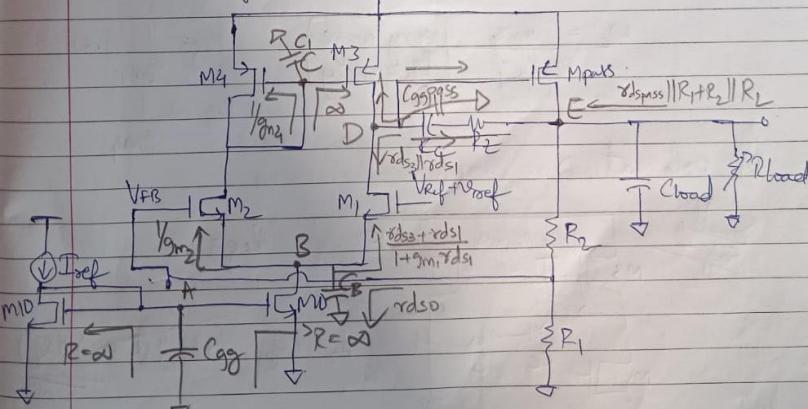
→ W.L.K every top node containing a pole

$M_3, M_4 \rightarrow$  identical  
 $M_1, M_2 \rightarrow$  identical



→ There are 5 nodes so there can be max 5 poles

→ For small signal  $V_{dd+V_{dd}}$



→ For small signal  $I_{ref} =$  open ch. and  $\beta$  looking at  $M_{10}$  &  $M_0$  are  $\omega$  and also  $C_{gg}$  of  $M_{10}$  &  $M_0$  is present (gate-to-ground capacitance) which is large.

(in pF range for 180nm)

a) So the pole at A is

$$\omega_A = \frac{1}{(g_m) C_g} \approx 0$$

b) pole location at node B.

$$\omega_B = \frac{g_{m2}}{C_B}$$

$\omega_B \rightarrow$  large (non dominant) frequency pole

$$R_{eq} = \frac{1}{g_{m2} (r_{ds2} + r_{ds1}) \| R_2 \| R_L}$$

$$R_{eq} \approx \frac{1}{g_{m2}}$$

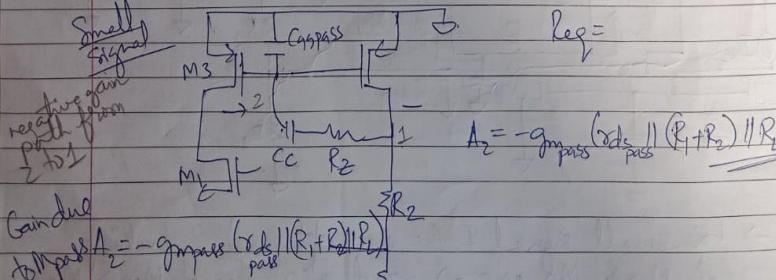
c) pole at C

$$\omega_C = \frac{g_{m4}}{C_C} \quad \text{(very large frequency)}$$

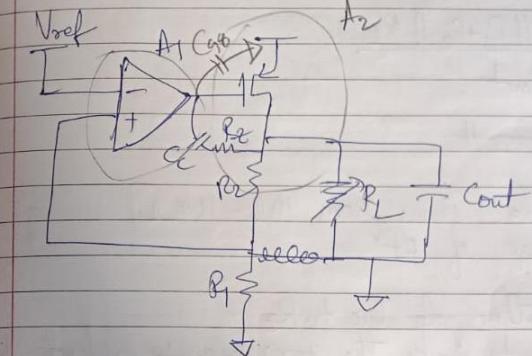
$$R_{eq} = \frac{1}{g_{m4}} \| \omega$$

$$R_{eq} \approx \frac{1}{g_{m4}}$$

d) pole at D.



This is common source config of  $M_{pass}$  and gain is negative



→  $A_2$  is negative gain so the  $C_c$  experience effect, so  $C_c$  is miller cap

$$C_{eq,D} = C_{gg} + C_c (A_2 + 1)$$

$$\omega_D = \frac{1}{(r_{ds2} + r_{ds1}) (C_{gg} + C_c (A_2 + 1))}$$

Large Impedance / Large Capacitance

so  $\omega_D$  becomes lower frequency

WKT

$$A_1 = g_{m1} (r_{ds3} + r_{ds1})$$

$$A_2 = -g_{m2} (r_{ds3} + r_{ds1}) \| (R_1 + R_2) \| R_L$$

e) pole at node E

$$R_{eq,E} = r_{ds3} \| (R_1 + R_2) \| R_L$$

$$C_{eq,E} = C_{out}$$

$$\omega_c = \frac{1}{R_{\text{pass}} + R_2 + R_L}$$

Cout

$$R_{\text{pass}} = \frac{1}{\omega_c C_{\text{out}}}$$

$R_L$  is variable [vary from 10Ω - 10MΩ]  
 $C_{\text{out}}$  in range of  $\mu F$

- There is another pole due to  $R_2$
- we added  $R_2$  to make the zero because present below of the ~~pass~~  $C_C$ , To nullify zero, we add  $R_2$

pole due to  $R_2$

$$R_{\text{eff}} = R_2, C_{\text{eq}} = \left( \frac{1}{C_C} + \frac{1}{C_{\text{gg}}} + \frac{1}{C_{\text{out}}} \right)$$

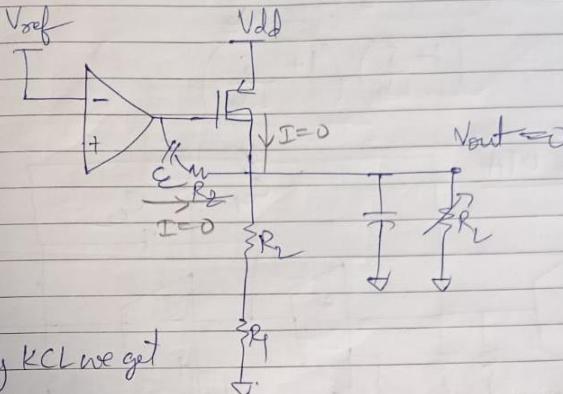
$$P_{R_2} = \frac{1}{R_2} \left( \frac{1}{C_C} + \frac{1}{C_{\text{gg}}} + \frac{1}{C_{\text{out}}} \right)$$

This  $P_{R_2}$  is very high frequency.

So there are total 6 poles and 1 zero

→ To find zero, for input = zero, output = 0

To find zero



Apply KCL we get

$$\omega_2 = \frac{1}{\left( \frac{1}{C_{\text{gg}}} + R_2 \right) C_C}$$

→ If we make  $R_2 > \frac{1}{C_{\text{gg}}}$  then  $\omega_2$  comes in left half plane

→ So we nullify the effect of R.H.P [because R.H.P zero is phase lagging]

→ pole at A the node will not be coming at signal path (bcz its bias path). So pole at A is not an important pole

→ So we get effective pole 2, one due to  $R_2$  and other at the output

→ So 2 effective pole ( $\omega_2, \omega_e$ )

dominant pole  
non dominant pole

one zero ( $\omega_2$ )

$$\text{Loop Gain}(s) = (-A_1 A_2) \times \left( 1 - \frac{s}{\omega_2} \right)$$

$$\left( 1 + \frac{s}{\omega_b} \right) \left( 1 + \frac{s}{\omega_e} \right)$$