Chipathon 2025
Team Nirvana

Team Project :

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5. Amit Kumar Sharma

Contents

Team Nirvana

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Team lead and Layout

Nithin Purushothama
Design and Architecture

Kelton Eckert
Design of Building Block

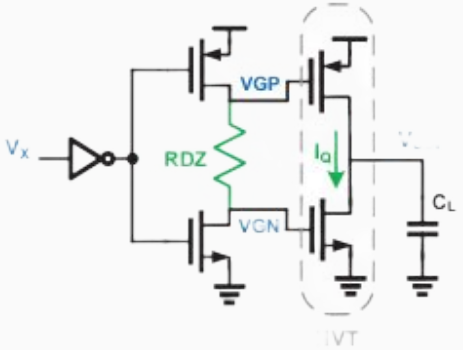
Kandias Wardhana
Layout

Amit Kumar Sharma
Design of Building Block

01

Reconfigurable **Fully Differential Ring Amplifier** with **Deadzone Regulation Circuit** for **Educational and RF-Mixed-Signal Applications**

Dynamic Amplifier, especially **Ring Amplifier**, have emerged as compelling alternatives to traditional small-signal operational amplifiers due to their high-speed and energy-efficient characteristics. Originally proposed by Benjamin Hershberg at Oregon State University (OSU), ring amplifiers offer an innovative solution for high-performance analog blocks, especially in pipelined or SAR ADCs and filter circuits.



Ring Amplifier using resistor for deadzone biasing, source from ieeexplore.ieee.org/abstract/document/8351242/

Design Purposes

01

Optimized for educational uses and mixed-signal integration

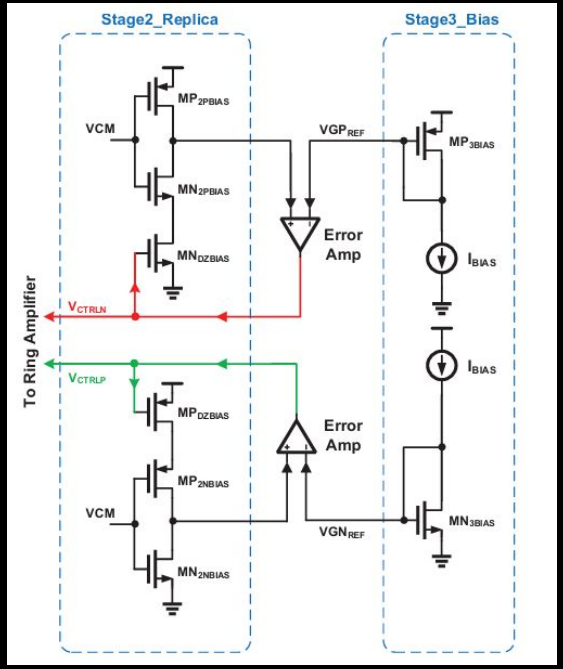
02

Enabling user-driven exploration and understanding of Ring Amplifier operation

03

Understanding the operation of large-signal dynamics, deadzone behaviour, and transition into small-signal behaviour

Reconfigurable Parts:
Dedicated Deadzone Regulation



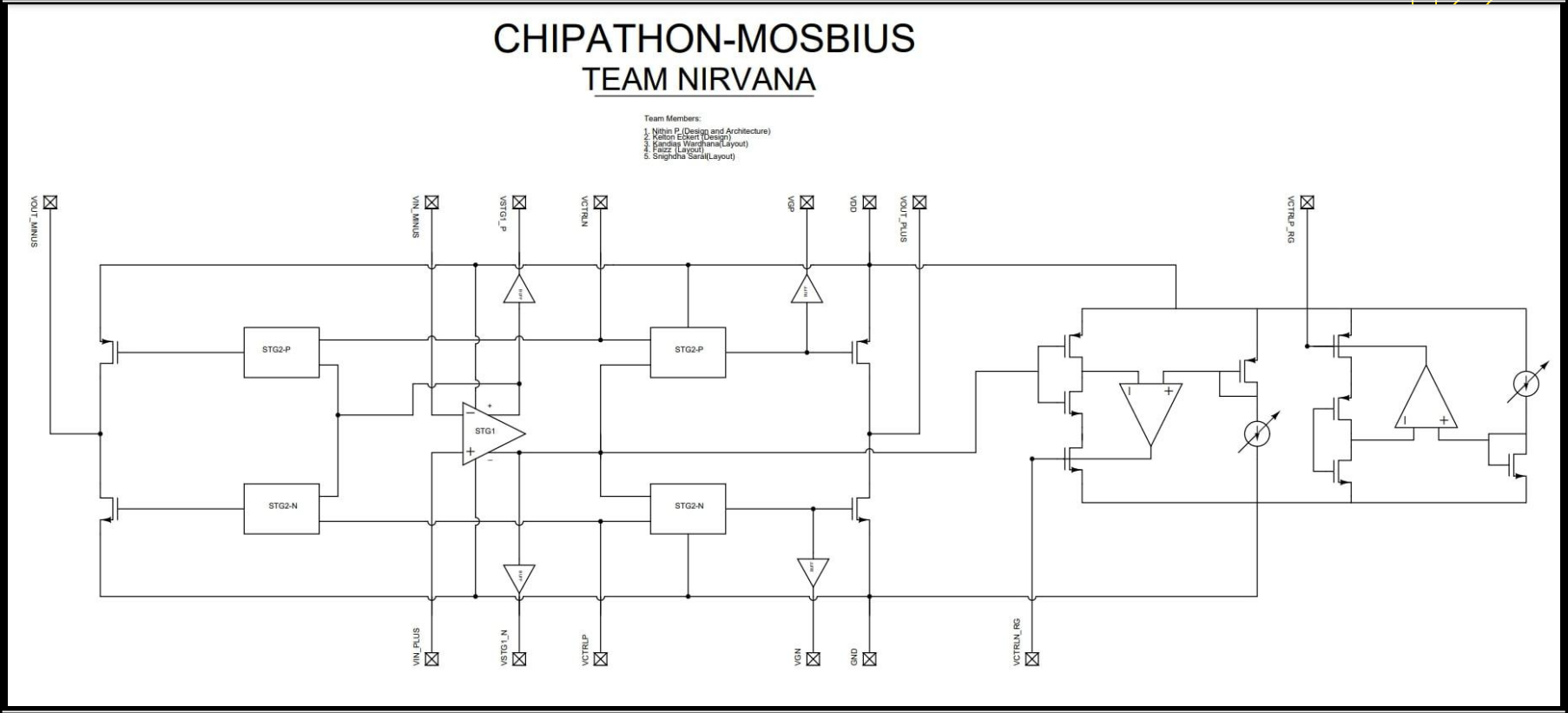
source from ieeexplore.ieee.org/abstract/document/8351242/

For needing a robust deadzone biasing to maintain an output stage across process variation, there is an proposed Deadzone Regulation Circuit

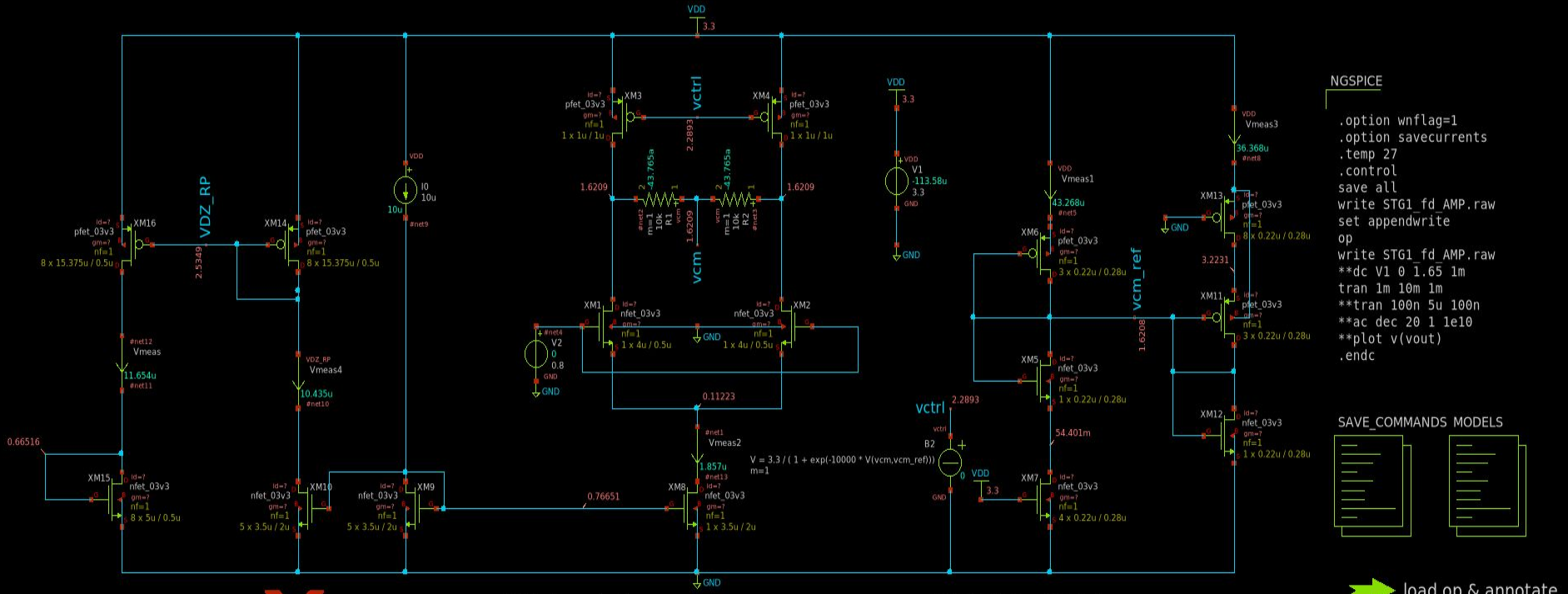
Deadzone Regulation Circuit contains of a Stage2_Replica and a error amplifier for a negative feedback loop, and also a Stage3_Bias

This Dedicated Deadzone Regulation Circuit allows fine control over the amplifier's transition between nonlinear and linear operating region. This tunability makes our implementation suitable for multiple cases while also serving as a pedagogical platform for analog circuit learns

Architecture



Stage 1: Ring Amp



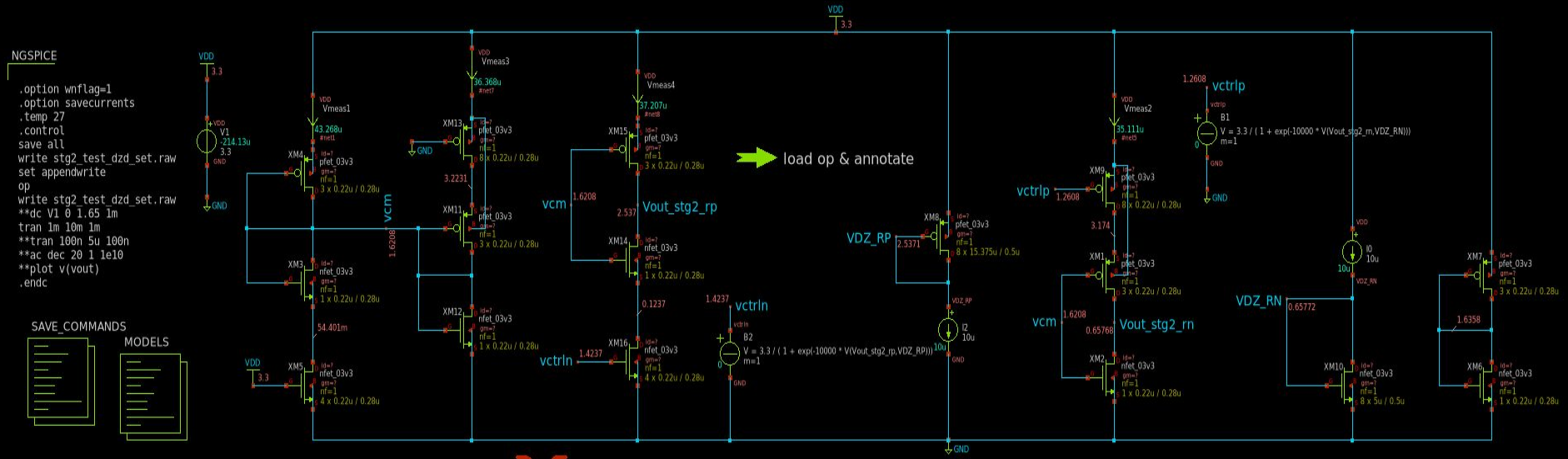

```
NGSPICE

.option wnflag=1
.option savecurrents
.temp 27
.control
save all
write STG1_fd_AMP.raw
set appendwrite
op
write STG1_fd_AMP.raw
**dc V1 0 1.65 1m
tran 1m 10m 1m
**tran 100n 5u 100n
**ac dec 20 1 1e10
**plot v(vout)
.endc
```

SAVE_COMMANDS MODELS

load op & annotate

Stage 2: Ring Amp

Stage-2 Ring Amplifier design Testbench



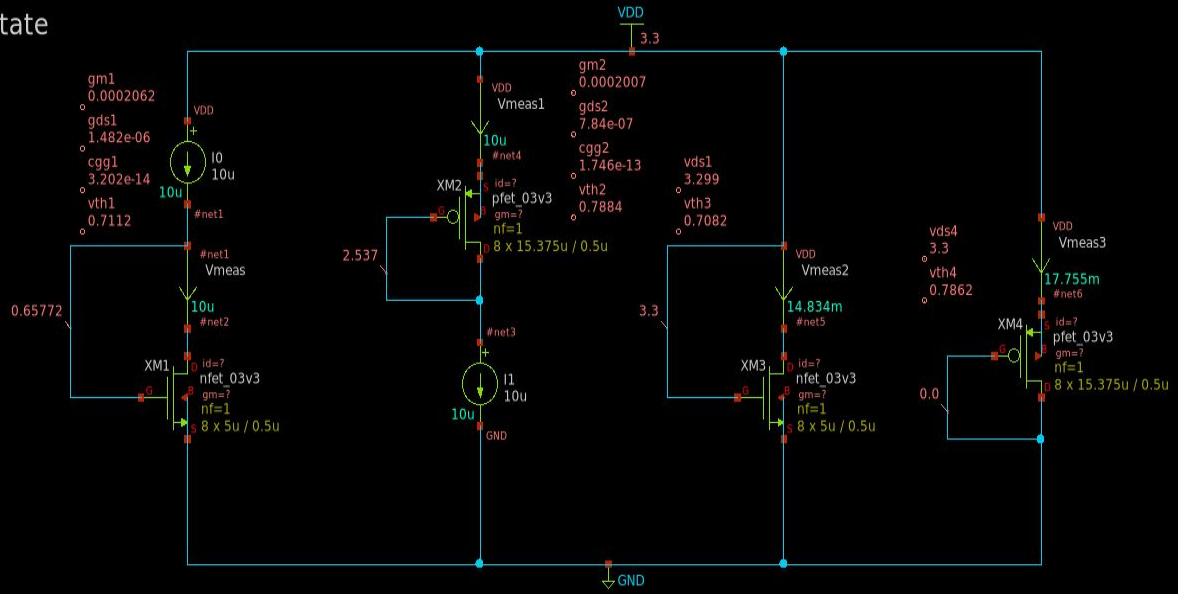
Load Cap: 250pF
BW: 50MHz
Gm3: 400uS
A1A2: 200
VDD: 3.3V

Stage-3 Ring Amplifier design Testbench

NGSPICE

```
.option wnflag=1
.option savecurrents
.temp 27
.control
save all
write stg3_test_dzd.raw
set appendwrite
op
write stg3_test_dzd.raw
**dc V1 0 1.65 1m
tran 1m 10m 1m
**tran 100n 5u 100n
**ac dec 20 1 1e10
**plot v(vout)
.endc
```

load op & annotate



SAVE_COMMANDS

MODELS

XSCHEM

Nithin Purushothama

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chipathon/Ring-amp/STG3/stg3_test_dzd.sch

Specification

Parameter	Min.	Tipical	Max
VDD	-	3.3 V	-
Bandwidth	-	-	50 MHz
Load Capacitor	-	250 pF	-
Settling Time	-	-	=<50 nS

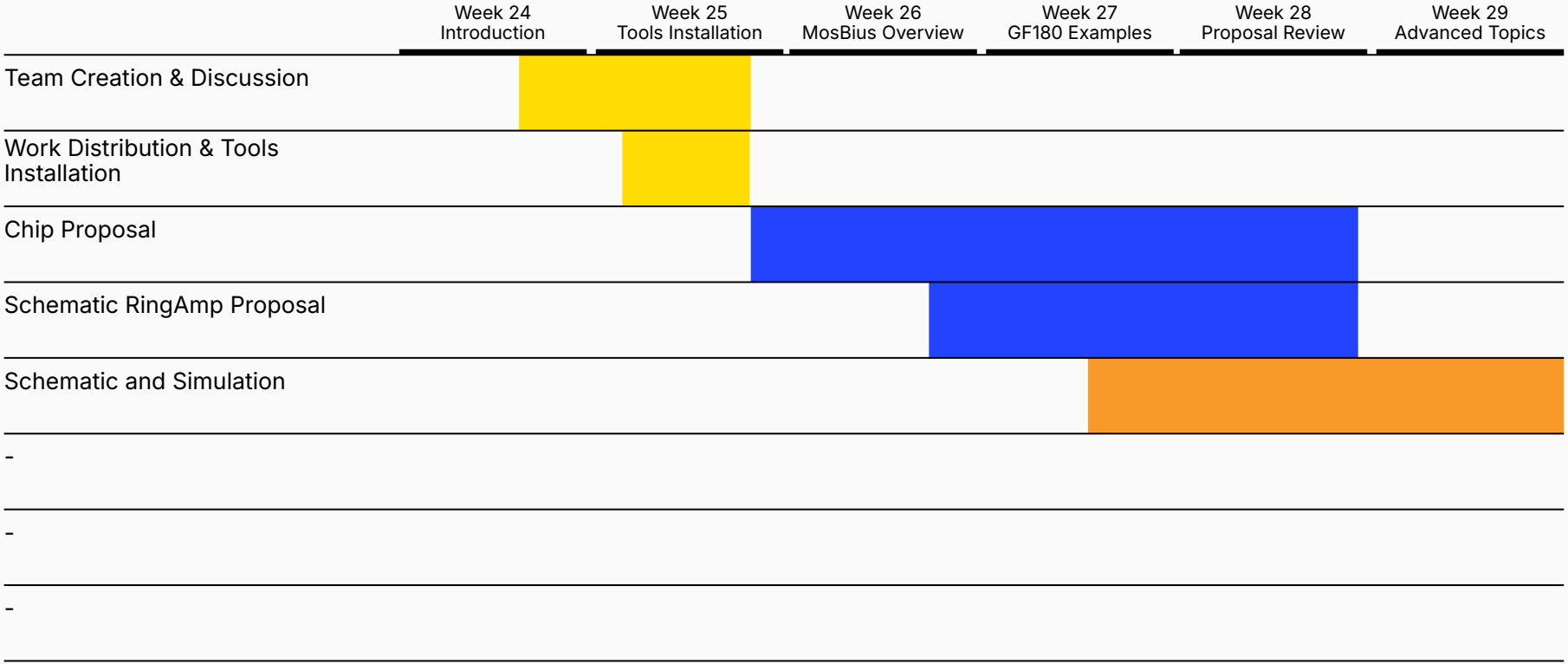
Pin-Out Diagram

Pin-Out Diagram

Pin Name	Direction	Type	Description
VIN_PLUS	Input	Analog	Positive input to Ring Amplifier
VIN_MINUS	Input	Analog	Negative input to Ring Amplifier
VSTG1_P	Output	Analog	Output of first stage of Ring Amplifier (positive branch)
VSTG1_N	Output	Analog	Output of first stage of Ring Amplifier (negative branch)
VCTRL_P	Input	Analog	Deadzone voltage for current-starved inverters (PMOS path)
VCTRL_N	Input	Analog	Deadzone voltage for current-starved inverters (NMOS path)
VCTRLP_RG	Output	Analog	Process-invariant PMOS bias from deadzone regulation circuit
VCTRLN_RG	Output	Analog	Process-invariant NMOS bias from deadzone regulation circuit
VGP	Input	Analog	Gate voltage for third stage PMOS
VGN	Input	Analog	Gate voltage for third stage NMOS
VDD	Power	Supply	Positive power supply (typically 3.3V)
GND	Power	Ground	Ground / reference voltage
VOUT_PLUS	Output	Analog	Positive output of Ring Amplifier
VOUT_MINUS	Output	Analog	Negative output of Ring Amplifier

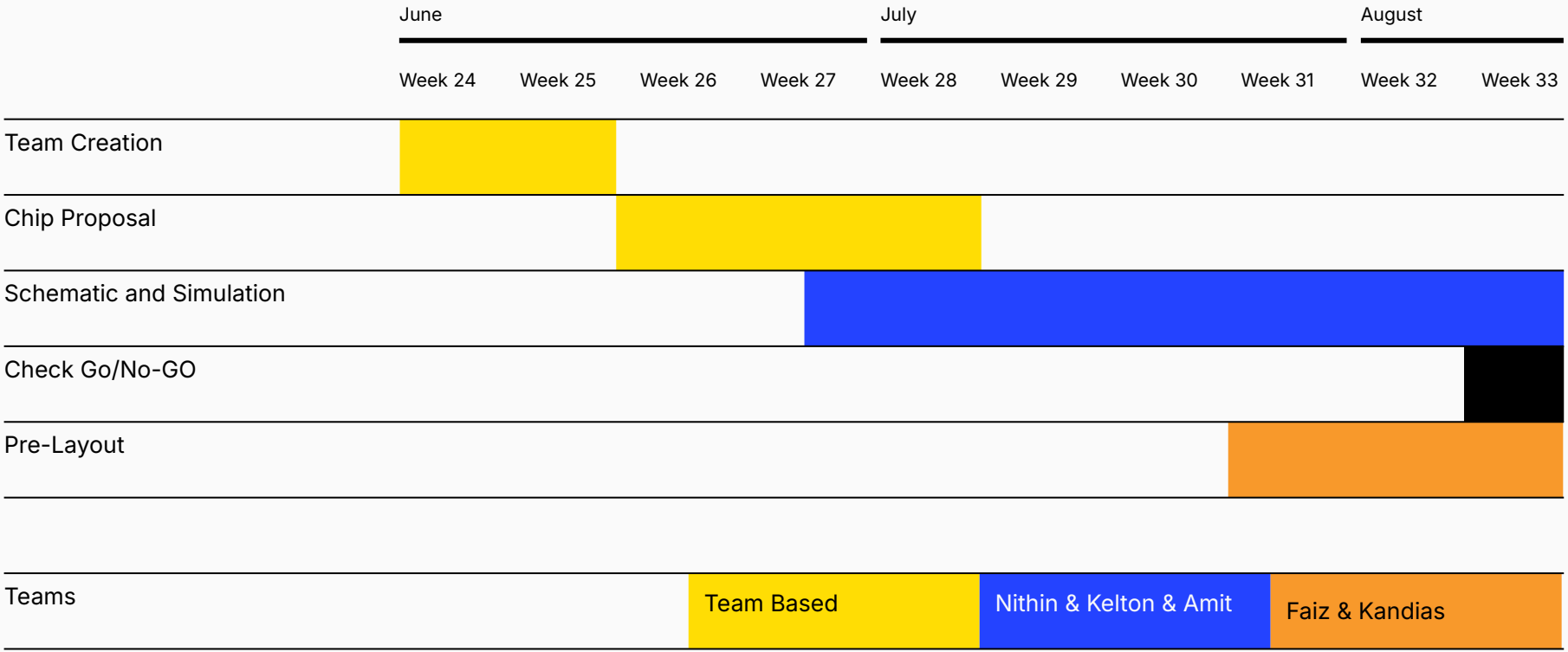
Project workflow

Reference from Github Chipathon 2025



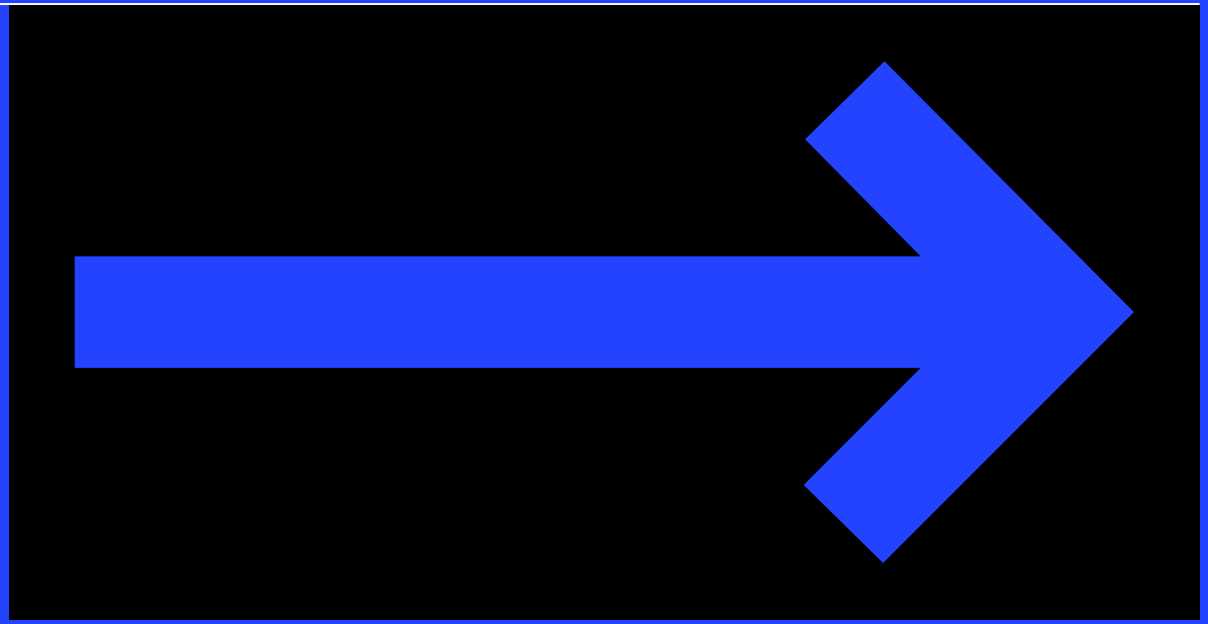
Project workflow (Overall)

Reference from Github Chipathon 2025



Q&A

Any questions?
Ask away!



Thank you!