# Ring Amplifiers for Switched Capacitor Circuits

Benjamin Hershberg, *Member, IEEE*, Skyler Weaver, Kazuki Sobue, Seiji Takeuchi, Koichi Hamashita, *Member, IEEE*, and Un-Ku Moon, *Fellow, IEEE*

***Abstract*—In this paper the fundamental concept of ring amplification is introduced and explored. Ring amplifiers enable efficient amplification in scaled environments, and possess the benefits of efficient slew-based charging, rapid stabilization, compression-immunity (inherent rail-to-rail output swing), and performance that scales with process technology. A basic operational theory is established, and the core benefits of this technique are identified. Measured results from two separate ring amplifier based pipelined ADCs are presented. The first prototype IC, a simple 10.5-bit, 61.5 dB SNDR pipelined ADC which uses only ring amplifiers, is used to demonstrate the core benefits. The second fabricated IC presented is a high-resolution pipelined ADC which employs the technique of Split-CLS to perform efficient, accurate amplification aided by ring amplifiers. The 15-bit ADC is implemented in a 0.18 $\mu$m CMOS technology and achieves 76.8 dB SNDR and 95.4 dB SFDR at 20 Msps while consuming 5.1 mW, achieving a FoM of 45 fJ/conversion-step.**

***Index Terms*—A/D, ADC, analog to digital conversion, analog to digital converter, CLS, correlated level shifting, high resolution, low power, nanoscale CMOS, rail-to-rail, RAMP, ring amp, ring amplification, ring amplifier, ringamp, scalability, scaling, slew-based, split-CLS, stabilized ring oscillator, switched capacitor.**

## I. Introduction

In many ways, the task of performing amplification in switched capacitor CMOS circuits is at a crossroads. The effects of technology scaling have made it increasingly difficult to implement accurate, efficient amplifiers from topologies that were conceived of at a time when 2.5 V supplies were considered low-voltage, and the intrinsic properties of transistors were quite different from that of a 14 nm FinFET [1]. And yet, for each scaling challenge that has arisen, a multitude of techniques which seek to solve it have emerged, and there are indeed many highly effective digital correction, gain-enhancement, and output-swing enhancement techniques now available to designers. However, the ability of these techniques to deliver favorable amplifier scaling characteristics in actual fabricated designs has fallen somewhat short of expectations. For example, the ADC performance surveys conducted in [2] and [3] indicate that there is both a notable scarcity of high-resolution ADCs implemented in nanoscale CMOS as well as a progressive decline in power efficiency for those that are reported. These observations are also a reflection of the net effect of opamp scaling challenges on system-level performance, since amplification is used in almost all high-resolution ADC architectures. By contrast, certain low and medium resolution ADC architectures that do not use opamps (such as SAR ADCs) have scaled very well into modern technologies.

For the most part, this failure-to-scale seems to have happened because the underlying structure—an opamp—is fundamentally ill-suited to scaling. Applying additional techniques may enable an opamp to function in nanoscale environments, but it will not grant it the ability to scale at the same pace as digital performance improvements. A truly scalable amplifier must operate in a way that implicitly uses the characteristics of scaled CMOS to its advantage, transforming potential weaknesses into inherent strengths. Because technology scaling is deliberately designed to favor the time-domain world of high-speed digital, such scalable analog techniques will likely be found in this realm as well. In order to fully exploit the abilities of a transistor, the biasing and small-signal properties of the device must be

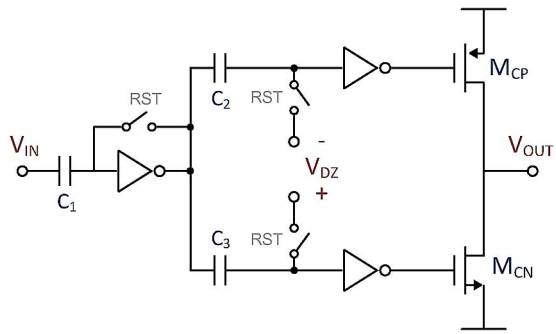


Fig. 1. Fundamental structure of a ring amplifier. A ring amplifier is created by splitting a ring oscillator into two signal paths and embedding a different offset in each path. When placed in switched-capacitor feedback, a set of internal mechanisms generate stability and allow the oscillator to be used as an amplifier.

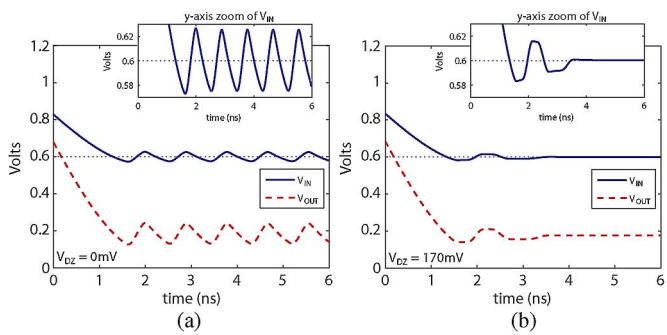


Fig. 2. Input and output charging waveforms of Fig. 1 when placed in the switched capacitor feedback structure of Fig. 3. In (a), when $V_{\rm DZ} = 0$ mV, the ringamp is functionally identical to a three-inverter ring oscillator. In (b), the dead-zone is set large enough to generate stability ($V_{\rm DZ} = 170$ mV) and the ringamp functions as an amplifier.

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B. Hershberg, S. Weaver, and U. Moon are with Oregon State University, Corvallis, OR 97331 USA.

K. Sobue is with the AKM Technology Corporation, Miyazaki-City, Miyazaki 880-0805 Japan.

S. Takeuchi and K. Hamashita are with the Asahi Kasei Microdevices Corporation, Atsugi, Kanagawa 243-0021, Japan.

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viewed as highly coupled, time-dependent variables which can be applied as feedback to each other with respect to time. In this paper, we introduce one such technique: ring amplification. A ring amplifier is a small modular amplifier derived from a ring oscillator which naturally embodies all the essential elements of scalability. It can amplify with rail-to-rail output swing, efficiently charge large capacitive loads using slew-based charging, scale well in performance according to process trends, and is simple enough to be quickly constructed from only a handful of inverters, capacitors, and switches.

This paper is organized as follows. In Section II we introduce the basic structure of a ring amplifier, and establish its basic theory of operation in Section III. We will identify and explore the key benefits of ring amplification as it relates to scalability in Section IV. Two fabricated IC designs are then presented. In Section V, we present a 10.5-bit pipelined ADC that demonstrates and characterizes the basic principles of the previous sections. Finally, in Section VI we present a high-resolution 15-bit pipelined ADC which uses the technique of Split-CLS to exploit the properties of both ring amplification and conventional opamps. Conclusions are given in Section VII.

## II. Basic Structure

Ring amplification is, at its core, a set of concepts—concepts that can be realized through a variety of structural implementations and design choices. One such implementation is depicted in Fig. 1. This simple structure embodies the key features of ring amplification, and in many ways can be thought of as the quintessential "base case". There are, however, a range of implementation approaches available, each with their own pros and cons in terms of speed, accuracy, and efficiency; we will address some of these broader considerations from within the context of Fig. 1 throughout this paper.

Fundamentally, a ring amplifier (alternately: ringamp or RAMP) is a ring oscillator that has been split into two (or more) separate signal paths. A different offset is embedded into each signal path in order to create a range of input values for which neither output transistor $M_{\mathrm{CN}}$ nor $M_{\mathrm{CP}}$ of Fig. 1 will fully conduct. If this non-conduction "dead-zone" is sufficiently large, the ring amplifier will operate by slewing-to, stabilizing, and then locking into the dead-zone region. When placed in the example switched capacitor MDAC feedback structure of Fig. 3, this charging and settling behavior results in the waveforms of Fig. 2(b).

Before we examine how and why this occurs (in Section III), it is useful to first understand some of the basic characteristics of the structure itself. To begin with, consider the capacitor $C_1$ of Fig. 3. $C_1$ is used to cancel the difference between the MDAC virtual-node sampling reference $(V_{\mathrm{CMX}})$ and the trip-point of the first stage inverter. This ensures that the ideal settled value for $V_{\mathrm{IN}}$ will always be $V_{\mathrm{CMX}}$, independent of the actual inverter threshold. Any sources of offset that are generated after the first stage inverter will not be removed by $C_1$, but the input-referred value of such offsets will typically be negligibly small.

The dead-zone of the ringamp in Fig. 3 is embedded prior to the second stage inverters by storing a voltage offset across capacitors $C_2$ and $C_3$. Any value for $V_{\mathrm{IN}}$ within the dead-zone region is a viable steady-state solution for the ring amplifier,

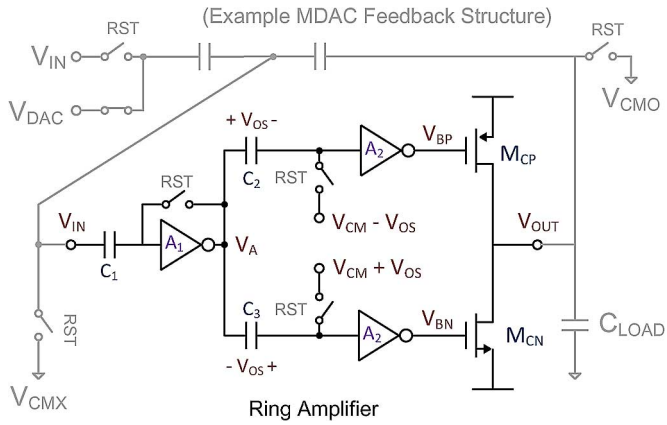


Fig. 3. The ringamp and basic switched-capacitor feedback network that we will primarily consider in the first half of this paper. Devices and parameters that are referenced throughout the paper are labeled. Also, $V_{\mathrm{DZ}}$ of Fig. 1 equals $2V_{\mathrm{OS}}$ here.

and the input-referred value of the dead-zone will determine the overall accuracy of the amplifier for most practical cases. In other words, the error at $V_{\mathrm{IN}}$ when the ringamp has stabilized and locked will be

$$-\left|\frac{V_{\mathrm{DZ}}}{2\cdot A_1}\right| \leq \epsilon_{V_{\mathrm{IN}}} \leq \left|\frac{V_{\mathrm{DZ}}}{2\cdot A_1}\right| \tag{1}$$

where $V_{\mathrm{DZ}} = 2V_{\mathrm{OS}}$, $A_1$is the final settled small-signal gain of the first stage inverter, and finite gain effects of the latter stages are ignored (revisited later).

It is worth briefly noting that there are many additional options for both where and how to embed the dead-zone offset into the ring amplifier, and for different target accuracies and design applications it may be useful to consider additional possibilities and their respective advantages and disadvantages. In this paper, however, we will focus solely on the embedding scheme of Fig. 3, which possesses several key benefits. First of all, embedding it with capacitors allows us to accurately and linearly set the dead-zone offset value, and it can be done with a high-impedance, low-power reference. Second, as we shall soon see in Section III, there are important stability benefits gained by embedding the offset prior to the second stage inverters, rather than the first or third stage. Finally, due to the accuracy limitations imposed by (1), we typically wish to create an input-referred dead-zone value of a few millivolts or less, and for medium accuracy ring amplifiers, embedding the dead-zone offsets immediately after the first gain stage will create input-referred dead-zone sizes small enough to achieve desired accuracies while still keeping the embedded offset large enough to easily tune with a simple DAC or voltage reference.

## III. Stabilization Theory

Although the fundamental structure of a ring amplifier is quite simple, a full understanding of the operational theory behind ring amplification is considerably more complex. The steady-state, small signal, and transient characteristics of a ring amplifier are highly co-dependent, and as such, its behavior cannot be fully explained by considering each operational domain (DC, AC, transient) separately, as is often the preferred approach in opamp design. Computer aided simulation is necessarily a major

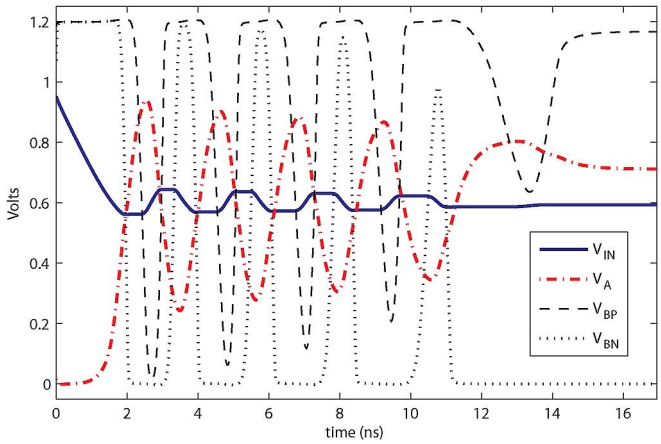


Fig. 4. Example ring amplifier operation for an exaggerated design biased at the edge of stability, showing the three key phases of operation: 1) initial ramping, 2) stabilization, and 3) steady-state.

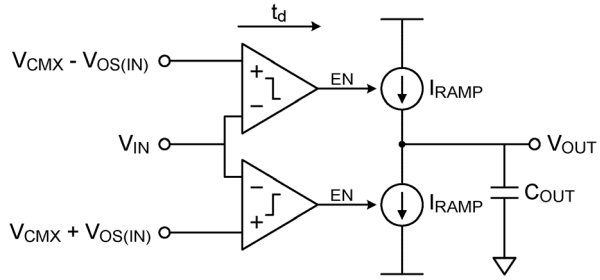


Fig. 5. Conceptual model of a ringamp during the initial slew-charging phase of operation. This model only applies to the initial charging phase and does not include the key ringamp stabilization mechanisms. $V_{\mathrm{OS(IN)}}$ is the input-referred value of the dead-zone offset.

component of ringamp design, and for this reason a good conceptual intuition is perhaps of more practical value than a strict analytic model. It is in this conceptual manner that we will proceed, by breaking the theory of operation down to several simple sub-concepts. First, ringamp operation can be subdivided with respect to different phases of operation in time: slewing, stabilization, and steady-state. Second, the theory of operation within each phase can be reduced to a chain of cause-and-effect mechanisms.

To illustrate key concepts, we will use the exaggerated charging waveform of Fig. 4 (taken from the ring amplifier of Fig. 3) that has been designed with relatively low bandwidth, excessive drive current, and a dead-zone size that biases the ringamp right at the edge of stability. Although one would never wish to make a real design in this way, as a teaching example it is quite useful. $V_{\mathrm{CMX}}$ is set to 0.6 V, and thus the ideal settled value of $V_{\mathrm{IN}}$ will also be 0.6 V. For the sake of simplicity and generality $V_{\mathrm{OUT}}$ is not shown (because it is simply a scaled, shifted, signal-dependent replica of $V_{\mathrm{IN}}$). Unless otherwise stated, any mention of the amplitude of the fed-back signal will refer to the amplitude seen at $V_{\mathrm{IN}}$.

In Fig. 4 we can clearly see three main phases of operation. Initially, from 0 ns to 2 ns, the ringamp rapidly charges toward the dead-zone. Then, from 2 ns to about 14 ns it oscillates around the dead-zone region as it attempts to stabilize. By 15 ns, with the output transistors $M_{\mathrm{CP}}$ and $M_{\mathrm{CN}}$ both completely cutoff, the ring amplifier reaches a steady-state solution within the dead-zone, and remains locked.

### A. Initial Ramping

In the initial slew-charging phase of operation, the ring amplifier is functionally equivalent to the circuit of Fig. 5. The first two stages of the ring amplifier act like a pair of bi-directional continuous-time comparators that correctly select which output transistor ($M_{\mathrm{CN}}$ or $M_{\mathrm{CP}}$) to use depending on the value of the input signal. The selected output transistor then operates as a maximally-biased current source and charges the output load with a ramp. In this initial charging phase the ringamp behaves similar to a zero-crossing based circuit [4], [5].

The ramping phase ends when the input signal crosses the threshold of the comparator and the current source turns off. Due to the finite time delay of the comparator, there will be some amount of overshoot beyond the comparator threshold, which will be given by

$$\Delta V_{\mathrm{overshoot}} = \frac{t_d \cdot I_{\mathrm{RAMP}}}{C_{\mathrm{OUT}}} \tag{2}$$

where $t_d$ is the time delay of the comparator decision, $I_{\mathrm{RAMP}}$ is the current supplied by the active current source, and $C_{\mathrm{OUT}}$ is the total loading capacitance seen at the output. This overshoot is with respect to the trip point, which will be on the boundary of the dead-zone. It will be more useful later on if we consider (1) as well, and express the input-referred overshoot with respect to the ideal settled value (the center of the dead-zone):

$$\Delta V_{\mathrm{init}} = \frac{t_d \cdot I_{\mathrm{RAMP}}}{\psi\, C_{\mathrm{OUT}}} - \left| \frac{V_{\mathrm{DZ}}}{2 \cdot \hat{A}_1} \right| \tag{3}$$

where $\psi$ is the scaling factor that refers the output overshoot to the ringamp's input (and depends on feedback factor, parasitics, and feedback structure) and $\hat{A}_1$ is the effective gain of the first stage inverter at the end of the ramping operation (explained later).

### B. Stabilization

After the initial charging ramp, the ring amplifier will begin to oscillate around the target settled value with amplitude $\Delta V_{\mathrm{init}}$. With no dead-zone, the structure is functionally identical to a three-inverter ring oscillator, and will continue to oscillate indefinitely (Fig. 2(a)). However, as the size of the dead-zone is increased, the ringamp will eventually reach an operating condition where it is able to self-stabilize, such as in Fig. 4. If the dead-zone size is increased further still, the time required to stabilize decreases substantially, and for most practical designs, a ringamp will stabilize in only one or two periods of oscillation (i.e., Fig. 2(b)).

The most fundamental mechanism in the process of stabilization is the progressive reduction in the peak overdrive voltage applied to the output transistors $M_{\mathrm{CN}}$ and $M_{\mathrm{CP}}$ on each successive period of oscillation. This effect is illustrated in Fig. 4 by the progressive decrease in amplitude of the signals $V_{\mathrm{BP}}$ and $V_{\mathrm{BN}}$. When the following relation is true, the trough (minimum

value) of $V_{\rm BP}$ will be limited by the finite-gain of the first two stages, and begin to de-saturate from rail-to-rail operation:

$$\hat{A}_2\left[\hat{A}_1\left(min(\tilde{V}_{\rm IN})-V_{\rm CMX}\right)-V_{\rm OS}\right]\geq V_{\rm SS}-V_{\rm CM} \quad (4)$$

(where $\tilde{V}_{\rm IN}$ is the peak-to-peak amplitude, and $\hat{A}_1, \hat{A}_2$ are the negative-valued effective instantaneous inverter gains). A similar relation can also be expressed for the lower signal path and $V_{\rm BN}$:

$$\hat{A}_2\left[\hat{A}_1\left(max(\tilde{V}_{\rm IN})-V_{\rm CMX}\right)+V_{\rm OS}\right]\leq V_{\rm DD}-V_{\rm CM}. \quad (5)$$

The key point to notice in these expressions is that each signal path is being fed a different shifted replica of the oscillatory waveform generated at $V_{\rm A}$. The upper path is given a replica where the *peaks* of the wave are *lowered* closer to the second stage inverter's threshold, and the lower path is given a replica where the *troughs* of the wave are *raised* closer to the threshold of the second stage inverter. For a sufficiently large shift in each path $(V_{\rm OS})$, this creates the possibility that even for relatively large values of $\tilde{V}_{\rm IN}$, finite gain effects will simultaneously limit the overdrive voltage that is applied to both $M_{\rm CP}$ and $M_{\rm CN}$. This stands in stark contrast to the behavior of a three-inverter ring oscillator, where the decrease in $V_{\rm OV}$ of one output transistor necessarily means an increase in $V_{\rm OV}$ applied to the other.

When (4) and (5) are true, the resulting reduction in $V_{\rm OV}$ applied to the output transistors $M_{\rm CN}$ and $M_{\rm CP}$ will reduce the magnitude of the output current $I_{\rm RAMP}$. This decrease in output current will also cause a decrease in the amplitude of $\tilde{V}_{\rm IN}$ by a proportional amount, due to (3). The left sides of (4) and (5) are therefore reduced further, and the $V_{\rm OV}$'s of $M_{\rm CN}$ and $M_{\rm CP}$ will decrease even more for the next oscillation cycle. This effect will continue to feedback until the input signal amplitude becomes smaller than the input-referred value of the dead-zone, at which point the ring amplifier will stabilize and lock into the dead-zone.

If we combine (4) and (5) and rearrange, we see that in order to trigger this progressive overdrive reduction effect, the input signal must satisfy the following relation:

$$\tilde{V}_{\rm IN}\leq\frac{1}{\hat{A}_1}\left(\frac{V_{\rm DD}-V_{\rm SS}}{\hat{A}_2}-V_{\rm DZ}\right). \quad (6)$$

Furthermore, at the beginning of the stabilization phase:

$$\tilde{V}_{\rm IN}=2\cdot\Delta V_{\rm init}. \quad (7)$$

Finally, using (2), (3), (6), and (7), we can express the stability criterion in terms of the dead-zone (i.e., settled accuracy) and the initial slew rate (i.e., speed):

$$\frac{t_d\cdot I_{\rm RAMP}}{\psi\, C_{\rm OUT}}\leq\frac{1}{2\cdot\hat{A}_1}\left(\frac{V_{\rm DD}-V_{\rm SS}}{\hat{A}_2}-2\cdot V_{\rm DZ}\right). \quad (8)$$

Recall once again that $\hat{A}_1$ and $\hat{A}_2$ are negative valued gains.

From this relation we see that there is a clear design tradeoff between accuracy, speed, and power. Let us assume for a moment that only $t_d$, $I_{\rm RAMP}$, and $V_{\rm DZ}$ can be adjusted. To increase speed, one can either increase the initial ramp rate or decrease the time required to stabilize. Both options require sacrificing either accuracy (by increasing $V_{\rm DZ}$) or power (by decreasing $t_d$). Likewise, to increase accuracy (by decreasing $V_{\rm DZ}$), one must either decrease $I_{\rm RAMP}$ or decrease $t_d$ accordingly. While these simple tradeoffs serve as a good starting point, as we will soon discover, every parameter in (8) is variable to some extent.

The discussion thus far is only a first-order model, and there are additional bandwidth, slewing, and device biasing dynamics which are not represented. Let us take a moment to evaluate this model in the form of a practical example. Consider a pseudo-differential ringamp where $A_1 = A_2 = -25$ V/V, $V_{\rm DZ} = 100$ mV, $V_{\rm DD} = 1.2$ V, and $V_{\rm SS} = 0$ V. By (1), the input-referred size of the dead-zone will be about 4 mV, which for a 2 V pk-pk input signal would ideally be accurate enough to achieve an input-referred SNDR of 54 dB. By (6), the maximum allowable peak-to-peak amplitude of $\tilde{V}_{\rm IN}$ is approximately 6 mV, and by (3), the maximum allowable input-referred overshoot at the end of the initial ramping phase must be less than 5 mV.

This is not a very encouraging result, since such a small overshoot will place a tight constraint on the parameters in (2). However, if one were to simulate this same scenario, it will turn out that the peak-to-peak amplitude of oscillation can be significantly larger than the predicted 6 mV and still achieve stability. A closer look at Fig. 4 reveals an important contributor to this disparity between theory and practice. Although the AC small-signal gain of the first stage inverter, $A_1$, may be $-25$ V/V, the effective instantaneous value

$$\hat{A}_1(t)=\frac{V_{\rm A}(t)}{V_{\rm IN}(t)} \quad (9)$$

in the actual transient waveform will be several times smaller at the beginning of stabilization. Thus, although the overall accuracy of the ringamp is determined by the final, settled, small-signal value of $A_1$, the stability criterion is determined by the initial, transient, large signal effective value of $A_1$. This reduction in $A_1$ occurs because the first stage inverter inherently operates around its trip point, where it will be slew limited. The maximum slewing current that the inverter can provide will be

$$I_{\rm slew}=I_{\rm P}-I_{\rm N} \quad (10)$$

and for a square law MOSFET model, this will become

$$I_{\rm slew}=2k'\frac{W}{L}\left(\frac{V_{\rm DD}-V_{\rm SS}}{2}\right)V_{\rm IN}. \quad (11)$$

Notice here that the slew current is linearly related (not quadratically) to the input voltage. Thus, for the first stage inverter, slew rate limiting (and finite bandwidth) has an important impact on determining the effective value of $\hat{A}_1$ during stabilization (and to a lesser extent, the value of $\hat{A}_2$). This dynamic adjustment of the effective inverter gain is a very attractive characteristic, and improves the design tradeoff between speed, accuracy, and power by a significant factor. Similar effects also influence the operation of the second stage inverters in an additional way: although (4) and (5) assume rail-to-rail swing for the second stage inverters when $\tilde{V}_{\rm IN}$ is large, in reality the output swing of the second stage inverters may never completely reach rail-to-rail, regardless of the value of $\tilde{V}_{\rm IN}$ due to slew rate limiting, finite bandwidth, and triode device operation.

The discussion of progressive overdrive reduction in this section can be conceptualized as a dynamic adjustment of the

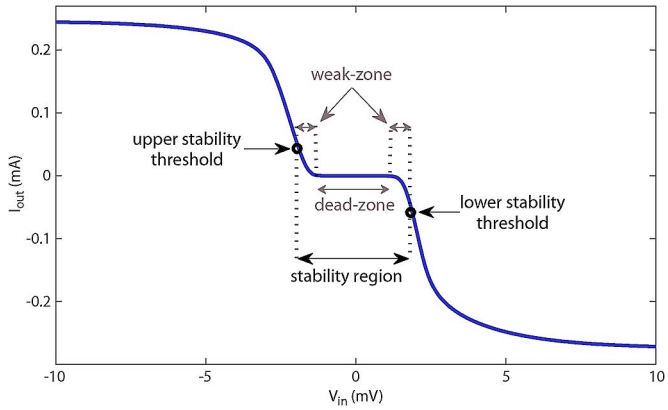


Fig. 6. DC sweep of $V_{\rm IN}$ vs. $I_{\rm OUT}$ for a typical configuration of Fig. 1, illustrating the full input-referred characteristic near the dead-zone region. In addition to a true "dead-zone" where both output transistors are in cutoff, there is also a small boundary region "weak-zone" where the output pole location is low enough to create stability.

ringamp's output pole corner frequency. The decrease in output current due to $V_{\rm OV}$ reduction increases the output impedance $(R_o)$ of the ringamp, and pushes the output pole (formed by $R_o$ and $C_{\rm LOAD}$) to lower frequency. As the $V_{\rm OV}$ reduction effect gains momentum on each successive oscillation half-period, the output pole progressively pushes to lower and lower frequency. By the time the ringamp is locked into the dead-zone and the output transistors are in cutoff, $R_o$ is infinite and the output pole is at DC.

### C. Steady State

Thus far, we have defined the steady-state condition for a ring amplifier as the complete cutoff of both output transistors, with the input signal lying solidly within the dead-zone, such as is the case in Fig. 4. However, considering the discussion about pole adjustment in the previous paragraph, it is clear that the ringamp can in fact be stable for a range of low frequency output pole locations down to DC. Such a situation will in practice occur often, even for a large dead-zone, since there is always a finite probability that the ring amplifier will happen to stabilize right at the edge of the dead-zone. If that happens, one of the output transistors will still conduct a small amount of current to the output, and may never fully shut off before the amplification period ends. The existence of this stable, boundary-region "weak-zone" is illustrated in the $V_{\rm IN}$ vs. $I_{\rm OUT}$ plot of Fig. 6. The weak-zone is not an inherent problem for ring amplification operation, since any low-bandwidth settling will only serve to further improve accuracy. However, there are sometimes higher-level structural considerations that make it advantageous to ensure that both output transistors are completely non-conducting once settled. The design presented in Section VI is one such case, and it is there that we will explore this issue in more detail.

## IV. Key Advantages

Ring amplifiers are in many ways both structurally and functionally quite different from conventional opamps, and it is in these differences that the ringamp finds a unique advantage in the context of modern low-voltage CMOS process technologies. In this section, we will examine several of these important benefits.

### A. Output Compression Immunity

In low-voltage scaled environments, kT/C noise, SNR, and power constraints will typically be dictated by the usable signal range available [2], and any practical amplification solution for scaled CMOS must therefore utilize as much of the available voltage range as possible. As it turns out, ring amplifiers are almost entirely immune to output compression, and this enables them to amplify with rail-to-rail output swing.

To understand the basis of this output compression immunity, we must consider two scenarios. First, imagine a ringamp whose dead-zone is large enough that when the ringamp is locked into the center of the dead-zone, both $M_{\rm CN}$ and $M_{\rm CP}$ will be in cutoff. In other words, when

$$V_{\rm DZ} \geq \left| \frac{V_{\rm DD} - V_{\rm SS} - 2V_{\rm T}}{A_2} \right|. \tag{12}$$

As a rule of thumb, this relation will usually hold for low and medium accuracy ringamps up to about 60 dB. Under this scenario, $M_{\rm CN}$ and $M_{\rm CP}$ function as current sources whose linearity and small-signal gain has no appreciable effect on settled accuracy. The internal condition of the ringamp depends only on the signal at the input, and it will continue to steer toward the dead-zone until $M_{\rm CN}$ and $M_{\rm CP}$ are completely cut off, regardless of whether they are in saturation or triode. Final settled accuracy will be governed by (1), independent of the characteristics at the output.

Now let us consider the condition where (12) does not hold. This will occur when the dead-zone is very small, and accuracies in the 60 dB to 90 dB range are desired. Although other practical issues in the ringamp structure of Fig. 3 may hinder such design targets, a theoretical discussion is still quite useful in understanding the issues relevant to high accuracy ringamp topologies in general. In this scenario, the stability region of Fig. 6 is so small that the two weak-zones touch, and $M_{\rm CN}$ and $M_{\rm CP}$ will still conduct a small amount once settled. The ringamp's steady state condition will essentially be that of a three stage opamp, and the open loop gain will be the product of the three stage gains. With no true dead-zone, the distortion term of (1) becomes zero, and finite loop gain will become the fundamental limitation on accuracy. At first glance, generating sufficient loop gain appears to be a problem, since the gain of $M_{\rm CN}$ and $M_{\rm CP}$ will depend on output swing (which must be as large as possible in nanoscale CMOS). Consider the case where all three stages have a gain of 25 dB when operating in saturation. In the best case, the open loop gain will be 75 dB, and in the worst case perhaps 50 dB. Even in the best case, this seems to suggest that to build an 80 dB accurate ringamp, an additional gain stage is required.

Luckily, there is another effect at play here. In the ideal square-law MOSFET model $M_{\rm CN}$ and $M_{\rm CP}$ will be in saturation when $V_{\rm OV}$ is less than $V_{\rm DS}$. Furthermore, the small signal output impedance, $r_o$, is inversely proportional to the drain current, $I_{\rm D}$. In the context of the progressive overdrive voltage reduction that occurs in ringamp stabilization, both

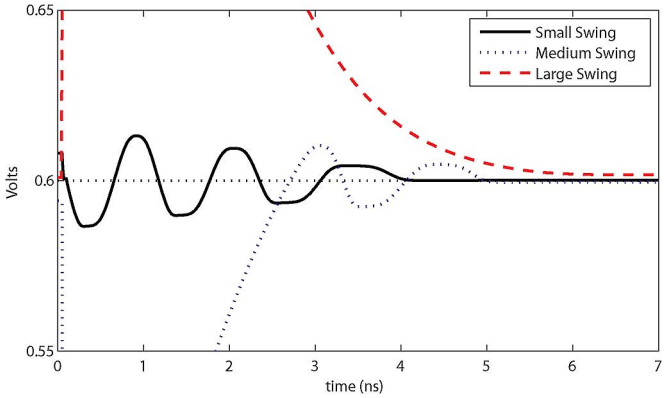


Fig. 7. Zoomed stabilization waveform of $V_{\rm IN}$ for three output swing cases: small (output near mid-rail), medium, and large (final output near the supply).

$V_{\rm OV}$ and $I_{\rm D}$ will in fact trend towards zero. This implies that during steady-state, $M_{\rm CN}$ and $M_{\rm CP}$ will remain in saturation or weak-inversion even for very small values of $V_{\rm DS}$, and moreover, that their gain will be enhanced by a dynamic boost in $r_o$. Thus, even for a nominal open loop gain of 75 dB, with a wisely chosen topology it is possible to have an enhanced steady-state gain of at least 90 dB, even when swinging close to the rails.

Although output swing has little effect on ringamp accuracy, it will indeed affect speed, both with respect to slewing and settling. In the initial ramping phase, the selected current source transistor will be biased with the maximum possible $V_{\rm OV}$, and this guarantees that for much of the possible output range it will initially be operating in triode. As seen in Fig. 7, for settled output values near mid-rail, $I_{\rm RAMP}$ will be the highest and the initial ramping will be faster, but more time will be required to stabilize for the reasons discussed in Section III-B. Likewise, for values close to the rails, $I_{\rm RAMP}$ will be smaller, so the initial ramping will be slower but the stabilization time will be shorter. For the most part, this works out quite nicely, since the total time required to reach steady state in each case turns out to be approximately the same. However, for extreme cases very close to the rails, the large RC time constant of the output transistor in triode operation will require a comparatively long time to reach its target value. Ultimately, it is this RC settling limitation that will usually dictate the maximum output swing possible for a given speed of operation.

### B. Slew-Based Charging

Whereas a conventional opamp charges its output load with some form of RC-based settling, the output transistors $M_{\rm CN}$ and $M_{\rm CP}$ in the ring amplifier behave like digitally switched current sources, and charge the output with slew-based ramping. This is a much more efficient way to charge, since only one of the current sources in Fig. 5 will be active at a time, and the only power dissipated will be dynamic. Furthermore, during the initial ramping operation, $M_{\rm CN}$ or $M_{\rm CP}$ (whichever is selected) will be biased with the maximum $V_{\rm OV}$ possible for the given supply voltage. This is a major benefit, because it means that even for large capacitive loads, small transistor sizes can still produce high slew rates, and with small output transistors, the second stage inverters will be negligibly loaded by $M_{\rm CN}/M_{\rm CP}$. This effectively decouples the internal power requirements from that of the output load size, and for typical load capacitances in the femto and pico-farad range, the internal power requirements are more-or-less independent of output capacitance. This unique property stands in stark contrast to the power-loading relationship for a conventional opamp, where settling speed is typically proportional to $g_m/C_{\rm LOAD}$. Even for large load capacitances, where the size of $M_{\rm CN}/M_{\rm CP}$ does have an appreciable effect on the internal power requirements, the ratio of static-to-dynamic power will scale very favorably.

### C. Performance Scaling With Process

In order for a technique to be truly scalable, it must meet two criteria. First, the given technique must operate efficiently *in* a scaled environment. This requirement has been our primary focus thus far. Second, the technique must inherently scale *with* advancing process technology, improving in performance simply by migrating into a newer technology. It is this second criteria that we will discuss now.

Intuitively, the ring amplifier seems like a prime candidate to benefit from process scaling, simply by its structural similarity to a ring oscillator. After all, the performance of ring oscillators track so closely with process technology that they are often used by foundries as a means of characterizing a given technology. And indeed, the stability criterion of (8) suggests this to be true. As we explored in Section IV-B, the internal power consumption of a ringamp is governed much more by inverter power-delay product and internal parasitics than the size of the output load (in stark contrast to conventional opamps). Since the power-delay product of an inverter decreases approximately linearly in accordance with decreasing feature size [6], the ringamp's inverter chain propagation delay, $t_d$, can be expected to scale according to digital process performance as well. With the relationships in (8), this reduction in $t_d$ can be directly traded for an improvement in any of the three main design specifications: speed, accuracy, and power.

As a general rule of thumb, using small internal device sizes will tend to yield the highest power efficiencies, since doing so will not only help to minimize the power-delay product, but also minimize crowbar currents, which are a major source of static power (since the first stage inverter is always close to its trip point when settled). Considering that the time delay of a minimum sized inverter scales as a function of minimum feature size, it also follows that the conversion speed at which a ringamp most efficiently operates will be a function of the technology's minimum feature size.

To demonstrate this scalability property of ringamps, the results of a simple experiment designed to predict scaling trends are presented in Fig. 8. The setup for the test is simple: using the ring amplifier structure and pseudo-differential switched-capacitor MDAC of Figs. 9 and 10, the structure must be designed to meet the required specifications of Table I for several different CMOS technology nodes while attempting to minimize total power consumption. Only transistor width and length resizing is allowed. The speed and accuracy targets are set at the upper-end of the given structure's practical limits, and the load capacitance is sized to be sufficient for an 11b pipelined ADC with 10 b ENOB. Although the ringamp structure could be more

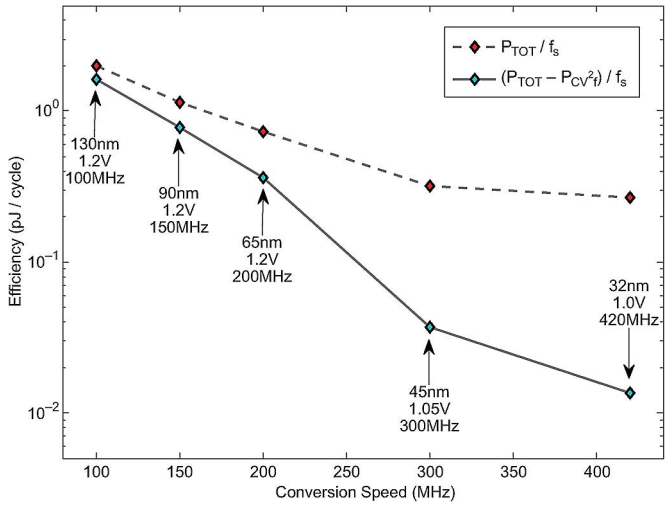


Fig. 8. Simulated ring amplifier scaling trends, characterized using the simple structures of Figs. 9 and 10 and predictive technology models for nanoscale CMOS [7]. Device sizes are adjusted for each technology node as necessary in order to meet the fixed design requirements given by Table I.

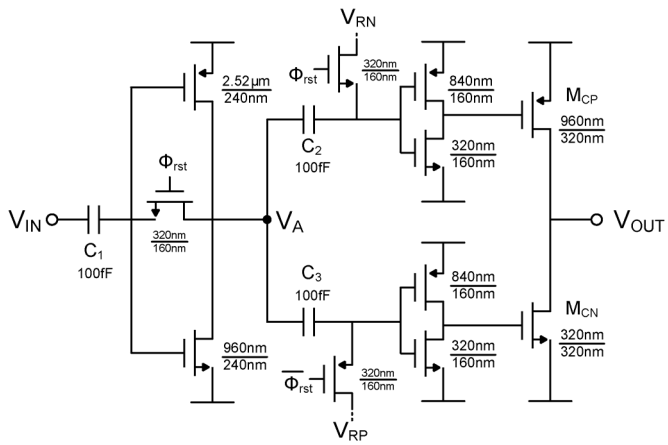


Fig. 9. Complete transistor-level ring amplifier structure of the 10.5-bit characterization ADC, with the actual component values used in the fabricated design.

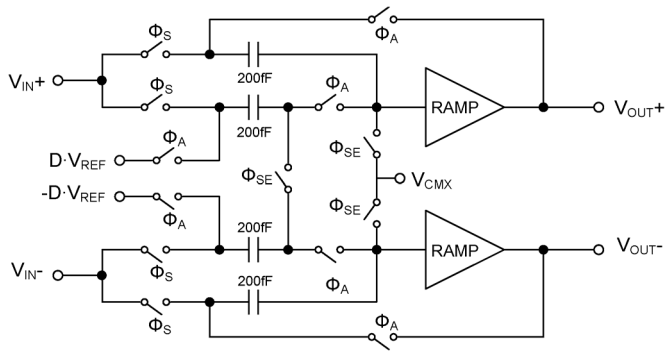


Fig. 10. Pseudo-differential float-sampled 1.5 b flip-around MDAC. In this structure, the differential gain is 2 and the common-mode gain is 1, eliminating the need for additional common-mode feedback.

efficient (for example, disabling itself during $\phi_s$), we are only interested in the *relative* power efficiencies across process technologies, and the bare-bones structure used here illustrates the underlying trends clearly.

TABLE I
DESIGN REQUIREMENTS FOR SCALING TEST

| | |
|---|---|
| $V_{DD}$ | process defined |
| $L_{min}$ | process defined |
| SNDR | $>$ 66dB (input-referred) |
| Output Range | $0.8{\cdot}V_{DD}$ (per side) |
| Sampling Speed | $13.5/L_{min}$ MHz |
| Total Load | 800fF (differential) |
| Power | minimize |

The predictive technology models provided by [7] were used to implement and simulate the design in the 130 nm, 90 nm, 65 nm, 45 nm, and 32 nm nodes. The results in Fig. 8 indicate that the core ring amplifier structure does indeed scale according to process technology (note the logarithmic scale of the y-axis). In the upper curve, which depicts the total energy-per-cycle with respect to $f_s$ (and thus $L_{min}$), the slope decreases after 45 nm. This is due to the fact that the load capacitance is not scaled (for thermal noise reasons), causing dynamic energy to eventually dominate the total energy per cycle. The fundamental lower bound for dynamic power can be directly calculated for this design, since the output load is deliberately reset to mid-rail every cycle and configured such that its envelope is that of a sine wave. This dynamic power is thus calculated as

$$P_{\mathrm{CV^2f}} = 800\ \mathrm{fF} \cdot \left(\frac{0.8\ \mathrm{V_{DD}}}{\sqrt{2}}\right)^2 \cdot f_s. \tag{13}$$

The energy-per-cycle with respect to the total power minus the $CV^2f$ power of (13) is shown in the lower trend line of Fig. 8. The ringamp's internal power continues to scale at pace into deep nanoscale nodes, and somewhat remarkably, the primary power contributor eventually becomes the ideal dynamic charging power itself. While this is a very encouraging result, there are many scaling effects that are not represented here that will cause the real trend to differ somewhat. In particular, the interconnect R, L, and C parasitics of the circuit are not modeled, which in upcoming nanoscale processes will become an increasingly dominant effect [8]. However, because digital circuits are also influenced by interconnect parasitics, whatever effect this has on ringamp performance will likely also affect digital circuits, and relative scaling trends will persist. The intrinsic device gains that determine the properties of $A_1$, $A_2$, $\hat{A}_1$, $\hat{A}_2$, $M_{\mathrm{CN}}$, and $M_{\mathrm{CP}}$ also change with scaling. For the designs represented in Fig. 8, sufficient inverter gains were maintained with device dimension adjustments alone (although architectural changes are also an option). Although scaling of planar transistors to 22 nm would begin to create challenges in maintaining sufficient gain in a three stage ringamp structure, newer process technologies appear to avoid this problem altogether. The good intrinsic FinFET device gains demonstrated in [1] indicate that the technologies being used in sub-32 nm nodes such as FinFET and silicon-on-insulator (SOI) are able to control short-channel effects much better than previous technologies, and can produce more than sufficient intrinsic device gains for practical ringamp applications.

TABLE II
CHARACTERIZATION ADC SUMMARY OF PERFORMANCE

| | |
|---|---|
| Resolution | 10.5 bits |
| Analog Supply | 1.3 V |
| Sampling Rate | 30 Msps |
| ERBW | 15 MHz |
| Input Range | 2.2 V pk-pk diff. |
| SNDR | 61.5 dB |
| SNR | 61.9 dB |
| SFDR | 74.2 dB |
| ENOB | 9.9 bits |
| Total Power | 2.6 mW |
| FoM | 90 fJ/c-step |
| Technology | 0.18 $\mu$m 1P4M CMOS |
| Active Area | 0.50 mm$^2$ (2.00 mm x 0.25 mm) |

## V. CHARACTERIZATION ADC

To demonstrate the properties that we have discussed in Sections III and IV, a 10.5-bit pipelined ADC was implemented and tested [9]. The ADC consists of nine identical 1.5-bit switched capacitor MDAC stages followed by a 1.5-bit backend flash. The transistor-level ringamp used is shown in Fig. 9. As we can see from the listed device sizes, the ringamp is quite small, and even the largest transistor in the design is only 2$\times$ the minimum W/L allowed by the process. In each stage, two of these single-ended ringamps are placed in the pseudo-differential configuration shown in Fig. 10. Due to the lack of common-mode feedback (CMFB) in such a configuration, the MDAC employs the 1.5 b flip-around pseudo-differential float sampling scheme of [10]. This scheme sets the differential-mode gain to 2 and the common-mode gain to 1. Thus, any common-mode errors along the pipeline will simply add, rather than multiply and potentially saturate the common-mode level.

The pipelined ADC was fabricated in a 1P4M 0.18 $\mu$m CMOS technology. A summary of performance is given in Table II. At 30 MHz sampling rate, the ADC achieves 61.5 dB SNDR, 61.9 dB SNR, and 74.2 dB SFDR. Total power consumption is 2.6 mW, with approximately 90 $\mu$W consumed per stage by the psuedo-differential ring amplifier block. The measured ERBW is greater than 15 MHz, and the figure-of-merit (FoM) is 90 fJ/conversion-step. Neither speed nor power were prioritized in this design (only accuracy), and with a more aggressive design and use of the power saving techniques discussed in Section VI, both can be improved significantly. The unit capacitor size for all MDAC stages is 200 fF, yielding a total differential input capacitance of 800 fF. The output spectrum is shown in Fig. 11, and the performance with respect to input frequency is given in Fig. 12(a).

Despite such small device sizes, the actual noise contribution from the ringamp is quite small. This highlights another key benefit of ring amplifiers: because the output pole of the ringamp will be at very low frequency or even DC at the end of the amplification period, any internal noise sources will be heavily attenuated at the output.

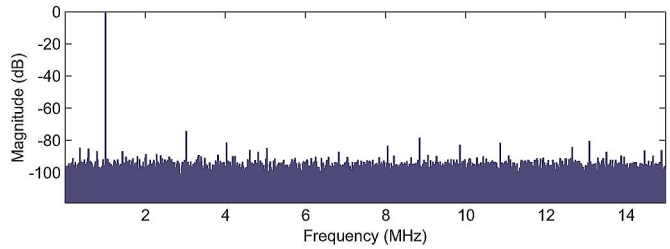


Fig. 11. Measured output spectrum of the characterization ADC for a 1 MHz input tone sampled at 30 Msps.

To demonstrate the key scalability benefit of output-swing compression immunity, the analog supply was reduced to 1.2 V, the MDAC references were set to the supply voltages (0 V and 1.2 V), and the sampling frequency was reduced to 4 MHz, with all other settings left unchanged. The results of an input amplitude sweep under this test setup is presented in Fig. 12(b). Because the transfer function of a 1.5 b MDAC spans the entire supply range, a rail-to-rail input signal will cause the ringamps to swing rail-to-rail at their outputs as well [11]. With this in mind, we see from Fig. 12(b) that the ringamp maintains linearity even in true rail-to-rail operation, and only begins to degrade within $\pm$15 mV of $V_{\rm DD}$ and $V_{\rm SS}$ due to insufficient RC settling time.

Fig. 12(c) shows the effect of dead-zone variation on performance. As can be seen, there is a wide, stable range of dead-zone values for which SNDR is largely unchanged. The roll-off on the right is due to (1), and the roll-off on the left is due to the ringamp becoming unstable. The SNDR plateau in the middle is a reflection of quantization and thermal noise limiting SNR in that region. The SFDR curve, by contrast, shows that distortion improves continuously to a peak value, not a plateau. The SFDR peak is somewhat compressed by the linearity of the frontend sampling switches, which are also the primary cause of the roll-off in Fig. 12(a). The bootstrapped sampling switches in both this design and the design of Section VI did not operate as expected due to an unintentionally fabricated deep N-well conduction path, and caused additional distortion and power consumption. The plot of ringamp supply current consumption in the first pipeline stage with respect to applied dead-zone size in Fig. 12(d) indicates that the faster a ringamp stabilizes, the less power it will consume (as one would expect). On the left half of this plot, where the dead-zone is less than 0 mV, the structure becomes a ring oscillator.

## VI. HIGH-RESOLUTION SPLIT-CLS ADC

In this section we will explore the design, features, and measured results of a 15-bit Split-CLS pipelined ADC. In a broader sense, this design describes a way to utilize ring amplifiers in the realm of high-accuracy switched-capacitor circuits.

### A. Split-CLS

Beyond their usefulness as a stand-alone technique, ring amplifiers are also prime candidates to be integrated into other techniques which require an amplifier that is both fast and efficient at charging large capacitive loads. One such technique that is ideally suited for ring amplifiers is that of Split-CLS [12], [13]. (In

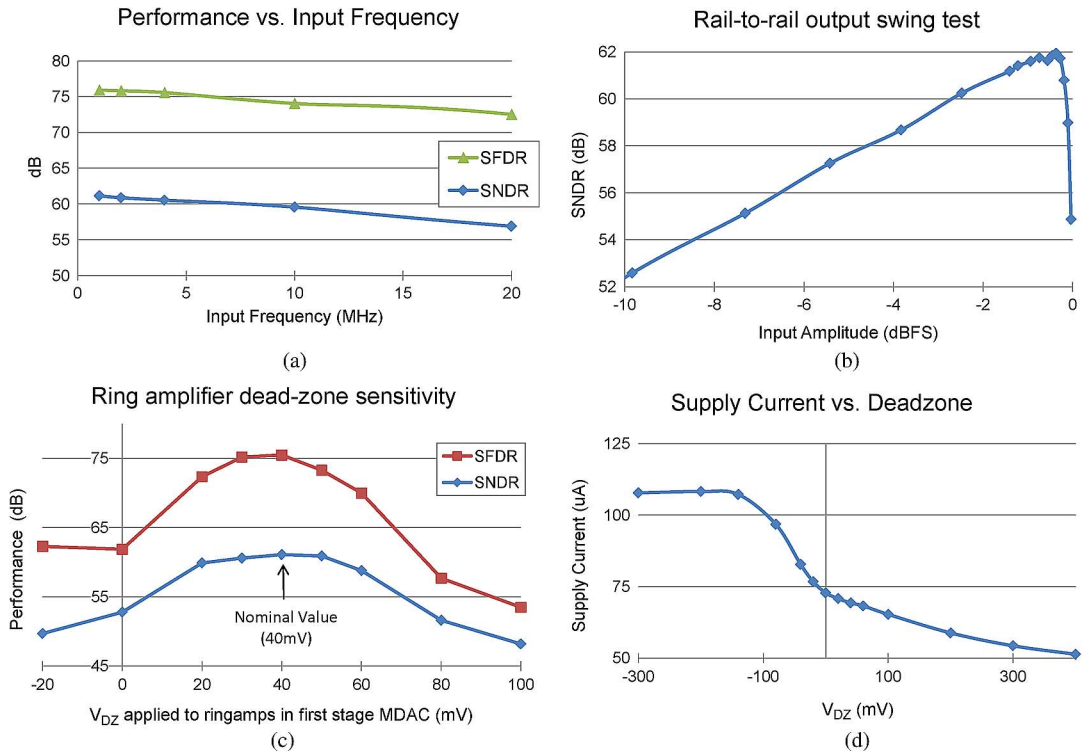


Fig. 12. Measured performance and characterization data for the 10.5-bit ADC.

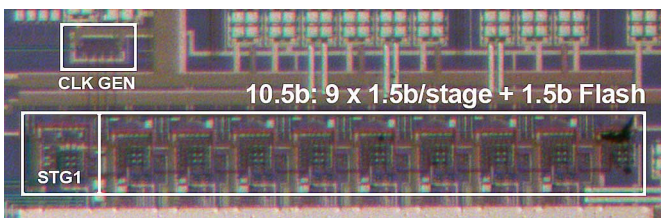


Fig. 13. Die micrograph of the 10.5b characterization ADC.

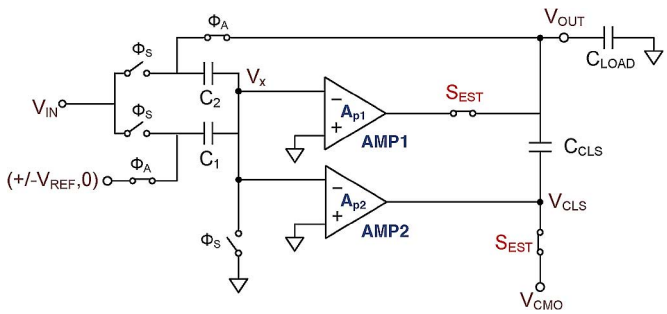


Fig. 14. A basic 1.5 b MDAC implementation of the Split-CLS technique. The effective gain at the end of $\phi_{\rm A}$ will be proportional to $A_{p1} \cdot A_{p2}$.

fact, it was the author's desire for a good Split-CLS coarse amplifier that inspired the idea of ring amplifiers in the first place). The basic concept of Split-CLS (split correlated level shifting) is illustrated in the single-ended switched capacitor MDAC of Fig. 14. The amplification phase, $\phi_{\rm A}$, is sub-divided into an estimation phase and a fine settling phase. In the first sub-phase, the switches $S_{\rm EST}$ are asserted, and AMP1 charges an estimate of the final settled value onto the output. Meanwhile, the capacitor $C_{\rm CLS}$ samples this estimation value and the output of AMP2 is shorted to mid-rail and held in standby. In the second sub-phase, the switches $S_{\rm EST}$ are de-asserted and AMP1 is disconnected from the output (and can be disabled). Meanwhile, AMP2 is coupled into the output via $C_{\rm CLS}$ and begins to fine-settle the output towards its ideal value. The key benefit derived from this operation is that by level-shifting the output of AMP2 back to mid-rail, AMP2 will process the error only, and the finite opamp gain error at its input will be substantially reduced. The final effective loop gain of the structure at the end of the amplification phase will thus be proportional to the product of the two independent amplifier gains:

$$A_{\rm eff} \approx \psi \cdot A_{p1} \cdot A_{p2} \tag{14}$$

where

$$\psi = \frac{\rm C_{CLS}}{\rm C_{CLS} + C_{LOAD} + \dfrac{C_1 \cdot C_2}{C_1 + C_2}} \cdot \left(\frac{\rm C_2}{\rm C_1 + C_2}\right)^2. \tag{15}$$

Thus, for a 55 dB accurate AMP1, and a 65 dB accurate AMP2, with $C_{\rm CLS} = C_{\rm LOAD} = 2C_1 = 2C_2$, the total effective loop gain at the end of $\phi_{\rm A}$ will be more than 100 dB. For a complete explanation of this analysis, see [14] and [15].

Consider for a moment the requirements of AMP1 and AMP2 during their respective phases of operation. AMP1 charges the output load directly, and must have a high slew rate and wide output swing. By contrast, AMP2 only processes the small error term left over from AMP1, and requires a much smaller output swing and slew rate. The key idea of Split-CLS is that by choosing amplifiers that are ideally suited for the differing requirements of AMP1 and AMP2, we can maximize the accuracy and efficiency of the overall structure. Ring amplifiers are clearly an attractive choice for AMP1, particularly in high-resolution designs where kT/C noise constraints require a relatively large loading capacitance. Due to the small output

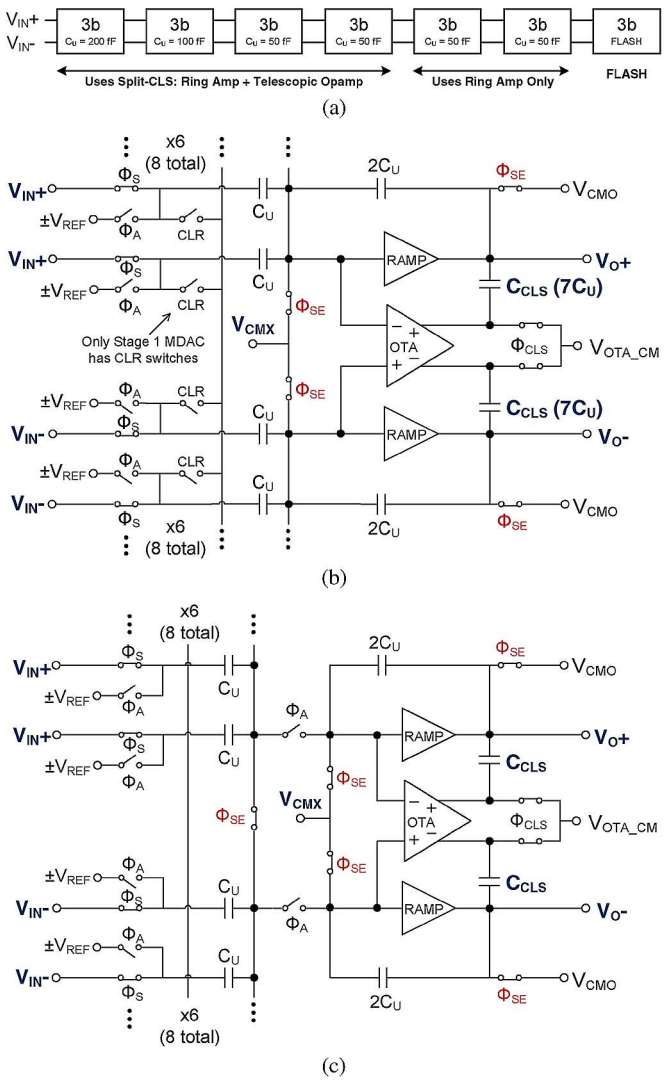


Fig. 15. Structural details of the 15-bit ADC. (a) Top level architecture, (b) the fully-differential Split-CLS 3-bit/9-level MDAC used for stage 1, and (c) the float-sampled, pseudo-differential Split-CLS MDAC used in stages 2–4. The stage 5–6 MDACs are the same as Fig. 15(c) except with the opamp and $C_{\mathrm{CLS}}$ removed.

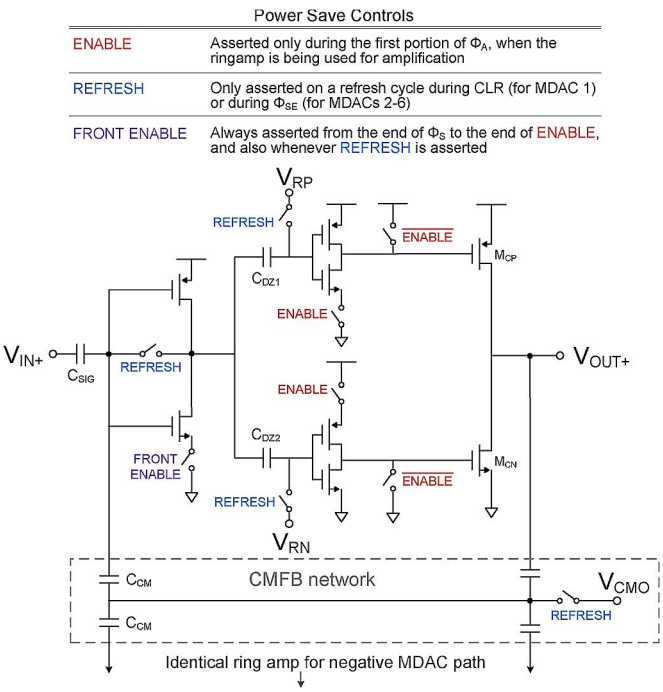


Fig. 16. Ring amplifier with power-save features and CMFB network used in the high-resolution ADC.

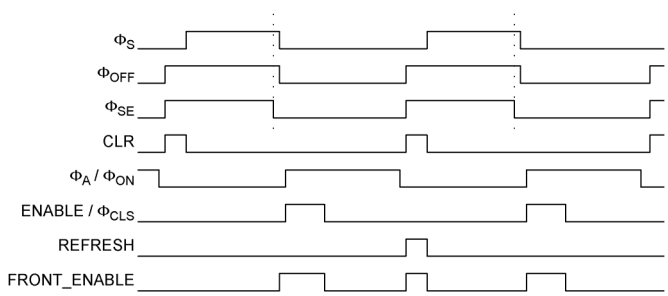


Fig. 17. Timing diagram for the first stage MDAC of Fig. 15(b) including the signals used by the ringamp of Fig. 16 and opamp of Fig. 18. The first clock period depicts a regular cycle, and the second depicts a refresh cycle. The timing for the latter MDAC stages is slightly different, with CLR removed (and $\phi_{\mathrm{S}}$ becoming $\phi_{\mathrm{OFF}}$), and REFRESH active during all of $\phi_{\mathrm{SE}}$.

swing requirement of AMP2, a single stage telescopic opamp is a good candidate even in low supply voltages, and provides superior gain and bandwidth for a given power budget compared to other conventional opamp structures. For the cautious designer, this combination is particularly appealing—one can benefit from the advantages of ring amplifiers and still have the final settled accuracy be determined by a conventional opamp.

To demonstrate the effectiveness of this pairing, the high resolution pipelined ADC of Fig. 15(a) is presented. The pipeline resolves 15 bits with 6 MDAC stages and a 3-bit backend flash. The first four stages employ Split-CLS (and stages 5 and 6 use ring amplifiers only). The fully-differential 3-bit/9-level first stage MDAC, shown in Fig. 15(b), uses two pseudo-differentially configured ringamps of Fig. 16 as the AMP1 coarse charging device and the opamp of Fig. 18 as the AMP2 fine settling device. A digitally programmable delay line controls the time allotted to the ringamp's coarse charge operation ($\phi_{\mathrm{CLS}}$), and the remainder of $\phi_{\mathrm{A}}$ is used by the opamp. A timing diagram for the first stage MDAC is given in Fig. 17. Due to the fact that the opamp common-mode feedback (CMFB) is applied at the opamp output (and not the stage output), the pseudo-differential ring amplifiers must control the stage output's common-mode voltage. The simple capacitive CMFB network depicted in Fig. 16 provides an effective solution. The CMFB gain must be several times smaller than the gain of the primary feedback paths, and can be configured by selecting the appropriate capacitor ratio between $C_{\mathrm{SIG}}$ and $C_{\mathrm{CM}}$. While this simple CMFB is adequate for most uses, it has inherently low common-mode accuracy, and under extreme circumstances may be insufficient. Therefore, to further relax the CMFB requirement, the stage 2–6 MDACs employ a 3-bit/9-level pseudo-differential MDAC similar to the 1.5 b flip-around MDAC of Fig. 10, but with a fixed feedback capacitor. Shown in Fig. 15(c), this scheme sets the differential-mode gain to 4 and the common-mode gain to 1. Split-CLS is not needed in stages 5 and 6, where the accuracy requirement is low, and to

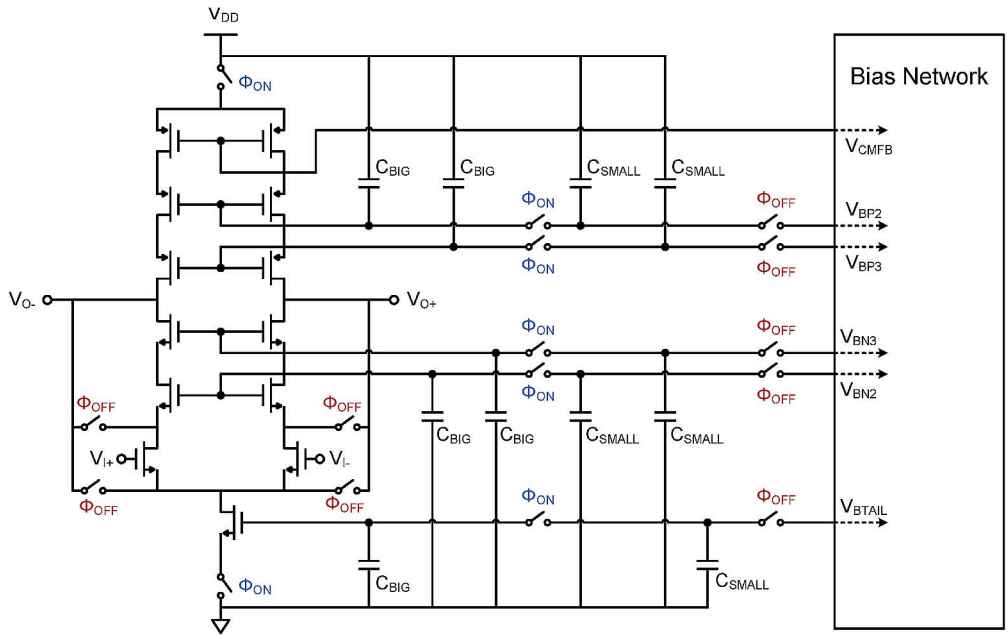


Fig. 18. The double-cascoded fully differential opamp used in the first four MDACs. The charge-biased opamp switching scheme shields the bias network from power-up and power-down voltage kickback.

save power the opamp and level-shifting capacitors ($C_{\rm CLS}$) are removed from these stages.

### B. Ringamp Power-Save Features

The ringamp shown in Fig. 16 is implemented almost identically in all stages, with only $M_{\rm CN}$ and $M_{\rm CP}$ sized differently in order to maintain the same slew rate across the differing output load sizes. For the vast majority of each period, the ringamp is unused, and can be disabled. This power-saving feature is implemented with the additional 'ENABLE' and 'FRONT ENABLE' switches depicted in Fig. 16. It is also important that the ringamp be completely disconnected from the output while the opamp is settling, and this operation guarantees that as well.

The input-offset and dead-zone voltages stored across capacitors $C_{\rm SIG}$, $C_{\rm DZ1}$, and $C_{\rm DZ2}$ must be refreshed periodically, and when doing so, the first stage inverter must be active (although the second and third stages can remain off). Therefore, during a refresh, the signals 'REFRESH' and 'FRONT ENABLE' will be asserted. These refresh operations must be done at a time when the ringamp is not in use. Although there are several options, a good choice for when to do the refresh in stage 1 is during the short window when 'CLR' is asserted and the input sampling capacitors are shorted together and cleared. At the end of this clearing pulse, the virtual node will be exactly equal to $V_{\rm CMX}$, allowing an accurate value to be sampled on $C_{\rm SIG}$. Performing the refresh operation while the input capacitors are sampling is also possible, but somewhat less accurate, because there will be a signal-dependent voltage drop across the virtual node sampling switch ($\phi_{\rm SE}$) that will also be sampled onto $C_{\rm SIG}$. However, for the later stages this problem does not exist, since the sampled signal is completely settled at the end of $\phi_{\rm SE}$, and thus $\phi_{\rm SE}$ is used as the refresh signal in these stages. The charge stored on $C_{\rm SIG}$, $C_{\rm DZ1}$, and $C_{\rm DZ2}$ will only be corrupted by small parasitic leakage currents, and it is sufficient to perform a refresh only once every N cycles (where N is controlled by an on-chip digital counter). Such an approach is used in this design, and reduces the contribution of additional static power due to refresh periods down to negligible levels. For the majority of conversion cycles, the ringamp is only briefly on at the beginning of $\phi_{\rm A}$, and completely off during the rest of the period.

TABLE III
SPLIT-CLS ADC SUMMARY OF PERFORMANCE

| | |
|---|---|
| Resolution | 15 bits |
| Analog Supply | 1.3 V |
| Sampling Rate | 20 Msps |
| ERBW | 10 MHz |
| Input Range | 2.5 V pk-pk diff. |
| SNDR | 76.8 dB |
| SNR | 77.2 dB |
| SFDR | 95.4 dB |
| ENOB | 12.5 bits |
| Total Power | 5.1 mW |
| FoM | 45 fJ/c-step |
| Technology | 0.18 $\mu$m 1P4M CMOS |
| Active Area | 1.98 mm$^2$ (3.05 mm x 0.65 mm) |

### C. Charge-biased Switched Opamp

To save additional power in the opamps, the switched opamp scheme of Fig. 18 is used. The opamp is only enabled during $\phi_{\rm A}$ (of Fig. 15), and uses the time at the beginning of $\phi_{\rm A}$ when the ringamps are amplifying to power up. Shorting switches are placed on the source and drain nodes of the input transistors to

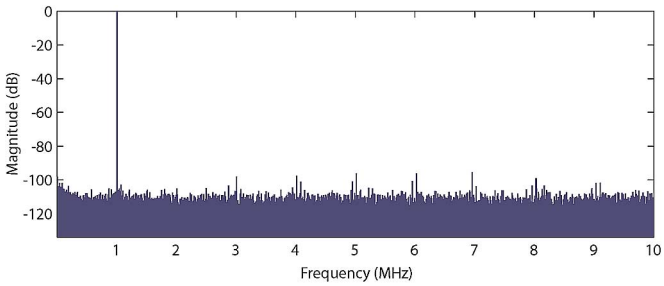


Fig. 19. Measured output spectrum of the high-resolution Split-CLS ADC for a 1 MHz input tone sampled at 20 Msps.

ensure that any kickback onto the MDAC virtual node during power-on will be signal independent.

In the conventional switched opamp approach, the bias lines are directly connected to the opamp, and both the power-up and power-down operations will kick charge from the parasitic capacitances of the main opamp transistors onto the bias network. The bias network must then try to absorb this kickback and re-settle to the correct bias voltages, which will increase the required power-on time of the opamp [16]. Our proposed solution to this problem is to bias the opamp in charge-domain rather than voltage-domain, as shown in Fig. 18. Imagine for a moment that $\phi_{\rm ON}$ is asserted, the opamp is amplifying, and the $C_{\rm BIG}$ capacitors hold the correct charge to properly bias the opamp. When the amplification period ends and $\phi_{\rm OFF}$ asserts, the opamp will switch off and a large amount of voltage will kickback onto $C_{\rm BIG}$. However, since the top-plate of $C_{\rm BIG}$ has no DC path to ground during $\phi_{\rm OFF}$, the charge stored on it is trapped. Meanwhile, a set of small capacitors ($C_{\rm SMALL}$) sample the bias network. Then, when the opamp is powered on again, $C_{\rm BIG}$ will be shorted to $C_{\rm SMALL}$ and some amount of charge transfer will occur. Since this charge transfer occurs during $\phi_{\rm ON}$, there is no unwanted voltage kickback present, and $C_{\rm SMALL}$ will update $C_{\rm BIG}$ with an incremental piece of charge corresponding to the correct bias voltage. This bucket-brigade that $C_{\rm SMALL}$ provides between the bias network and $C_{\rm BIG}$ isolates the bias network from opamp kickback and enables rapid power-up.

### *D. Measurement Results*

The 15-bit pipelined ADC was fabricated in a 1P4M 0.18 $\mu$m CMOS process. A summary of performance is given in Table III. At 20 MHz sampling rate it achieves 76.8 dB SNDR (12.5 ENOB), 77.2 dB SNR and 95.4 dB SFDR, consuming 5.1 mW. The ERBW is found to be above 10 MHz, which results in a Figure-of-Merit of 45 fJ/conv-step. The MDAC references are set at 25 mV and 1275 mV, allowing the input signal to utilize 96% of the available supply range. Capacitor matching was good enough that no digital calibration was needed. The first stage MDAC unit capacitance is 200 fF, giving a total differential input capacitance of 3.2 pF (or 3.76 pF when the Flash sub-ADC capacitors are included). Total accuracy is fundamentally limited by noise, and the SNR is almost exactly equal to the kT/C noise limit predicted for this design. Due to jitter injected by the off-chip clock source and internal clock generator, noise also becomes a limitation with

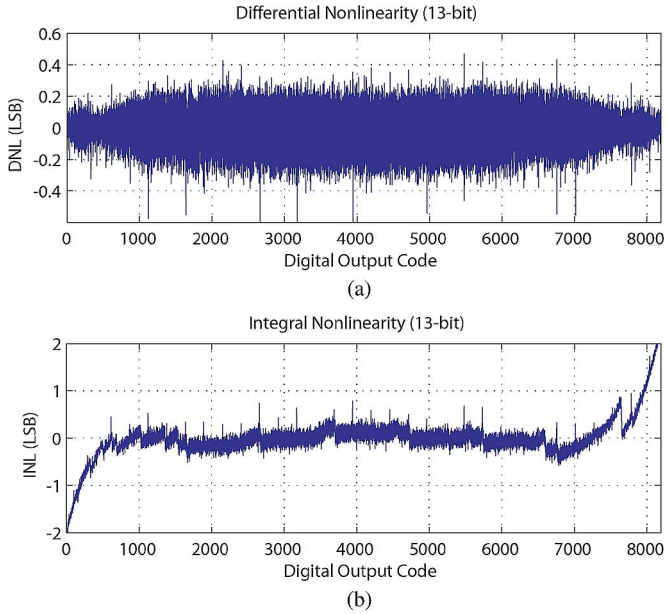


Fig. 20. Measured DNL (top) and INL (bottom) normalized to LSB $= 2^{-13}$.

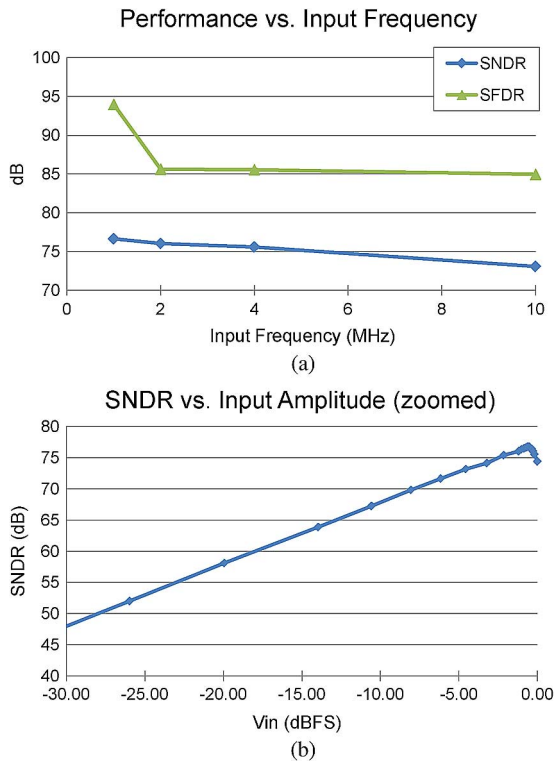


Fig. 21. Measured input signal performance data for the high-resolution Split-CLS ADC.

respect to input frequency, as seen in Fig. 21(a). A relatively conservative design target of 20 Msps was chosen in order to manage risk and ensure that the key features of accuracy and power efficiency would be demonstrated, and with a few modifications higher speeds are certainly possible.

Stage scaling is performed for the first three stages, with the unit capacitance for each stage listed in Fig. 15(a). To minimize power, the 3-bit/9-level flash sub-ADCs of stages 2–7 use an architecture similar to [17], where the only load placed on the

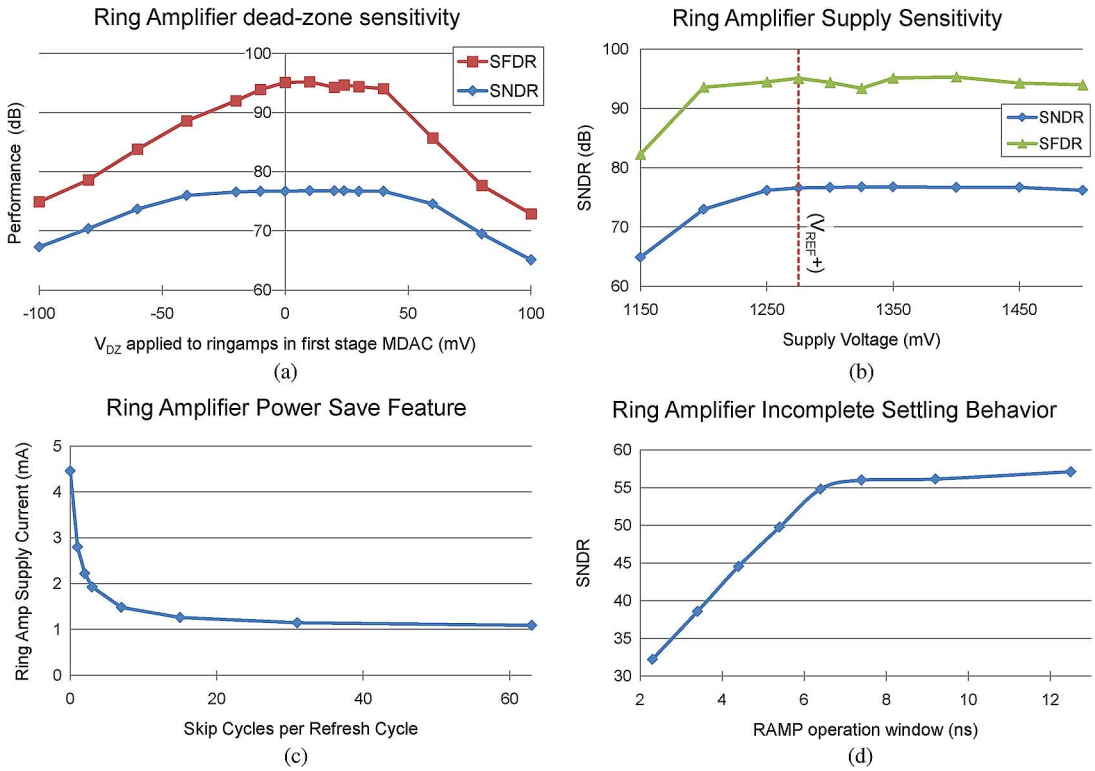


Fig. 22. Measured ringamp sensitivity and characterization data for the high-resolution Split-CLS ADC.

previous stage's output will be due to the gate capacitance of the 8 sub-ADC latches. In order to minimize aperture and skew related errors for fast moving inputs, the first stage's sub-ADC uses the opposite approach, in which the moving input signal is first sampled, then subtracted from the reference and quickly latched.

All analog portions of the circuit operate at 1.3 V, including the ringamps and opamps. Opamp switching is measured to reduce the total opamp power by 35%, and improve SNDR by 0.6 dB. An unfortunate issue with the physical layout caused a node in the bootstrapped input sampling switches to be shorted into a deep-nwell substrate, causing them to operate as NMOS-only statically biased switches. In order to compensate, the digital and switch supply had to be operated above 1.3 V. Based on follow-up simulations and measurements, this issue is estimated to have increased total power consumption by approximately 23%, and is included in the 5.1 mW reported. The impact on performance can be seen in the end-code non-linearity in Fig. 20(b), and in the roll-off above $-0.6$ dBFS in Fig. 21(b). For this reason, the output spectrum of Fig. 19 and results in Table III are collected for a $-0.6$ dBFS input signal.

When the sampling frequency is increased to the point that the opamps never have a chance to amplify, the contribution of the ringamps to overall accuracy can be measured, and is found to be 55 dB SNDR at $f_s = 80$ MHz. This result is also confirmed by the result of Fig. 22(d), where the digitally controlled timing generator that sets the ringamp amplification window is swept with the opamps disabled. What we find is that ringamp performance decreases logarithmically with respect to incomplete settling time, and that the ringamp settles to about 55 dB SNDR in roughly 6 ns.

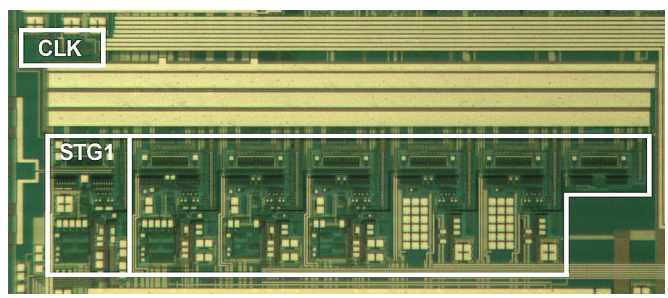


Fig. 23. Die micrograph of the active area of the high-resolution Split-CLS ADC.

The ADC exhibits a high tolerance to dead-zone variation, as shown in Fig. 22(a) and (b). In Fig. 22(a), the dead-zone applied to the ringamps in the 1st stage MDAC is swept with everything else held constant. For the most part, this plot tells the same story as Fig. 22(c) of Section V, with the roll-off above $+50$ mV due to the dead-zone becoming large and increasing distortion and the roll-off below $-50$ mV due to the ringamps going unstable. The curve's peak has a systematic offset of roughly $-25$ mV, and is caused by the asymmetry of the 'ENABLE' switches that control the second stage inverters of Fig. 16. The true effective dead-zone of the ringamp is the sum of $V_{\mathrm{DZ}}$ plus any inherent systematic offsets, including this asymmetry. The opamp, via Split-CLS, helps to absorb small errors and further flattens the SNDR curve of Fig. 22(a) into a wide stable plateau where kT/C noise is the fundamental limitation of SNDR. The SFDR curve contains a plateau region as well, which occurs when distortion effects other than finite gain begin to dominate, such as input-switch linearity. When

the ring amplifier supply voltage is swept with all other voltages and biases held constant (Fig. 22(b)), SNDR and SFDR are virtually unchanged. At 1275 mV the supply voltage equals the positive MDAC reference, and explains the roll-off seen below that point.

The benefit of the ringamp power-save feature is demonstrated in Fig. 22(c). Total ringamp power consumption is reduced by about 4.5× when the ringamps are only refreshed once every 64 cycles. For the ADC presented in Section V, switching the ringamps off during $\phi_S$ could have reduced ringamp power by almost 50%.

## VII. Conclusion

Looking back at the individual benefits of a ring amplifier we find many parallels with other pre-existing techniques: zero-crossing based circuits also have the ability to charge efficiently and decouple internal power from external load requirements [4], [5], dynamic current adjustment is a common attribute of class-AB amplifiers in general [18], using simple inverter-based amplifiers has long been a topic of interest [10], [19]–[21], and CLS can already be used to achieve rail-to-rail output swing [15]. Ultimately, it is both logical and encouraging that we should find such similarities. Each one of these parallels represent a specific trait desired in a scalable amplifier topology, and the fact that a ring amplifier encompasses all of them indicates that it is a convergence point for many lines of research in scalable amplification. In other words, the unique aspect of a ring amplifier lies not in the traits that it possesses, but rather in the particular solution by which it is able to embody them all.

In this paper we have laid out the basic theory of ring amplification, discussed the key benefits that it brings to scaled CMOS, and studied two examples of its practical implementation. We have primarily considered the specific case of a medium-accuracy ring amplifier structure suited for use in switched capacitor circuits. As demonstrated in this paper, this simple ringamp incarnation is highly effective, and can be integrated into more complex topologies, such as Split-CLS, to cover a range of speed and accuracy targets. And yet, the concepts of ring amplification are applicable to a broader range of structural approaches, and what we have examined here is simply the foundation for a deeper exploration of the topic.

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**Benjamin Hershberg** (S'06–M'12) received H.B.S. degrees in both electrical engineering and computer engineering from Oregon State University, Corvallis, in 2006, and the Ph.D. degree in electrical engineering from Oregon State University in 2012. His dissertation work has concentrated on the development of scalable, low-power switched-capacitor amplification solutions, including the techniques of ring amplification and split-CLS.

**Skyler Weaver** received the H.B.S. degree in electrical engineering from Oregon State University, Corvallis, in 2006. He received the Ph.D. degree in electrical engineering from Oregon State University in 2010 researching synthesizable ADCs.

He is currently working with Intel Corporation, Hillsboro, Oregon, researching scalable high-speed serial links.

Dr. Weaver received the ICECS Best Paper Award in 2009.

**Kazuki Sobue** was born in Aichi, Japan, in 1972. He received the B.S. degree in information engineering from Nagoya University, Aichi, Japan, in 1995.

Then he joined the Design and Development Center of Asahi Kasei Microdevices Corporation, Atsugi, Japan. He has been engaged in the design and development of CMOS mixed-signal LSIs for audio. His current interest is in the development of high-speed and low-power ADCs.

**Seiji Takeuchi** was born in Shizuoka, Japan, in 1961. He received the B.S. degree in applied physics engineering from Tohoku University, Miyagi, Japan, in 1984.

He joined Asahi Kasei in 1984. Since then, he has been engaged in the design of CMOS LSIs especially in the field of high speed ADC and DAC. He is currently Section Manager of Asahi-Kasei Microdevices Corporation, Atsugi, Japan.

**Koichi Hamashita** (M'89) was born in Ishikawa, Japan, in 1957. He received B.S. and M.S. degrees in mechanical engineering from Kyoto University, Kyoto, Japan, in 1979 and 1981, respectively.

He joined Asahi Kasei in 1981. Since 1985, he has been engaged in the design of CMOS LSIs especially in the field of delta-sigma ADC and DAC. He is currently CTO Executive Officer of Asahi-Kasei Microdevices Corporation, Atsugi, Japan.

**Un-Ku Moon** (S'92–M'94–SM'99–F'09) received the B.S. degree from the University of Washington, Seattle, in 1987, the M.Eng. degree from Cornell University, Ithaca, NY, in 1989, and the Ph.D. degree from the University of Illinois at Urbana-Champaign in 1994.

He has been with the School of Electrical Engineering and Computer Science, Oregon State University, Corvallis, since 1998. Before joining Oregon State University, he was with Bell Laboratories from 1988 to 1989, and from 1994 to 1998. His technical contributions have been in the area of analog and mixed-signal circuits including high linearity filters, timing recovery, PLLs, data converters, and low voltage circuits for CMOS.

Dr. Moon is the Editor-in-Chief of the IEEE JOURNAL OF SOLID-STATE CIRCUITS. He also serves on the Technical Program Committee of the IEEE International Solid-State Circuits Conference. He has served as a Distinguished Lecturer of the IEEE Solid-State Circuits Society, as an Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, as Editor-in-Chief and Deputy Editor-in-Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II, as IEEE Solid-State Circuits Society representative to IEEE Circuits and Systems Society, and as a Technical Program Committee member of the IEEE VLSI Circuits Symposium and the IEEE Custom Integrated Circuits Conference.