Process Invariant Biasing of Ring Amplifiers Using Deadzone Regulation Circuit

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***Abstract*—In this paper, process invariant biasing is proposed for robust operation of ring amplifiers. The ring amplifier is an efficient solution for high accuracy amplification in sub-micron CMOS process. A traditional ring amplifier structure requires an external control voltage, defined as the deadzone voltage, to set the optimum quiescent current at the output stage. Other structures of ring amplifiers use on-chip resistors or current starved inverters to set the deadzone voltage. Since the deadzone voltage is a function of the threshold voltage of transistors in the output stage inverter, ring amplifiers are susceptible to process variations. In this paper, a deadzone regulation circuit is proposed that utilizes a constant current source and a negative feedback loop to regulate the quiescent current of the output stage inverter across process corners. Transistor level simulations are used to validate the operation of the proposed deadzone regulation technique across FF, TT and SS corners in a 65nm CMOS process. The design example uses a current starved inverter based ring amplifier in a switched capacitor amplifier to achieve a closed loop gain of 4 with a settling accuracy of $\leq$ 0.05% and operated at a sampling rate of 125MHz.**

***Index Terms*—Ring Amplifiers, Process variation, PVT biasing, Switched Capacitor Amplifier, High resolution ADCs.**

I. Introduction

With the increasing demand for high efficiency battery powered devices, there is a significant drive to design low power analog circuits that integrate with the digital circuits in the latest CMOS processes. In sub-micron CMOS process, the reduced intrinsic gain and the reduced voltage swings make the conventional operational transconductance amplifiers (OTAs) [1] inefficient in performing low power and high accuracy amplification.

In the recent years, ring amplifiers [2]–[11] have emerged as a power efficient solution to achieve high accuracy amplification with rail to rail output swings. However, the traditional ring amplifier [2] requires external reference voltage, defined as the deadzone voltage, for optimum performance. Other structures of ring amplifiers have been proposed in [3]–[5]. The structure in [3], [4] requires an on-chip resistor to create the deadzone voltage. The structure in [5] uses current starved inverters to create the deadzone voltage. The deadzone voltage is used to optimally set the quiescent current in the output stage of a ring amplifier and it is a function of the threshold voltage of the transistors. This makes ring amplifiers susceptible to process variations.

In this paper, a deadzone regulation circuit is proposed that automatically tunes the deadzone voltage across process variations to regulate the quiescent current flowing through the output stage inverter. To demonstrate the operation, the proposed technique is applied to a current starved inverter based ring amplifier [5]. However, the technique can also be applied to a traditional ring amplifier [2] and the resistor based ring amplifiers [3]–[11] in general.

The organization of the paper is as follows. Section II provides a brief overview of the operation of a ring amplifier and the existing deadzone biasing structures. Section III describes the effect of process variation on the small signal ac response and transient response of a ring amplifier, with a current starved inverter based ring amplifier as a design example. Section IV describes the proposed deadzone regulation circuit. Simulation results are discussed showing the effectiveness of the technique across TT, FF and SS process corners. Section V concludes the paper.

II. Overview of Ring Amplifiers and Existing Deadzone Biasing Structures

This section describes: A) The basic concept of the dynamic operation of a ring amplifier, B) The existing deadzone biasing structures for a ring amplifier.

A. Dynamic Operation of a Ring Amplifier

To illustrate the concept of a ring amplifier, consider the basic structure of the three stage ring amplifier in a switched capacitor negative feedback loop as shown in Fig. 1. The structure of the ring amplifier is similar to a three stage ring oscillator, but with an embedded offset voltage defined as the deadzone voltage at the input of the second stage inverter (VDZ_P and VDZ_N in Fig. 1) [2]. Without the deadzone voltage, the circuit tends to oscillate due to the absence of compensation in the loop. However, with the appropriate deadzone voltage, the output stage inverter is biased with a very low quiescent current, I_Q. This results in a dominant pole at the output, that dynamically stabilizes the negative feedback loop.

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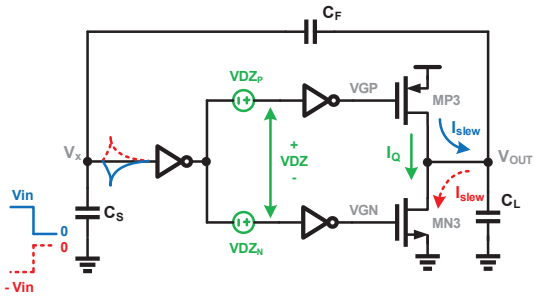

Figure 1. Traditional ring amplifier in a switched capacitor negative feedback [2].

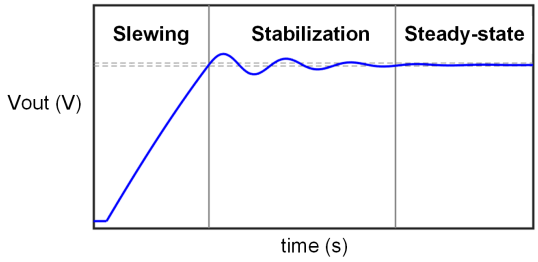

Figure 2. Settling response of a ring amplifier.

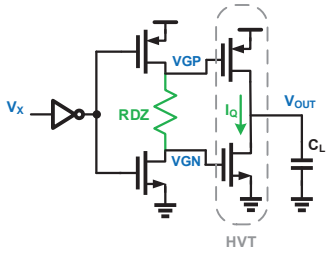

Figure 3. Ring amplifier using a resistor for deadzone biasing [3].

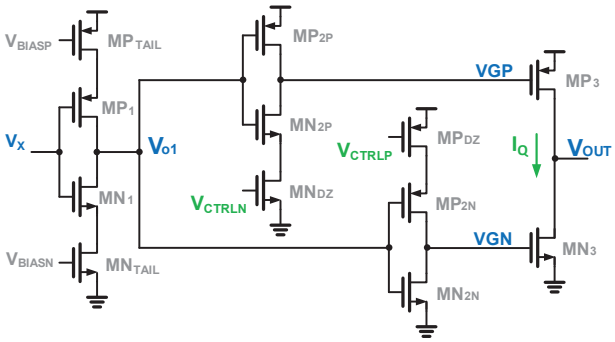

Figure 4. Ring amplifier using current starved inverters for deadzone biasing [5].

The transient response of a ring amplifier mimics the response of a conventional operational transconductance amplifier (OTA) as shown in Fig. 2. Unlike OTAs, the dynamic current in the output stage results in a very low static power consumption. In addition, the inherent slew assist capability relaxes the required loop gain bandwidth product (GBW) of the ring amplifier, which makes it highly power efficient in achieving high accuracy amplification in switched capacitor circuits. The transient response is divided into three phases: the slewing phase, the stabilization phase and the steady state [2].

During the slewing phase, the first two stages (Fig. 1) act as digital inverters resulting in rail to rail gate voltages at the input of the third stage. This turns on the third stage which charges/discharges the load capacitor with maximum slew current I_{slew}. As the charge across the load capacitor builds up and the output voltage approaches close to the steady state value, the amplifier enters the stabilization phase.

During the stabilization phase, the reduced voltage swing at the virtual ground (node V_X in Fig. 1) causes the ring amplifier to behave like a three stage amplifier with a dynamic dominant pole at the output. Both small signal and large signal stability are essential to minimize the overshoot and ringing during this phase [12]. Finally, the amplifier enters the steady state when the output stage is biased with a very low quiescent current, I_Q resulting in low bandwidth and high settling accuracy.

B. Deadzone Biasing in Existing Ring Amplifier Stuctures

Fig. 3 [3] and Fig. 4 [5] show alternate ring amplifier structures that differ in the way deadzone biasing is implemented. The figures show single ended structure for simplicity. Differential structure is preferred for better supply and common mode rejection. The structure in Fig. 3 implements deadzone biasing using a resistor at the output of the second stage. The structure in Fig. 4 implements deadzone biasing using current starved inverters in the second stage.

Irrespective of the structure of a ring amplifier, the deadzone voltage or the deadzone resistor is chosen such that, the steady state gate voltages (VGP and VGN) of the output stage inverter, bias the output stage to have a very small quiescent current, I_Q. Since the dominant pole of the ring amplifier is due to the output stage inverter, this quiescent current controls the loop gain bandwidth during the small signal operation of a ring amplifier. However, the quiescent current is a function of the threshold voltages of transistors in the third stage inverter.

Thus for a given value of deadzone voltage or deadzone resistor, the quiescent current, I_Q in the output stage can vary across process corners due to variations in threshold voltage. This significantly affects the loop gain bandwidth of the ring amplifier. The effect is discussed with a design example in the next section.

III. Effect of Process Variation on A Ring Amplifier Response

To illustrate the effect of process variation on the performance of a ring amplifier, consider the current starved inverter based ring amplifier in Fig. 4. A fully differential structure is designed in a 65nm CMOS process with a 1.2V supply voltage. A single ended schematic is shown in the figure for simplicity.

For the design example, the ring amplifier is used in the switched capacitor amplifier shown in Fig. 5, which is setup

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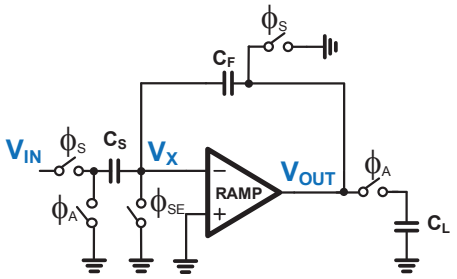

Figure 5. Switched capacitor amplifier setup.

for a closed loop gain of 4 and operated at a sampling rate (F_S) of 125MHz with $C_S = 2pF$, $C_F = 500fF$ and $C_L = 700fF$. The open loop gain of the ring amplifier is designed such that the settling accuracy of the output voltage is $\leq$0.05%.

The small signal gain bandwidth of the loop during the end of stabilization phase is given by (1)

$$GBW_{=} \left(\frac{\beta(0) A_1 A_2 g m_3}{C_{out}} \right) \tag{1}$$

$\beta(0)$ is the feedback factor at dc. $\beta(0) = C_F/(C_F + C_S + C_{IN})$ where C_S, C_F and C_{IN} are the sampling capacitor, feedback capacitor and the input capacitance of the ring amplifier. $C_{out} = C_L + (C_F C_S/(C_F + C_S))$ is the effective load at the output of the amplifier. A_1 and A_2 are the dc gains of the first two stage inverters towards the end of stabilization phase. gm_3 is the transconductance of the third stage inverter towards the end of stabilization phase. Unlike OTAs, the choice of feedback factor can result in varying degrees of small signal and large signal effects on the settling of ring amplifiers [13]. The discussion in this paper ignores the large signal effects [12]. The control voltages V_{CTRLP} and V_{CTRLN} set the gate bias voltages VGP and VGN of the third stage inverter during the steady state. This in turn sets the quiescent current, I_Q and the transconductance, gm_3 of the third stage during the steady state.

The slewing current is given by (2)

$$I_{slew} = C_L \left(\frac{V_{out}}{T_{slew}} \right) \tag{2}$$

I_{slew} is set by sizing the transistors in the third stage inverter with rail to rail gate voltages.

For this example, the required GBW is $\geq$ 375MHz ($\approx 3F_S$) and a phase margin $\geq$ 60 degrees. The deadzone bias voltages are V_{CTRLP}= 795mV and V_{CTRLN} = 390mV to set a quiescent current of 3.5uA in the third stage inverter, at TT process corner. Table. I shows the drastic variation in the small signal parameters of the ring amplifier such as GBW and phase margin (PM) across TT, FF and SS corners, when the deadzone bias corresponds to that of the TT case.

Fig. 6 shows the transient response of the ring amplifier with a fixed deadzone bias, for a differential peak output swing of 800mV across FF, TT and SS process corners. The deadzone bias is fixed at the values corresponding to TT case. It can be seen that the settling accuracy requirements are not met for the SS case, due to the reduced GBW and slower response. Based on these observations, a robust deadzone biasing is required, that aims to maintain a constant quiescent current in the output stage across process variations.

Table I
VARIATION IN SMALL SIGNAL PARAMETERS OF THE RING AMPLIFIER WITH A FIXED DEADZONE BIAS.

Process Corners	SS	TT	FF
GBW (MHz)	9	415	1500
PM (degrees)	85	68	53

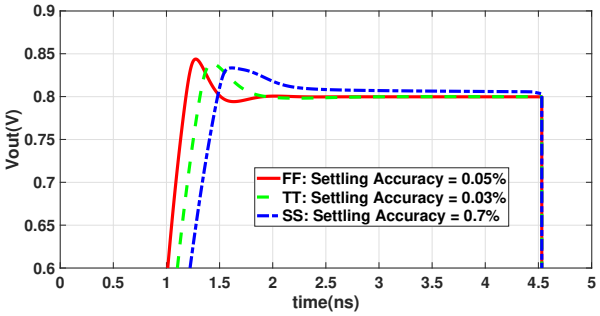

Figure 6. Transient response with fixed deadzone bias.

IV. Proposed Deadzone Regulation Circuit

A. Circuit Description

Fig. 7 shows the proposed regulation circuit. As seen from the figure, the diode tied transistors and the constant current source set the gate bias voltages VGP_{REF} and VGN_{REF} of the third stage inverter for a given bias current I_{BIAS}. The voltages VGP_{REF} and VGN_{REF} track the threshold voltage variation across process corners for a fixed bias current.

A negative feedback loop is formed using the replica of the second stage inverters and the error amplifiers. Each error amplifier senses the steady state output of the replica of the second stage and sets the control voltages V_{CTRLN} and V_{CTRLP}, such that, the steady state value of the second stage output approaches the reference bias voltages VGP_{REF} and VGN_{REF}, respectively. This negative feedback action regulates the quiescent current I_Q in the third stage inverter. By appropriately choosing the value of I_{BIAS} as a factor of the required I_Q, the control voltages V_{CTRLN} and V_{CTRLP} obtained from this circuit can be used in the ring amplifier shown in Fig. 4 for process invariant operation.

Although a constant current source is used in the design example, this current source can be potentially replaced with a constant transconductance based current source [1] to maintain the transconductance of the output stage constant over process, voltage and temperature (PVT) variations [1]. It should also be noted that the gain-bandwidth requirement of the error amplifier is relaxed as the deadzone regulation loop is a dc biasing network, independent of the signal path. The gain of the error amplifier used in this design is around 30dB.

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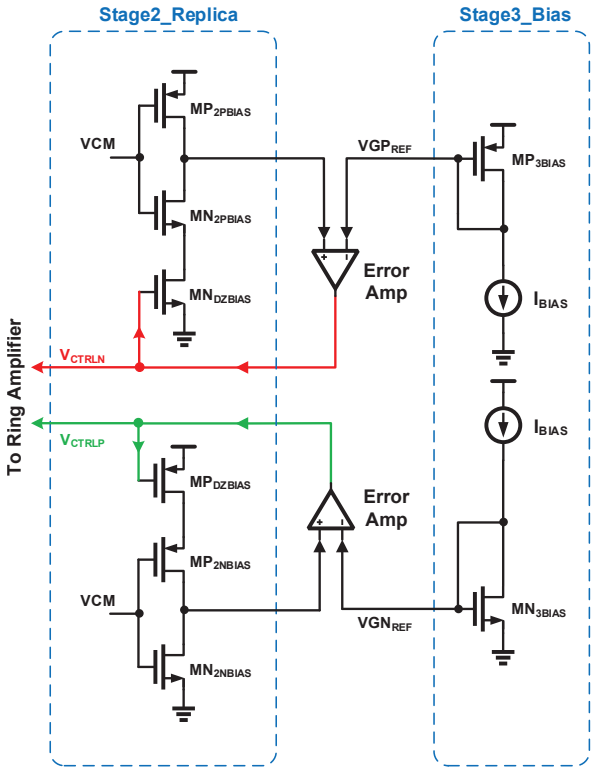

Figure 7. Deadzone regulation circuit for current starved inverter based ring amplifier.

B. Simulation Results

Table. II shows the consistency in the small signal parameters of the ring amplifier (GBW and PM) across TT, FF and SS corners, when the deadzone voltages are generated by the deadzone regulation circuit. The slightly higher value of GBW and reduced PM for SS case compared to FF case is due to the fact that, the dc gain from the first two stages are higher for the SS case compared to FF case. This is captured in the GBW equation shown in (1).

Fig. 8 shows the transient response of the ring amplifier with the deadzone regulation circuit, for a differential peak output swing of 800mV across FF, TT and SS process corners. The figure shows consistent results of $\leq$0.05% settling accuracy across TT, FF and SS corners.

Even though the proposed deadzone regulation technique is demonstrated for a current starved inverter based ring amplifier [5], the technique can also be adopted to other ring amplifier topologies [2]–[4], [6]–[11]. For example, in the traditional ring amplifier [2], shown in Fig. 1, the quiescent current, I_Q can be monitored in a similar fashion as in Fig. 7, while the feedback voltages control the deadzone voltage at the input of the second stage inverters. Similarly, in the resistor based ring amplifiers [3], [4], [6]–[11], shown in Fig. 3, the resistor in the second stage can be replaced with a voltage controlled resistor, which can be automatically tuned by the feedback action described in IV-A.

Thus by using the proposed deadzone regulation technique, the ring amplifiers can be made less sensitive to process variations, irrespective of the topology being used.

Table II
CONSISTENT SMALL SIGNAL PARAMETERS OF THE RING AMPLIFIER WITH DEADZONE REGULATION CIRCUIT.

Process Corners	SS	TT	FF
GBW (MHz)	475	415	380
PM (degrees)	61	68	72

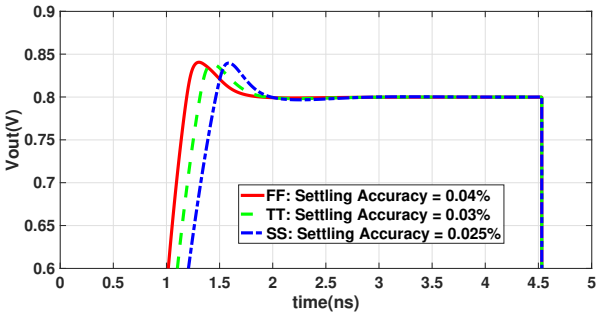

Figure 8. Transient response with the deadzone regulation circuit.

V. CONCLUSION

A deadzone regulation circuit is proposed to realize process invariant biasing of ring amplifiers. Traditional ring amplifier topologies are susceptible to process variations as the the deadzone biasing is a function of the threshold voltage of the transistors in the output stage inverter. This results in variation in the quiescent current I_Q at the output stage and variation in GBW across process corners. The proposed regulation circuit uses a replica of the ring amplifier and a negative feedback loop to track the threshold voltage variations, while maintaining a constant quiescent current I_Q at the output stage of the ring amplifier. The proposed technique is validated using transistor level simulations, showing improved ac and transient response of a ring amplifier across TT, FF and SS corners. The circuit is designed in 65nm CMOS process with a 1.2V supply to achieve a closed loop gain of 4 with a settling accuracy of $\leq$0.05% and operated at a sampling rate of 125MHz. Compared to a fixed deadzone voltage, the proposed technique shows consistent ac and transient response. The technique is demonstrated with a current starved inverter based ring amplifier. However, the technique can also be applied to other ring amplifier topologies as well.

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