SCSA1201	FUNDAMENTALS OF DIGITAL SYSTEMS	L	T	P	Credits	Total Marks
		3	0	0	3	100

COURSE OBJECTIVES

- To understand number systems and codes.
- To illustrate simplified Boolean expressions using Gates.
- To construct combinational logic circuits.
- To design sequential logic circuits.
- To analyze circuits and latches.

UNIT 1 NUMBER SYSTEMS,COMPLIMENTS AND CODES 9 Hrs.

Number Systems – Binary Numbers-Number base conversions-Octal and Hexa Decimal Numbers – Complements –Signed Binary Numbers-Binary Arithmetic –Binary Codes-Decimal Code-Error Detection code-Gray Code- Reflection and Self Complementary codes-BCD number representation – Alphanumeric codes ASCII/EBCDIC –Hamming Code- Generation, Error Correction.

UNIT 2 BOOLEAN ALGEBRA AND LOGIC GATES 9 Hrs.

Axiomatic definitions of Boolean Algebra – Basic Theorems and Properties of Boolean Algebra – Boolean Functions-Canonical and Standard forms-Digital Logic Gates– Simplification of Boolean Expressions: The map method- SOP and POS – NAND and NOR implementation-Don't Cares –The Tabulation Method-Determination and Selection of Prime Implicants.

UNIT 3 COMBINATIONAL LOGIC 9 Hrs.

Design Procedure-Adder – Subtracter – Code Conversion – Analysis Procedure –Multilevel NAND/NOR circuits-Exclusive OR functions – Binary adder and subtractor– Decimal adder – BCD adder – Magnitude Comparator – Decoders – Demultiplexer – Encoder – Multiplexers.

UNIT 4 SYNCHRONOUS SEQUENTIAL LOGIC 9 Hrs.

Flip Flops – Analysis of clocked sequential circuit –Reduction and Assignments–Flip flop excitation tables-Design Procedure-Design of counters-Registers-Shift registers-Synchronous Counters-Timing sequences-Algorithmic State Machines-ASM chart-timing considerations-control implementation.

UNIT 5 ASYNCHRONOUS SEQUENTIAL LOGIC AND MEMORY UNIT 9 Hrs.

Circuits with Lathes-Analysis procedure and Design Procedure-Reduction of state and Flow tables-Race –Free State Assignment.

Max. 45 Hrs.

COURSE OUTCOMES

On completion of the course, student will be able to

CO1 - Perform conversions between number systems.
CO2 - Simplify Boolean expressions and model using gates.
CO3 - Discover the principles behind combinational logic circuits used in real time.
CO4 - Survey the flip-flops needed for sequential logic circuits design.
CO5 - Analyze the sequential logic circuits.
CO6 - Discuss about memory unit and arithmetic logic unit.

TEXT / REFERENCE BOOKS

1. Morris Mano, "Digital Logic and Computer Design", Prentice Hall India, 2006.
2. Thomas L Floyd, "Digital Fundamentals", 10th Edition, Pearson Education, 2009.
3. A.P.Malvino and D.P.Leach, "Digital Principles and Applications", 6th Edition, McGraw-Hill, 2006.
4. Thomas C. Bartee, "Computer Architecture Logic Design", 3rd Edition, 2002.

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks : 100 **Exam Duration : 3 Hrs.**
PART A : 10 Questions of 2 marks each-No choice **20 Marks**
PART B : 2 Questions from each unit with internal choice, each carrying 16 marks **80 Marks**