Unit: 4 SEQUENTIAL CIRCUITS. (10hrs)

1. Flip flops:
   - SR, JK, D and T Flipflops. (2 hrs)
2. Master-Slave Flip Flops
   - Characteristics and excitation table. (1 hr)
3. Shift registers. (1 hr)
4. Counters. (1 hr)
   - Synchronous and Asynchronous Counters (1 hr)
   - Modulus Counters
   - up/down counters. (1hr)
5. State diagram, state table, state minimization, implication chart method. (3 hrs)

Introduction.

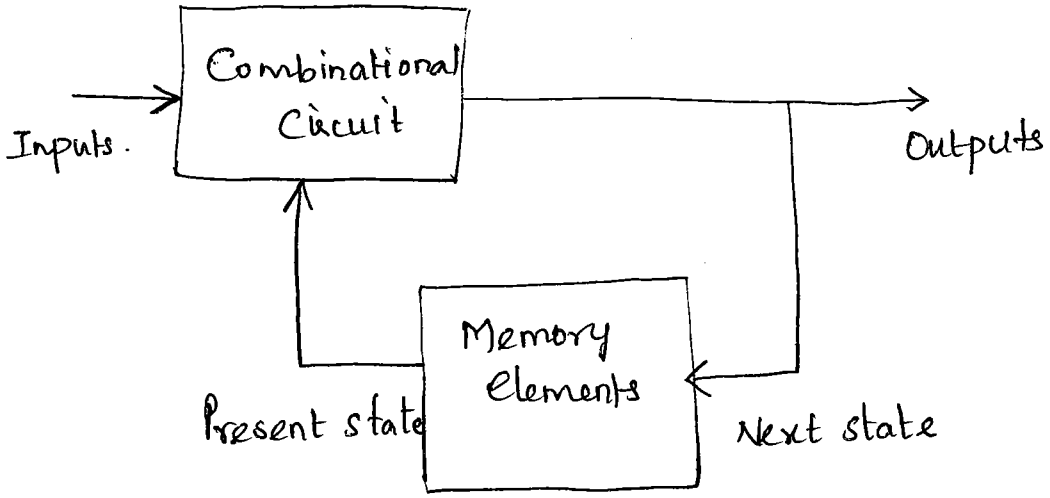
* There are many applications in which digital outputs are required to be generated in accordance with the sequence in which the input signal are received.

* This requirement cannot be satisfied using a Combinational logic system.

* These applications require outputs to be generated that are not only dependent on the present input conditions but they also depend upon the past history of these inputs.

* The past history is provided by feedback from the output back to the input.

* Memory elements are connected to the Combinational circuit as the feedback path.



Block diagram of sequential circuit.

Comparison between combinational and sequential circuit.

Combinational circuit	sequential circuit.
1. Memory unit is not required	Memory unit is required to store the past history of the input.
2. The o/p of any instant of time are dependent only on the present input	The output of any instant of time dependent not only on the present input but also on the past.
3. They are faster because the delay between the input and o/p is due to propagation delay of gates only	It is slower than the combinational circuits.
4. It is easy to design	It is harder to design.

classification of sequential circuit.

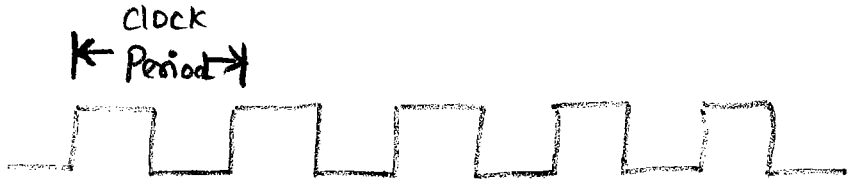
1. Synchronous sequential circuit
2. Asynchronous sequential circuit

synchronous sequential	Asynchronous sequential.
1. Memory elements are clocked ff's.	Memory elements are either unclocked FF's or time delay elements

The change in input signals can affect memory elements upon activation of clock signal	The change in input signal can affect memory elements at any instant of time.
The max operating speed of the clock depends on time delays involved.	Because of the absence of the clock, asynchronous circuits can operate faster than synchronous circuit.
Easier to design	more difficult to design.

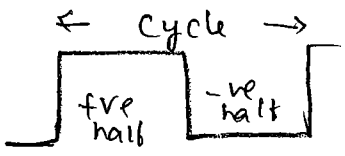
Clock:

A clock signal is a particular type of signal that oscillates between a high and a low state and is utilized to co-ordinate actions of circuits.



Clock signal

* Most of the clock signal is in the form of a square wave with 50 % duty cycle.
* Signal generated by clock generator.
* Circuits using the clock signal for synchronization may become active at either the rising edge, falling edge. or in case of double data rate, both in the raising and falling edges of the clock pulse.
* The time required to complete one cycle is called "clock period" or "clock cycle".

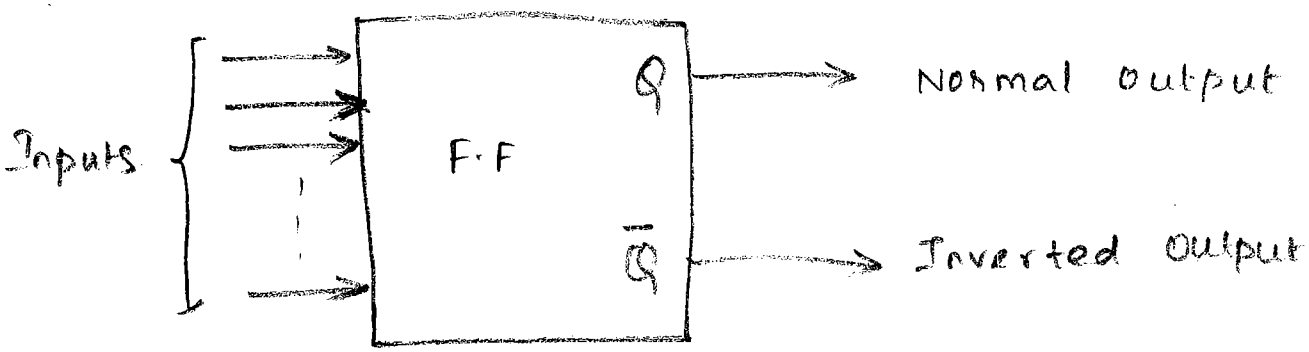


Latches and flip flops:

The most important memory element is the flip-flop, which is made up of an assembly of logic gates.

Even though the logic gate by itself has no storage capability, several logic gates can be connected together to permit information to be stored.

Flip flop: * known formally as a bistable multivibrator, has two stable state. It can remain in either of the states indefinitely. Its state can be changed by applying the proper triggering signal. It is also called as "binary or one bit memory".



General flip flop symbol.

* Flip flop has 2 outputs (Q and $\bar{Q}$)
  Q - Normal output $\bar{Q}$ - inverted output.
* The state of the flip flop always refers to the state of the Normal output Q.
  The inverted output is the opposite state.

A flip flop is said to be in High state or logic 1 state or Set state when $Q = 1$

Low state or logic 0 or Reset state or Clear state when $Q = 0$.

Here the flip flop has got more than one inputs.

"The Input signals which Command the flip flop to change state are called excitations".

These inputs are used to cause the flip flop to switch back and forth between its possible output states.

A Flip-flop input has to be pulsed momentarily to cause a change in the flip flop output, and the output will remain in the new state even after the input pulse has been removed. This is the flip flop's memory characteristics.

Application: Flip flop serves as a storage device. It stores 1 when its output is 1

It stores 0 when its output is 0

Shift registers, Counters.

Latch:

It refers to non-clocked Flip-Flops, because these flip flops 'latch on' to a 1 or 0 immediately upon receiving the input pulse called Set or Reset.

They are not dependent on the clock signal

for their operation. Latch is a sequential device that checks all its inputs continuously and changes its output accordingly at any time independent of a Clock signal.

In the absence of ENABLE or gating signal, the latch does not respond to the changes in its inputs.

On the other hand, a flip flop is a sequential device that normally samples its input and changes its output only at times determined by clock pulse.

Latch can be built up using two NAND gate or two NOR gate

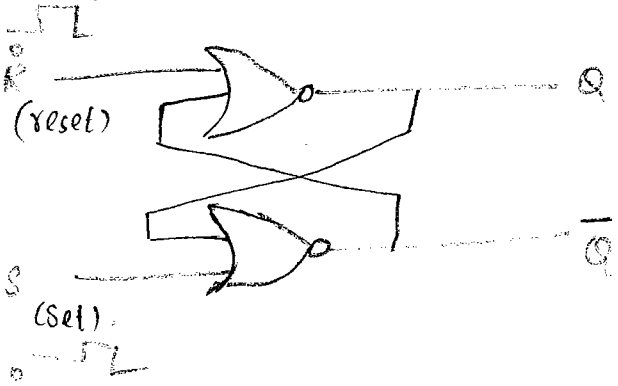
RS latch:

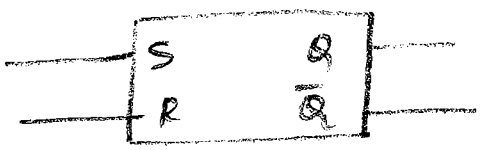
Two inputs S and R. S is called Set R is called Reset

S input is used to produce a 1 in Q, it stores a binary 1 in FF.

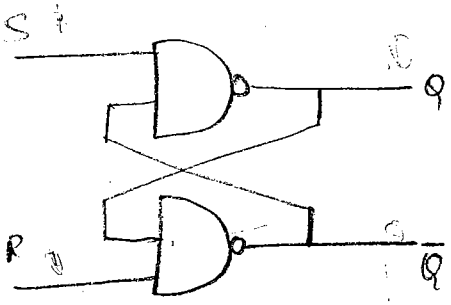
R input is used to produce a 0 in Q, it stores a binary 0 in FF.

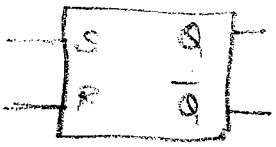
This type of FF is sometimes called direct Coupled RS FF.





S	R	Q	$\bar{Q}$
0	0	Previous State	
1	0	1	0
0	1	0	1
1	1	invalid	





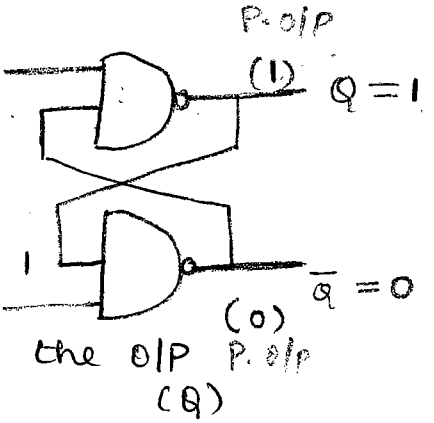
S	R	Q	$\bar{Q}$
1	1	Previous state	
0	1	1	0
1	0	0	1
0	0	invalid.	

The circuit is such that the cross coupled connection from the output of one gate to the input of the other gate constitutes a feedback path. Hence the circuit is called "asynchronous sequential circuits".

Operation of NAND latch.

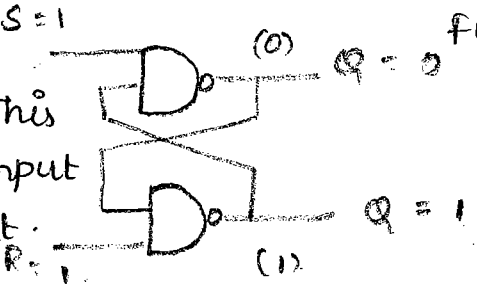
(1) when $S=1$ $R=1$

A one in Q and 1 in R produces 0 in $\bar{Q}$ This together with a 1 in S input produces a 1 in the O/P



for Q = 1

A zero in Q along with 1 in R produces a 1 in $\bar{Q}$. This together with a 1 in the S Input Produces a 0 in Q output.

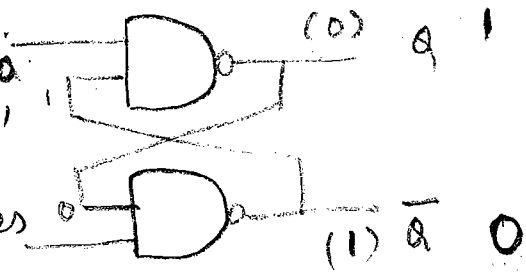


for Q = 0

* so both high inputs have no effects on the output. The previous state output are shown in paranthesis.

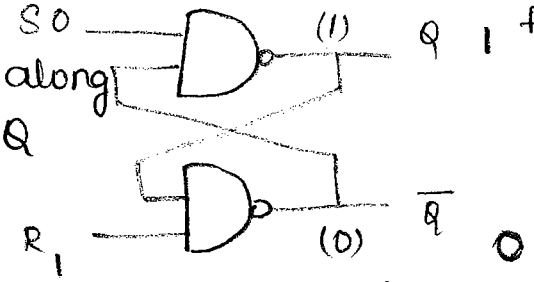
(2) when $S=0$; $R=1$

A zero in Q with $R=1$ Produces 0 in $\bar{Q}$, This with a 0 in S produces 1 in Q O/P Hence $\bar{Q}=0$.



for Q = 0

A one in Q with R = 1 so produces a 0 in $\bar{Q}$. This along with S = 0 produces 1 in Q

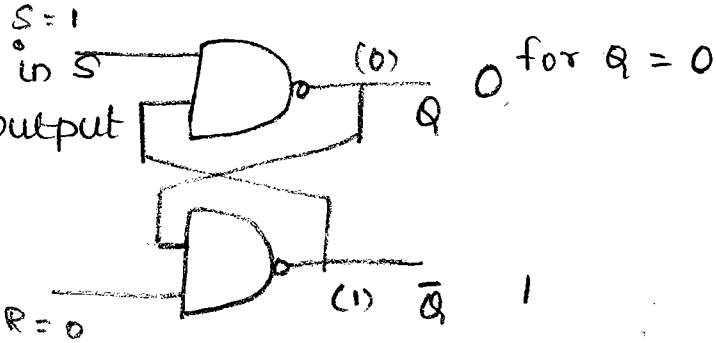


$\therefore$ Q = 1 $\bar{Q}$ = 0

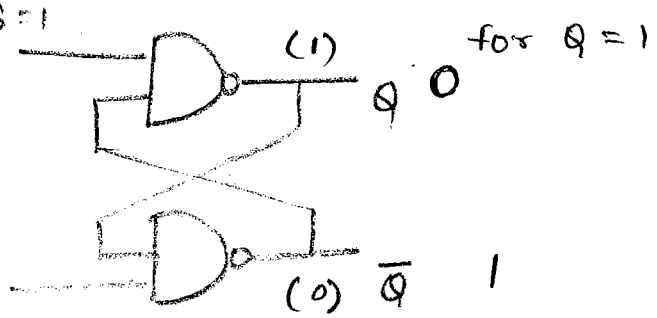
So when S = 0 ; R = 1 , Flip flop is set whatever the previous O/P's are. (Q = 1)

3. when S = 1 ; R = 0

The one in $\bar{Q}$ with 1 in S produces a 0 as Q output hence $\bar{Q}$ = 1



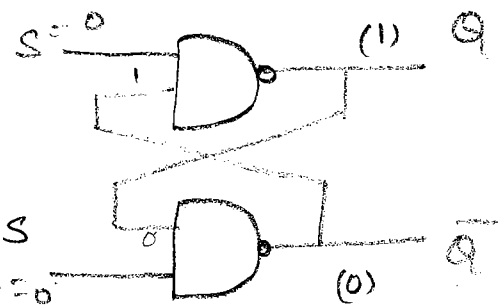
The zero in $\bar{Q}$ with R = 0 1 in S produces 0 as Q output hence $\bar{Q}$ = 1



So when S = 1 and R = 0, irrespective of the previous outputs, the ff is Reset (Q = 0).

4. when S = 0 ; R = 0

The one in Q along with 0 in R produces 1 in $\bar{Q}$ which in turn with 0 in S Produces 1 in Q



Since both outputs are high this indicates an invalid Output Q = $\bar{Q}$ which is not true. Hence S=0 and R=0 condition produces such an ambiguous output, this condition is termed as invalid or NAND latch.

operation of NOR latch:

1. NAND latch Output is invalid for S=R=0
   NOR latch Output is invalid for S=R=1

2. TO set a NAND latch S=0
   TO set a NOR latch S=1

3. TO reset NAND latch R=0
   TO reset NOR latch R=1

4. The NAND latch has no change in output when both the inputs are 1
   The NOR latch has no change in output when both the inputs are 0.

Latches Vs Flipflops:

A simple latch forms the basis for the flip flops. Latches are controlled by enable signal, and they are level triggered, either positive level triggered or negative level triggered. The output is free to change according to the S and R input values, when active level is maintained at the enable inputs.

Flip flops are different from latches Flip flops are pulse or clock edge triggered instead of level triggered.

Level and Edge Triggering.

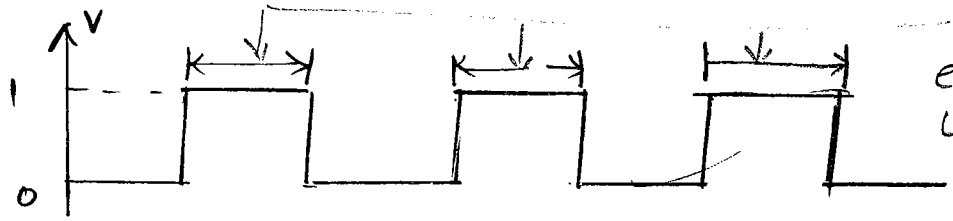
Level Triggering:

In the level triggering, the output state is allowed to change according to input(s) when active level is maintained at the enable input.

There are two types of level triggered latches.

- Positive level triggered:

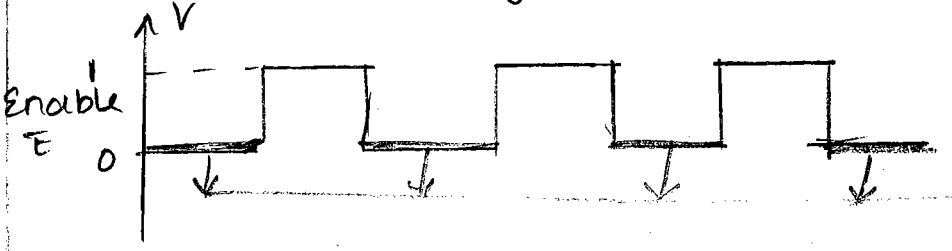
The output of flip flop responds to the input changes only when its enable input is 1(high)



Flip Flop is enabled only when the level of E input is high.

Negative level triggered:

The output of the flip flop responds to the input changes only when its enable input is 0(low)



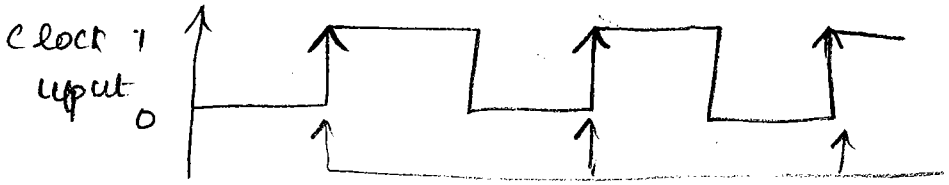
Flip Flop is enabled only when the level of E input is low.

Edge Triggering:

In the edge triggering, the output responds to the changes in the input only at the positive or negative edge of the clock input. There are two types of edge triggering.

Positive edge triggering:

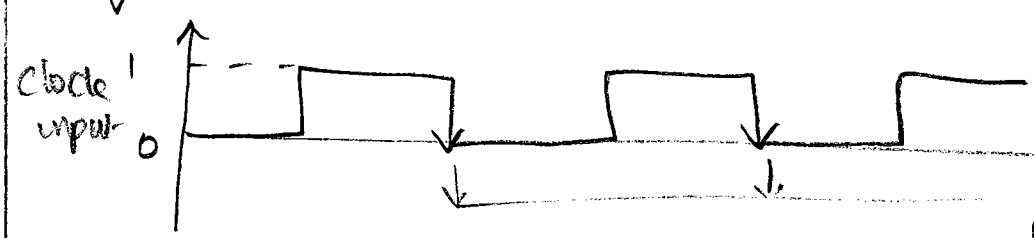
Here, the output responds to the changes in the input only at the positive edge of the clock pulse at the clock input.



output responds only at the positive edges of the pulse

Negative edge triggering:

Here the output responds to the changes in the input only at the negative edge of the clock pulse at the clock input.



output responds only at the negative edges of the pulse

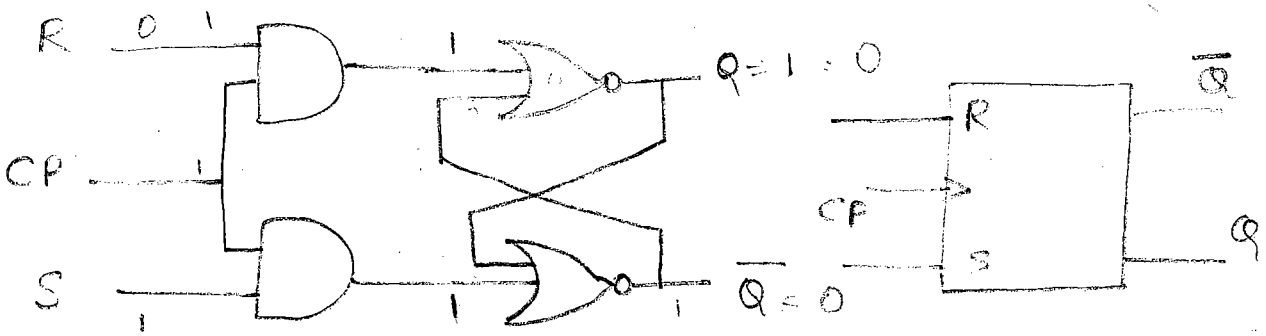
RS Flip Flop.

* It consist of 2 additional AND gates at the input of RS latch

* When clock pulse is low, the output of AND gates are low & changes in S and R inputs will not affect the output.

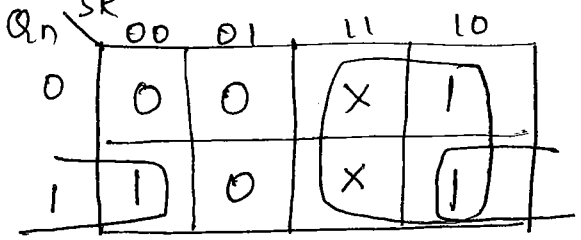
C·P = 0 ; O/P of AND gate = 0 ; input S & R = 0 0 , 0 1 , 1 0 , 1 1 O/P has NO change.

* When clock pulse is high, the values of S and R will be passed to the output of AND gates.



Clock	S	R	Q_n	Q_{n+1}	State.
1	0	0	0	0	No change
1	0	0	1	1	No change
1	0	1	0	0	Reset
1	0	1	1	0	Reset.
1	1	0	0	1	Set
1	1	0	1	1	Set
1	1	1	0	1	indeterminate
1	1	1	1	0	indeterminate

Expression:

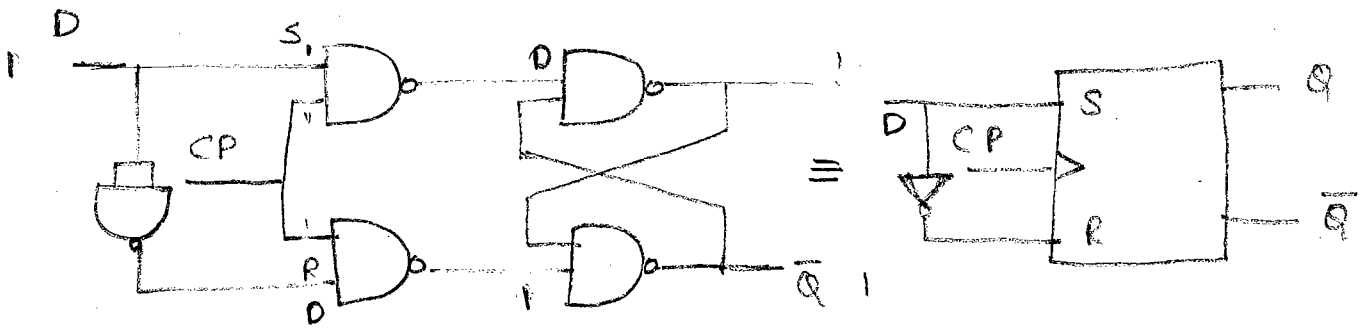


$$Q_{n+1} = S + \bar{R} Q_n$$

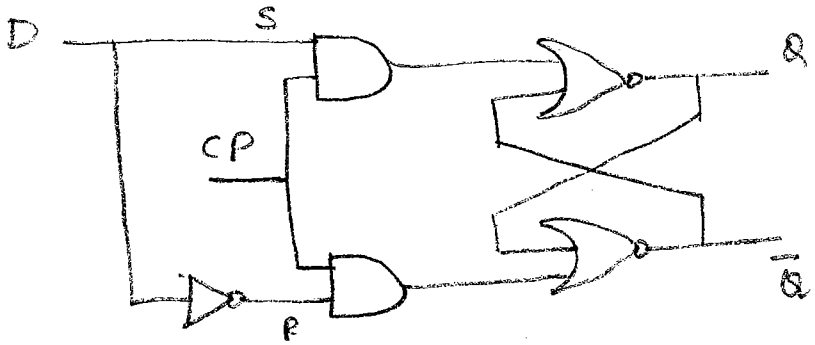
D- Flip Flop: (Delay)

D (Delay) FF has only one input called D- i/p and two outputs Q and $\bar{Q}$.

Insert inverter between S and R and give D i/p directly to S and $\bar{D}$ input to R.



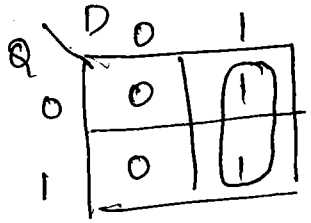
(or)



Characteristic table:

CP	D	Q_n	Q_{n+1}
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Expression for Q_{n+1}



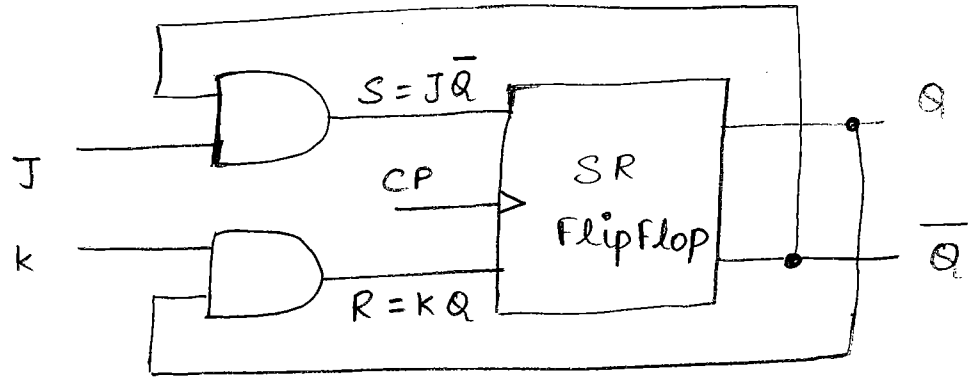
$$Q_{n+1} = D.$$

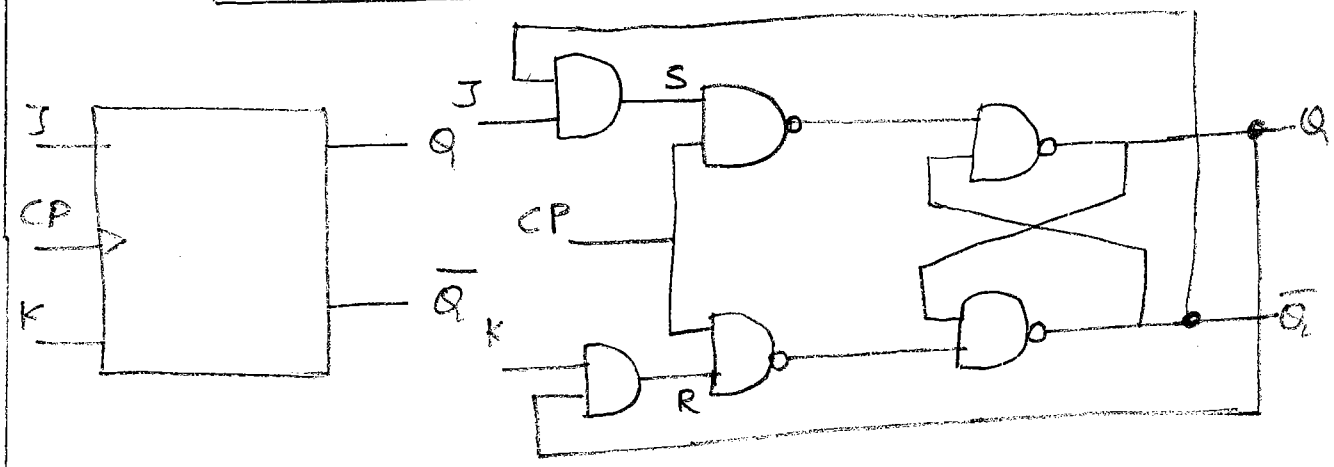
* CP = 1 ; D = Q_{n+1}

JK flip flop:

The uncertainity in the state of an SR FlipFlop when S = R = 1 can be eliminated by Converting it into a JK Flip Flop.

The data inputs are J and K which are ANDed with $\bar{Q}$ and Q respectively, to obtain S and R inputs, as shown. Thus $S = J\bar{Q}$; $R = KQ$.





Case 1.

J = K = 0

when J = K = 0, S = R = 0 and according to truth table there is no change in the Output.

Case 2:

J = 0 ; K = 1

for $Q_n = 0$, Q = 0 ; $\bar{Q} = 1$; S = 0 ; R = 0 ;

Since SR = 00 there is no change in the Output and therefore Q = 0 $\bar{Q} = 1$

if Q = 1 ; $\bar{Q} = 0$; S = 0 ; R = 1 According to truth table of SR flip flop it is a reset state and the Output Q will be 0.

Case 3

$J = 1 \quad K = 0$

for $Q = 0, \bar{Q} = 1$

Now $S = 1$; $R = 0$. According to truth table SR Flip flop is set state and the output $Q = 1$

for $Q = 1 \quad \bar{Q} = 0$

Now $S = 0$; $R = 0$ Since $SR = 00$, there is no change in the o/p therefore $Q = 1$ and $\bar{Q} = 0$.

for $J = 1$ & $K = 0$ $Q = 1$ i.e, Set State.

Case 4:

$J = 1 \quad K = 1$

For $Q = 0$; $\bar{Q} = 1$

$S = 1$; $R = 0$ According to truth table of SR flip flop it is a set state and Output Q will be 1

for $Q = 1 \quad \bar{Q} = 0$

$S = 0 \quad R = 1$, According to truth table SR FF is reset state i.e, $Q = 0$.

if $J = 1$; $K = 1$ toggles the F'F o/p.

Race around Condition:

When $J = K = 1$ and clock is applied, the o/ps go on Complementing as long as clock is present.

At the end of the clock pulse the flip flop is disabled and the value of Q is uncertain.

This is called Race around condition.

o/p changes from either 0 to 1 or 1 to 0

J	K	Q_n	Q_{n+1}	State
0	0	0	0	NO change
0	0	1	1	NO change
0	1	0	0	Reset
0	1	1	0	Reset
1	0	0	1	Set
1	0	1	1	Set
1	1	0	1	Toggles
1	1	1	0	Toggles

J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

Truth table

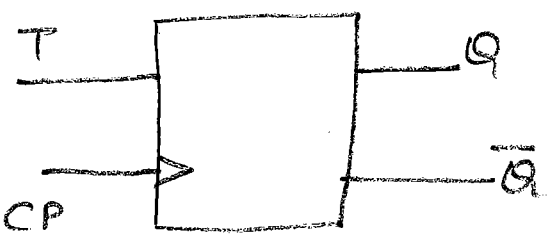
Expression for J K FF.

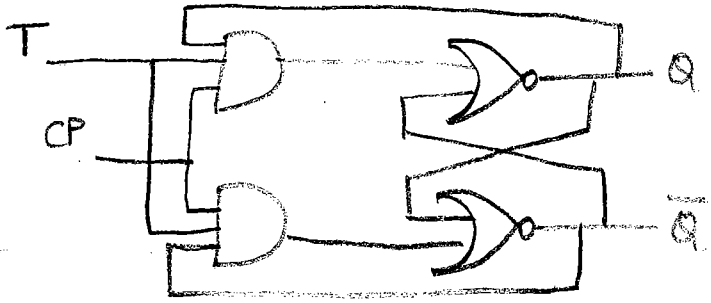
Q_n \ Jk	00	01	11	10
0	0	0	01	01
1	1	0	0	1

$$Q_{n+1} = \overline{Q}_n J + \overline{K} Q_n$$

T Flip Flop.

* T (or) Trigger (or) Toggle FF.
* It has one input and two outputs Q and $\overline{Q}$
* T FF is obtained by connecting its J and K inputs together
* It has the ability to toggle or Complement its state





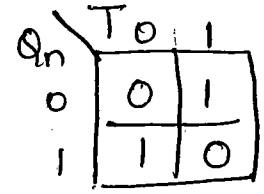
Characteristics Table

T	Q_n	Q_{n+1}
0	0	0
1	0	1
0	1	1
1	1	0

$T = 0 \; ; \; Q_{n+1} = Q_n$

$T = 1 \; ; \; Q_{n+1} = \bar{Q}_n$

Expression for Q_{n+1}



$Q_{n+1} = T\bar{Q}_n + \bar{T}Q_n$

Note: The time delay of FF and propagation delay of clock pulse are same so to overcome this width of clock pulse is shorter, even then accuracy is not proper so move on to master slave or edge triggered.

Master-Slave Flip Flops:

The problem of race around conditions can be solved by master-slave FF.

This improvement is acheived by introducing a known time delay between the time that the Flip Flop responds to a clock pulse and the time the response appears at its output.

The master-slave FlipFlop is also called pulse-triggered Flip-flip because the length of the time required for its output to change the state equals the width of one clock pulse.

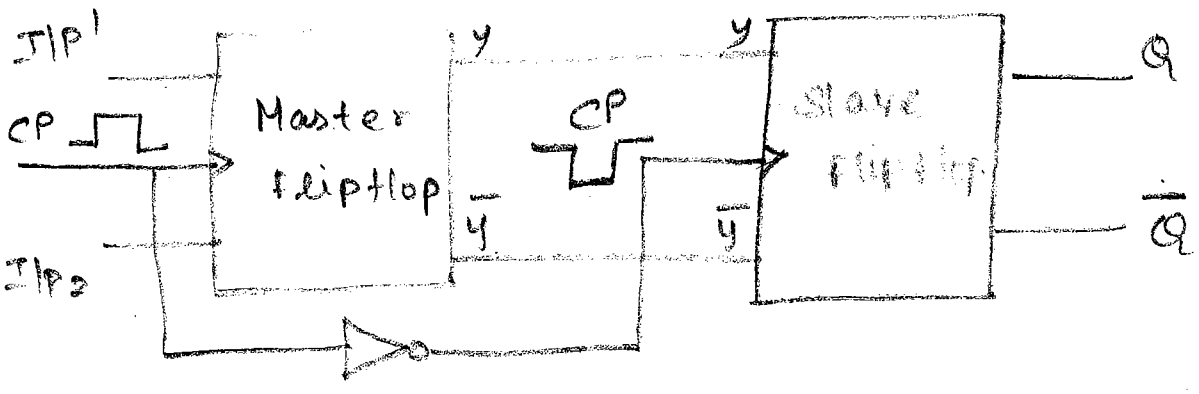
* The master-slave flipflop or pulse triggered Flip-Flop actually Contains two Flip Flops.

1) master Flip Flop.
2) slave Flip Flop.

* Control inputs are applied to the master FlipFlop and maintained constant for a time prior to the application of the Clock pulse.

Master FlipFlop → output is determined on the rising edge of the clock pulse, levels on the control inputs.

On the falling edge of the clock pulse, state of the master is transferred to the slave, whose outputs are Q and $\bar{Q}$

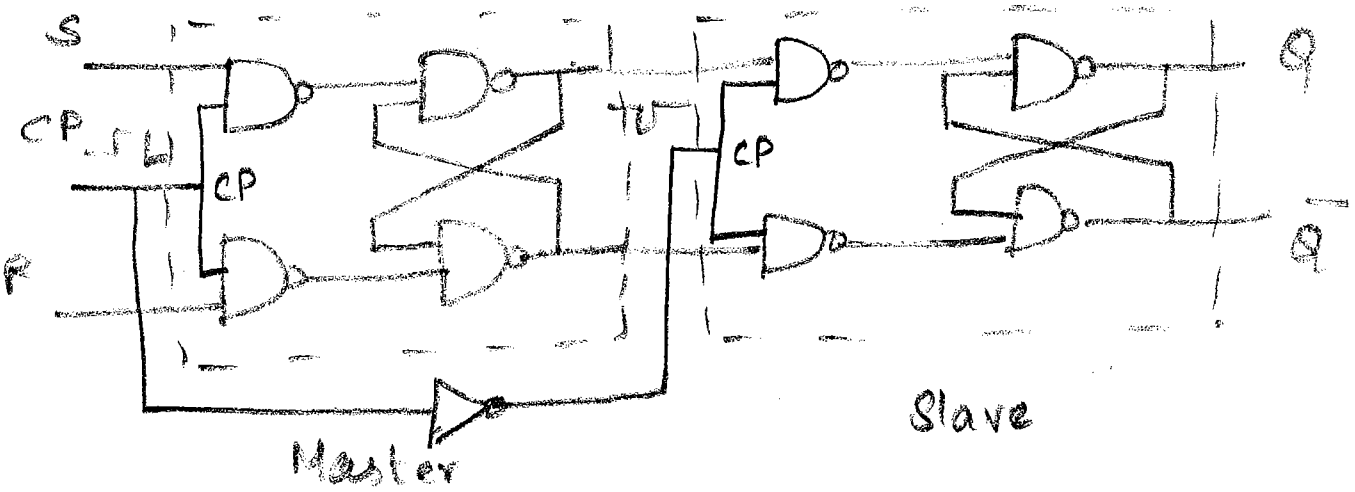


The Master-slave (Pulse triggered) S-R Flip Flop.

The truth table operation is same as that of the S-R Flip flop.

Externally Ips are S and R given to master section and this SR will work for the positive edge of the clock signal. the output of master given as it is to the slave. this slave works for the same in negative going pulse.

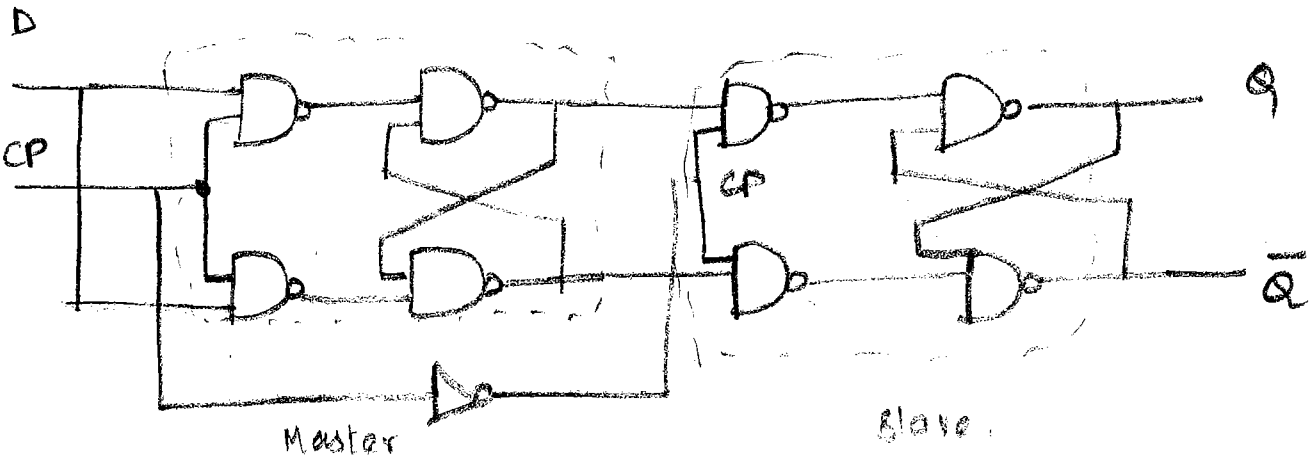
i.e, The slave copies the state of the master at the negative going edge of the clock Pulse. The state of the slave then immediately appears on its Q and $\overline{Q}$ outputs.



S	R	Q	Q_n	state
0	0	Q_0		No change
0	1	0		Reset
1	0	1		Set
1	1	?		invalid.

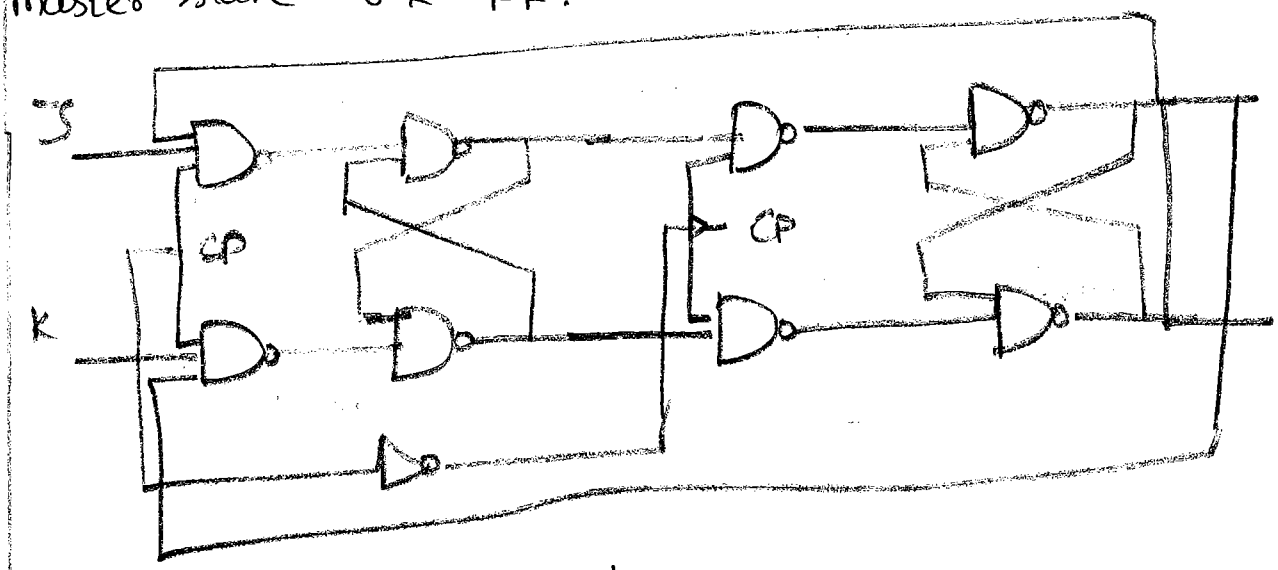
Truth table of master slave Flip Flop.

Master- slave D f.f.



D	Q	State.
0	0	Reset
1	1	Set

master slave J K FF.



J	K	Q	state.
0	0	Q_0	No change
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}_0$	Toggle.

Operation of Master Slave Flip Flop.

The external Control inputs S & R are applied to the master section.

master FlipFlop: Gated SR latch → O|p is obtained during the +ve going edge of the clock.

Slave FlipFlop: Gated SR latch → O|p is obtained during the -ve going edge of the clock.

* Ouput of master FF is y & $\bar{y}$.
* y and $\bar{y}$ as input to slave and output is Q and $\bar{Q}$
* During positive going edge ⇒ master is activated.
* During Negative going edge ⇒ Slave is activated.

When CP = 0

Master = disabled

Slave = enabled., Now $Q = y$ and $\bar{Q} = \bar{y}$

When CP = 1

Master = enabled., operates as SR FF.

Slave = disabled.

* When pulse returns to 0, master is isolated and slave goes to the same state as master.

* If S=1; R=0; State with Q=1; pulse from 0 to 1 master → set so $y = 1$

* Since master in internal circuit the changes are not noticable but S, R state can be changed accordingly Q and $\bar{Q}$ output is got.

* Thus in master slave FF, it is possible to switch the output of the FF and its input information with the same C·P.

Flip Flop excitation Table.

* Excitation table is needed, to design a sequential cucuit.

* It is obtained from the characteristic table.

for SR Flip flop.

Characteristic table.

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	X

Excitation table.

Q_n	Q_{n+1}	S	R
0	0	0	0/1
0	1	1	0
1	0	0	1
1	1	0/1	0

for JK flip Flop.

J	k	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

Excitation table

Q_n	Q_{n+1}	J	k
0	0	0	0/1
0	1	1	0/1
1	0	0/1	1
1	1	0/1	0.

for D flip Flop.

D	Q_{n+1}
0	0
1	1

Excitation table.

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

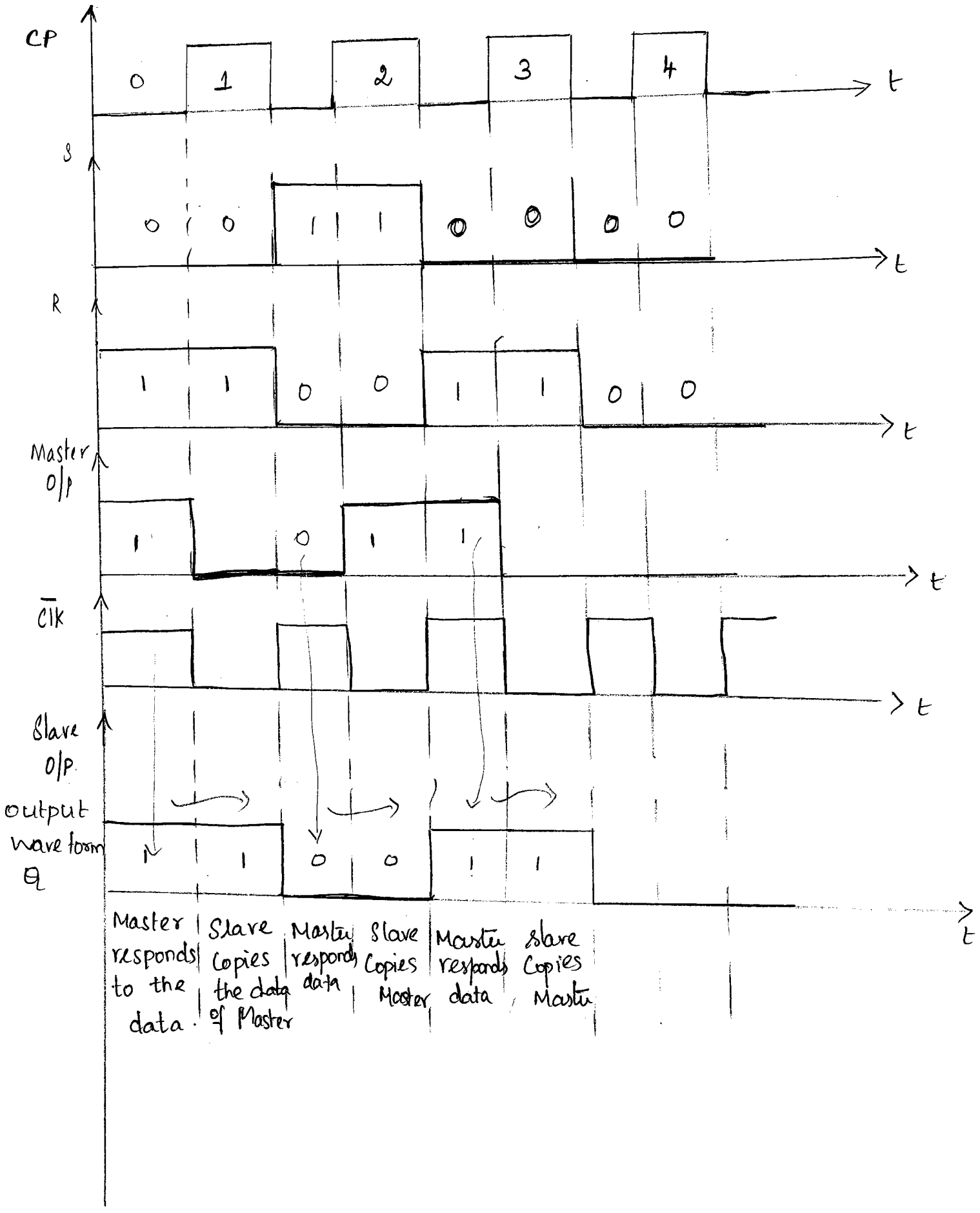
for T flip Flop.

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

Excitation table.

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

waveform for Master Slave Flip Flop.



Shift Registers:

* The FlipFlop is the temperory storage element stores a single bit.
* Register is a combination of FlipFlop, work is to store the digital data of any kind.
* Shifting is also possible on the application of the CP.

Register — data storage
Register — data movement.

The storage capacity of register is the total number of 1's and 0's in the data.

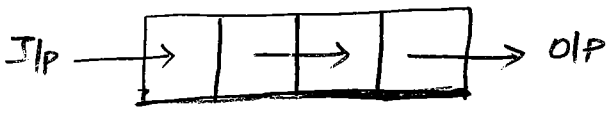
Shift Register:

The movement of data from stage to stage within the register or into or out of the register upon application of Clock pulse.

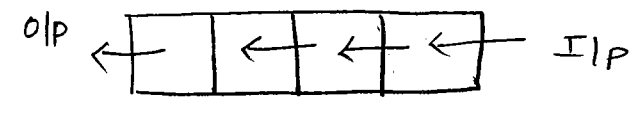
The types of data movement in shift register are.

1. Serial in Serial Out (SISO)
2. Serial in parallel out (SIPO)
3. parallel in parallel out (PIPO)
4. Parallel in Serial Out (PISO)
5. Bidirectional.
6. Rotational Right.
7. Rotational left.

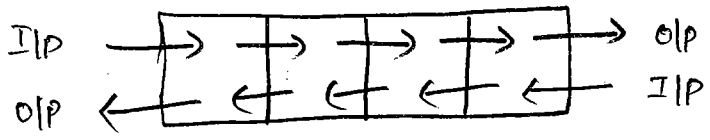
SISO:



Right shift register

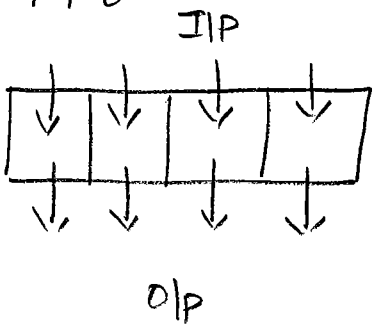


Left shift register.

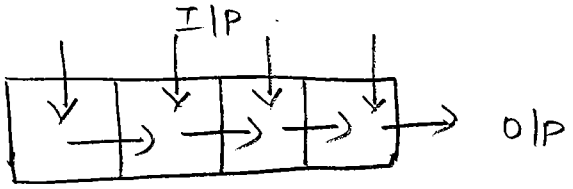


Bidirectional.

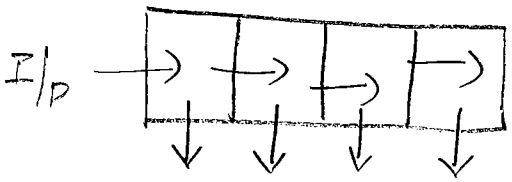
PI PO



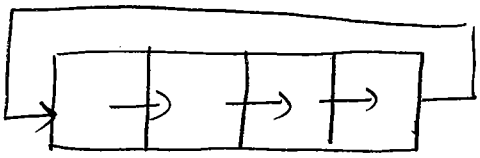
PI SO



SIPO



Rotate Right.



Rotate left.

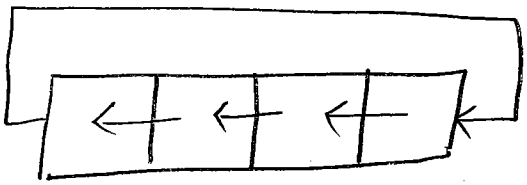
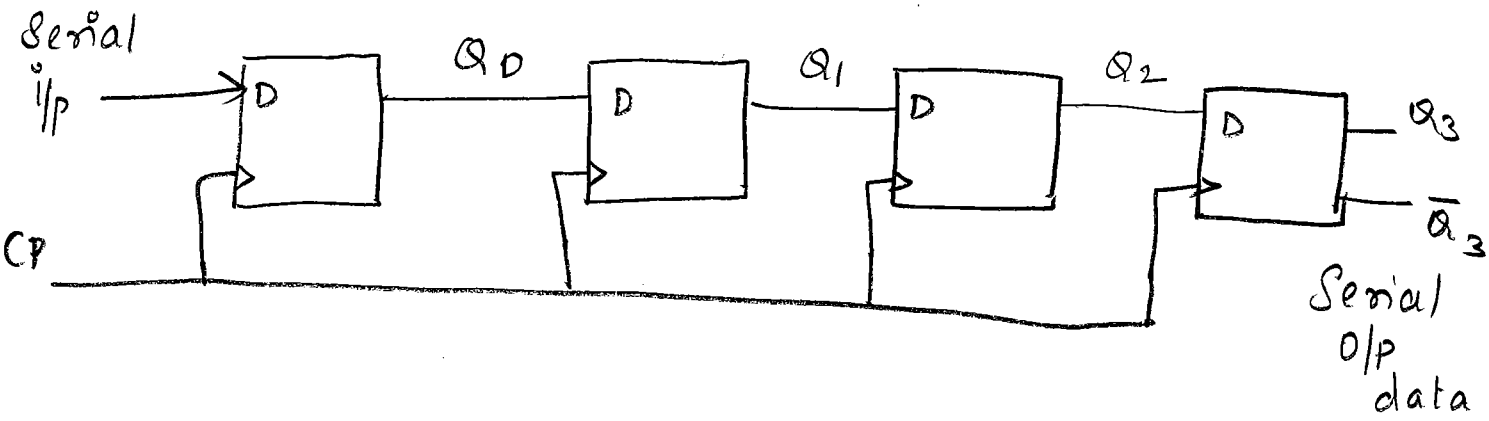
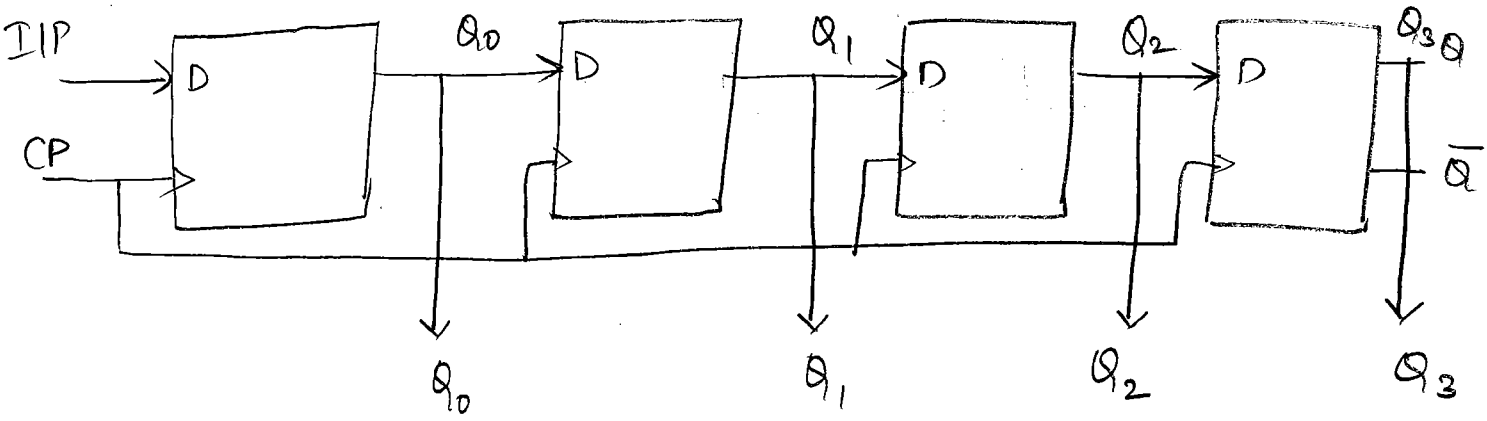


Illustration:

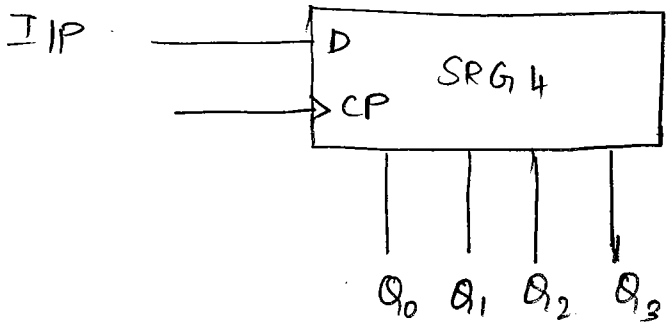
SISO Shift register:



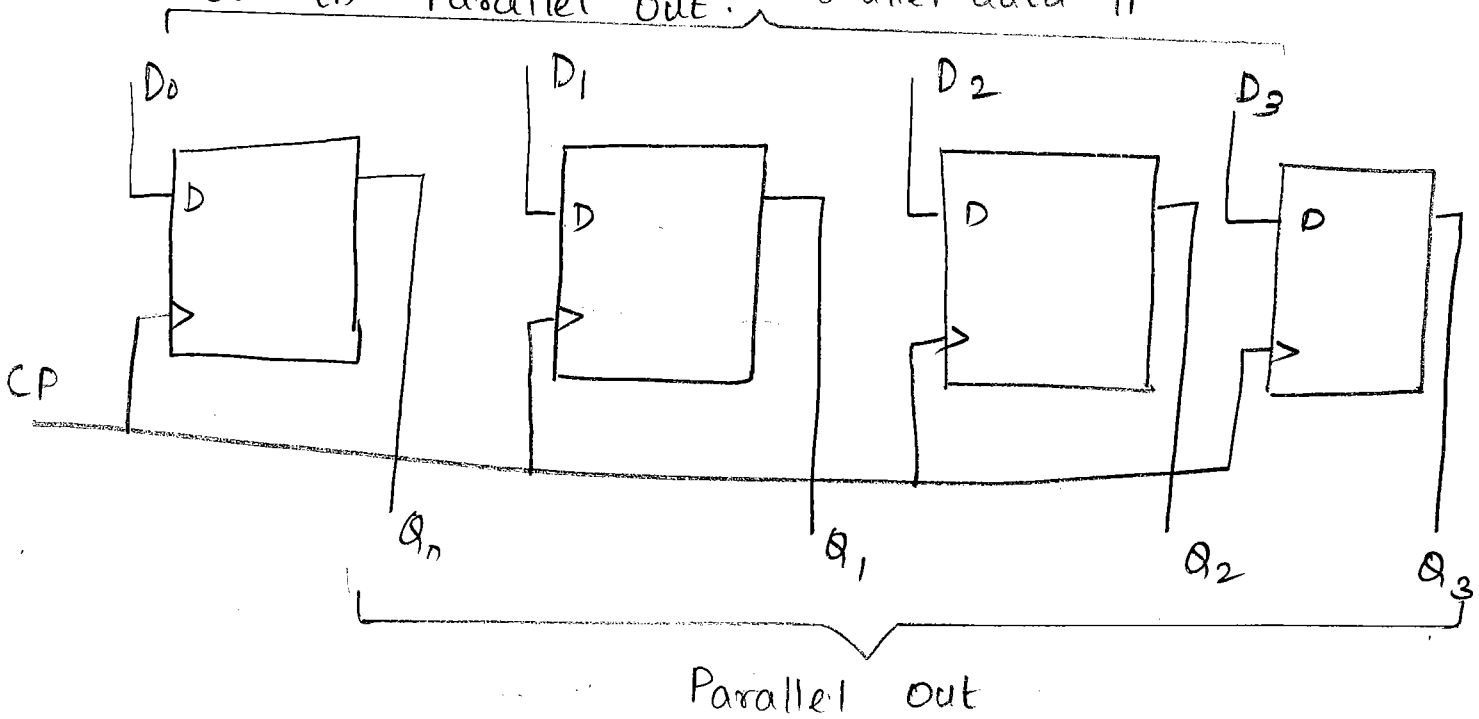
Serial in Parallel out shift register:



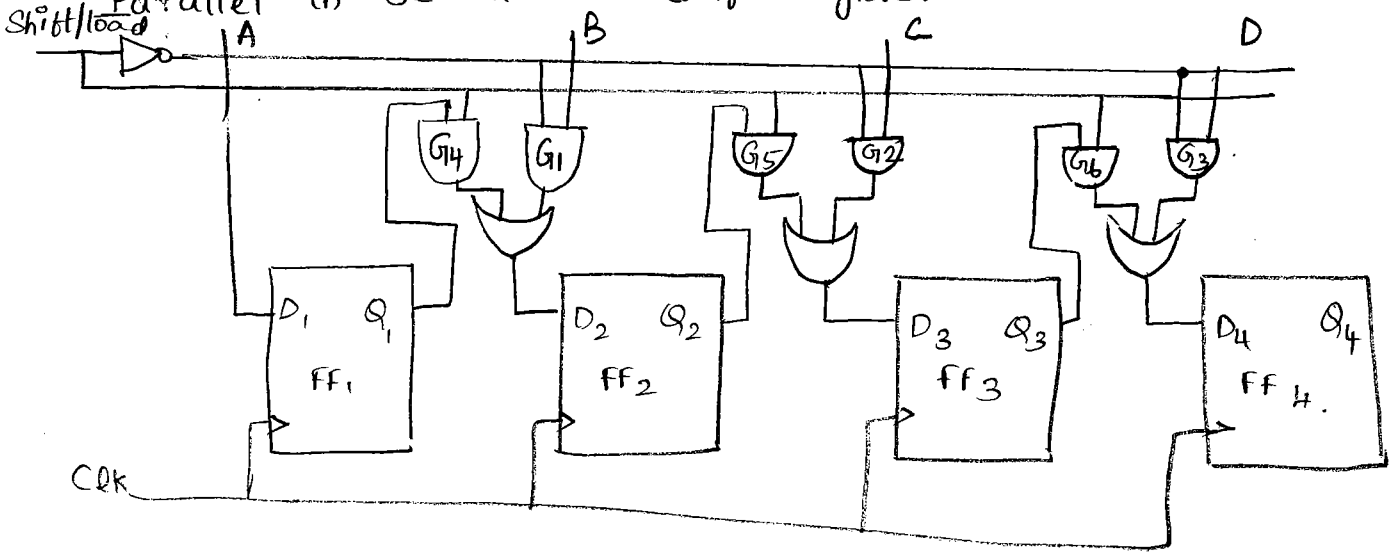
(or)



Parallel in Parallel out. Parallel data i/p



Parallel in Serial Out Shift Register.



* The data ABCD through which the data is entered into register in parallel form.

* The signal shift/$\overline{\text{load}}$ allows.

a) data to be entered in parallel form into the register

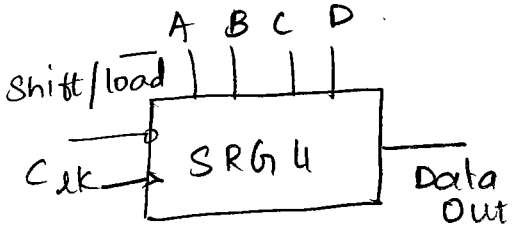
b) data to be shifted out serially from Q_4.

* when shift/$\overline{\text{load}}$ is high

$G_1, G_2, G_3 \rightarrow$ disabled.

$G_4, G_5, G_6 \rightarrow$ enabled

The data from first stage to the next is shifted.



* when shift/$\overline{\text{load}}$ is low

$G_1, G_2, G_3 \rightarrow$ enabled

$G_4, G_5, G_6 \rightarrow$ disabled

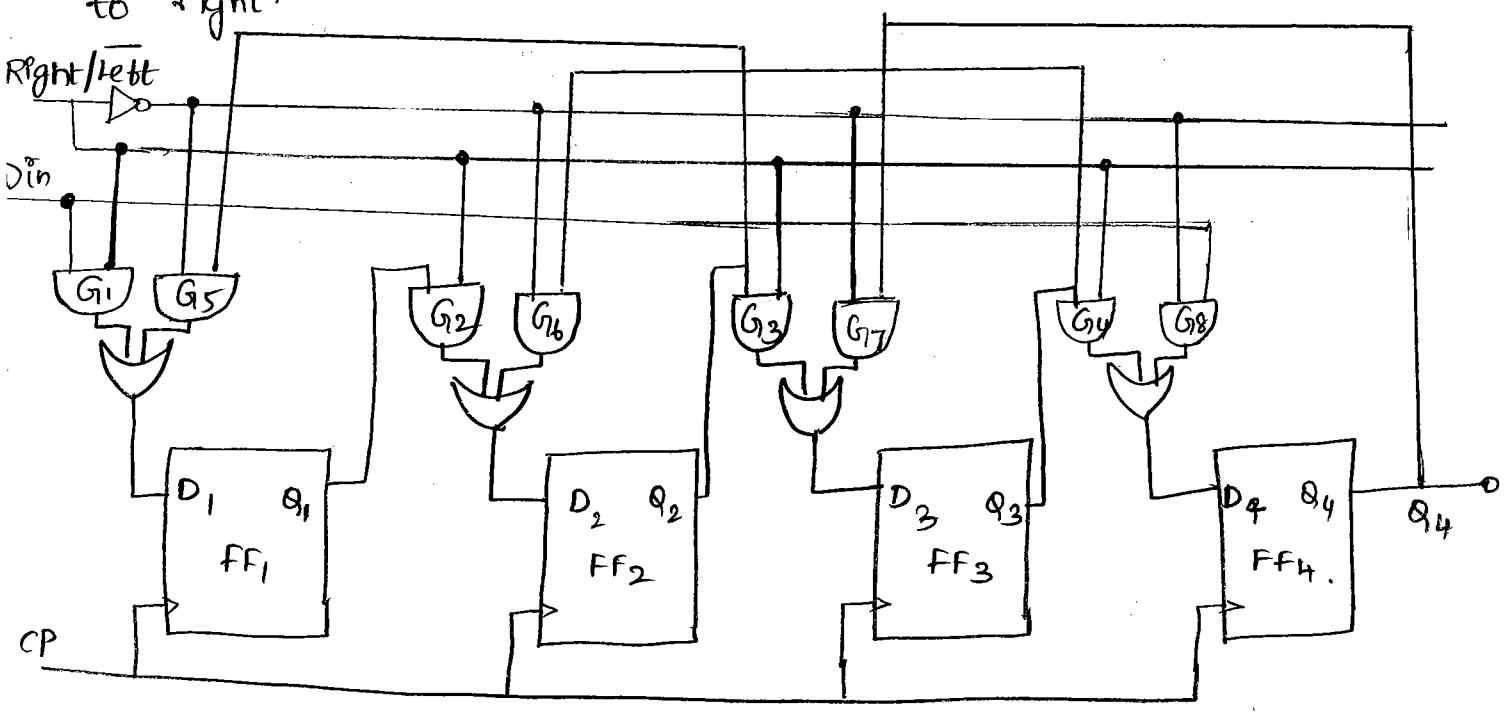
The data input appear at the each FF.

* when Clock pulse is applied, these data bits are shifted to the Q output terminals.

* OR gate allows either the normal shifting Operation or the parallel data entry depending on which AND gates are enabled according to shift/$\overline{\text{load}}$.

Bidirectional shift register:

Data shifted either from right to left or left to right.



If Right/$\overline{Left}$ = high ⇒ shift right shift register.

If Right/$\overline{Left}$ = Low ⇒ shift left shift register.

Operation:

(1) $R/\overline{I} = 1$: G_1, G_2, G_3, G_4 enable.

G_5, G_6, G_7, G_8 disable.

Data D_{in} entered into FF_1 then with CP to Q_1 then to D_2 then the Q_2 then to next stage of Q_4.

(2) $R/\overline{I} = 0$: G_5, G_6, G_7, G_8 enable

G_1, G_2, G_3, G_4 disable.

The data from FF_4 to FF_1 is shifted

Thus the data is shifted right and left for $R/\overline{I} = 1$ and 0 respectively.

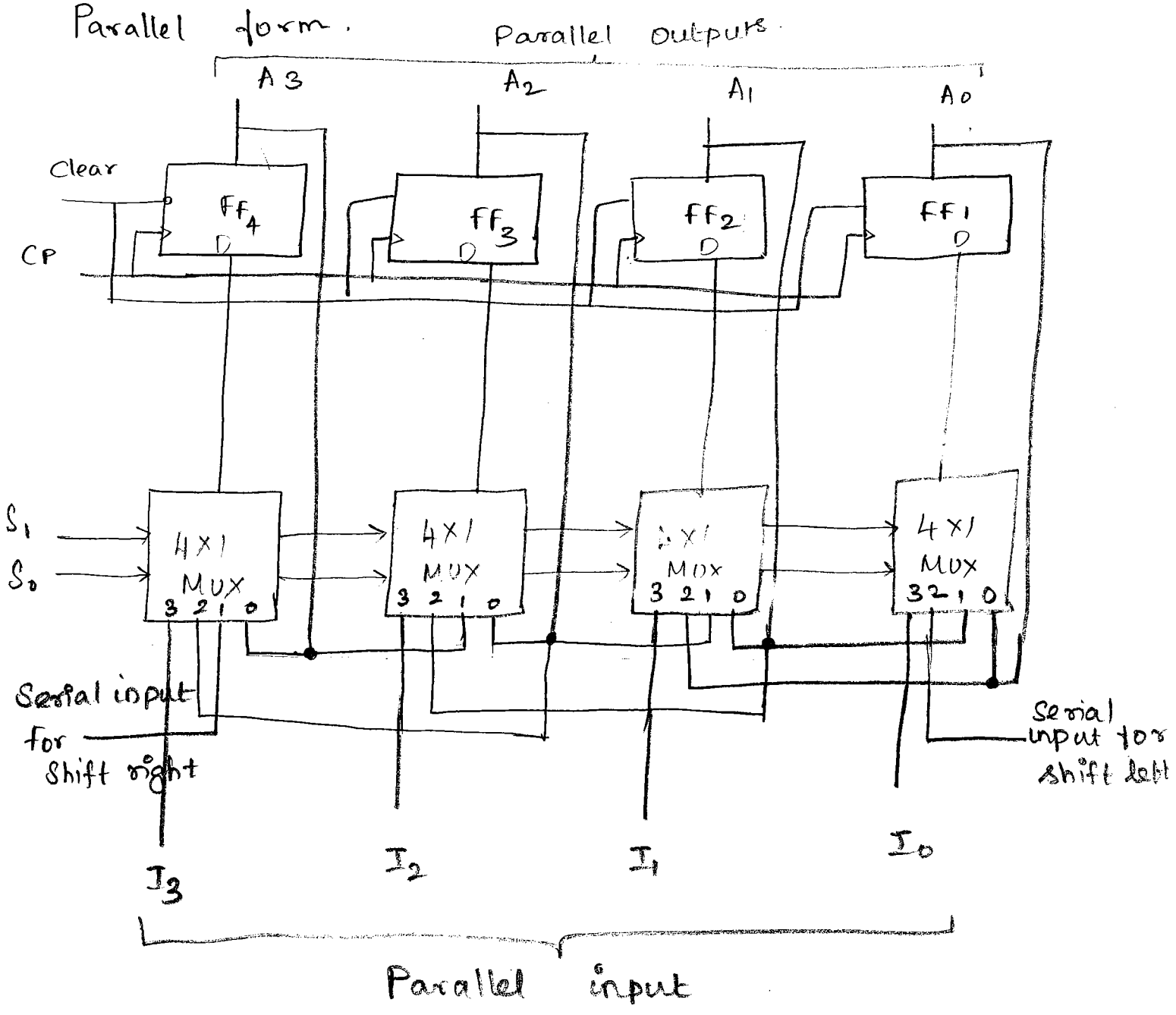
So called Bidirectional shift Register.

Universal Shift Registers:

A register capable of shifting in one direction only is a unidirectional shift register. A register capable of shifting in both direction is a bidirectional shift register.

* If the register has both shifts and parallel load capabilities, it is referred to as universal shift register.

* The universal shift register is a bidirectional register, whose output can be either in serial form or in parallel form and o/p can be in serial or Parallel form.



* It Consists of 4 FF and 4 mux
* four Mux are with same select inputs S_1 S_0.
* I/p = 0 (I_0) for all mux is selected. for
  $S_1 S_0 = 0\ 0$
* I/p = 1 (I_1) for all Mux is selected for
  $S_1 S_0 = 0\ 1$
* I/p = 2 (I_2) is selected for $S_1 S_0 = 1\ 0$.
* I/p = 3 (I_3) is selected for $S_1 S_0 = 1\ 1$.

For

I_0 => There is No change in the register Value

I_1 => Mux I/p have a path to D_1 FF and this causes FF to shift right the I/p. from f_1 to f_4.

I_2 => mux I/p has a Path to D_4 FF and causes FF to shift left the I/p from f_4 to F_1

I_3 => The Binary information is transferred through parallel lines into the register. simultaneously during next clock edge.

Mode Control

S_1	S_0	Register operation
0	0	No change in data.
0	1	shift right
1	0	shift left
1	1	parallel load.

Application of Shift Registers:

1. Digital Building Blocks.
2. Ring Counters etc.,
3. Temperory data Storage.
4. Bit Manipulation.

Counter:

It is a sequential circuit consisting of set of FF connected in a suitable manner to count the sequence of the input pulses presented to it in digital form.

Classification

1. Asynchronous and synchronous counters.
2. Single and multimode counters.
3. Modulus counters.

Asynchronous Counter:

* Also called as ripple counter or serial counter.
* Each Flip Flop is triggered by the output of the Previous Flip Flop.
* Speed of the operation is limited.
* Settling time of asynchronous counter is the cummulative sum of the individual settling time of Flip Flop

Synchronous Counter:

Also called as parallel counter.

Speed limitation of the above is overcome by applying clock pulse simultaneously to all the Flip Flop.

Settling time of this is equal to the propagation delay of a single Flip Flop.

Single mode Counter:

It operates in single mode

i.e) it counts either in up mode or in down mode.

Multimode counter:

It operates in both up and down modes.

Modulus Counter:

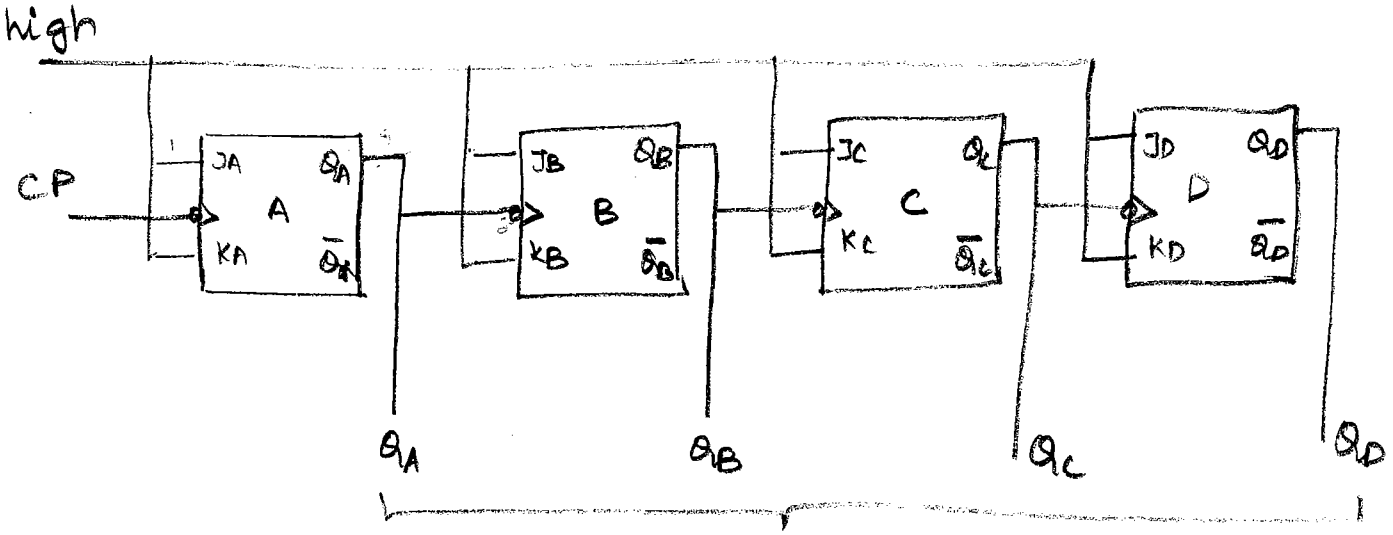
Modulus counters are defined based on the number of states they are capable of counting.

Applications:

Pulse Counting, frequency division, time measurement and Control.

Asynchronous Counter :-

up counter or Ripple Counter.



* CP is given to FF A
* In Asynchronous counter, the o/p of FF A is given as CP to FF B, o/p of FF B is given as the CP to FF C and so on.
* It has cummulative settling time, so its speed of operation is limited.
* T FF is used.
* Negative edge triggering is used
* Input is always high.

Operation:

1. Initially all the flipflops are cleared. so $Q_A = Q_B = Q_C = Q_D = 0$
2. CP is given to FF A, where as CP of FF B, FF C, FF D = 0 so $Q_A = 1$; $Q_B = Q_C = Q_D = 0$.
3. CP is given to FF A continuously; $Q_A = 0$

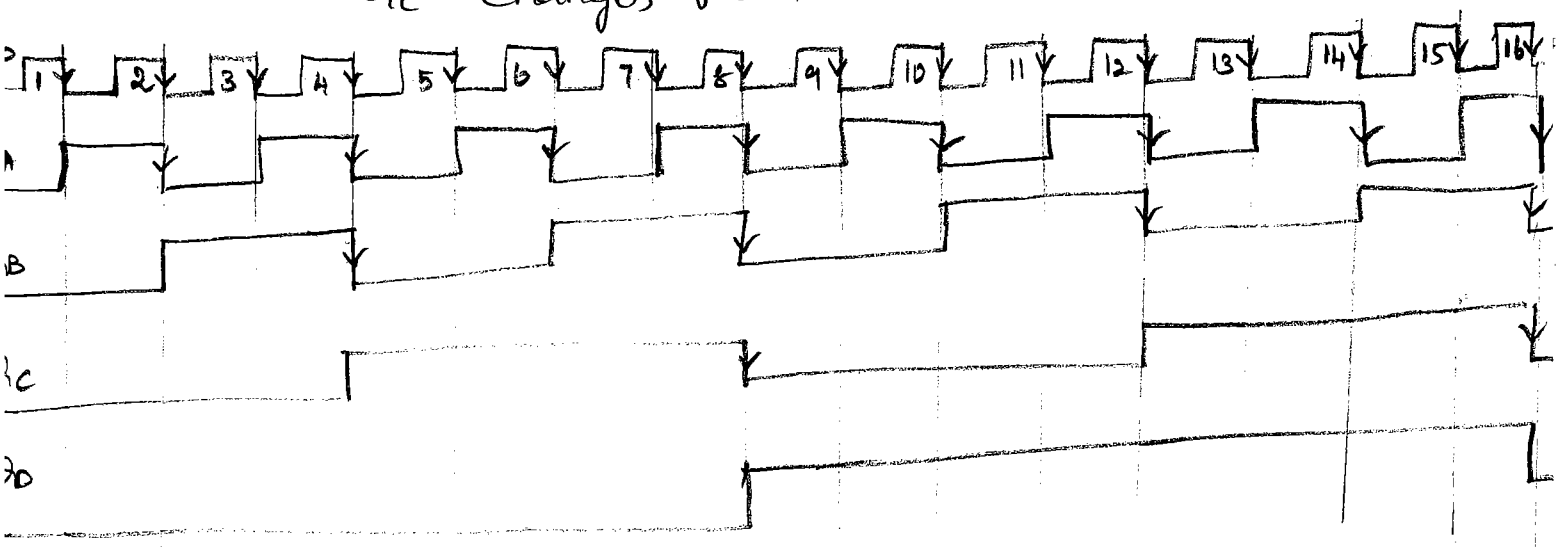
CP of Flip Flop B is 1 ; $Q_B = 1$; $Q_C = Q_D = 0$ and so on.

Note: During the negative transition i.e, from 1 to 0 change of state takes place.

When Q_A changes from 1 to 0 ; Q_B varies.

IIIrdly Q_B changes from 1 to 0 ; Q_C varies.

Q_C changes from 1 to 0 ; Q_D varies.



state	CP	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0	0
1	1	0	0	0	1
2	2	0	0	1	0
3	3	0	0	1	1
4	4	0	1	0	0
5	5	0	1	0	1
6	6	0	1	1	0
7	7	0	1	1	1
8	8	1	0	0	0
9	9	1	0	0	1
10	10	1	0	1	0
11	11	1	0	1	1
12	12	1	1	0	0
13	13	1	1	0	1
14	14	1	1	1	0
15	15	1	1	1	1

T FF

Q_n	T	Q_{n+1}
0	0	0
1	0	1
0	1	1
1	1	0

Modulus Counter:

* It has 16 different states. so it is called as MOD - 16 ripple counter.

MOD Number $= 2^n$

where n → NO- of F.F.

* The max binary no. counted by the counter $= 2^n - 1$

Frequency division or frequency scaling:

I/p pulses = Frequency f_o.

Q_A = Two i/p pulses result in a single pulse frequency $f_o/2$.

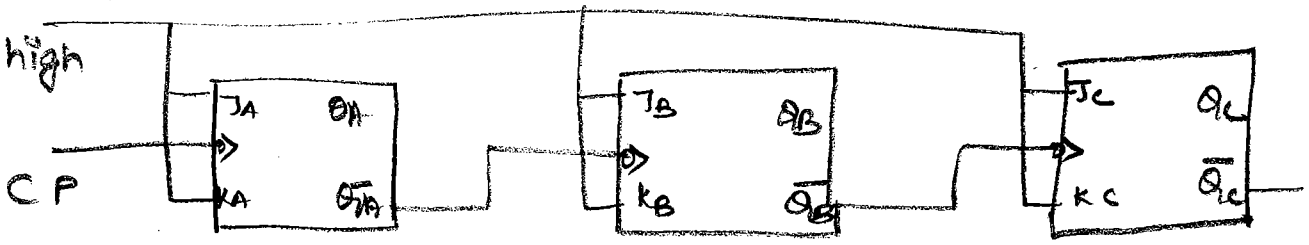
Q_B = Half of $Q_A = f_o/4$

$Q_C = f_o/8$

$Q_D = f_o/16$.

* used to devide the input frequency. It is called Frequency divider.
* Frequency $/2^n$.

DOWN COUNTER:



when $\overline{Q_A}$ changes from 0 to 1 ; Q_B varies.

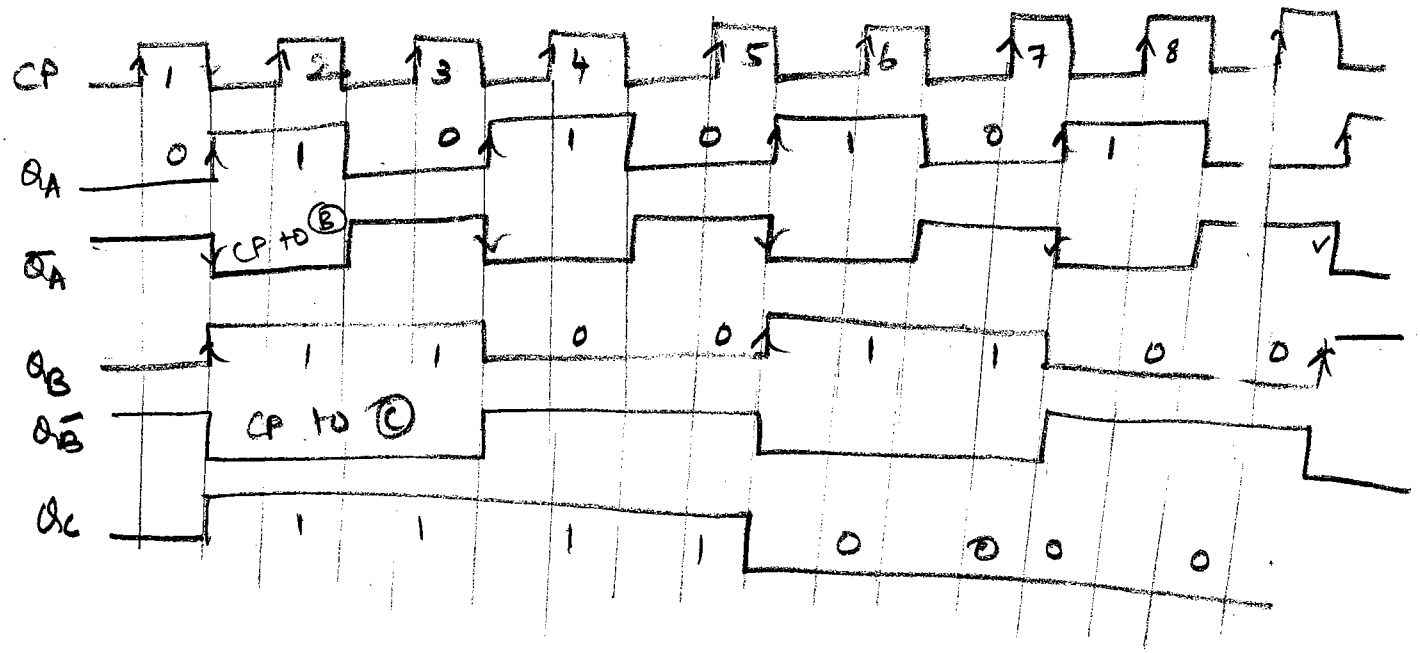
$\overline{Q_B}$ changes from 0 to 1 ; Q_C varies.

Initially $Q_A = Q_B = Q_C = 0$

CP given to FF1 NOW $Q_A \Rightarrow 0$ to 1;

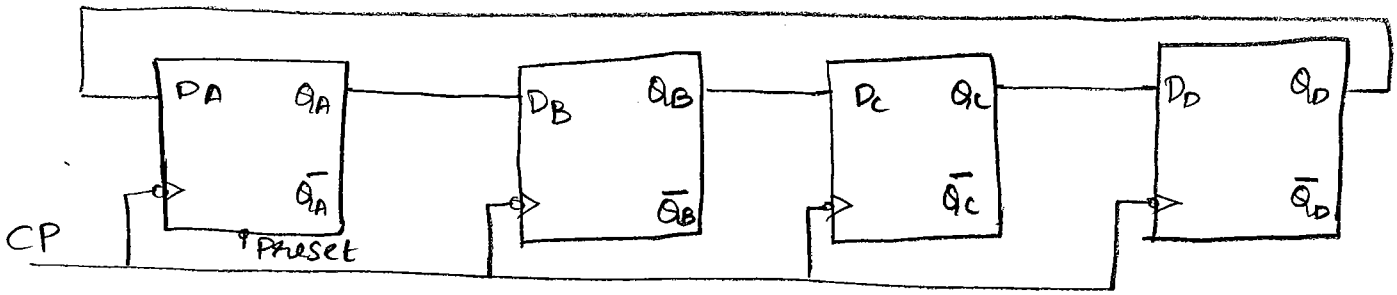
NOW Q_B varies and so on

state	Q_C	Q_B	Q_A
	0	0	0
7	1	1	1
6	1	1	0
5	1	0	1
4	1	0	0
3	0	1	1
2	0	1	0
1	0	0	1
0	0	0	0
7	1	1	1



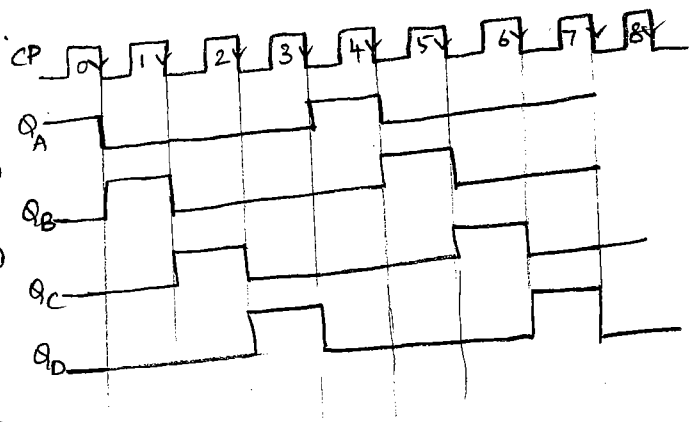
Shift Register Counter.

RING COUNTER:



* Output of the last stage is given as input to the first stage.
* Initially all the FF are cleared.
* Preset the FF A, so the O/P of $Q_A = 1$ when $CP = 0$ where $Q_B = Q_C = Q_D = 0$.
* Q_A O/P is given as a input for D_B $\therefore D_B = 1$ CP is applied; $Q_B = 1$ where $Q_A = Q_C = Q_D = 0$. and so on.

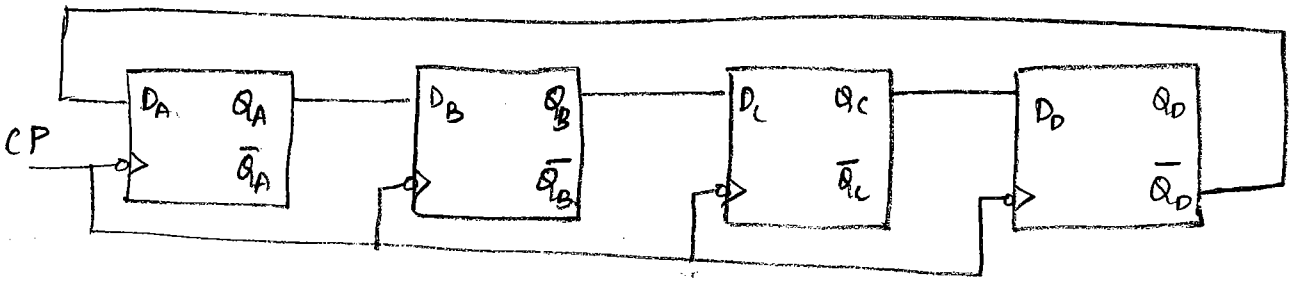
CP	Q_A	Q_B	Q_C	Q_D
0	1	0	0	0
1	0	1	0	0
2	0	0	1	0
3	0	0	0	1
4	1	0	0	0
5	0	1	0	0
6	0	0	1	0
7	0	0	0	1



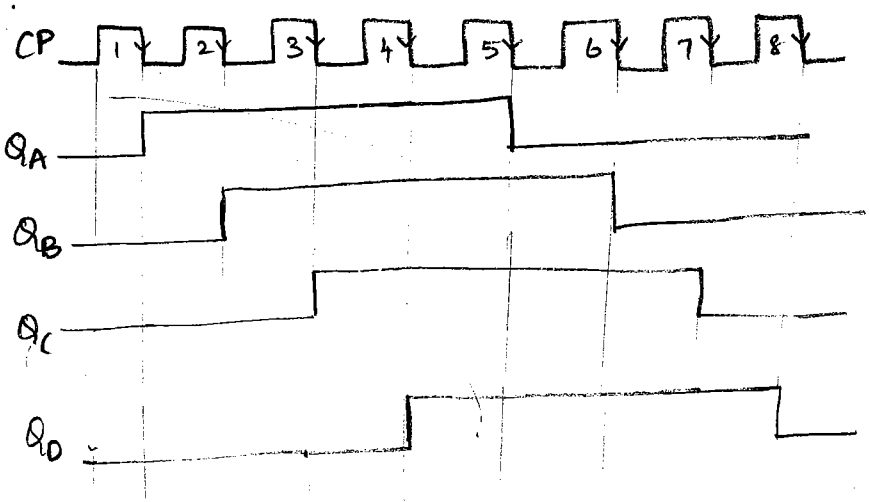
Johnson Counter (or) Twisted Ring Counter:

The output of each stage is connected as the input to the next stage.

$\bar{Q}$ o/p of last stage is given as a input to the first stage.



CP	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0



Design of Asynchronous Counter:

To Construct MOD-N Counter.

1. Find the no. of flip flop required

$$2^{n-1} \leq N \leq 2^n.$$

2. Connect all the FF as a ripple Counter.
3. Find the binary no. for N.
4. Connect all FF o/p's for which Q = 1 when the Count is N as inputs to NAND gate.
5. Connect the NAND gate o/p to the CLEAR i/p of each FF when the counter reaches its N^{th} state, the o/p of the NAND gate goes low resulting the FF to 0.
6. So the counter counts from 0 thr' N-1, having N- States.

1. Design of a MOD-6 Counter (Asynchronous Counter) using T FF.

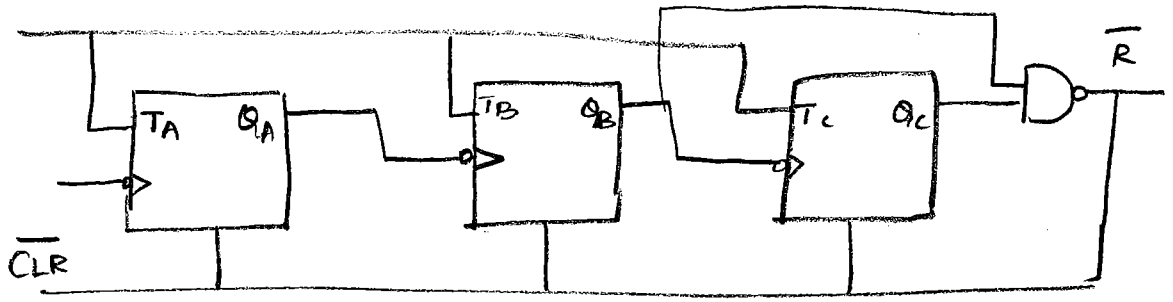
1. $2^{n-1} \leq N \leq 2^n$

$2^{3-1} \leq 6 \leq 2^3$ $\quad \therefore n = 3$

$4 \leq 6 \leq 8$

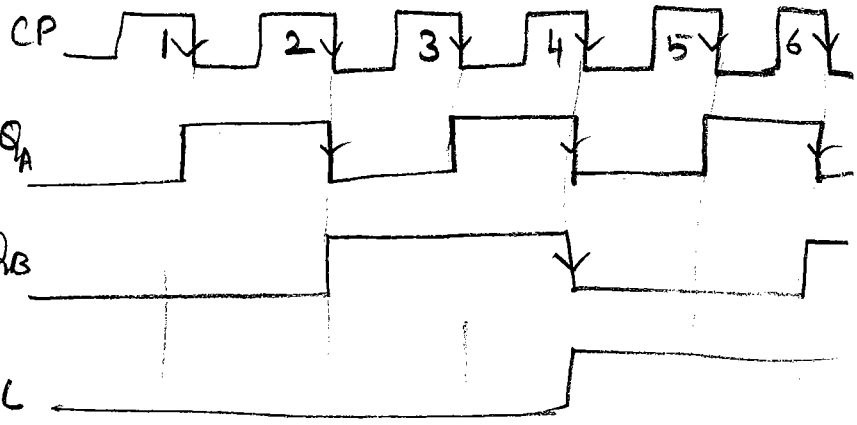
So No. of FF required is 3.

2. Construct the asynchronous counter.



* The binary value of N = 6 is 110
* o/p of Q_C & Q_B = 1, so it is connected to NAND gate
* o/p of NAND is given as CLEAR I/p for all FF
* When the Counter reaches 6; all the FF is Cleared. $Q_C Q_B Q_A$ $\quad Q_C = Q_B = 1$

State	Q_C	Q_B	Q_A	$\bar{R}$
0	0	0	0	1
1	0	0	1	1
2	0	1	0	1
3	0	1	1	1
4	1	0	0	1
5	1	0	1	1
6	1	1	0	0
7	0	0	0	→ All FF will be cleared.

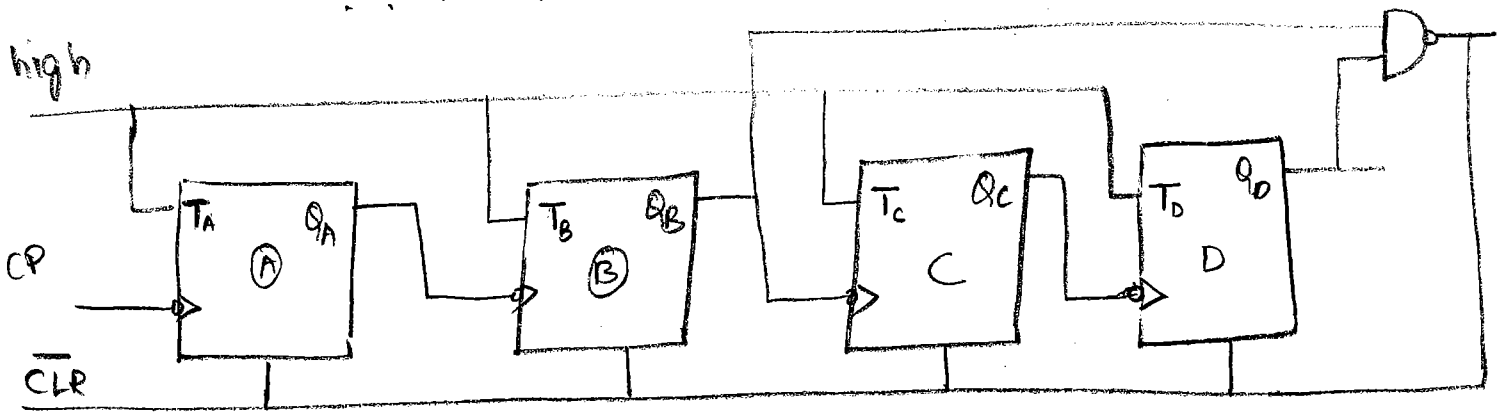


* Design of MOD-10 asynchronous counter.

1. $2^{n-1} \leq N \leq 2^n$

$2^3 \leq 10 \leq 2^4$.

$\therefore n = 4$.



Binary value of 10 is 10 10.

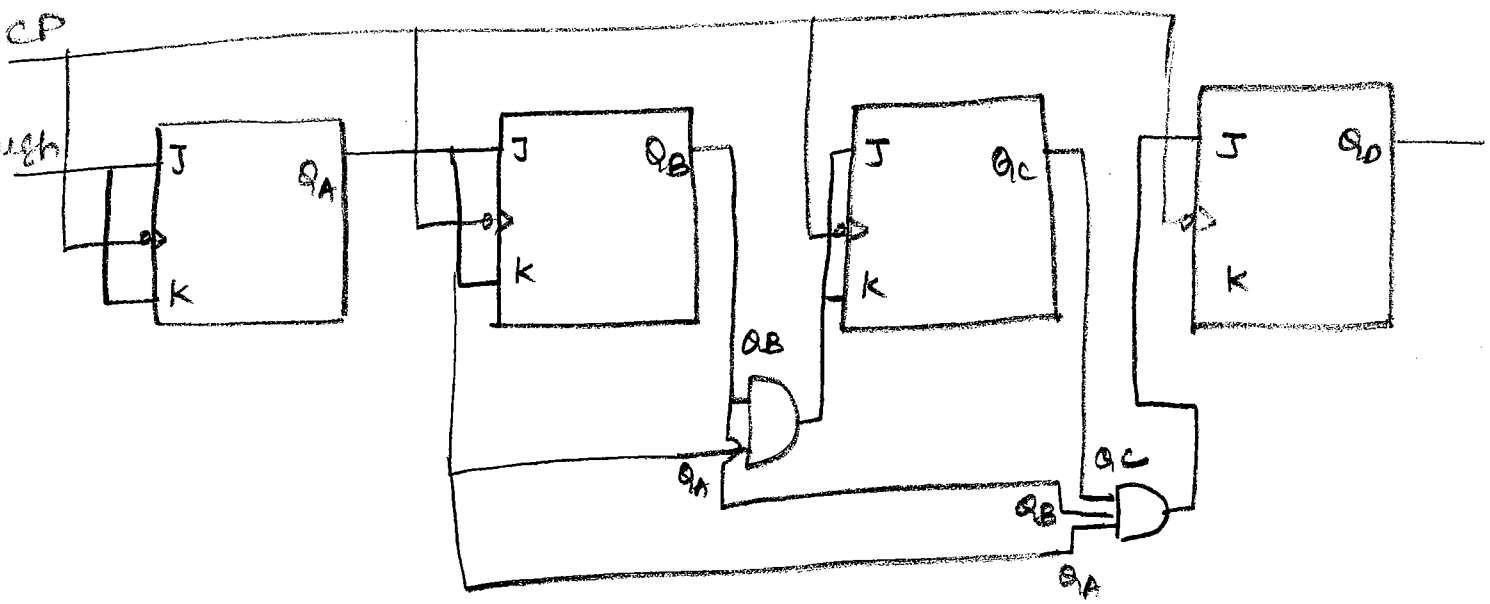
Q_D Q_C Q_B Q_A

1 0 1 0.

$Q_B = Q_D = 1$ clear all the flip flop.

Synchronous Counter

UP COUNTER:



Input pulses applied simultaneously to each ff.
FF A has its inputs J and K.
Input of other FlipFlop are driven by some combinations of FF outputs.

I/p of FF - A => 1

I/p of FF - B => Q_A.

I/p of FF - C => $Q_A \cdot Q_B$.

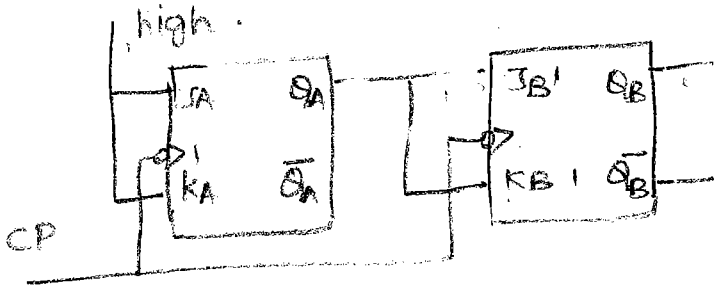
I/p of FF - D => $Q_A \cdot Q_B \cdot Q_C$.

Total delay = propogation delay of one FF + propagation delay of AND gate.

state	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

---

2 bit synchronous counter.



CP	Q_A	Q_B
0	0	0
1	1	0
2	0	1
3	1	1

Initially $Q_A = Q_B = 0$

CP is applied.

FF - A → toggle i.e., $J_A = K_A = 1$

FF - B output will be zero because $J_B = K_B = 0$.

After first clock pulse $Q_A = 1$ $Q_B = 0$

Step 2 : Negative going CP, both FF toggles.

$Q_A \Rightarrow 1 = 0$

$Q_B = 0 = 1$

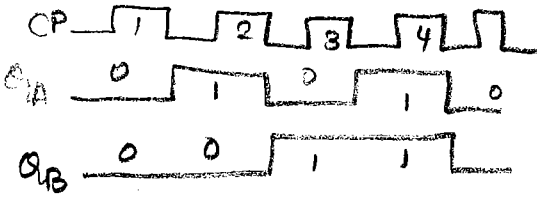
Here I/ps of

$J_A = K_A = J_B = K_B = 1$

After 2nd CP.

$Q_A = 0$

$Q_B = 1$ toggles.



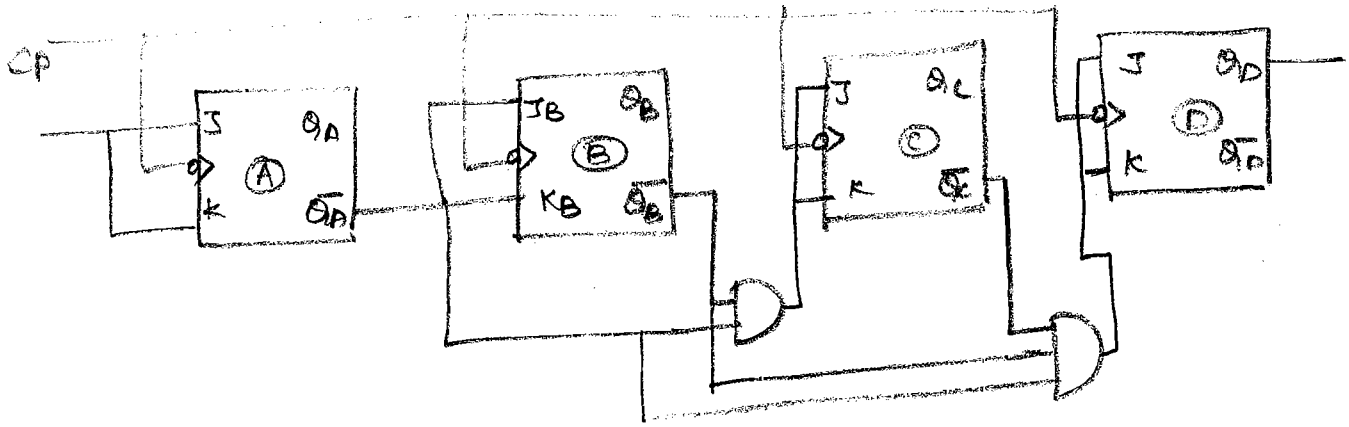
At Negative going edge 3rd pulse

FF A toggles making $Q_A = 1$

FF B remains same $Q_B = 1$.

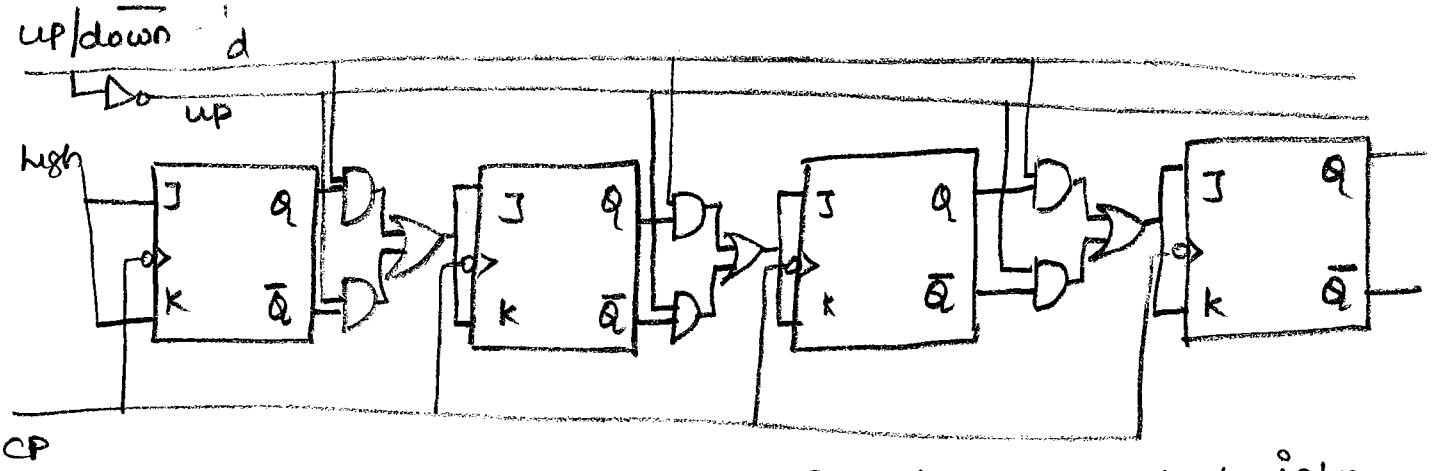
finally $Q_A = Q_B = 0$.

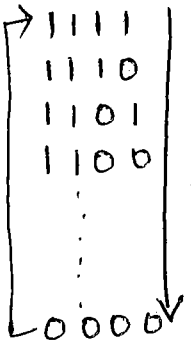
Synchronous Down Counter:



State	Q_D	Q_C	Q_B	Q_A
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0

Synchronous up/down Counter:





* up counter can be converted into down counter by connecting $\bar{Q}_A, \bar{Q}_B, \bar{Q}_C, \bar{Q}_D$ o/p in place of Q_A, Q_B, Q_C, Q_D.

* up/$\overline{\text{down}}$ is used to control FF o/p's are fed to the J and K inputs of the following FF.

* when up/$\overline{\text{down}}$ = 1 ⇒ ckt behave has a up counter.

* when up/$\overline{\text{down}}$ = 0 ⇒ ckt behaves has a down counter

Design of Synchronous Counter:

* determine the required no. of FF ($N \leq 2^n$)

* Draw the state diagram showing all the possible states. state diagram also called as transition diagram.

* Select the type of ff to be used.

* using K-map, obtain the minimal expressions for the excitations of FF's.

* Draw a logic diagram.

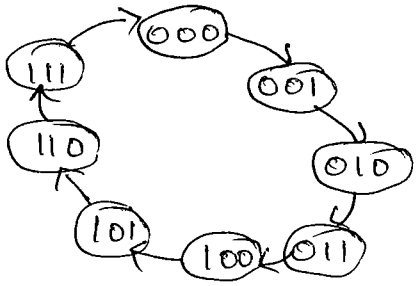
Note:

write the excitation table [PS and NS is to be listed].

1. Design of synchronous 3 bit up counter:

I No. of FF (n) : $n = 3$.

II State diagram.



Q_n	Q_{n+1}	J	K
0	0	0	0/1
0	1	1	0/1
1	0	0/1	1
1	1	0/1	0

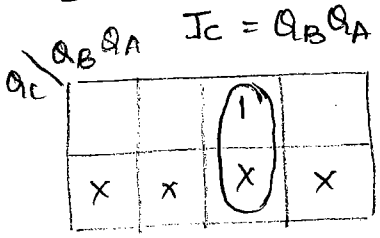
III Select JK Flip Flop.

Excitation table:

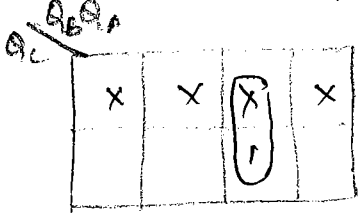
PS			NS								
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

IV K-Map reduction:

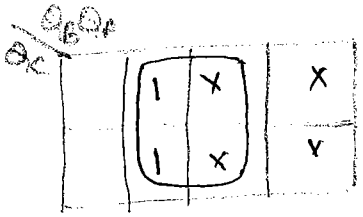
$J_C = Q_B Q_A$



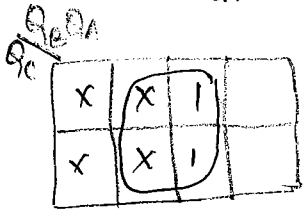
$K_C = Q_B Q_A$



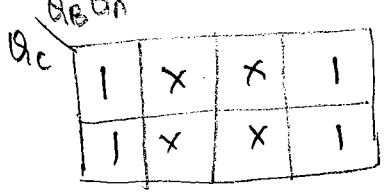
$J_B = Q_A$



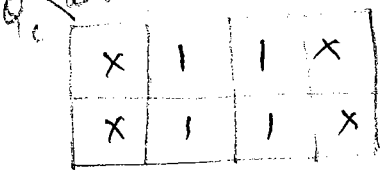
$K_B = Q_A$



J_A

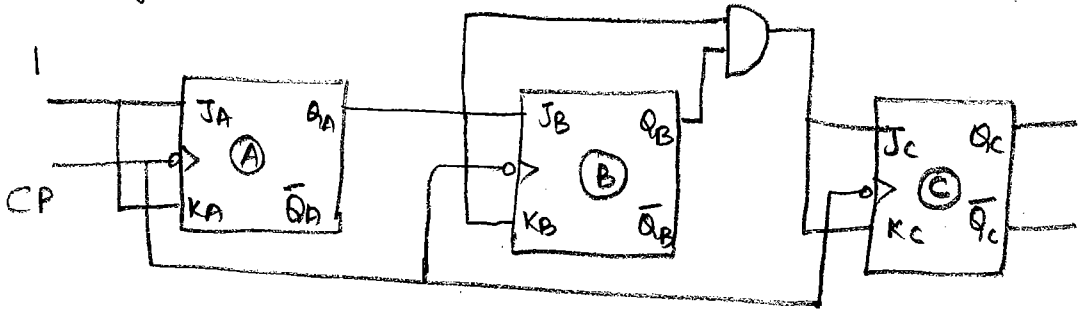


K_A.



$J_A = K_A = 1$

V Logic diagram:



2. Design of Synchronous MOD-6 Counter.

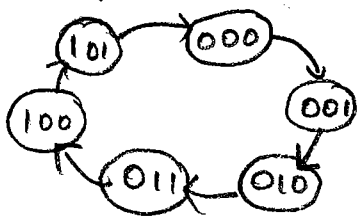
I No. of FF : $N \leq 2^n$

$6 \leq 2^3$ (8)

$\therefore n = 3$

II State diagram:

6, 7 Don't Care

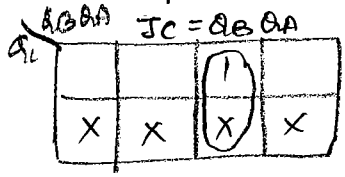


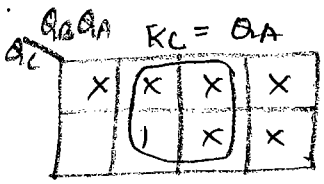
III Select JK FF

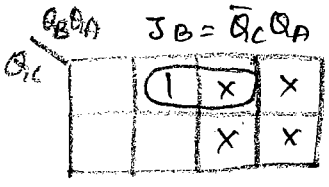
Excitation table.

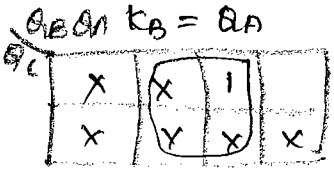
PS			NS								
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	X	X	X	X	X	X	X	X	X
1	1	1	X	X	X	X	X	X	X	X	X

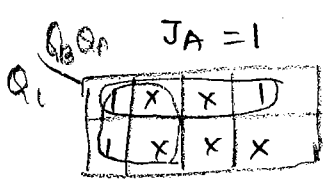
IV K-Map Reduction.

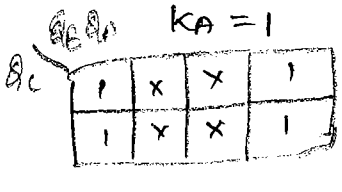




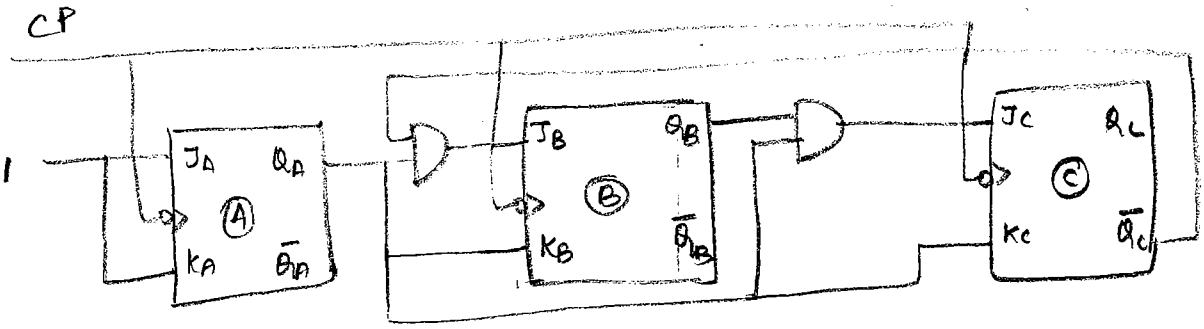






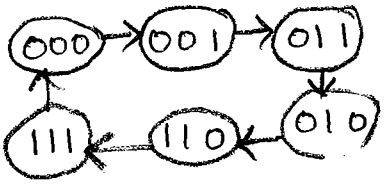


V Logic diagram.



3. Design of a synchronous MOD-6 gray Counter.

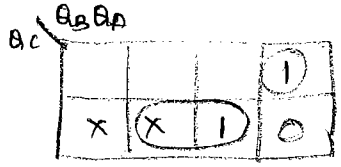
1. No. of FF = 3
2. State diagram
3. Select T FF Excitation Table.



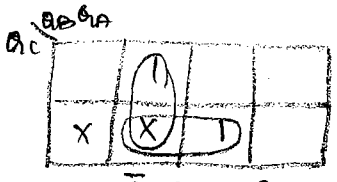
binary	gray
000	000
001	001
010	011
011	010
100	110
101	111
110	101 x
111	100 x

PS			NS					
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	0	1	0	0	0	1
0	1	0	1	1	0	1	0	0
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1
1	0	1	x	x	x	x	x	x
1	0	0	x	x	x	x	x	x

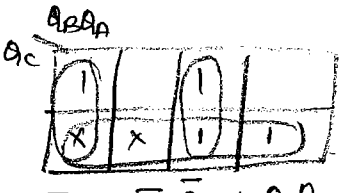
4. K-map reduction



$T_C = Q_C Q_A + \bar{Q}_C Q_B \bar{Q}_A$

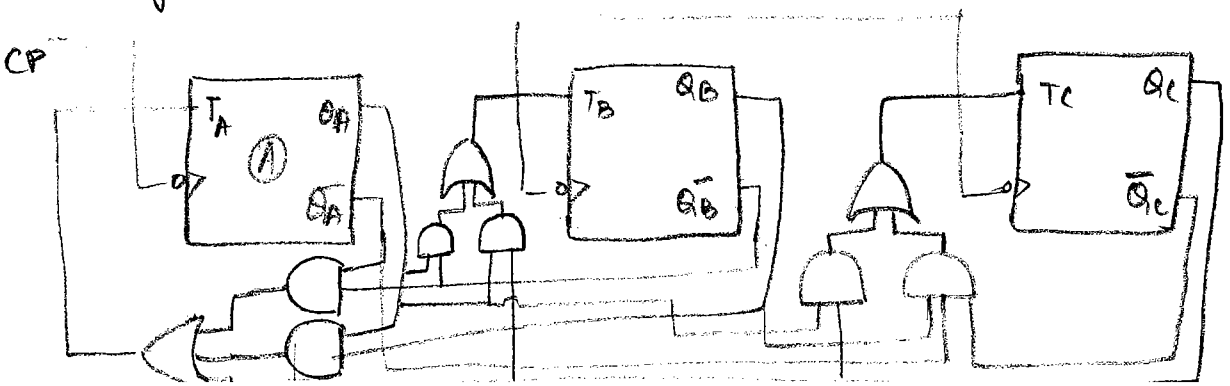


$T_B = \bar{Q}_B Q_A + Q_C Q_A$



$T_A = \bar{Q}_B \bar{Q}_A + Q_B Q_A + Q_C$.

5. Logic diagram.



Sequential Circuits.
(Finite State Machines FSMs)

The synchronous or clocked sequential circuits are represented by two models.

(1) Moore Circuit.
(2) Mealy Circuit.

Moore Circuit:

In this model, the o/p depends only on the Present state of the FF.

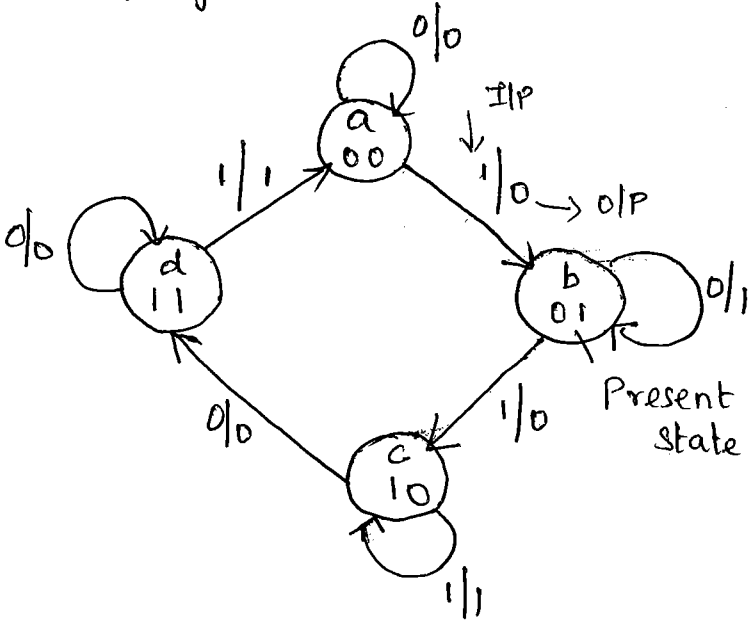
Mealy circuit:

In this model, the o/p depends on both the present state of the FF and the inputs.

State diagram.

* pictorical representation of the relationship between the present state, input, Next state and output.

Mealy Circuit:



State diagram

State Table.

PS	Next state I/P x		output	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	b	c	1	0
c	d	c	0	1
d	d	a	0	1

* State is represented by a circle also called node or vertex.
* Transition b/w the states is indicated by directed lines connecting the circles.

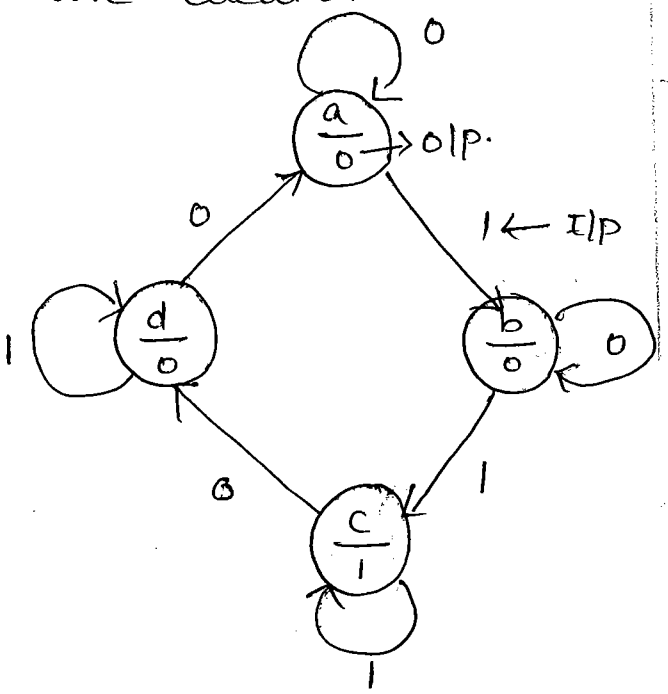
* The line connecting a circle with itself indicates, the next state is same as the present state.

* The directed lines are labelled with 2 binary numbers seperated by a symbol (/ slash).

* The input value is labelled first

o/p value is labelled next.

Moore circuit:-



P.S	NS x=0	NS x=1	o/p
a	a	b	0
b	b	c	0
c	d	c	1
d	a	d	0

State diagram.

* The directed lines are labelled with only one binary no. representing the i/p.

* The o/p is indicated within the circle below the Present state.

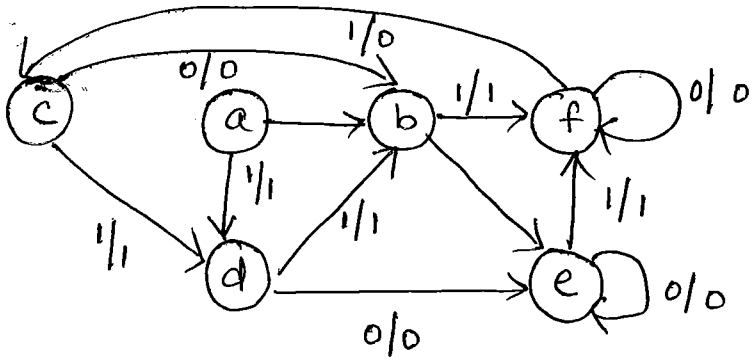
NS → Next state of the flip flop after the application of clock pulse.

State Reduction:

* It avoids the introduction to redundant state.

* Redundant state reduces the no. of FF and logic gates, reducing the cost of the final circuit

* When two states are equivalent one of them can be removed without altering i/p - o/p relationship



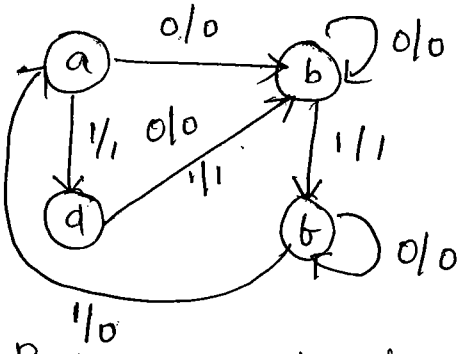
PS	NS x=0	NS x=1	O/P x=0	O/P x=1
a	b	d	0	1
b	b	f	0	1
d	b	b	0	1
f	f	a	0	0

Reduced state table

PS	NS x=0	NS x=1	O/P x=0	O/P x=1
a	b	d	0	1
b	e	f	0	1
c	b	d	0	1
d	e	b	0	1
e	e	f	0	1
f	f	c	0	0

instead of c use a

instead of d use b



Reduced state diagram.

State assignment

* The process of assigning binary values of the states of the sequential machine is known as state assignment.

Rules of state assignment

I states having the same Next state for a given input condition should have assignments which can be grouped into logically adjacent cells in a k-map.

II states that are the next state of a single state should have assignments which can be grouped into logically adjacent cells in k-map.

Transition of o/p table.

It can be obtained from the state table by modifying the entries of the state table with the selected state assignment.

Excitation table:

* It gives information about the excitations to be applied to the FF to bring the m/c from the present state to the next state.

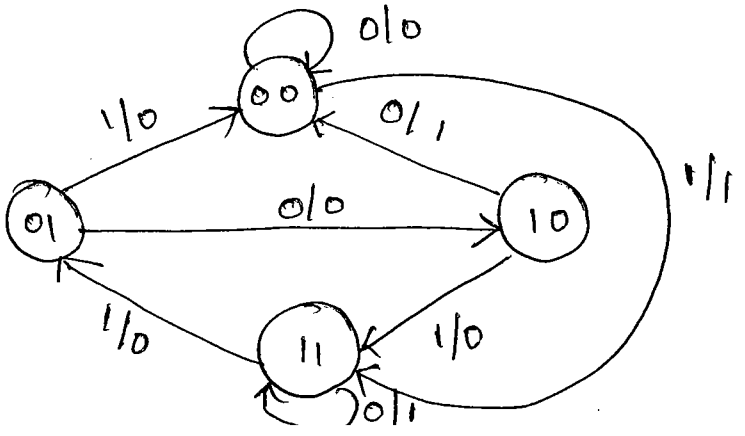
Design of synchronous sequential circuit.

1. Obtain the design specifications and study the same clearly to understand the operational behaviour of the circuit.
2. Construct the state diagram.
3. Develop the state table.
4. Reduced standard form state table - by removing the redundant states.
5. State assignment & transition table - Assign the binary values to the states and write the transition table.
6. Choose the type of FF & form the excitation table.
7. Draw the K-map and find the minimal expressions.
8. Draw the circuit to realize the minimal expressions obtained above.

1. A sequential circuit has one i/p and one o/p. The state diagram is shown.

Design the sequential circuit with (1) D FF

2. T FF.



State table:

P.S	N.S		O/P	
	x=0	x=1	x=0	x=1
00	00	11	0	1
01	10	00	0	0
10	00	11	1	0
11	11	01	1	0

No. of states = 4 states.

No. of Flip flop $\Rightarrow 2^{n-1} \leq N \leq 2^n$. $n=2$.

$2^1 \leq N \leq 2^2$

$2 \leq 4 \leq 4$

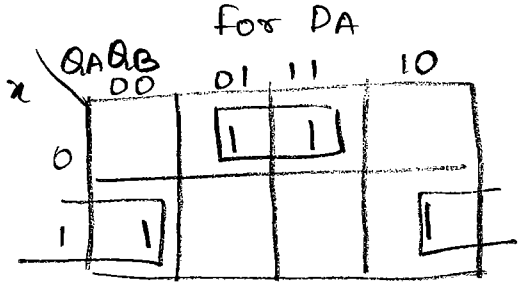
$\therefore$ No. of FF = 2

Design using D Flip Flop.

x	Q_A	Q_B	Q_{A+1}	Q_{B+1}	D_A	D_B	Y.
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	0	1
0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1
1	0	1	0	0	0	0	0
1	1	0	1	1	1	1	0
1	1	1	0	1	0	1	0

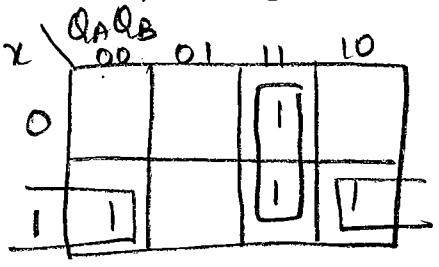
K-Map Reduction:

For D_A



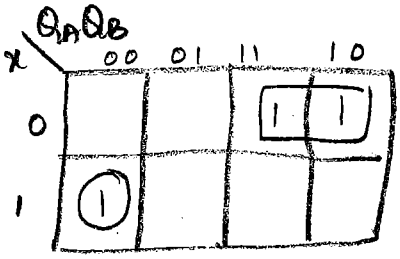
$D_A = \bar{x}Q_B + x\bar{Q}_B$

For D_B

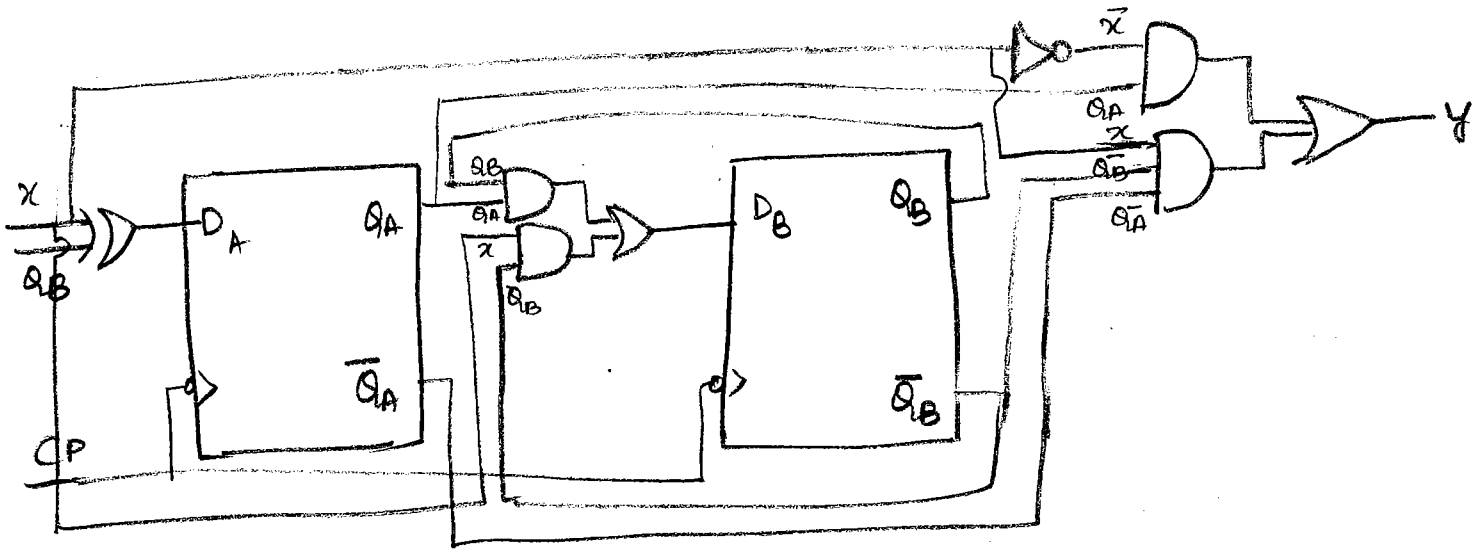


$D_B = Q_AQ_B + x\bar{Q}_B$

For Y



$Y = \bar{x}Q_A + x\bar{Q}_A\bar{Q}_B$

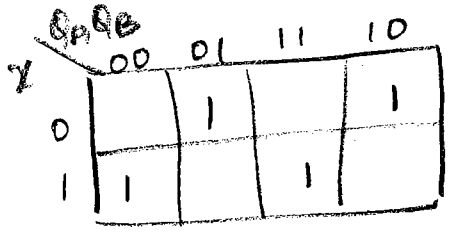


Design using T Flip Flop.

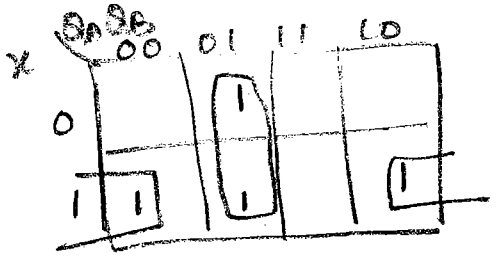
X	PS Q_A	PS Q_B	NS Q_{A+1}	NS Q_{B+1}	T_A	T_B	Y
0	0	0	0	0	0	0	0
0	0	1	1	0	1	1	0
0	1	0	0	0	1	0	1
0	1	1	1	1	0	0	1
1	0	0	1	1	1	1	1
1	0	1	0	0	0	1	0
1	1	0	1	1	0	1	0
1	1	1	0	1	1	0	0

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

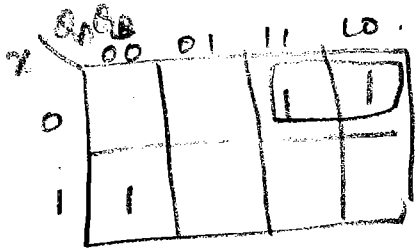
K-map reduction:



FOR TA



for T_B

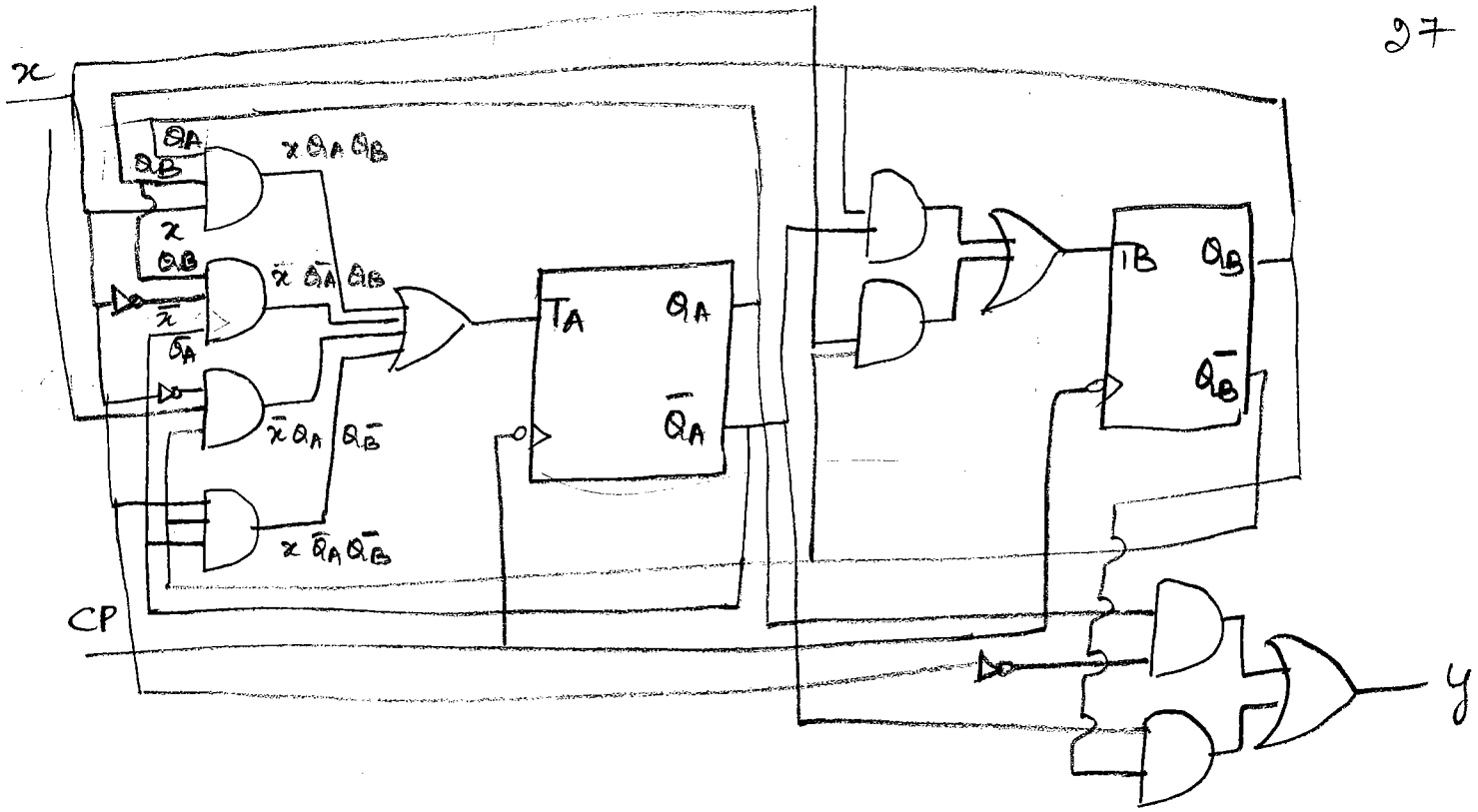


for Y.

$$T_A = \bar{x}\bar{Q}_A Q_B + \bar{x} Q_A \bar{Q}_B + x \bar{Q}_A \bar{Q}_B + x Q_A Q_B$$

$$T_B = \bar{Q}_A Q_B + x \bar{Q}_B$$

$$y = \bar{x} Q_A + \bar{Q}_A Q_B$$



2. A sequential circuit with two D FF's A and B, two i/p's X & Y; o/p Z is specified by the following eq.

$$A(t+1) = \bar{x}y + xA$$

$$B(t+1) = \bar{x}B + xA$$

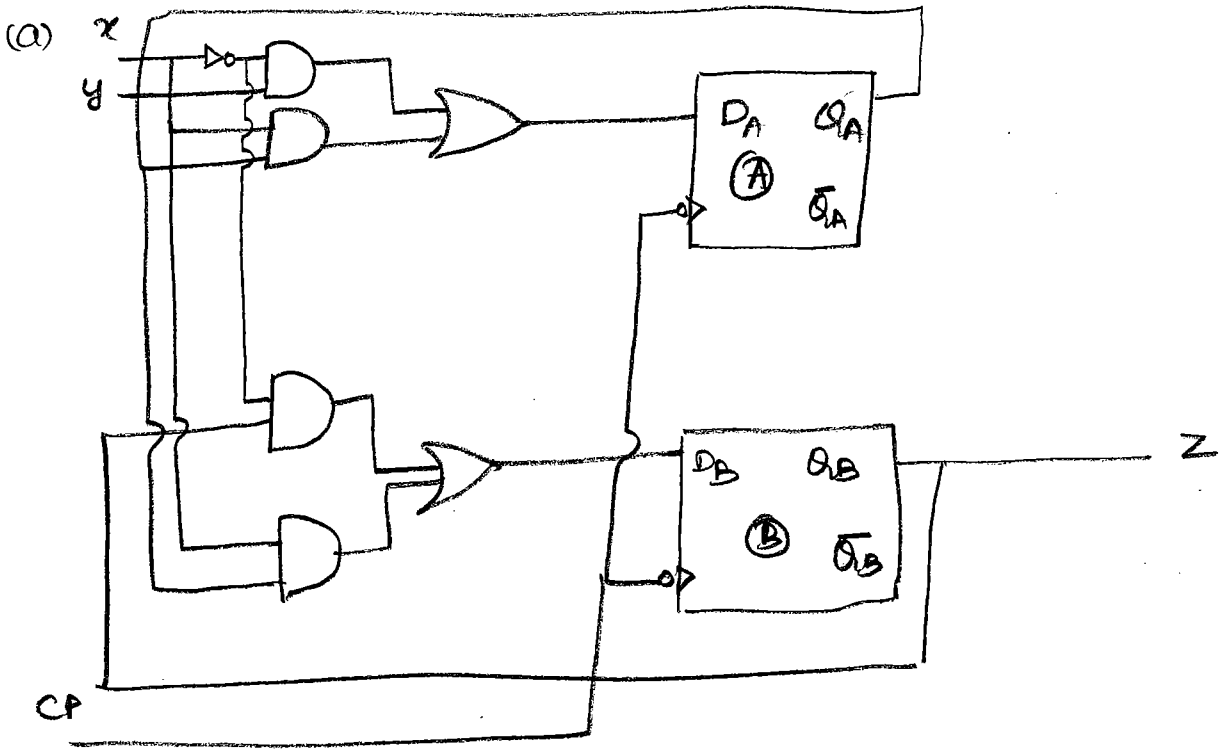
$$Z = B.$$

a) Draw the logic diagram of the circuit.

b) Derive the state table

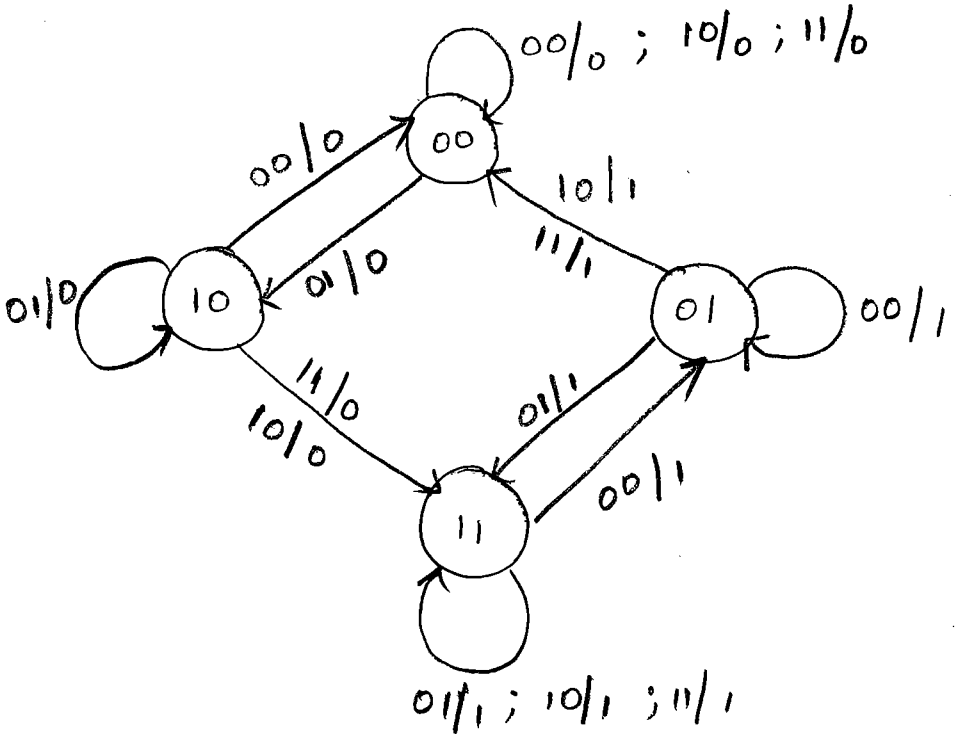
c) Derive the state diagram.

(a)

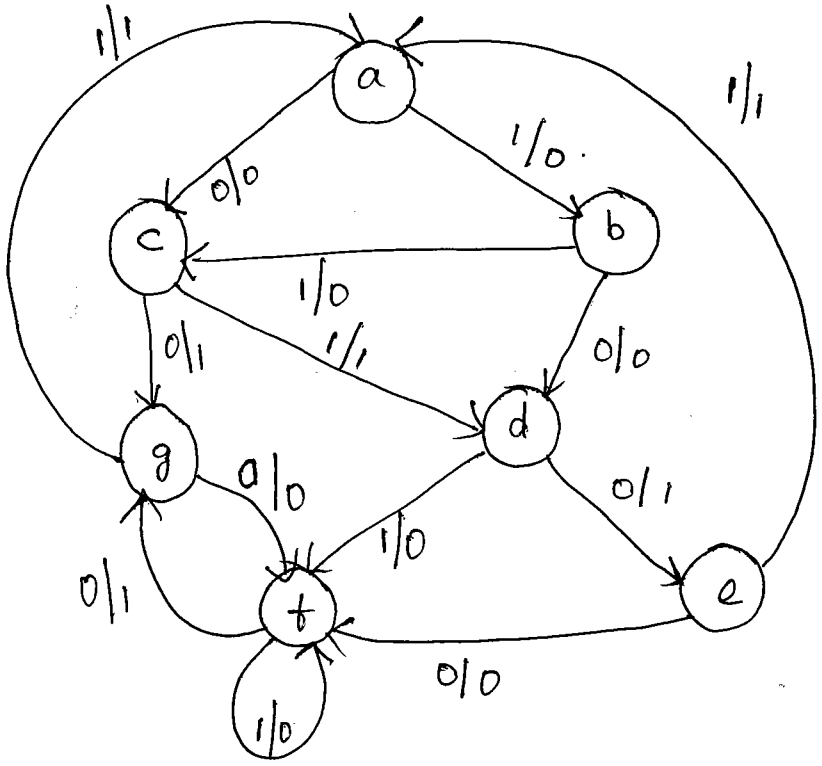


	PS	(00) NS x=0; y=0		O/P	PS	(01) NS		O/P	PS	10 NS		O/P	PS	(11) NS		O/P
q_A	q_B	Q_{A+1}	Q_{B+1}	Z	Q_A	Q_B	Q_{A+1}	Q_{B+1}	Z	Q_A	Q_B	Q_{A+1}	Q_{B+1}	Z	Q_A	Q_B	Q_{A+1}	Q_{B+1}	Z
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	1	0	1	1	1	1	0	1	0	0	1	0	1	0	0	1
1	0	0	0	0	1	0	1	0	0	1	0	1	1	0	1	0	1	1	0
1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

State diagram



3. Design a clocked Sequential circuit for state diagram.



State table.

PS	NS		O/P y	
	x=0	x=1	x=0	x=1
a	c	b	0	0
b	d	c	0	0
c	g	d	1	1
d	e	f	1	0
e	f	a	0	1
f	g	f	1	0
g	f	a	0	1

→ Replace 'e' by 'g' (or) 'g' by 'e'

PS	NS		Output	
	x=0	x=1	x=0	x=1
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	f	1	0
e	f	a	0	1
f	e	f	1	0

Replace F by d or d by f.

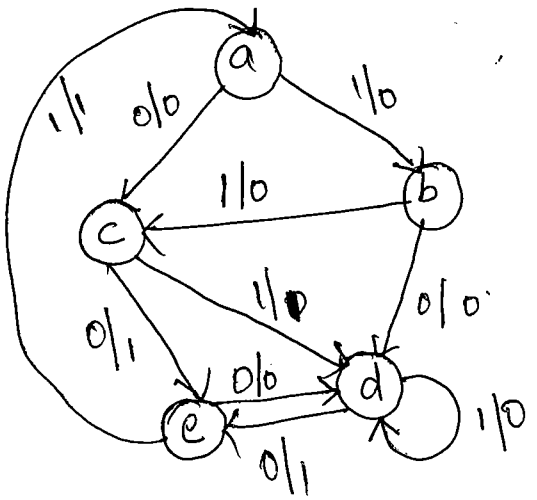
PS	NS		Output	
	x=0	x=1	x=0	x=1
a	c	b	0	0
b	d	c	0	0
c	e	d	1	1
d	e	d	1	0
e	d	a	0	1

Reduced state table

No. of states = 5

No. of FF = 3.

Reduced state diagram.



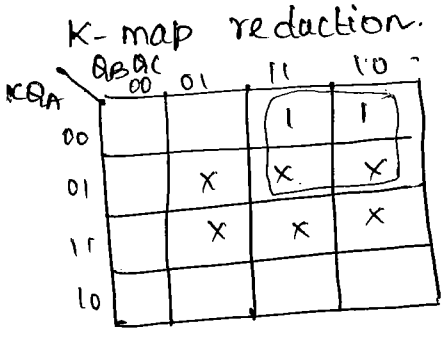
a = 000
b = 001
c = 010
d = 011
e = 100

PS	NS		O/P	
	x=0	x=1	x=0	x=1
000	010	001	0	0
001	011	010	0	0
010	100	011	1	1
011	100	011	1	0
100	011	000	0	1

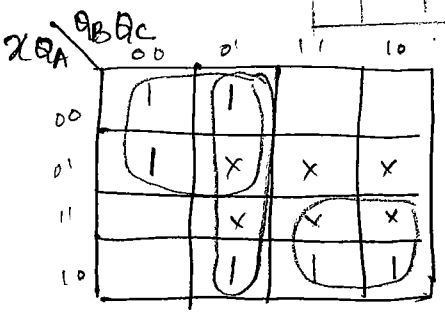
Here; 0101, 0110, 0111, 1101, 1110, 1111 are don't Cares.

x	Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	y	D_A	D_B	D_C
0	0	0	0	0	1	0	0	0	1	0
0	0	0	1	0	1	1	0	0	1	1
0	0	1	0	1	0	0	1	1	0	0
0	0	1	1	1	0	0	1	1	0	0
0	1	0	0	0	1	1	0	0	1	1
1	0	0	0	0	0	1	0	0	0	1
1	0	0	1	0	1	0	0	0	1	0
1	0	1	0	0	1	1	1	0	1	1
1	0	1	1	0	1	1	0	0	1	1
1	1	0	0	0	0	0	1	0	0	0

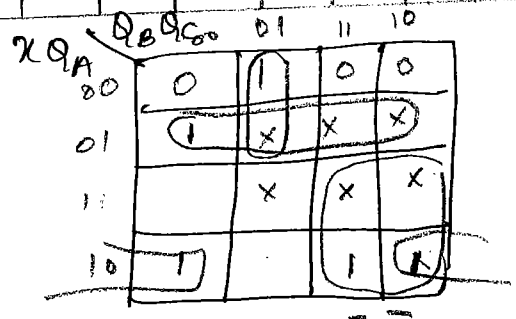
K-map reduction.



$\bar{x}Q_B$

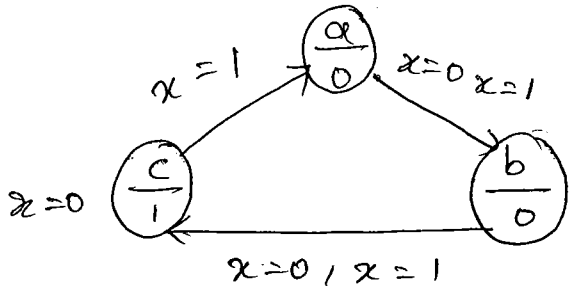


$\bar{x}\bar{Q}_B + \bar{Q}_BQ_C + xQ_B$



$\bar{x}Q_A + xQ_B + \bar{x}\bar{Q}_BQ_C + x\bar{Q}_AQ_C$

Realise a Sequential Circuit for the state diagram using DFF.



State table :

PS	NS		O/P
	x=0	x=1	
a	b	b	0
b	c	c	0
c	c	a	1

No. of state = 3.

No. of ff = 2.

State Assignment :

PS		NS				O/P
		x=0		x=1		
Q_A	Q_B	Q_{A+1}	Q_{B+1}	Q_{A+1}	Q_{B+1}	
0	0	0	1	0	1	0
0	1	1	0	1	0	0
1	0	1	0	0	0	1

x	PS Q_A	PS Q_B	NS Q_{A+1}	NS Q_{B+1}	D_A	D_B
0	0	0	0	1	0	1
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	x	x	x	x
1	0	0	0	1	0	1
1	0	1	1	0	1	0
1	1	0	0	0	0	0
1	1	1	x	x	x	x

x \ Q_AQ_B	00	01	11	10
0		1	X	1
1		1	X	

$$D_A = Q_B + \bar{x}Q_A$$

x \ Q_AQ_B	00	01	11	10
0	1		1	
1	1		1	

$$D_B = \bar{Q}_A\bar{Q}_B$$