Runzhou, Chen

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EDUCATION

University of California, Los Angeles (UCLA) *M.S. in Electronic and Computer Engineering* *Sep. 2021 - Jun. 2023*

- GPA 3.7/4.0
- Courses: Signaling and Synchronization, Analysis and Design of RF Circuits and Systems, Analog Integrated Circuit Design, Design of VLSI Circuits and Systems

Hong Kong University of Science and Technology *B.Eng. in Electronic and Computer Engineering* *Sep. 2017 - Jun. 2021*

- GPA 3.82 / 4.3 (1st Class honor)
- Courses: High Frequency Integrated Circuits Design, Advanced Analog IC Analysis and Design, Integrated Power Electronics, FPGA-based Design: From Theory to Practice, Introduction to Embedded Systems

Swiss Federal Institute of Technology Zurich (ETH Zurich) *International Exchange* *Feb.2020 - Aug. 2020*

- Courses: Power Semiconductors, Information System for Engineers, Communication Networks

SKILLS

Programing Language: MATLAB, VHDL, Verilog, Python, C, C++, Java, SQL, MIPS Assembly

Engineering Software: Cadence Virtuoso, LTspice, ADS, HFSS, HSpice, PSpice, Synopsys, Keil, Xilinx ISE, Android Studio, etc.

PUBLICATION

- "LiDR: Visible Light Communication-Assisted Dead Reckoning for Accurate Indoor Localization," in IEEE Internet of Things Journal, doi: 10.1109/JIOT.2022.3151664.
- "Camera Pose Estimation using a VLC-Modulated Single Rectangular LED for Indoor Positioning," in *IEEE Transactions on Instrumentation & Measurement* doi: 10.1109/TIM.2022.3212980

RESEARCH EXPERIENCE

Master Research Project: "135GHz BiCMOS ×15 Frequency Multiplier with High Harmonic Rejection"

UCLA, ECE Dept., High Speed Electronics Lab (HSEL) (Advisor: Professor M. C. Frank Chang) *Jun.2022 – Sep.2022*

- Design the 135GHz ×15 Frequency Multiplier in Global Foundry 40-nm BiCMOS (tape-out by Global Foundry on Sep 2022). The frequency multiplier is expected to have 4-dB conversion gain, 6-dBm P_{sat} and 97mW DC power.
- Achieve high harmonic rejection (>30dB) with the help of inter-stage filtering in-stage filtering.

Master Research Project: "Reconfigurable Transceiver for D-Band FMCW and Spread-Spectrum (SS) Radars"

UCLA, ECE Dept., High Speed Electronics Lab (HSEL) (Advisor: Professor M. C. Frank Chang) *Dec.2021 – May.2022*

- Design and test the D-Band low noise amplifier (LNA) in TSMC 16-nm CMOS for the Frequency-Modulated Continuous Wave radar. The LNA is expected to have 10-GHz bandwidth, 20-dB gain and less than 9-dB NF.
- Implement the novel noise-cancelling strategy for the LNA to further reduce its noise by over 3dB per stage.
- Develop the × 8 frequency multiplier that generates the operating frequencies (144GHz) for the FMCW radar based on the 2nd to 4th harmonics of the input frequency (tape-out by TSMC on May 2022).

Senior Year Project: "Smart Displays and Projectors with Embedded Visible Light Communication (VLC)"

HKUST, ECE Dept., Optical Wireless Lab (OWL) (Advisor: Professor Patrick Yue) *Sep.2020 – May.2021*

- Proposed a smart display system using VLC technology for IoT application. Made use of perspective geometry and homogeneous matrix to develop a new algorithm in MATLAB and C++ for indoor positioning and Pedestrian Dead Reckoning (PDR) based on single rectangular LED. Then measured the accuracy of the algorithm and applied it to the indoor positioning for robotic vehicles.
- Won the Silver Award for ECE Final Year Project Industry Day 2021 and contributed to two IEEE publications.

PROJECT EXPERIENCE

"An 8-Gbps High-Speed I/O Link with Equalization and Offset Cancellation"

UCLA, ECE Dept., EE 215E Signaling and Synchronization (Instructor: Professor Sudhakar Pamarti) *Mar.2022 – May.2022*

- Design and simulate a differential link over a given channel (based on Cadence Spectre model) while maximizing the data rate.
- Implement the I/O equalizations including Tx pre-emphasis and Rx-CTLE based on the generic 90nm PDK. Then enable a ±50% range of

programmability for the Tx pre-emphasis and a $\pm 20mV - \pm 2.5mV$ digital offset cancellation at the Rx-CTLE.

- The link operates at 8 Gbps with an output eye-opening larger than 100mV (under SS, TT and FF conrners) and an average power of 30mW. The Tx slew rate is limited to less than $T_{bit}/3$ each.

"A 200-GHz Broadband Power Amplifier with 2-to-1 Power Combining"

UCLA, ECE Dept., EE 279AS Special Topics in Physical and Wave Electronics (Instructor: Professor Aydin Babakhani) *Mar.2022 – May.2022*

- Design a 200-GHz broadband power amplifier using the ADS and transistors provided in the IHP design kit.
- Use the transmission lines with a loss of 0.4 dB per 90 degrees for the tunning and a 2-to-1 Wilkinson power divider to improve the $P_{out.}$ Then run the HB simulation in ADS to verify its behavior.
- The PA has a performance of 21-dB small-signal gain, 134-GHz 3-dB bandwidth, 12% PAE, input and output matching between 180GHz and 220GHz, 10.4-dBm P_{sat}, 7-dBm P_{IIP3} and unconditionally stability.

"A 5.2-GHz Direct Conversion Receiver 90-nm CMOS"

UCLA, ECE Dept., EE 215C Analysis and Design of RF Circuits and Systems (Instructor: Professor Behzad Razavi) *Jan.2022 – Mar.2022*

- Design the direct conversion receiver with LNA, I/Q mixer, oscillator and frequency-division circuit on TSMC 90nm CMOS PDK.
- Simulate the receiver's performance (NF, IIP_3, input/output resistance, LO phase noise and gain) and make adjustments on building blocks to meet the specific requirements and limitations.
- Tune the receiver and realize the performance of 30-dB Gain, 3.5-dB NF, -10dBm IIP3 and -110-dBc/Hz LO phase noise.

"A 28-GHz Heterodyne Receiver in 40-nm CMOS"

HKUST, ECE Dept., ECE 5280 High Frequency Integrated Circuits Design (Instructor: Professor Patrick Yue) *Mar.2021 – May.2021*

- Implemented the receiver building blocks in Cadence including 2-stage LNA, I/Q mixer and VGA on TSMC 40nm CMOS PDK.
- Assembled the receiver and verified its performance (input impedance, bandwidth, gain, NF, S11, IIP_3, power consumption and EVM) by the Cadence-ADS-MATLAB co-simulation platform provided by the lab.

Achieved the performance of 50-ohm input resistance, 500-MHz bandwidth, 29-dB Gain, -14-dB S11, 5.9-dB NF, -14.1dBm IIP_3 and 60-mW Power Consumption and 10% EVM.

"A Continuous-Time Low-Pass Filter for UHF RFID Applications"

HKUST, ECE Dept., ECE 5040 Advanced Analog IC Analysis and Design (Instructor: Professor Howard Luong) *Sep.2020 – Dec.2020*

- Designed a low power 80-dB two-stage op-amp with 92-dB voltage gain, 60-degree phase margin, 600MHz unity-gain frequency and 1.38mW power consumption.
- Implemented a continuous-time filter based on the op-amp for UHF RFID applications. The whole circuit consists of 3 parts: a gain stage, negative feedback to emulate the source resistance, and the Chebyshev type I filter stage.
- Verified the result using Hspice, Cadence and MATLAB. Satisfied the performance requirement of 10 – 20dB passband gain, 0.1-dB passband ripple, 50dBc adjacent channel attenuation and 77KHz upper -3dB frequency.