

Polar Cube

Senior Project Technical Reference Manual

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Abstract

The Polar Cube project is a multidisciplinary effort to develop 3U CubeSat form factor satellite that has the capability to passively sense atmospheric noise temperature for climate modeling. The project as a whole is being developed as a collaborative effort between the Colorado Space Grant Consortium, the Center for Environmental Technology Lab run by Professor Albin Gasiewski, and a capstone team of electrical engineers.

The overall goal of the capstone team was to design a microwave temperature sensing payload that meets the physical and communication interface specifications of the ALL-STAR CubeSat bus. The radiometer payload measures temperature by scanning the Earth for microwave noise at and around the diatomic oxygen resonant frequency of 118 GHz via a set of selective channels. These channels are down mixed to an intermediate frequency and then sampled and transmitted to a ground base station for processing. This data is ultimately used to map temperature as a function of elevation for climate modeling and weather prediction.

Purpose

The purpose of the Polar Cube project is to develop a highly accurate, compact atmospheric temperature sensing satellite as a pathfinder for launching a fleet of relatively low cost satellites. A fleet of such satellites would revolutionize climate modeling, both in terms of latency and spatial resolution. This satellite will also be able to identify polar ice/sea boundaries to accurately characterize polar ice retreat.

As the amount of greenhouse gasses in the atmosphere increase, global warming will become more severe. It is very important to be able to characterize the effect this will have on Earth's climate and model weather on a global scale. A fleet of cheap, compact and accurate orbital temperature sensors will enable a scale of modeling that has never before been possible.

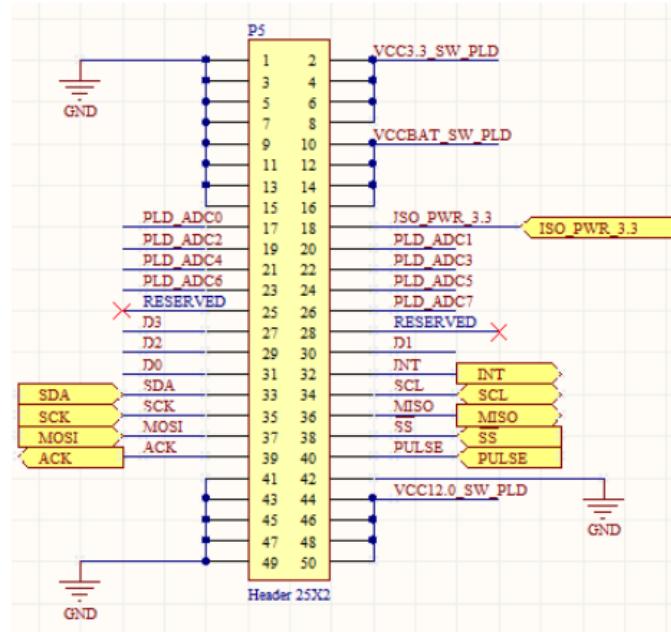
Overview

ALL-STAR Bus

ALL-STAR is a compact satellite bus that was designed to 3U CubeSat specifications. This bus is currently being designed and developed by students at the Colorado Space Grant Consortium (COSGC) as a partnership with Lockheed Martin Space Systems Corporation. The

ALL-STAR bus is capable of supporting a 1-year life cycle, and each bus is designed to operate completely independently of other satellites (handles its own management, downlink, etc.).

The capabilities offered to the payload by the ALL-STAR bus include a power supply (5 Watt nominal supply) and line of sight data downlink to base station (250 kbps with a goal of 1 Mbps). Since the ALL-STAR bus is highly compact, any payload must be less than 16.50 cm long, 1277 cm³ in volume, and 2000 g of mass. The electrical interface to the ALL-STAR bus is through a Samtec LS2-125-01-S-D connector, and the primary bus communication protocol is SPI.



Polar Cube Radiometer Payload

The Polar Cube hardware is designed to interface with an ALL-STAR bus to support the collection of atmospheric temperature data. The payload is designed to passively measure emissions at the 118 GHz diatomic oxygen resonance from atmospheric oxygen on the Earth. The payload passively receives these emissions and uses these emissions to make temperature data measurements.

The system is divided into three subsystems: Radio Frequency (RF) Chain, Intermediate Frequency (IF) System, and Digital Board.

The microwave signal will first be received by the radio frequency system. By passing through the rexolite lens and reflecting on the reflector plate, the signal is transmitted into the RF system. The function of the RF system is mainly down mixing the original of the signal

frequency, and also it still has to keep the signal power level high enough for the IF system power detection requirements. The output signal should have a frequency of about 59GHz and a power level of about -12dBm.

The output of the RF system will be passed into the IF system. By first dividing the frequency into two bands with a diplexer, lower from 0.1GHz to 1.3GHz and higher from 1.3GHz to 6.5GHz, the signal will be further split into eight distinct frequency channels with eight different filters. Based on the weighting function, each specific frequency channel with a unique weighted temperature corresponds to a function of altitude. To make sure there is enough power to be passed into the digital system behind the IF system, the power level has to be approximated -23dBm to transmit into the tunnel diode, so that it will function of square law. After RC circuit, the output signal of the tunnel diode will be converted to a range of 0-5V DC voltage and sent to the digital system.

The output data of the IF system is handled by the Digital system. Two 24 bit analog-to-digital converters (ADCs) present on the Digital PCB sample voltage at the output of the IF system, as well as voltage produced by the thermistors. The IF system output represents the noise temperature data collected by the entire RF chain and IF systems, and the thermistor data is used to calibrate the system to allow noise temperature data to be converted to atmospheric temperature data in post-processing on the ground.

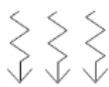
Samples are collected from the ADCs by the microprocessor on the payload's digital PCB. The processor stores, averages, and formats the data for transmission to the ALL-STAR Command and Data Handling (CDH) system.

The digital system will also control power for future iterations of the payload. Switching and linear regulators can be powered on and off via General Purpose Input/Output (GPIO) of the microprocessor. Various components of the payload can be powered on and off as needed to meet the power constraints of the ALL-STAR bus.

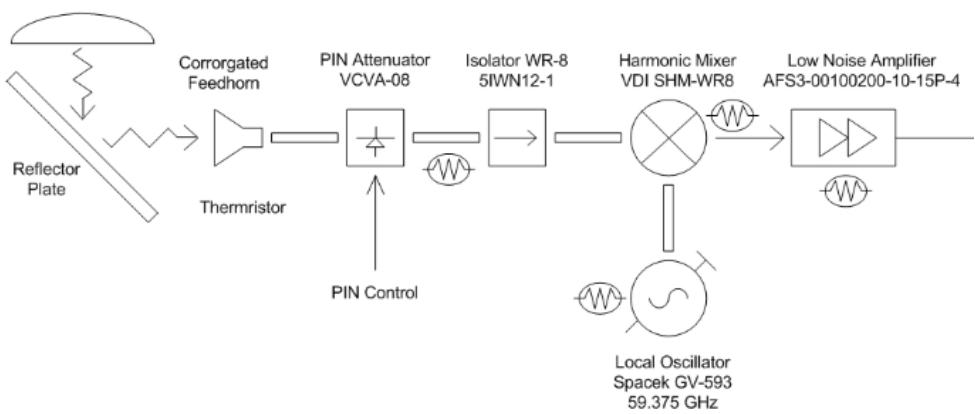
System Description

RF Front End

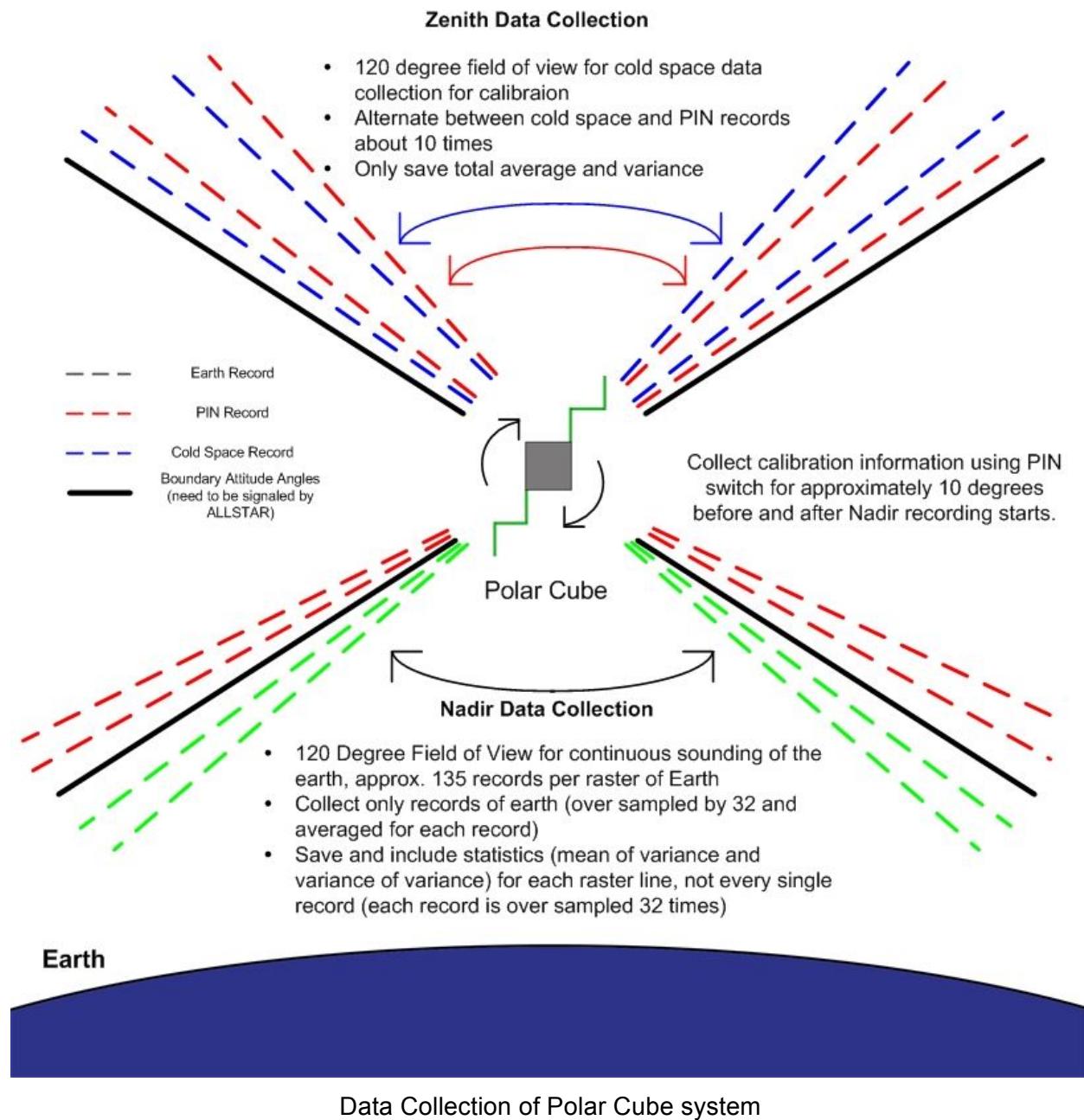
~ 150K to 310k



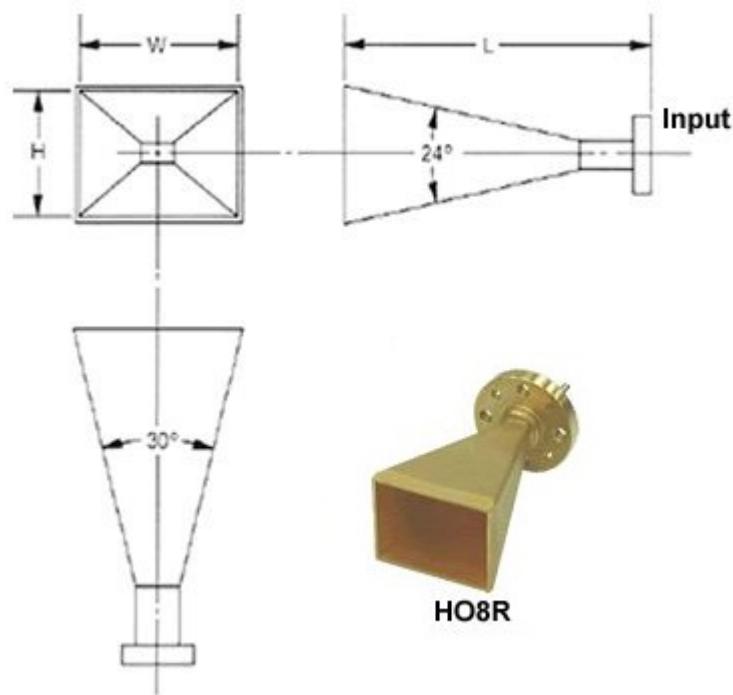
Rexolite Lens
Diameter 8 cm
Radius of Curvature = 7.0 cm
F# 1.245



Feedhorn and Radiation Collection



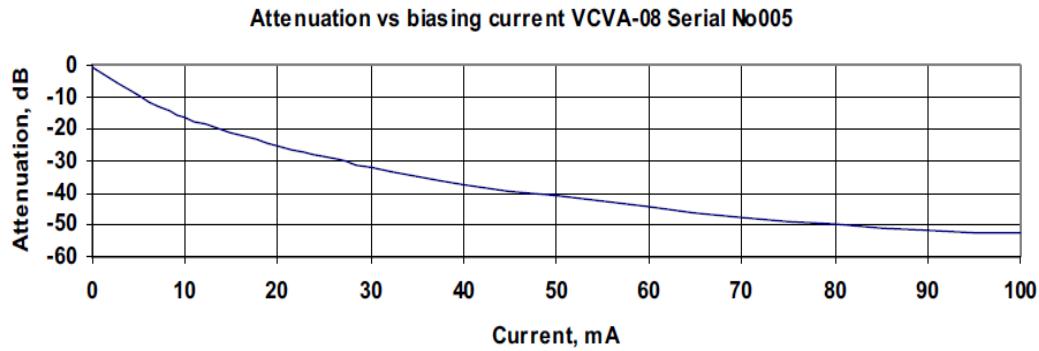
Radiated microwave emissions are focused by a lens and reflected off a reflector plate into the feedhorn. While the satellite is facing between the limbs of the earth it will be sampling data. While pointed away from the earth at cold space the satellite will gather two types of calibration data. The first is noise temperature of the system, which will be acquired by driving the PIN attenuator which will remove background radiation meaning all sampled data will be from noise produced within the payload system. The second calibration data is cold space temperature, which is a known temperature that the earth's emissions are compared with to in order to determine brightness temperature of the earth.



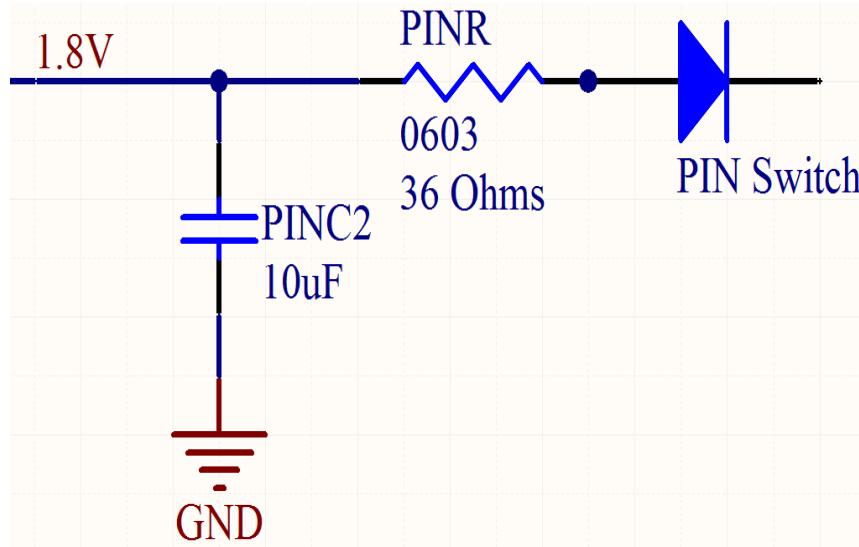
Mechanical Diagram of HO8R Feedhorn

PIN Switch

A pin switch functions as a variable attenuator. Its attenuation is can be determined by the forward current as shown in the following figure provided in its manufacturer's datasheet.



The PIN diode has a voltage drop of ~0.7V when forward biased. A driving current of approximately 30 mA was chosen in order to provides approximately 30 dB of attenuation. To drive the PIN switch, a 1.8V supply was connected to it through a series resistor of 36 ohms to provide 30.6 mA when the supply is enabled by the processor.

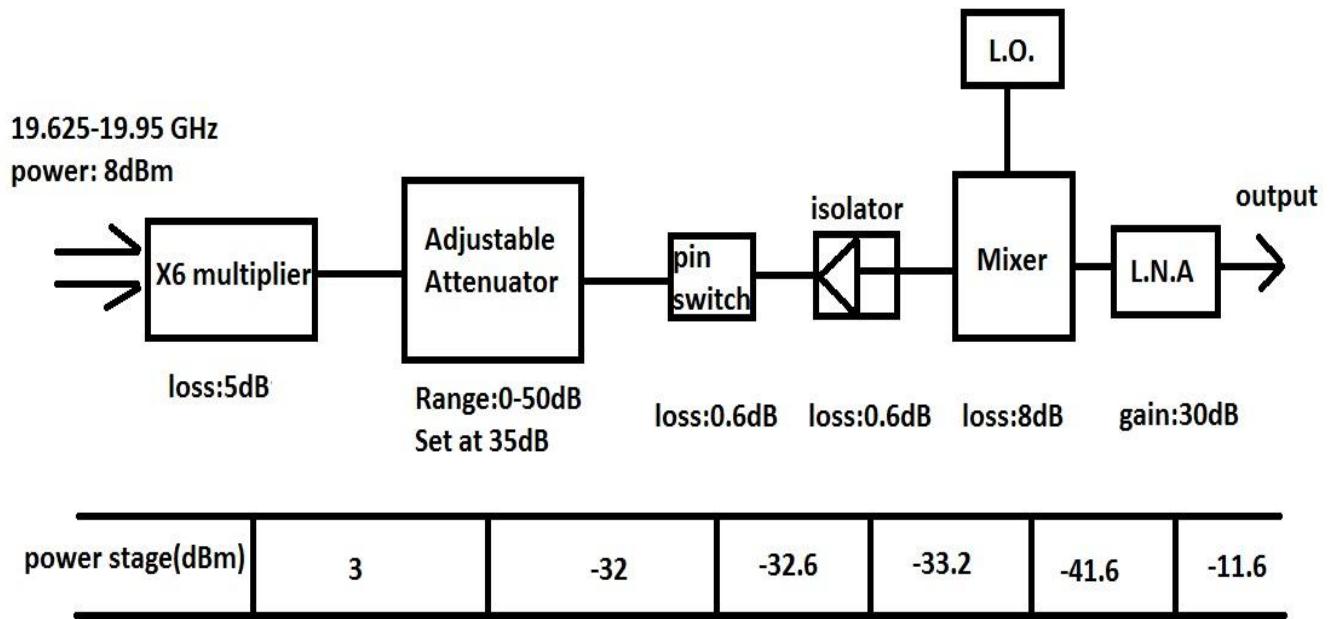


Down mixing

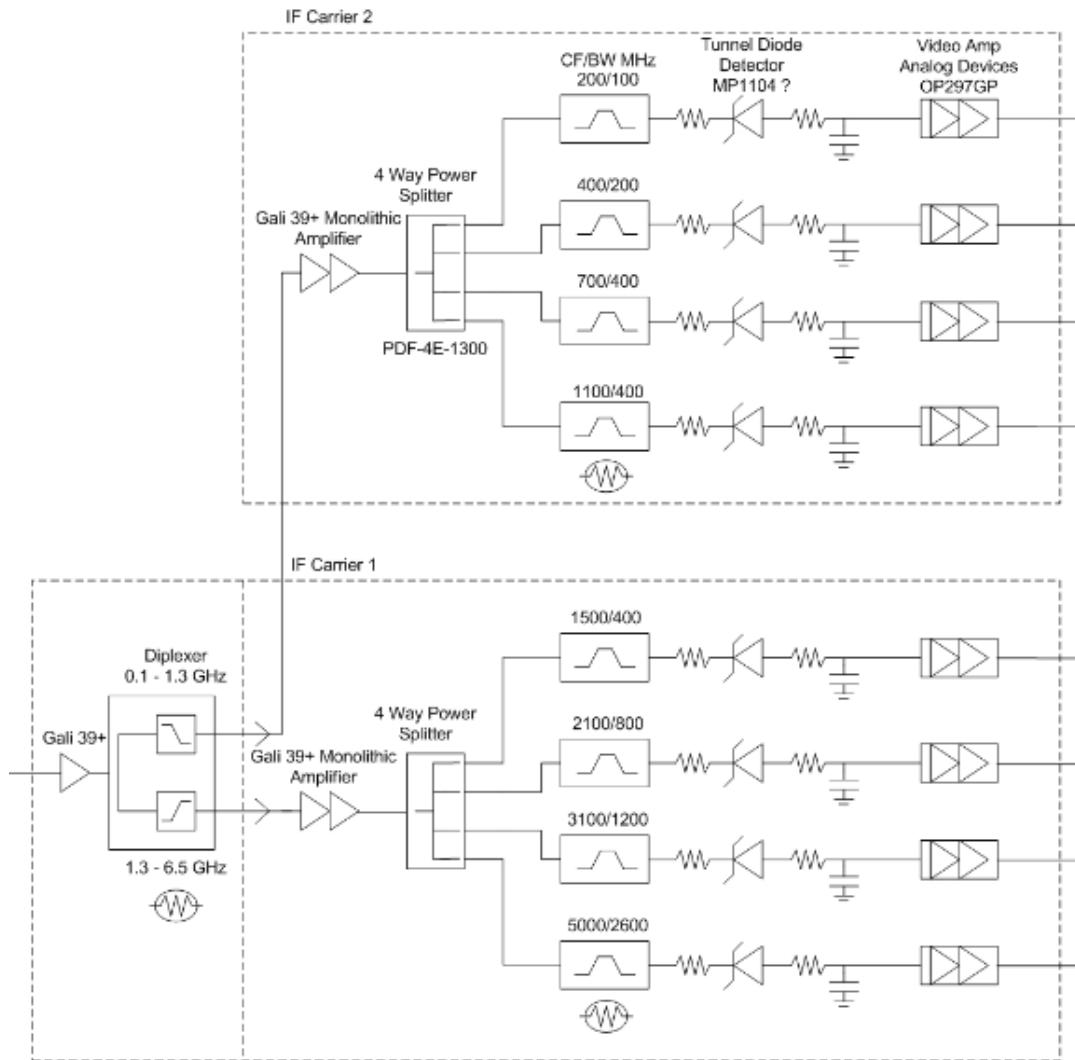
By using the SHM-WR8 mixer combined with the GV-593 S/N 1L08 Gunn local oscillator, the frequency of the signal can be shifting down to half of its original frequency, which is approximated 59.35GHz. The purpose of this signal down mixing is to make the signal usable by components that are not designed to work at radio frequencies such as splitters, amplifiers and ADCs.

Amplification

The purpose of the low noise amplifier (LNA) is for the power detection in the Intermediate Frequency system after the RF chain. As the signal passing through all the components before, the signal power has been lost about 10dBm, so to compensate this power loss and also satisfy the detected power requirement in the IF system later on, the system is designed to use the AFS3-00100600-25-LN amplifier, and its performance at the frequency about 59GHz is approximated 30dB gain. The output signal of the RF chain will be passed into the IF system.



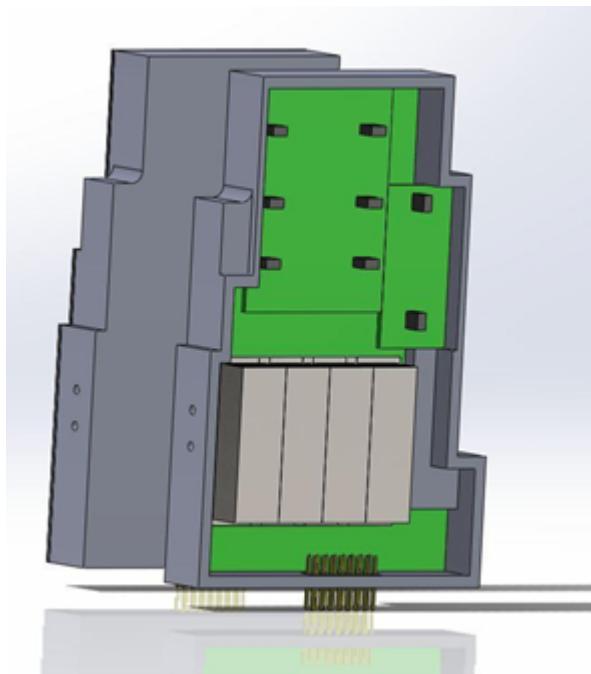
Intermediate Frequency System



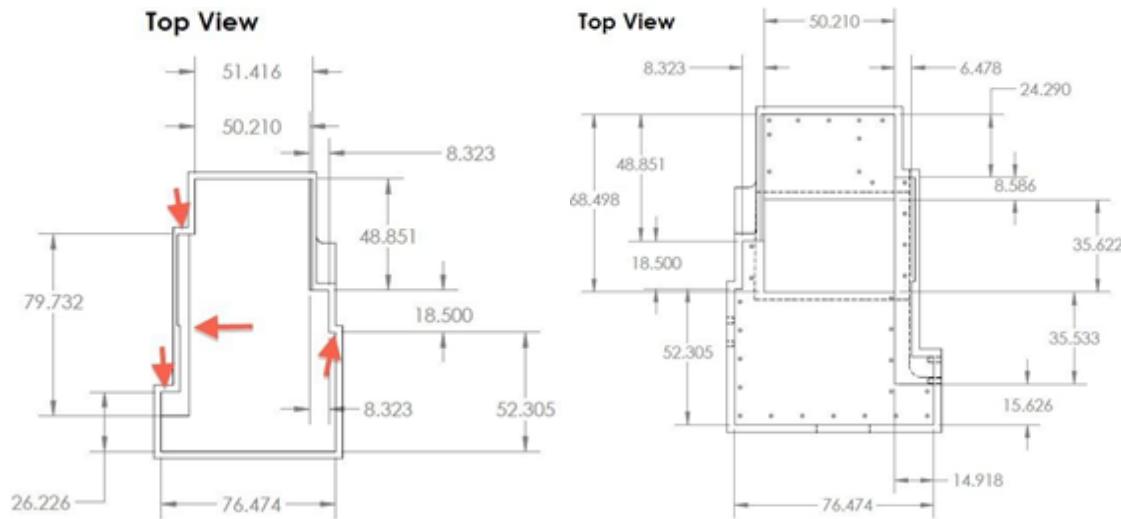
Block diagram of intermediate frequency system

After the down mixing processing, the frequency of the signal has been shifted from the original 118.75GHz down to half of it which is 59.38GHz. Treating this signal as the input wave, the IF system will highly amplify, filter and split it to eight distinct frequency channels by using a diplexer, two power splitters, amplifier-attenuator pad, and eight filters; and the power level of each channel is detect through a tunnel diode. After a RC circuit and amplification again, the signal will be converted to DC signal in the range from 0 to 5V, and finally it will be passed on to the digital sampling system.

Mechanical design



One of the advantages of Polar Cube project is its small size, so the physical constraints become a challenging issue. The figure below shows the mechanical drawings of both IF carriers. Carrier 1, shown on the right, has an extra cavity which will hold the diplexer system. The reason for this design that the higher frequency filters have a smaller footprint size than the lower frequency filters, so there is some extra room in this carrier for the diplexer.



IF Carrier Mechanical Drawings

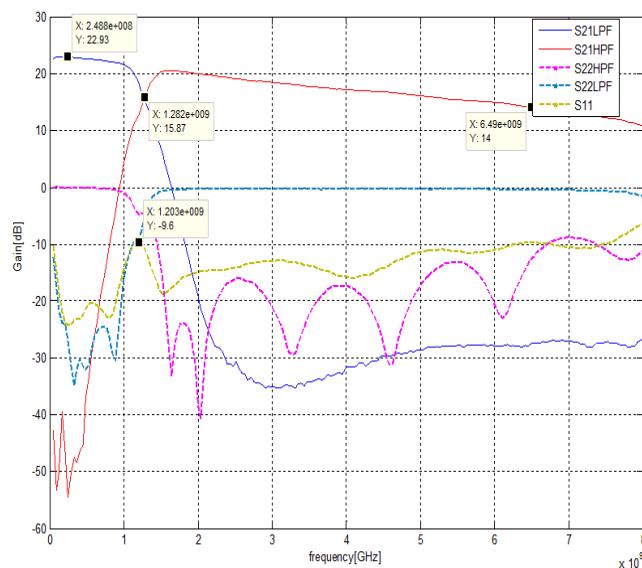
IF System Function Decomposition

Diplexer

The diplexer is the first component in the IF system that the signal will pass, its main function is splitting the signal into two frequency bands, they will be passed into different carriers. The LPF is 0.1GHz-1.3GHz, the HPF is 1.3GHz-6.5GHz. Additionally, it has been tested the S-parameter output by adding a one-stage Gali39+ amplifier before the input of the Diplexer system, which shows a perfect performance.



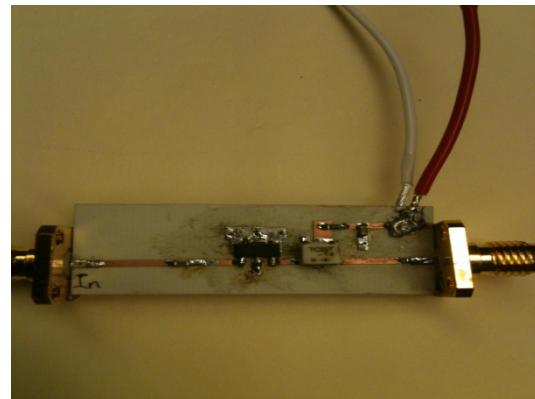
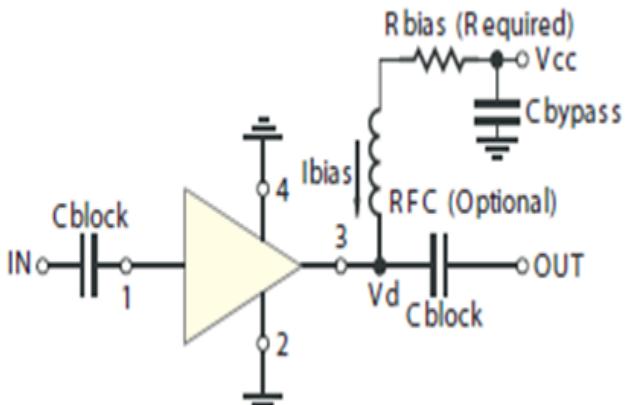
One-Stage Gali39+ & Diplexer



S-Parameter: One-stage Gali39+ & Diplexer

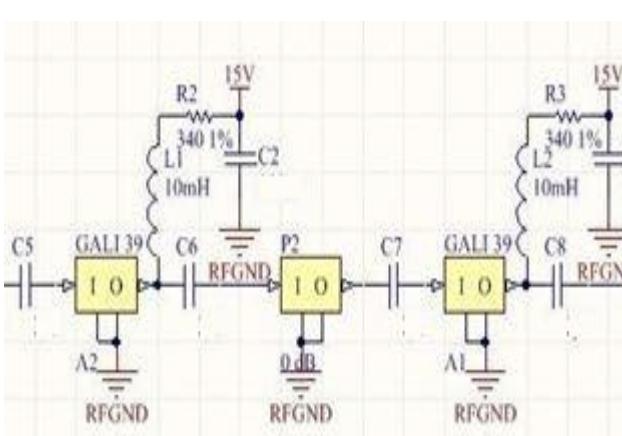
Amplification

The purpose of IF amplifier is to make sure the power of the signal will be large enough to drive the tunnel diode to perform the square law function, which needs a -23dBm(5uW) signal power. It can be treated the Gali39+ amplifier combining with TCBC Bias Tee, which includes a RC circuit and a inductor, as one-stage amplifier pad. The operation voltage for both components is +15V, and to make sure we have a stable supply power, the RC circuit is necessary. For the capacitor in the DC bias path, using $C=0.1\mu F$. For the Cblock ones, using $C=2400nF$. For the resistor in the DC bias circuit, using $R=340\text{ohms}$ (15V dc).The performance of this pad is providing gain of average 20dB depending on the frequency of the signal.

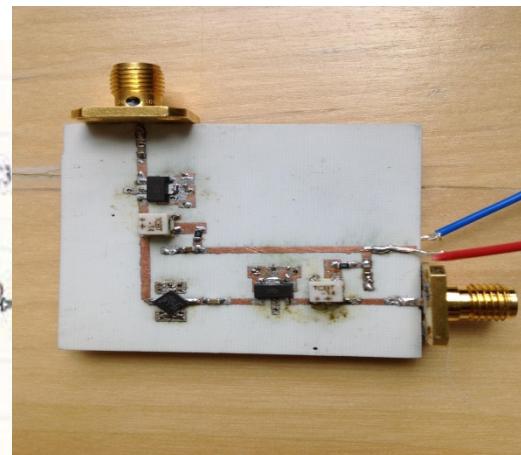


Prototype PCB

For two or more amplification stage, the GAT-0+ attenuator with loss of 3dB will assist with isolation of the signals between each two Gali39+ amplifiers. Also, forcing to achieve -23dBm power before passing into the tunnel diode, each channel might also need another attenuator to assist the power level at the detection stage.



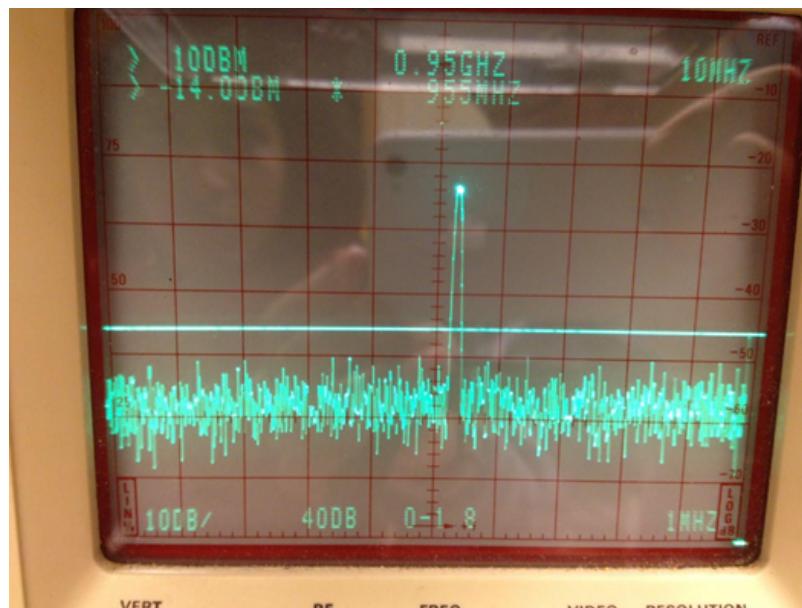
Schematic



Prototype PCB

Oscillation problem:

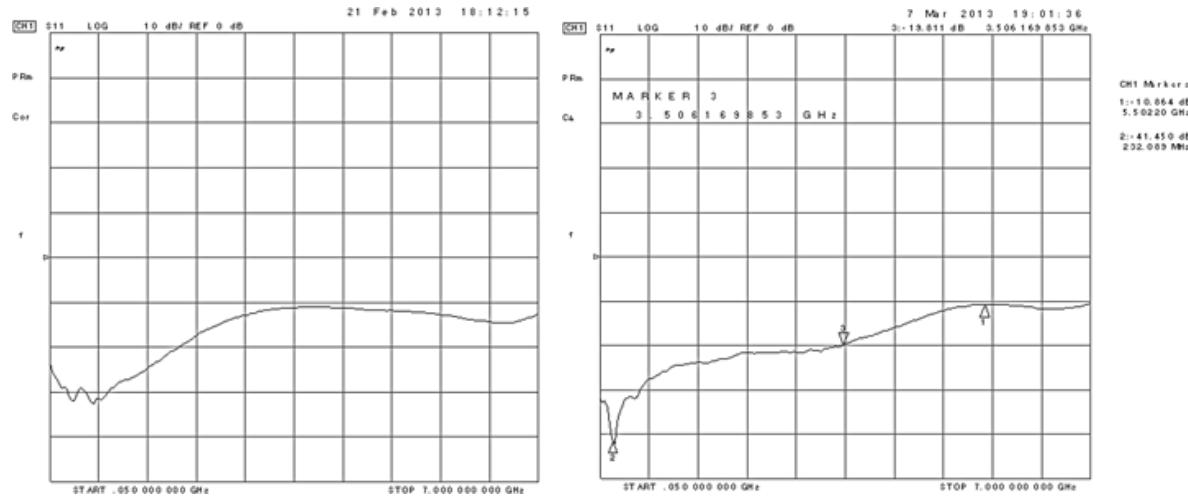
One of the big issues that happened during the project was the oscillation problem, which shows in the image below. The screen shows the S11 parameter of a three-stage amplifier pad without any input signal, the spark shows there is an oscillation issue at frequency 0.95GHz.



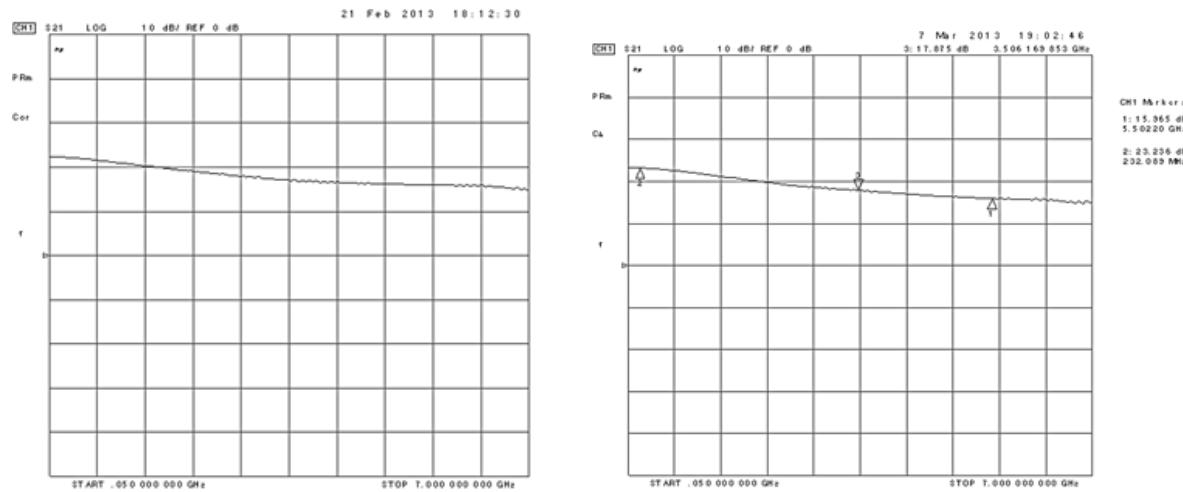
S11 parameter screenshot with no input signal of three-stage amplifier pad

However, after we double check with the data sheet of the Gali39+ amplifier and the TCBC Bias Tee, we found the problem is that the designer did not follow the parameters on the sheets, such as the number of vias around the Gali39+, the width of the trace, etc. The new performance of a one-stage amplifier pad is showing below, we list the comparison among the S11 and S21 performances of our design and the Minicircuits Test Board.

S11: Minicircuit T.B (-15dBm input)/ours (-20dBm input) [in order]



S21: Minicircuit T.B (-15dBm input)/ours (-20dBm input)/Data-sheet [in order]



Conclusion: without following the parameter correctly from the data sheet, the impedance of the trace does not match up with the requirements of the Gali amplifier system, which should be 50ohms; therefore, the waves have been reflected a lot which causes the oscillation problem.

Power division (two types of divider)

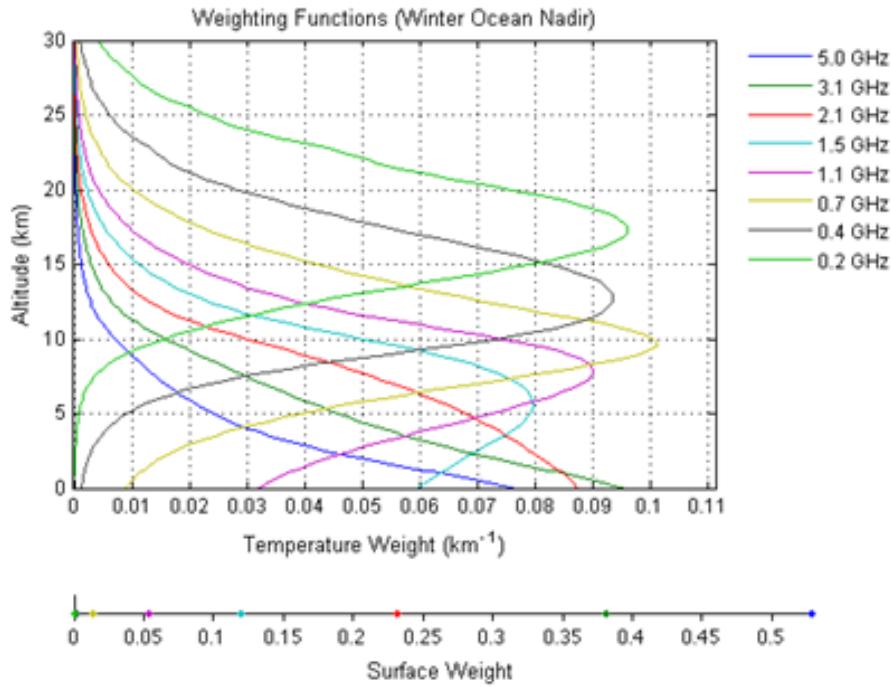
In the two carries, the input signal power levels of all eight channels have to be even. To achieve this, two types of power divider have been implemented. For the lower band four channels carrier, range from 0.1GHz-1.3GHz, it is used the 4-way power splitter PDG-4E to divide the signal power into four equal power signals. For the higher band four channels carrier, range from 1.3GHz-6.5GHz. Concerning of the physical restraint, and also the technical restraint in the market, it is determined to use three 2-ways power dividers to performance a 4-way divider function. The signal will first be divide into a lower band and a higher band first by using P2D100800. Then they will be passed into other two power divider TCP233X+ and GP2X1+ respectively. Finally, the function will be just as the same as a normal 4-way divider which divides the signal power into four equal signals without changing the frequency.

Filtering

There are eight distinct filters, every four of them placed in one carrier. The values of their central frequency and bandwidth are in the following table.

Carrier 2		Carrier 1	
Center Frequency [MHz]	Bandwidth [MHz]	Center Frequency [MHz]	Bandwidth [MHz]
200	100	1500	400
400	200	2100	800
700	400	3100	1200
1100	400	5000	2600

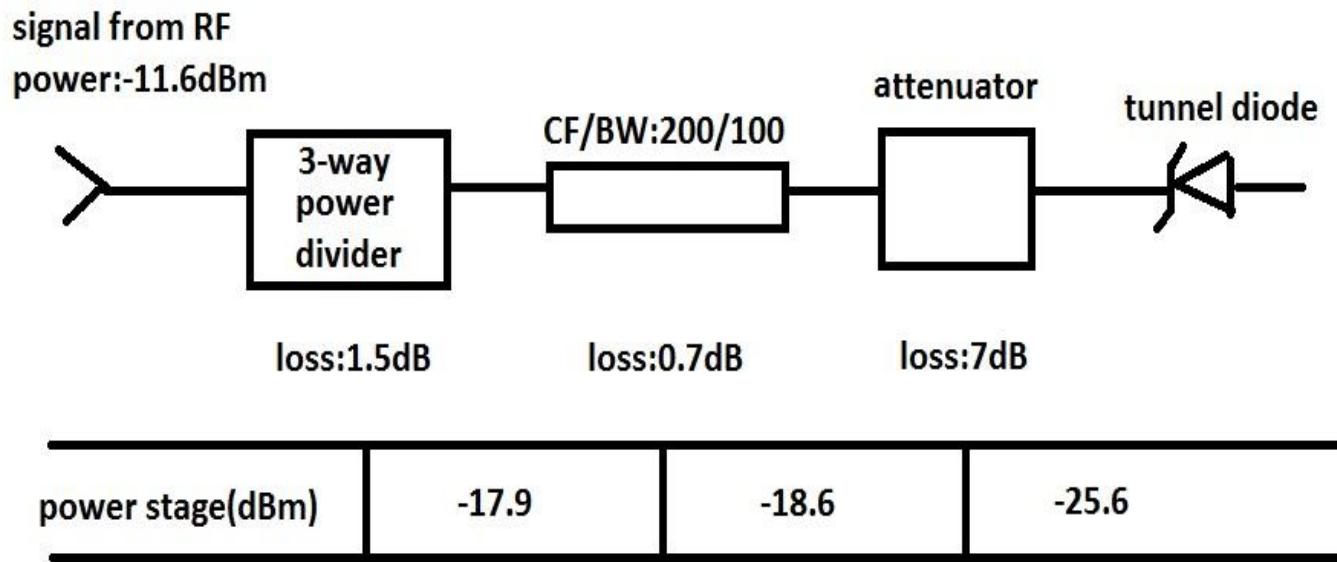
Each channel has a corresponding weighting function which gives that channel's weight on atmospheric temperature as a function of altitude. By using MRT simulation software, the theoretical weighting function of each channel's center frequency is shown below. By using the weighting function, the weight of a given channel can be determined based on any given altitude.



Detection by tunnel diode

Signal detection is the main goal in the IF system, and the tunnel diode plays the leading role in the detection mission. By using tunnel diode MP1104, the detection input signal power has to be close to -23dBm (5uW). The test one can tell whether the diode functions well is by measuring the input and output voltage, and if the output voltage is as twice as much as the input voltage, then it shows the input signal of the tunnel diode satisfies the approximated -23dBm driven power requirements, and this is the square law of the tunnel diode. The purpose of this power detection is to make sure there is enough power of the noise temperature presenting for the later data processing.

Power stage diagram before tunnel diode (lowest channel):



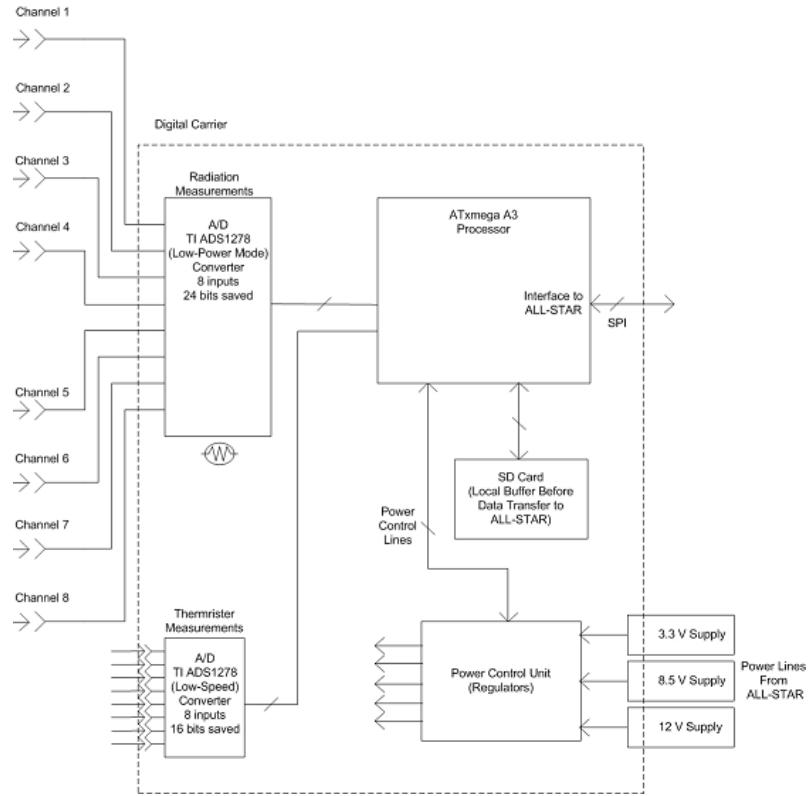
Output signal of IF system

The IF system has a main goal which is dividing the original signal into eight different frequency channel, and then by a low pass filter in each channel, the signal will be converted to a DC signal in the range of 0-5V in different frequency depending on the channels; hence, the digital signal system behind the IF will be able to sampling the data.

Digital System

The digital system consists of the ATxmega128A3 processor, two ADS1278 ADCs, one 6.5 V V78-1000-SMT switching regulator and associated components, one MAX766 -15V switching regulator, and one ADP1613 regulator configured for +15V operation. One required feature for future iterations of this payload, which is not currently implemented is a micro SD card for data storage before transmission to the ALL-STAR CDH.

The general layout of these components and their interactions with each other is seen in the following block diagram.



Data Collection

The IF-sampling ADS1278 is configured to provide data for each channel serially through its SPI-compatible output. The ADS chips are also currently designed to sample within a voltage range of 0V - 5V, and connect to the IF boards through single ended connectors (due to current video board designs). Given the timing constraints required to collect and average 8 channels of data quickly enough out of the one ADC, data for each channel is sampled at 429 samples per second (calculations for which can be found in the Mission Parameters appendix). Per the datasheet for the ADS1278, this allows the use of low power mode for sampling.\

The thermistor-sampling ADS1278 is configured similarly to the IF system, but is used in low-speed mode due to the relatively slower rate at which thermistor values change.

Both ADCs sampling input clocks are signaled with a small 27 MHz crystal oscillator on board the Digital PCB.

The ADS1278 is an SPI-compatible device, but is not fully SPI compliant. The ADS1278 lacks a Slave Select pin, and therefore must use dedicated lines to connect to the processor. As a result the SPI between the microprocessor and the ADC utilizes only the Master Input, Slave Output (MISO) and Serial Clock (SCLK).

Several non-SPI connections are made to each ADC as well. The DRDY pin is pulled low by the ADC when data is available. After a new acquisition has been made per the configured speed of the ADC, the DRDY pin is pulsed high to indicate that new samples have been collected, after which the DRDY pin is again held low. The processor is timed to collect data before these pulses arrive, as data will be lost or corrupted if it is being collected during the time where new samples have been acquired. The SYNC pin is used to synchronize ADCs. When pulsed low the ADCs stop their conversion process until their digital filters are reset and SYNC is brought high again. During normal sampling the SYNC pin is held high to allow conversion of samples.

The particular connections required for each ADC to configure the mode and data format can be found in the appendices.

Thermistor Measurements

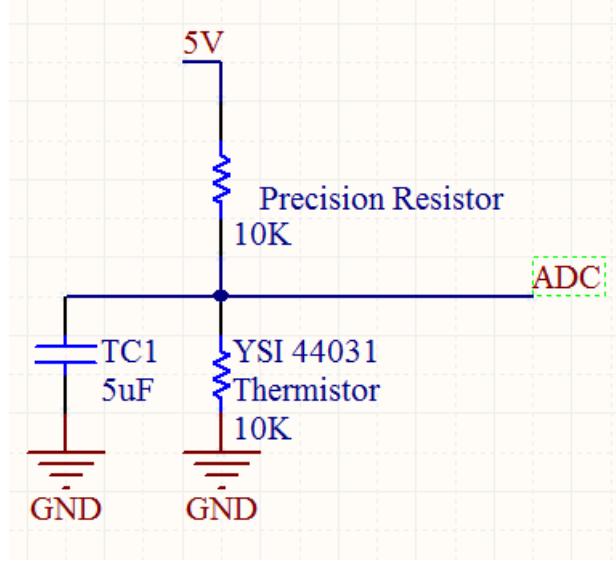
In order to accurately process the sampled temperature noise data for atmospheric temperature, knowing the temperature of the radiometer is paramount. The temperature of the sensor itself will eventually add an offset to the sampled values, so it is important to be able to determine the temperature of critical components of the payload to within ~0.1K accuracy so that sampled data can be adjusted to within that amount of the actual measured temperature.

^[1]The YSI 44031 follows a non-linear, inverse temperature to resistance relationship and has the following characteristics:

$$R_{ref} = 10 \text{ k}\Omega \text{ (@ } T_{ref} = 298.15 \text{ K)}$$

$$\beta = 3574 \text{ K (@ 273-323K)}$$

The following schematic shows the voltage divider circuit used to determine the resistance of the thermistor.



The voltage, V_{therm} , measured by the ADC can be determined through a simple voltage divider in which the resistance of the thermistor is the variable of importance. From V_{therm} , the resistance of the thermistor can be solved for, and the resistance of the thermistor can be used to accurately determine the temperature of the critical points of the payload:

$$R_{therm} = R_{ref} e^{\beta \left(\frac{1}{T_{therm}} - \frac{1}{T_{ref}} \right)} \quad [1]$$

$$T_{therm} = \frac{T_{ref} \beta}{\beta + T_{ref} \ln \frac{R_{therm}}{R_{ref}}} \quad [1]$$

$$T_{therm} = \frac{T_{ref} \beta}{\beta + T_{ref} \ln \frac{V_{therm}}{V_{ref} - V_{therm}}} \quad [1]$$

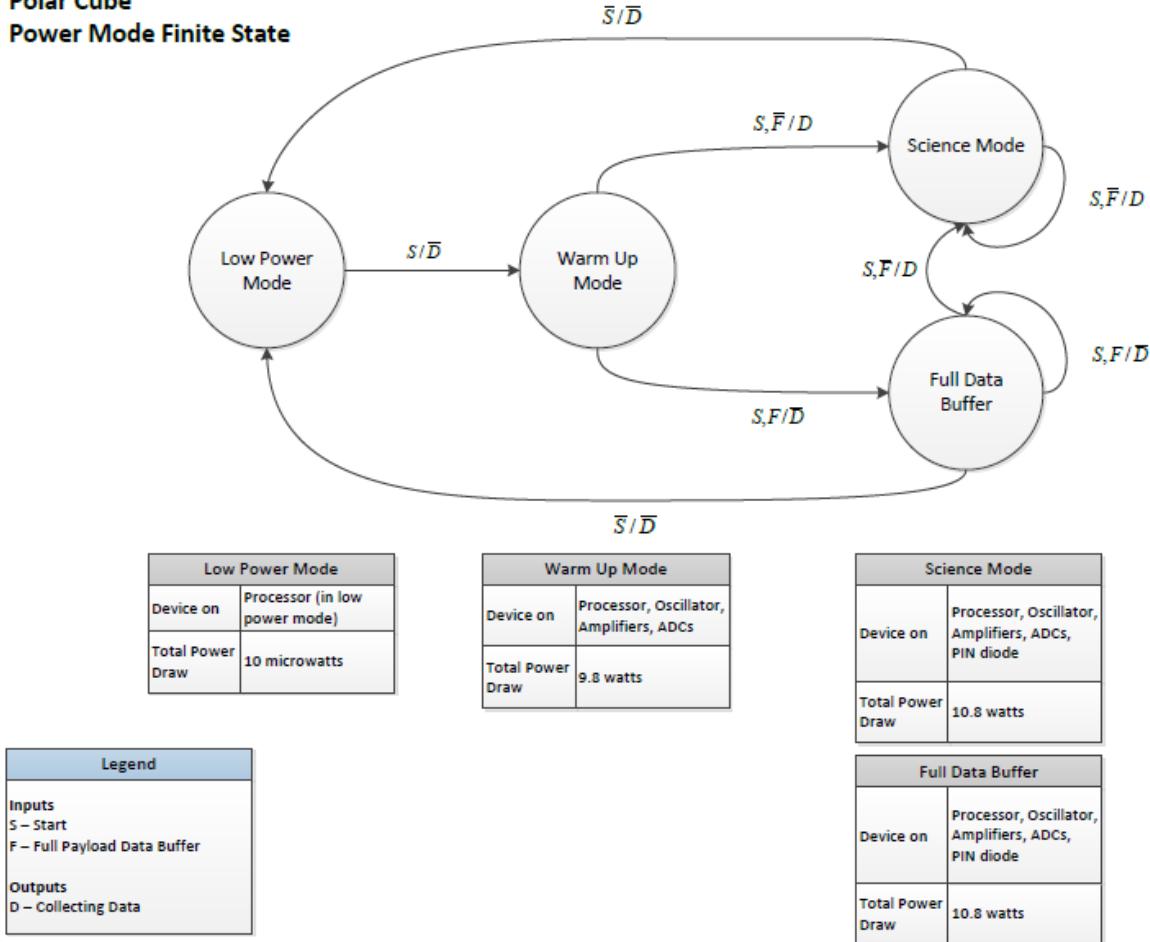
Power Management

Since the ALL-STAR bus provides a power supply of 5W nominally to the payload and power is generally a scarce commodity on satellites, power management is important to ensure correct functionality of the system. A summary of the power draws of all components is shown below.

Component	Number of Components	Power Draw All Components (mW)
ADS1278 ADC (Low-Power)	2	496
ATxmega128A3-AU Processor	1	59.4
SD Card (S25FL Series from Spansion, 100mA for Erase)	1	52.8
Oscillator	1	4875
Thermistor Biases	8	10
PIN Attenuator Driver (Power Draw During -60dB Attenuation)	1	500
IFLNA	1	1950
Gali 39+ Amplifier Bias Losses	4	1666
Gali 39+ Amplifiers	4	434
Video Amplifiers	16	264
Total Power Draw (W)		10.3072

The Gunn Oscillator consumes the majority of power at approximately 4.9 W. In order to keep average power draw below 5 W the payload must be able to enter states of varying levels of reduced power draw at the request of the CDH system. The modes of operation and the events required to change modes are shown in the finite state machine below.

Polar Cube Power Mode Finite State



Data collection duty cycles can be controlled by the CDH system so they are flexible and dynamic regardless of unexpected changes in power draw throughout the mission.

A Dielectric Resonator Oscillator (DRO) is under consideration as a replacement for the Gunn Oscillator due to its substantially lower power requirements. The DRO being considered requires 3.2 W nominally and would reduce the total power draw of the payload in science mode to approximately 8.6 W.

Power Supplies

The ALL-STAR bus provides regulated 12V and 3.3V supply lines to the payload. In addition to these lines, a 15V line is required by amplifiers in the IF system, a -15V line for the video amplifiers, and a 6.5V line was needed to supply the local oscillator. On the digital side, a 5V line was needed to supply AVDD on the ADCs, along with 1.8V for DVDD of the ADCs (1.8V was also used to drive the PIN attenuator switch). Switching converters were used to generate

most of the supply voltages, but linear regulators were used for the ADCs due to their relatively lower switching ripple and smaller footprint.

To regulate the different supplies to switch between operational modes, the enable/shutdown pin of each supply driven by GPIO lines from the ATXmega128A3 microprocessor.

Appendices

Datasheets

RF Chain Components

Feedhorn

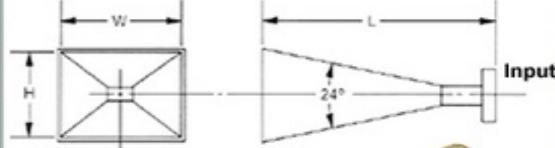
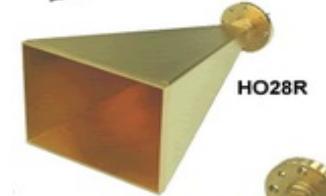
   

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Custom Microwave, Inc. - Catalog

Select Part Type: Horns - Rectangular

Select Part: HO8R

Part	Ports
Catalog #: HO8R	Description: Input Waveguide: WR8 Flange: Round - 0.750
Dimensions	Data Gain & Radiation Pattern
All dimensions in inches Height - H: .591 Length - L: 1.560 Width - W: .775	Optional Features Flanges: If your flange requirements differ from those listed, that may be specified when ordering at an additional cost.
RF Parameters	
VSWR (Max.): 1.1:1	
Ordering Information	
To order please send email to Sales and indicate the part #s and quantities desired.	
General Part Information	Part Description
    	These are our standard 24 dB conical horns. Gain Curves and Radiation Patterns are available under the details for each catalog horn. We can modify the standard horns to other values ranging from 5 through 26 dB. Ordering Example: HO28S is a rectangular Horn in WR28 with a Square flange.

[\[Site Map\]](#)

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Pin switch



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Phone: +371-7-065100
Fax: +371-7-065102
Mm-wave Division in St.Petersburg, Russia
Phone: +7-812-326-59-24
Fax: +7-812-326-10-60

CERTIFICATE

Voltage Controlled Variable Attenuator



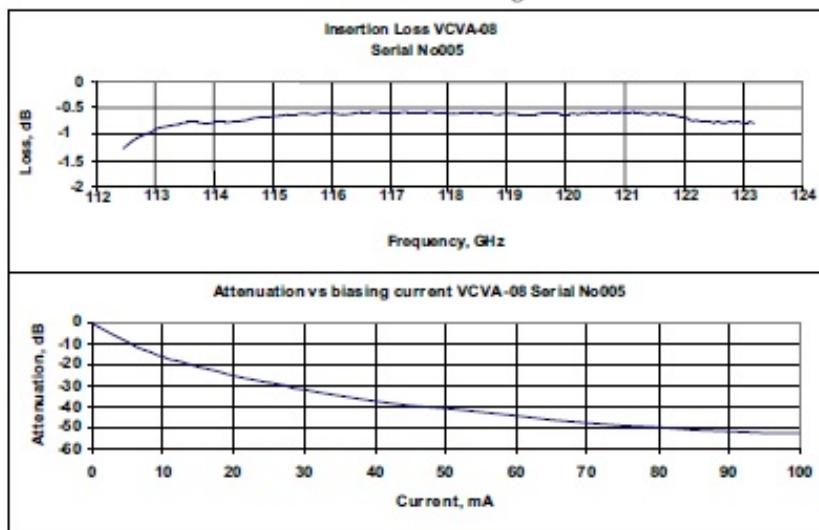
Part No. VCVA-08

Serial No 005

Specifications.

Frequency Band and Range, 113-123 GHz
Insertion loss dB: 1
Isolation dB (min): 50
Power Handling (peak): 1.0
Switching time msec: 50
DC max mA: 100
Flanges: UG-387/U-M

Data of measuring



Scheme of control voltage feeding of VCVA attenuator:



Mixer



SHM-WR8 Receiver Testing NOAA PO - 40RANR1N1763

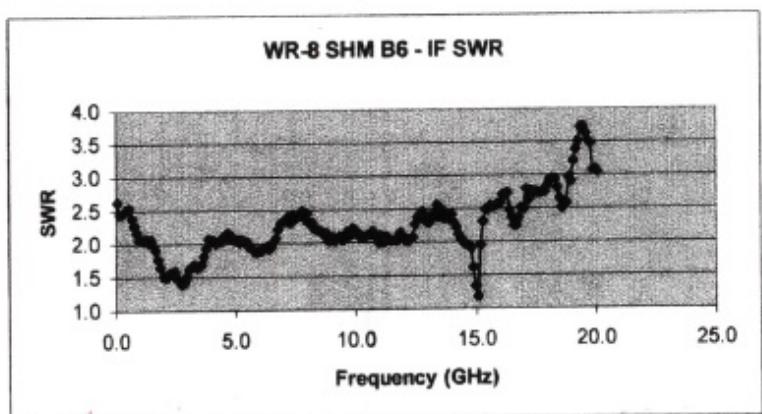
LO Source
NOAA Gunn - 59 GHz

TEST DATA:

Date	Freq	T95	T254	T424	Tm	Lm	Lm	SWR	Gam	Tmc	Lmc	Lmc	Comments
	(GHz)	(K)	(K)	(K)	(K)	(lin)	(dB)			(lin)	(dB)		
1/20/2002	118	790	1230	1700	527.3	2.8	4.4	1.7	0.26	473	2.6	4.1	1.8 GHz Amp, IF 20jan02b
2/20/2002	118	720											1.8 GHz Amp

Verified Oscillator Frequency --> Freq_LO = 59.4 GHz
Measured NOAA Miteq Amp --> TIF = 100 K = 1.3 dB

Date Freq T100 Comments
2/20/2002 118 780 NOAA Amp



1.8 GHz IF Amplifier		
L	T	NF
32	95	1.23
44	254	
47	424	
Tcirc = 290		

Notes:

T## is the system noise temperature for IF chain of ## degrees
Tm and Lm are the least-squares fit to T95, T254 and T424

Local oscillator



THE DIELECTRIC RESONATOR OSCILLATOR
A HIGHLY STABLE CLASS
OF MICROWAVE SIGNAL SOURCES



DRO-1000
Free Running DRO

FEATURES

- DIELECTRIC RESONATOR
- INTERNAL VOLTAGE REGULATOR
- 150 MHz BAND WIDTH
- LOW PHASE NOISE
- MIC FABRICATION
- LOW MICROPHONICS
- LOW POWER CONSUMPTION
- UP TO +25dBm OUTPUT POWER
- AVAILABLE FROM 1 -50GHz
- OPERATING RANGE -55° TO +105°C

APPLICATION

- SATELLITE COMMUNICATIONS
- CABLE TV LINKS (CATV)
- LOCAL AREA NETWORKS (LAN)
- GLOBAL POSITIONING SYSTEMS (GPS)
- TEST EQUIPMENT
- UP / DOWN CONVERTERS
- LMDS
- TRANSMITTER & RECEIVERS
- DIGITAL RADIOS
- MISSILE GUIDANCE
- POINT TO POINT
- MILITARY, SPACE, COMMERCIAL

DESCRIPTION

DRO-1000 series Dielectric Resonator Oscillator (DRO) utilizes state-of-the-art MIC to provide a highly stable, reliable and efficient signal source at microwave frequencies up to 50 GHz. The low profile and rugged construction provide excellent durability against harsh environmental conditions.

DRO-1000 series oscillator is designed using FET or BJT amplifier with series feedback at source and Dielectric Resonator at the gate. High gain, low-noise FETs/BJTs are biased positively or negatively at the gate to ensure minimum phase-noise. The device is carefully matched for maximum power, minimum phase-noise and Voltage Standing Wave Ratio (VSWR). The oscillator is matched for maximum temperature stability and optimum negative resistance.

DRO-1000 series oscillator is buffered by cascaded low-noise driver and power amplifiers for minimum load pulling, maximum isolation and power. FET/BJT devices are directly attached to gold plated Kovar carriers to minimize heat effect and maximize heat sinking. Kovar carriers are mounted to the chassis to provide an efficient thermal junction and a stable structure for reduction of microphonics. To ensure oscillator stability over the full temperature range, high-Q low dielectric constant resonators are chosen with proper temperature coefficient to compensate for frequency drift. Where extreme stability is required, a miniature heater can be provided to ensure constant temperature and minimum drift.

DRO-1000 series provide several advantages over other microwave signal sources, such as Gunn Cavity Oscillators and Crystal Multiplier Chains. Table 1 offers a brief summary comparison of the other sources.

DRO-1000 series is internally voltage regulated to avoid reverse bias, frequency pushing, bias modulation and voltage transients. Mechanical frequency adjustment is provided for desired frequency setting with in the bandwidth.

CHARACTERISTIC	CRYSTAL MULTIPLIER CHAIN	GUNN CAVITY OSCILLATOR	DRO-1000 SERIES
Reliability	GOOD	FAIR	EXCELLENT
Efficiency	LOW	LOW	HIGH
Temperature Range	GOOD	POOR	EXCELLENT
Power Variation	HIGH	HIGH	LOW
FM Noise	VERY GOOD	EXCELLENT	EXCELLENT
Frequency Stability	EXCELLENT	GOOD	VERY GOOD
Environmental Stability	FAIR	FAIR	EXCELLENT
Size	LARGE	MEDIUM	SMALL

Table 1

DRO-1000 Rev. 5/10

SPECIFICATION

Model Number	DRO-1000-XX.XX (Where XX.XX is freq.in GHz)
Single Frequency	1.00 to 50.00 GHz
Mechanical Tuning Range	100 MHz
Electrical Tuning	Optional
Power Output	+13 dBm, up to +25 dBm Optional
Load VSWR, Maximum	2.0 :1.0
Power Requirements	+15, +12, +10VDC, 90mA
Power Variation	+/-0.5dBm
Pushing	2 ppm/V Max.
Pulling (12 dB Return Loss)	+/- 90 ppm Max.
Frequency Stability	4 ppm / °C
Phase Noise	See Phase Noise Envelope (Fig.A)
Spurious	-85 dBc
Harmonics	-25 dBc
Operating Temperature	-55° to +105°C Optional; 0° to 50° Standard
Storage Temperature	-55° to +125°C
Connectors	SMA Female
Size	2.25" x .93" x .67"
Finish	Nickel

PHASE NOISE ENVELOPE

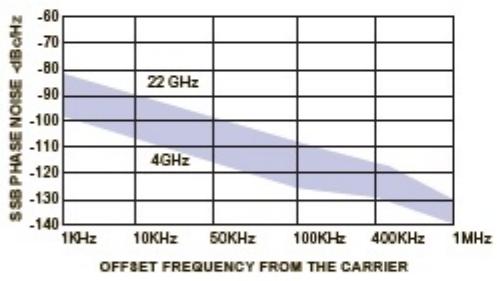
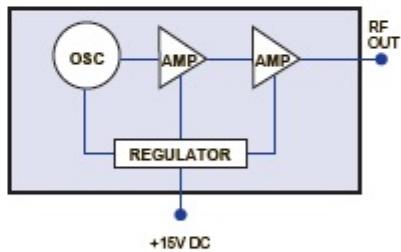


FIGURE A

BLOCK DIAGRAM



OUTLINE DRAWING



MICROWAVE DYNAMICS, 16541 Scientific Way, Irvine, CA 92618 PHONE: 949-679-7788 FAX: 949-679-7748

Web Page : <http://www.microwave-dynamics.com> * Email: info@microwave-dynamics.com

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SPECIFICATIONS ARE SUBJECT TO CHANGE WITHOUT NOTICE

LNA



 MITEQ PROJECT No: PI

PROJECT No: PI 25311

MODEL No: AES3-00100200-10-15P-4

SERIAL No: 952952

CUSTOMER: MASC FINANCIAL MANAGEMENT DIV

P.O. No.: RA133003SU0302

100 Davids Drive, Hauppauge, NY 11788

卷之三

TEL: (631) 436-7400

AA (631) 436-7430
www.milton.com

IMPORTANT - **MUST USE HEAT SINK IF CASE TEMPERATURE EXCEEDS 70°C**

SPECIFICATIONS AT +23°C:					
FREQUENCY:	.10	to 2.00	GHz	OUTPUT POWER @1dB GAIN COMPRESSION	+15
MIN. GAIN:	38		dB	VOLTAGE:	+15
MAX.GAIN FLATNESS:	+/- 1.0		dB	MEASURED CURRENT:	130
MAX. VSWR INPUT:	3.0		:1	MAX. NOISE FIGURE:	1.0
MAX. VSWR OUTPUT:	2.0		:1	HOUSING NO:	112158(546)

NOTE: TEST DATA TAKEN WITH CASE TEMP. OF +23° C

COMMENTS :-

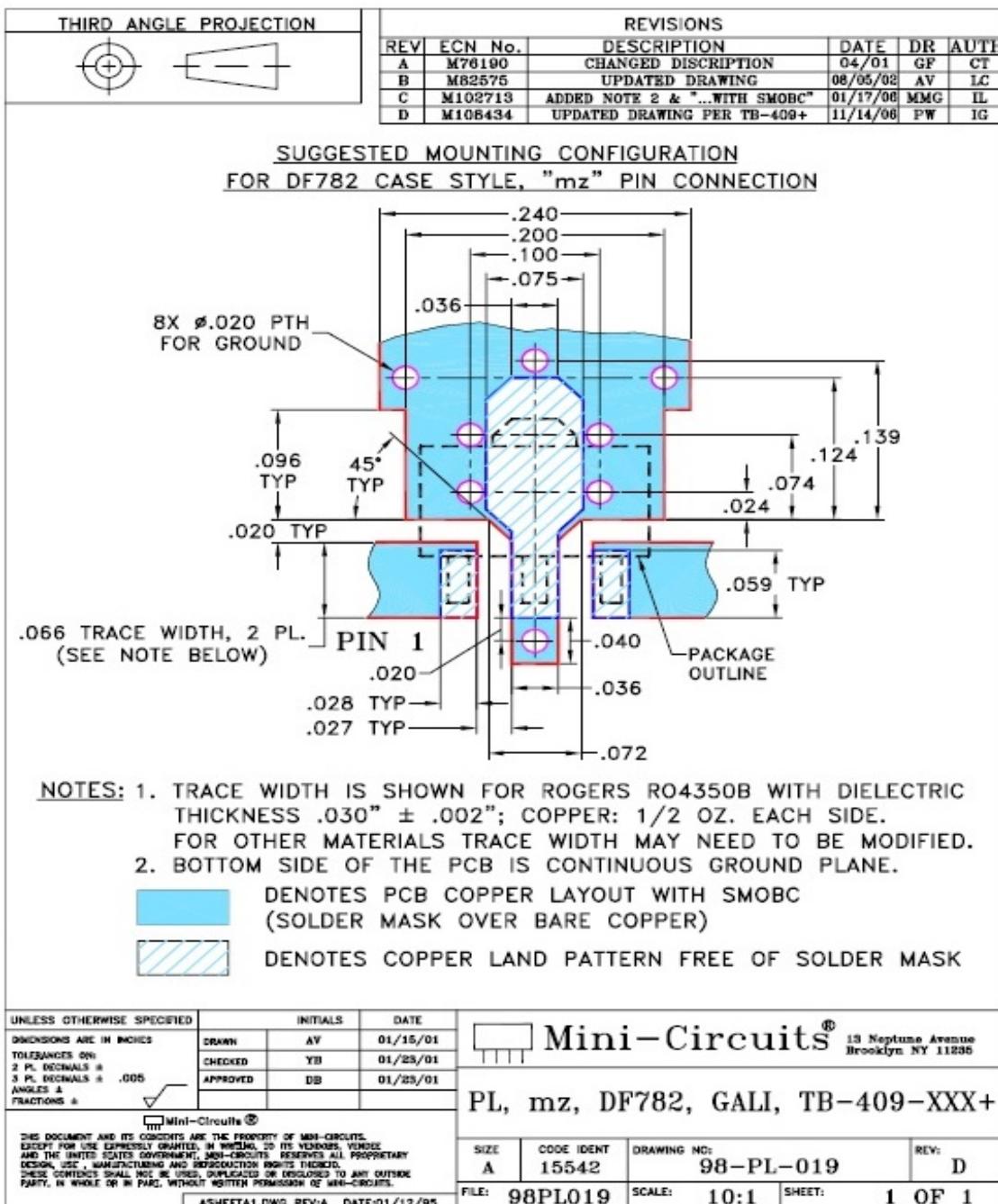
TESTED BY:

J. Schwinn
(J. SCHWINN)

DATE: 07/22/03

IF System Components Datasheet

Gali39+ amplifier



Attenuator (3dB loss)

Miniature Plastic Fixed Attenuator

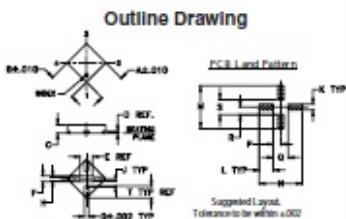
50Ω 0.5W 0dB DC to 8000 MHz

Maximum Ratings

Operating Temperature -45°C to 85°C
Storage Temperature -55°C to 100°C
Permanent damage may occur if any of these limits are exceeded.

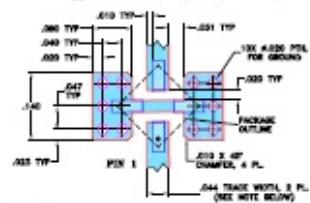
Pin Connections

INPUT	1
OUTPUT	3
GROUND	2,4



Outline Dimensions (inch)									
A	B	C	D	E	F	G	H	J	K
0.118	0.118	0.036	0.008	0.07	0.024	0.017	0.018	0.021	0.024
3.00	3.00	0.09	0.20	1.76	0.61	0.43	0.46	0.53	0.61
K	L	M	N	P	Q	R	S	T	wL
0.024	0.001	0.196	0.196	0.032	0.064	0.032	0.064	0.05	0.001
0.61	1.56	4.72	4.72	0.81	1.63	0.81	1.63	1.27	0.02

Demo Board MCL P/N: TB-154 Suggested PCB Layout (PL-126)



NOTES:
1. TRACE WIDTH IS SHOWN FOR ROGERS RO4300B WITH ELECTROLYTIC THICKNESS (.007 ± .0005); COPPER 1/2 OZ. TIN-LEAD Solder. For other materials, dimensions may need to be modified.
2. BOTTOM SIDE OF THE PCB IS A CONTINUOUS GROUND PLANE.
3. DENOTES PCB COPPER LAYOUT WITH TM90C (SOLDER MASK OVER BARE COPPER).
4. DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK.

Features

- miniature package MCL™ 3x3 mm
- specified to 8000 MHz, useable to 10000 MHz
- excellent VSWR, 1:15:1 typ.

Applications

- cellular
- PCS
- communications
- radar
- defense

GAT-0+



CASE STYLE: FG873

PRICE: \$2.35 ea. QTY (10-49)

+ RoHS compliant in accordance with EU Directive (2002/95/EC)

The "S" suffix has been added to model to identify RoHS Compliance. See our web site for RoHS Compliance methodology and qualifications.

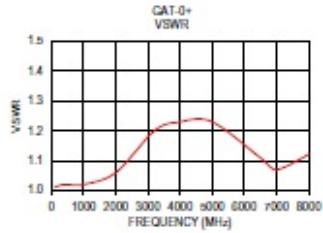
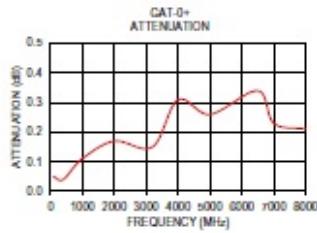
Electrical Specifications at 25°C

FREQ. RANGE (MHz)	ATTENUATION (dB) Flatness			VSWR (: λ)			MAX. INPUT POWER ¹ (W)			
	DC-1 Nom.	1-5 GHz Typ.	5-8 GHz Typ.	DC-1 Typ.	1-5 GHz Max.	5-8 GHz Max.				
DC-8000	0±0.2	0.1	0.2	0.2	1.05	1.2	1.15	1.35	1.25	0.5

1. RF power at 25°C case temperature: \leq 1Watt. Derate linearly to 0.2 Watt at 60°C.
2. Flatness: variation over band divided by 2

Typical Performance Data

Frequency (MHz)	Attenuation (dB)	VSWR (: λ)
100.00	0.05	1.01
400.00	0.04	1.02
1000.00	0.11	1.03
2000.00	0.17	1.06
3000.00	0.15	1.20
4000.00	0.31	1.23
5000.00	0.26	1.23
6500.00	0.34	1.11
7000.00	0.29	1.07
8000.00	0.21	1.12



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IPRF MICROWAVE COMPONENTS

For detailed performance specs & shopping online see web site

REV C
M108294
CAT-0+
ED-0450
090812

P.O. Box 350166, Brooklyn, New York 11235-0003 (718) 334-4500 Fax (718) 332-4601 The Design Engineers Search Engine Provides ACTUAL Data Instantly at minicircuits.com

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First stage power divider

2-WAY POWER DIVIDER
SURFACE MOUNT MODEL: P2D100800

WIDE BANDWIDTH **1000 - 8000 MHz**

FEATURES:

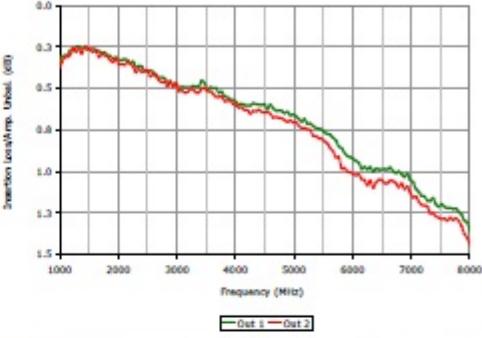
- ▶ Excellent Performance
- ▶ Wide Bandwidth
- ▶ Small Size, Surface Mount
- ▶ Moderate Power
- ▶ Lead Free RoHS Compliant

APPLICATIONS:

- ▶ Signal Splitting & Low Power Combining



RoHS Compliant

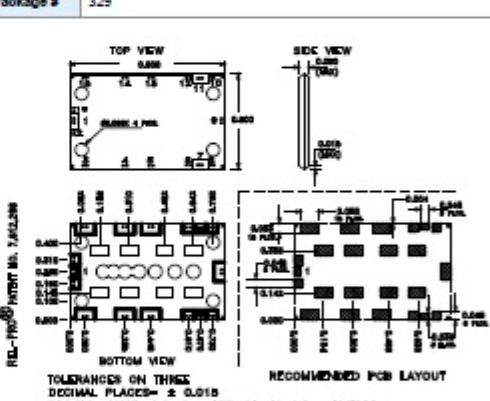


SPECIFICATIONS (Rev. D 12/01/11)

Frequency	1000 - 8000 MHz		
Insertion Loss (dB) *	Freq. (MHz)	Typ.	Max.
	1000-4000	0.5	0.8
Isolation (dB)	Freq. (MHz)	Typ.	Min.
	1000-8000	25	15
Phase Unbalance	Freq. (MHz)	Typ.	Max.
	1000-4000	0.3	2°
Amplitude Unbalance (dB)	Freq. (MHz)	Typ.	Max.
	1000-4000	0.05	0.2
4000-8000	0.1	0.3	
Input Power **	2 Watt (Max.)		
VSWR	1.2:1 (Typ.)		
Impedance	50 Ohms (Nom.)		
Operating Temperature Range	-40 to +85 °C		
Storage Temperature Range	-55 to +100 °C		

* Above 3.0 dB theoretical split loss.
** Handling power applies to splitter mode and assumes ideal 50 Ohms impedance matching on all ports.

Package # 329



RECOMMENDED PCB LAYOUT

PORT CONFIGURATION		
Input	Output	Ground
1	7,11	All Other

Second stage lower frequency divider

Surface Mount Power Splitter/Combiner

2 Way-0° 50Ω 1000 to 3000 MHz

Maximum Ratings

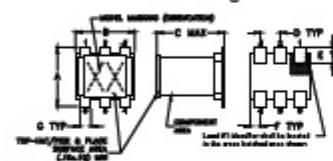
Operating Temperature	-40°C to 85°C
Storage Temperature	-55°C to 100°C
Power Input (as a splitter)	0.5W max.

Permanent damage may occur if any of these limits are exceeded.

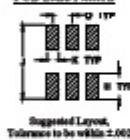
Pin Connections

SUM PORT	2,5,6
PORT 1	3
PORT 2	4
GROUND	1
EXT. RESISTOR 200Ω	3,4

Outline Drawing



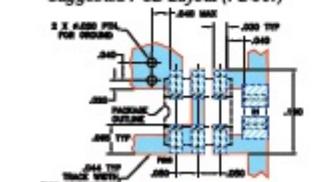
PCB Layout Patterns



Outline Dimensions (Inch)

A	B	C	D	E	F
.160	.150	.160	.060	.040	.025
4.06	3.61	4.06	1.27	1.02	0.64
G	H	J	K	wt.	
.026	.065	.190	.030	grams	
0.71	1.65	4.83	0.78		0.15

Demo Board MCL P/N: TB-464+ Suggested PCB Layout (PL-357)



NOTES: 1. TRACE WIDTH IS 0.005" FOR ROGERS RO4003 WITH 0.005" THICKNESS. 2. 0.005" COPPER 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE ADJUSTED. 3. BOTTOM SIDE OF PCB IS CONTINUOUS GROUND PLANE. 4. MINIMUM FOR COPPER LAYOUT WIDTH 0.005" (0.0125MM). 5. MINIMUM COPPER LAYER PATTERN FREE OF SOLID MARK.

P.O. Box 350165, Brooklyn, New York 11235-0003 (718) 934-4500 Fax (718) 332-4991 The Design Engineers Search Engine Provide ACTUAL Data Instantly at minicircuits.com

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TCP-2-33X+



CASE STYLE: DB1627
PRICE: \$1.99 ea. QTY. (20)

+RoHS Compliant

The +Suffix identifies RoHS Compliance. See our web site for RoHS Compliance methodologies and qualifications



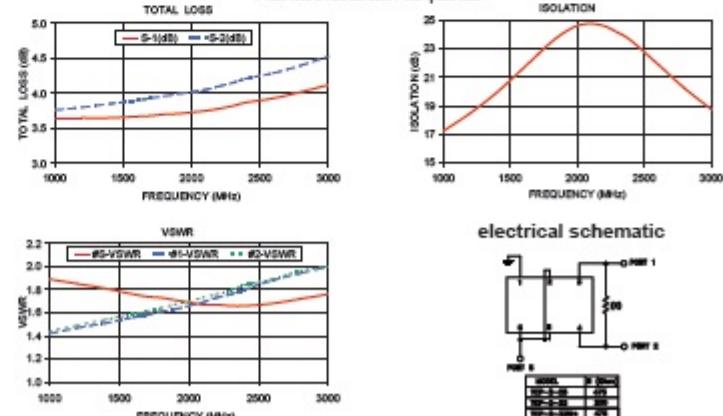
Electrical Specifications

FREQ. RANGE (MHz)	ISOLATION (dB)		INSERTION LOSS (dB) ABOVE 3.0 dB		PHASE UNBALANCE (Degrees)	AMPLITUDE UNBALANCE (dB)
	L-1	Typ. Min	Typ.	Max.		
1000-3000	18	15	0.6	1.9	5.0	0.9

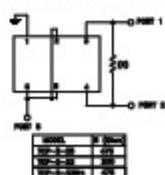
Typical Performance Data

Frequency (MHz)	Total Loss ¹ (dB)		Amplitude Unbalance (dB)	Isolation (dB)	Phase Unbalance (deg.)	VSWR 8	VSWR 1	VSWR 2
	S-1	S-2						
1000.00	3.65	3.75	0.11	17.21	0.35	1.99	1.42	1.44
1200.00	3.65	3.80	0.15	18.45	0.37	1.85	1.47	1.49
1400.00	3.65	3.85	0.20	19.93	0.41	1.81	1.51	1.54
1600.00	3.67	3.90	0.23	21.66	0.50	1.75	1.55	1.59
1700.00	3.68	3.93	0.25	22.55	0.53	1.74	1.59	1.61
1800.00	3.70	3.96	0.26	23.43	0.59	1.73	1.61	1.64
1900.00	3.71	3.99	0.28	24.14	0.65	1.71	1.63	1.67
2000.00	3.73	4.02	0.29	24.63	0.74	1.69	1.68	1.70
2100.00	3.75	4.05	0.30	24.76	0.82	1.67	1.69	1.73
2200.00	3.79	4.10	0.31	24.62	0.91	1.67	1.73	1.76
2300.00	3.82	4.15	0.32	24.17	0.97	1.66	1.76	1.79
2400.00	3.87	4.21	0.34	23.60	1.16	1.66	1.80	1.84
2500.00	3.93	4.29	0.35	21.94	1.27	1.69	1.89	1.93
2600.00	4.02	4.40	0.36	20.24	1.45	1.72	1.94	1.98
2800.00	4.12	4.53	0.41	16.75	1.73	1.76	2.00	2.00

1. Total Loss = Insertion Loss + 3dB splitter loss.



electrical schematic



REV. A
M12428
TCP-2-33X+
ID-1715
DRAFT V1.0
12/21/09

Second stage higher frequency divider

Surface Mount Power Splitter/Combiner

2 Way-0° 50Ω 2800 to 7200 MHz

Maximum Ratings

Operating Temperature	-40°C to 85°C
Storage Temperature	-65°C to 150°C
Power Input (as a splitter)	1.5W max.
Internal Dissipation	0.75W max.
Permanent damage may occur if any of these limits are exceeded.	

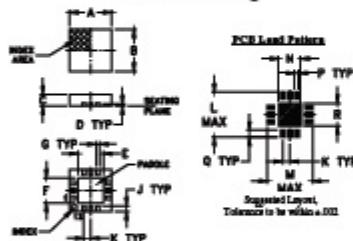
Pad Connections

SUM PCRT	2
PORT 1	7
PORT 2	9
GROUND	1,3,4,5,6,8,10,11,12, paddle

Product Marking



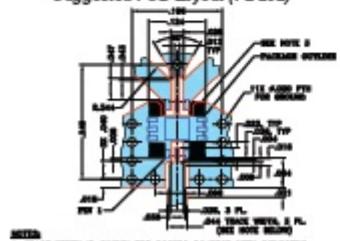
Outline Drawing



Outline Dimensions (Inch)

A	B	C	D	E	F	G	H	J
.118	.118	.095	.005	.057	.057	.009	—	.096
3.00	3.00	0.89	0.28	1.45	1.45	0.23	—	0.41
K	L	M	N	P	Q	R	wt	
.020	.127	.127	.049	.010	.020	.049	grams	
0.51	3.23	3.23	1.24	0.25	0.51	1.24		0.02

Demo Board MCL PN: TB-453-GP2X1+ Suggested PCB Layout (PL-282)



NOTES:
1. TRACE WIDTH IS SHOWN FOR ROBOTS READING WITH SELECTIVE THICKNESS (.007" & .0015") COPPER 1/2 OZ. EACH SIDE. FOR OTHER AUTOMATION THE TRACE THICKNESS MAY HAVE TO BE REDUCED.
2. SAW TUNING TRACES ARE NOT ALLOWED ON THIS SIDE OF THE BOARD.
3. SIGNAL TRACES ARE NOT ALLOWED ON THIS SIDE OF THE BOARD.
4. APPROVAL OF DESIGN AND SAW TUNING IS REQUIRED.
5. CENTER FOR COMMERCIAL LAYER NEEDS BASIC COUPLER MASK OVER BASE COPPER.
6. MONITOR COPPER LAYER PATTERN FREE OF SOLDER MASK.

Features

- very wide bandwidth, 2800 to 7200 MHz
- excellent amplitude unbalance, 0.1 dB typ.
- good phase unbalance, 3 deg. typ.
- small size, 0.118" x 0.118" x 0.035"
- high ESD level
- aqueous washable

Applications

- WiMAX • WLAN
- radar • satellite communication
- ISM • instrumentation

GP2X1+



CASE STYLE: DQ1225

PRICE: \$1.49 ea. CITY. (20)

+RoHS Compliant
The +S suffix identifies RoHS Compliance. See our website for RoHS Compliance methodology and qualifications



Electrical Specifications

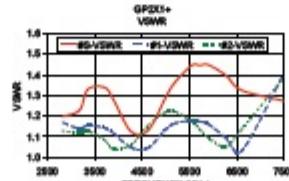
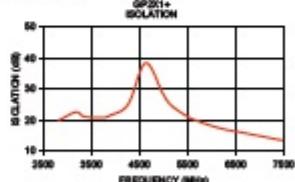
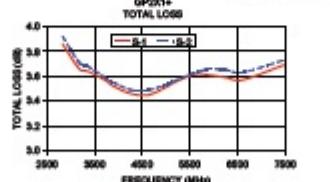
FREQ. RANGE (MHz)	ISOLATION (dB)		INSERTION LOSS* (dB) ABOVE 3.0 dB		PHASE UNBALANCE (Degrees)	AMPLITUDE UNBALANCE (dB)	VSWR (:1) Typ.	
	L-1 ₀	TYP. Min.	TYP.	Max.			Port S	Port 1,2
2800-7200	22	10	0.8	1.9	10.0	0.4	1.5	1.2

* De-embedded from demo board loss.

Typical Performance Data

Frequency (MHz)	Total Loss ¹ (dB)		Amplitude Unbalance (dB)	Isolation (dB)	Phase Unbalance (deg.)	VSWR S	VSWR 1	VSWR 2
	S-1	S-2						
2850.00	3.96	3.92	0.06	19.96	2.37	1.20	1.07	1.13
3100.00	3.66	3.71	0.05	22.55	2.72	1.23	1.14	1.12
3350.00	3.64	3.65	0.04	21.14	2.42	1.33	1.15	1.13
3720.00	3.57	3.59	0.03	20.82	3.20	1.34	1.14	1.08
3900.00	3.52	3.55	0.02	21.57	3.30	1.29	1.12	1.04
4270.00	3.46	3.49	0.04	25.19	5.55	1.12	1.05	1.08
4650.00	3.45	3.49	0.04	35.44	5.97	1.13	1.06	1.15
4990.00	3.51	3.53	0.02	25.55	4.35	1.29	1.13	1.22
5170.00	3.55	3.56	0.01	24.69	4.55	1.58	1.16	1.22
5540.00	3.61	3.62	0.01	20.53	4.94	1.45	1.15	1.15
5720.00	3.62	3.64	0.03	19.75	5.14	1.45	1.17	1.13
5930.00	3.61	3.66	0.05	18.68	5.49	1.45	1.16	1.09
6280.00	3.59	3.65	0.05	17.10	6.01	1.49	1.10	1.05
6600.00	3.57	3.63	0.06	16.13	6.37	1.53	1.03	1.14
7470.00	3.69	3.73	0.04	13.51	7.31	1.27	1.40	1.35

1. Total Loss = Insertion Loss + 9dB splitter loss.



electrical schematic



ESD Rating
Human Body Model (HBM): Class 1A (250 to < 300V) in accordance with ANSI/ESD STM 5.1 - 2001
Machine Model (MM): Class MM (100V to < 250V) in accordance with ANSI/ESD STM 5.2 - 1999

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Notes: 1. Performance and quality attributes and conditions do not imply that the item will be reliable and do not form part of this specification sheet. 2. Electrical specifications and performance data contained herein are based on Mini-Circuits' application experience and performance obtained in laboratory test conditions. 3. The parts covered by this specification sheet are subject to Mini-Circuits standard delivery terms and terms and conditions (Customer Terms). Standard Terms of sale of this part apply to the rights and benefits contained therein. For a full statement of Standard Terms and the exclusive rights and remedies thereunder, please visit Mini-Circuits' website minicircuits.com/MCL.html#Terms.

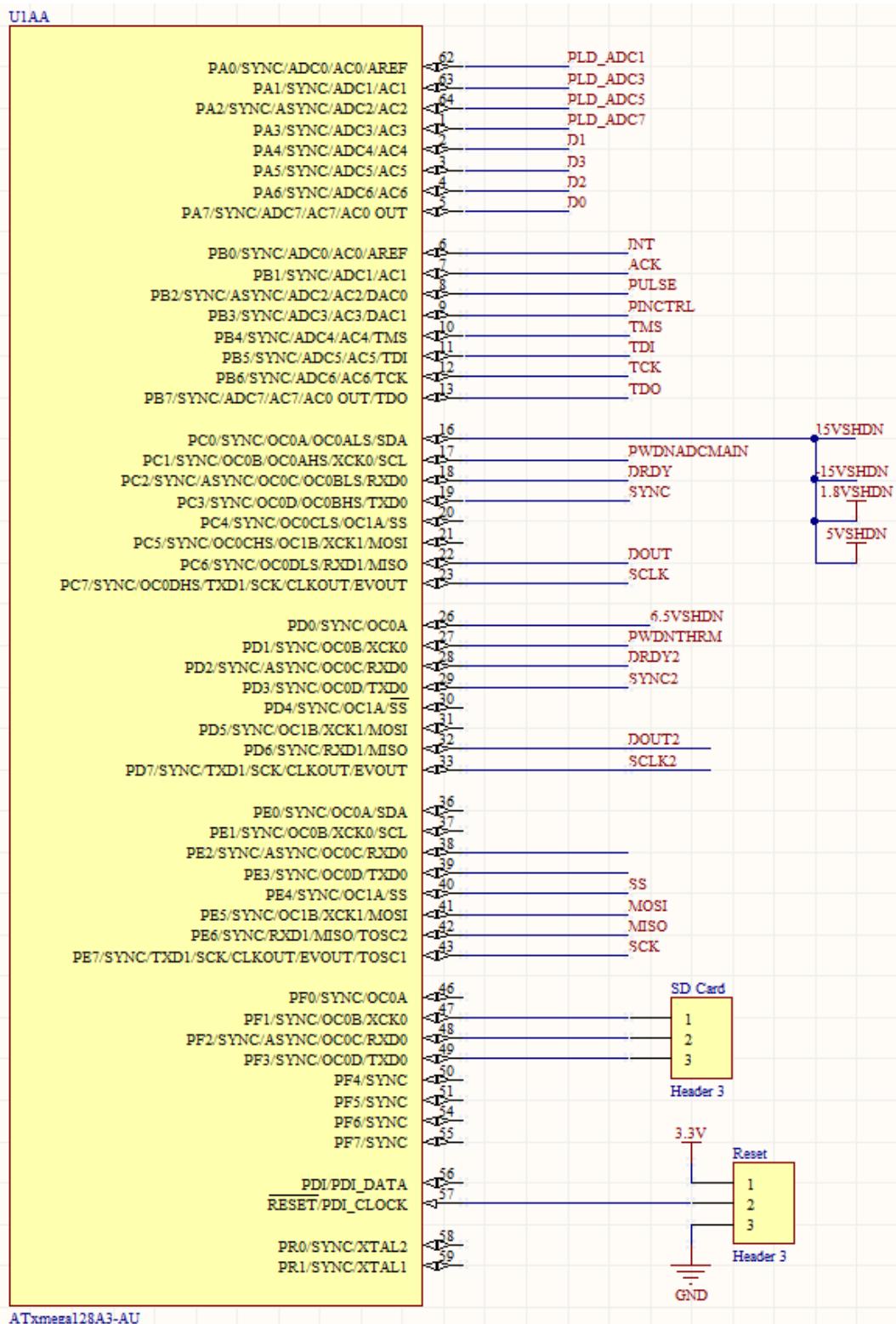
Ref. G
GP2X1+
SD-13012AG
RS-CHM8
12029

TCBC Bias Tee

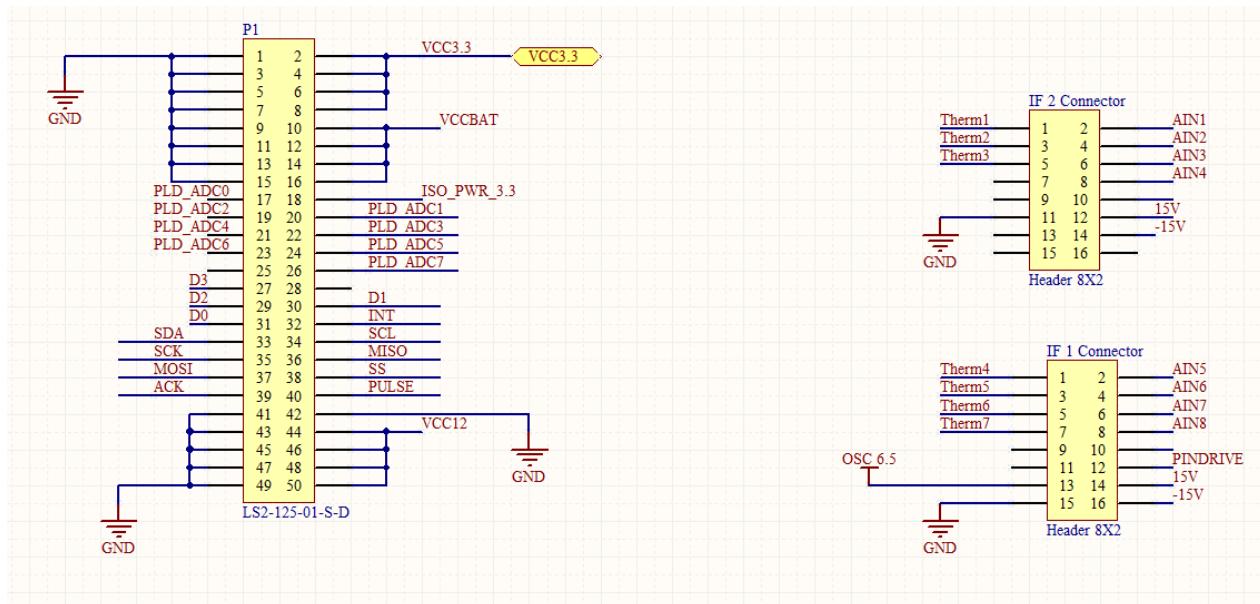
THIRD ANGLE PROJECTION		REVISIONS																													
REV OR A	ECN No. M125202 M130676	DESCRIPTION NEW RELEASE MODIFIED PATTERN		DATE 01/18/10 03/14/11	DR MMG AV																										
<u>SUGGESTED MOUNTING CONFIGURATION FOR GU1414 CASE STYLE, "04BT02" PIN CONNECTION</u>																															
<p>CAPACITOR C1: .010 μF, 0603 SIZE.</p> <p>NOTES: 1. COPLANAR WAVEGUIDE PARAMETERS ARE SHOWN FOR ROGERS R04350B WITH DIELECTRIC THICKNESS .020" \pm .0015"; COPPER: 1/2 OZ. EACH SIDE. FOR OTHER MATERIALS TRACE WIDTH MAY NEED TO BE MODIFIED. 2. FOOTPRINT OF C1 IS SHOWN FOR REFERENCE. 3. BOTTOM SIDE OF THE PCB IS CONTINUOUS GROUND PLANE.</p> <p> DENOTES PCB COPPER LAYOUT WITH SMOBC (SOLDER MASK OVER BARE COPPER) DENOTES COPPER LAND PATTERN FREE OF SOLDER MASK</p> <table border="1"> <tr> <td>UNLESS OTHERWISE SPECIFIED</td> <td>INITIALS</td> <td>DATE</td> </tr> <tr> <td>DIMENSIONS ARE IN INCHES</td> <td>DRANDI</td> <td>12/30/09</td> </tr> <tr> <td>TOLERANCES ON: 3 PL DECIMALS \pm .005</td> <td>MMSG</td> <td>01/18/10</td> </tr> <tr> <td>ANGLES \pm FRACTIONS \pm</td> <td>AV</td> <td>01/18/10</td> </tr> <tr> <td></td> <td>APPROVED</td> <td>01/18/10</td> </tr> <tr> <td></td> <td></td> <td></td> </tr> </table> <p>Mini-Circuits® 13 Neptune Avenue Brooklyn NY 11225</p> <p>PL, 04BT02, GU1414, TB-510+</p> <table border="1"> <tr> <td>SIZE A</td> <td>CODE IDENT 15542</td> <td>DRAWING NO: 98-PL-321</td> <td>REV: A</td> </tr> <tr> <td>FILE: 98PL321</td> <td>SCALE: 10:1</td> <td> SHEET: 1 OF 1</td> <td></td> </tr> </table> <p>THIS DOCUMENT AND ITS CONTENTS ARE THE PROPERTY OF MINI-CIRCUITS. EXCEPT FOR USE EXPRESSLY GRANTED IN WRITING, TO ITS VENDORS, VENDOR'S AND THE UNITED STATES GOVERNMENT, MINI-CIRCUITS RESERVES ALL PROPRIETARY DESIGN, USE, MANUFACTURING AND REPRODUCTION RIGHTS THERETO. THESE CONTENTS SHALL NOT BE USED, DUPLICATED OR DISCLOSED TO ANY OTHER PARTY, IN WHOLE OR IN PART, WITHOUT WRITTEN PERMISSION OF MINI-CIRCUITS.</p> <p>MINI-CIRCUITS®</p> <p>ADDITIONAL DRAWING REVISED DATE 01/18/10</p>						UNLESS OTHERWISE SPECIFIED	INITIALS	DATE	DIMENSIONS ARE IN INCHES	DRANDI	12/30/09	TOLERANCES ON: 3 PL DECIMALS \pm .005	MMSG	01/18/10	ANGLES \pm FRACTIONS \pm	AV	01/18/10		APPROVED	01/18/10				SIZE A	CODE IDENT 15542	DRAWING NO: 98-PL-321	REV: A	FILE: 98PL321	SCALE: 10:1	SHEET: 1 OF 1	
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Schematics

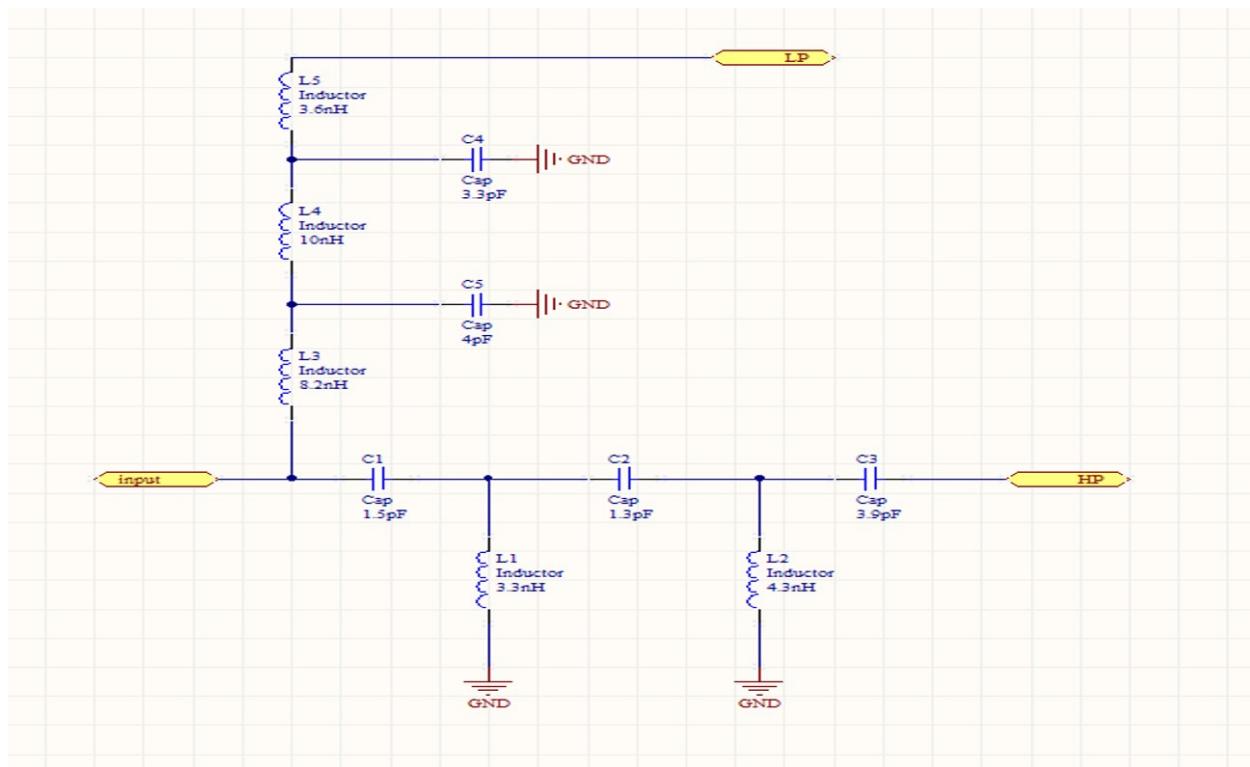
ADC connections to processor



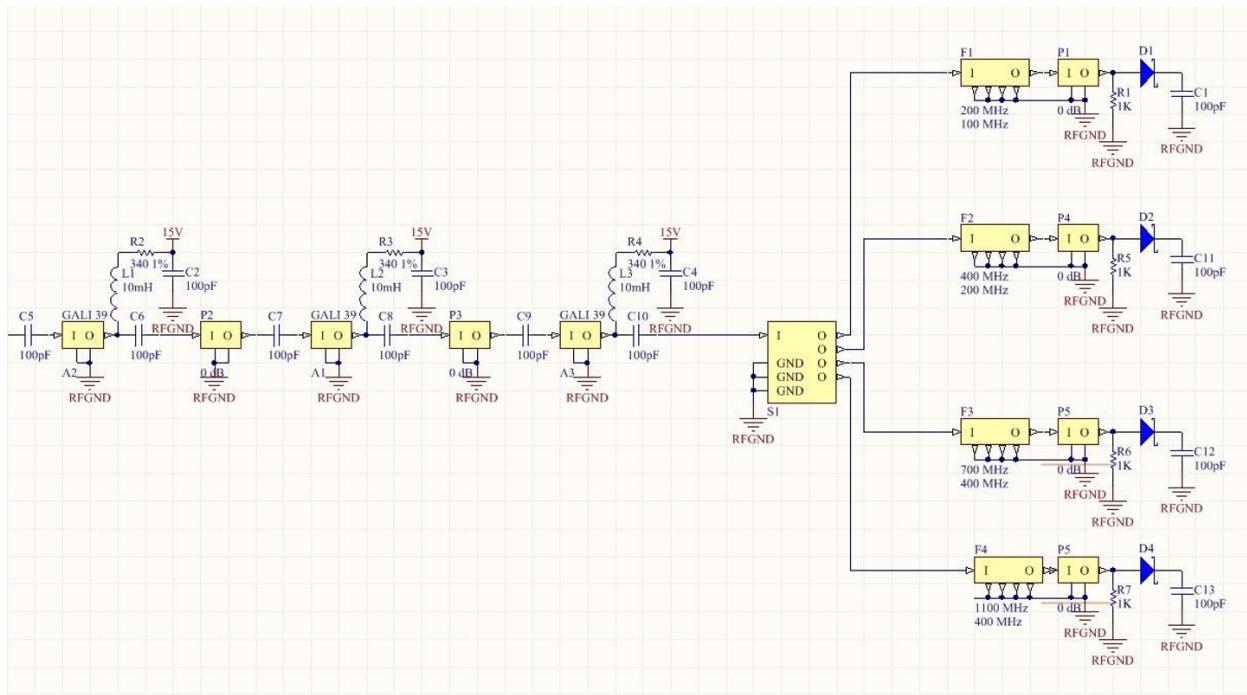
IF and thermistor connections to ADC



Diplexer



Lower Band IF (Ending at Tunnel Diode)



Software

Test software code

```
#include <asf.h>
#include <stdio.h>
#include <stdlib.h>
#include "spi_master.h"

#define PA1 IOPORT_CREATE_PIN(PORTA, 1)
#define PA0 IOPORT_CREATE_PIN(PORTA, 0)

#define PD1 IOPORT_CREATE_PIN(PORTD, 1)

//SPI Definitions
#define ADS_SPI           &SPIC
    //defines an SPI to use, either SPIC or SPID
#define ADS_SPI_CS        IOPORT_CREATE_PIN(PORTC, 4)
//! SCK pin
#define ADS_SPI_MASTER_SCK      IOPORT_CREATE_PIN(PORTC, 7)
//! MOSI pin
#define ADS_SPI_MASTER_MOSI     IOPORT_CREATE_PIN(PORTC, 5)
//! MISO pin
#define ADS_SPI_MASTER_MISO     IOPORT_CREATE_PIN(PORTC, 6)

//SPI Device Struct
struct spi_device ADS_SPI_DEVICE = {
    .id = ADS_SPI_CS
};

int main (void)
{
    board_init();
    sysclk_init();
    gfx_mono_init();

    /*
    osc_enable(OSC_ID_RC32MHZ);
    do {} while(!osc_is_ready(OSC_ID_RC32MHZ));
    sysclk_set_source(SYSCLK_SRC_RC32MHZ);
    sysclk_set_prescalers(SYSCLK_PSADIV_1, SYSCLK_PSBCDIV_1_1);
    pll_disable(0);
    osc_disable(OSC_ID_RC2MHZ);
    */

    ioport_configure_pin(PA0, IOPORT_DIR_OUTPUT | IOPORT_INIT_HIGH);      //sync
    ioport_configure_pin(PA1, IOPORT_DIR_INPUT);
    //drdy

    ioport_configure_pin(PD1, IOPORT_DIR_OUTPUT | IOPORT_INIT_HIGH);      //Port D SPI
    SCK

    gpio_set_pin_high(NHD_C12832A1Z_BACKLIGHT);
    gpio_set_pin_high(PD1);
```

```

//SPI Setup
ioport_configure_pin(ADS_SPI_MASTER_SCK, IOPORT_DIR_OUTPUT           //output when
master
| IOPORT_INIT_HIGH);
ioport_configure_pin(ADS_SPI_MASTER_MOSI, IOPORT_DIR_OUTPUT          //output when
master
| IOPORT_INIT_HIGH);
ioport_configure_pin(ADS_SPI_MASTER_MISO, IOPORT_DIR_INPUT); //input when master
ioport_configure_pin(ADS_SPI_CS, IOPORT_DIR_OUTPUT | IOPORT_INIT_HIGH);
//add in "| IOPORT_INIT_HIGH" to use as a master

spi_master_init(ADS_SPI);
spi_master_setup_device(ADS_SPI,&ADS_SPI_DEVICE,SPI_MODE_0,8000000,0);
spi_select_device(ADS_SPI, &ADS_SPI_DEVICE);

spi_enable(ADS_SPI);      //Enable defined SPI

uint8_t temp = 0;
char buff[24];
char buff2[24];
char buff3[24];

//***ADC start up

sprintf(buff, "Starting..."); 
gfx_mono_draw_string(buff, 0, 0, &sysfont);
delay_s(2);

//sync toggle code
sprintf(buff, "SYNC high 1 ");
gfx_mono_draw_string(buff, 0, 0, &sysfont);
gpio_set_pin_high(PA0);    //sets SYNC high
delay_s(1);

sprintf(buff, "SYNC low    ");
gfx_mono_draw_string(buff, 0, 0, &sysfont);
gpio_set_pin_low(PA0);
delay_s(1);

sprintf(buff, "SYNC high 2 ");
gfx_mono_draw_string(buff, 0, 0, &sysfont);
gpio_set_pin_high(PA0);
delay_s(1);

uint32_t test_data = 0x0; //0x7fffffff is VREF
uint8_t data0 = 0;
uint8_t data1 = 0;
uint8_t data2 = 0;
float voltage = 0;
uint8_t v1;
uint8_t v2;
uint8_t v3;
uint8_t x = 0;

double vref = 2.5;

```

```

while (true)
{
    while(gpio_pin_is_high(PA1))           //waits for DRDY to go low
    {

    }

    //Read SPI
    spi_read_packet(ADS_SPI, &temp, 1);
    test_data = (uint32_t)temp;
    test_data = test_data << 8;

    spi_read_packet(ADS_SPI, &temp, 1);
    test_data += temp;
    test_data = test_data << 8;

    spi_read_packet(ADS_SPI, &temp, 1);
    test_data += temp;

    //sprintf(buff, "Updating...      ");
    //gfx_mono_draw_string(buff, 0, 0, &sysfont);
    for (x = 0; x < 48; x++)
    {
        gfx_mono_draw_pixel(x,30,1);
        gfx_mono_draw_pixel(x,31,1);
        delay_ms(5);
    }
    delay_ms(50);
    clear_bar();

    data2 = (uint8_t)(test_data);           //8 least significant bits
    data1 = (uint8_t)(test_data>>8);     //8 middle significant bits

    if(test_data >= 0x800000)   //if two's compliment is negative
    {
        //determines two's compliment
        data0 = (uint8_t)((test_data>>16) - 0x80);      // 8 most
significant bits, removes sign bit
        sprintf(buff2, "2's Comp: -%01x%02x%02x ", data0, data1,data2);

        //determines original value
        data0 = (uint8_t)(test_data>>16);
        sprintf(buff, "Original: %01x%02x%02x ", data0, data1,data2);

        //determines voltage to 2 decimal places
        voltage = ((double)((test_data ^ 0xffffffff) + 1) / 0x7fffff) * vref;
    //flip all bits then add 1
        v1 = (uint8_t)voltage;
        v2 = (uint8_t)((voltage - (uint8_t)voltage) * 10);
        v3 = (uint8_t)((voltage * 10 - (uint8_t)(voltage * 10)) * 10);
        sprintf(buff3, "Voltage: -%01u.%01u%01u V", v1, v2, v3);
    }
    else //two's compliment is positive
    {
        //determines two's compliment
    }
}

```

```

    data0 = (uint8_t)(test_data>>16);
    sprintf(buff2, "2's Comp: %01x%02x%02x ", data0, data1,data2);

    //determines original value
    sprintf(buff, "Original: %01x%02x%02x ", data0, data1,data2);

    //determines voltage to 2 decimal places
    voltage = ((double)(test_data) / 0x7fffff) * vref;
    v1 = (uint8_t)voltage;
    v2 = (uint8_t)((voltage - (uint8_t)voltage) * 10);
    v3 = (uint8_t)((voltage * 10 - (uint8_t)(voltage * 10)) * 10);
    sprintf(buff3, "Voltage: %01u.%01u%01u V", v1, v2, v3);
}

//Write data on LCD
gfx_mono_draw_string(buff, 0, 0, &sysfont);
gfx_mono_draw_string(buff2, 0, 9, &sysfont);
gfx_mono_draw_string(buff3, 0, 18, &sysfont);
delay_s(1);

data0 = 0;
data1 = 0;
data2 = 0;

}
}

```

Future Project Notes

ADC testing concerns

The ADS1278EVM-PDK is an effective platform to test and debug software for use with the ADS1278. However, there are a few concerns when using it that must be mitigated before it can be used for testing.

The datasheet for the ADS1278EVM-PDK is lacking. Specifically, a number of silk screen labels on the PDK differ from labels present in the datasheet. This includes labels for crucial header pins and the like. Generally, the headers which are being referenced by the datasheet can be clarified by determining the pin count on the header being discussed, as the headers on the board are each unique in their pin count.

A minor detail that also caused difficulty in using the PDK is that there is a flip-flop present at the DOUT data output pin on the header discussed as J5 in the datasheet. Avoid using this pin and instead use the DOUT1 pin on the top right of the header discussed as J2 in the datasheet.

Finally, the EVM board does not seem to honor the FS/SPI switch present. Rather, the format argument sent in on the FORMAT pins of the ADC indicate that the ADC should stay in frame-sync mode, which will cause issues when attempting to use SPI. This is regardless of which SPI/FS selection is made. To get around this for the EVM, a user must install the software called “ADCPro” which is referenced in the datasheet. Upon installing this software and interfacing with the ADC EVM board over USB, the software can be used to force the ADC board into the correct mode by selecting “TDM Dynamic” as the format option. This will cause the FORMAT2 pin to be set correctly and allow the ADC to operate in its SPI-compatible mode. It is important that the EVM not actually be used to collect data if any of the default configurations (such as jumpers or switches) have been changed, otherwise this may damage the EVM board. If any problems are being encountered with the ADC, it is recommended to use an oscilloscope to test the FORMAT pin values.

Outstanding ADC Data Concern

One problem that needs to be addressed regarding the ADCs is their continuous operation regardless of the processor data handling state. This means that it is likely that data in the process of being collected will at some point be overwritten, causing subsequent data to be useless in the context of the collected data.

A likely solution to this problem would be to time the data collection such that at most one sample of the 32 averaged samples per channel is corrupted, and then interrupt on the DRDY pin transitioning high (indicating that a new set of data has been sampled). Using this, it would be possible to throw out the current sample set completely, but resume collecting the additional samples required for the 32 samples needed for the average.

Xplained Boards and Software

For prototyping and testing software, the XMEGA A3BU Xplained boards are extremely useful, as the required setup is minimal. These are a platform specifically for getting introduced to the ATxmega architecture and development, are well documented, and have a number of relevant examples present on Atmel.com and in the Atmel Software Framework. To get started on software development using the Xplained boards, one need to install Atmel Studio 6 for development and the Atmel Flip software for programming the Xplained board. When building a project, Atmel Studio 6 will produce a .hex file which can be read with the Flip software, and the Flip software will program the processor on the Xplained board with this file. Each of these software packages have a manual which can be read for more detail. To program an Xplained board, hold down SW0 while plugging it into the USB port of the programmer computer to initialize the USB bootloader which interfaces with the Flip software. An application can then be run on the board by clicking “Start Application” in the Flip software. The Xplained board users guide goes over a number of other concerns as well.

It is recommended that one begin use one of the example projects provided by the Atmel Software Framework. Crucial learning objectives to succeed on a similar project are interfacing with GPIO, using SPI, and writing interrupt service routines to allow for full-duplex SPI operation and external data signal handling. Examples of such software can be found in previous appendices as well.

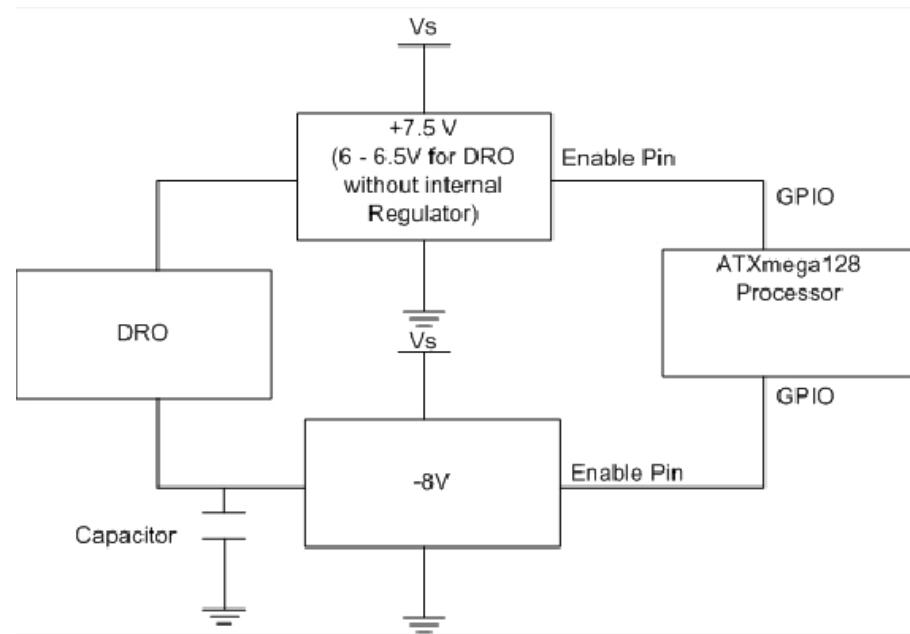
DRO concerns

The power circuitry for the current iteration of the digital PCB are for that of a Gunn oscillator, rather than the selected DRO. The DRO is the future direction of new iterations of this project and was discussed at length.

The DRO has two power ports: one positive and one negative. The DRO might end up being used in one of two configurations. The DRO has an internal voltage regulator, but it may be available without that regulator (allowing the project team to regulate voltage externally). If

used in this configuration, the DRO's positive power port will be at +6.5 V (a regulator for which is used in the current project iteration). With the regulator, this port must be powered at +7.5 V nominally. This port is expected to draw 450 mA at minimum. The negative power port is powered at -8 V and is expected to draw 10 mA nominally.

Importantly, the negative supply port must be powered before the positive supply port. The delay between powering the negative supply and positive supply should be at least 100 ms. Furthermore, the reverse order must happen during power down of the DRO. In the case of the ALL-STAR system cutting off power to the payload or any sort of payload device failure, this sequence must still be present to prevent damage to the DRO. This can be accomplished by having a large capacitance at the negative supply pin. Care must be taken to ensure the capacitance is large enough to support the 100 ms difference required between the positive port falling to zero and the negative supply being turned off.



Component Selection and Board Populating

Currently, several of the components (EEE-FP1E680AP capacitor, Switching converter inductors NR10050Txxx, crystal oscillator) on the digital board are not designed to be easily hand soldered (contacts are on the bottom). For hand soldering, different components should be selected.

Errata

Final PCB

On the final PCB, footprint errors exist for the ADC reference chip (the footprint was much too large for the actual chip) and the ADC oscillator (Pin assignments were flipped in the footprint).

Works Cited

- [1] Capstone Team 2011 (RadSat) Technical Reference Manual.