

IMPERIAL

# Charge Noise in Semiconductor Qubits for Quantum Computing

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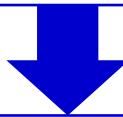
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# Background & Motivation

Why do we need quantum computing?

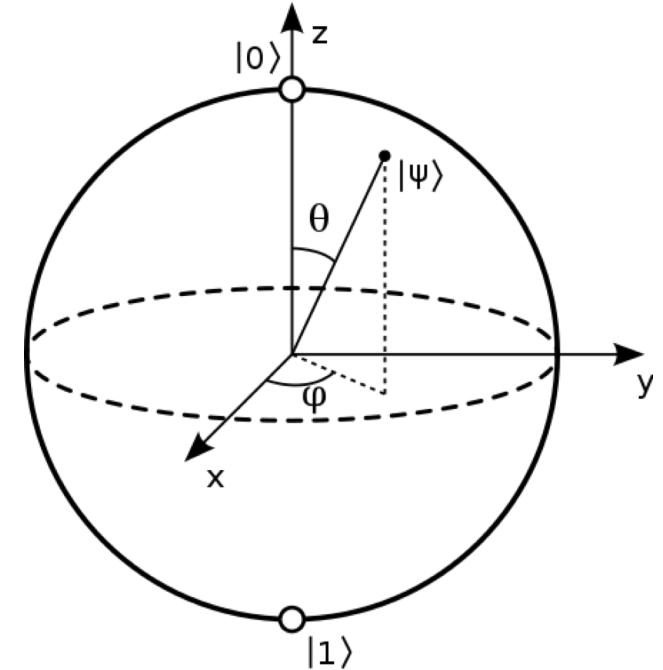
## Classical computing is reaching its limits

- Moore's law is slowing down
- Some problems (e.g., quantum simulations, cryptography) are impractical on classical computers



## Quantum computing offers exponential speed-ups

- Superposition  $|\psi\rangle = \cos\frac{\theta}{2}|0\rangle + e^{i\varphi}\sin\frac{\theta}{2}|1\rangle$
- Entanglement  $|\psi\rangle = \frac{1}{\sqrt{2}}(|00\rangle + |11\rangle)$
- Parallel computation



# Background & Motivation

## Why semiconductor qubits?

### DiVincenzo criteria

- **Scalability:** Thousands of qubits for practical use
- **Initialization:** Well-defined starting state
- **Coherence:** Long-lived quantum states
- **Universal gate set:** High-fidelity quantum logic gates
- **Measurement:** Reliable quantum state readout

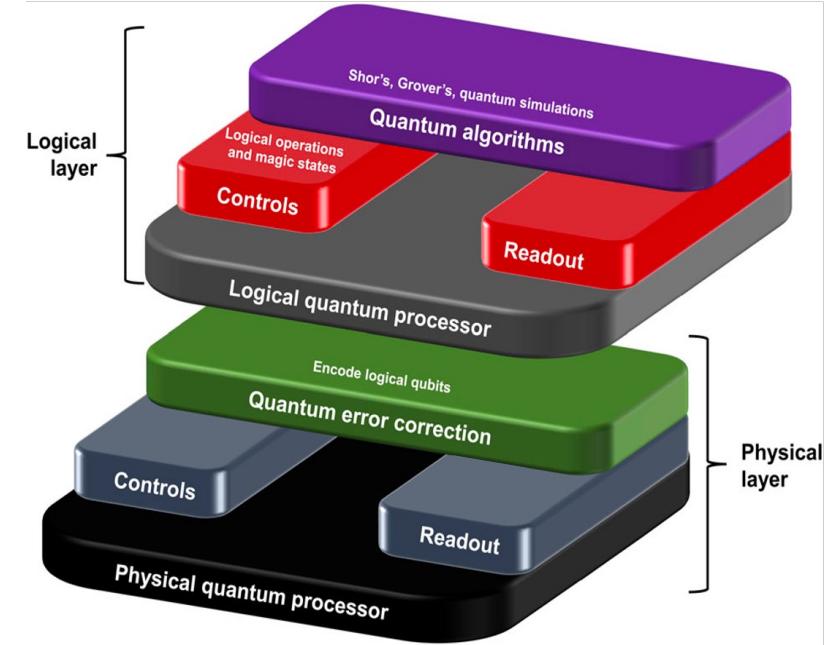
**Platforms:** superconducting circuits, trapped ions, neutral atoms, **semiconductors**



### Advantages

- **Scalability** - Compatible with existing fabrication processes
- **Compact sizes** – High-density qubit arrays on a chip
- **Potential for long coherence times** at cryogenic temperatures

**Figure:** Gambetta, J.M., Chow, J.M. & Steffen, M. Building logical qubits in a superconducting quantum computing system. *npj Quantum Inf* **3**, 2 (2017). <https://doi.org/10.1038/s41534-016-0004-0>



How to build a quantum computer?

# Background & Motivation

## Charge noise

### Key challenge - Charge noise

- Random fluctuations in the electric field around a qubit
- Caused by material defects, impurities, and trapped charges
- Character: 1/f noise

### Impact

- Gate fidelity reduction
- Shorten coherence time
- Scalability challenge

### Goal

- Build a charge noise model

### Mitigation strategies

- Improved material design
  - High-purity materials
  - Better fabrication techniques
- Dynamic decoupling
- Use control pulses to average out noise effects

# Theory

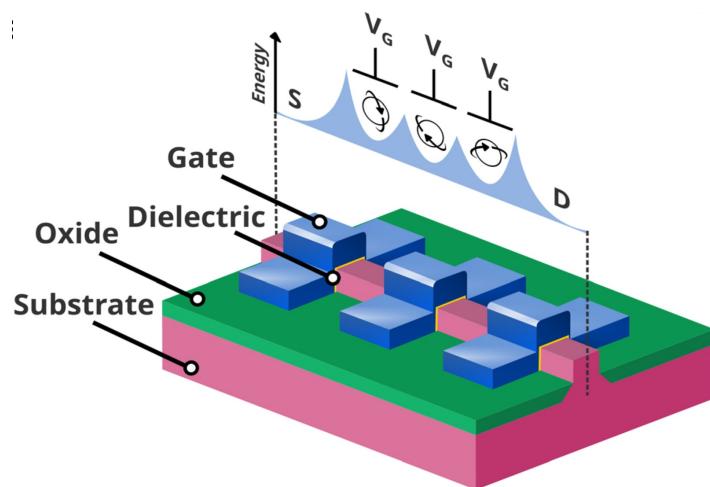
## Semiconductor qubits

### Quantum dot (QD)

nanoscale semiconductor traps that confine single electrons

### Semiconductor qubits

- Spin qubits:  $\uparrow$  or  $\downarrow$
- Charge qubits: electron's position



	Spin Qubit	Charge Qubit
<b>Physical Representation</b>	Electron spin in a quantum dot	Electron position in a double quantum dot
<b>Control</b>	Magnetic field	Electric field (gate voltage)
<b>Coherence Time</b>	Long (ms)	Short ( $\mu$ s)
<b>Gate Operation Speed</b>	Slower (GHz range)	Faster (THz range)
<b>Current Experimental Performance</b>	Longer coherence, but complex fabrication and control	Short coherence but easier fabrication and fast operation
<b>Sensitivity to Charge Noise</b>	Low (indirectly via spin-orbit coupling, hyperfine interaction)	High (directly affected by charge fluctuations)

Figure: J. Michniewicz, M. S. Kim; Leveraging off-the-shelf silicon chips for quantum computing. *Appl. Phys. Lett.* 24 June 2024; 124 (26): 260502. <https://doi.org/10.1063/5.0207162>

# Theory

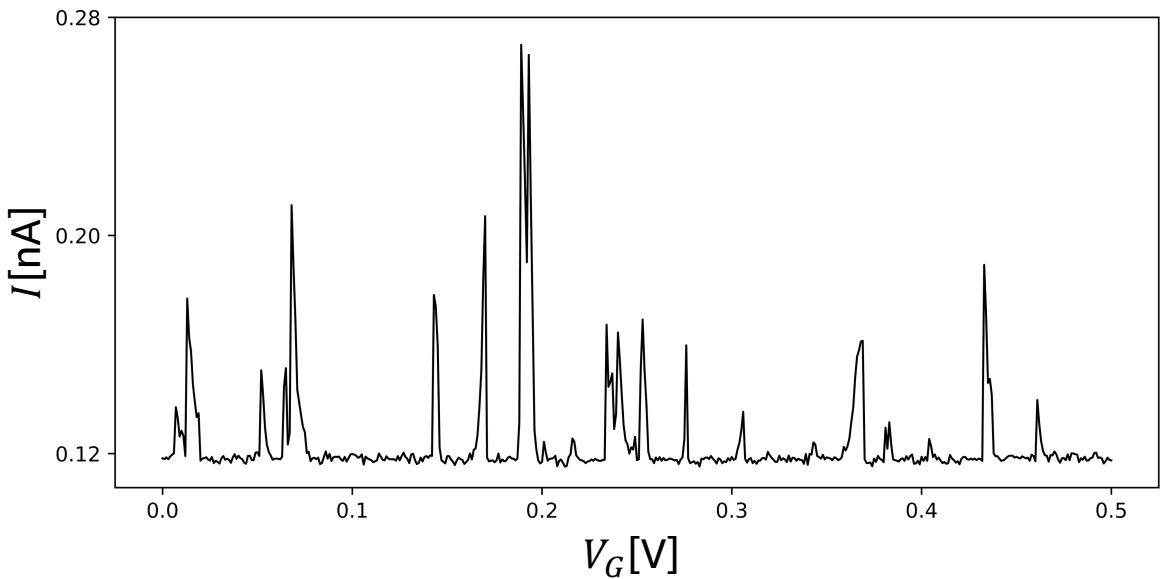
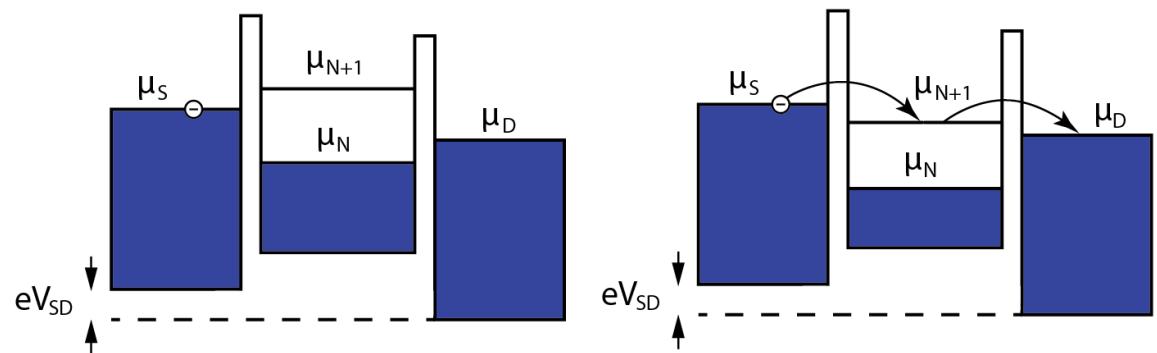
## Coulomb blockade

**Rule:** *electrons can only enter/exit if external energy overcomes electrostatic repulsion.*

- At room temperature  $\rightarrow$  high thermal excitation
- At ultra-low temperatures and small bias voltage  
 $\rightarrow$  Gate voltage adjusts dot potential  
 $\rightarrow$  Electrons added one by one  
 $\rightarrow$  Coulomb peaks

### Coulomb peaks:

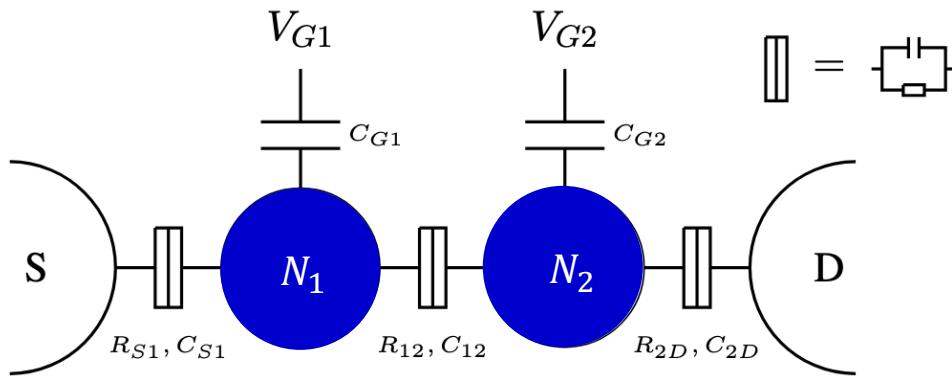
Current spikes at specific gate voltages  
 $\rightarrow$  mark when an electron enters/leaves the dot



# Theory

## Charge stability diagram

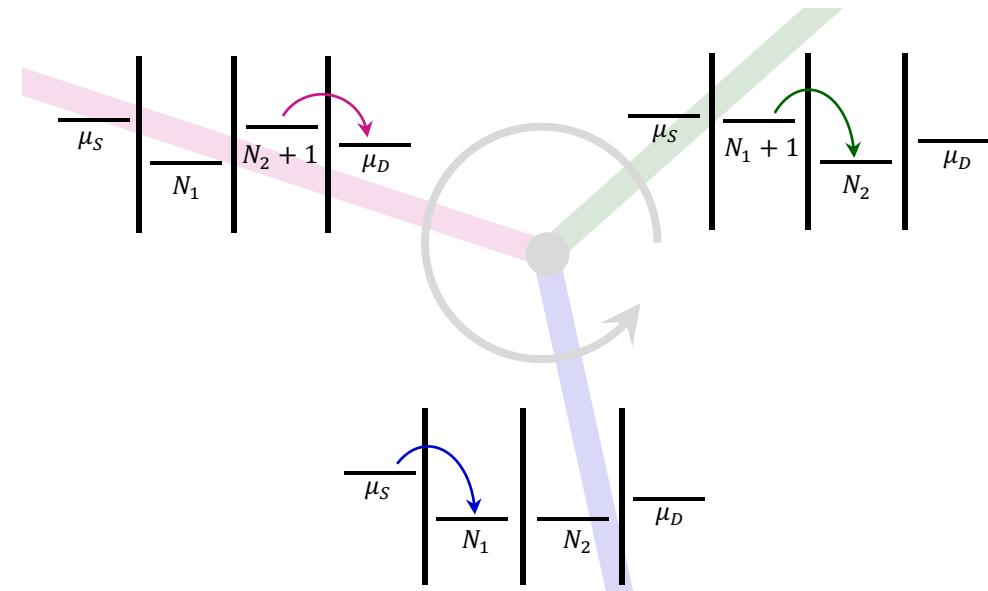
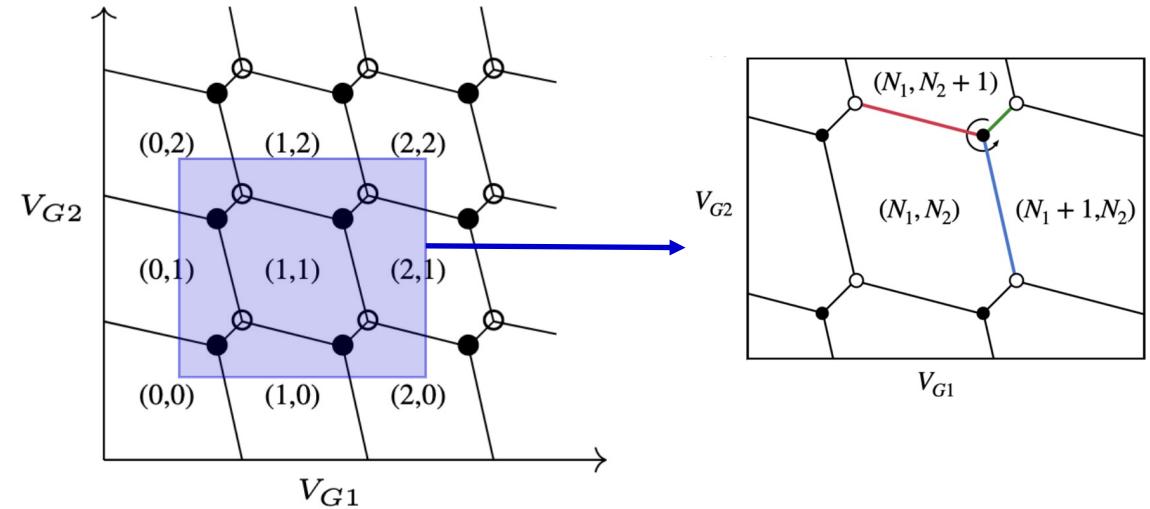
### Double quantum dot (DQD)



### Charge stability diagram

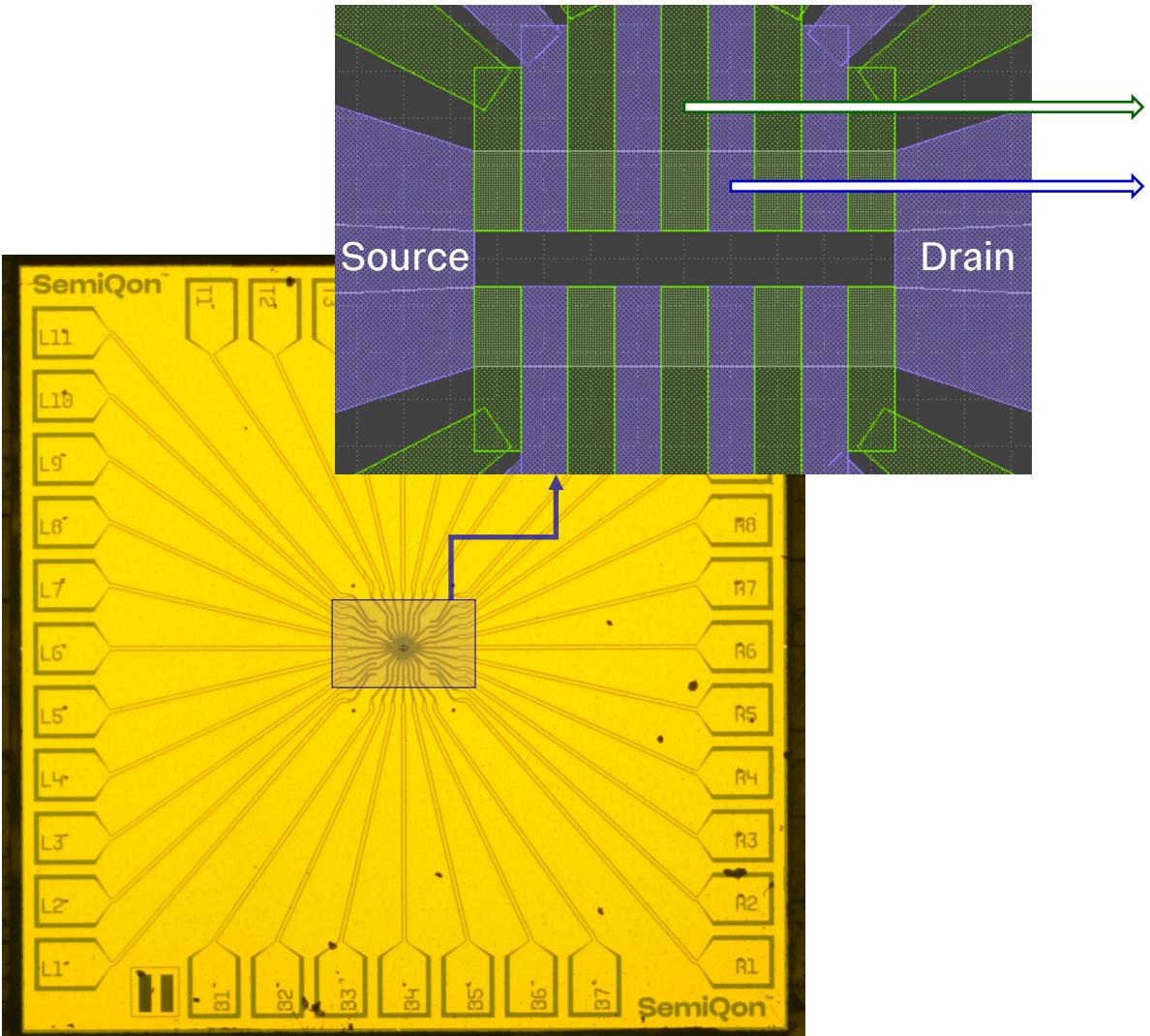
Electron occupancy vs. gate voltages

- Device tuning
- Qubit state definition
- Noise sensitivity analysis



# Method & Progress

## Device & Experiments



Silicon-based quantum chip

**Barrier gate:** control tunneling

**Plunger gate:** control quantum dot potential

### Experiments

- **Preparation**

- Wire bonding to connect chip to holder
- Verify gate control functionality across all gates

- **Measurements**

- Conduct pinch-off measurements at room and ultra-low temperatures
- Characterize Coulomb diamonds
- Deploy quantum dot as charge sensor
- Implement lock-in amplifier measurements
- Investigate charge noise vs. temperature

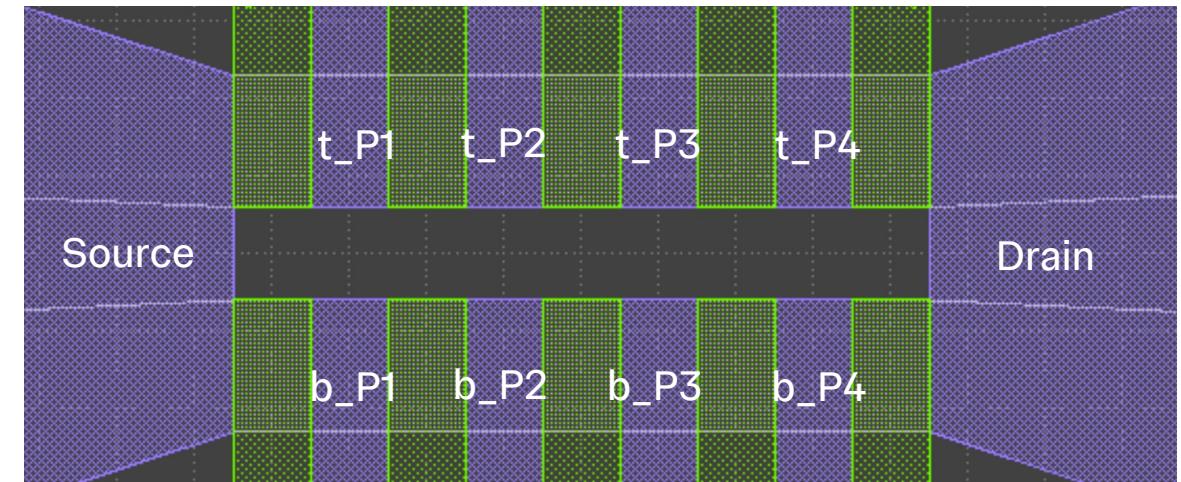
# Method & Progress

## Pinch-off measurements

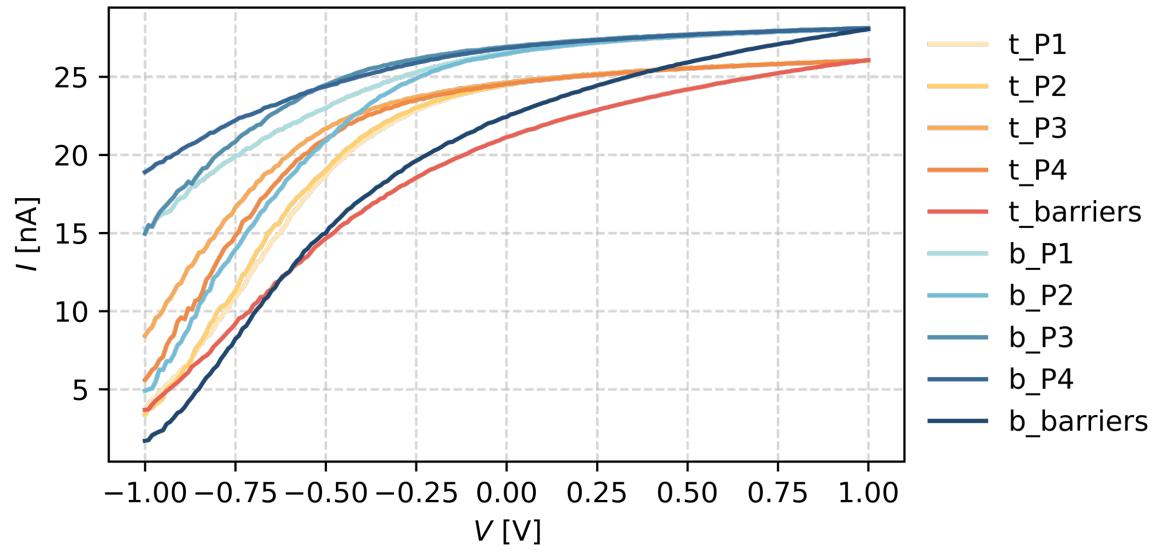
Sweep: each gate voltage

Measure: current

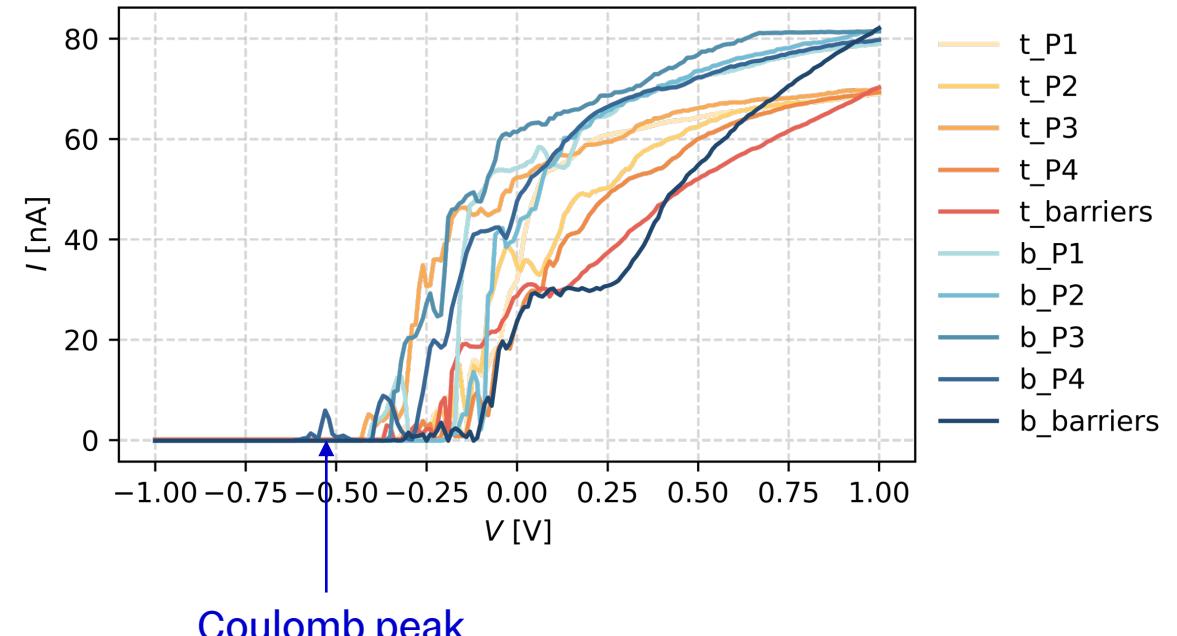
**Cool down → Physics happening in the lab!**



- At room temperature



- At 10 mK



# Method & Progress

## Coulomb diamond characterization

### Coulomb diamond

- Electrons cannot tunnel in/out freely
- Zero current regions (diamonds)

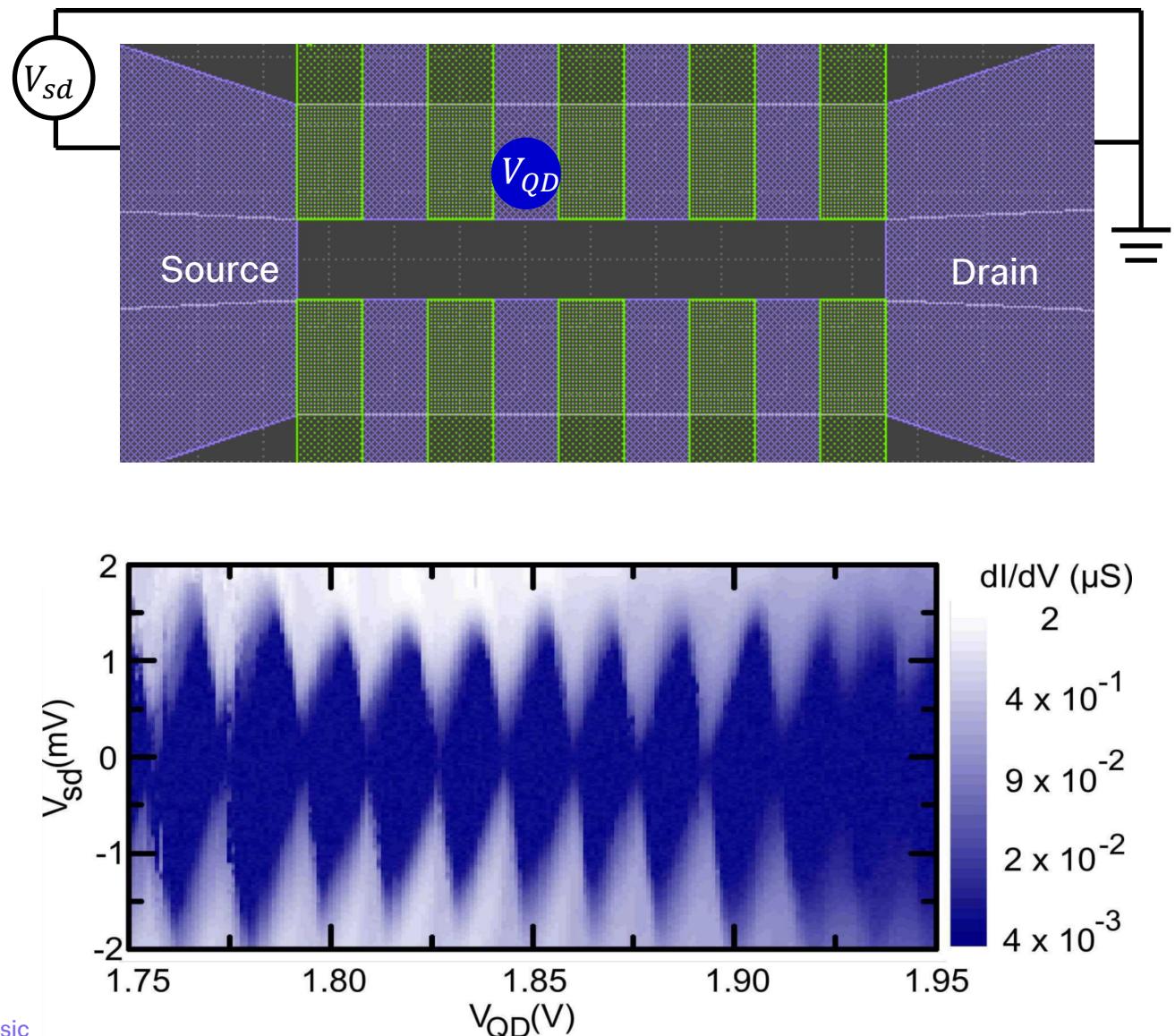
### Key information from boundaries

- Capacitance ratio  $\leftarrow$  Slope of diamond edges
- Charge state transition
- Energy gaps  $\leftarrow$  Diamond size

### Method

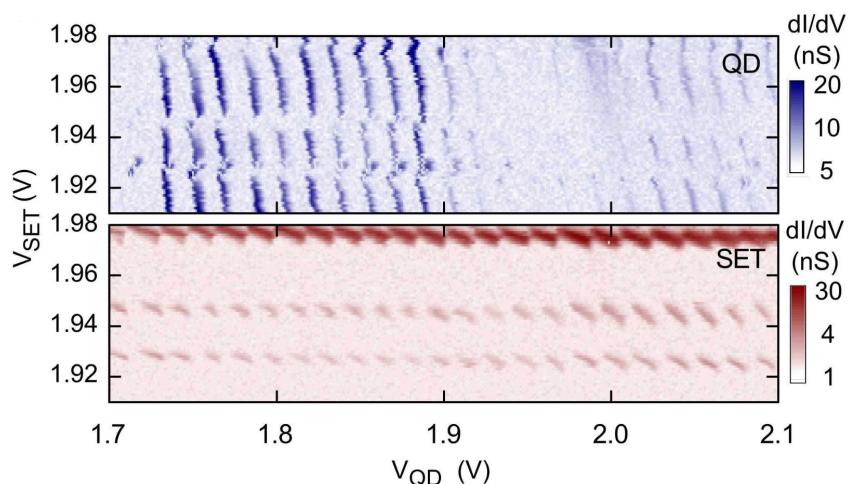
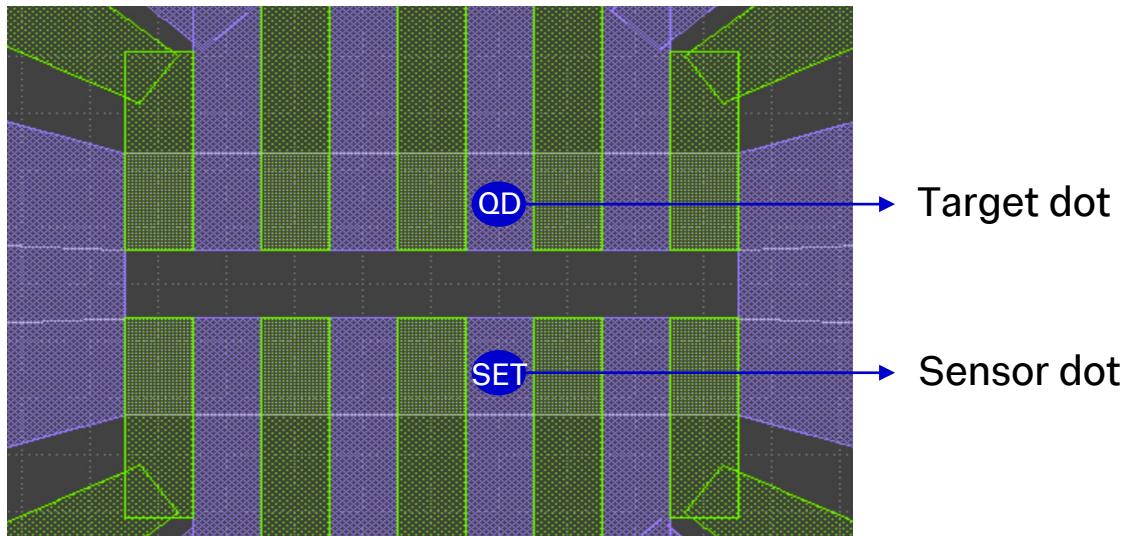
- Sweep gate voltage and bias voltage
- Measure current  $\rightarrow$  Generate 2D plot

**Figure (bottom):** G. J. Podd, S. J. Angus, D. A. Williams, A. J. Ferguson; Charge sensing in intrinsic silicon quantum dots. *Appl. Phys. Lett.* 22 February 2010; 96 (8): 082104. <https://doi.org/10.1063/1.3318463>



# Method & Progress

## Charge sensing



### Sensor dot

One dot acts as a charge sensor, coupled to the target dot.

### Charge detection

Electron occupation in the target dot shifts the sensor dot's chemical potential  
→ modulates conductance

### Lock-in amplifier

Apply a small AC voltage  
→ detect only the response at a specific frequency  
→ filter out unwanted noise

**Figure (bottom):** G. J. Podd, S. J. Angus, D. A. Williams, A. J. Ferguson; Charge sensing in intrinsic silicon quantum dots. *Appl. Phys. Lett.* 22 February 2010; 96 (8): 082104. <https://doi.org/10.1063/1.3318463>

# Thank you

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- 2 Why semiconductor qubits?
- 3 Why charge noise?
- 4 How semiconductor qubits work?
- 5 Experimental setups & Measurements

Charge Noise in Semiconductor Qubits for Quantum Computing

14/02/2025

# Appendix

## Semiconductor qubits

Property	Spin Qubit	Charge Qubit
<b>Physical Representation</b>	Electron spin in a quantum dot	Electron position in a double quantum dot
<b>Main Control Mechanism</b>	Magnetic field (EPR, ESR, EDSR)	Electric field (gate voltage)
<b>Sensitivity to Charge Noise</b>	Low (indirectly via spin-orbit coupling, hyperfine interaction)	High (directly affected by charge fluctuations)
<b>Sensitivity to Magnetic Noise</b>	High (nuclear spin noise in GaAs, reduced in Si)	Low (not directly influenced by magnetic noise)
<b>Coherence Time T2*</b>	Milliseconds (Si-based); limited by nuclear spin noise	Microseconds; limited by charge noise
<b>Gate Operation Speed</b>	Slower (GHz range)	Faster (THz range)
<b>Scalability</b>	Challenging due to variability in quantum dot arrays	Easier to scale but highly sensitive to noise
<b>Current Experimental Performance</b>	Longer coherence, but complex fabrication and control	Short coherence but easier fabrication and fast operation

# Appendix

## Qubit platforms

Qubit Type	Advantages	Disadvantages
<b>Superconducting</b>	<ul style="list-style-type: none"><li>Fast gate operations (ns)</li><li>Scalable microfabrication</li><li>Mature technology (1000+ qubits demonstrated)</li></ul>	<ul style="list-style-type: none"><li>Requires extreme cryogenics (~10 mK)</li><li>Moderate coherence times (milliseconds)</li><li>Higher error rates than trapped ions</li></ul>
<b>Semiconductor</b>	<ul style="list-style-type: none"><li>Leverages existing semiconductor industry</li><li>Long spin coherence times (seconds in silicon)</li><li>Potential for dense integration</li></ul>	<ul style="list-style-type: none"><li>Complex control (microwave/magnetic fields)</li><li>Slower gate speeds (microseconds)</li><li>Readout and scalability challenges</li></ul>
<b>Trapped Ions</b>	<ul style="list-style-type: none"><li>Long coherence times (seconds to minutes)</li><li>High-fidelity gates (&gt;99.9%)</li><li>All-to-all connectivity</li></ul>	<ul style="list-style-type: none"><li>Slow gate operations (ms to <math>\mu</math>s)</li><li>Complex vacuum/laser systems</li><li>Scaling challenges (trap size)</li></ul>
<b>Neutral Atoms</b>	<ul style="list-style-type: none"><li>Long coherence times (seconds)</li><li>Scalable 2D/3D arrays</li><li>Programmable Rydberg interactions</li></ul>	<ul style="list-style-type: none"><li>Slower gates (ms)</li><li>Complex laser/optical setups</li><li>Lower gate fidelity vs. trapped ions</li></ul>
<b>Photonic</b>	<ul style="list-style-type: none"><li>Room-temperature operation</li><li>Low decoherence (ideal for communication)</li><li>High-speed operations (fs/ps)</li></ul>	<ul style="list-style-type: none"><li>Probabilistic entanglement generation</li><li>Difficult two-qubit gates (nonlinear optics required)</li><li>Photon loss and storage challenges</li></ul>