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**Charge Noise in Semiconductor Qubits
for Quantum Computing**

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“All over the place were sixpence, but he looked up at the moon.”

— popular summary of W. Somerset Maugham’s *The Moon and Sixpence*

Dedication

To those who, even when surrounded by sixpence,
still choose to look up at the moon —
to wonder, to question, to create.

For my mom and dad,
who taught me to follow curiosity,
and always look up at the moon.

献给我的爸爸妈妈：
是你们教会我心向星辰，追问万物。

也献给那些，
即使身边满是六便士，
也依然在仰望月亮的人。

Declaration

I hereby declare that, except where explicit reference is made to the work of others, the content of this thesis is entirely my own. The thesis contains fewer than 20,000 words, excluding the title page, table of contents, appendices, and bibliography. All uses of AI tools conform to the academic standards and policies of Imperial College London.

Chen Huang
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Acknowledgements

From a small town in Southeast China, I couldn't have imagined the journey that brought me here: from the best high school in my province to a top Chinese university, through a gap year working in a quantum computing company, and now, to Imperial. Yet, one thing always remained the same: my deep passion for physics and the childhood dream of becoming a physicist.

Once at Imperial, the initial excitement soon gave way to a fresh set of personal challenges. Living abroad for the first time, I was fully immersed in a new culture and language. I often found myself rehearsing conversations, my brain's "CPU" feeling overwhelmed after even a short chat. The language barrier was tough, making it hard to connect easily with my supervisor and colleagues.

Amidst these personal adjustments, I was also thrown into a completely new field: semiconductor physics. It was a fresh start, demanding endless hours of reading and learning. At the same time, I managed a remote internship with a quantum operating system group. My days started early, finishing tasks and joining discussions with collaborators in China before heading to campus for my master's research. This period was incredibly intense, yet it gave me an invaluable, complete map of full-stack quantum computing - from hardware to software, and across diverse platforms like neutral atoms, trapped ions, and semiconductors. This deep dive truly helped me discover where my passion and motivation truly lie.

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Keep walking your path in the quantum world. Stay curious. Keep exploring.

And may you always enjoy the journey in your own Xanadu.

Abstract

This thesis experimentally investigates charge noise in silicon-based semiconductor quantum dots (QDs), a major source of decoherence for semiconductor qubits. Using a custom Python automation framework, the study characterized QDs in a linear array device at cryogenic temperatures. It revealed enhanced gate control and stable QD formation under specific plunger gates (t_P1 , t_P4 , b_P1 , b_P4), with Coulomb peak periods ranging from 26 mV to 28 mV. Frequency-resolved current noise measurements consistently showed $1/f^\beta$ -like noise, with exponents β between 0.766 ± 0.270 (t_P4) and 1.268 ± 0.234 (b_P4). Current noise amplitudes at 1 Hz varied spatially, from 4.14 ± 6.26 pA/ $\sqrt{\text{Hz}}$ (t_P1) to 8.69 ± 4.76 pA/ $\sqrt{\text{Hz}}$ (b_P4). These values are consistent with typical noise levels reported in similar SiMOS and Si/SiGe systems. A strong correlation was found between the clarity of Coulomb diamond features and lower charge noise, with b_P4 exhibiting both the clearest diamonds and lowest noise. These findings highlight the significant influence of device geometry and material quality on charge stability and the pervasive nature of charge traps. This work advances the understanding of charge noise in silicon-based QDs, informing the design of more robust qubit architectures.

Contents

| | | |
|----------|---|-----------|
| 1 | Introduction | 1 |
| 2 | Theory | 3 |
| 2.1 | Quantum dots and charge transport | 3 |
| 2.1.1 | Formation of quantum dots | 3 |
| 2.1.2 | Coulomb blockade | 5 |
| 2.1.3 | Double quantum dot systems and honeycomb diagrams | 7 |
| 2.2 | Transistor as hosts for quantum dots | 9 |
| 2.2.1 | MOSFET transport regimes and characteristics | 10 |
| 2.2.2 | Carrier transport mechanisms | 12 |
| 2.2.3 | Short-channel effects | 13 |
| 2.3 | Qubit implementation within quantum dots | 14 |
| 2.3.1 | Spin qubits | 15 |
| 2.3.2 | Charge qubits | 19 |
| 2.3.3 | Summary of qubit performance | 20 |
| 2.4 | Charge noise in quantum dot systems | 20 |
| 2.4.1 | Two-level fluctuators | 22 |
| 2.4.2 | Charge noise effects on qubit performance | 24 |
| 3 | Experimental methods | 27 |
| 3.1 | Experimental setup | 27 |
| 3.1.1 | Silicon-based quantum dot device | 27 |
| 3.1.2 | Chip-to-PCB connection using wire bonding | 28 |
| 3.1.3 | Dilution refrigerator | 31 |
| 3.2 | Electronics for gate control and signal readout | 32 |
| 3.2.1 | DAC resolution and voltage granularity | 33 |
| 3.2.2 | Analog input noise spectrum | 34 |
| 3.2.3 | Oversampling and input noise performance | 35 |
| 3.3 | Instrument calibration | 37 |
| 3.3.1 | Nanonis SC5 output calibration | 37 |
| 3.3.2 | Current-to-voltage amplifier calibration | 37 |

| | | |
|-------------------|--|-----------|
| 3.3.3 | Nanonis SC5 input offset adjustment | 38 |
| 3.3.4 | Nanonis SC5 input noise spectrum | 39 |
| 3.4 | Control software and automation | 39 |
| 4 | Device characterization | 41 |
| 4.1 | Room temperature measurements | 41 |
| 4.1.1 | Uniform gate sweep | 41 |
| 4.1.2 | Pinch-off measurements of individual gates | 43 |
| 4.2 | Cryogenic measurements | 43 |
| 4.2.1 | Uniform turn-on behavior | 43 |
| 4.2.2 | Output characteristics and saturation behavior | 45 |
| 4.2.3 | Pinch-off measurements of individual gates | 46 |
| 4.2.4 | Coulomb diamond spectroscopy | 49 |
| 4.2.5 | Field-effect mobility analysis | 51 |
| 5 | Noise measurements | 54 |
| 5.1 | Selection of stable Coulomb peaks | 54 |
| 5.2 | Converting time series to frequency spectra | 55 |
| 5.3 | Frequency-resolved noise characterization | 57 |
| 5.4 | Discussion | 61 |
| 6 | Conclusion | 66 |
| References | | 68 |

Chapter 1

Introduction

The burgeoning field of quantum computing holds transformative promise, poised to address computational challenges intractable for even the most powerful classical machines. This paradigm shift offers potential breakthroughs across diverse domains, including the development of provably secure communication protocols, the discovery of novel materials, and advancements in machine learning and optimization algorithms [1]. Central to this potential is the quantum bit, or qubit, which fundamentally departs from its classical counterpart. Unlike a classical bit restricted to definite states of 0 or 1, a qubit harnesses quantum mechanical phenomena such as superposition, allowing it to exist in a linear combination of states, e.g., $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ [2]. This unique property, alongside entanglement, enables quantum computers to process information in fundamentally new ways, facilitating the exploration of exponentially large computational spaces in parallel and thereby offering significant speedups for certain complex problems [3]. However, the formidable challenge lies in translating this theoretical power into practical utility. Achieving the full promise of quantum computing necessitates the engineering of physical qubit platforms that are not only scalable to large numbers of qubits but also maintain high degrees of quantum coherence and precise controllability [4, 5].

Within the landscape of solid-state quantum computing architectures, semiconductor quantum dots (QDs) have emerged as a particularly compelling platform. These nanoscale structures enable the precise electrostatic confinement of individual electrons or holes, thereby allowing quantum information to be encoded in either their charge or spin degrees of freedom. A significant advantage of semiconductor-based qubits lies in their compatibility with established silicon microfabrication technologies, offering a scalable pathway towards large-scale quantum processors through seamless integration with classical control electronics [6, 7].

However, a major obstacle to advancing semiconductor qubits is the omnipresent issue of charge noise. This noise originates from fluctuations in the local electrostatic environment [8], primarily driven by factors such as charge traps in nearby interfaces and dielectrics, as well as mobile charges. These fluctuations directly perturb the energy levels of the quantum dot, lead-

ing to qubit dephasing and operational errors. Despite extensive research efforts, the precise microscopic origins of charge noise remain challenging to fully characterize, and its effective mitigation continues to be a critical bottleneck for achieving the requisite qubit fidelity and coherence for fault-tolerant quantum computation.

This thesis experimentally investigates charge noise in semiconductor QDs. Specifically, this work characterizes the fundamental properties and charge noise of silicon-based QDs. Based on this characterization, I discuss the origins of the observed noise and analyze factors influencing its fluctuations. Furthermore, I developed a Python package for automated noise measurement, streamlining future research efforts. This study thus enhances the understanding of charge noise and its effects, aiming to inform the development of more robust semiconductor qubits and advance fault-tolerant, large-scale quantum computing.

The remainder of the thesis is structured as follows:

- Chapter 2 introduces the theoretical foundations of QD-based quantum computing, including charge transport, device architecture, qubit encoding, and the mechanisms by which charge noise influences qubit performance.
- Chapter 3 describes the experimental setup, including the cryogenic platform, voltage control and signal acquisition electronics, electronic instrument calibration, and experiment automation software.
- Chapter 4 presents a characterization of the QD devices, including their transport properties and suitability for noise measurements.
- Chapter 5 analyzes the experimental data and discusses models of charge noise and its spectral characteristics.
- Chapter 6 summarizes the key findings and outlines directions for future work.

Chapter 2

Theory

This chapter establishes the theoretical foundations essential for understanding the experimental work presented in this thesis. It begins by introducing the fundamental principles of QDs and the analytical tools employed to characterize charge transport within these systems. Subsequently, the role of the transistor as a host structure for QDs is discussed. The chapter then provides an overview of the two principal types of QD-based qubits—charge qubits and spin qubits—examining their distinct control mechanisms, coherence properties, and scalability attributes. The concluding section is dedicated to a detailed discussion of charge noise, which stands as the dominant source of decoherence in these systems and constitutes the central subject of this thesis.

2.1 Quantum dots and charge transport

2.1.1 Formation of quantum dots

QDs are nanoscale potential wells within semiconductor materials, typically sized on the order of 100 nm laterally [9, 10]. The strong spatial confinement in all three dimensions leads to discrete energy levels, hence their designation as “artificial atoms” [11]. While some QDs are created using etching or lithographic patterning, most quantum computing applications rely on gate-defined QDs [9]. These form when negative voltages applied to metallic surface electrodes patterned on a semiconductor heterostructure locally deplete the underlying two-dimensional electron gas (2DEG) [12].

Common material platforms for gate-defined QDs include GaAs/AlGaAs and silicon-based heterostructures. GaAs-based systems benefit from high-quality 2DEGs and well-established fabrication processes [13], but strong hyperfine interactions with host nuclear spins limit qubit coherence. Conversely, silicon-based devices offer key advantages such as weak spin-orbit coupling and the possibility of isotopic purification to suppress nuclear spin noise, enabling significantly longer coherence times [14, 15]. Specifically, Si/SiO₂ MOS structures, utilized

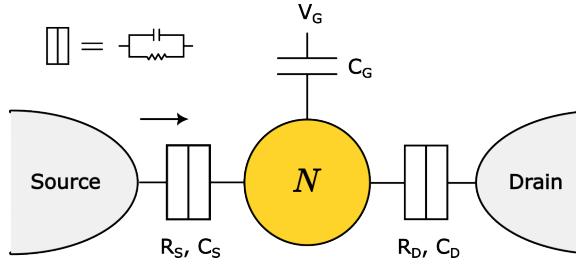


Figure 2.1: Schematic representation of a single QD coupled to source and drain leads via tunnel barriers. The central island represents the QD, confining N electrons and capacitively coupled to a gate electrode via capacitance C_G , controlled by gate voltage V_G . Source and drain leads connect through tunnel junctions, characterized by resistances R_S and R_D and capacitances C_S and C_D .

in this thesis, are attractive for their compatibility with standard CMOS fabrication and their ability to form deeper potential wells. However, the Si/SiO₂ interface typically contains a higher density of charge traps and oxide defects, consequently rendering charge noise a more prominent concern in these devices [16].

Therefore, understanding QD formation and electrostatics is essential for constructing robust qubit devices and diagnosing the impact of environmental disorder on their stability. A simple electrostatic model, depicted in Figure 2.1, captures this core physics: a QD capacitively coupled to a gate and tunnel-coupled to source and drain leads.

Within this model, the QD's total electrostatic potential is determined by surrounding voltages and their respective capacitive couplings. The total dot capacitance, $C_{\Sigma} = C_S + C_D + C_G$, defines the electrostatic potential as

$$V = \frac{Q_{\text{total}}}{C_{\Sigma}} = \frac{Q + C_S V_S + C_D V_D + C_G V_G}{C_{\Sigma}}. \quad (2.1)$$

Assuming zero source-drain bias ($V_S = V_D = 0$), the dot's electrostatic energy, dependent on the number of confined electrons N and the gate voltage V_G , is given by

$$U(N, V_G) = \int_0^{-Ne} V(Q, V_G) dQ = \frac{N^2 e^2}{2C_{\Sigma}} + eNC_G V_G. \quad (2.2)$$

The chemical potential, defined as the energy required to add an additional electron to the dot, is calculated as

$$\mu(N, V_G) = U(N, V_G) - U(N - 1, V_G) = E_C \left(N - \frac{1}{2} - \frac{C_G V_G}{e} \right). \quad (2.3)$$

Here, the charging energy $E_C = e^2/C_{\Sigma}$ quantifies the energy cost of adding a single electron. Following QD formation, its discrete energy levels and associated charging effects centrally determine electron transport, which the subsequent section will discuss.

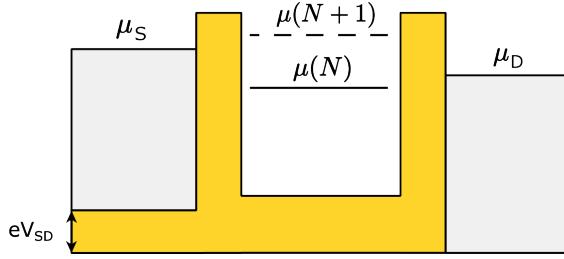


Figure 2.2: Illustration of Coulomb blockade in a QD, depicting discrete energy levels $\mu(N)$ and $\mu(N+1)$. Electron transport is blocked when $\mu(N) < \mu_S, \mu_D < \mu(N+1)$. The source-drain bias V_{SD} defines the bias window as $\mu_S - \mu_D = eV_{SD}$.

2.1.2 Coulomb blockade

A fundamental mechanism governing electron transport in QDs is the Coulomb blockade effect [17, 18]. As established in the previous section, adding an electron to the dot incurs a finite charging energy due to electrostatic repulsion from confined electrons [9]. Consequently, electron transport becomes quantized: an electron tunnels into the dot only when the applied bias and gate voltages compensate this energy cost.

At room temperature, thermal excitations typically smear out this quantization, leading to continuous current flow through the QD. Observing quantum effects such as Coulomb blockade therefore necessitates cooling the system to cryogenic temperatures, typically below 1 K. In this regime, the thermal energy $k_B T$ falls well below the charging energy E_C , suppressing thermal fluctuations and enabling clear observation of the Coulomb blockade.

As Figure 2.2 illustrates, the electrochemical potential $\mu(N)$ represents the energy required to add the N th electron to the dot. When $\mu(N) < \mu_S, \mu_D < \mu(N + 1)$, the dot becomes energetically isolated, preventing electrons from tunneling in or out, thus blocking current. This condition defines the Coulomb blockade regime. The blockade can be lifted by two primary mechanisms: tuning the gate voltage V_G to shift $\mu(N + 1)$ into the source-drain bias window, or increasing the bias voltage V_{SD} to widen this window. In both scenarios, a previously forbidden charge state becomes energetically accessible, enabling a single electron to tunnel into the dot.

A typical Coulomb blockade measurement involves sweeping the gate voltage while applying a small bias between the source and drain. When $\mu(N + 1)$ enters the bias window, an additional electron tunnels into the dot, resulting in a sharp conductance peak—termed a Coulomb peak. Increasing the source-drain bias reveals a series of Coulomb peaks [19]. Plotting these peaks as a function of source-drain bias and gate voltage generates a two-dimensional map known as the Coulomb diamond diagram, shown in Figure 2.3. This diagram powerfully visualizes and analyzes the Coulomb blockade regime. It presents the differential conductance $\partial I_{SD} / \partial V_{SD}$ as a function of gate voltage V_G and source-drain bias V_{SD} , demonstrating how electron transport is either suppressed or allowed based on the QD's electrochemical potential [20]. Regions of suppressed current form distinct diamond-shaped patterns, each

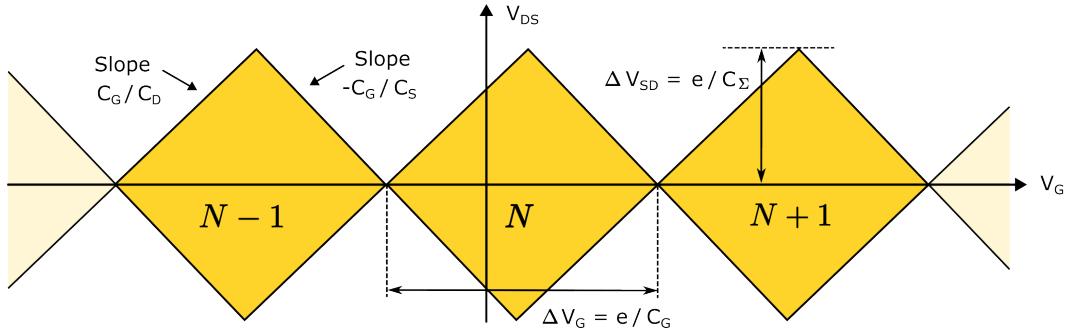


Figure 2.3: Coulomb diamond diagram depicting the differential conductance as a function of gate voltage V_G and source-drain bias V_{SD} . Diamond-shaped regions indicate Coulomb blockade, suppressing current due to the energy cost of adding or removing an electron. The diamonds' extent along the V_{SD} axis reflects the charging energy $E_C = e^2/C_\Sigma$, while their spacing in gate voltage $\Delta V_G = e/C_G$ reveals the strength of gate coupling. The slopes of the diamond edges are determined by the capacitive coupling to the source and drain, given by the ratios C_S/C_G and C_D/C_G , respectively.

representing a fixed electron number on the dot.

At the diamond edges, where either $\mu(N)$ or $\mu(N + 1)$ enters the bias window, single-electron tunneling becomes permissible. These transitions manifest as sharp changes in differential conductance, marking the boundaries between stable charge states. Conversely, within a diamond, the dot's energy levels lie outside the bias window defined by the source and drain chemical potentials μ_S and μ_D , rendering tunneling energetically forbidden.

The geometry of the Coulomb diamonds directly encodes key physical parameters of the QD. The horizontal spacing in gate voltage, corresponding to the separation between Coulomb peaks, determines the gate capacitance

$$\Delta V_G = \frac{e}{C_G}. \quad (2.4)$$

The vertical extent along the V_{SD} axis reflects the charging energy, defined as

$$\Delta V_{SD} = \frac{E_C}{e} = \frac{e}{C_\Sigma}. \quad (2.5)$$

Under symmetric bias (i.e., $V_S = +V_{SD}/2$, $V_D = -V_{SD}/2$), current commences when the electrochemical potential $\mu(N)$ aligns with either μ_S or μ_D . These transitions manifest as sloped lines defining the edges of each Coulomb diamond. Capacitive voltage division, as described by Equation (2.1), determines these slopes, which are given by:

$$\left. \frac{dV_{SD}}{dV_G} \right|_{\mu=\mu_S} = -\frac{C_G}{C_S}, \quad \left. \frac{dV_{SD}}{dV_G} \right|_{\mu=\mu_D} = \frac{C_G}{C_D}. \quad (2.6)$$

Another important parameter, the gate lever arm α , relates changes in gate voltage to energy

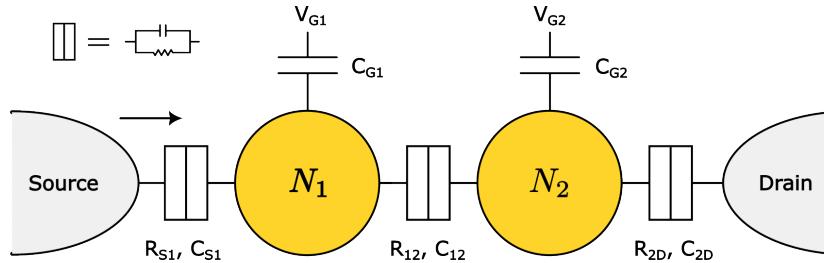


Figure 2.4: Schematic of a DQD system with two coupled dots, charge occupations N_1 and N_2 , connected in series between a source (S) and a drain (D). Each dot tunnel-couples to its respective lead via resistive and capacitive elements (e.g., R_{S1} and C_{S1} for the source lead and R_{2D} and C_{2D} for the drain lead). A central tunnel junction, characterized by resistance R_{12} and mutual capacitance C_{12} , connects the two dots. Gate voltages V_{G1} and V_{G2} control the dot energy levels through capacitive couplings C_{G1} and C_{G2} .

shifts in the QD levels:

$$\alpha = \frac{\Delta V_{SD}}{\Delta V_G} = \frac{C_G}{C_\Sigma}. \quad (2.7)$$

Beyond parameter extraction, Coulomb diamond diagrams also function as sensitive probes of device quality. While ideal systems exhibit regular, symmetric, and reproducible diamonds, practical devices often show distortions due to fabrication imperfections, material quality variations, and charge noise. For instance, fluctuating background charges can shift diamond positions, alter their shape over time, or induce irregular transitions.

2.1.3 Double quantum dot systems and honeycomb diagrams

Extending from the single-dot case, this section introduces the double quantum dot (DQD) system—a fundamental building block for scalable qubit architectures [21, 22]. DQD transport properties become more complex due to the interplay between the two dots’ quantized states. For basic understanding, we focus on the DQD system’s classical regime. Here, a double dot models as a network of capacitors and tunnel junctions, as illustrated in Figure 2.4. Charge occupations N_1 and N_2 denote the number of electrons on the left and right dots, respectively. Independent gate voltages V_{G1} and V_{G2} control each dot, modulating their electrochemical potentials via gate capacitances C_{G1} and C_{G2} . The dots tunnel-couple to the source and drain, and interact with each other via an interdot tunnel junction characterized by mutual capacitance $C_m = C_{12}$.

The charge stability diagram, shown in Figure 2.5, visualizes a DQD’s equilibrium charge configurations as a function of gate voltages V_{G1} and V_{G2} . Each hexagonal cell represents a distinct charge configuration (N_1, N_2) , with boundaries between cells indicating transitions between charge states.

To elucidate the diagram’s essential features, we again consider the classical regime and describe the system using a capacitance matrix model [9]. The total electrostatic energy, depen-

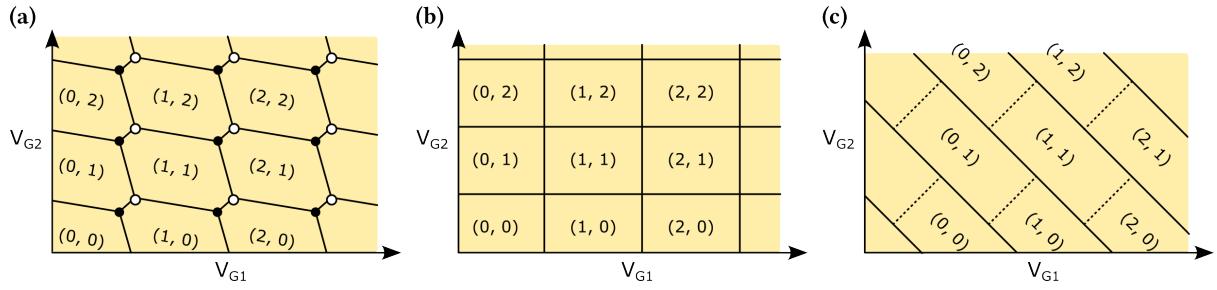


Figure 2.5: Charge stability diagrams depicting the equilibrium charge configurations (N_1, N_2) of a DQD as a function of gate voltages V_{G1} and V_{G2} . (a) Capacitive coupling between the two dots and to the gates gives rise to a characteristic honeycomb pattern. Each cell delineates a region of constant charge configuration. The charge transition lines separating these regions signify conditions where two charge states become degenerate, while triple points, where three regions intersect, represent points of three-state degeneracy, facilitating electron transport. (b) In the limit of negligible inter-dot coupling ($C_m \rightarrow 0$), the diagram forms a rectangular grid, reflecting decoupled charge states. (c) In the strong coupling regime ($C_m \rightarrow C_{\Sigma 1(2)}$), enhanced mutual capacitance tilts the boundaries, distorting the honeycomb pattern.

dent on the gate voltages and electron occupations on each dot, is given by

$$\begin{aligned} U(N_1, N_2; V_{G1}, V_{G2}) = & \frac{1}{2} N_1^2 E_{C_{\Sigma 1}} + \frac{1}{2} N_2^2 E_{C_{\Sigma 2}} + N_1 N_2 E_{C_m} \\ & - \frac{C_{G1} V_{G1}}{e} (N_1 E_{C_{\Sigma 1}} + N_2 E_{C_m}) \\ & - \frac{C_{G2} V_{G2}}{e} (N_1 E_{C_m} + N_2 E_{C_{\Sigma 2}}) + f(V_{G1}, V_{G2}), \end{aligned} \quad (2.8)$$

where $f(V_{G1}, V_{G2})$ is a background energy term independent of N_1 and N_2 . The electrochemical potentials, which determine the tunneling conditions for each dot, are given by

$$\mu_1(N_1, N_2; V_{G1}, V_{G2}) = \left(N_1 - \frac{1}{2} + \frac{C_{G1} V_{G1}}{e} \right) E_{C_{\Sigma 1}} + \left(N_2 + \frac{C_{G2} V_{G2}}{e} \right) E_{C_m}, \quad (2.9)$$

$$\mu_2(N_1, N_2; V_{G1}, V_{G2}) = \left(N_2 - \frac{1}{2} + \frac{C_{G2} V_{G2}}{e} \right) E_{C_{\Sigma 2}} + \left(N_1 + \frac{C_{G1} V_{G1}}{e} \right) E_{C_m}, \quad (2.10)$$

where the charging energies are defined as

$$E_{C_{\Sigma 1}} = e^2 \frac{C_{\Sigma 2}}{C_{\Sigma 1} C_{\Sigma 2} - C_m^2}, \quad E_{C_{\Sigma 2}} = e^2 \frac{C_{\Sigma 1}}{C_{\Sigma 1} C_{\Sigma 2} - C_m^2}, \quad E_{C_m} = e^2 \frac{C_m}{C_{\Sigma 1} C_{\Sigma 2} - C_m^2}. \quad (2.11)$$

At fixed gate voltages, a charge transition from (N_1, N_2) to $(N_1 + 1, N_2)$ corresponds to an energy change of $\mu_1(N_1 + 1, N_2) - \mu_1(N_1, N_2) = E_{C_{\Sigma 1}}$. Similarly, a transition from (N_1, N_2) to $(N_1, N_2 + 1)$ yields an energy change of $\mu_2(N_1, N_2 + 1) - \mu_2(N_1, N_2) = E_{C_{\Sigma 2}}$. The mutual charging energy manifests in the cross terms as $\mu_1(N_1, N_2 + 1) - \mu_1(N_1, N_2) = \mu_2(N_1 + 1, N_2) - \mu_2(N_1, N_2) = E_{C_m}$.

To further interpret the charge stability diagram, we examine the slopes of the charge transition lines in the V_{G1} - V_{G2} plane. These lines correspond to conditions where a dot's electro-

chemical potential aligns with the reservoir's Fermi level, permitting a charge to go through the dot. At fixed N_2 , the boundary between N_1 and $N_1 + 1$ charge states is defined by $\mu_1(N_1 + 1, N_2; V_{G1}, V_{G2}) = \mu_S$, where μ_S is the (constant) source chemical potential. This yields a linear relation between V_{G1} and V_{G2} with a slope of

$$\left. \frac{dV_{G2}}{dV_{G1}} \right|_{\Delta N_1=1, \Delta N_2=0} = -\frac{C_{G1}C_{\Sigma 2}}{C_{G2}C_m}, \quad (2.12)$$

Similarly, for transitions in N_2 at fixed N_1 , the slope is

$$\left. \frac{dV_{G2}}{dV_{G1}} \right|_{\Delta N_1=0, \Delta N_2=1} = -\frac{C_{G1}C_m}{C_{G2}C_{\Sigma 1}}. \quad (2.13)$$

These slopes determine the orientation of the cell boundaries in the charge stability diagram. In the limit $C_m \rightarrow 0$, the transition lines become axis-aligned, reducing the diagram to a square grid of decoupled dots (Figure 2.5(a)). As C_m increases, mutual capacitance introduces coupling between the dots, distorting the grid into a honeycomb pattern (Figure 2.5(b)). When C_m approaches $C_{\Sigma 1}$ or $C_{\Sigma 2}$, the cells skew, reflecting strong inter-dot interaction (Figure 2.5(c)).

This honeycomb structure not only diagnoses charge configurations but also underpins qubit implementations in DQD systems, a topic discussed in Section 2.3.

2.2 Transistor as hosts for quantum dots

Building on the capacitance model from the previous section, which elucidated how QD charge states arise from electrostatic interactions, this section transitions to the practical implementation of QDs. Realizing these quantum phenomena in devices necessitates a platform providing precise nanoscale electrostatic control and compatibility with large-scale integration. Metal-oxide-semiconductor field-effect transistors (MOSFETs), fundamental components of classical electronics, offer such a platform and serve as widely used hosts for gate-defined QDs.

Gate-defined QD systems employ similar gate structures to locally modulate the potential landscape and confine individual electrons. Rather than enabling continuous current flow, these gate electrodes create electrostatic wells and tunnel barriers, segmenting the inversion layer or 2DEG into isolated charge islands [23]. Although the resulting system enters the quantum regime, classical electrostatics still govern the underlying control [24].

Figure 2.6 illustrates a representative n-channel MOSFET structure. The fundamental gate control mechanism in MOSFETs, modulation of surface potential to form conductive paths, directly underpins the electrostatic confinement and barrier control essential for QD architectures.

This section elucidates classical transistor physics as a foundation for QD engineering. The

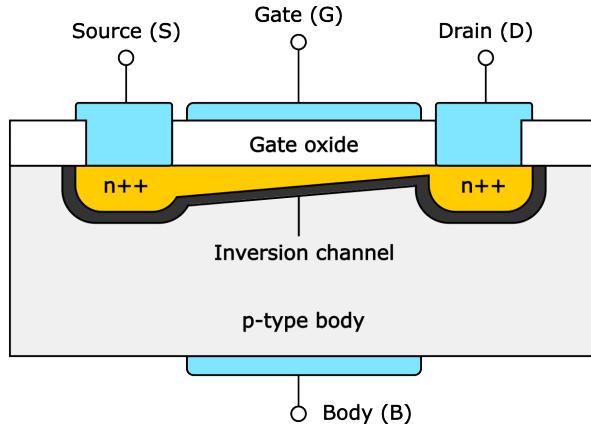


Figure 2.6: Cross-sectional schematic of an n-channel MOSFET. A positive gate voltage induces an inversion channel in the p-type body, enabling electron flow from the n++ source (S) to the n++ drain (D). The gate (G) controls this conductive path by modulating the surface potential through the gate oxide. The body (B) terminal controls threshold voltage and suppresses short-channel effects.

following subsections review key aspects of MOSFET operation (including transport regimes, carrier dynamics, and short-channel effects) that directly define, tune, and enable understanding of QDs in semiconductor platforms.

2.2.1 MOSFET transport regimes and characteristics

Cutoff, linear, and saturation regimes

The current-voltage characteristics of a MOSFET describe how the drain current I_{DS} responds to changes in gate voltage V_G and source-drain bias V_{DS} . These characteristics define three distinct operating regimes: cutoff, linear, and saturation.

In the cutoff regime, where the gate voltage falls below the threshold voltage $V_G < V_{th}$, no inversion channel forms, and the drain current remains negligible. This state directly analogizes to a QD system with a completely closed tunnel barrier, suppressing electron tunneling and establishing the Coulomb blockade regime.

As the gate voltage exceeds the threshold, the device enters the linear (or triode) regime, forming a conductive channel that allows current flow between the source and drain. In this regime, for small V_{DS} the drain current increases approximately linearly with V_G , expressed as

$$I_{DS} = K_n \left[(V_G - V_{th})V_{DS} - \frac{1}{2}V_{DS}^2 \right], \quad (2.14)$$

where $K_n = \mu C_i W/L$ encompasses carrier mobility μ , oxide capacitance per unit area C_i , and channel width W and length L . The term $V_G - V_{th}$ is commonly termed the gate overdrive voltage, quantifying the effective voltage modulating channel carrier density. In QD systems, this regime parallels a partially opened tunnel barrier, where gate-defined constrictions initiate

current flow through a confined region.

When V_{DS} increases further such that $V_{DS} > V_G - V_{th}$, the MOSFET enters the saturation regime. Here, the channel pinches off near the drain end, and the current saturates, becoming largely independent of V_{DS} . The saturated drain current is

$$I_{DS}^{\text{sat}} = \frac{1}{2}K_n(V_G - V_{th})^2. \quad (2.15)$$

This pinch-off condition exemplifies how gate voltages create sharp potential drops. In QD architectures, such sharp potential changes are critical for defining tunable tunnel barriers between dots or between a dot and a reservoir. The precise adjustment of these gate voltages, combined with the quantum nature of QDs, enables electron transport quantization and control at the single-electron level.

Transconductance and gate sensitivity

A key performance metric in both classical and quantum systems is the transconductance, g_m , which quantifies the drain current's sensitivity to gate voltage changes:

$$g_m = \frac{\partial I_{DS}}{\partial V_G}. \quad (2.16)$$

In the saturation regime, Equation (2.15) yields the transconductance $g_m = K_n(V_G - V_{th})$. Thus, g_m increases linearly with the gate overdrive voltage. In QD applications, high transconductance reflects strong gate coupling to the electrostatic potential, enabling precise tuning of tunnel barriers and energy levels. Such control is essential for defining sharp charge transitions, stable qubit operation, and high-fidelity readout.

Subthreshold swing and gate efficiency

Another important figure of merit is the subthreshold swing (SS), which characterizes the gate voltage's effectiveness in modulating the drain current within the subthreshold regime, where $V_G < V_{th}$ and the MOSFET is nominally off. In this regime, current increases exponentially with gate voltage due to thermally activated carrier transport. The subthreshold swing defines the required change in gate voltage to increase the drain current by one order of magnitude:

$$\text{SS} = \frac{dV_G}{d \log_{10}(I_{DS})} = \ln(10) \frac{k_B T}{e} \left(1 + \frac{C_d}{C_{\text{ox}}}\right), \quad (2.17)$$

where k_B is the Boltzmann constant, T is the temperature, e is the elementary charge, C_{ox} is the gate oxide capacitance per unit area, and C_d is the depletion layer capacitance. A smaller SS indicates stronger gate control and sharper switching behavior.

At room temperature ($T = 300$ K), the theoretical limit for SS in an ideal MOSFET approximates 60 mV/decade. Real devices, however, often exceed this value due to non-idealities

such as interface traps, gate leakage, or parasitic capacitances.

Although a classical concept, subthreshold swing holds significant implications for QD systems. Specifically, the ability to induce sharp current transitions with small gate voltage changes proves essential for cleanly defining charge states and controlling tunnel barriers. Conversely, devices with poor electrostatic efficiency (high SS) may exhibit smeared or unstable transitions, directly impairing qubit initialization and readout fidelity.

2.2.2 Carrier transport mechanisms

Carrier transport in semiconductors results from the interplay between externally applied electric fields and internal scattering processes. A key quantity characterizing this transport is the carrier mobility, which reflects charge carriers' ability to move through a material under an electric field. High mobility proves essential for fast and efficient transistor switching. It is defined as

$$\mu = \frac{v_d}{E}, \quad (2.18)$$

where v_d is the drift velocity of the carriers and E is the electric field across the channel. At the device level, mobility can also be extracted from the transconductance using the relation

$$\mu = \frac{1}{C_i} \cdot \frac{L}{W} \cdot \frac{1}{V_{SD}} \cdot \frac{dI_{SD}}{dV_G}, \quad (2.19)$$

where L and W are the channel length and width, respectively, and C_i is the gate capacitance per unit area. The term dI_{SD}/dV_G represents the transconductance in the linear regime. One can estimate the gate capacitance per unit area as $C_i = \epsilon_r \epsilon_0 / t_{ox}$, where ϵ_r is the relative permittivity of the gate oxide, ϵ_0 is the vacuum permittivity, and t_{ox} is the oxide thickness.

The scattering processes that impede carrier motion can be further understood through the concept of the mean free path l . The mean free path represents the average distance a carrier travels between successive scattering events. A longer mean free path generally correlates with higher mobility, as carriers can accelerate for longer periods under an electric field before being scattered. In many semiconductor devices, particularly at lower temperatures or in high-quality materials, the mean free path can become comparable to or even exceed the device dimensions. The relationship between mobility and mean free path can often be expressed as

$$\mu = \frac{el}{m^* v_{th}}, \quad (2.20)$$

where e is the elementary charge, m^* is the effective mass of the carrier, and v_{th} is the thermal velocity for semiconductors, which can be calculated by $v_{th} = \sqrt{3k_B T/m^*}$.

2.2.3 Short-channel effects

As transistor dimensions scale down, short-channel effects gain increasing significance. These effects emerge when the channel length approaches key electrostatic or transport length scales, such as the depletion width or mean free path, leading to a breakdown in ideal gate control and the manifestation of parasitic behaviors.

In long-channel MOSFETs, the gate voltage primarily controls the potential barrier regulating carrier injection from the source. In short-channel devices, however, the drain voltage can also significantly influence the source-side barrier. As drain bias increases, it lowers the source energy barrier, enabling carriers to tunnel through even below threshold. This phenomenon, drain-induced barrier lowering (DIBL), effectively reduces the threshold voltage and increases off-state leakage. DIBL is typically quantified by

$$\text{DIBL} = -\frac{V_{\text{th}}(V_{\text{DS}}^{\text{high}}) - V_{\text{th}}(V_{\text{DS}}^{\text{low}})}{V_{\text{DS}}^{\text{high}} - V_{\text{DS}}^{\text{low}}}, \quad (2.21)$$

where $V_{\text{th}}(V_{\text{DS}})$ denotes the threshold voltage extracted under a given drain bias. A larger DIBL value reflects stronger short-channel effects and weaker gate control.

Similar electrostatic challenges manifest in QD architectures. Because QDs typically rely on multiple, closely spaced gate electrodes for definition, capacitive crosstalk between these gates can degrade local electrostatic precision. Tuning one gate to control a tunnel barrier or dot potential may unintentionally perturb adjacent regions, destabilizing charge states or affecting tunnel rates. These issues mirror DIBL, where a distant terminal (e.g., the drain) influences a region (e.g., the source barrier) that ideally demands independent control.

Channel length modulation (CLM) represents another important consequence of channel length reduction. In an ideal long-channel MOSFET, the drain current saturates and remains constant with increasing V_{DS} once the device enters saturation. In short-channel devices, however, the effective channel length decreases as V_{DS} increases, facilitating additional carrier injection from the source. Consequently, the current continues to rise even in saturation. This non-ideal behavior is captured by modifying the drain current expression to include a linear correction term

$$I_{\text{DS}}^{\text{sat}} = \frac{1}{2}K_n(V_G - V_{\text{th}})^2(1 + \lambda V_{\text{DS}}), \quad (2.22)$$

where $\lambda = 1/V_A$ is the CLM parameter and V_A is the Early voltage. In practice, λ is often approximated as $\lambda \approx -0.1/L [\text{V}^{-1}]$, where L is the channel length in micrometers. Figure 2.7 illustrates this behavior.

Although QD devices do not rely on classical drain current, the physical origin of CLM, stemming from electrostatic influence extending beyond the immediate gate region, has a clear analogue. In QD systems, nearby gates or electrodes can unintentionally modulate the confinement potential and tunnel barriers, particularly with closely spaced dots. This long-range

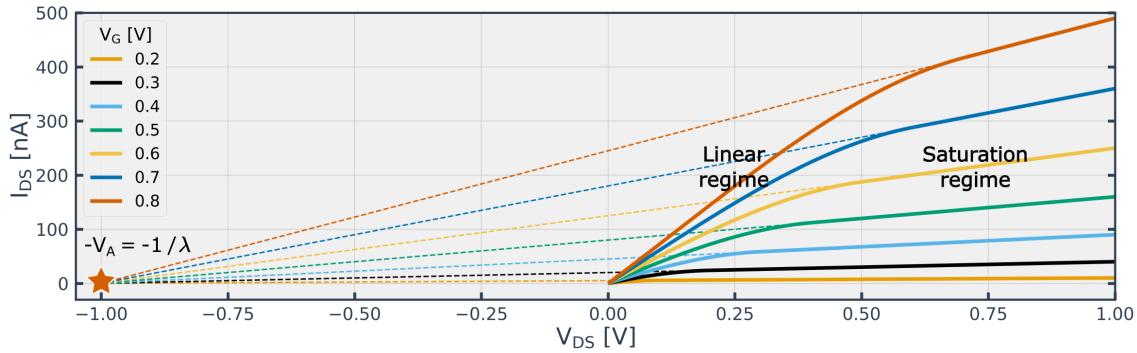


Figure 2.7: Illustration of CLM in a short-channel MOSFET. Output characteristics I_{DS} versus V_{DS} are shown for various gate voltages. Ideally, current saturates and forms a flat curve beyond the linear region. Due to CLM, the current continues to increase with V_{DS} , producing a non-zero output conductance. Dashed lines extrapolate each curve to intercept the V_{DS} -axis at $-V_A = -1/\lambda$, defining the Early voltage. A smaller V_A (larger λ) indicates stronger CLM.

capacitive coupling can reduce local gate control precision and destabilize charge configurations.

In summary, classical semiconductor devices like MOSFETs provide the foundational electrostatic and transport principles underpinning gate-defined QD systems. The ability to locally shape potential landscapes (e.g., defining tunnel barriers, reservoirs, and confinement regions) inherits directly from transistor physics. As device dimensions shrink and temperature decreases, quantum effects such as energy level quantization, tunneling, and Coulomb interactions begin to dominate system behavior.

2.3 Qubit implementation within quantum dots

QDs provide a natural and highly controllable platform for encoding quantum information in solid-state systems. Building on the electrostatic confinement techniques and device physics introduced in the previous sections, this section examines the physical principles and practical approaches for implementing qubits within these structures.

Two widely studied approaches for qubit implementation in gate-defined QDs are spin qubits and charge qubits, distinguished by their underlying physical principles. Spin qubits encode quantum information in the spin degree of freedom of one or more electrons, leveraging the intrinsic angular momentum of charge carriers. In contrast, charge qubits utilize the spatial charge distribution of electrons across multiple dots to define computational basis states [25]. These fundamental differences manifest in distinct Hamiltonians, control mechanisms, and sensitivities to various environmental noise sources. A visual comparison of these qubit implementations is presented in Figure 2.8.

In practice, many experimental implementations of semiconductor qubits combine features of both spin and charge degrees of freedom [26, 14]. These hybrid qubit designs aim to leverage

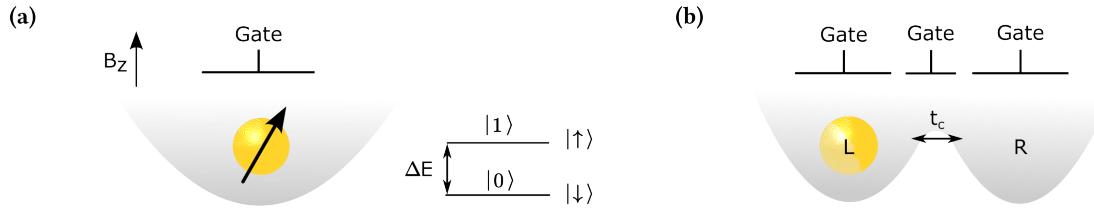


Figure 2.8: Comparison between single-spin and charge qubit implementations. (a) A single-spin qubit is formed by a single electron confined in a QD, with spin states $|\uparrow\rangle$ and $|\downarrow\rangle$ split by a magnetic field B_z . (b) A charge qubit consists of an electron localized in a DQD potential, with tunneling amplitude t_c enabling transitions between the left $|L\rangle$ and right $|R\rangle$ sites.

the fast electrical control characteristic of charge-based systems while preserving the longer coherence times typically associated with spin-based systems. The following subsections will introduce the operational principles, relevant Hamiltonians, and inherent trade-offs associated with each major qubit type.

2.3.1 Spin qubits

Spin qubits can be further classified into single-spin and multi-spin qubits, depending on how the spin degrees of freedom are distributed across multiple dots. Examples of multi-spin architectures include singlet-triplet (ST) qubits (formed by two electrons in a double dot) and exchange-only (EO) qubits (formed by three electrons in a triple dot) [27, 28].

Single-spin qubits

Single-spin qubits, often referred to as Loss-DiVincenzo (LD) spin qubits, encode quantum information in the spin-up $|\uparrow\rangle$ and spin-down $|\downarrow\rangle$ states of a single electron confined within a QD [29]. This represents the most elementary realization of a spin qubit.

To manipulate the spin state, a static magnetic field is typically applied along the z -axis to define the qubit quantization axis and split the spin states via the Zeeman effect. An oscillating magnetic field, typically applied along the x -axis, then drives coherent spin rotations. The dynamics of such a qubit are governed by the Zeeman Hamiltonian:

$$H = g\mu_B \frac{1}{\hbar} \vec{B} \cdot \hat{S} = \frac{1}{2} g\mu_B (B_z \sigma_z + B_x \sigma_x \cos(\omega t + \phi)), \quad (2.23)$$

where ω and ϕ denote the frequency and phase of the oscillating field, g is the Landé g -factor (a dimensionless quantity relating the magnetic moment of an electron to its spin angular momentum), and μ_B is the Bohr magneton. The value of g is material-dependent, for instance, $g \approx -2$ in silicon [30] and $g \approx -0.44$ in GaAs [31].

The first term, $H_z = \frac{1}{2} g\mu_B B_z \sigma_z$, describes the Zeeman splitting between the $|\uparrow\rangle$ and $|\downarrow\rangle$ states due to the static magnetic field B_z . This energy separation, $\Delta E_z = |g|\mu_B B_z$, defines the qubit's

Larmor frequency (or resonance frequency) $f_q = \Delta E_z/h$, which typically falls in the 5-50 GHz range for silicon spin qubits [26].

The second term, $H_{xy} = \frac{1}{2}g\mu_B B_x \sigma_x \cos(\omega t + \phi)$, introduced by the oscillating field B_x along the x -axis, enables coherent spin control. When the drive frequency ω matches the qubit's resonance frequency $\omega_q = g\mu_B B_z/\hbar$ (i.e., on-resonance driving), the fast-oscillating term averages out in the rotating frame approximation. Under this condition, the effective Hamiltonian simplifies to

$$H_{\text{eff}} = \frac{1}{2}g\mu_B (B_x \cos \phi \sigma_x + B_x \sin \phi \sigma_y), \quad (2.24)$$

which describes a rotation of the spin state in the x - y plane of the Bloch sphere with an amplitude proportional to B_x . The eigenenergies of H_{eff} are $E_{\pm} = \pm|g|\mu_B B_x/2$, yielding an energy splitting $\Delta E = |g|\mu_B B_x$. From this splitting, the Rabi frequency, which dictates the speed of coherent operations, is defined as:

$$f_R = \frac{\Delta E}{h} = \frac{|g|\mu_B B_x}{h}. \quad (2.25)$$

In conventional electron spin resonance (ESR), the transverse driving field B_x is applied via a microwave antenna. A typical π -pulse in ESR results in gate speeds of 0.5-2 MHz, corresponding to pulse durations of 0.5-2 μ s [32]. Faster gate operations can be achieved using electric dipole spin resonance (EDSR), where spin control is driven by oscillating electric fields coupled through spin-orbit interaction, allowing operation at frequencies exceeding 10 MHz [33].

The choice between ESR and EDSR for single-spin qubit control is largely determined by the host material properties. In GaAs, which features relatively strong intrinsic spin-orbit coupling, EDSR is particularly effective and widely used. Silicon, by contrast, exhibits inherently weak spin-orbit interaction. While this limits EDSR efficiency, it results in significantly longer spin coherence times, making silicon an attractive platform. As a result, silicon-based qubits typically employ ESR, often enhanced with micromagnets for localized field gradients, whereas GaAs and other III-V semiconductors favor EDSR for faster control.

The readout of single-spin qubits typically relies on spin-to-charge conversion, where the spin state is mapped onto a detectable charge configuration. This is commonly achieved by leveraging the Pauli exclusion principle in a DQD system, a technique known as Pauli spin blockade (PSB) [34]. To perform a readout, the electron is momentarily allowed to tunnel from the qubit dot into an adjacent “readout” dot, often at energies tailored to the spin state. For instance, if the qubit electron is in the $|\uparrow\rangle$ state, it may be allowed to tunnel onto a readout dot already occupied by another electron in the $|\downarrow\rangle$ state, forming a spin singlet. If the qubit electron is in the $|\downarrow\rangle$ state, tunneling may be blocked if the readout dot is already occupied by a $|\downarrow\rangle$ electron, due to PSB. The presence or absence of an electron in the readout dot, indicative of the original spin state, is then detected using a nearby charge sensor, such as a quantum point contact (QPC) or a single-electron transistor (SET) [34]. These charge sensors are highly sensitive electrometers that measure changes in the local electrostatic environment caused

by the presence or absence of a single electron, translating this into a measurable current or voltage change. Readout fidelities for single-spin qubits in silicon have reached impressive levels, exceeding 99% [35].

When extended to multiple single-spin qubits, the total Hamiltonian describing their interaction can be expressed as:

$$H = \frac{1}{4} \sum_{\langle i,j \rangle} J_{ij}(t) \boldsymbol{\sigma}_i \cdot \boldsymbol{\sigma}_j + \frac{1}{2} \sum_i g\mu_B \vec{B}_i \cdot \boldsymbol{\sigma}_i, \quad (2.26)$$

where $J_{ij}(t)$ is the time-dependent exchange coupling between neighboring qubits i and j . This exchange coupling provides the mechanism for controllable two-qubit gates, enabling entanglement and multi-qubit operations [36]. Crucially, the strength of the exchange coupling can be precisely tuned via gate voltages that control the tunneling barrier between adjacent quantum dots [37].

Singlet-triplet qubits

ST qubits utilize the combined spin states of two electrons confined within a DQD. Their combined spin states span a four-dimensional Hilbert space, comprising one singlet state, $|S\rangle = (|\uparrow\downarrow\rangle - |\downarrow\uparrow\rangle)/\sqrt{2}$, with total spin $S = 0$ and spin projection $S_z = 0$. This singlet state is typically the ground state of the system, influenced by exchange and Coulomb interactions. The Hilbert space also includes three triplet states with total spin $S = 1$: the unpolarized triplet $|T_0\rangle = (|\uparrow\downarrow\rangle + |\downarrow\uparrow\rangle)/\sqrt{2}$, which also has $S_z = 0$; and the polarized triplets $|T_+\rangle = |\uparrow\uparrow\rangle$ and $|T_-\rangle = |\downarrow\downarrow\rangle$, with $S_z = +1$ and $S_z = -1$, respectively. These polarized triplet states are generally higher in energy due to Zeeman splitting.

In ST qubits, quantum information is encoded in the $\{|S\rangle, |T_0\rangle\}$ subspace, with logical states often defined as $|0_L\rangle = |S\rangle$ and $|1_L\rangle = |T_0\rangle$. A key advantage of this encoding is that these two states share the same total spin projection $S_z = 0$. This property makes them robust against uniform magnetic field fluctuations across the DQD, as such noise primarily affects states with different S_z , thus forming a decoherence-protected subspace [37].

Qubit control is achieved using two primary parameters: the exchange interaction $J(\epsilon)$, which dictates the energy splitting between singlet and triplet states and depends on the interdot detuning ϵ , and the magnetic field gradient ΔB_z between the two dots [38]. The effective Hamiltonian in the $\{|S\rangle, |T_0\rangle\}$ subspace is given by

$$H = \frac{1}{2}J(\epsilon)\sigma_z + \frac{1}{2}g\mu_B\Delta B_z\sigma_x, \quad (2.27)$$

where $J(\epsilon)$ enables rotations about the z -axis (e.g., through pulsing the detuning parameter ϵ), and ΔB_z enables x -axis control. It is important to distinguish this exchange interaction, which controls the relative phase of the singlet and triplet states within the DQD, from the

inter-qubit exchange coupling J_{ij} introduced for multiple single-spin qubits. The magnetic field gradient ΔB_z can be realized using micromagnets integrated on-chip [39] or via dynamic nuclear spin polarization in materials such as GaAs [37].

Initialization of ST qubits is typically achieved by pulsing the gate voltages to the (0, 2) charge configuration (i.e., zero electrons in the left dot, two in the right), where only the singlet state is energetically accessible for the two electrons. Readout is then performed using PSB in the (1, 1) charge configuration, which discriminates between the $|S\rangle$ and $|T_0\rangle$ states based on their subsequent charge occupation. Specifically, a singlet state allows an electron to tunnel out to a reservoir, while a triplet state blocks this tunneling due to spin parity conservation and the Pauli exclusion principle, leading to a measurable charge difference [37].

Coherent control of ST qubits has been demonstrated with gate speeds in the tens of megahertz and coherence times on the order of microseconds [40]. However, their performance is fundamentally limited by charge noise, which strongly couples to the detuning axis ϵ and thereby destabilizes the exchange interaction $J(\epsilon)$. Additionally, unwanted leakage to the polarized triplet states $|T_+\rangle$ and $|T_-\rangle$, which lie outside the logical subspace, must be suppressed by ensuring a sufficiently large Zeeman splitting between the singlet and triplet states.

Exchange-only qubits

EO qubits are implemented by confining three electron spins in a linear triple quantum dot (TQD) system. Unlike single-spin or ST qubits, EO qubits encode quantum information entirely within the total spin $S = 1/2$, spin projection $S_z = 1/2$ subspace of the three-electron system [41]. This unique encoding enables full single-qubit control solely through electrically tunable exchange interactions, eliminating the need for applied magnetic field gradients or resonant microwave fields.

A common choice of logical basis states for EO qubits is the two-fold degenerate doublet manifold within the $S = 1/2, S_z = 1/2$ subspace:

$$|0_L\rangle = \frac{1}{\sqrt{2}}(|\uparrow\downarrow\uparrow\rangle - |\downarrow\uparrow\uparrow\rangle), \quad |1_L\rangle = \frac{1}{\sqrt{6}}(|\uparrow\downarrow\uparrow\rangle + |\downarrow\uparrow\uparrow\rangle - 2|\uparrow\uparrow\downarrow\rangle). \quad (2.28)$$

These states are specifically chosen to lie entirely within the computational subspace and remain orthogonal to higher-spin leakage states, such as the quartet states. The system Hamiltonian describes the exchange interactions between neighboring spins, where the time dependence for control arises from dynamically tuning the interdot detuning parameters $\epsilon(t)$ via gate voltages:

$$H = \frac{1}{2}J_{12}(\epsilon)\mathbf{S}_1 \cdot \mathbf{S}_2 + \frac{1}{2}J_{23}(\epsilon)\mathbf{S}_2 \cdot \mathbf{S}_3, \quad (2.29)$$

where $J_{12}(\epsilon)$ and $J_{23}(\epsilon)$ are the exchange couplings between spin 1 and 2, and spin 2 and 3, respectively, precisely controlled by the gate-defined detuning parameters. By pulsing these exchange couplings in specific sequences, universal single-qubit gates can be implemented

rapidly and without leaving the logical subspace.

Since EO qubits rely entirely on electrical control of gate voltages, they are particularly well-suited for integration into densely packed qubit arrays and offer compatibility with cryogenic classical control hardware, simplifying qubit addressing and scaling. However, their performance faces limitations primarily from charge noise, which directly affects the stability and precision of the exchange interactions, and from unwanted leakage to non-computational spin states, especially during rapid exchange pulses. This leakage can reduce gate fidelity and requires careful pulse engineering.

2.3.2 Charge qubits

Charge qubits encode quantum information in the spatial position of a single electron confined within a DQD. The computational basis states are typically defined by the localized charge configurations $|L\rangle$ and $|R\rangle$, corresponding to the electron predominantly occupying the left or right quantum dot, respectively. In this localized basis, the system is governed by the effective two-level Hamiltonian:

$$H = \frac{\epsilon}{2} \sigma_z + t_c \sigma_x, \quad (2.30)$$

where ϵ represents the energy detuning between the two dots, adjusted by gate voltages, and t_c is the tunnel coupling amplitude between the dots, which controls the rate of coherent electron tunneling.

The corresponding eigenenergies of this Hamiltonian are given by:

$$E_{\pm} = \pm \frac{1}{2} \sqrt{\epsilon^2 + 4t_c^2}, \quad (2.31)$$

resulting in a total energy splitting $\Delta E = \sqrt{\epsilon^2 + 4t_c^2}$ between the eigenstates. A crucial operating point is the charge degeneracy point (also known as the “sweet spot”), where $\epsilon = 0$. At this point, the qubit energy gap simplifies to $\Delta E = 2t_c$, and the system becomes first-order insensitive to fluctuations in ϵ , since $\partial(\Delta E)/\partial\epsilon = 0$. This insensitivity to detuning noise is a key advantage of operating at the sweet spot, offering improved resilience to low-frequency charge noise, which is a common source of decoherence.

The corresponding eigenstates $|E_{\pm}\rangle$ are given by:

$$|E_{\pm}\rangle = \cos\left(\frac{\theta}{2}\right) |L\rangle \pm \sin\left(\frac{\theta}{2}\right) |R\rangle, \quad (2.32)$$

where the mixing angle θ is defined by $\tan \theta = 2t_c/\epsilon$. These eigenstates illustrate the continuum between two regimes: the localized regime (when $|\epsilon| \gg t_c$), where they approximate the basis states $|L\rangle$ and $|R\rangle$, and the delocalized regime (at or near $|t_c| \gg |\epsilon|$), where they form symmetric and antisymmetric superpositions, specifically $|E_{\pm}\rangle = \frac{1}{\sqrt{2}}(|L\rangle \pm |R\rangle)$ at the sweet spot.

Initialization of a charge qubit is typically achieved by pulsing the gate voltages to a large positive or negative detuning ($\epsilon \gg 0$ or $\epsilon \ll 0$), which favors one of the localized charge states (e.g., $|L\rangle$ or $|R\rangle$) and allows for charge relaxation into that state. Readout is then performed by mapping the qubit state to a distinct charge configuration that can be detected by a nearby charge sensor. By pulsing the detuning, the electron's position causes a measurable change in the current through the charge sensor, providing a direct measurement of the qubit's charge state.

Charge qubits support very fast single-qubit gate operations due to their strong electric dipole moments, which allow for direct manipulation using high-frequency voltage pulses. However, this same strong electric-field sensitivity makes them particularly vulnerable to charge noise, which directly couples to the detuning parameter ϵ , significantly limiting their coherence times to typically nanoseconds or, at best, a few microseconds. Despite these limitations in coherence, charge qubits play a key role in the development of high-speed quantum control protocols and serve as a valuable platform for hybrid integration with other qubit types, often being used as fast intermediaries for spin-based gates or for charge sensing itself.

2.3.3 Summary of qubit performance

Table 2.1 provides a comprehensive summary of the key trade-offs between various spin and charge qubit implementations, evaluated in terms of their physical realization, control mechanisms, coherence, gate speed, scalability, and readout methods. Generally, spin-based qubits, such as single-spin, ST, and EO qubits, offer intrinsically longer coherence times due to their reduced coupling to environmental charge fluctuations. In contrast, charge-based qubits enable significantly faster gate operations but are inherently more susceptible to charge noise, which severely limits their coherence. ST and EO qubits, while spin-based in their encoding, are distinct in their reliance on electrical control of exchange interactions. This makes them susceptible to charge noise, albeit less so than pure charge qubits, granting them valuable hybrid characteristics, balancing fast electrical control with spin-coherence benefits.

The optimal choice of qubit architecture for a given quantum processor ultimately depends on the specific demands of the application, including the required balance between gate speed, fidelity, noise tolerance, and the overall scalability roadmap [42].

2.4 Charge noise in quantum dot systems

Having discussed the implementation and control mechanisms of semiconductor qubits, it becomes apparent that one of the most significant sources of decoherence stems from charge noise, primarily owing to the qubits' inherent sensitivity to electrostatic potentials. Charge noise refers to fluctuations in the local electrostatic environment, which can significantly alter the energy levels, control parameters, and ultimately, the coherence properties of these

Table 2.1: Comparison of spin and charge qubit implementations in terms of physical realization, control, coherence, gate speed, scalability, and readout. Charge noise is a dominant decoherence source for all electrically controlled qubits.

| | Single-spin qubit | Singlet-triplet qubit | Exchange-only qubit | Charge qubit |
|-----------------------------|--|---|---|--|
| Physical realization | Single-electron spin in a QD | Two-electron spin in a DQD | Three-electron spin in a TQD | Single-electron position in a DQD |
| Control mechanism | Magnetic resonance (ESR/EDSR) | Electric field (detuning) and magnetic field gradient | Electric field (exchange) | Electric field (detuning) |
| Coherence time | Milliseconds (Si); limited by hyperfine, spin-orbit, magnetic noise | Microseconds; limited by charge, magnetic field, and detuning noise | Microseconds; limited by charge noise | Nanoseconds; limited by strong charge noise |
| Gate speed | 0.5–100 MHz (ESR); >10 MHz (EDSR) | ~10–100 MHz | ~100 MHz–GHz | ≥10 GHz |
| Scalability | Moderate; challenge due to individual magnetic field/microwave lines | High; electrical control facilitates scaling | High; all-electrical control for compact arrays | Moderate; limited by strong decoherence despite electrical control |
| Readout method | Spin-to-charge conversion (PSB) | Spin-to-charge conversion (PSB) | Spin-to-charge conversion (PSB) | Direct charge state sensing |

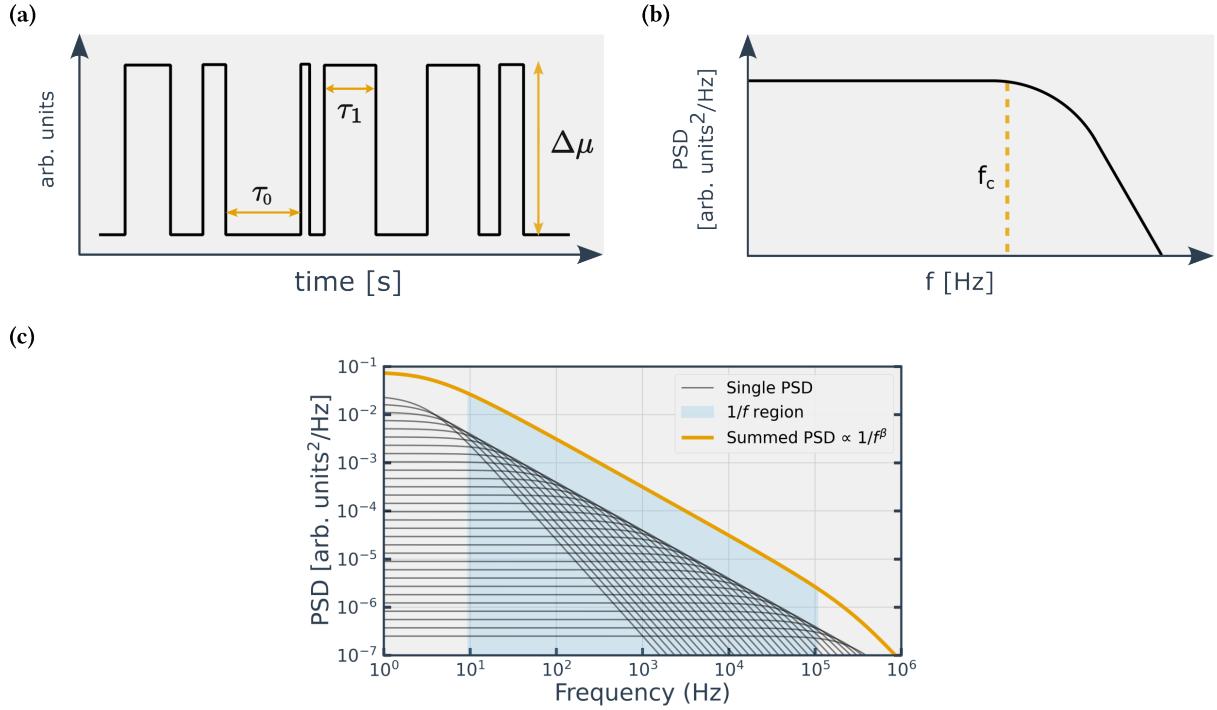


Figure 2.9: (a) Schematic of a RTS generated by a single TLF, characterized by its amplitude $\Delta\mu$ and dwell times τ_0 (state 0) and τ_1 (state 1). (b) PSD of a single TLF, exhibiting a Lorentzian spectrum with a characteristic cutoff frequency f_c [43]. (c) Simulated total PSD resulting from the superposition of multiple TLFs. Each TLF contributes a Lorentzian spectrum (gray lines) with a characteristic time constant τ logarithmically distributed between $1 \mu\text{s}$ and 0.1 s , summing to produce an overall $1/f^\beta$ spectrum (orange).

sensitive quantum systems. In this section, we delve into the microscopic origins of charge noise and detail how it couples to and impacts the performance of semiconductor qubits.

2.4.1 Two-level fluctuators

The microscopic origin of charge noise in solid-state devices is commonly attributed to ensembles of two-level fluctuators (TLFs) [8]. These are individual defects or charge traps, often located in amorphous regions such as oxides, semiconductor-insulator interfaces, or within the substrate. As schematically illustrated in Figure 2.9(a), each TLF switches randomly between two distinct charge states, generating a bistable electrical signal known as a random telegraph signal (RTS). For a single TLF characterized by average dwell times τ_0 and τ_1 in its two states, the corresponding power spectral density (PSD) of the induced potential fluctuation is given by

$$S(f) = \frac{2\Delta\mu^2}{(\tau_0 + \tau_1) \left[\left(\frac{1}{\tau_0} + \frac{1}{\tau_1} \right)^2 + (2\pi f)^2 \right]} = \frac{\Delta\mu^2}{\pi(\tau_0 + \tau_1)f_c^2} \cdot \frac{1}{1 + (f/f_c)^2}, \quad (2.33)$$

where $\Delta\mu$ is the amplitude of the induced potential change and the cutoff frequency $f_c = \frac{1}{2\pi} \left(\frac{1}{\tau_0} + \frac{1}{\tau_1} \right)$ is determined by the average switching rate of the fluctuator, typically lying in the kilohertz range. As depicted in Figure 2.9(b), when the frequency $f \ll f_c$, the PSD is approximately constant, indicative of white noise. Conversely, when $f \gg f_c$, the PSD rolls off as $1/f^2$, characteristic of pink noise [44].

Assuming symmetric switching times ($\tau_0 = \tau_1 = \tau$), the PSD simplifies to

$$S(f) = \frac{\Delta\mu^2\tau}{4 + (2\pi f)^2\tau^2}. \quad (2.34)$$

When many such fluctuators with distinct switching rates and amplitudes coexist, their collective contribution sums to produce a broadband noise spectrum. For an ensemble of N fluctuators, the total PSD is given by

$$S_N(f) = \lim_{N \rightarrow \infty} \sum_{i=1}^N \frac{\Delta\mu_i^2\tau_i}{4 + (2\pi f)^2\tau_i^2} = \int_{\tau_{\min}}^{\tau_{\max}} \frac{\Delta\mu^2\tau}{4 + (2\pi f)^2\tau^2} D(\tau) d\tau, \quad (2.35)$$

where each term describes the Lorentzian contribution of the i -th fluctuator. $D(\tau)$ is the distribution of switching times, which is often empirically observed to be log-uniform [43], i.e., $D(\tau) \propto 1/\tau$. Evaluating this integral under a log-uniform distribution of τ yields a power-law behavior for the ensemble-averaged spectrum:

$$S(f) \propto \frac{1}{f^\beta}, \quad \text{with } \beta \approx 1. \quad (2.36)$$

This low-frequency noise, widely known as $1/f$ noise (or flicker noise), is particularly detrimental to qubit performance because it causes quasi-static, long-term fluctuations in the qubit's energy levels and control parameters during gate operations [45]. Such noise is commonly observed over several decades of frequency, from millihertz to kilohertz, as illustrated in Figure 2.9(c).

The exponent β characterizes how the noise power scales with frequency. When $\beta = 0$, the spectrum is white, with equal power across all frequencies. For $0 < \beta < 1$, the noise exhibits weak temporal correlations, whereas $\beta > 1$ indicates strong low-frequency dominance and long-time correlations. In many solid-state systems, including quantum dot qubits, experimental studies often report values around $\beta \approx 1.2$, which is consistent with a log-uniform distribution of TLF switching times.

To characterize the magnitude of this charge noise, it is common practice to quote the PSD at a specific reference frequency, typically 1 Hz, denoted as $S_\epsilon(1 \text{ Hz})$. This value provides a standardized measure of the low-frequency noise strength and allows for direct comparison between different devices and materials. For instance, charge noise levels for silicon quantum dots are often reported as $S_\epsilon(1 \text{ Hz})$ in units of $(\mu\text{eV})^2/\text{Hz}$.

To quantify the overall impact of this noise on qubit energy levels and estimate dephasing, the variance of the detuning fluctuations σ_ϵ^2 over a relevant frequency band can be computed by integrating the PSD

$$\sigma_\epsilon^2 = 2 \int_{f_{\text{low}}}^{f_{\text{high}}} S(f) \, df, \quad (2.37)$$

where σ_ϵ represents the standard deviation of these fluctuations. This variance directly reflects the magnitude of the random phase accumulation caused by the noise, providing a critical parameter for predicting qubit coherence times.

2.4.2 Charge noise effects on qubit performance

Charge noise couples to key control parameters in quantum dot (QD) qubits, most notably the energy detuning ϵ and the tunnel coupling t_c . For a charge qubit formed in a DQD, described in the $(1, 0)$ and $(0, 1)$ basis, the effective Hamiltonian is given by Equation (2.30). Building on this, charge noise perturbs both the detuning ϵ and the tunnel coupling t_c by modifying local electrostatic potentials near the QD device. For detuning, which reflects the energy difference between the left and right dots, we write $\epsilon = \sum_i \alpha_i V_i$, where V_i are the applied gate voltages and α_i are the corresponding lever arms relating voltage changes to energy shifts. Charge fluctuations (from TLFs) near the gates or in the substrate effectively appear as time-dependent voltage shifts $\delta V_i(t)$, leading to detuning noise:

$$\delta\epsilon(t) = \sum_i \alpha_i \delta V_i(t). \quad (2.38)$$

Beyond its influence on detuning, charge noise also critically affects the tunnel coupling t_c . This parameter, which governs the coherent hybridization between the two charge states, is exponentially sensitive to the barrier height and width between the dots. It can be approximated as

$$t_c \propto \exp\left(-\frac{d}{\lambda}\right), \quad (2.39)$$

where d is the effective barrier width and λ is the wavefunction decay length, which in turn depends on the barrier potential V_b via $\lambda \propto \hbar/\sqrt{2m^*V_b}$. Charge fluctuations that locally modify V_b perturb λ and thereby modulate t_c . Linearizing this relation yields

$$\frac{\delta t_c(t)}{t_c} \approx \frac{d}{4\lambda^2} \cdot \frac{\delta V_b(t)}{V_b}, \quad (2.40)$$

demonstrating that even small potential changes can significantly affect tunnel coupling due to its inherent exponential dependence.

Although charge noise does not couple directly to the electron's spin degree of freedom, it can significantly degrade the performance of spin qubits indirectly through its influence on the exchange interaction. In many spin qubit designs, the exchange interaction $J(\epsilon)$ is highly

sensitive to detuning, as exemplified by the approximate relation

$$J(\epsilon) \approx \frac{4t_c^2}{U + \epsilon} + O(t_c^4), \quad (2.41)$$

where U is the on-site charging energy. Variations in ϵ caused by charge noise thus lead to fluctuations in J , which in turn degrades the coherence of both ST and EO qubits by introducing phase errors during gate operations [38].

A simplified derivation of this dependence can be obtained using second-order perturbation theory for a two-electron DQD. The singlet state $|S(1, 1)\rangle$ couples virtually to the doubly occupied state $|S(0, 2)\rangle$ via tunnel coupling t_c , while the triplet $|T(1, 1)\rangle$ (specifically $|T_0(1, 1)\rangle$) remains uncoupled due to spin symmetry. The energy shift of the singlet is

$$\delta E_S \approx -\frac{2t_c^2}{U + \epsilon}, \quad (2.42)$$

thereby lowering its energy relative to the triplet. The resulting exchange splitting $J(\epsilon)$ is then approximately given by

$$J(\epsilon) \approx E_T - E_S \approx \frac{4t_c^2}{U + \epsilon}. \quad (2.43)$$

This strong, nonlinear dependence implies that even small fluctuations in detuning can cause significant fluctuations in J , leading to substantial dephasing in spin qubits.

For quasi-static detuning noise, the pure dephasing time T_2^* is well approximated by the qubit's sensitivity to energy fluctuations

$$\frac{1}{T_2^*} \approx \frac{1}{\hbar} \left| \frac{dE}{d\epsilon} \right| \sigma_\epsilon, \quad (2.44)$$

where σ_ϵ is the standard deviation of detuning fluctuations. Operating near a “sweet spot” such as the charge degeneracy point ($\epsilon = 0$) minimizes the first-order derivative $\partial E / \partial \epsilon$, thereby significantly reducing sensitivity to noise.

As a concrete example, typical detuning noise amplitudes on the order of $\sigma_\epsilon \sim 1 \mu\text{eV}$ can lead to T_2^* times ranging from 10 to 100 ns for charge qubits. These values are consistent with experimental observations in semiconductor DQD systems [46, 47]. For spin qubits, where the influence of charge noise enters indirectly through the detuning dependence of $J(\epsilon)$, coherence times may reach the microsecond regime. Nevertheless, charge noise remains a dominant decoherence source for electrically controlled qubits unless mitigated through strategies such as operating at sweet spots, employing symmetric operating points, or utilizing dynamical decoupling sequences [38, 48, 49].

Despite these drawbacks, various strategies have been proposed to mitigate the effects of charge noise. Nevertheless, a complete understanding of its microscopic origin and a comprehensive predictive model remain elusive. Current research efforts focus on gathering systematic data across different materials, device geometries [50], and temperature regimes, with the

ultimate goal of developing predictive noise models to guide the design of more robust and scalable qubit systems [51].

Chapter 3

Experimental methods

This chapter outlines the experimental setup and procedures used in this work, beginning with the device architecture and continuing through the bonding process, cryogenic environment, and control systems. The goal is to present a coherent engineering narrative: how a fragile QD device is mounted, electrically connected, and operated with precision at millikelvin temperatures to enable reproducible charge noise measurements.

3.1 Experimental setup

Establishing a functional QD system at cryogenic temperatures presents significant engineering challenges. It necessitates integrating a nanoscale silicon device on a chip with a printed circuit board (PCB), ensuring stable electrical connections, and maintaining low-noise conditions within a dilution refrigerator. This section details the components and procedures developed to address these challenges, from device preparation to system cooling.

3.1.1 Silicon-based quantum dot device

This study utilizes a silicon-based quantum chip developed by SemiQon. The device features a dual-layer gate architecture engineered to electrostatically define QDs within a silicon MESA structure—a laterally confined and etched region forming the conduction channel.

Figure 3.1 presents a schematic cross-section of the device. From top to bottom, the device stack consists of a metal top gate (serving as a routing layer), two gate layers, the silicon MESA layer, a buried oxide (BOX) layer, and a backgate. The metal top gate, made from a superconducting metal, connects different regions of the device and has a minimum linewidth of 400 nm, with a measured sheet resistance of $1.4 \pm 0.3, \Omega/\square$. This top gate is electrically isolated from the underlying gate stack by a top gate oxide. The two gate layers are composed of heavily n-doped polysilicon (n++), with thicknesses of 80 nm (Gate 2) and 50 nm (Gate 1). Each gate layer has a minimum linewidth of 40 nm, with sheet resistances of $209 \pm 26, \Omega/\square$.

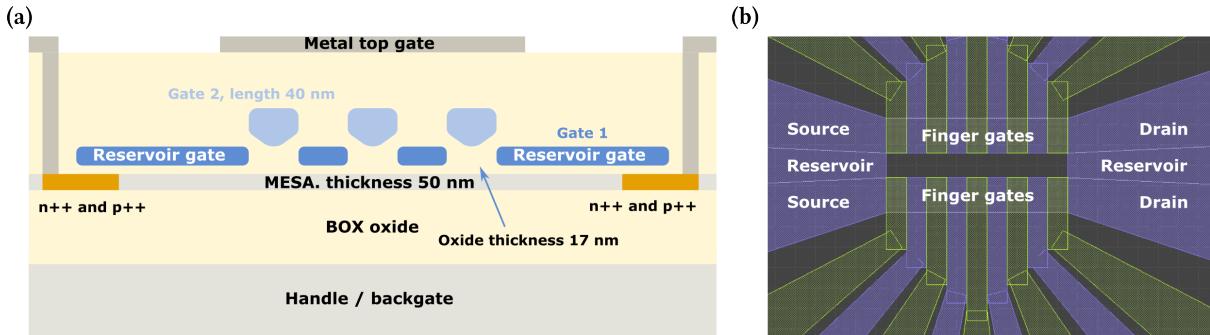


Figure 3.1: (a) Cross-sectional schematic of the silicon-based QD device. The structure is built on a handle/backgate substrate with a BOX layer. The active conduction channel is formed in a 50 nm-thick silicon MESA layer, flanked by n++ and p++ source/drain contacts. The dual-layer gate architecture features Gate 1 (reservoir gates) separated from the MESA by a 17 nm gate oxide, and Gate 2 (individual QD gates), with a minimum gate length of 40 nm, positioned above Gate 1. A metal top gate forms the uppermost layer. This multi-gate configuration enables electrostatic accumulation of reservoirs and precise lateral confinement for quantum dot formation. (b) Top-down view of the device layout. The device comprises two mirror-symmetric quantum dot arrays, each featuring nine finger gates. Source, reservoir, and drain regions are indicated. These arrays are electrically isolated, enabling independent operation and providing a versatile platform for multi-dot experiments and charge noise measurements.

and $250 \pm 27, \Omega/\square$, respectively. A 17 nm-thick oxide separates Gate 2 from the underlying MESA, which serves as the conduction channel where quantum dots are formed. The MESA layer, fabricated from either natural silicon or isotopically enriched ^{28}Si , is 50 nm thick with a channel width of 75 nm and a minimum lateral linewidth of 20 nm. According to data obtained from SemiQon (private communication, 2024), the sheet resistivity is $274 \pm 20 \Omega/\square$ for n-doped silicon and $887 \pm 74, \Omega/\square$ for p-doped silicon. The MESA is embedded in a 380 nm-thick silicon dioxide (SiO_2) BOX layer that electrically insulates it from the backgate. The backgate itself is made of low-doped naturally abundant silicon (Nat. Si) and acts as a global gate for tuning the device potential.

From a top-down perspective, the device layout consists of mirror-symmetric top and bottom quantum dot arrays. Each array contains nine finger gates that enable the formation of multiple quantum dots and allow fine control over tunnel barriers. Source and drain contacts, defined by n++ and p++ doping, are positioned at either end of the transport channel, allowing charge sensing and current measurements. The two arrays are electrically isolated from each other, allowing independent operation and offering a versatile platform for charge noise measurements.

3.1.2 Chip-to-PCB connection using wire bonding

Reliable wire bonding is a critical step in integrating QD devices with macroscopic measurement infrastructure. Initial attempts encountered several challenges, including mechanical damage during sample mounting and insufficient wire support, which frequently resulted in

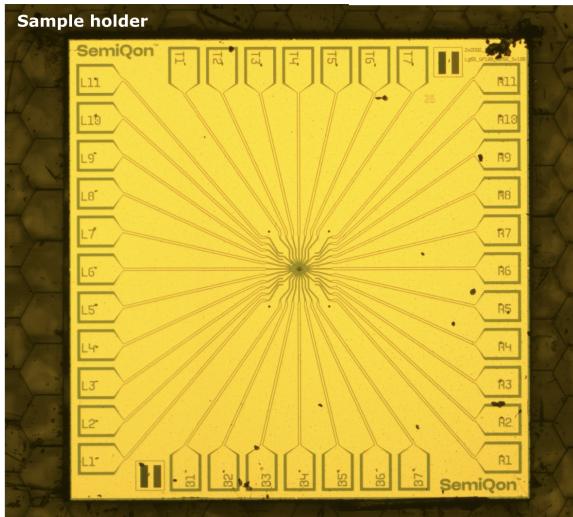


Figure 3.2: Photograph of the SemiQon chip mounted onto a PCB using a custom 3D-printed sample holder. The holder's slightly elevated and enlarged frame supports the bonding wires and prevents them from resting on the device edge, thereby reducing the risk of surface damage and ground shorts during wire bonding.

surface scratches and ground shorts, ultimately rendering the devices unusable. These early failures underscored the necessity for a more robust and reproducible bonding strategy.

Sample preparation

The SemiQon chip was mounted onto the PCB using GE varnish. To prevent surface scratches, a cotton swab was gently pressed onto the center of the chip, avoiding the use of sharp metal tools. A common issue observed was that bonding wires tended to rest on the raised device edge, increasing the risk of ground shorts, as the chip surface sits slightly higher than the surrounding PCB. To mitigate this, a custom 3D-printed hollow square sample holder with curved inner edges was designed and fabricated. The holder was intentionally made slightly larger than the chip's actual dimensions (2.58 mm × 2.54 mm vs. 2.50 mm × 2.50 mm) to accommodate mounting tolerances. As depicted in Figure 3.2, the holder performed effectively: its height (0.56 mm) slightly exceeded that of the chip (0.54 mm), allowing bonding wires to rest securely on the insulating frame rather than on the device edge, thereby eliminating the shorting issue.

Following this improved preparation process, the chip surface was inspected under an optical microscope. The surface condition was satisfactory, with only minor dust particles observed on the contact pads.

Wire bonding

After mounting, the SemiQon chip was connected to the PCB via wire bonding using silver (Ag) wires. Figure 3.3(a) illustrates the chip's position within the PCB and the corresponding bonding scheme. Each bonding wire connects a designated PCB pad to a chip pad along a

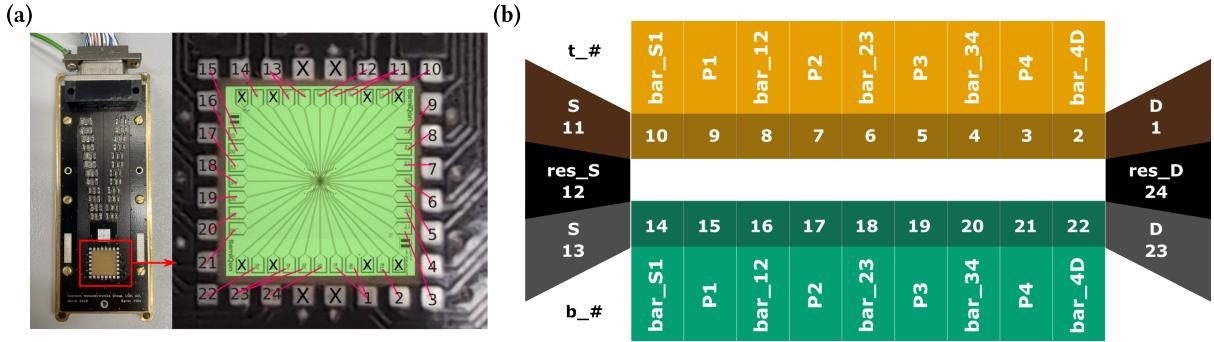


Figure 3.3: (a) Left: Photograph of a PCB used in this work. Right: Wire bonding scheme, where red lines indicate the bonding paths from PCB pads to chip pads. (b) Schematic of the device layout showing the top (orange) and bottom (green) gate layers. “S” and “D” denote the source and drain terminals. The numbered gates correspond to their respective PCB pads as shown in (a).

predefined route. The bonding process initiates at the PCB pad, after which the wire is gently guided and bent toward the chip pad to complete the connection. This approach ensures consistent wire geometry and minimizes the risk of damaging chip pads from repeated bonding attempts.

To ensure robust bonds, parameters such as ultrasonic power, bonding time, and applied force were systematically optimized. These improvements significantly minimized the need for re-bonding, thereby reducing the risks of misalignment, pad delamination, and surface contamination.

Figure 3.3(b) presents a schematic of the device layout, specifically highlighting the top (orange) and bottom (green) gate layers relevant to the wire bonding scheme. Each layer forms an independent linear array of quantum dots, with “res_S” and “res_D” denoting the source and drain reservoirs, respectively, and “S” and “D” indicating the source and drain terminals. Due to the limited number of available pads on the PCB, some chip pads were connected to the same PCB pad. This shared routing was meticulously planned to avoid interference between control lines and to maintain reliable device operation. For instance, as detailed in Table 3.1, chip pad L4 controls the p++ bottom source contact (b_S+), while L5 controls the n++ bottom source (b_S-); both are routed through the same PCB pad.

A complete bonding map is provided in Table 3.1, listing the chip pad labels, PCB pad numbers, and corresponding gate or contact names. This table served as the reference for assigning gate voltages and configuring measurement channels throughout the experiment.

Leakage test

Following wire bonding, each electrical line was tested using a source-measure unit (SMU) to evaluate leakage currents and identify potential ground shorts. A 10 mV bias was applied to each line, and the resulting current was recorded.

Table 3.1: Mapping between chip pads, PCB pad numbers, and their corresponding device labels. Chip pads are labeled according to their physical position (e.g., L for left, R for right, T for top, B for bottom). Some chip pads are intentionally connected to the same PCB pad due to limited available connections, as indicated by repeated PCB pad numbers. Empty entries (marked with “ \times ”) denote unused or unconnected pads.

| Chip | PCB | Device | Chip | PCB | Device |
|------|----------|----------|------|----------|----------|
| L1 | \times | | R1 | \times | |
| L2 | 14 | b_bar_S1 | R2 | 22 | b_bar_4D |
| L3 | \times | | R3 | \times | |
| L4 | 13 | b_S+ | R4 | 23 | b_D+ |
| L5 | 13 | b_S- | R5 | 23 | b_D- |
| L6 | 12 | res_S | R6 | 24 | res_D |
| L7 | 11 | t_S+ | R7 | 1 | t_D+ |
| L8 | 11 | t_S- | R8 | 1 | t_D- |
| L9 | \times | | R9 | \times | |
| L10 | 10 | t_bar_S1 | R10 | 2 | t_bar_4D |
| L11 | \times | | R11 | \times | |
| T1 | 9 | t_P1 | B1 | 15 | b_bar_P1 |
| T2 | 8 | t_bar_12 | B2 | 16 | b_bar_12 |
| T3 | 7 | t_P2 | B3 | 17 | b_P2 |
| T4 | 6 | t_bar_23 | B4 | 18 | b_bar_23 |
| T5 | 5 | t_P3 | B5 | 19 | b_P3 |
| T6 | 4 | t_bar_34 | B6 | 20 | b_bar_34 |
| T7 | 3 | t_P4 | B7 | 21 | b_P4 |

The source and drain terminals exhibited resistances in the megaohm ($M\Omega$) range, consistent with expectations for transport pathways in semiconductor devices. All gate and reservoir lines showed resistances exceeding several gigaohms ($G\Omega$), corresponding to current levels below the SMU’s detection threshold of 0.05 nA. Any measured current at or below this level was interpreted as being below the detection limit, thereby confirming the absence of measurable leakage. In contrast, a resistance near $30\text{ k}\Omega$ typically indicated a ground short, often caused by unintended contact between a bonding wire and a conducting layer. This value is consistent with the combined resistance of the PCB, fridge wiring, or other low-impedance paths to ground.

3.1.3 Dilution refrigerator

To observe quantum behavior in the device, the system must be operated at cryogenic temperatures below 1 K, where thermal excitations are strongly suppressed. This is achieved using a dilution refrigerator, capable of reaching temperatures below 10 mK.

The PCB holding the QD device was mounted on the mixing chamber plate, the coldest stage of the dilution refrigerator, which typically achieves a base temperature of below 10 mK under minimal thermal load. As depicted in Figure 3.4, the PCB was thermally anchored to this stage

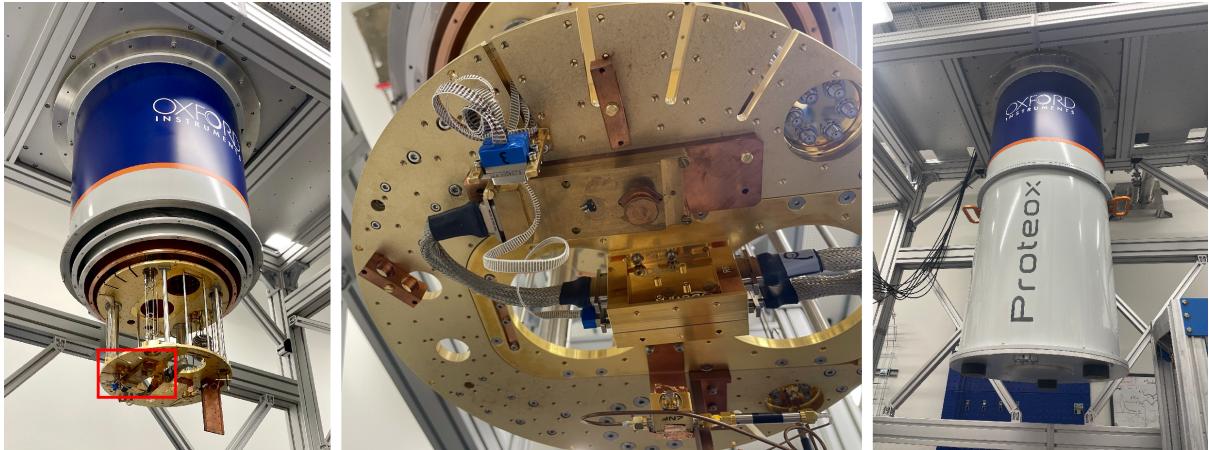


Figure 3.4: Proteox dilution refrigerator system (Oxford Instruments). Left: full system with the experimental insert installed. The mixing chamber stage, highlighted in red, hosts the sample PCB. Middle: close-up of the mixing chamber plate where the PCB is anchored. RF and DC lines are routed to the sample through thermally anchored stages. Right: exterior view of the fully assembled system.

to ensure efficient heat sinking and thermal equilibrium. The mixing chamber temperature is precisely controlled by adjusting the flow rate of the circulating ^3He - ^4He mixture within the dilution unit. It is important to note that, in practice, the actual device temperature may be slightly higher than the measured base temperature due to dissipative elements such as filtering components, wiring heat load, and local power dissipation from nearby electronics.

Signal lines, including both coaxial cables and twisted pairs, are routed from room temperature down to the mixing chamber. These lines are meticulously thermally anchored at successive cryogenic stages (typically 50 K, 4 K, still, and cold plate) to minimize parasitic heat transfer to the coldest stage. This careful configuration enables low-noise, high-fidelity voltage control and current readout, crucial for maintaining the ultralow-temperature environment required for stable quantum dot operation.

3.2 Electronics for gate control and signal readout

Voltage control and signal acquisition in this study are performed using the Nanonis Signal Conversion Interface (SC5). Gate electrodes are biased by analog voltages delivered through the SC5 outputs, enabling precise tuning of QD potentials. This platform is widely used in QD experiments due to its high-resolution analog outputs, low-noise signal acquisition, and integrated capabilities for real-time data processing and visualization. To evaluate the system's suitability for charge-sensitive measurements, it is essential to understand its analog output and input characteristics, as well as how its noise performance depends on the chosen operating parameters.

Each of the eight analog output (AO) and eight analog input (AI) channels is accessible via front-panel BNC connectors, as shown in Figure 3.5. These serve as the primary interface for

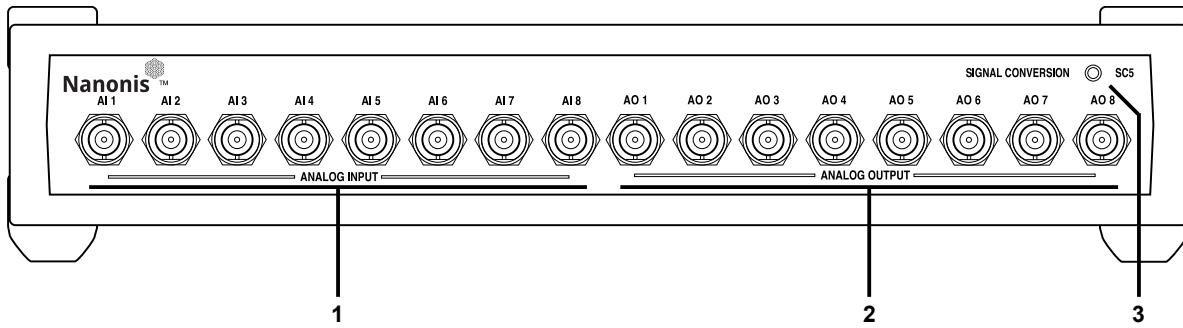


Figure 3.5: Front panel of the Nanonis SC5 signal conversion interface. (1) Analog Inputs (AI1-AI8): Eight connectors used for differential analog signal acquisition, accepting input voltages up to ± 10 V with a -3 dB bandwidth of 100 kHz. (2) Analog Outputs (AO1-AO8): Eight connectors for generating analog output signals up to ± 10 V with a current limit of ± 20 mA; the output bandwidth is 40 kHz (-3 dB). (3) Power LED: Indicates that the device is powered on.

applying gate voltages and acquiring signals from the device.

Internally, the SC5 architecture includes high-resolution digital-to-analog converters (DACs), analog-to-digital converters (ADCs), and low-pass filters (LPFs) on both input and output paths. The LPFs are designed to suppress high-frequency noise, which is particularly important for charge sensing and long-term stability measurements. A Complex Programmable Logic Device (CPLD) coordinates timing and control logic across modules, while galvanic isolation separates the analog and digital domains to reduce cross-domain interference. The system is powered by regulated ± 15 V and ± 5 V supplies, stabilized using a linear power supply to minimize ripple and switching noise. A field-programmable gate array (FPGA) handles communication with the host computer and manages internal data routing.

With the internal structure of the SC5 system described, we now focus on the parameters most relevant to noise-sensitive QD measurements. Among these, the DAC resolution determines the minimum voltage step size and thus influences quantization noise during gate voltage sweeps. The analog input oversampling setting affects the input-referred noise floor and effective resolution. Finally, the analog signal bandwidth, shaped by both hardware filtering and sampling settings, controls the trade-off between noise rejection and measurement speed. These factors collectively determine how precisely charge transitions and fluctuations can be resolved, and they will be discussed in detail in the following sections.

3.2.1 DAC resolution and voltage granularity

The DAC translates digital voltage values set in the control interface into real analog voltages applied to the device gates. One key property of the DAC is its minimum voltage step size, which determines the smallest possible change in gate voltage during sweeps. This directly affects the precision of voltage control and, consequently, the resolution of data acquisition in charge sensing or transport measurements.

The minimum voltage step size is given by

$$\Delta V = \frac{V_{\text{range}}}{2^N}, \quad (3.1)$$

where N is the DAC bit resolution and V_{range} is the output voltage range. For the SC5, which uses a 20-bit DAC with an output range of ± 10 V, the minimum voltage step size is approximately $19 \mu\text{V}$. If upgraded to a 22-bit DAC, the step size would reduce to about $5 \mu\text{V}$. This finer granularity lowers the quantization noise and allows for more accurate voltage tuning, especially important when operating in regimes where small voltage changes can cause large variations in qubit state or charge configuration.

One practical method to further reduce the effective voltage step size is to use a potential divider at the DAC output. In typical QD operations, the required voltage range is often within ± 2 V, significantly lower than the SC5's full ± 10 V output capability. By introducing a potential divider with a 1:5 ratio, the output voltage range is scaled down to ± 2 V, and the minimum effective voltage step size becomes approximately $1 \mu\text{V}$ with 22-bit DAC. This approach sacrifices the maximum voltage range in favor of improved resolution and is well-suited for fine-tuning gate voltages in low-voltage regimes.

3.2.2 Analog input noise spectrum

While voltage granularity determines how precisely we can control the gate, another critical factor is how cleanly we can measure the result. Understanding the intrinsic noise level of the analog input channels is essential for interpreting small voltage signals, particularly in charge sensing and noise spectroscopy. Building upon the discussion of spectral noise in the previous section, the amplitude spectral density (ASD) is used here to quantify the noise level, typically expressed in units of $\text{V}/\sqrt{\text{Hz}}$. Table 3.2 presents the typical reference noise levels for the SC5 analog input channels as provided in the user manual. While these values serve as a baseline, the intrinsic noise levels can vary between individual instruments, and the calibrated noise performance of the specific instrument used in this study will be detailed in the next section.

Table 3.2: Reference noise level of the SC5 analog input channels. Data are from the SC5 User Manual.

| Frequency | Spectral noise [$\text{nV}/\sqrt{\text{Hz}}$] |
|-----------|---|
| 1 Hz | 2000 |
| 10 Hz | 620 |
| 100 Hz | 220 |
| 1 kHz | 155 |
| 10 kHz | 140 |
| 50 kHz | 140 |
| 100 kHz | 145 |

3.2.3 Oversampling and input noise performance

Although the spectral noise sets a fundamental limit, the actual measurement precision can be improved through oversampling. The SC5 system provides a range of oversampling settings for its analog input channels, which significantly affect the input-referred voltage noise. Table 3.3 summarizes the system’s performance under various oversampling conditions, including peak-to-peak noise, RMS noise, and the corresponding effective resolution.

In this table, the oversampling factor refers to the number of raw samples averaged to produce each recorded data point. Increasing the oversampling factor leads to better noise suppression, at the cost of reduced bandwidth and slower acquisition. The “Measurement BW” column in Table 3.3 indicates the effective noise bandwidth, representing the frequency range of the input signal passed after digital filtering. This bandwidth becomes narrower as the oversampling increases.

The noise performance is characterized both by the peak-to-peak noise and the root mean square (RMS) noise. While the peak-to-peak value gives a sense of the total voltage swing due to noise, the RMS value provides a more meaningful measure of average signal fluctuation and is more commonly used to quantify system noise. The last column shows the effective resolution in bits, which indicates how many bits of the ADC output remain distinguishable from noise. Although the SC5 uses a high-resolution ADC, the presence of electronic noise reduces the usable bit depth. Oversampling helps recover part of this loss, effectively enhancing the resolution.

As shown in Table 3.3, the RMS noise decreases from 99 μV at 1 \times oversampling to approximately 6.2 μV at 1024 \times and above. In parallel, the effective resolution increases from 17.6 bits to more than 21.6 bits. This improvement arises from averaging out high-frequency noise, thereby enhancing the signal-to-noise ratio.

However, beyond 1024 \times , the improvement becomes marginal due to the increasing contribution of low-frequency 1/ f noise. In practice, oversampling factors between 128 \times and 1024 \times are often used to achieve a good balance between noise suppression and measurement speed.

This tunability is particularly valuable for experiments requiring high sensitivity, such as charge noise spectroscopy or stability measurements. Conversely, for fast scanning tasks such as 2D mapping or tuning of device parameters, lower oversampling factors (e.g., 32 \times or 64 \times) are typically sufficient and preferred due to their higher acquisition rates.

In addition to the oversampling factor, the acquisition time per point is a critical parameter that affects both noise performance and measurement speed. It determines how long the input signal is sampled and averaged at each data point, and is typically set in units of milliseconds. In the SC5 system, the acquisition time t_{acq} is related to the oversampling factor $N_{\text{oversampling}}$

Table 3.3: Analog input noise performance of the SC5 under different oversampling settings. Data are from the SC5 User Manual.

| Oversampling | Measurement BW | Peak-peak [μ V] | RMS [μ V] | Effective resolution [bits] |
|--------------|------------------|-------------------------|-------------------|--------------------------------|
| 1× | 489 Hz–500 kHz | 665 | 99 | 17.62 |
| 2× | 244 Hz–250 kHz | 480 | 71 | 18.10 |
| 4× | 122 Hz–125 kHz | 345 | 50 | 18.61 |
| 8× | 61 Hz–62.5 kHz | 245 | 35 | 19.12 |
| 16× | 30.5 Hz–31.3 kHz | 175 | 25 | 19.61 |
| 32× | 15.3 Hz–15.6 kHz | 125 | 18 | 20.08 |
| 64× | 7.6 Hz–7.8 kHz | 93 | 14 | 20.45 |
| 128× | 3.8 Hz–3.9 kHz | 71 | 10 | 20.93 |
| 256× | 1.91 Hz–1.95 kHz | 56 | 8.1 | 21.24 |
| 512× | 0.95 Hz–977 Hz | 49 | 6.9 | 21.47 |
| 1024× | 0.48 Hz–488 Hz | 43 | 6.3 | 21.60 |
| 2048× | 0.24 Hz–244 Hz | 42 | 6.2 | 21.62 |
| 4096× | 0.12 Hz–122 Hz | 41 | 6.2 | 21.62 |
| 8192× | 0.06 Hz–61 Hz | 41 | 6.2 | 21.62 |
| 16384× | 0.03 Hz–30.5 Hz | 41 | 6.2 | 21.62 |
| 32768× | 0.015 Hz–15.3 Hz | 40 | 6.4 | 21.58 |

and the base sampling rate f_{base} by

$$t_{\text{acq}} = \frac{N_{\text{oversampling}}}{f_{\text{base}}}, \quad (3.2)$$

where f_{base} is the internal sampling rate of the SC5 ADC (typically 500 kHz). This relation implies that higher oversampling directly leads to longer acquisition times, which improves signal averaging and reduces random noise.

In practice, the acquisition time is either set manually or adjusted automatically by the control software according to the chosen oversampling level. For slow charge sensing scans or noise spectroscopy, acquisition times in the range of 1–10 ms per point are often used to ensure a sufficiently low noise floor. In contrast, fast 2D mapping typically uses shorter acquisition times with moderate oversampling to maintain reasonable scan durations.

In summary, the combination of high DAC resolution, low spectral noise, and flexible oversampling allows the SC5 system to support both fast device tuning and high-sensitivity charge detection. These capabilities form the basis for the voltage control and signal acquisition strategies used throughout this study.

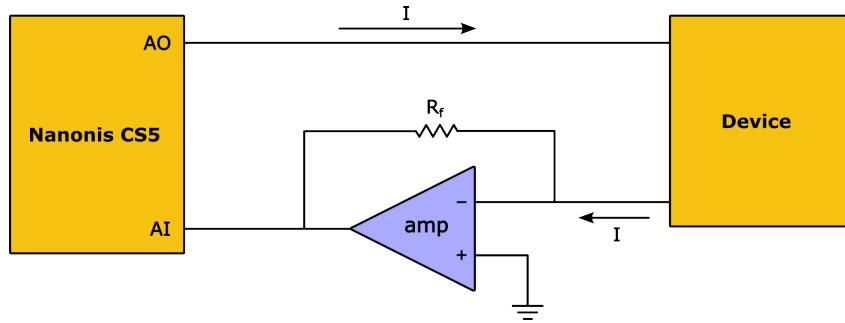


Figure 3.6: Simplified schematic of the instrument system used for current measurement. The Nanonis SC5 outputs a voltage through the analog output (AO) channel to bias the device under test. The resulting current flows through the device and is fed into a current-to-voltage amplifier, which converts it into a measurable voltage signal. This signal is then read by the analog input (AI) of the Nanonis SC5. The feedback resistor R_f determines the transimpedance gain of the amplifier.

3.3 Instrument calibration

To ensure high-precision data acquisition, it is essential to calibrate the measurement instruments. In this setup, the Nanonis SC5 system outputs a voltage that drives current through the device. The return current is converted to a voltage by a current-to-voltage amplifier with a gain of 10^8 . A simplified diagram of the overall instrument system is shown in Figure 3.6. The components requiring calibration include the voltage output of the Nanonis SC5, the current-to-voltage amplifier, and the input measurement channel of the Nanonis SC5.

3.3.1 Nanonis SC5 output calibration

To calibrate the analog output channels of the Nanonis SC5, each output was directly connected to a calibrated multimeter, which serves as a trusted voltage reference. The output voltage was swept from 1 mV to 1000 mV, and the corresponding values were recorded using the multimeter. A linear fit was then applied to extract the gain factor and offset for each channel. The results are summarized in Table 3.4. Based on the calibration results, the gain factor and offset for AO1 to AO8 were set accordingly in the Nanonis SC5 control software to ensure accurate voltage output during experiments.

3.3.2 Current-to-voltage amplifier calibration

Once the voltage output of the Nanonis SC5 has been calibrated, it can be used as a reliable voltage source to calibrate the current-to-voltage amplifier. Since the amplifier measures current, but the Nanonis SC5 provides a voltage output, a series resistor is used to convert the output voltage into a known current. A resistor of nominal value $10\text{ k}\Omega$ is connected between the Nanonis SC5 output and the amplifier input. The actual resistance was measured using an SMU and found to be $9.95\text{ k}\Omega$.

Table 3.4: Calibration results of the Nanonis SC5 analog outputs. Each channel shows an ideal gain of 1.000, with small negative offsets on the order of hundreds of microvolts.

| Nanonis output | Factor | Offset [mV] |
|----------------|-------------------|--------------------|
| AO1 | 1.000 ± 0.000 | -0.450 ± 0.004 |
| AO2 | 1.000 ± 0.000 | -0.535 ± 0.004 |
| AO3 | 1.000 ± 0.000 | -0.452 ± 0.004 |
| AO4 | 1.000 ± 0.000 | -0.464 ± 0.004 |
| AO5 | 1.000 ± 0.000 | -0.472 ± 0.008 |
| AO6 | 1.000 ± 0.000 | -0.527 ± 0.004 |
| AO7 | 1.000 ± 0.000 | -0.522 ± 0.004 |
| AO8 | 1.000 ± 0.000 | -0.481 ± 0.005 |

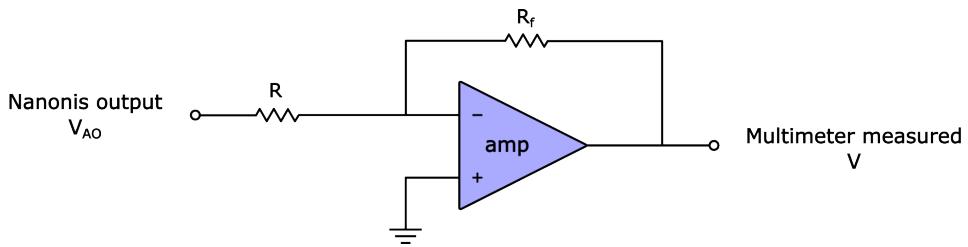


Figure 3.7: Calibration setup for the current-to-voltage amplifier. A $10\text{ k}\Omega$ resistor (measured as $9.95\text{ k}\Omega$ using an SMU) is used to convert the Nanonis SC5 voltage output into a current. The amplifier, labeled with a nominal gain of 10^8 , is experimentally calibrated to 1.13×10^8 .

The amplifier is nominally labeled with a gain of 10^8 V/A with bandwidth of 1.25 kHz . Its offset can be manually adjusted through an access hole on the device. The calibration setup is shown in Figure 3.7 and the relationship between the measured voltage V and the applied voltage V_{AO} is given by

$$k = \frac{V}{V_{AO}} = -\frac{R_f}{R}, \quad (3.3)$$

where R_f is the feedback resistor of the amplifier, and R is the series resistor. The ratio k can be obtained experimentally by measuring the output voltage V for known values of V_{AO} .

To perform the calibration, the output voltage of the Nanonis SC5 was swept from 1 mV to 5 mV , and the resulting output voltage of the amplifier was recorded using a multimeter. The measured ratio was $k = -11350 \pm 10$, and the output offset was 187 ± 3.317 . The offset is not critical for calibration purposes, as it can be compensated using the input offset setting in the Nanonis SC5 control software. The actual gain of the amplifier can be calculated using the relation $R_f = -kR$, which gives $R_f = 1.13 \times 10^8 \text{ V/A}$.

3.3.3 Nanonis SC5 input offset adjustment

The input channels of the Nanonis SC5 were calibrated using the setup shown in Figure 3.6. To ensure that no current flows through the device during calibration, the device was placed in a non-conductive state by applying low gate voltages to fully pinch off the channel while its

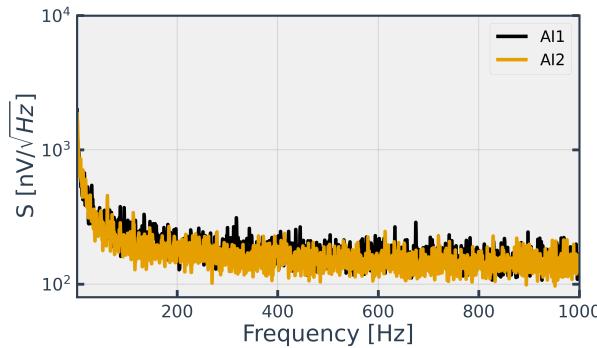


Figure 3.8: ASD of the SC5 analog input channel (AI1 and AI2). The noise level is measured at $1 \mu\text{V}/\sqrt{\text{Hz}}$ at 1 Hz, which is comparable to the typical noise floor of the SC5.

source and drain contacts were left unbiased. Under these conditions, the expected current is effectively zero. The “Auto Offset” function in the Nanonis SC5 control software was then used to automatically adjust the input offset, effectively nulling the measured current to zero. This procedure ensures that subsequent current measurements reflect only the signal of interest, with baseline offsets removed.

3.3.4 Nanonis SC5 input noise spectrum

To characterize the noise of the SC5 system, the input was grounded and Fast Fourier Transforms (FFTs) with a Hann window were performed over time traces of 20,000 points. The resulting ASD is shown in Figure 3.8. The noise characteristics are further quantified by their integrated RMS values over the relevant bandwidth.

3.4 Control software and automation

To streamline the measurement process and minimize the risk of manual errors, a Python-based software framework named `gate-manager` was developed for automating gate voltage control and data acquisition. The system is designed to flexibly integrate with a variety of voltage sources and measurement instruments, enabling scalable and repeatable QD experiments with minimal operator intervention.

The framework is modular and consists of three core components:

- **Instrument communication:** The `connection.py` module manages low-level communication with external devices. It provides a unified interface for connecting to hardware such as the Nanonis control system, simplifying backend switching and allowing offline development and debugging.
- **Gate voltage control:** The `gate.py` module defines a `Gate` class that serves as the main controller for setting and reading voltages on individual gates. It supports both scalar and vectorized operations across multiple gates, and includes safety mechanisms such

as range checks and staged voltage ramping to prevent accidental overbiasing or device damage.

- **Automated sweeps:** The `sweeper.py` module implements routines for performing 1D, 2D, and time-dependent voltage sweeps over user-defined ranges. It coordinates with the `Gate` class to apply precise voltage steps and interfaces with measurement instruments to acquire current or charge sensor data. For time sweeps, the module holds the gate voltage constant and records data as a function of time at a specified sampling rate. Sweep parameters such as voltage ranges, sampling rates, integration times, and slew rates are all configurable.

The software was validated through a series of benchmark tests, including static voltage accuracy, dynamic sweep integrity, and data logging reliability. Initial experiments included the acquisition of 1D and 2D charge stability diagrams, where automated results showed excellent agreement with manually collected data, confirming the framework's precision and robustness. The full source code is available at: <https://github.com/chenx820/gate-manager>.

Chapter 4

Device characterization

This chapter details the electrical characterization of the fabricated devices, encompassing analyses of their turn-on and pinch-off behavior, as well as Coulomb diamond spectroscopy. Measurements were conducted at both room temperature and cryogenic temperatures to comprehensively assess device performance across various operational regimes.

4.1 Room temperature measurements

4.1.1 Uniform gate sweep

To verify the functionality of each gate and investigate the turn-on behavior of both the top and bottom gate arrays, a uniform gate sweep was performed at room temperature. As an illustrative example, consider the top array shown in Figure 4.1(a). All finger gates (including both plunger and barrier gates) were grouped and labeled as “fingers”. These gates were swept simultaneously from -1.5 V to 1.0 V in 10 mV steps while monitoring the source-drain current I_{SD} at the top drain contact “t_D”. A source-drain bias of $V_{SD} = 10$ mV was applied to top source “t_S”, and the reservoir potential was set to 800 mV.

For each measurement, either the top or bottom gate array was selected for sweeping, while the other was grounded. The resulting I_{SD} versus V_G characteristics for both channels are presented in Figure 4.1(b). The threshold voltage V_{th} signifies the onset of conduction and reflects the turn-on behavior of the channel, while the pinch-off point indicates the beginning of current saturation. These characteristic points were extracted using a machine learning model provided by the collaborators via the Conductor Quantum API. Focusing on the top channel, the threshold voltage was determined to be $V_{th} = -0.45$ V, indicating that the channel is fully closed when the gate voltage is below -0.45 V. When the fingers’ gate voltage exceeds 0.5 V, the channel becomes fully open. At even higher voltages, the current no longer saturates and begins to rise, which is indicative of short-channel effects. Similarly, for the bottom channel, the threshold voltage was -0.48 V and the pinch-off voltage was 0.43 V.

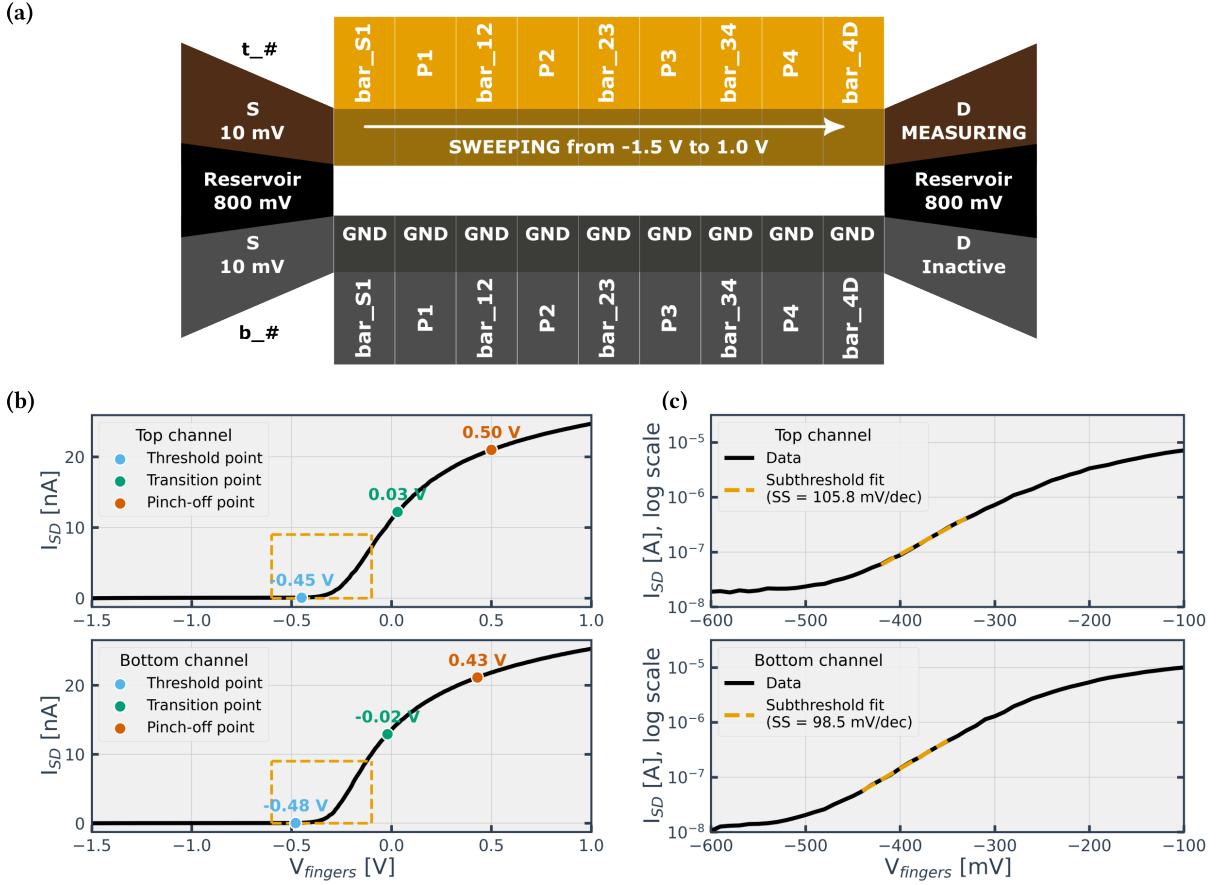


Figure 4.1: Characterization of a uniform gate sweep at room temperature. (a) Schematic of the measurement setup for the top channel, showing the gate array with individually addressed gates and the source-drain current I_{SD} measurement. (b) Source-drain current (I_{SD}) as a function of the collective finger gate voltage ($V_{fingers}$) for both the top and bottom channels, highlighting key characteristic points including threshold, transition, and saturation. The orange dashed boxes indicate the region expanded in panel (c). A source-drain bias of $V_{SD} = 10$ mV was applied, and the reservoir potential was set to 800 mV. The gate voltage was swept from -1.5 V to 1.0 V in 10 mV steps. (c) Semilogarithmic plots of I_{SD} versus $V_{fingers}$ for the top and bottom channels, focusing on the subthreshold region and showing subthreshold fits.

Figures 4.1(c) display semi-log plots of I_{SD} versus V_G for both the top and bottom channels. In this representation, the subthreshold region is clearly visible, characterized by an exponential increase in current with gate voltage. This behavior reflects thermally activated carrier transport prior to the onset of strong inversion in the channel. From linear fits in the subthreshold region, SS values of approximately 105.8 mV/decade and 98.5 mV/decade were extracted for the top and bottom channels, respectively. These values indicate moderate gate control, which is expected for accumulation-mode silicon devices with complex gate geometries. The similarity between the two channels also suggests uniform gate oxide quality and consistent electrostatics across the device.

4.1.2 Pinch-off measurements of individual gates

To assess individual gate control, pinch-off measurements were performed on each plunger and barrier gate independently. During each sweep, the target gate voltage was varied from negative to positive, while all other finger gates in the selected array were held at 0.8V to maintain channel conduction. Gates in the opposite array were grounded, as illustrated in Figure 4.2(a). The reservoir potential was fixed at 800mV, and a source-drain bias of 10mV was applied, consistent with the setup used for uniform gate sweeps. The measured current-voltage characteristics are shown in Figures 4.2(b-e). In all cases, the source-drain current I_{SD} increases as the gate voltage V_G is raised, reflecting the gradual formation of a conductive channel. At more negative gate voltages, I_{SD} dropped sharply, indicating the pinch-off point, beyond which the channel is fully depleted and conduction is suppressed.

Figures 4.2(b) and (d) present the responses of the plunger gates in the top and bottom arrays, respectively. The pinch-off voltages vary slightly across gates, typically falling between -0.35 V and -0.15 V. The threshold voltage, signifying the onset of significant current, is approximately -1.3V for the top channel and -1.5 V for the bottom channel. The overall uniformity in response suggests consistent capacitive coupling and fabrication quality among the plunger gates within each array.

Figures 4.2(c) and (e) display the characteristics of the barrier gates. Compared to the plunger gates, the barrier gates generally exhibit turn-on at less negative voltages and pinch-off at more positive voltages. This difference may arise from variations in gate geometry or local oxide thickness, even though the physical gate configuration is nominally identical to that of the plungers. Among the top barrier gates, “t_bar_S1” and “t_bar_12” exhibit comparatively weaker gate control, as indicated by a more gradual increase in I_{SD} with gate voltage and a higher residual current at large negative biases. These features suggest reduced capacitive coupling to the channel or localized fabrication non-uniformities for these specific gates.

Overall, these measurements confirm good electrostatic tunability of all gates at room temperature. The same characterization was also performed at cryogenic temperature, as discussed in the subsequent section.

4.2 Cryogenic measurements

4.2.1 Uniform turn-on behavior

After cooling the device to approximately 7 mK, the same set of measurements performed at room temperature was repeated to evaluate its low-temperature performance. All finger gates in either the top or bottom array were swept simultaneously from -1.0 V to 1.5 V, while monitoring the source-drain current. For these subsequent measurements, the reservoir voltage was set to 800 mV and the source-drain bias to 10 mV. The results are presented in Figure 4.3(a).

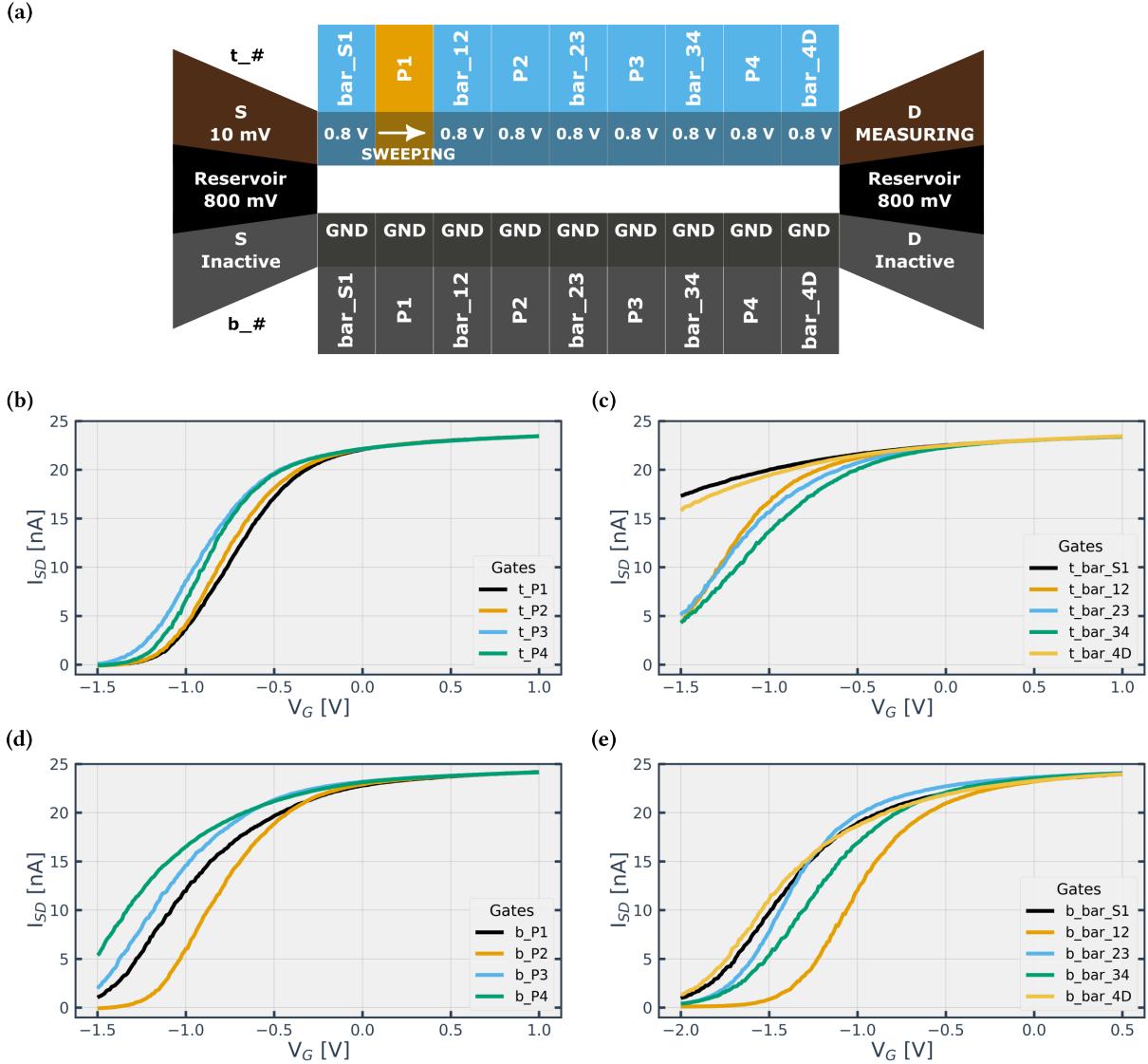


Figure 4.2: Room-temperature pinch-off characterization of individual gates. (a) Schematic illustration of the measurement configuration. During each pinch-off sweep, a single gate within the selected array was swept from negative to positive voltage, while all other gates in the same array were held at 0.8 V to maintain channel conduction. Gates in the opposite array were grounded. A source-drain bias of $V_{SD} = 10$ mV was applied, with the reservoir potential set to 800 mV. (b-e) Source-drain current (I_{SD}) as a function of individual gate voltage for: (b) plunger gates in the top array, (c) barrier gates in the top array, (d) plunger gates in the bottom array, and (e) barrier gates in the bottom array. Each curve represents a sweep of a distinct gate, demonstrating individual gate control and pinch-off behavior.

The threshold, transition, and pinch-off points were extracted using the identical method employed for the room-temperature measurements. All these characteristic values are notably shifted to more positive voltages at cryogenic temperatures. Specifically, for the top channel, the threshold voltage is 0.12 V and the pinch-off voltage is 1.08 V. For the bottom channel, the threshold voltage is also 0.12 V, while pinch-off occurs at 1.25 V. Additionally, the saturation current is higher than at room temperature, which is likely attributable to the suppression of phonon scattering at millikelvin temperatures, leading to increased carrier mobility in the

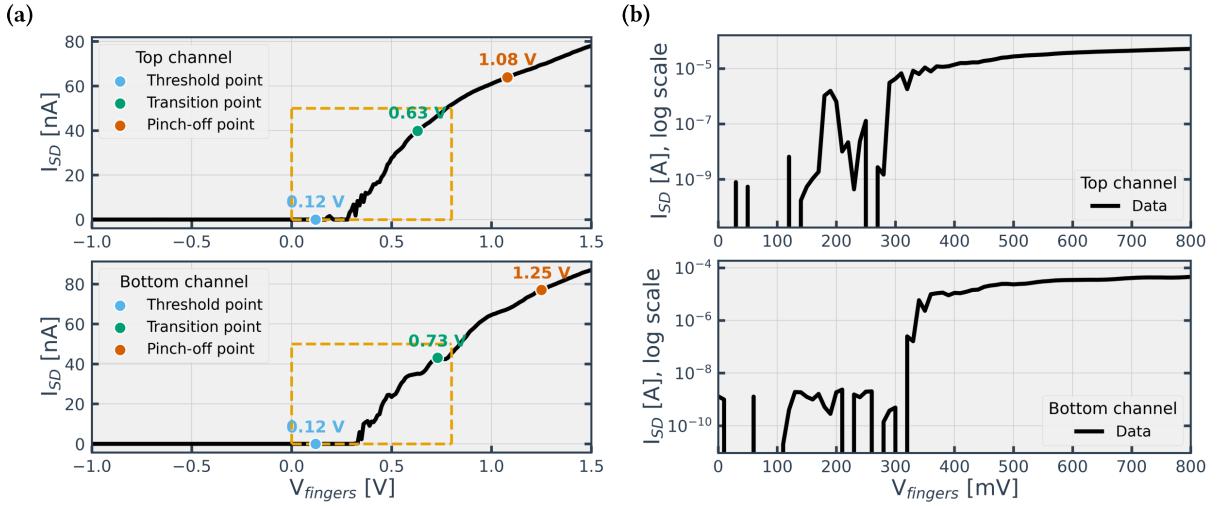


Figure 4.3: Characterization of a uniform gate sweep at cryogenic temperature. (a) Source-drain current (I_{SD}) as a function of the collective finger gate voltage (V_G) for both the top and bottom channels at a cryogenic temperature of approximately 7 mK. The gate voltage was swept from -1.0 V to 1.5 V in 10 mV steps. A source-drain bias of 10 mV was applied, and the reservoir potential was set to 800 mV. Threshold, transition, and pinch-off points are indicated. (b) Semi-logarithmic plots of I_{SD} versus V_G for the top and bottom channels. At this ultra-low temperature, the classical subthreshold region is not clearly identifiable, and a direct extraction of the SS is not meaningful due to the dominance of quantum transport phenomena.

channel [52].

Figure 4.3(b) displays the source-drain current plotted on a logarithmic scale. At this ultra-low temperature of 7 mK, the fundamental charge transport mechanisms deviate significantly from classical thermal-diffusion-driven behavior. Consequently, a clear, exponentially rising subthreshold region, characteristic of conventional MOSFET operation, is not observed. The current in the low-voltage regime exhibits significant noise and step-like features, which is indicative of phenomena such as localized states, hopping conduction, or quantum tunneling, rather than a well-defined thermal subthreshold regime [53]. Due to the absence of a clear linear region on the semi-log plot, a meaningful extraction of the classical SS is not feasible at this temperature. This challenges the direct comparison of SS values with those obtained at higher temperatures, where thermal effects dominate.

4.2.2 Output characteristics and saturation behavior

To further characterize the device performance at cryogenic temperatures, the output characteristics and saturation behavior of both channels were investigated. For these measurements, all finger gates in the selected array (top or bottom) were collectively biased at fixed gate voltages. The source-drain bias V_{SD} was then swept from 0 V to 1.0 V in 4 mV steps, while continuously recording the source-drain current I_{SD} .

Figures 4.4(a) and (c) display the measured I_{SD} versus V_{SD} curves for the top and bottom chan-

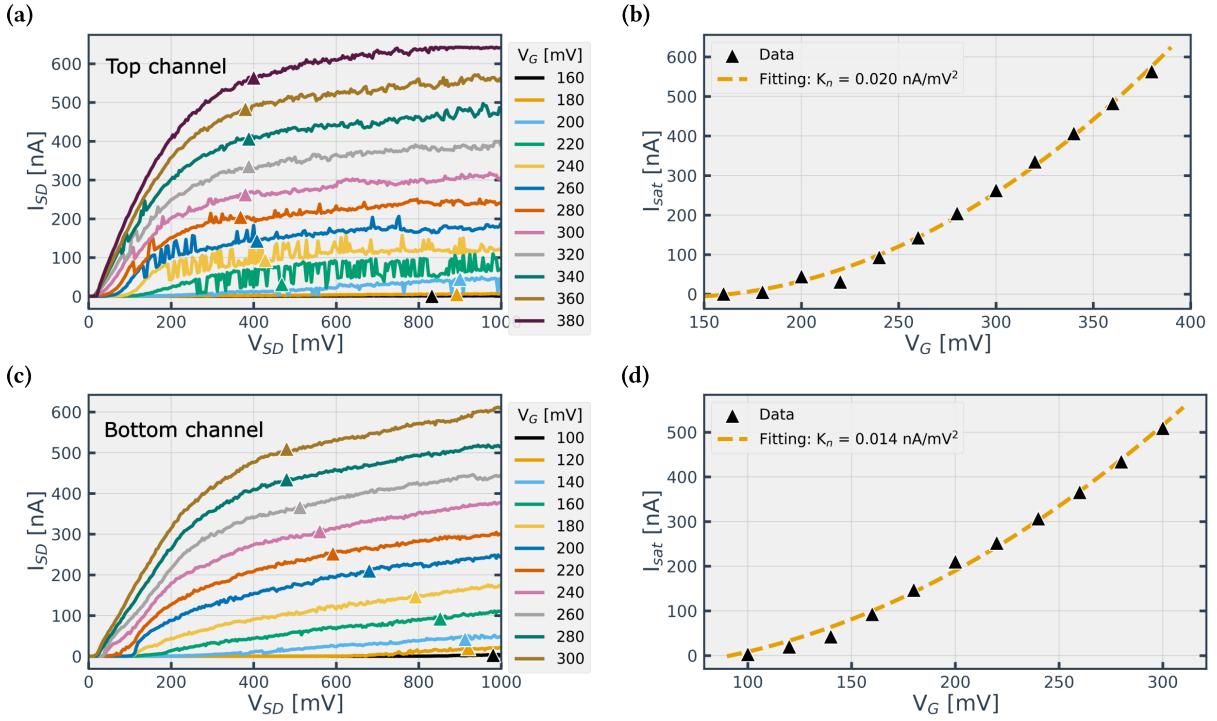


Figure 4.4: Cryogenic output characteristics and saturation current analysis. (a, c) Output I_{SD} – V_{SD} characteristics for the top (a) and bottom (c) channels at various fixed collective finger gate voltages (V_G), measured at cryogenic temperatures. These plots illustrate the transition from linear to saturation regimes. (b, d) Extracted saturation current (I_{sat}) as a function of the collective finger gate voltage (V_G) for the top (b) and bottom (d) channels. The solid lines represent fits to the square-law model, from which the process transconductance parameter (K_n) and threshold voltage (V_{th}) can be derived. The extracted K_n values from the fitting are 0.020 nA/mV² for the top array and 0.014 nA/mV² for the bottom array.

nels, respectively. As expected for field-effect transistors, the current exhibits linear behavior at low V_{SD} and gradually saturates at higher V_{SD} . This saturation indicates the formation of a pinch-off region near the drain, limiting further current increase. The saturation current I_{sat} was extracted at various gate voltages and subsequently plotted in Figures 4.4(b) and (d). These extracted data were then fitted using the well-established square-law model for MOSFET saturation from Equation (2.15). The process transconductance parameter, K_n , which quantifies the transistor's efficiency in converting gate voltage into drain current and encapsulates key device characteristics such as carrier mobility and effective channel geometry, was determined from these fits to be 0.020 nA/mV² for the top array and 0.014 nA/mV² for the bottom array. These measurements confirm robust transistor operation and good current saturation at cryogenic temperatures, essential for defining and manipulating quantum dots.

4.2.3 Pinch-off measurements of individual gates

The pinch-off behavior of individual gates was characterized at cryogenic temperatures using the same measurement protocol as in the room-temperature tests. A source-drain bias of 10 mV was applied. During the sweep of a target gate from -1.0 V to 1.5 V in 10 mV increments,

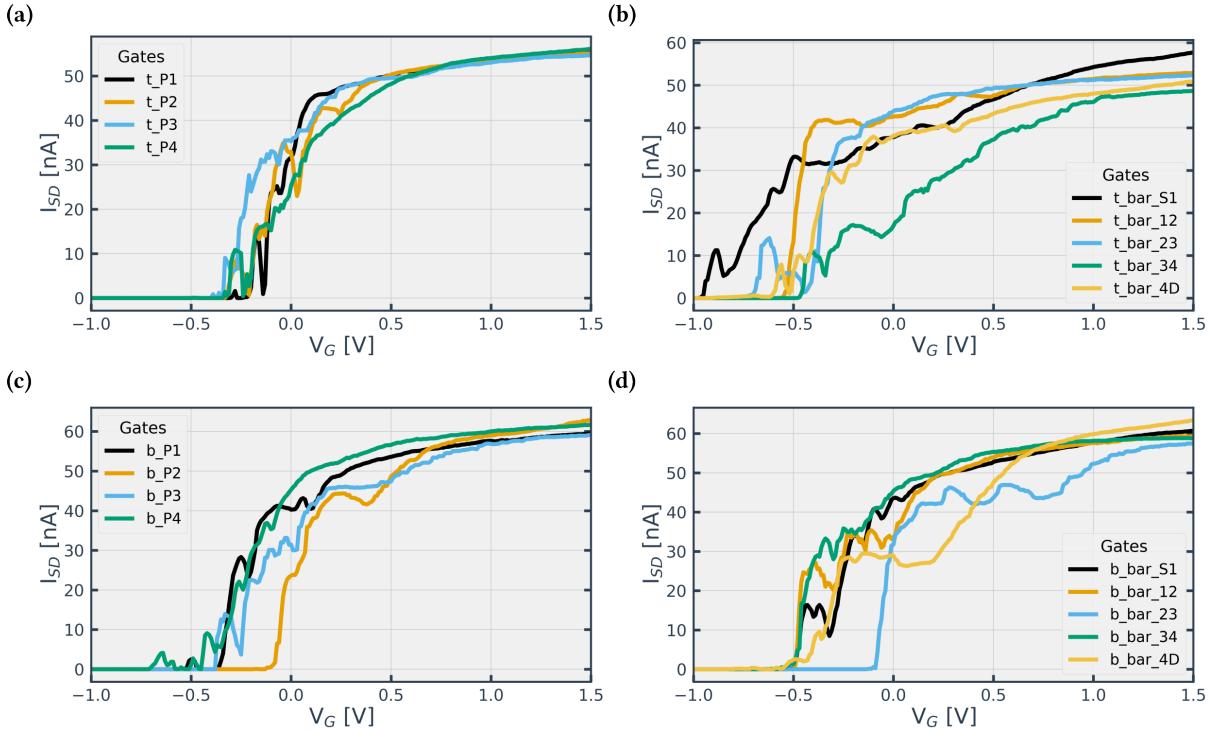


Figure 4.5: Cryogenic pinch-off characteristics of individual gates. Each plot shows the source-drain current (I_{SD}) as a function of the swept gate voltage (V_G), measured at a cryogenic temperature of approximately 8 mK. A fixed source-drain bias of $V_{SD} = 10$ mV was applied. During each sweep, the target gate was varied from -1.0 V to 1.5 V in 10 mV steps, while all other gates in the same array and both reservoirs were held at 800 mV. Gates in the opposite array were grounded. (a) Top-array plunger gates; (b) Top-array barrier gates; (c) Bottom-array plunger gates; (d) Bottom-array barrier gates. These characteristics demonstrate individual gate control and their respective pinch-off behavior under cryogenic conditions.

both reservoirs and all non-swept gates within the same array were held at 800 mV. All finger gates in the opposite array were grounded.

Figure 4.5 presents the resulting source-drain current I_{SD} as a function of gate voltage V_G for individual plunger and barrier gates. Panels (a) and (b) correspond to gates on the top array, while (c) and (d) show gates on the bottom array. Each curve exhibits a clear onset of conduction as V_G increases, transitioning from a low-current regime to a saturated current plateau. The general switching behavior is consistent across the gate array, indicating effective individual gate control, although minor variations in threshold and pinch-off voltages are observed. These discrepancies are likely attributable to fabrication-induced differences such as local gate geometry or gate-to-channel capacitance variations. The extracted threshold and pinch-off voltages for all individual gates are comprehensively summarized in Figure 4.6. Each bar in this visualization represents a single plunger or barrier gate, segmented into three distinct regions determined by an automated machine learning model. These regions include: the cutoff region (red), indicating gate voltages below the threshold where the current remains negligible due to channel depletion; the transition region (yellow), spanning between the threshold and pinch-off voltages, characterized by a rapid increase in current; and the sat-

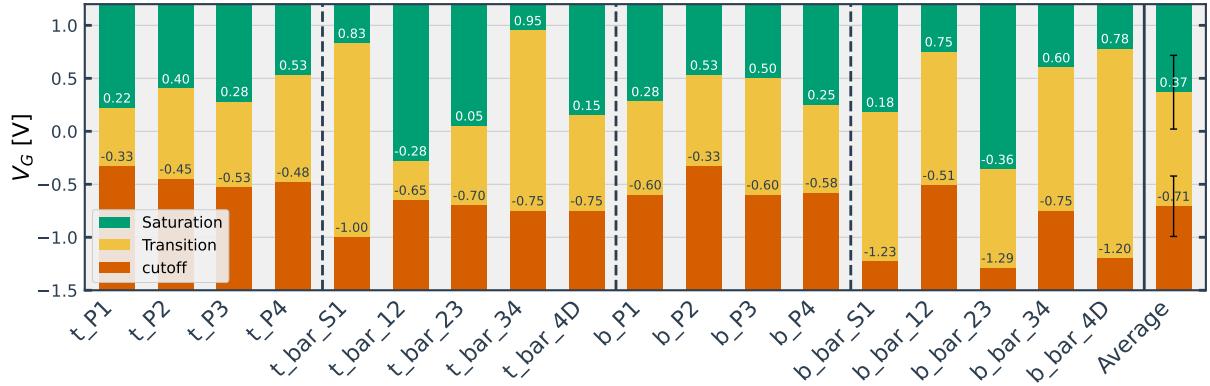


Figure 4.6: Summary of individual gate threshold, transition, and pinch-off voltages at cryogenic temperature. Each bar represents a single plunger or barrier gate, with an additional bar representing the average across all individual gates (rightmost bar). The bars are segmented into three distinct regions, determined by an automated machine learning model: the cutoff region (red) indicates gate voltages below the threshold, where the channel is fully depleted and the current remains negligible; the transition region (yellow) spans the voltage range from the threshold to the pinch-off, characterized by a rapid increase in channel conductance; and the saturation region (green), beyond the pinch-off voltage, corresponds to the gate voltage range where the source-drain current reaches a near-constant, saturated value.

ration region (green), beyond the pinch-off voltage, where the current reaches a near-constant value. The rightmost bar, labeled “Average”, represents the mean threshold, transition, and saturation voltages calculated across all individual gates. This detailed visualization enables a direct comparison across all gates and highlights minor non-uniformities, particularly among certain barrier gates, which exhibit broader or shifted transition regions. Such variations may result from local disorder or differences in electrostatic coupling efficiency.

Notably, when comparing these individual gate characteristics to the uniform gate sweep measurements presented in Figure 4.3(a), a key observation emerges. For instance, the threshold voltage of the uniform channel sweep (approximately 0.32 V) is significantly higher than the average individual gate threshold (around -0.71 V) and even exceeds the threshold of most individual gates. Similarly, the uniform pinch-off voltage (1.08 V for top channel, 1.25 V for bottom channel) is notably greater than the highest individual pinch-off voltage observed (e.g., 0.95 V for t_bar_34, 0.78 V for b_bar_4D). This phenomenon suggests that in a multi-gate device where gates are in series, the overall channel conductance in the uniform sweep is effectively governed by the “hardest-to-open” or “hardest-to-pinch-off” gate within the array. In other words, the complete channel opening (or closing) requires a gate voltage sufficient to overcome the highest individual threshold or pinch-off barrier present in the series of gates. The accurate extraction of these threshold and pinch-off voltages serves as a crucial guideline for subsequent quantum experiments, facilitating precise and selective control over individual gate states by ensuring specific gates are open while others are held closed for quantum dot formation.

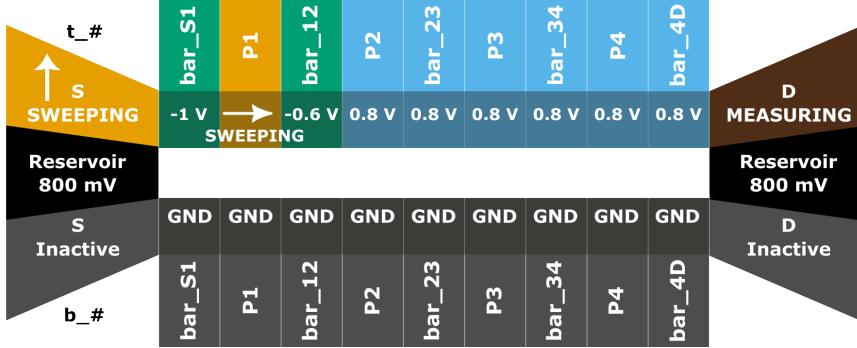


Figure 4.7: Example schematic illustrating the setup for a Coulomb diamond measurement on the t_P1 plunger gate. The source-drain bias (V_{SD}) was swept symmetrically from -10 mV to 10 mV, while the t_P1 gate voltage was incrementally stepped. Barrier gates t_bar_S1 and t_bar_12 were biased near their respective threshold voltages to define the dot, and other gates in the same array were held at 0.8 V to ensure channel conduction. The reservoir was biased at 800 mV.

4.2.4 Coulomb diamond spectroscopy

Coulomb diamond spectroscopy is a key characterization technique for quantum dot devices. It provides direct evidence of Coulomb blockade behavior and allows for a qualitative and quantitative assessment of the confinement potential and electrostatic stability of the formed quantum dot. To obtain well-defined diamond patterns, a voltage was applied to the target plunger gate while the source-drain bias V_{SD} was swept symmetrically around 0 V. The corresponding plunger gate voltage was incrementally stepped. This intricate measurement procedure was fully automated using the custom-developed gate-manager script.

To enhance the visibility and robustness of the diamond features, measurements were performed in the high-electron regime. The barrier gate voltages were adjusted to be near their respective threshold values, and the target plunger gate voltage was increased until clear transport peaks appeared, indicating electron conduction through the dot. The remaining gates in the same array were held at 0.8 V to provide a stable background potential and ensure proper channel formation. An example configuration for measuring the t_P1 gate is illustrated in Figure 4.7.

Coulomb diamond measurements were systematically carried out for all eight plunger gates in the device to comprehensively assess their electrostatic control and confinement quality. The resulting differential current dI_{SD}/dV_{SD} maps are shown in Figure 4.8. Panels (a-d) correspond to the top array gates (t_P1 to t_P4), while panels (e-h) display data for the bottom array gates (b_P1 to b_P4). In each case, the differential current is plotted as a function of source-drain bias V_{SD} and the respective plunger gate voltage V_p . These measurements reveal notable variations in quantum dot behavior across different gate positions.

Gates t_P1, t_P4, b_P1, and b_P4 exhibit clean, periodic Coulomb diamonds with sharp, symmetric edges and consistent periodicity. These features are characteristic of well-defined

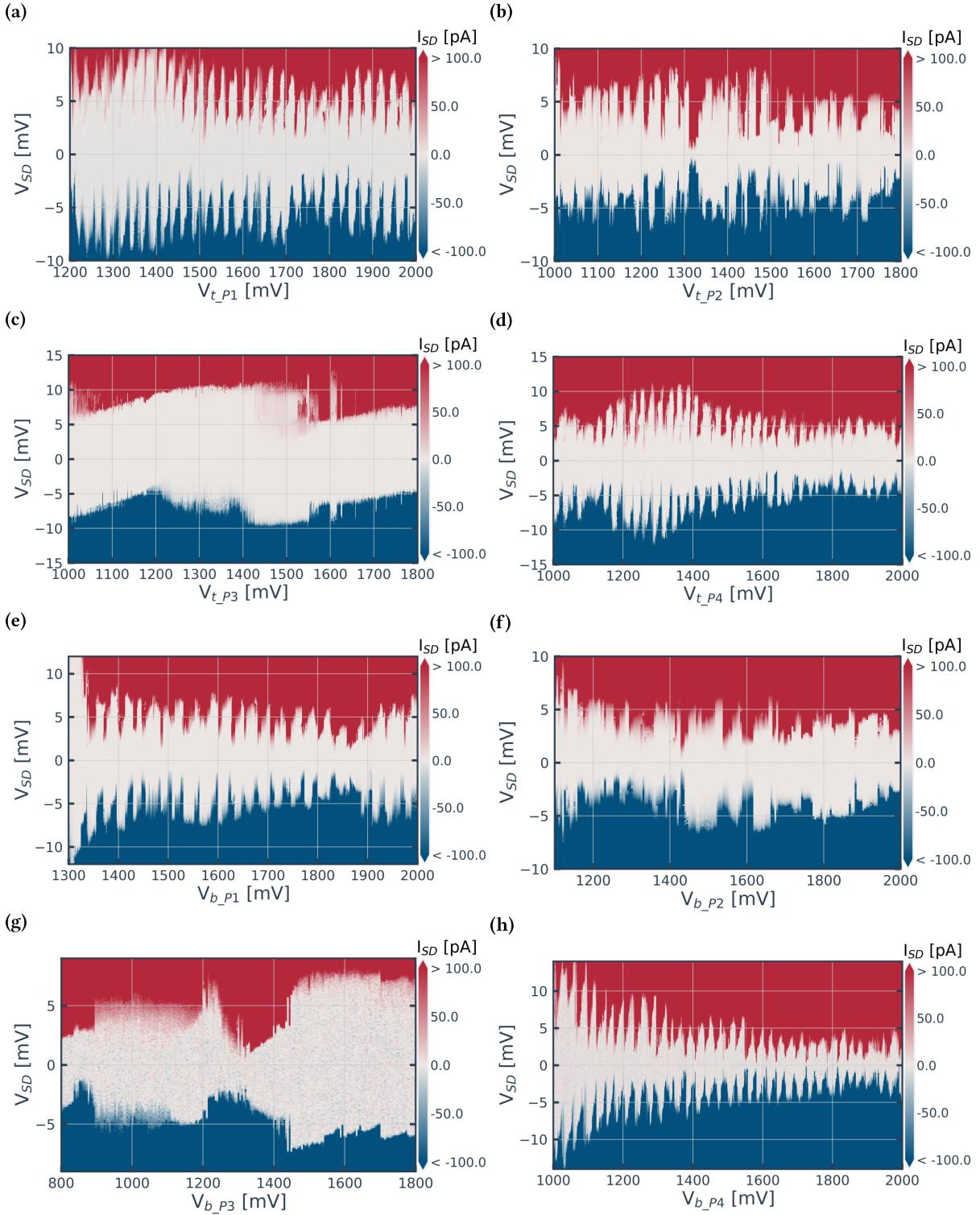


Figure 4.8: Cryogenic Coulomb diamond measurements for individual plunger gates. Each panel displays the differential current (dI_{SD}/dV_{SD}) as a function of source-drain bias (V_{SD}) and the respective plunger gate voltage (V_P). These measurements were performed at cryogenic temperatures. Panels (a-d) correspond to the top array plunger gates (t_P1 to t_P4), and panels (e-h) correspond to the bottom array plunger gates (b_P1 to b_P4). Gates t_P1 , t_P4 , b_P1 , and b_P4 clearly exhibit clean, periodic Coulomb diamonds, indicative of robust single-electron confinement. Other gates show features suggesting deviations from ideal single-dot behavior, such as multiple dots, poor confinement, or the influence of local disorder.

single-dot behavior, indicating stable tunnel barriers and minimal influence from spurious charge traps or significant disorder in the local potential environment. The size of the diamonds provides information on the charging energy E_c and the lever arm α of the plunger gate.

By contrast, gates such as t_P2 and b_P2 show less regular diamond structures. While current blockade regions and charging transitions are still visible, the boundaries are more uneven and the sizes of the diamonds vary. This irregularity suggests asymmetries in tunnel coupling, fluctuations in the local potential environment, or the presence of multiple weakly coupled dots contributing to the transport.

Gates t_P3 and b_P3 display the most irregular behavior. The diamond features are faint or fragmented, and the current maps are dominated by noisy or erratic signals. These signatures likely result from strong disorder, insufficient electrostatic confinement leading to ill-defined dots, or the strong influence of multiple weakly coupled quantum dots that cannot be clearly resolved.

Overall, as in Figure 4.9, these Coulomb diamond measurements confirm that t_P1, t_P4, b_P1, and b_P4 offer the most stable and reproducible single-electron confinement. These specific gates are therefore well-suited for subsequent quantum experiments, particularly those aimed at extracting and characterizing charge noise, as their well-defined behavior simplifies interpretation.

4.2.5 Field-effect mobility analysis

Field-effect mobility μ is a critical parameter characterizing the transport efficiency in semiconductor devices and directly impacts quantum dot performance. This section details the extraction of mobility from both uniform gate sweeps and individual Coulomb diamond measurements at cryogenic temperatures.

Based on the device specifications provided by SemiQon, each gate finger has a nominal length of $L_{\text{finger}} = 40$ nm. With nine gate fingers forming the full transport channel, the total channel length is $L = 9 \times L_{\text{finger}} = 360$ nm. The effective channel width per gate is $W = 75$ nm. The gate oxide thickness is $t_{\text{ox}} = 17$ nm. Assuming a silicon dioxide (SiO_2) dielectric with a relative permittivity $\epsilon_r = 3.9$ and vacuum permittivity ϵ_0 , the gate capacitance per unit area is calculated as $C_i = \epsilon_r \epsilon_0 / t_{\text{ox}} \approx 203 \text{ nF/cm}^2$.

At a base temperature of 7 mK, using the uniform gate sweep data discussed in Section 4.2.1, the source-drain bias was set to $V_{\text{SD}} = 10$ mV. The field-effect mobility μ can be extracted from the process transconductance parameter K_n , which was obtained from the saturation current fits presented in Figures 4.4(b) and (d). Using the relationship $\mu = K_n / (C_i W / L)$, and with extracted K_n values of 0.020 nA/mV² for the top array and 0.014 nA/mV² for the bottom array, the calculated field-effect mobilities are $\mu = 472.9 \text{ cm}^2/\text{V}\cdot\text{s}$ for the top array and $\mu = 331.0 \text{ cm}^2/\text{V}\cdot\text{s}$ for the bottom array.

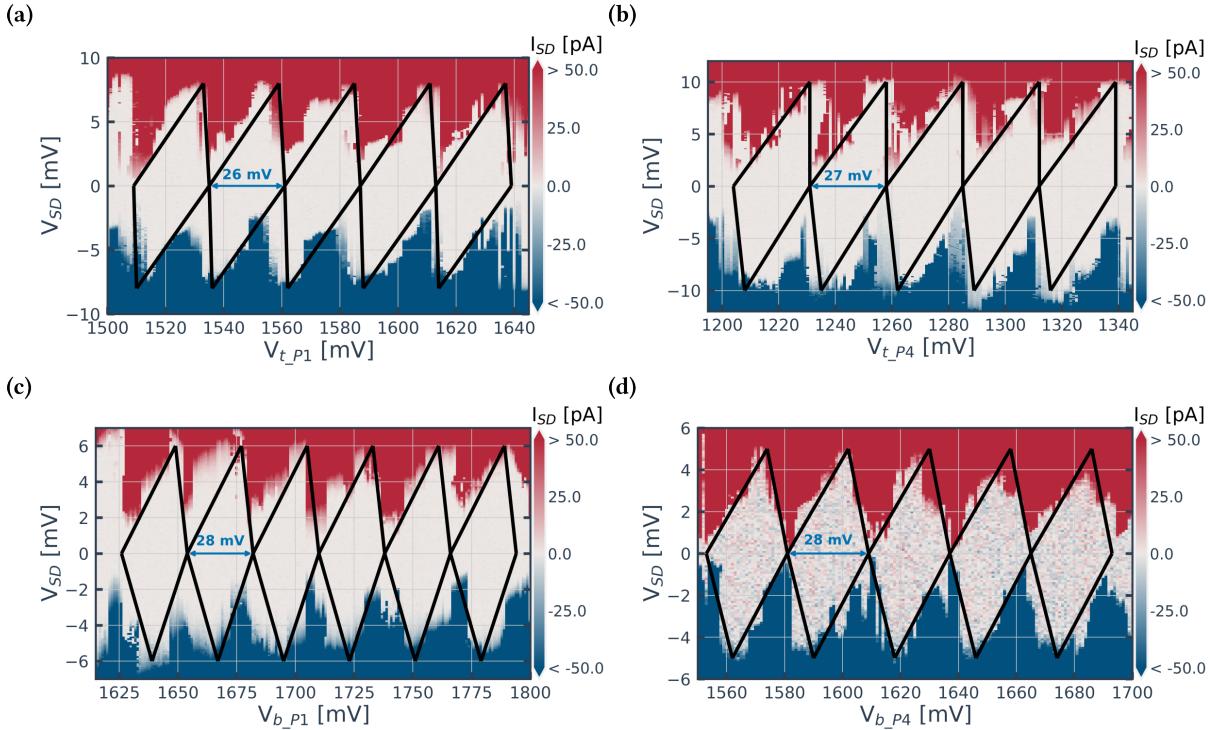


Figure 4.9: Representative Coulomb diamonds for well-confined quantum dots. Current I_{SD} maps as a function of source-drain bias (V_{SD}) and plunger gate voltage (V_P), measured at cryogenic temperatures. The solid black lines delineate the boundaries of the Coulomb blockade regions. The annotated values (e.g., “26 mV”) indicate the width of the diamond along the V_G axis. (a) Top plunger gate t_P1 ; (b) Top plunger gate t_P4 ; (c) Bottom plunger gate b_P1 ; (d) Bottom plunger gate b_P4 .

For individual gate segments, the Coulomb diamond measurements described in Section 4.2.4 provide an alternative method to estimate the total capacitance of a single quantum dot C_Σ . This is derived from the height of the Coulomb diamond along the V_{SD} axis, which corresponds to $C_\Sigma = e/\Delta V_{SD}$. As shown in Figure 4.8, the measured ΔV_{SD} for diamonds typically ranges from 5 mV to 10 mV under different gate voltages, although some gates’ diamonds are not well-defined. The effective area of a single quantum dot segment can be approximated as $A = W \times L_{\text{finger}} = 3000 \text{ nm}^2$. Using this area, the effective gate capacitance per unit area for a single dot is $C_{i,\text{dot}} = C_\Sigma/A$, from 533.3 to 1066.7 nF/cm².

Considering the transconductance (dI_{SD}/dV_G) for individual gate segments, the control ability is quite variable. For example, in Figure 4.5 the strongest transconductance observed is for b_bar_23 , which is around 400 nA/V, while the weakest is for t_bar_34 , at approximately 30 nA/V. With $V_{SD} = 10$ mV, the extracted field-effect mobility for a single dot ranges from $1.4 \text{ cm}^2/\text{V}\cdot\text{s}$ to $40 \text{ cm}^2/\text{V}\cdot\text{s}$. This value is significantly lower than the full channel mobility. One possible explanation for this discrepancy is that when measuring the Coulomb diamond, the barrier gates are almost closed, significantly impeding charge movement. Another potential reason is the lack of clarity or “blurring” in some quantum dot diamonds, which may indicate the presence of multiple dots under a single gate or other complex electrostatic conditions,

leading to an uncertain capacitance value.

Chapter 5

Noise measurements

Building on the initial device characterization, this chapter focuses on the central aim of this study: investigating charge noise in semiconductor quantum dots. It details the experimental procedures used to perform current noise measurements and analyzes the resulting frequency-dependent spectra across various gate-defined quantum dots. Emphasis is placed on spatial variability in noise behavior, particularly under different plunger gates, to identify the dominant noise sources and their spectral characteristics. These findings shed light on the relationship between device layout, gate geometry, and the surrounding charge environment, which can inspire low-charge-noise future quantum dot architectures aimed at qubit applications.

5.1 Selection of stable Coulomb peaks

To identify suitable regions for charge noise characterization, we examined quantum dots that exhibited clear Coulomb diamond patterns, specifically t_P1, t_P4, b_P1, and b_P4, as shown in Figure 4.9. In these configurations, stable conductance peaks were observed when sweeping the plunger gate voltage while monitoring the source-drain current I_{SD} .

Among them, the gate configuration b_P4 displayed particularly clear Coulomb features. As shown in Figure 5.1(a), a two-dimensional map of I_{SD} as a function of source-drain bias V_{SD} and plunger gate voltage V_{b_P4} reveals well-defined Coulomb diamonds, characteristic of a robustly formed quantum dot with clearly resolved charging energy. A line cut at fixed $V_{SD} = 1.478\text{mV}$, presented in Figure 5.1(b), shows periodic Coulomb oscillations in I_{SD} , with a peak spacing of $\Delta V_{SD} = 28.4 \pm 2.9\text{ mV}$. The consistency, sharpness, and reproducibility of these peaks confirm the device's stability and its suitability for charge noise measurements.

In contrast, quantum dots such as t_P2, t_P3, b_P2, and b_P3 did not display well-defined Coulomb diamonds, as shown in Figure 4.8(b)(c)(f)(g). In these cases, the origin of the observed conductance peaks was unclear. To evaluate their stability, the plunger gate voltage

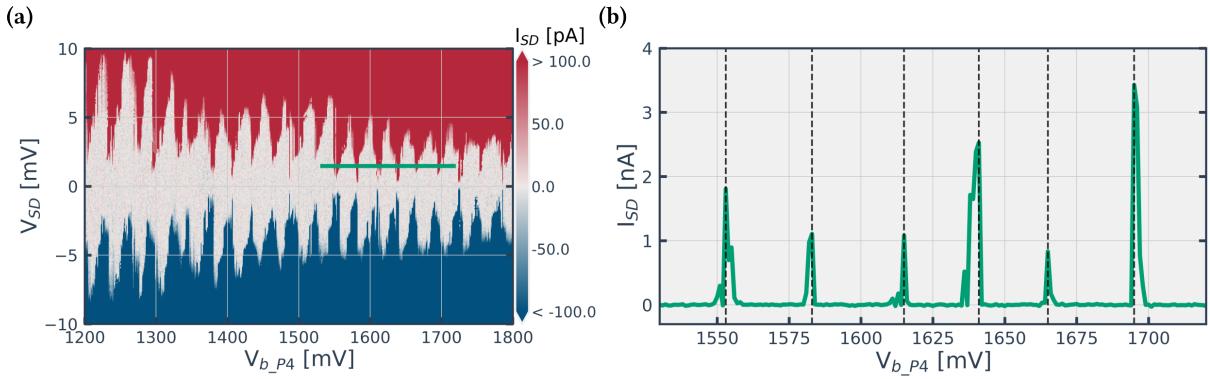


Figure 5.1: Coulomb diamond measurement for the QD under gate b_P4 , showing stable and periodic conductance peaks. (a) Source-drain current I_{SD} (color scale) plotted as a function of source-drain bias V_{SD} and plunger gate voltage V_{b_P4} . The well-resolved Coulomb diamonds indicate a stable quantum dot with clearly defined charging behavior. (b) Line cut at fixed $V_{SD} = 1.478$ mV, showing periodic Coulomb oscillations in I_{SD} , with peak spacing $\Delta V_{SD} = 28.4 \pm 2.9$ mV. The consistency and sharpness of the peaks indicate that this region is well suited for charge noise characterization.

was swept in 1 mV steps while measuring I_{SD} , repeated three times at one-minute intervals. As shown in Figure 5.2, the peak positions and shapes varied significantly between consecutive runs, even though the time span of each measurement was short.

These instabilities are likely indicative of a less-controlled electrostatic environment or the presence of mobile charge traps in close proximity to the quantum dot region [54]. Fluctuations in the position or occupancy of these traps can lead to shifting background potentials, resulting in erratic and irreproducible peak behavior. This suggests that these particular gate configurations may not have formed quantum dots with sufficient isolation from extrinsic charge fluctuations [55], or that the device architecture in these specific areas is more susceptible to trapping/detrapping events. This made it difficult to determine the peak edges or associate the features with specific physical mechanisms, rendering these configurations unsuitable for reliable charge noise analysis.

Based on the observations, this work focuses on the quantum dots that exhibit stable Coulomb peaks, namely t_P1 , t_P4 , b_P1 , and b_P4 , for charge noise measurements.

5.2 Converting time series to frequency spectra

To analyze charge noise, it is often more informative to examine its characteristics in the frequency domain. However, the current fluctuations are initially measured in the time domain. Therefore, a conversion is required to transform time-resolved current traces into frequency-resolved information.

In these experiments, the source-drain current I_{SD} is measured at a fixed gate voltage, which refers to a fixed position on a Coulomb peak. Ideally, if the quantum dot were perfectly stable

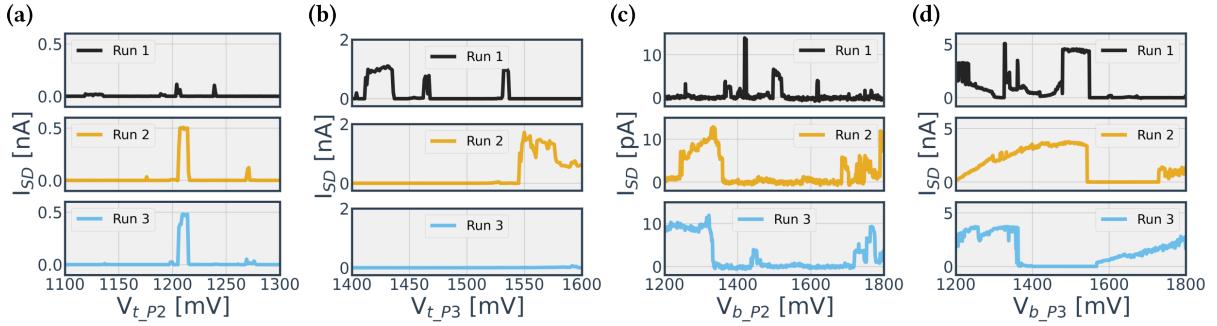


Figure 5.2: Instability of conductance peaks in repeated measurements. Each panel shows three consecutive sweeps of the plunger gate voltage with 1 mV steps, measuring the source-drain current I_{SD} . Substantial variations in both peak shape and position are evident between runs, highlighting the lack of stability. Panels correspond to different gates: (a) t_P2, (b) t_P3, (c) b_P2, and (d) b_P3. These instabilities prevent accurate charge noise extraction from these configurations.

and the measurement system noise-free, I_{SD} would remain constant over time, resulting in a perfectly flat line. Even such ideal traces in real measurement systems may still exhibit minimal background electronic noise, for example, from environmental interference or instrument electronics. However, as conceptually illustrated in Figure 5.3, the measured I_{SD} exhibits significant fluctuations around its mean value, even at a fixed gate voltage (as shown by the blue trace in Figure 5.3(b)), corresponding to a measurement on the Coulomb peak). This observed temporal variation indicates the presence of both intrinsic charge noise within the quantum dot and external measurement system noise, which prevent the current from being perfectly stable over time.

The current traces were digitized with a sampling interval of $\Delta t = 50 \mu\text{s}$, corresponding to a sampling rate of 20 kHz. Each trace was recorded for a total duration of $T = 1000 \text{ s}$, resulting in 20,000 data points. This sets the minimum resolvable frequency to approximately $1/T \approx 1 \text{ mHz}$.

For each Coulomb peak, three characteristic gate voltage positions were selected: the rising or falling edge of the peak (where the current changes most rapidly with gate voltage), the peak center, and a background region away from the peak. These regions respectively correspond to maximum charge sensitivity, moderate sensitivity, and a baseline dominated by white noise. Most measurements adhered to this three-point sampling approach, though adjustments were made in cases where the peak position shifted during acquisition.

After collecting the time series data, it is converted into the frequency domain using the FFT, which decomposes the signal into its constituent frequency components. This transformation allows for the identification of dominant noise features across a broad frequency range. To estimate the PSD of the current fluctuations, the `scipy.signal.welch` function with a Hanning window is employed [56]. Welch's method enhances the statistical reliability of the PSD by segmenting the time trace into overlapping windows, applying the FFT to each segment, and

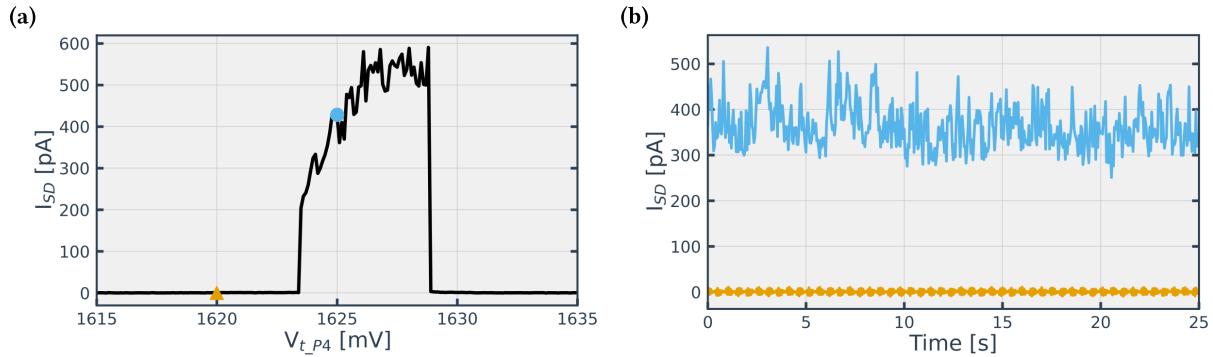


Figure 5.3: (a) Source-drain current I_{SD} as a function of gate voltage V_{t_P4} , displaying a typical Coulomb peak. The orange triangle indicates a gate voltage where the current is off-resonance (zero current), and the blue circle marks a gate voltage on the rising edge of the Coulomb peak. (b) Time traces of the source-drain current I_{SD} measured at fixed gate voltages corresponding to the points marked in (a). The orange trace (orange triangle) shows current fluctuations when the quantum dot is off-resonance. The blue trace (blue circle) illustrates the significant temporal fluctuations in I_{SD} even when measured at a fixed point on the Coulomb peak. This deviation from an ideal flat line highlights the combined effects of intrinsic charge noise and measurement system noise.

averaging the results [57].

5.3 Frequency-resolved noise characterization

The charge noise measurements were performed at a base temperature of approximately 7 mK. Across all QDs selected under the four gates, the PSDs reveal characteristic low-frequency behavior commonly observed in semiconductor QD systems. In particular, at frequencies below around 10 Hz, the spectra exhibit a power-law dependence consistent with $1/f^\beta$ noise, as shown in Figure 5.4(a). In this example, the extracted exponent is $\beta = 1.15$, which aligns with the expected value for an ensemble of fluctuating TLSs with a uniform distribution of switching rates. This $1/f$ type noise is a ubiquitous feature in semiconductor devices and is typically attributed to the trapping and de-trapping of charges in defects located at interfaces or within the bulk material [58, 59].

In some cases, however, the PSD deviates from a pure $1/f^\beta$ profile. As illustrated by the green trace in Figure 5.4(b), the spectrum displays a pronounced roll-off at higher frequencies. This suggests the influence of localized TLFs with a non-uniform or narrow switching rate distribution [60]. In such cases, a combined model that incorporates both a $1/f$ term and a Lorentzian component provides a better description of the noise spectrum [61]. The PSD is modeled using the expression

$$S \propto \frac{A}{f^\beta} + \frac{B}{f^2/f_c^2 + 1}, \quad (5.1)$$

where A , B , β , and the characteristic frequency f_c are fitting parameters. This formulation captures both the broad-band background noise and discrete contributions from individual

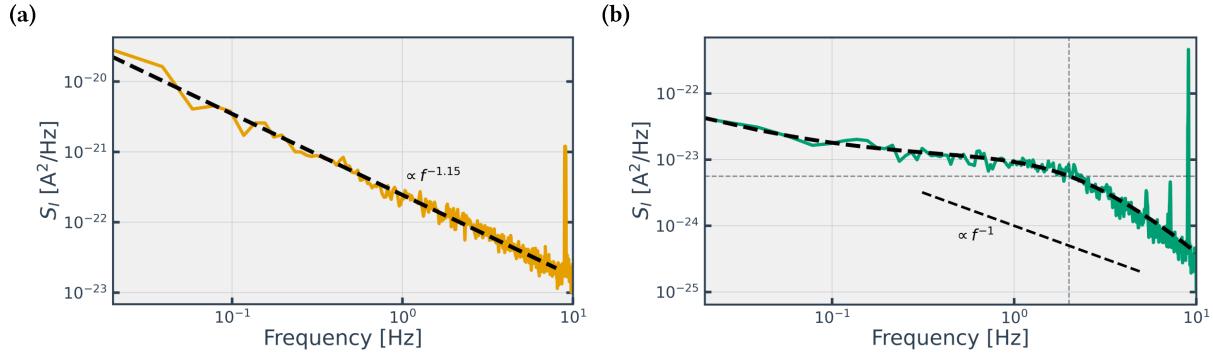


Figure 5.4: Examples of measured current noise PSDs. (a) The spectrum exhibits a $1/f^\beta$ dependence with $\beta = 1.15$, indicating dominant low-frequency charge noise. (b) A combined model $A/f^\beta + B/(f^2/f_c^2 + 1)$ fits the data well, capturing both $1/f$ and Lorentzian components. Fitted parameters are $\beta = 0.89$ and $f_c = 2$ Hz.

fluctuators. In the example of Figure 5.4(b), the best-fit parameters are $\beta = 0.89$ and $f_c = 2$ Hz.

The PSDs of charge noise measured at four different plunger gates, labeled t_P1, t_P4, b_P1, and b_P4, are shown in Figures 5.5 to 5.8. Each figure includes four subplots, corresponding to different Coulomb peaks from the same quantum dot. The PSDs were obtained from current fluctuation traces recorded in the time domain during direct current transport through the dot. Across the four quantum dots, the fitted noise exponents typically range from 0.8 to 1.3. This power law scaling indicates that the dominant charge noise originates from ensembles of TLFs with a broad distribution of switching times. Such behavior is consistent with charge traps or defects located near the oxide interface or within the substrate. At a reference frequency of 1 Hz, the charge noise amplitude is typically around $10 \text{ pA}/\sqrt{\text{Hz}}$, while the background level measured far from the Coulomb peaks is approximately $0.3 \text{ pA}/\sqrt{\text{Hz}}$. This background level represents the experimental noise floor, primarily dominated by the room-temperature pre-amplifier of the current meter and the input impedance of the measurement cables.

QD under gate t_P1 As shown in Figure 5.5, the power spectral densities measured at gate t_P1 exhibit characteristic low-frequency behavior dominated by a $1/f^\beta$ trend. Across the four Coulomb peaks analyzed, the extracted exponent is $\beta = 1.014 \pm 0.266$, consistent with charge fluctuations originating from a broad ensemble of TLFs. The spectra show relatively uniform magnitude and shape across the different peaks, suggesting that the local electrostatic environment and distribution of charge traps near this gate remain stable during the measurement. A slight variation in spectral magnitude is observed across different positions within the same Coulomb peak. This may be attributed to the full depletion of a nearby charge trap at lower plunger gate voltage V_{t_P1} , which reduces its contribution to noise. However, further investigation is needed to clarify the physical origin and spatial location of the responsible trap [61]. At a reference frequency of 1 Hz, the current noise amplitude is approximately $4.14 \text{ pA}/\sqrt{\text{Hz}}$, while the background white noise floor remains around $0.3 \text{ pA}/\sqrt{\text{Hz}}$.

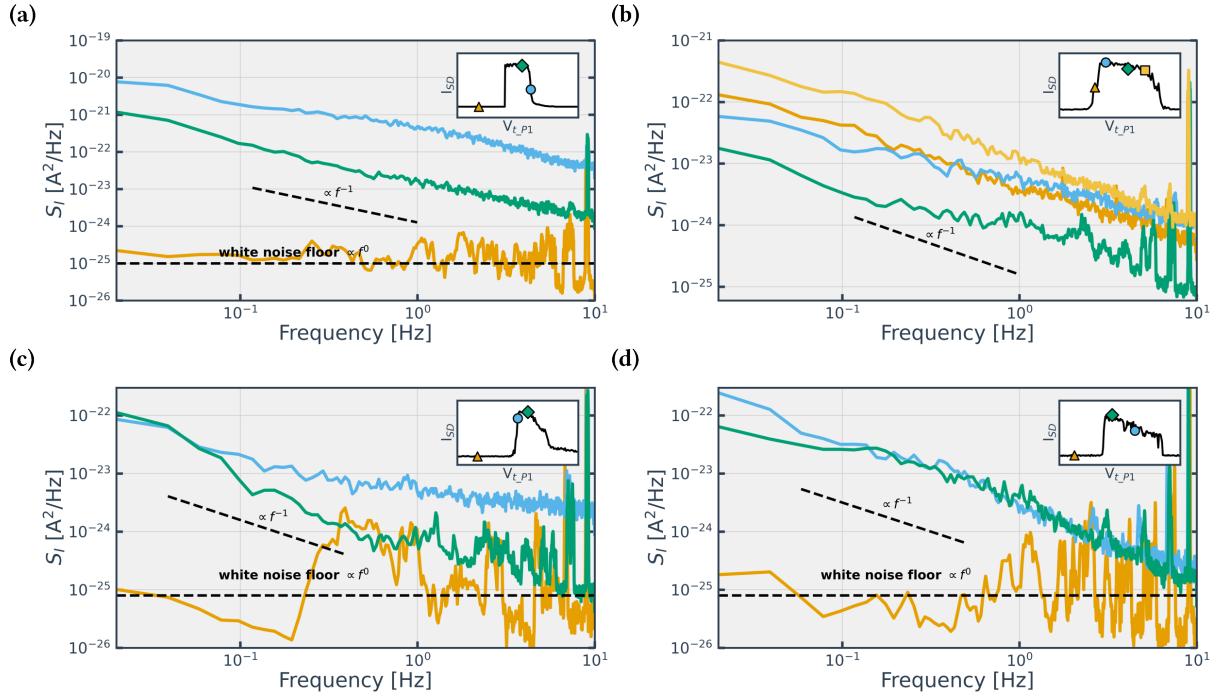


Figure 5.5: Current noise power spectral densities measured at gate **t_P1**. (a)-(d) show spectra recorded at different Coulomb peaks. All plots are presented on a log-log scale and reveal clear $1/f^\beta$ behavior at low frequencies. The white noise floor is estimated to be approximately $0.3 \text{ pA}/\sqrt{\text{Hz}}$. Dashed reference lines proportional to $1/f$ are included for comparison.

QD under gate **t_P4** Compared to the QD under gate **t_P1**, the QD under gate **t_P4** exhibits larger fluctuations in the power spectral densities and more pronounced deviations from the ideal $1/f^\beta$ scaling. This behavior suggests a more complex local noise environment, likely influenced by strongly coupled or unstable charge traps. While most spectra still follow a general $1/f^\beta$ trend, the elevated noise floor indicates a higher density of active fluctuators near the QD. Some traces also show significant curvature, especially at higher frequencies, consistent with Lorentzian features arising from individual fluctuators with discrete switching rates. Fitting the PSD using the expression $A/f^\beta + B/(f^2/f_c^2 + 1)$ yields typical values of $\beta = 0.766 \pm 0.270$ and $f_c = 2 \text{ Hz}$. At a reference frequency of 1 Hz, the average current noise amplitude is approximately $16.41 \text{ pA}/\sqrt{\text{Hz}}$, while the white noise floor remains near $0.3 \text{ pA}/\sqrt{\text{Hz}}$. Among the measurements at **t_P4**, two data points from peak 2 in Figure 5.6(b) display unusually high noise levels, with values exceeding $80 \text{ pA}/\sqrt{\text{Hz}}$ at 1 Hz. These outliers are likely associated with transient switching events or a nearby strongly coupled charge trap. Although they are retained for completeness in the figure, they are excluded from statistical averaging and error bar calculations to avoid distortion of the typical device performance. One trace, shown in orange, corresponds to a measurement taken at the sharp edge of a Coulomb peak, where charge sensitivity is highest. In the time domain, this trace exhibits strong switching behavior, with the current jumping between two distinct levels. This suggests that the system is experiencing non-stationary dynamics, likely due to a bistable charge configuration [62, 63, 64]. Because this behavior reflects instability rather than intrinsic charge noise,

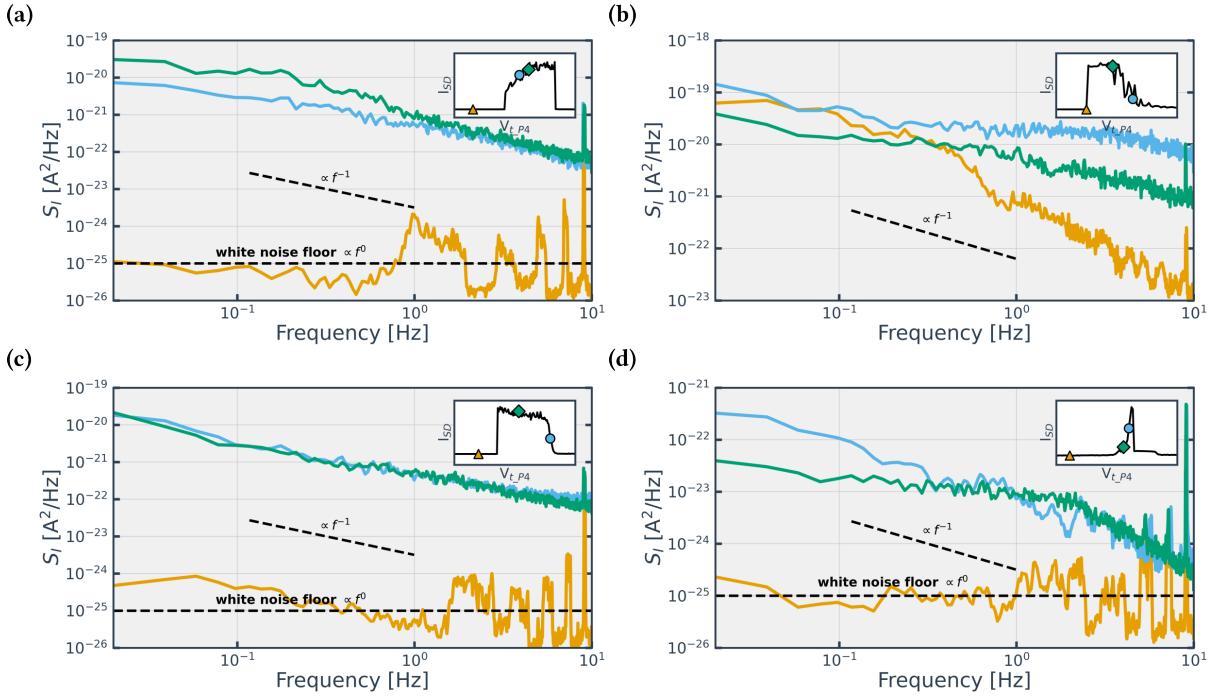


Figure 5.6: Current noise PSDs measured at gate **t_P4**. Panels (a) to (d) present data recorded at different Coulomb peaks. Several spectra deviate from ideal $1/f^\beta$ scaling and are better described by the expression $A/f^\beta + B/(f^2/f_c^2 + 1)$, which captures both broadband background noise and Lorentzian contributions from individual fluctuators. The orange spectrum corresponds to a measurement taken at the sharp edge of a Coulomb peak, where switching events are observed in the time trace. These non-stationary dynamics result in a steeper slope and enhanced noise amplitude. This trace is retained for completeness but excluded from statistical analysis. Dashed lines proportional to $1/f$ are included as reference.

it is excluded from subsequent analysis. Only traces taken near the top and stable edge of the Coulomb peaks are used in further calculations, in order to isolate the contributions from stationary charge noise processes.

QD under gate b_P1 The PSDs obtained from gate b_P1 indicate lower current noise compared to t_P1 and t_P4, and show excellent consistency across different Coulomb peaks. The spectra exhibit well-defined $1/f^\beta$ scaling, with minimal variation in magnitude and shape between peaks. This uniformity suggests that the electrostatic environment near b_P1 is relatively clean, with fewer active fluctuators contributing to charge noise. These features make b_P1 a promising configuration for future charge-sensitive or spin qubit experiments that require noise stability and spectral predictability. Quantitatively, the fitted exponent is $\beta = 1.179 \pm 0.291$, consistent with a broad ensemble of slow fluctuators. The current noise amplitude at 1 Hz is $S_I^{1/2}(1 \text{ Hz}) = 31.31 \pm 11.80 \text{ pA}/\sqrt{\text{Hz}}$.

QD under gate b_P4 Among all four gates, b_P4 exhibits the lowest and most stable current noise across the measured frequency range. The extracted exponent is $\beta = 1.268 \pm 0.234$, and the current noise amplitude at 1 Hz is $S_I^{1/2}(1 \text{ Hz}) = 8.69 \pm 4.76 \text{ pA}/\sqrt{\text{Hz}}$. The PSDs for

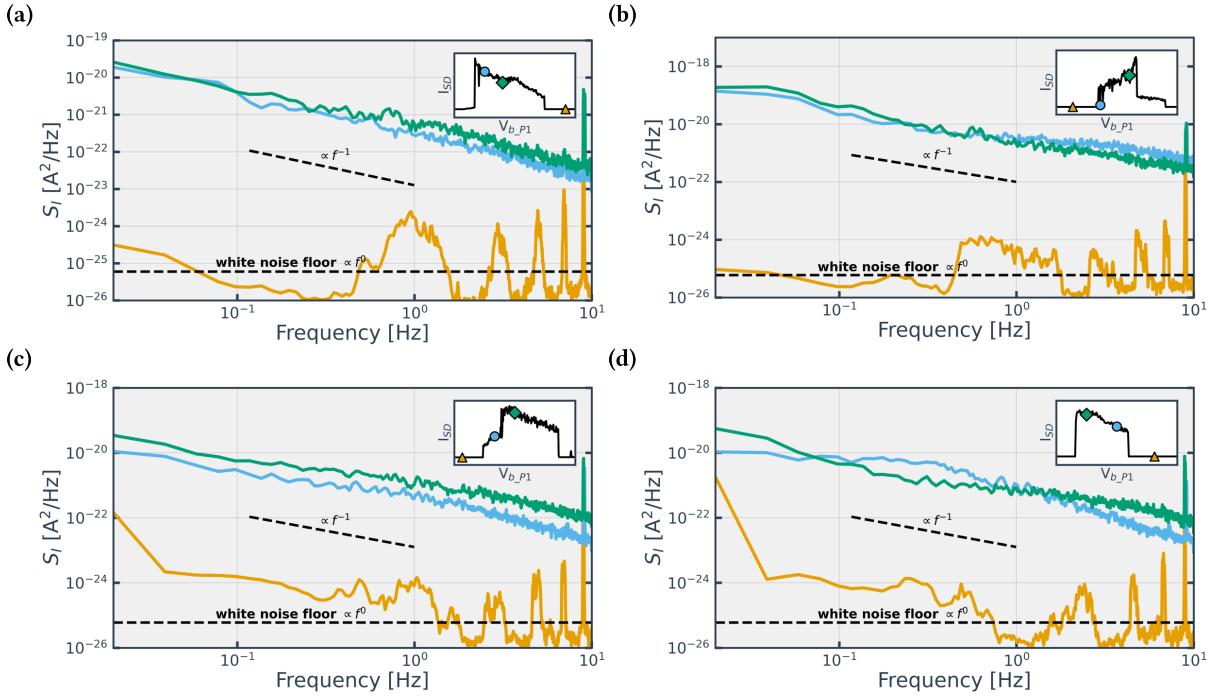


Figure 5.7: Current noise power spectral densities measured at gate **b_P1**. (a)-(d) correspond to different Coulomb peaks. The **b_P1** configuration exhibits lower current noise compared to both **t_P1** and **t_P4**, with well-defined $1/f^\beta$ scaling and minimal variation between peaks. Dashed lines proportional to $1/f$ are shown for reference.

b_P4 remain consistently below those of **t_P1**, **t_P4**, and even **b_P1**, particularly in the sub-10 Hz regime where charge noise is most relevant for qubit dephasing. This behavior suggests either weaker coupling to environmental charge fluctuations or a significantly lower density of nearby traps and defects. The $1/f^\beta$ scaling is consistently observed across all Coulomb peaks, and no distinct Lorentzian features are present, indicating the absence of dominant discrete fluctuators. These properties make **b_P4** the most favorable configuration among the tested gates for precise charge noise characterization and stable operation of charge- or spin-based qubits.

5.4 Discussion

An interesting observation is that among all four gates, **b_P4** not only exhibited the lowest current noise but also displayed the clearest and most well-defined Coulomb diamonds, as discussed in Section 4.2.4. This co-occurrence suggests that diamond clarity may serve as an indirect indicator of overall device quality, particularly in terms of charge stability and a reduced level of environmental noise. While Coulomb diamonds reflect static transport behavior and noise spectra probe dynamic fluctuations, both are influenced by the same underlying physical factors, including material quality, gate geometry, and the distribution of charge traps [65]. As such, a well-resolved Coulomb diamond may qualitatively correlate with lower charge noise, although it does not provide a direct or quantitative prediction.

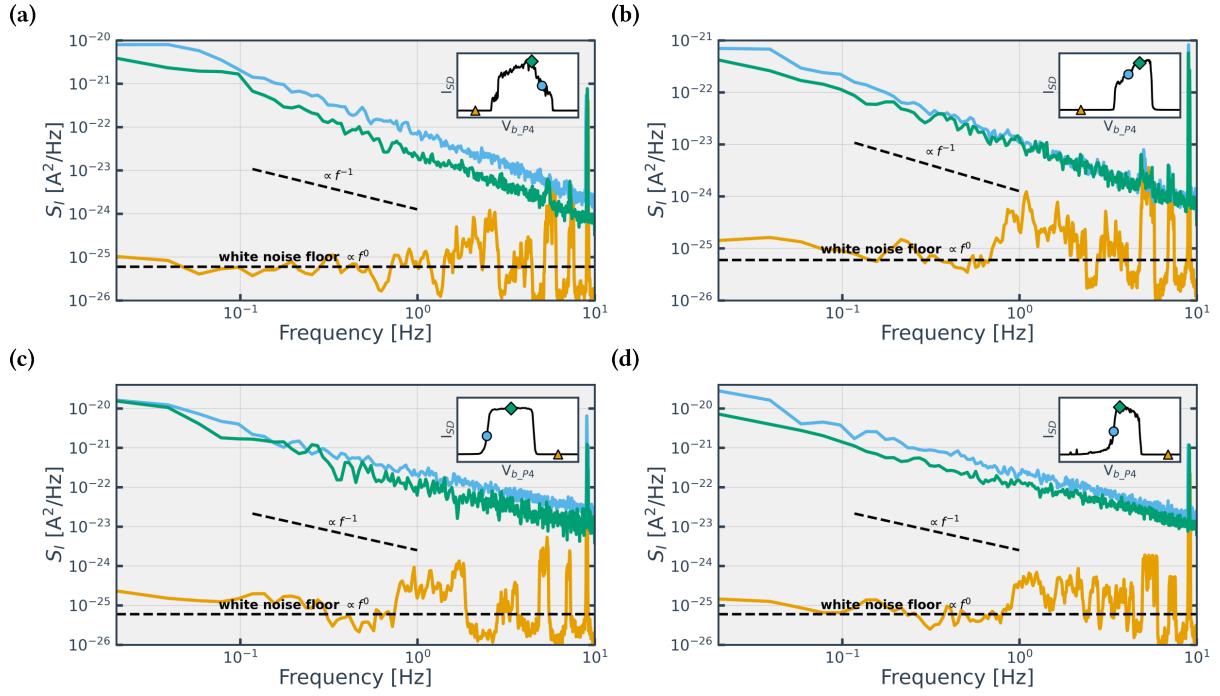


Figure 5.8: Current noise power spectral densities measured at gate **b_P4**. Panels (a) to (d) show data collected at different Coulomb peaks. Among all tested gates, b_P4 exhibits the lowest and most stable noise, especially in the frequency range below 10 Hz. This suggests reduced environmental coupling or a lower density of active charge traps. Insets indicate the corresponding measurement setup or sensor placement. Dashed lines proportional to $1/f$ are shown for reference.

Figure 5.9 summarizes the spatial configuration of the measured quantum dots and the extracted charge noise parameters for the four selected plunger gates. Panel (a) illustrates the device layout, with the positions of the plunger gates color-coded as follows: t_P1 (orange), t_P4 (blue), b_P1 (green), and b_P4 (pink). These gates define the quantum dots used for transport and noise measurements. Figure 5.9(b) compares the fitted noise exponents β extracted from the low-frequency behavior of the current noise spectra. All four gates yield β values near or above unity, consistent with dominant $1/f^\beta$ noise. Notably, b_P4 exhibits the narrowest spread and lowest mean, suggesting a highly stable noise environment. In addition, the extracted exponents tend to be larger for the quantum dots formed under the bottom channel gates (b_P1 and b_P4) compared to those under the top gates (t_P1 and t_P4). A larger value of β corresponds to a steeper frequency dependence, indicating that the noise decays more rapidly at low frequencies. This behavior may result from reduced contributions from slow fluctuators or improved electrostatic screening in the bottom channel. Figure 5.9(c) presents a comparison of current noise amplitudes at 1 Hz. Among the four configurations, t_P4 shows the largest variation and the highest outliers, whereas b_P4 demonstrates the lowest and most consistent noise amplitude across different Coulomb peaks. These findings reinforce the earlier conclusion that b_P4 represents the quietest and most stable operating point for charge-sensitive applications. Table 5.1 provides a summary of the extracted parameters for each

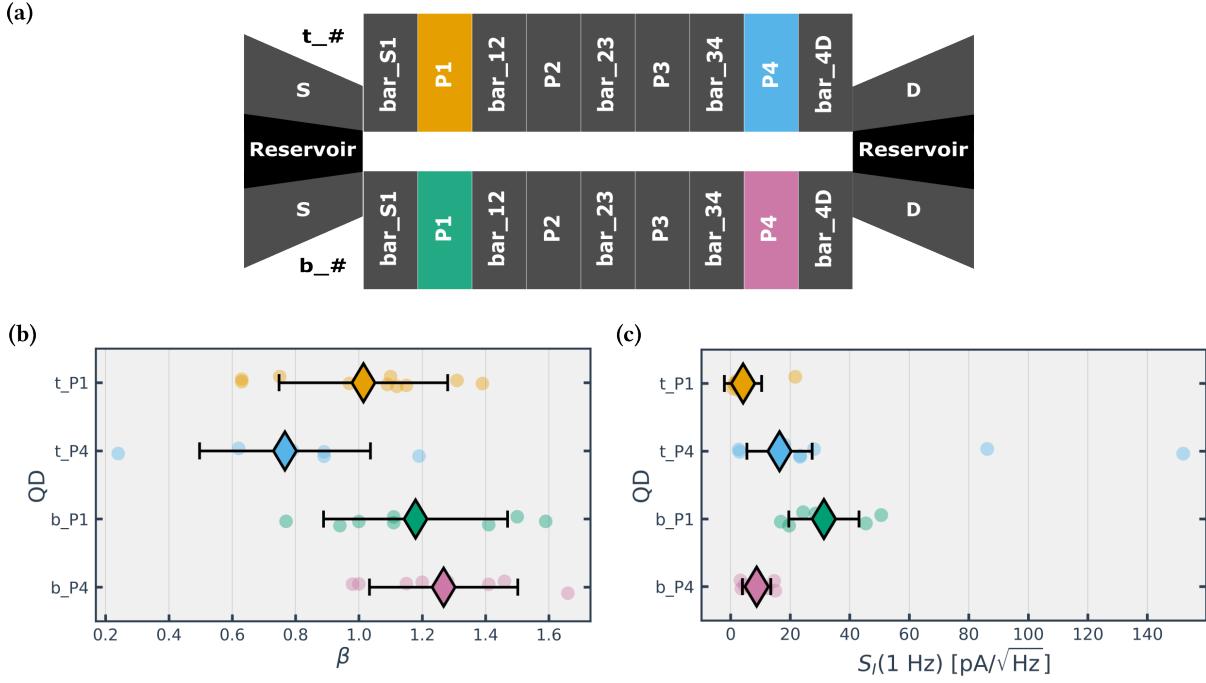


Figure 5.9: Summary of charge noise measurements. α is the lever arm, β is the exponent of the $1/f^\beta$ noise, and $S_I^{1/2}(1 \text{ Hz})$ is the current noise amplitude at 1 Hz. For gate t_P4, the reported value excludes two outlier points with noise above 80 pA/ $\sqrt{\text{Hz}}$, which were associated with transient switching events.

quantum dot, including the lever arm α , the noise exponent β , and the current noise amplitude at 1 Hz. For t_P4, the two outlier points with unusually high noise values were excluded from the reported average to avoid skewing the representation of typical device behavior.

Table 5.1: Summary of charge noise measurements. α is the lever arm, β is the exponent of the $1/f^\beta$ noise, and $S_I^{1/2}(1 \text{ Hz})$ is the noise level at 1 Hz.

| QD | α [eV/V] | β | $S_I^{1/2}(1 \text{ Hz})$ [pA/ $\sqrt{\text{Hz}}$] |
|------|-------------------|-------------------|---|
| t_P1 | 0.308 ± 0.009 | 1.014 ± 0.266 | 4.14 ± 6.26 |
| t_P4 | 0.370 ± 0.011 | 0.766 ± 0.270 | 16.41 ± 10.96 |
| b_P1 | 0.214 ± 0.007 | 1.179 ± 0.291 | 31.31 ± 11.80 |
| b_P4 | 0.179 ± 0.007 | 1.268 ± 0.234 | 8.69 ± 4.76 |

Overall, this analysis reveals clear spatial variability in the current noise behavior across the four plunger gates, reflecting differences in gate design, material uniformity, and local trap environments. All quantum dots exhibit low-frequency $1/f^\beta$ noise, with exponents β near or above unity, consistent with charge fluctuations from ensembles of two-level fluctuators. Notably, b_P4 consistently shows the lowest and most stable noise, both in spectral magnitude and shape, making it a strong candidate for future spin or charge qubit operation.

In principle, the current noise spectrum S_I can be converted to the charge noise spectrum S_ϵ

using the relation [66]:

$$S_\epsilon = \frac{\alpha^2 S_I}{|dI/dV_G|^2} \quad (5.2)$$

where α is the lever arm and dI/dV_G is the transconductance. However, due to temporal drift and peak shape instability, it was not possible to reliably extract this derivative, and thus S_ϵ is not computed in this study. This limitation means we are reporting current noise, S_I , rather than the intrinsic charge noise, S_ϵ . While S_I provides a valuable relative measure of noise across different gate configurations in the same device, it limits direct quantitative comparison to fundamental charge noise values (e.g., in $e/\sqrt{\text{Hz}}$ or $\mu\text{eV}/\sqrt{\text{Hz}}$) reported in the literature for other device platforms, where dI/dV_G could be reliably extracted. Nonetheless, the consistent methodology employed across all my measurements allows for robust relative comparisons within this study.

Nevertheless, the frequency-resolved S_I data alone offer valuable insight into the microscopic charge environment of the device. The observed $1/f^\beta$ noise characteristics and typical noise amplitudes are broadly consistent with previous results from similar SiMOS and Si/SiGe systems [55, 61, 66, 67, 68, 69]. For instance, the reported current noise levels for silicon quantum dots can vary widely depending on the device characteristics and measurement conditions, but typical values in the sub-10 Hz range often fall between $1 \text{ pA}/\sqrt{\text{Hz}}$ to $100 \text{ pA}/\sqrt{\text{Hz}}$. Studies investigating charge noise in Si/SiGe quantum dots, often conducted at base temperatures around 50 mK and exploring temperature dependence up to 1 K, have shown that charge noise generally increases with aluminum oxide gate dielectric thickness. [66, 61]. The measured values in this study, ranging from $4.14 \text{ pA}/\sqrt{\text{Hz}}$ ($t_{_P1}$) to $31.31 \text{ pA}/\sqrt{\text{Hz}}$ ($b_{_P1}$) at 1 Hz, are therefore consistent with previously reported noise levels for similar systems, which serves as a positive validation of the measurements.

The spatial variability in noise performance observed across the different gates is a key finding of this study. The fact that the bottom gates ($b_{_P1}$, $b_{_P4}$) tend to exhibit larger β exponents and that $b_{_P4}$ has the lowest overall noise amplitude compared to the top gates ($t_{_P1}$, $t_{_P4}$) suggests a significant influence of device geometry and material properties. This could be due to several factors:

1. **Oxide thickness and quality:** If the dielectric layer (oxide) under the bottom gates is inherently thicker or of higher quality (i.e., fewer defects and traps) than under the top gates, it would lead to reduced trap density and thus lower noise. Fabrication processes often lead to non-uniformities or different interface qualities depending on the gate layer, with thicker or better-annealed oxides typically exhibiting fewer charge traps [65, 70].
2. **Electrostatic screening:** The specific geometry of the bottom gates might provide better electrostatic screening from remote charge fluctuations in the substrate or overlying layers compared to the top gates, leading to a weaker coupling of external noise sources to the quantum dot.

3. Local material environment: The specific location and processing history for these individual gates might result in a locally cleaner or less strained semiconductor region, which would correlate with lower defect densities and thus lower noise.

While direct quantification of device characteristics like mobility was not performed in this study, the observed correlation between b_P4's consistently clear Coulomb diamonds and its superior noise performance reinforces the link between overall device "cleanliness" and both stable DC transport and low-frequency charge fluctuations. Previous studies have indeed linked high-quality material parameters, often reflected by high mobility, to reduced noise performance, as both ultimately depend on the density of impurities and defects in the semiconductor and dielectric layers [67]. These findings underscore the importance of optimizing fabrication processes and gate architecture for robust, low-noise quantum dot operation [70], especially in the context of scaling up for quantum computing applications.

Chapter 6

Conclusion

In this thesis, the investigation into charge noise in semiconductor QDs has advanced the understanding of this critical decoherence source, charge noise, particularly in silicon-based qubits. By combining theoretical foundations with meticulous experimental characterization, this work aimed to quantify charge noise behavior and analyze its implications for device performance, ultimately informing the development of more robust quantum computing platforms.

The experimental efforts, conducted on a two-dimensional linear Silicon-based QD array device from SemiQon, involved detailed transport measurements at both room and cryogenic temperatures. A significant achievement was the development and implementation of a Python-based automation framework, gate-manager. This tool proved invaluable for streamlining voltage control, data acquisition, and ultimately, extracting noise spectral densities from time-domain current measurements. Its modular design and validated performance offer a robust foundation for future, more extensive experimental campaigns.

A key experimental result was the consistent observation of $1/f^\beta$ -like noise across the characterized QDs, with exponents β generally found to be near or above unity (ranging from 0.766 to 1.268). This behavior is a hallmark of charge fluctuations arising from ensembles of TLFs, likely residing in the gate oxide or at the semiconductor-insulator interface. The measured current noise amplitudes at 1 Hz were typically in the range of a few to tens of $\text{pA}/\sqrt{\text{Hz}}$. For instance, t_P1 exhibited a noise amplitude of $4.14 \pm 6.26 \text{ pA}/\sqrt{\text{Hz}}$, while b_P1 showed the highest at $31.31 \pm 11.80 \text{ pA}/\sqrt{\text{Hz}}$. These values are broadly consistent with previously reported charge noise levels in similar SiMOS and Si/SiGe systems, validating my experimental methodology and findings within the broader literature.

A particularly insightful finding was the observed spatial variability in charge noise characteristics across different plunger gates. Notably, the quantum dot formed under gate b_P4 consistently exhibited the lowest and most stable current noise, coupled with the clearest and most well-defined Coulomb diamonds. This strong correlation suggests that the clarity of

Coulomb diamond features, while a static transport characteristic, can serve as a qualitative indicator of the underlying dynamic charge stability and reduced environmental noise in a QD. Furthermore, the bottom gates (b_P1, b_P4) generally displayed larger β exponents compared to the top gates (t_P1, t_P4). This steeper frequency dependence implies a potentially reduced contribution from slow fluctuators or enhanced electrostatic screening in the bottom channel, possibly due to variations in oxide thickness and quality, or more favorable local material environments resulting from fabrication processes.

The primary aims of quantifying charge noise behavior in silicon-based QDs and understanding its implications have been substantially met. I successfully characterized the frequency dependence and amplitude of current noise, identified spatial variations, and established a qualitative correlation between Coulomb diamond clarity and noise performance. The development of the automation framework was also a significant accomplishment, directly addressing the need for streamlined and repeatable measurements.

Despite these successes, the project encountered certain experimental challenges and limitations. The breakdown of a plunger gate under relatively low bias and higher-than-expected threshold voltages for some gates highlighted the inherent variability and fragility of current-generation silicon quantum dot devices. Such issues underscore the critical importance of rigorous device preparation, comprehensive leakage testing, and careful voltage ramping procedures, as emphasized during the experimental setup. Another limitation was the inability to reliably extract the transconductance derivative dI/dV_G due to temporal drift and peak shape instability in some measurements. This prevented the conversion of current noise S_I to the intrinsic charge noise spectrum S_ϵ , thus precluding direct quantitative comparison of the results with fundamental charge noise values reported for other device platforms. While S_I provided a valuable relative measure of noise within this study, obtaining S_ϵ remains a crucial step for a more universal characterization. While the project aimed for a comprehensive understanding of charge noise origins, the inability to directly convert to S_ϵ means that a full microscopic characterization in terms of fundamental charge fluctuations remains a direction for future work.

Building on these findings, future work should prioritize strategies to enable reliable extraction of dI/dV_G , possibly through faster sweep rates, real-time feedback mechanisms to stabilize peak positions, or advanced data analysis techniques that can compensate for drift. This would allow for the direct calculation of S_ϵ and facilitate quantitative comparisons with other qubit platforms. A more detailed temperature dependence study of charge noise would provide crucial insights into the underlying physical mechanisms, particularly distinguishing between thermal activation of traps and quantum tunneling phenomena [66, 71]. Implementing pulsed-gate spectroscopy or dynamically decoupled sequences could probe noise at different frequency regimes and offer more precise control over the qubit environment, potentially revealing contributions from specific TLFs that are averaged out in continuous measurements [67, 42]. Applying the developed analysis pipeline to devices with different oxide

interfaces, dopant profiles, or even entirely different material systems would provide invaluable comparative data for guiding future qubit fabrication processes. Finally, a more direct investigation into the correlation between field-effect mobility and charge noise performance would be beneficial, as high mobility is often linked to reduced defect densities [72].

Ultimately, the insights gained from this thesis underscore the complex interplay between device architecture, material quality, and the quantum coherence of semiconductor qubits. By persistently identifying and characterizing the sources and behavior of charge noise, we move closer to designing and fabricating more robust, coherent, and scalable qubit architectures essential for realizing fault-tolerant quantum computing.

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