# A Programmable Memory Built-In Self Test Circuit Based on 7-March-Algorithm for DICE SRAM

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***Abstract*—The technology of programmable memory built-in self-test (PMBIST) has been widely used in the testing of the static random-access memory (SRAM) because it can generate test vectors, automatically capture the responses on chip, and provide test results. A lot of research on the PMBIST for the SRAM is based on 6-T cell, but few is based on dual interlocked storage cell (DICE) that can resist Single Event Upset (SEU). In this paper, the spot defects in the 12-T DICE cell are analyzed with theoretical models and simulation results. The electrical behavior of spot defects are transformed and classified into fault models at the SRAM cell level. 7 widely-used March algorithms are selected to test DICE SRAM from both fault coverage and test time. A highly flexible and extensible architecture of the PMBIST is presented to meet the test requirement. The proposed 7-March PMBIST algorithm has been implemented as an IP core hanging on AXI bus by using FPGA to test the fabricated 1024×8-bit DICE SRAM chip using a 0.18-$\mu$m CMOS process. The result shows that it can precisely detect the spot defects under the operating frequency of 100 MHz and chip area overhead is 81445.24 $\mu$m$^2$.**

***Index Terms*—PMBIST, Spot Defects, March algorithms, DICE, Fault Models**

## I. Introduction

THE static random-access memory (SRAM) is one of the most important IP cores in SoC owing to its large storage capacity and high access speed. Each cell of SRAM must be fully tested to ensure correct memory function. There are basically two types of memory defects in SRAM memory chips, i.e. global defects and local defects. The local defects affect only a small area of the integrated circuits, these defects have been called spot defects (SDs) and are the primary testing target in SRAM memory chips [8].

The memory built-in self-test (MBIST) is one effective method for testing chip-embedded memory. Various MBIST testing algorithms have been studied, including ad-hoc algorithm, walking 1/0 algorithm, checkboard algorithm, March algorithm etc., which is shown in [1], [2]. March algorithm is the most popular because of its high fault coverage and short testing time [3]. However, the traditional MBIST that can only generate a fixed test algorithm once the design is completed has low flexibility and may not meet the test requirement of different memories on the chip. Thus, many Programmable MBIST architectures are developed in [4]-[7]. The PMBIST can generate various March algorithms to meet test requirements of different memories. In addition, the PMBIST avoids re-implementing new test algorithms that need the support of different requirements during the life cycle of a memory device fabrication. Besides, numerous studies of SDs and fault models of SRAM have been made on the basis of the 6-T structure, but few focus on the dual interlocked storage cell (DICE) SRAM which is composed of 12 transistors and has a good anti-radiation performance [8]- [11].

The SDs in the 12-T DICE SRAM cells have been analyzed and classified in this paper. For different kinds of defects, corresponding algorithms are proposed to detect them. Considering both fault coverage and time efficiency, a flexible and extensible Finite State Machine (FSM) based PMBIST architecture is proposed that can generate various March algorithms to meet test requirements of a DICE SRAM. In this design, only one FSM is required, rather than using the nesting state machine method in [5].

This paper is organized as follows: Section II provides a briefly introduction of the traditional 6-T SRAM SDs and tests. Section III analyzes the SDs and fault models in the 12-T DICE cell. Section IV proposed the PMBIST architecture for 7-march-algorithm and the test result of the tape-out DICE SRAM is presented in Section V. Section VI ends with summary.

## II. Spot Defects and tests in the Traditional 6-T SRAM

The traditional 6-T SRAM circuit consists of a latch and a pair of switches, as shown in Fig.1. The research on BIST for 6-T SRAM is usually carried out for SDs. The defects can be classified by inserting an equivalent resistance $R \in (0,\infty)$ between key nodes, including open defect D1, short defect D2 and bridge defect D3, where the defect D could be defined as Eq.1 [8].

$$\mathrm{D} = \begin{cases} \mathrm{D}_1(\text{Two nodes in one cell}) \\ \mathrm{D}_2(\text{Node and power or ground in one cell}) \\ \mathrm{D}_3(\text{Two nodes in one and nearby cell}) \end{cases} \quad (1)$$

Basically, all the models of the SDs can be obtained through simulation by constructing a circuit according to Eq.1. Introduced in [12], several terms are defined as follows, when considering the symmetrical structure of the SRAM cell. First, complementary behavior: the location of SD1 and SD2 is symmetrical in the circuit, and the fault behavior they cause

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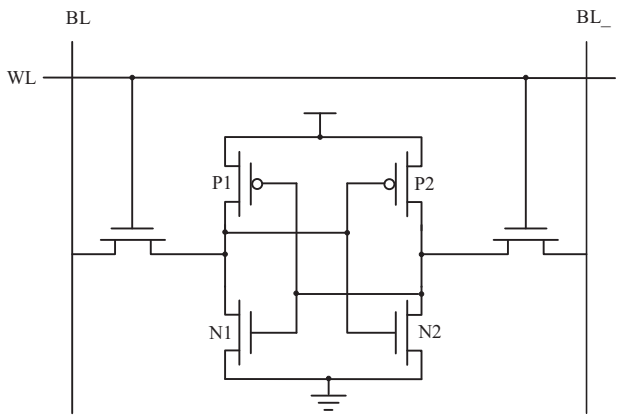



Fig. 1. Transistor-level schematics of the traditional 6-T SRAM cell.

shows complementary, noted as Comp.b.. Second, interchange behavior: the location of aggressor cell (SD1) and victim cell (SD2) is symmetrical and the aggressor or the victim cell are interchanged, noted as Inter.b.. Third, interchanged complementary behavior: it is the combination of Comp.b. and Inter.b., noted as I.C.b..

Considering the tradeoff between testing coverage and time, usually one or several March algorithms with the characteristics of high fault coverage and relatively short testing time are fixed on chip for SRAM testing, which makes the flexibility of MBIST architecture fail to meet different testing requirements of different SRAM configuration and different development periods [13]. The sequence length and fault coverage of the common March algorithm are summarized in Table I.

TABLE I
FAULT COVERAGE OF MARCH ALGORITHM

| Algorithm name | Sequence lengh | Fault coverage |
|---|---|---|
| MATS+ | 5n | SAF TF- RDF IRF CFst- CFds- CFtr- CFrd- Cfir- |
| March X | 6n | SAF TF RDF IRF CFst- CFds- CFtr- CFrd- Cfir- |
| March C- | 10n | SAF TF RDF IRF CFst CFds- CFtr CFrd Cfir |
| March B | 17n | SAF TF RDF IRF CFst- CFds- CFtr- CFrd- Cfir- |
| March U | 13n | SAF TF RDF IRF CFst CFds- CFtr CFrd Cfir |
| March LR | 14n | SAF TF RDF IRF CFst CFds CFtr CFrd Cfir |
| March SS | 22n | SAF TF RDF DRDF IRF CFst CFds CFtr CFrd Cfir |

## III. SPOT DEFECTS AND FUNCTIONAL MODELS IN 12-T DICE CELL

### A. Classification of Spot Defects

In the radiation environment, high-energy particles incident into the sensitive area of semiconductor devices, then an incorrect logic level will be generated will be latched by the circuit to cause the wrong logic function, which is Single Event Upset (SEU). In general, the value of Linear Energy Transfer (LET) is used to indicate the resistance of the device to SEU, as shown in Eq.2, where $\rho$ is the density of silicon, and $dE/dx$ is the power loss rate. The structure of DICE SRAM cell is relatively fixed and has no special requirements on the size of the transistor, moreover it can avoid the problem of high-energy particles incident on the sensitive region of the device. Therefore, the DICE structure can be used to design SRAM memory cells to increase their anti-radiation characteristics [14].

$$LET = \frac{1}{\rho} \times \frac{dE}{dx} \tag{2}$$

The circuit of memory cell with 12-T DICE structure, as shown in Fig.2, it adopts a four-node redundant structure, a single transistor realizes inverter logic, and a feedback loop is constructed to realize the latch function. Specifically, it consists of two pairs of horizontal and vertical latches (P2-N1, P4-N3; P1-N4, P3-N2) to realize the storage of two sets of complementary logic values (Q1_, Q1, Q2_, Q2). If the values of nodes (Q1_, Q1, Q2_, Q2) are '1010', it means that the logical value stored in this cell is '1', then '0101' means the logical value stored in this cell is '0'. The value of each node is controlled by two adjacent nodes, like Q1_ is controlled by Q1 and Q2. If the values of Q1_, Q1, Q2_, Q2 are '0101', the value of Q1 is flipped due to the SEU, from '1' to '0', the transistor of P3 will turn on, then the value of Q2_ will changed from '0' to '1' and Q2 is not affected due to the truncation of P4, the value of Q1_ will not change too, then the cell returns to its original state. The double Inter-Lock structure that has a much stronger ability to resist SEU than the traditional 6-T dice.

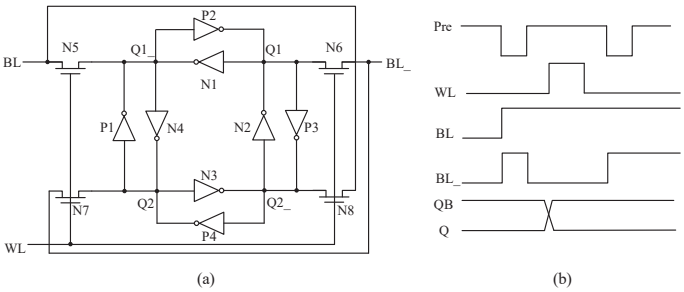



Fig. 2. The 12-T DICE SRAM cell with (a) the logic structure schematic and (b) the timing diagram of logic state transitions.

Compared to the traditional 6-T SRAM structure, the 12-T DICE cell has more nodes and the models of SDs are more complex. In order to further reduce the number of simulations, four new terms are proposed in this paper in addition to the 6-T SRAM terms which already introduced in Section II. First, similar behavior: equivalent connection failure at nodes Q1/Q1_ and Q2/Q2_, noted as Sim.b.. Second, similar complementary behavior: the combination of Comp.b. and Sim.b., noted as S.C.b.. The functional fault behavior of SD1/SD1c (or SD2/SD2c) are complementary and SD1 and SD2 are equivalent connection in the cell. Third, interchanged similar behavior: the combination of Inter.b. and Sim.b., noted as I.S.b.. The victim cell and aggressor cell in the fault behavior of SD1 and SD2 are interchanged. Fourth, interchanged similar complementary behavior: the combination of Comp.b., Inter.b. and Comp.b., is noted as I.S.C.b..

According to the behavior description, SDs can be further classified. First, the open-type SDs can be divided into three categories, i.e. open within a cell (OCs), open at word lines (OWs) and open at bit lines (OBs). The OCs could be seen

in Fig.3, OCn and OCns are similar behavior, OCn and OCnc are complementary fault behavior. There is just only one fault behavior should be considered and other opens can be derived due to the similar or complementary behavior, The details of the OCs have been listed in Table II.

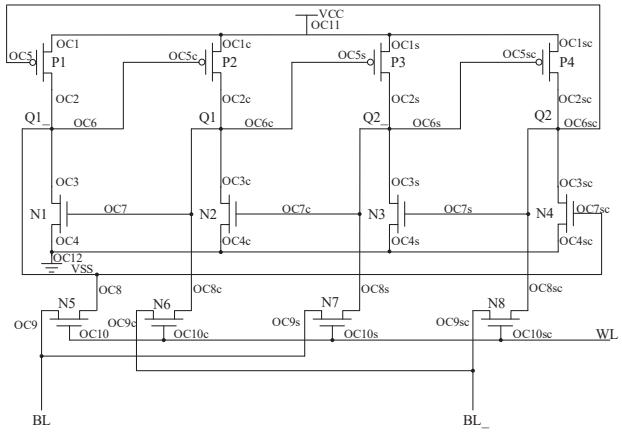



Fig. 3. The opens within a DICE SRAM cell.

TABLE II
OPENS WITHIN ONE CELL

| Classification | Description |
|---|---|
| OC1/OC2 | Drain or source of pull up PMOS is broken |
| OC3/OC4 | Drain or source of pull down NMOS is broken |
| OC5 | Gate of pull up PMOS is broken |
| OC6 | Cross coupling PMOS is broken |
| OC7 | Gate of pull down NMOS is broken |
| OC8 | Pass MOS connection to true node is broken |
| OC9 | Pass MOS connection to bit line is broken |
| OC10 | Gate of pass MOS is broken |
| OC11/OC12 | VCC or VSS connection to cell is broken |
| OB | Bit line is broken |
| OW | Word line is broken |

There are about 14 short defects within a cell, similar to the opens, the defects of short can be classified into 3 classes, shorts within a cell (SC), shorts at bit lines (SB) and shorts at word lines (SW). The short at Q1 has a complementary behavior to the short of Q1_, noted as Comp.b., while the shorts of Q1 and Q2 has a similar behavior noted as Sim.b., then the combination of similar and complementary behavior is noted S.C.b., as shown in Table III.

Finally, the bridge-type defects can be divided into two categories of bridges within one cell (BCs) and bridges between two cells (BCCs) as shown in Fig.4. For the BCs, a node can be connected to all other nodes in the same cell, considering the fact that each cell consists of 7 nodes, there are $C_7^2 = 21$ possible bridges that can be classified into 8 classes listed in Table IV. The complementary behavior (Comp.b.), similar behavior (Sim.b.) and the combination of similar and complementary behavior (S.C.b.) are also displayed in Table IV.

TABLE III
SHORT DEFECTS WITHIN ONE CELL

| Classification | Short | Comp.b | Sim.b | S.C.b |
|---|---|---|---|---|
| SC1 | Q1-VCC | Q1_-VCC | Q2-VCC | Q2_-VCC |
| SC2 | Q1-VSS | Q1_-VSS | Q2-VSS | Q2_-VSS |
| SB1 | BL-VCC | BL_-VCC | | |
| SB2 | BL-VSS | BL_-VSS | | |
| SW1 | WL-VCC | | | |
| SW2 | WL-VSS | | | |

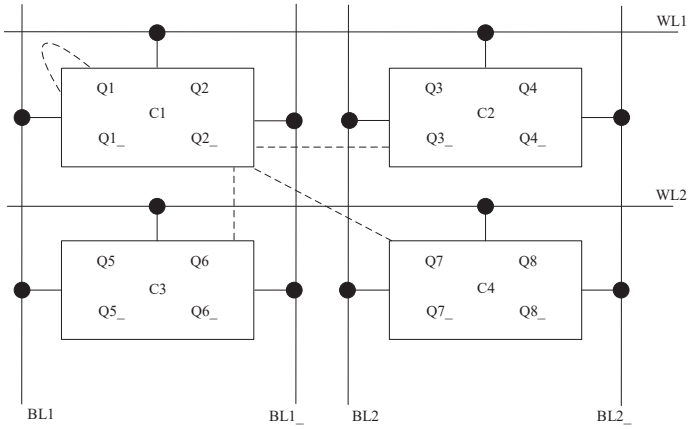



Fig. 4. The bridges in a 2x2 cells array.

The BCCs can be divided into three groups: bridges in the same row (rBCCs), bridges in the same column (cBCCs) and bridges between diagonal cells (dBCCs). Furthermore, these three types of defects can be classified further. Each cell of them is composed of 7 nodes, since the cells C1 and C2 are in the same row so they share the same word line (WL1), then the rBCCs defects include 36 possible bridges that can be classified into 8 classes. Similarly, there are 25 possible bridges classified into 6 classes for cBCCs, due to the cells in the same column have common bit lines, (i.e., both cell C1 and C3 are connected to BL1 and BL1_). For the diagonal cells, each cell has 4 bridges to the diagonal cell, so there are 16 possible bridges and the bridges can be classified into 6 classes for dBCCs. All bridge defects between two cells can be seen in Table V.

TABLE IV
BRIDGES WITHIN ONE CELL

| Classification | Bridge | Comp.b | Sim.b | S.C.b |
|---|---|---|---|---|
| BC1 | Q1-Q1_ | | Q2-Q2_ | |
| BC2 | Q1-Q2 | Q1_-Q2_ | | |
| BC3 | Q1-Q2_ | Q1_-Q2 | | |
| BC4 | Q1-BL | Q1_-BL_ | Q2-BL | Q2_-BL_ |
| BC5 | Q1-BL_ | Q1_-BL | Q2-BL_ | Q2_-BL |
| BC6 | Q1-WL | Q1_-WL | Q2-WL | Q2_-WL |
| BC7 | BL-BL_ | | | |
| BC8 | BL-WL | BL_-WL | | |

TABLE V
BRIDGES BETWEEN TWO CELLS

| Classification | Bridge behavior | Comp.b. | Inter.b. | Sim.b. | I.C.b. | S.C.b. | I.S.b. | I.S.C.b. |
|---|---|---|---|---|---|---|---|---|
| Bridges in the same row (rBCCs) | Q1-Q3<br>Q1-Q3_<br>Q1-Q4<br>Q1-Q4_<br>Q1-BL2<br>Q1-BL2_<br>BL1-BL2<br>BL1-BL2_ | Q1_-Q3_<br>Q1_-Q3<br>Q1_-Q4_<br>Q1_-Q4<br>Q1_-BL2_<br>Q1_-BL2<br>BL1_-BL2_ | Q3-BL1<br>Q2-BL2_<br>BL1_-BL2 | Q2-Q4<br>Q2-Q4_<br>Q2-Q3<br>Q2-Q3_<br>Q2-BL2<br>Q2-BL2_ | Q3_-BL1_<br>Q3_-BL1 | Q4-BL1<br>Q4_-BL1_ | Q2_-Q4_<br>Q2_-Q4<br>Q1_-Q2_<br>Q1-Q2_<br>Q2_-BL2_<br>Q2_-BL2 | Q4_-BL1_<br>Q4_-BL1 |
| Bridges in the same column (cBCCs) | Q1-Q5<br>Q1-Q5_<br>Q1-Q6<br>Q1-Q6_<br>Q1-WL2<br>WL1-WL2 | Q1_-Q5_<br>Q1_-Q5<br>Q1_-Q6_<br>Q1_-Q6<br>Q1_-WL2 | WL1-Q6 | Q2-Q6<br>Q2-Q6_<br>Q2-Q5<br>Q2-Q5_<br>Q2-WL2 | WL1-Q6_ | WL1-Q5 | Q2_-Q6_<br>Q2_-Q6<br>Q2_-Q5_<br>Q2_-Q5<br>Q2_-WL2 | WL1-Q5_ |
| Bridges between diagonal cell (dBCCs) | Q1-Q7<br>Q1-Q7_<br>Q1-Q8<br>Q1-Q8_ | Q1_-Q7_<br>Q1_-Q7<br>Q1_-Q8_<br>Q1_-Q8 | | Q2-Q8<br>Q2-Q8_<br>Q2-Q7<br>Q2-Q7_ | | Q2_-Q8_<br>Q2_-Q8<br>Q2_-Q7_<br>Q2_-Q7 | | |

### *B. Functional Fault Models and Simulation Result*

There are a lot of SDs in the 12-T DICE SRAM cell and these SDs are complicated due to the cell has more circuit nodes such as Q2 and Q2_. The SDs of opens, shorts and bridges can be transformed into functional fault models and the it can be described by fault primitives [15]. These functional fault models are: stuck-at faults (SAFs), transition faults (TFs) and coupling faults (CFs).

The SAFs is one of the most common fault models, in this fault model, the logic value of the storage node Qn/Qn_ is always "0" or "1". The value stored in the cell remains unchanged no matter read or write ("0" or "1") operation. This kind of fault model may occurred in the open, short and bridge defects (i.e. OC6, SC1/SC2 and BC4). The detection method of SAF is <w0,r0,w1,r1> to all the cells to be tested. The "w" and "r" here stand for the write and read operations, and "0" or "1" are the logic values.

The TFs is that the logic value of the storage node Qn/Qn_ cannot be converted from "0" to "1" (or from "1" or "0") during a write operation. This kind of fault model may occurred in the open and short defects (i.e. OC8, OC9, SB1 and SB2). This fault model can be detected by <w0,w1,r1,w0,r0> operation.

The CFs is that writing to one cell will affect the value of other cells. When the A-cell is written, the value of B-cell is converted or kept at a specific value. This kind of fault model may occurred in the open, short and bridge defects (i.e. SW1, OC10, BC2, and r/c/dBCCs). This fault model can be detected by <↑w0,↑r0,↓w1,↓r1> operation. The "↑" and "↓" here represent the read/write operations in up or down address order.

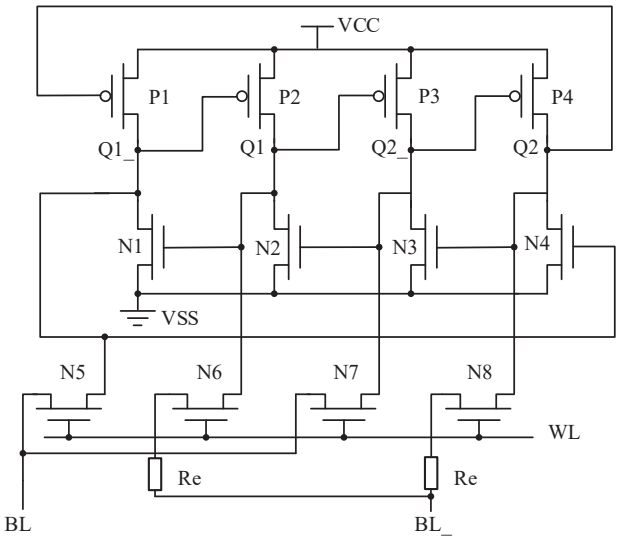



Fig. 5. Transistor-level schematics of the defect OC9x with the equivalent resistance Re.

Take OC9x defect as an example, it belongs to TFs. The equivalent resistance Re is introduced between the transmission gates (N6 and N8) and node BL_, then the point defect of OC9x could be happened between the drain of N6 and N8, as shown in Fig. 5. The OC9x could cause a failure when writing "0" to the node of Q1 which is in the state of "1" because the existence of Re limits the dropping voltage of Q1 during

conversion. Under extreme conditions, it cannot drop below the threshold voltage $V_{thn}$ of N1, and this fails the operation. In a normal mode of operation, the initial states of Q1 and Q1_ are "1" and "0" respectively. After the WL has been set to "1", the transistors of N5 and N6 are turned on, and the states of Q1 and Q1_ become "0" and "1" respectively. However, if OC9x exists, $V_{Q1}$ could be affected by Re in the falling and cannot reach to "0". As the initial voltage of $V_{Q1\_}$ is 0 V in this case, the transistor of P2 can be turn on, and its on-current follows the typical second-order equation in saturation region.

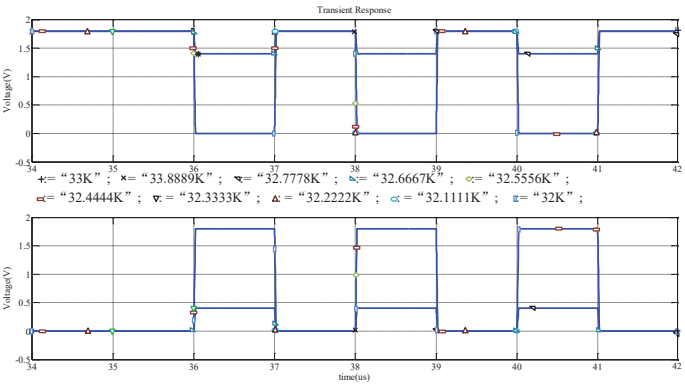



Fig. 6. The simulation result of OC9x with different resistance values.

$$\frac{1}{2}\mu_p C_{ox}(V_{DD} - V_{thp})^2 \times R_e \geq V_{thn} \quad (3)$$

When the equivalent resistance exists and the Eq. 3 is satisfied, the transistor N2 cannot be turned off smoothly during the conversion, so P2 is always in the on-state, resulting in the failure of writing "0" to Q1 node. As the simulation result of OC9x shown in Fig. 6, the resistance value only influences the simulation result when the value is greater than 10 kΩ.

## IV. Proposed PMBIST Based on 7-March-Algorithm for DICE SRAM

At present, the March algorithm is the most widely used test algorithm because of it is linear, symmetrical and efficient. Considering the time and reliability of the test, the proposed PMBIST architecture is based on March SS and March LR algorithms and it can cover all the algorithms in Table I. The circuits of proposed PMBIST consists of 6 modules: PMBIST controller, address generator, data generator, control generator, compare circuit and mux, as shown in Fig.7. The PMBIST controller is a Moore-type FSM which produces configuration information to the rest of three generators.

At first, a corresponding value of alg_sel is provided for each March algorithm, as shown in Table VI, in which March elements are shown in Table VII. If the value of alg_sel is set to "100", then the March B algorithm will work. The state transition diagram of the March B algorithm is shown in Fig.8. The overflow signal coming from address generator indicates the complete of one March element and the start of another March element. The value of signal mbist_done_o becomes "1" when the whole algorithms has been done.

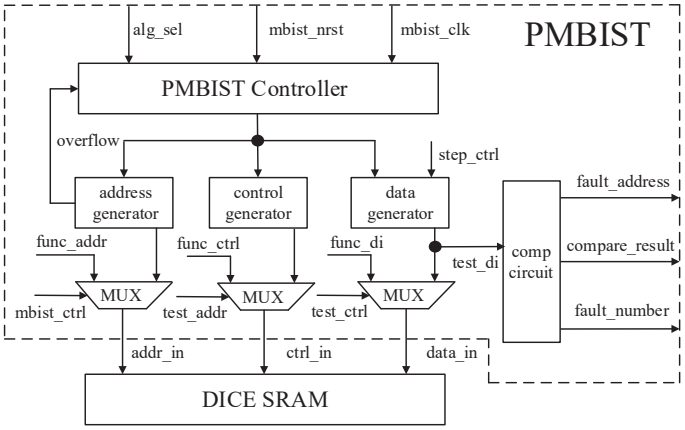



Fig. 7. Architecture of the proposed PMBIST topology

TABLE VI
MICROCODE OF MARCH ALGORITHMS.

| alg_sel | Algorithm | March Element |
|---|---|---|
| 001 | MATS+ | M1 M2 M3 |
| 010 | March X | M1 M2 M3 M4 |
| 011 | March C- | M1 M2 M3 M4 M5 M6 |
| 100 | March B | M1 M7 M8 M9 M10 |
| 101 | March U | M1 M2 M3 M11 M12 |
| 110 | March LR | M1 M4 M5 M6 M11 M13 |
| 111 | March SS | M1 M4 M14 M15 M16 M17 |

TABLE VII
STATE CODE AND MARCH ELEMENTS

| State Code | March Element | State Code | March Element |
|---|---|---|---|
| M1(00000) | ↑w0 | M10(01001) | ↓r0, w1, w0 |
| M2(00001) | ↑r0, w1 | M11(01010) | ↑r0, w1, r1, w0 |
| M3(00010) | ↓r1, w0 | M12(01011) | ↓r1, w0, r0, w1 |
| M4(00011) | ↑r0 | M13(01100) | ↑r1, w0, r0, w1 |
| M5(00100) | ↑r1, w0 | M14(01101) | ↑r0, r0, w0, r0, w1 |
| M6(00101) | ↓r0, w1 | M15(01110) | ↑r1, r1, w1, r1, w0 |
| M7(00110) | ↑r0, w1, r1, w0, r0, w1 | M16(01111) | ↓r0, r0, w0, r0, w1 |
| M8(00111) | ↑r1, w0, w1 | M17(10000) | ↓r1, r1, w1, r1, w0 |
| M9(01000) | ↓r1, w0, w1, w0 | | |

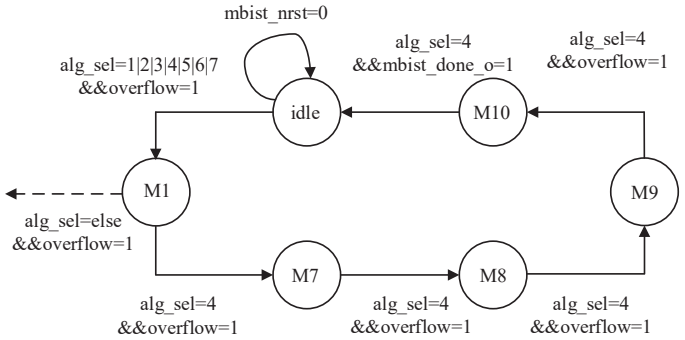
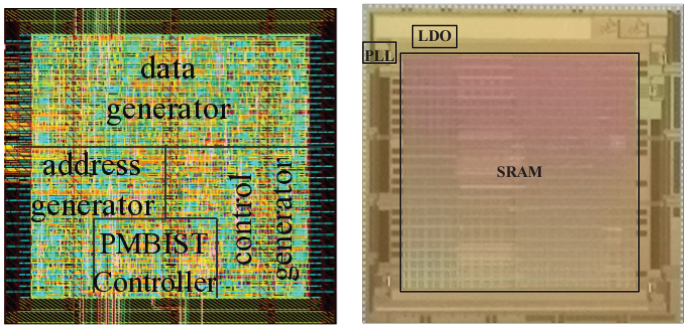



Fig. 8. The logical state transition diagram of March B.



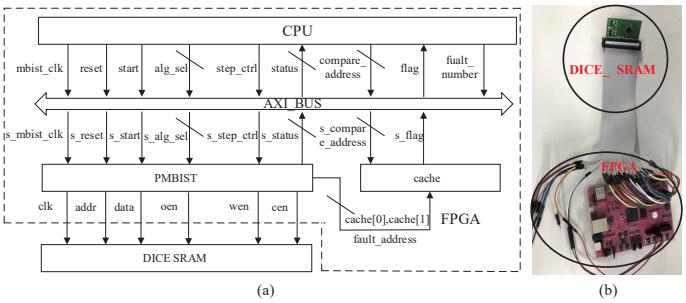

(a) (b)

Fig. 9. Layout of the proposed PMBIST cell (a) and the microphotograph of the fabricated 12-T DICE SRAM chip (b).

Then, the rest three generators start to generate test signals into the DICE SRAM, including data, address and control signals. The compare_result signal turns high when some faults are detected. The related signals of fault_address and fault_number which indicate the address and the number of faults can be displayed after the compare circuit. The layout of the proposed PMBIST is implemented by SMIC 0.18 $\mu$m process, its area overhead is 81445.24 $\mu m^2$ as shown in Fig. 9 (a) and Fig. 9(b) is a microphotograph of the 12-T DICE SRAM chip.

## V. Experimental Results with DICE SRAM Chip

The circuits of proposed PMBIST is implemented hanging on the AXI bus as an IP core with a FPGA chip to test the fabricated $1024 \times 8$ bits of DICE SRAM, as shown in Fig.10. The maximum number of fault addresses is 39 detected by the test system as shown in Fig.11.




(a) (b)

Fig. 10. Architecture of the proposed test system topology (a) and the test setup of the proposed design using FPGA (b).

The performance summary and comparison with prior arts is shown in Table VIII. Compared to all of the prior arts, only this PMBIST circuits is designed for DICE SRAM. Compared to [16] and [17], the architecture of these PMBIST circuits is programmable and can achieve a higher test coverage by using seven March algorithms. Compared to [18], the FSM is chosen as the architecture of PMBIST to reduce the cost of power consumption and area, though the FSM has been chosen in [19] and [20], but they can only be used for 6-T SRAM test.

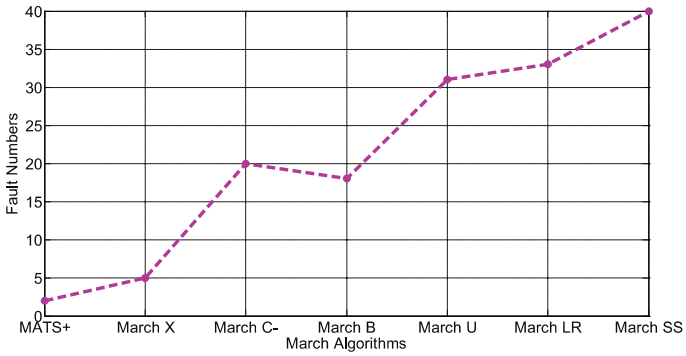



Fig. 11. The test result of the proposed PMBIST with 7-March-Algorithm for DICE SRAM.

TABLE VIII
Performance Summary and Comparison with Prior Art

| MBIST for SRAM | | | | | | |
|---|---|---|---|---|---|---|
| Reference | [16] | [17] | [18] | [19] | [20] | This work |
| SRAM Type | 6-T SRAM | 6-T SRAM | 6-T SRAM | 6-T SRAM | 6-T SRAM | 12-T DICE SRAM |
| Test algorithm | March C-, MATS | March Q, March C- | March | MATS+, March X, March C-, March A, March B, March U, March LR, March SS | MATS+ March C- | MATS+, March X, March C-, March B, March U, March LR, March SS |
| Realization | On-chip | On-chip | On-chip | FPGA | On-chip | FPGA and On-chip |
| CMOS process | 65(nm) | 100(nm) | 130(nm) | - | 90(nm) | 180(nm) |
| Programmable architecture | No support | No support | Instruction | FSM | FSM | FSM |
| Max frequency | 200(MHz) | - | - | 195.01(MHz) | - | 100(MHz) |
| Area($\mu m^2$) | - | 25184 | - | - | - | 81445 |

## VI. Conclusion

The 12-T DICE cell has more possible spot defects than 6-T cell owing to its more circuit nodes but it still contains the old fault models as 6-T cell. A highly flexible and extensible PMBIST architecture is proposed, which can generate seven types of March algorithms to test DICE SRAM. In addition, the proposed PMBIST can be extended to generate arbitrary March algorithm because there are enough test elements. The compare circuit can report fault address and compare result which can facilitate diagnostics in SRAM. The proposed PMBIST is also implemented on FPGA to test the tape-out DICE SRAM, showing the proposed PMBIST can detect faults precisely.

## References

[1] A. K. S. Pundir, "Novel modified memory built in self-repair (MMBISR) for SRAM using hybrid redundancy-analysis technique," *IET Circuits, Devices and Systems*, vol. 13, no. 6, pp. 836-842, Sept, 2019.

[2] N. Q. M. Noor, Y. Yusof and A. Saparon, "Low area FSM-based memory BIST for synchronous SRAM," in *5th International Colloquium on Signal Processing & Its Applications,*Kuala Lumpur, Malaysia 2009, pp. 409–412.

[3] C.-C. Wang, C.-F. Wu, R.-T. Hwang and C.-H. Kao, "Single-ended SRAM with high test coverage and short test time," *IEEE Journal of Solid-State Circuits,*, vol. 35, no. 1, pp. 114-118, Jan, 2000.

[4] G. Theodorou, N. Kranitis, A. Paschalis and D. Gizopoulos, "Software-based self-test for small caches in microprocessors," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,*, vol. 33, no. 12, pp. 1991-2004, Jan, 2014.

[5] P.-C. Tsai, S.-J. Wang and F.-M. Chang, "FSM-based programmable memory BIST with macro command," in *2005 IEEE International Workshop on Memory Technology, Design, and Testing,*Taipei, Taiwan 2005, pp. 72–77.

[6] K. Zarrineh, and S. J. Upadhyaya, "On programmable memory built-in self test architectures," in *Design, Automation and Test in Europe Conference and Exhibition,*Munich, Germany, Germany 1999, pp. 708–713.

[7] N. Q. M. Noor, A. Saparon and Y. Yusof, "An overview of microcode-based and FSM-based programmable memory built-in self test (MBIST) controller for coupling fault detection," in *IEEE Symposium on Industrial Electronics & Applications,*Kuala Lumpur, Malaysia 2009, pp. 469–472.

[8] W. Pei, W. Jone and Y. Hu, "Fault modeling and detection for drowsy SRAM caches," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,*, vol. 26, no. 6, pp. 1084-1100, June, 2014.

[9] C. Lin, H. Chen, H. Yang, C. Huang, M. C. -. Chao and R. Huang, "Fault models and test methods for subthreshold SRAMs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems,*, vol. 62, no. 3, pp. 468-481, May, 2013.

[10] C. Hu, J. F. Chen, S. Chen, S. Chang, K. Lee and C. Lee, "Improvement of poly-pimple-induced device mismatch on 6T-SRAM at 65-nm CMOS technology," *IEEE Transactions on Electron Devices,*, vol. 57, no. 4, pp. 956-959, April, 2010.

[11] J. Kinseher, M. Voelker and I. Polian, "Improving testability and reliability of advanced SRAM architectures," *IEEE Transactions on Emerging Topics in Computing,*, vol. 7, no. 3, pp. 456-467, July, 2019.

[12] S. Hamdioui, G. Gaydadjiev and A. J. van de Goor, "The state-of-art and future trends in testing embedded memories," in *Records of the 2004 International Workshop on Memory Technology,*San Jose, CA, USA, 2004, pp. 54–59.

[13] S. Hamdioui, A. J. van de Goor and M. Rodgers, "March SS: a test for all static simple RAM faults," in *Proceedings of the 2002 IEEE International Workshop on Memory Technology, Design and Testing,*Isle of Bendor, France 2002, pp. 95–100.

[14] Ahmed S. Sajit and Michael A. Turi, "SEU tolerance of FinFET 6T SRAM, 8T SRAM and DICE memory cells," in *IEEE 7th Annual Computing and Communication Workshop and Conference,*Las Vegas, NV, USA 2017.

[15] S. Hamdioui and A. J. Van De Goor, "An experimental analysis of spot defects in SRAMs: realistic fault models and tests," in *Proceedings of the Ninth Asian Test Symposium,*Taipei, Taiwan 2000, pp. 131–138.

[16] E. Nelson, J. Dreibelbis and R. McConnell, "Test and repair of large embedded DRAMs. I," in *Proceedings International Test Conference 2001,*Baltimore, MD, USA 2001, pp. 173–181.

[17] A. K. S. Pundir, "Efficient testing of SRAM with optimized march sequences and a novel DFT technique for emerging failures due to process variations," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,*, vol. 13, no. 11, pp. 1286-1295, Nov, 2005.

[18] S. Boutobza, M. Nicolaidis, K. M. Lamara and A. Costa, "A transparent based programmable memory BIST," in *Eleventh IEEE European Test Symposium,*Southampton, UK 2006, pp. 89–96.

[19] N. Q. M. Noor, A. Saparon, Y. Yusof and M. Adnan, "New Microcode's generation technique for programmable memory built-in self test," in *19th IEEE Asian Test Symposium,*Shanghai, China 2010, pp. 407–412.

[20] Kun-Lun Luo, Ming-Hsueh Wu, Chun-Lung Hsu and Chen-An Chen, "Built-In Self-Test Design for the 3D-Stacked Wide-I/O DRAM," *Journal of Electronic Testing,*, vol. 32, no. 2, pp. 111-123, Feb, 2016.