实验报告一
PB14000556 陈晓彤

实验题目：运算器 ALU 设计

实验要求：

设计一算数运算单元 ALU

- 采用纯组合逻辑设计
- 32bit 位宽
- 完成指定运算功能
- 自行设计测试例对所设计的 ALU 进行仿真

设计思路：

采用 always 和 case 语句可直接完成题目要求，同时设置一个一位变量检测溢出情况即可

源代码:

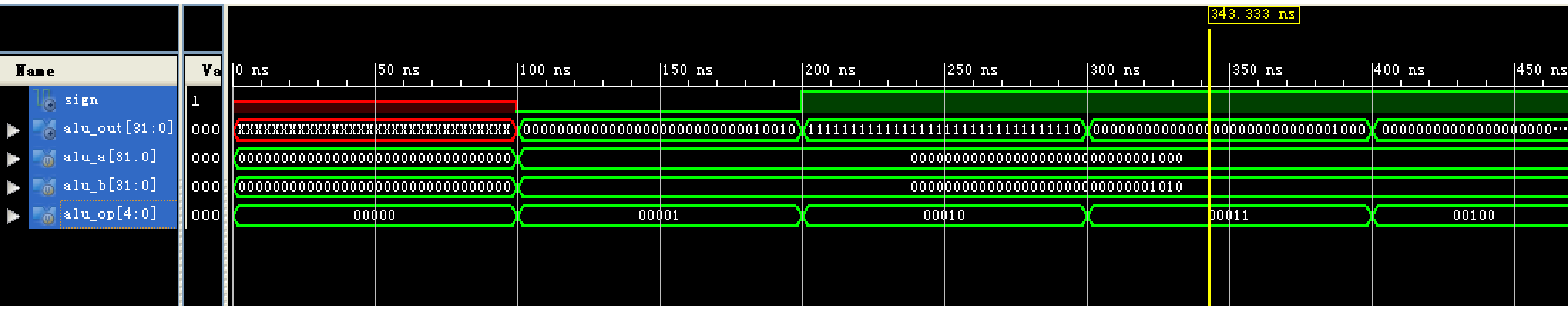
```
module ALU(
   input    signed        [31:0] alu_a,
   input    signed        [31:0] alu_b,
   input                  [4:0]   alu_op,
   output reg                                  sign,
   output    reg               [31:0]     alu_out
);
      parameter     A_NOP = 5'h00; //空运算
      parameter     A_ADD   = 5'h01;  //符号加
      parameter     A_SUB    = 5'h02;  //符号减
      parameter     A_AND = 5'h03;    //与
      parameter     A_OR    = 5'h04;    //或
      parameter     A_XOR = 5'h05;    //异或
      parameter     A_NOR = 5'h06;    //或非


      always@(*)
      begin
            case(alu_op)
                  A_ADD:{sign,alu_out}=alu_a+alu_b;
                  A_SUB:{sign,alu_out}=alu_a-alu_b;
                  A_AND:alu_out=alu_a&alu_b;
                  A_OR:alu_out=alu_a|alu_b;
                  A_XOR:alu_out=alu_a^alu_b;
                  A_NOR:alu_out=~(alu_a|alu_b);
                  A_NOP:alu_out=alu_out;
                  default:alu_out=alu_out;
            endcase

      end
```

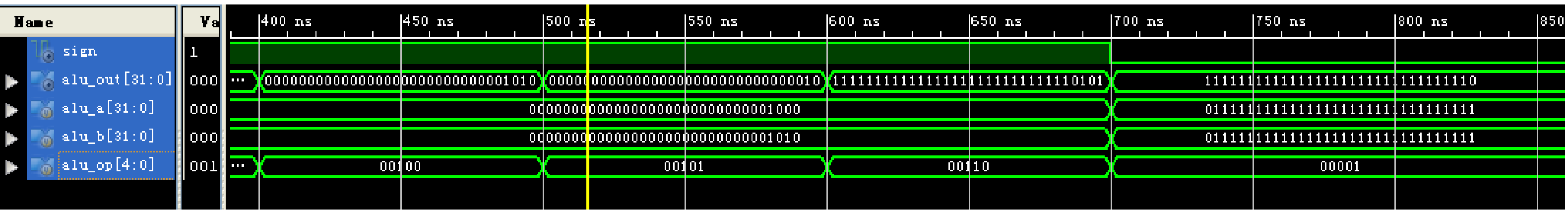
```
endmodule
```

仿真代码：

```
module lab1_alu_test;

    // Inputs
    reg [31:0] alu_a;
    reg [31:0] alu_b;
    reg [4:0] alu_op;

    // Outputs
    wire sign;
    wire [31:0] alu_out;

    // Instantiate the Unit Under Test (UUT)
    ALU uut (
        .alu_a(alu_a),
        .alu_b(alu_b),
        .alu_op(alu_op),
        .sign(sign),
        .alu_out(alu_out)
    );

    initial begin
        // Initialize Inputs
        alu_a = 0;
        alu_b = 0;
        alu_op = 0;

        // Wait 100 ns for global reset to finish
        #100;
      alu_a = 32'h00000008;
        alu_b = 32'h0000000a;
        alu_op = 1;

        #100;
        alu_op = 2;

        #100;
        alu_op = 3;

        #100;
        alu_op = 4;
        #100;
        alu_op = 5;

        #100;
        alu_op = 6;

        #100;
      alu_a = 32'h7fffffff;
        alu_b = 32'h7fffffff;
        alu_op = 1;
        // Add stimulus here

    end

endmodule
```

仿真图：


343.333 ns
Name
Va
0 ns
50 ns
100 ns
150 ns
200 ns
250 ns
300 ns
350 ns
400 ns
450 ns
sign
alu_out[31:0]
alu_a[31:0]
alu_b[31:0]
alu_op[4:0]
1
000
000
000
000
XXXXXXXXXXXXXXXXXXXXXXXXXXXXXXXX
00000000000000000000000000010010
11111111111111111111111111111110
00000000000000000000000000001000
0000000000000000000000000000···
00000000000000000000000000000000
00000000000000000000000000001000
00000000000000000000000000000000
00000000000000000000000000001010
00000
00001
00010
00011
00100


Name
Va
400 ns
450 ns
500 ns
550 ns
600 ns
650 ns
700 ns
750 ns
800 ns
850
sign
alu_out[31:0]
alu_a[31:0]
alu_b[31:0]
alu_op[4:0]
1
000
000
000
001
···
00000000000000000000000000001010
00000000000000000000000000000010
11111111111111111111111111110101
11111111111111111111111111111110
00000000000000000000000000001000
01111111111111111111111111111111
00000000000000000000000000001010
01111111111111111111111111111111
00100
00101
00110
00001