实验报告一

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实验题目：运算器ALU设计

实验要求：

设计一算数运算单元ALU

采用纯组合逻辑设计

32bit位宽

完成指定运算功能

自行设计测试例对所设计的ALU进行仿真

设计思路：

采用always和case语句可直接完成题目要求，同时设置一个一位变量检测溢出情况即可

源代码:

module ALU(

input signed [31:0] alu\_a,

input signed [31:0] alu\_b,

input [4:0] alu\_op,

output reg sign,

output reg [31:0] alu\_out

);

parameter A\_NOP = 5'h00; //空运算

parameter A\_ADD = 5'h01; //符号加

parameter A\_SUB = 5'h02; //符号减

parameter A\_AND = 5'h03; //与

parameter A\_OR = 5'h04; //或

parameter A\_XOR = 5'h05; //异或

parameter A\_NOR = 5'h06; //或非

always@(\*)

begin

case(alu\_op)

A\_ADD:{sign,alu\_out}=alu\_a+alu\_b;

A\_SUB:{sign,alu\_out}=alu\_a-alu\_b;

A\_AND:alu\_out=alu\_a&alu\_b;

A\_OR:alu\_out=alu\_a|alu\_b;

A\_XOR:alu\_out=alu\_a^alu\_b;

A\_NOR:alu\_out=~(alu\_a|alu\_b);

A\_NOP:alu\_out=alu\_out;

default:alu\_out=alu\_out;

endcase

end

endmodule

仿真代码：

module lab1\_alu\_test;

// Inputs

reg [31:0] alu\_a;

reg [31:0] alu\_b;

reg [4:0] alu\_op;

// Outputs

wire sign;

wire [31:0] alu\_out;

// Instantiate the Unit Under Test (UUT)

ALU uut (

.alu\_a(alu\_a),

.alu\_b(alu\_b),

.alu\_op(alu\_op),

.sign(sign),

.alu\_out(alu\_out)

);

initial begin

// Initialize Inputs

alu\_a = 0;

alu\_b = 0;

alu\_op = 0;

// Wait 100 ns for global reset to finish

#100;

alu\_a = 32'h00000008;

alu\_b = 32'h0000000a;

alu\_op = 1;

#100;

alu\_op = 2;

#100;

alu\_op = 3;

#100;

alu\_op = 4;

#100;

alu\_op = 5;

#100;

alu\_op = 6;

#100;

alu\_a = 32'h7fffffff;

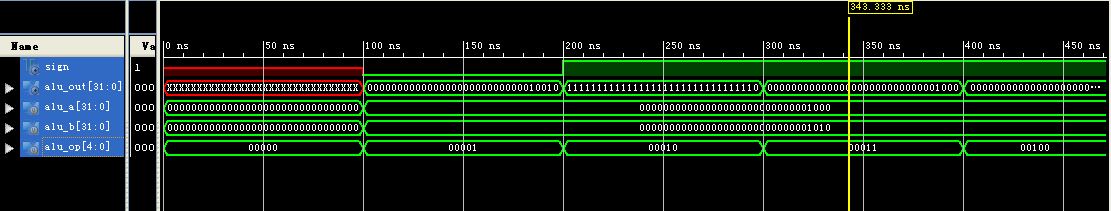
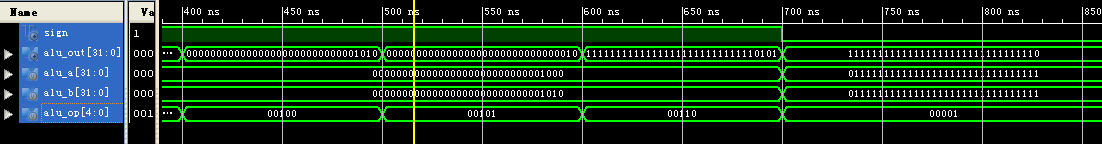
alu\_b = 32'h7fffffff;

alu\_op = 1;

// Add stimulus here

end

endmodule

仿真图：