2K EEPPROM IP 简介

* 存储器大小：2kbits(64x32)
* 读取工作电压低至0.7v，8bits输出
* 编程电压1.6v~2.3v，16bits写入
* 低功耗，1v工作电压下读取电流低至1uA
* 支持全片擦除和扇区擦除
* 读取时间：6us/8bits
* 编程时间：4.5ms/16bits

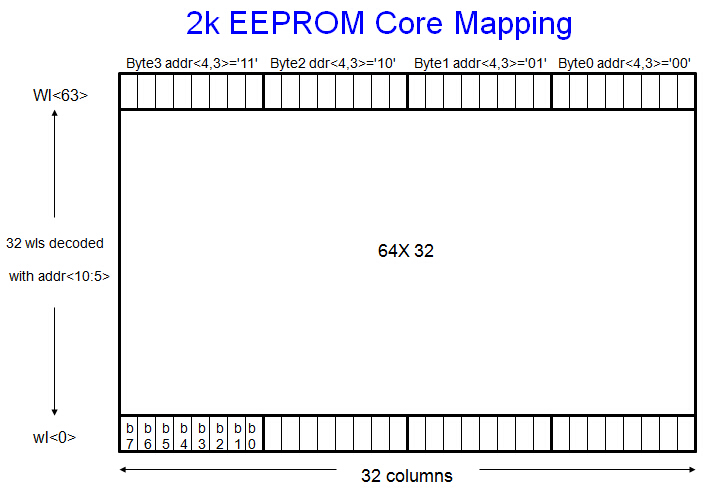
**概述**

EE2K IP是一个2K bits并行输入并行输出的 CMOS EEPROM,内部含有256个8位字节。编程方式为字编程，即每次编程2个字节。同时提供页擦除和全片擦除模式。编程和擦除的时序由内部产生，但需要数字控制模块按照时序要求给予足够的脉冲宽度

IP 特性

|  |  |
| --- | --- |
| **特性** | **描述** |
| 名称 | EE2k |
| 存储密度 | 2Kbits |
| 工艺 | SMIC 0.18um 2Poly/4Metal EEPROM process |
| 电压范围 | 0.5 ~ 2.4 V |
| 温度范围 | -40 ~ 85 °C |
| 编程 | word program current: <40uA@1.92MHz word program time: 4.5ms |
| 读取 | Read current: <1.2uA Read time: 6us/Byte |

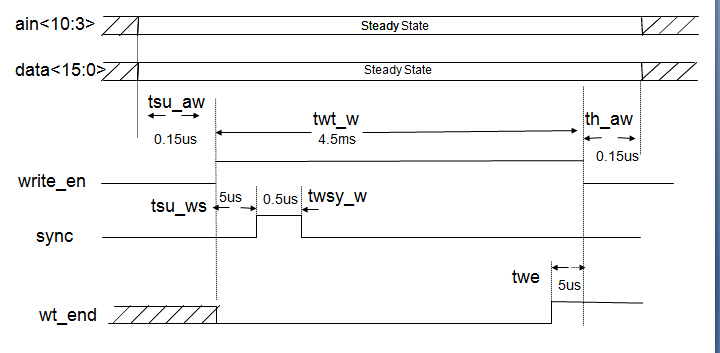
2k EEPROM Core Mapping



端口描述

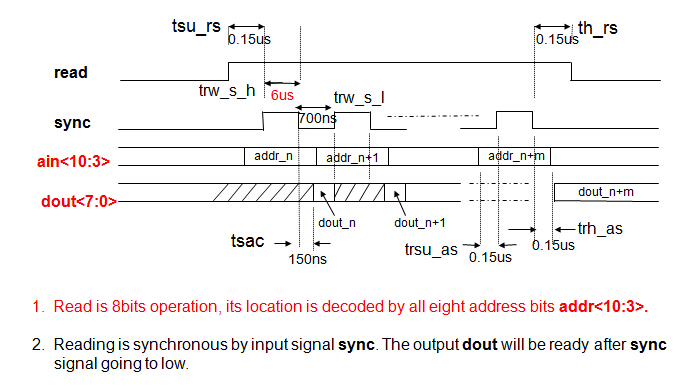
|  |  |  |
| --- | --- | --- |
| **Pin Name** | **I/O** | **Description** |
| ain<10:3> | I | From Digital,address signal |
| read | I | From Digital,Read enable signal |
| write\_en | I | From Digital,Write enable signal |
| sync | I | From Digital,Synchronous signal for data loading and read operation |
| clk | I | From Analog, Clock for driving high voltage charge pump |
| data<15:0> | I | From Digital,Parallel data inputs for write operation |
| dout<7:0> | O | To Digital,Memory parallel bit outputs |
| allrow<1:0> | I | From Digital,Turning on all or half portion's word lines for fast chip erase |
| robust\_p | I | From Digital,Programming verification."1" for robust programming. |
| wt\_end | O | To Digital,After writing is finished,IP send this flag to digital circuit. |
| vpp | P | To monitor,To monitor internal charge pump output for EEPROM |
| vcca!(UNK) | P | From Analog,Power supply for memory operation,connected to UNK |
| gnd! | P | From Analog,ground |

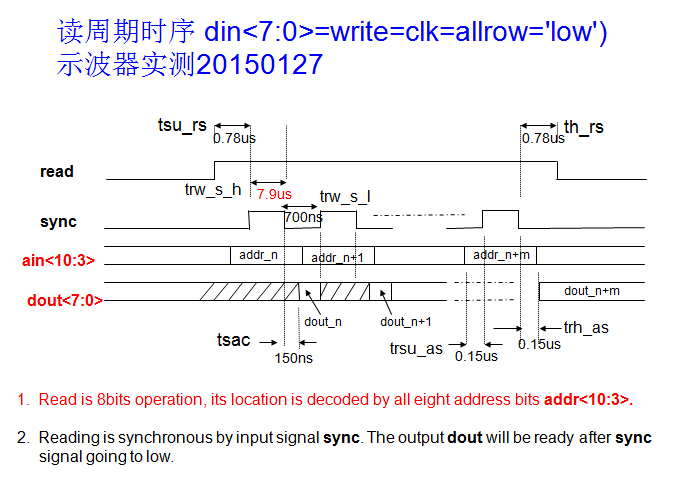
写周期时序(write\_en='1',read=allrow='0')



|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Description** | **Min.** | **Type** | **Max** | **Unit** |
| tsu\_aw | Setup time of ain to write\_en high in write mode | 0.15 |  |  | us |
| th\_aw | Hold time of ain to write\_en low in write mode | 0.15 |  |  | us |
| tsu\_ws | Setup time of write\_en high to sync high in write mode | 5 |  |  | us |
| twsy\_w | Pulse width of sync high in write mode | 0.5 |  |  | us |
| trh\_as | Hold time of wt\_end high to write\_em low in write mode | 5 |  |  | us |

读周期时序 din<7:0>=write=clk=allrow='low')

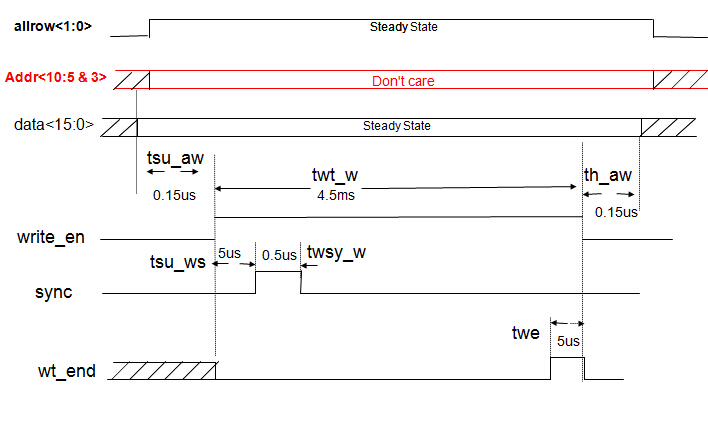




|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter** | **Description** | **Min.** | **Type** | **Max** | **Unit** |
| tsu\_rs | Setup time from read high to sync high | 0.15 |  |  | us |
| th\_rs | hold time from read low to sync low | 0.15 |  |  | us |
| trw\_s\_h | Pulse width of sync high in read mode |  | 6 |  | us |
| trw\_s\_l | Pulse width of sync low in read mode | 0.7 |  |  | us |
| trcyc\_s | Cycle time of sync in read mode |  | 7 |  | us |
| tsac | Dout ready after sync low | 0.15 |  |  | us |
| trsu\_as | Setup time of addr to sync high in read mode | 0.15 |  |  | us |
| trh\_as | Hold time of addr to sync low in read mode | 0.15 |  |  | us |

Allrow (All Word Lines On Mode):

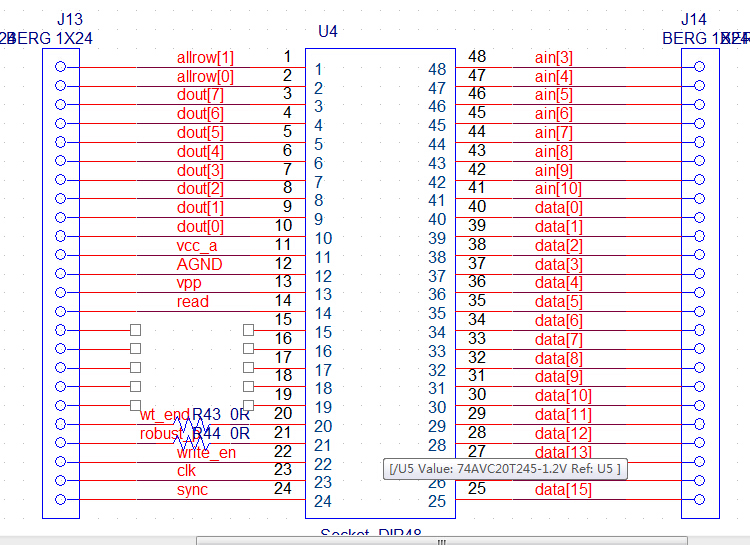
* allrow模式提供全片擦除或扇区擦除
* In the "All Word Lines On" mode, The word data will be written into all the same word locations respectively in all 64 word lines.
* The word loaction is defined by address bit ain<4>.
* Treat signal allrow as an one of the regular address bit. All the timing spec will be same as that of the regular write.



Allrow<1:0> Truth Table

|  |  |
| --- | --- |
| **allrow<1：0>** | **Which Portion All Word Lines Will Be Activated** |
| 0 0 | Regular single word line operation |
| 0 1 | All 32 word lines of lower 1kbit’s block |
| 1 0 | All 32 word lines of upper 1kbit’s block |
| 1 1 | All 64 word lines |

EEPROM管脚信息：



EEPROM测试关键点：

1. stm32与eeprom接口之间的电平转换，需采用多级转换（参照电源转换芯片的datasheet）
2. 示波器抓取读写时序，测试STM32读写驱动是否满足eeprom的读写要求
3. 各种条件下的读写数据测试。