Introduction to Pipelining

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- Conclude the discussion on multi-cycle computations from last lecture
- Introduce pipelining, a technique that uses registers to improve the throughput of a circuit
- Examine the tradeoffs of different design styles (combinational, pipelined, multi-cycle) through a multiplier case study

Reminder: Multi-Cycle Computations

- Sequential circuits can implement more computations than combinational circuits
  - Variable amount of input/output
  - Variable number of steps

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- Sequential circuits can implement more computations than combinational circuits
  - Variable amount of input/output
  - Variable number of steps

- Multi-cycle circuits implement a computation over multiple cycles
  - New computation is started by setting inputs at a particular cycle
  - Circuit takes several cycles (possibly a variable number) to finish computation, then makes output available
  - Circuit performs only one computation at a time; a new computation cannot begin until previous one has finished

Reminder: GCD Circuit

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def gcd(a, b):
  x = a
  y = b
  while x != 0:
    if x >= y:
      x = x - y
    else:
      (x, y) = (y, x)
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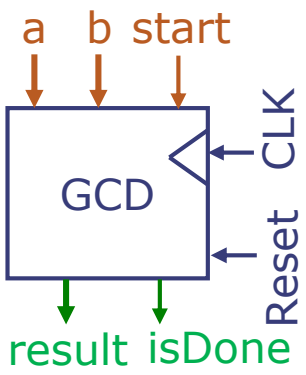


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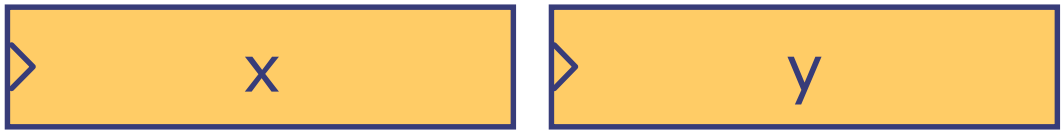

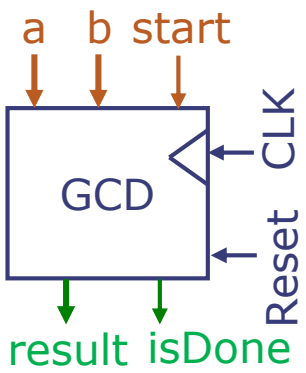


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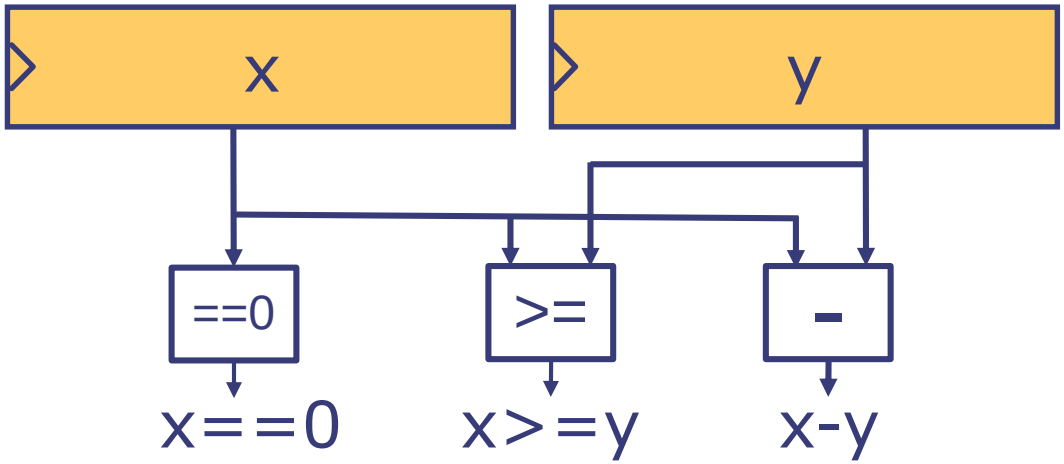

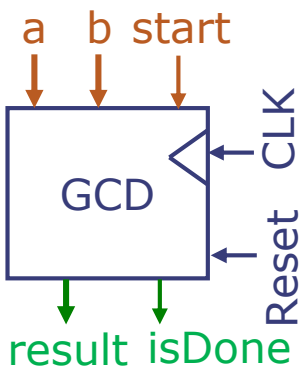


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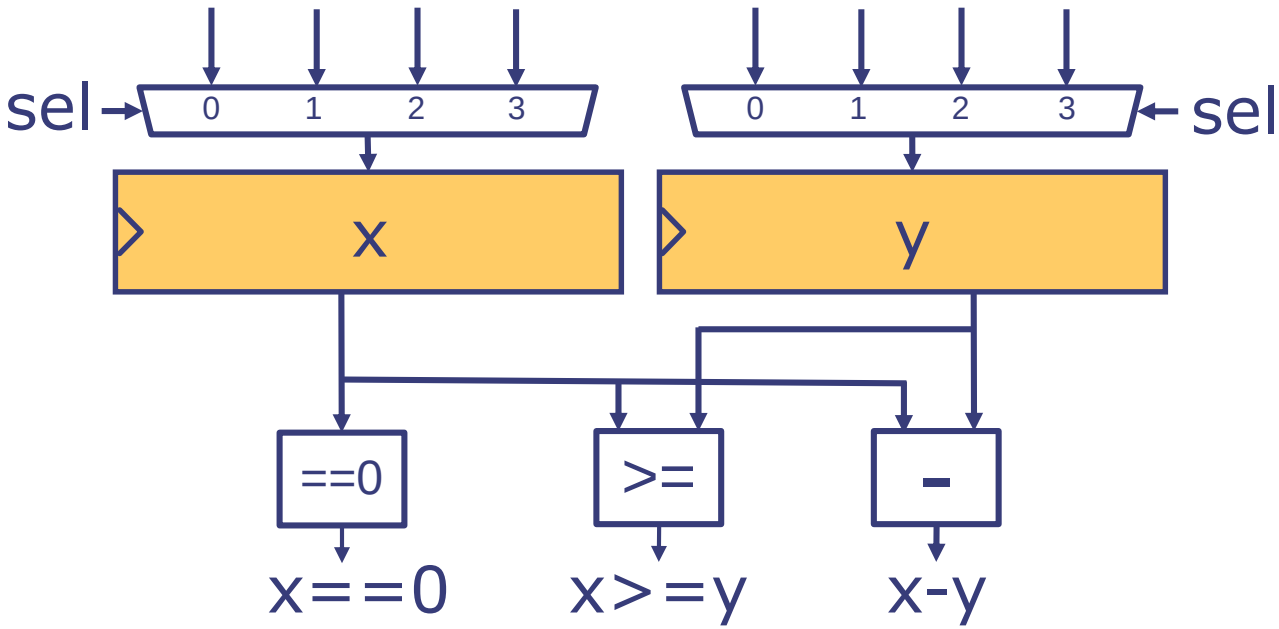

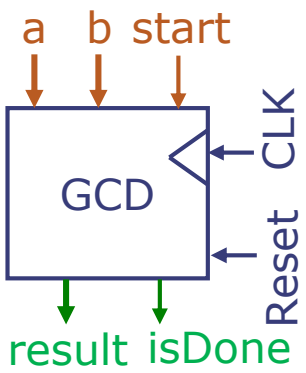


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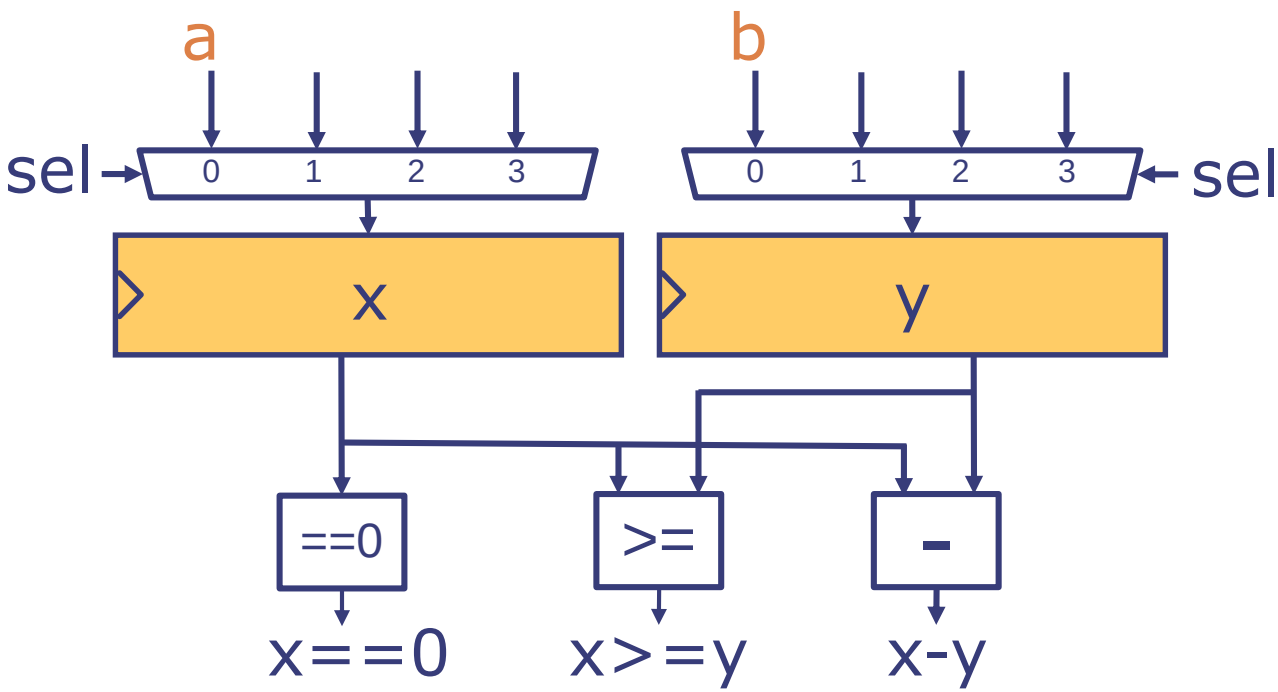

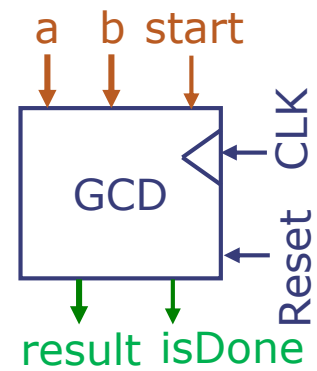


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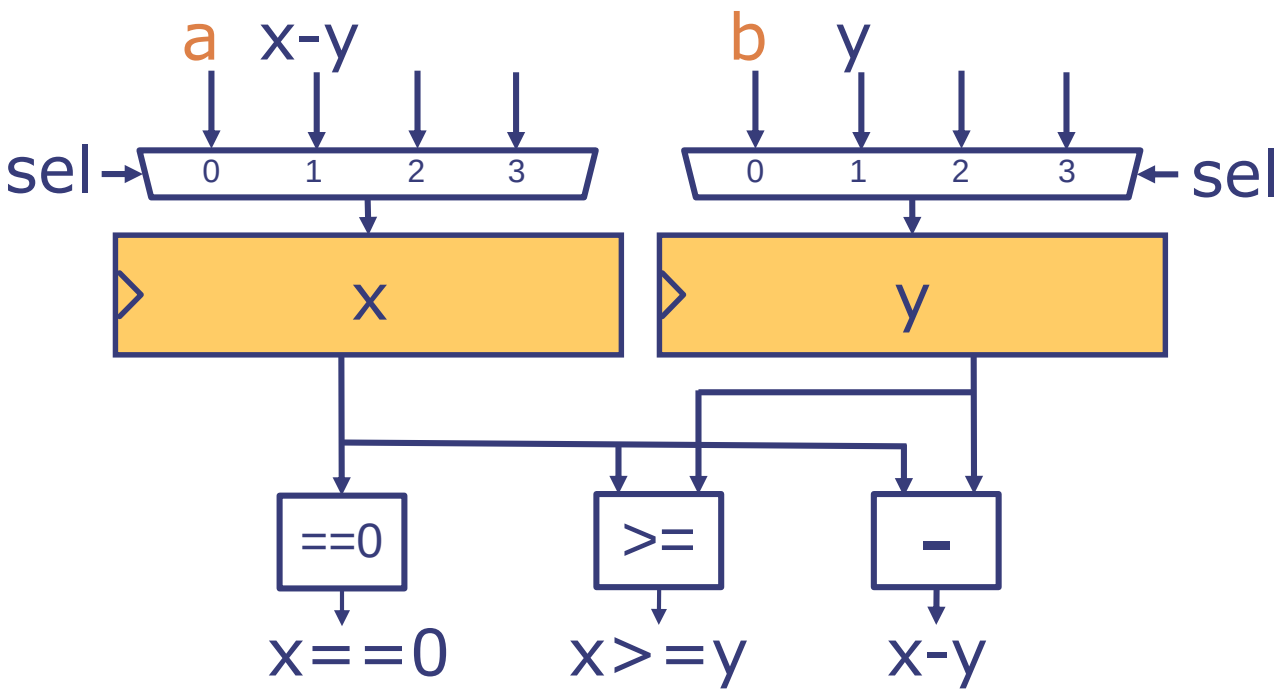

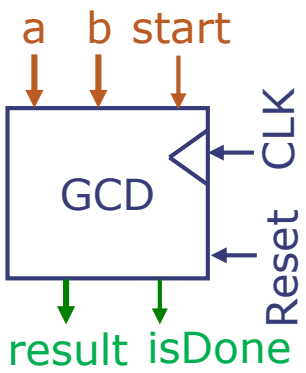


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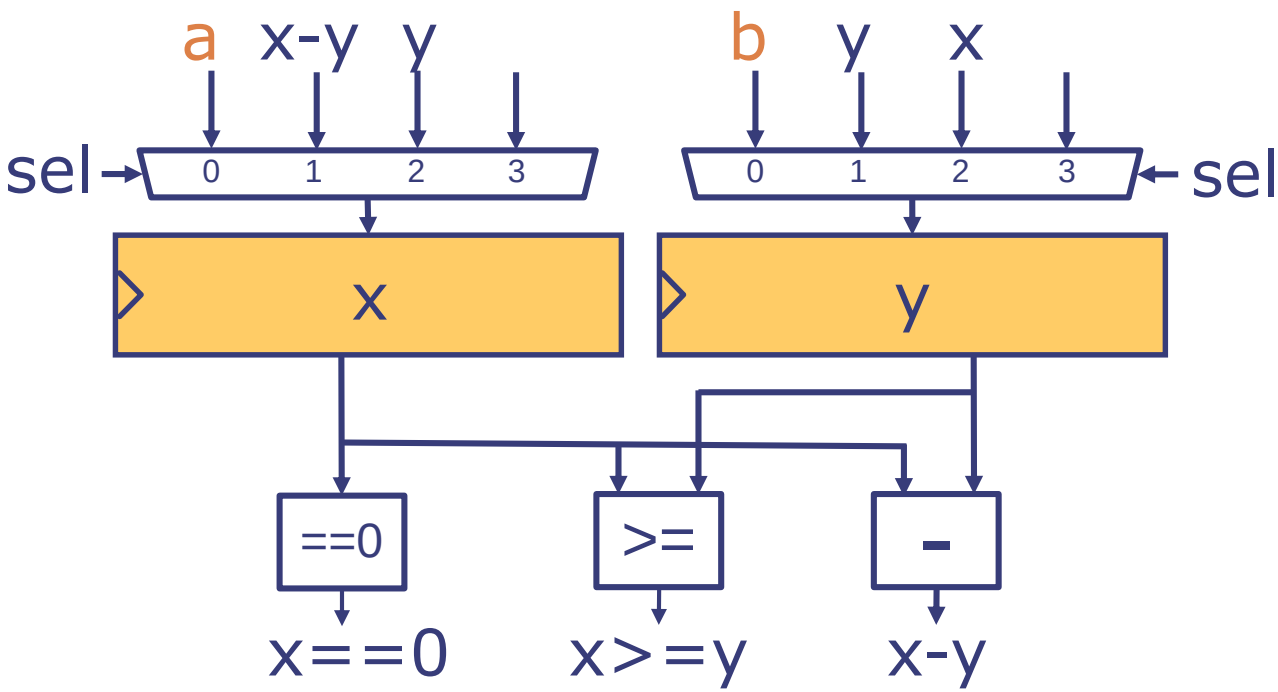

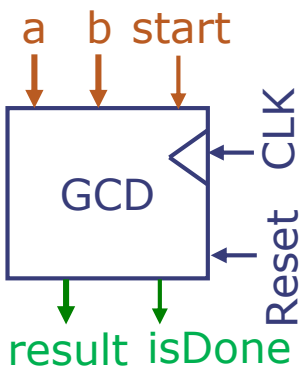


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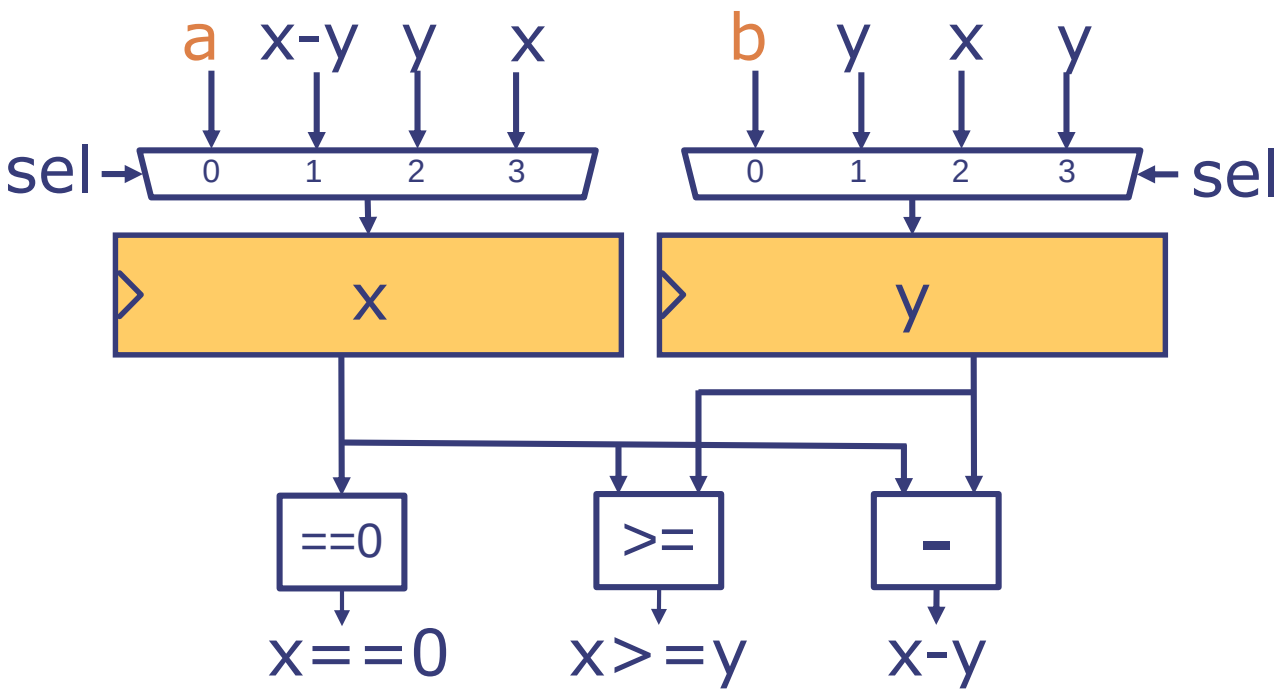

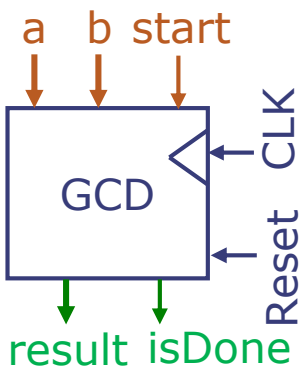


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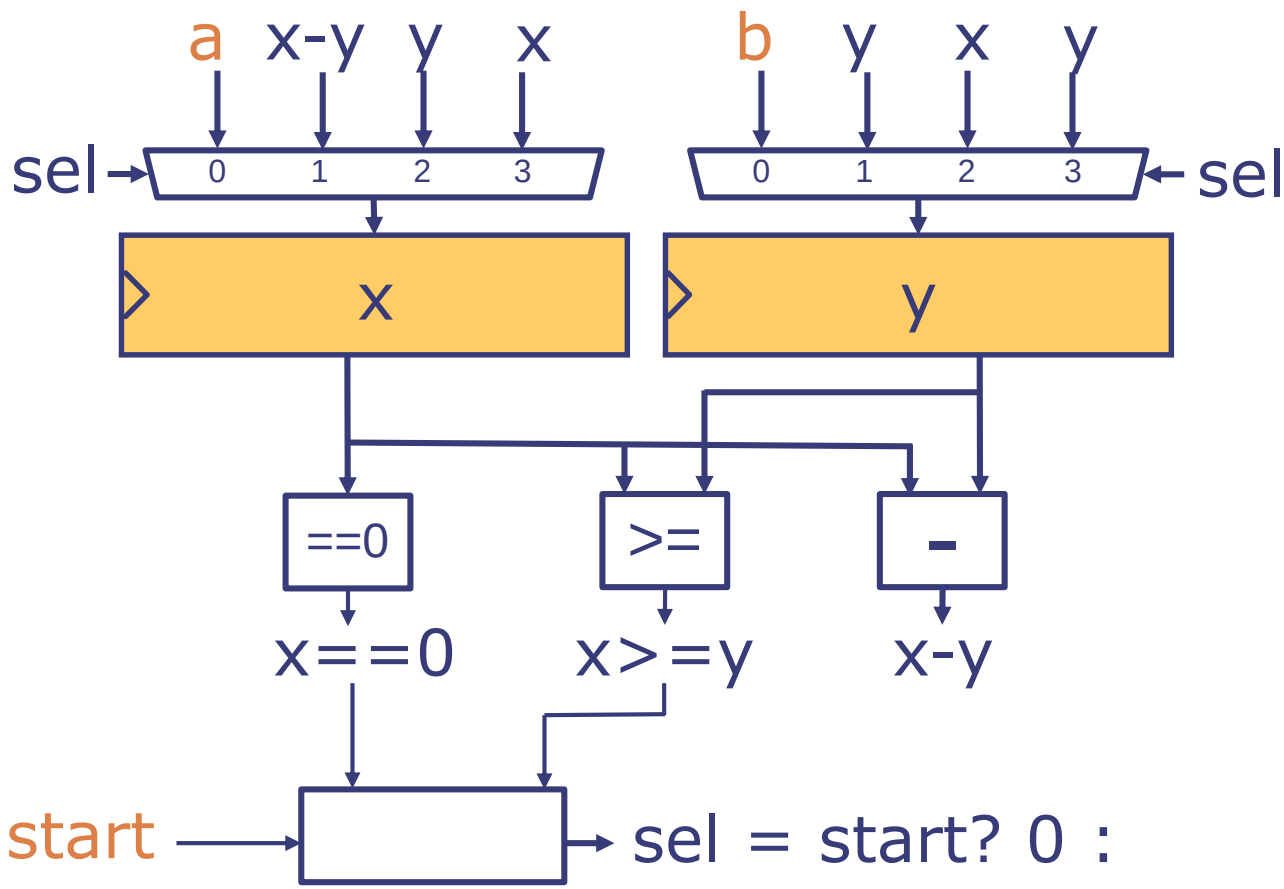

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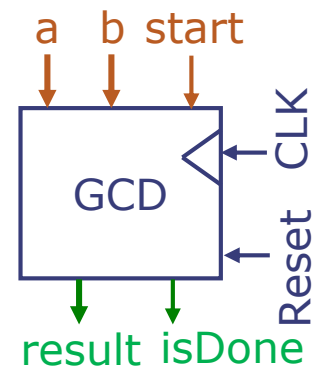


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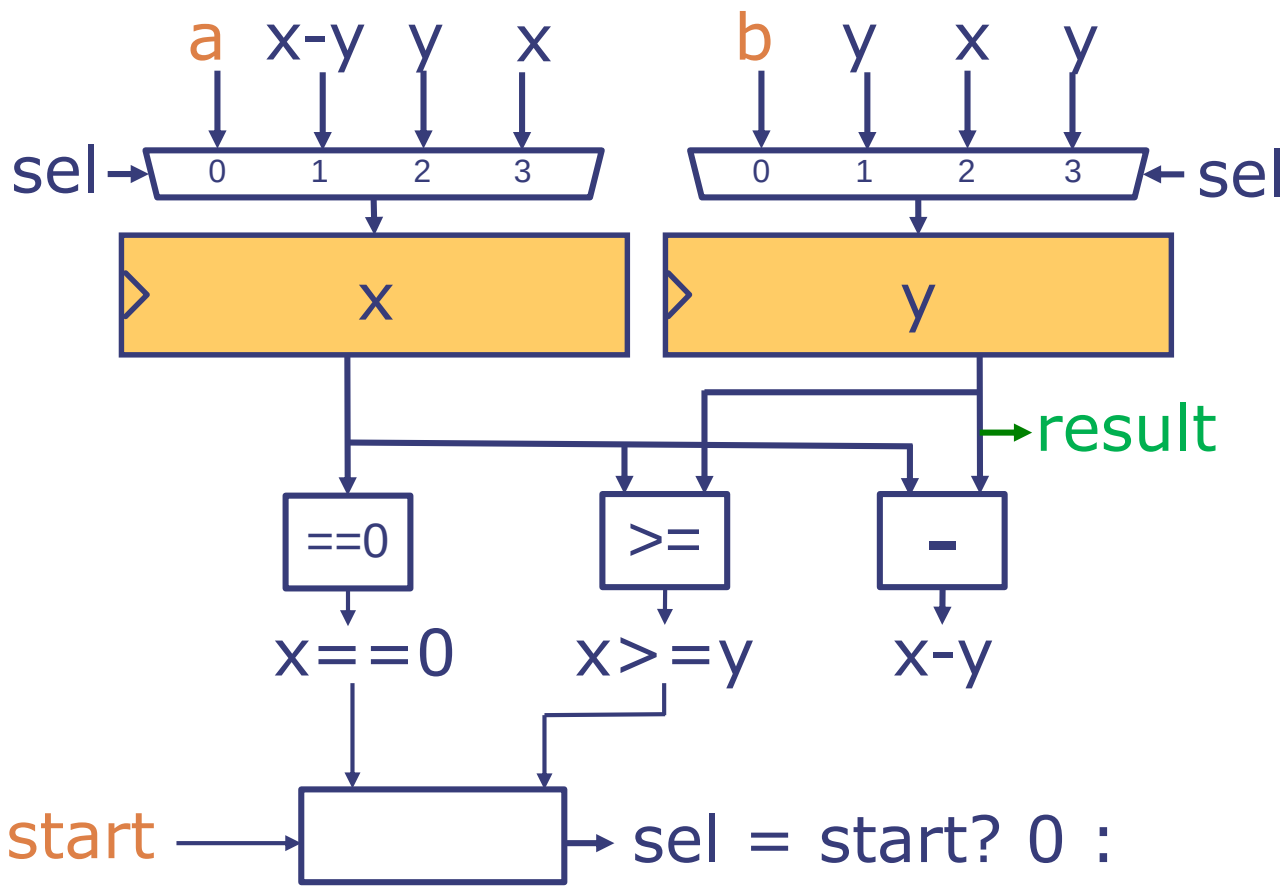

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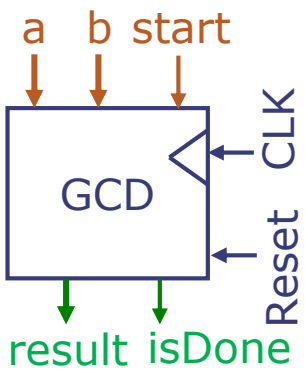


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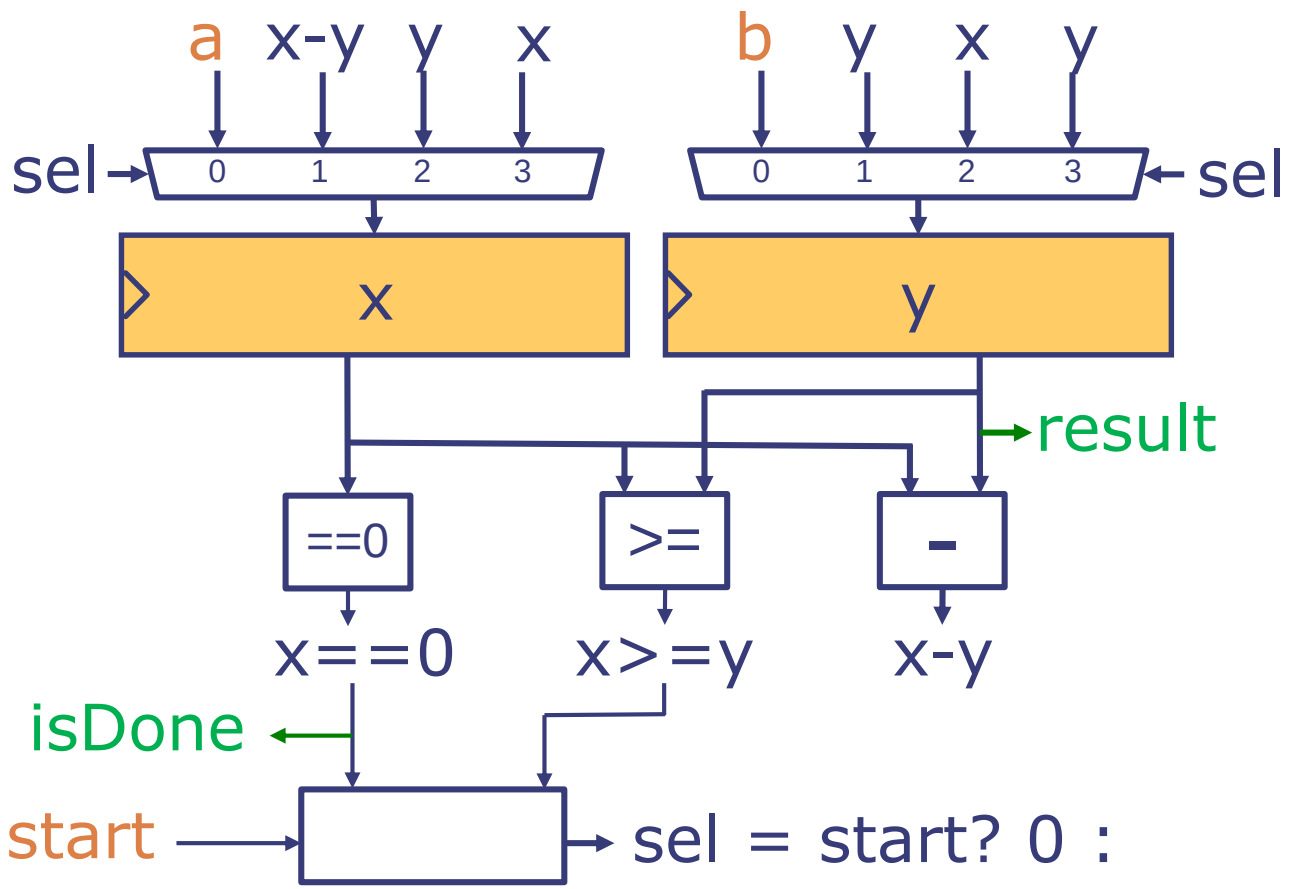

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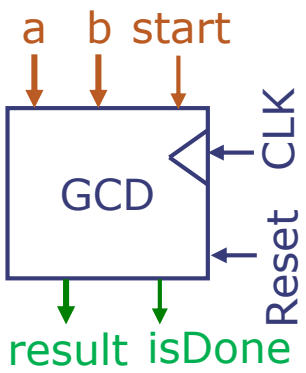


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- Several cycles later, the module signals that it has finished by having *isDone* return True; only then, the *result* method returns the correct result for gcd(a,b)

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  - This requires we learn about one last type…

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Maybe#(Word) x = Invalid;    // no need to give value!
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Maybe#(Word) x = Invalid;     // no need to give value!
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if (isValid(y))               // check validity
  Word z = fromMaybe(?, y);   // extract valid value
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Improved GCD Module
Using Maybe Types

```
typedef struct {Word a; Word b;} GCDArgs;
module GCD;
  Reg#(Word) x(1);
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endmodule
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Single input and output:

- New GCD computation is started by setting a Valid input *in* (which always includes a and b)
- When GCD computation finishes, *result* becomes a Valid output

Pipelined Circuits

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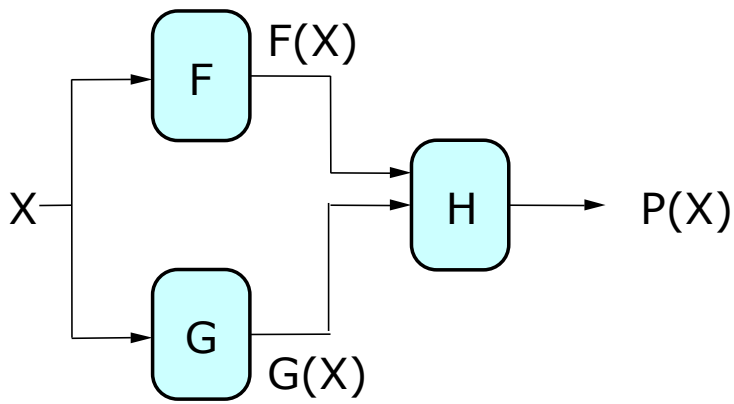
  - *Airbag deployment system?* Latency
  - *General-purpose processor?* Throughput (maximize instructions/second)

Performance of Combinational Logic

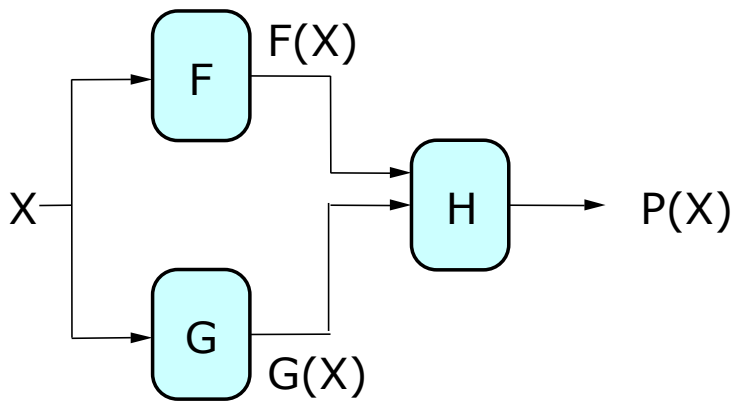


For combinational logic:

latency = t_{PD}

throughput = $1/t_{PD}$

Performance of Combinational Logic



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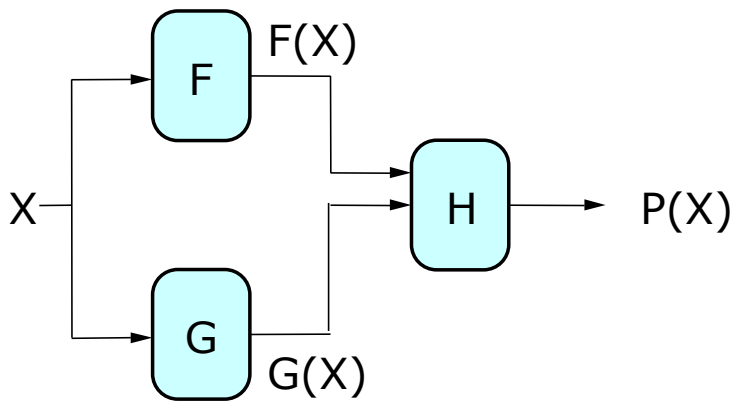

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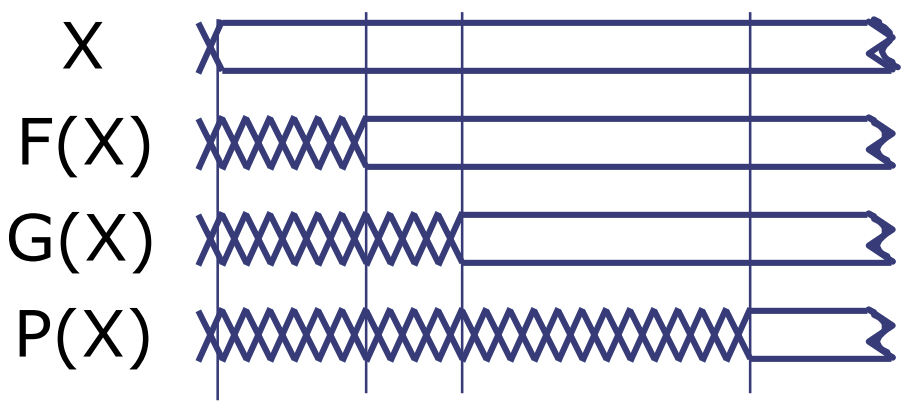

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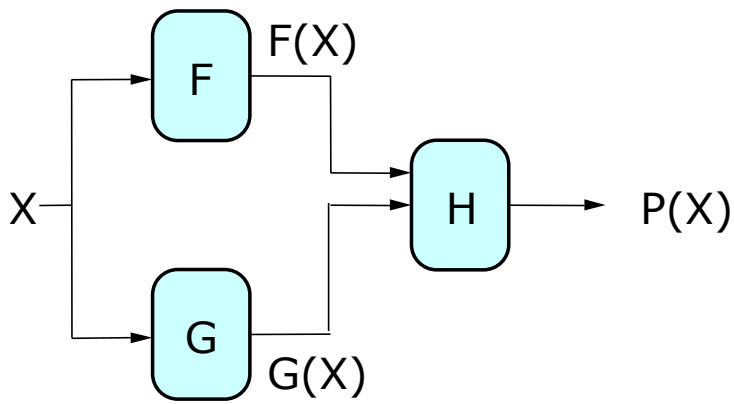

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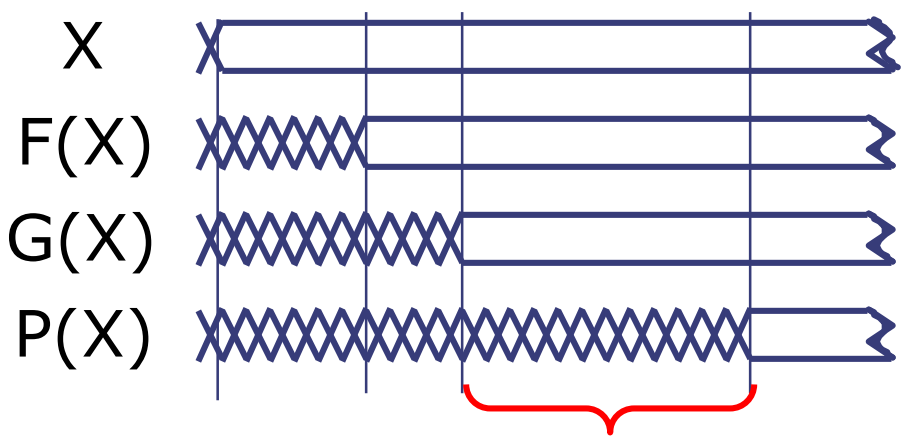
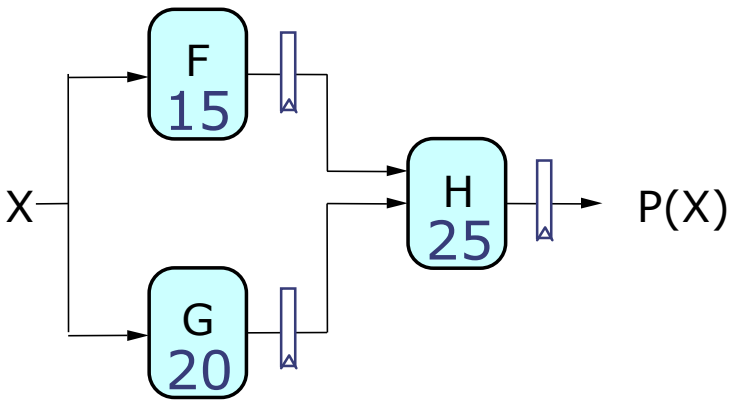


F & G are "idle", just holding their outputs stable while H performs its computation

Pipelined Circuits

Use registers to hold H's input stable!



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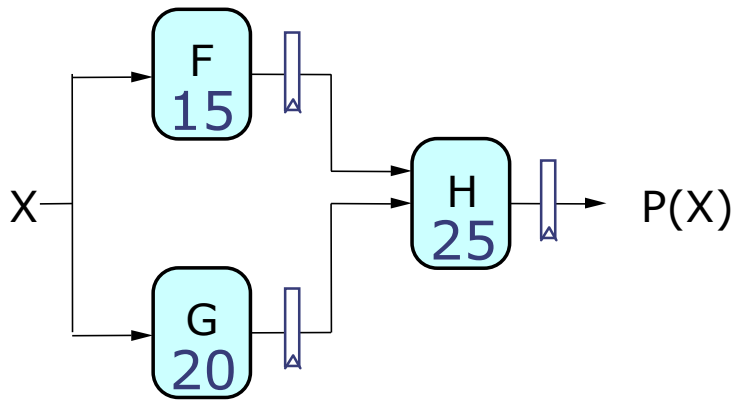

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unpipelined	45 ns	1/(45 ns)
2-stage pipeline	_____	_____

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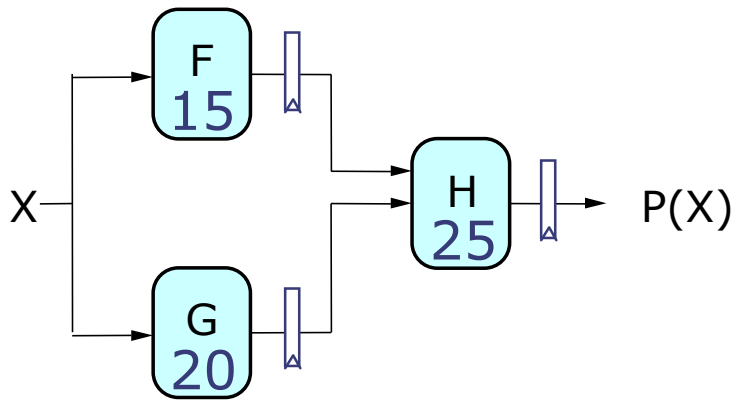

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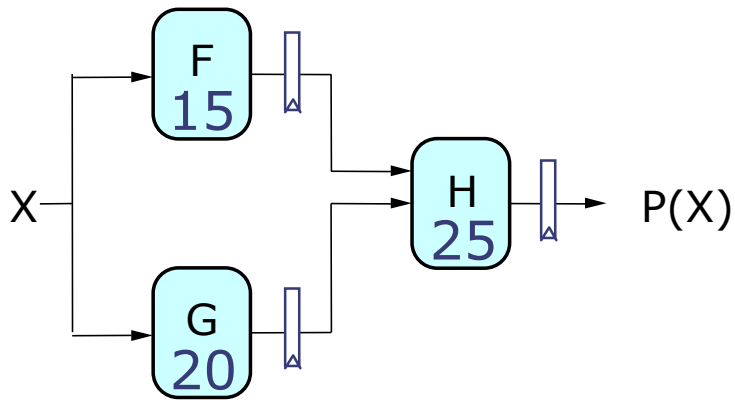

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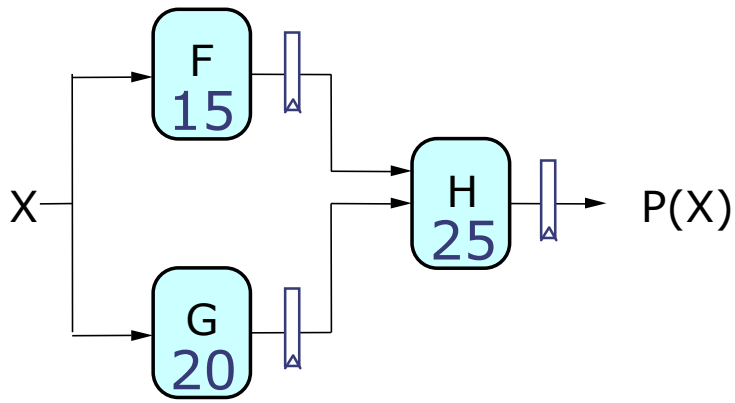

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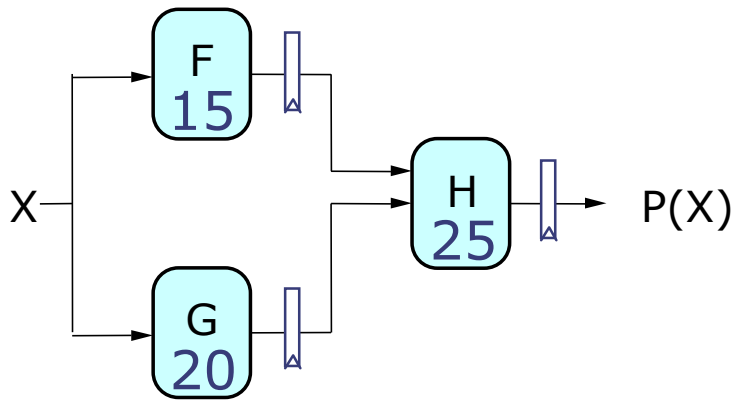

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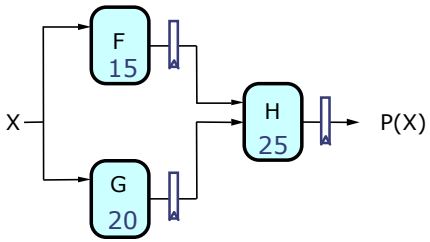
	worse	better!

Pipeline Diagrams



Clock cycle →

Pipeline stages ↓	i	i+1	i+2	i+3	
F & G					
H					

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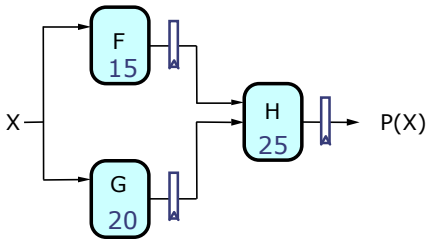

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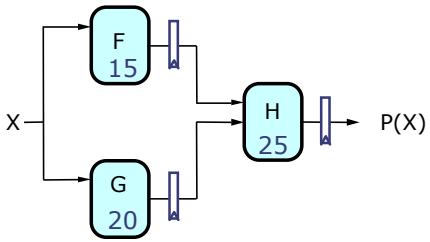

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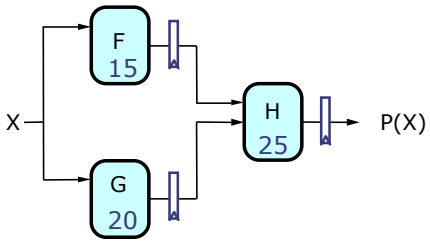

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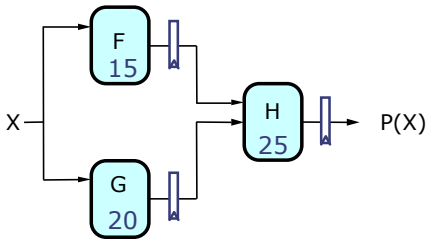

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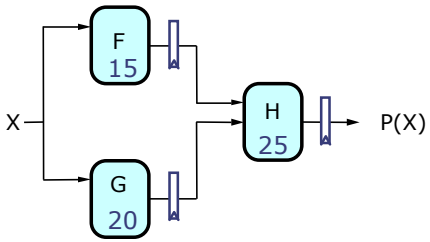

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The results associated with a particular set of input data moves *diagonally* through the diagram, progressing through one pipeline stage each clock cycle.

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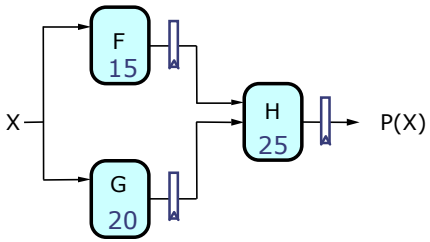

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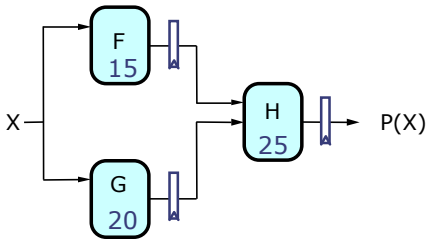

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H		$H(X_i)$	$H(X_{i+1})$	$H(X_{i+2})$

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Pipeline Conventions

Definition:

A well-formed *K-Stage Pipeline* ("K-pipeline") is an acyclic circuit having exactly K registers on *every* path from an input to an output.

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K-pipeline latency $L = K * t_{CLK}$

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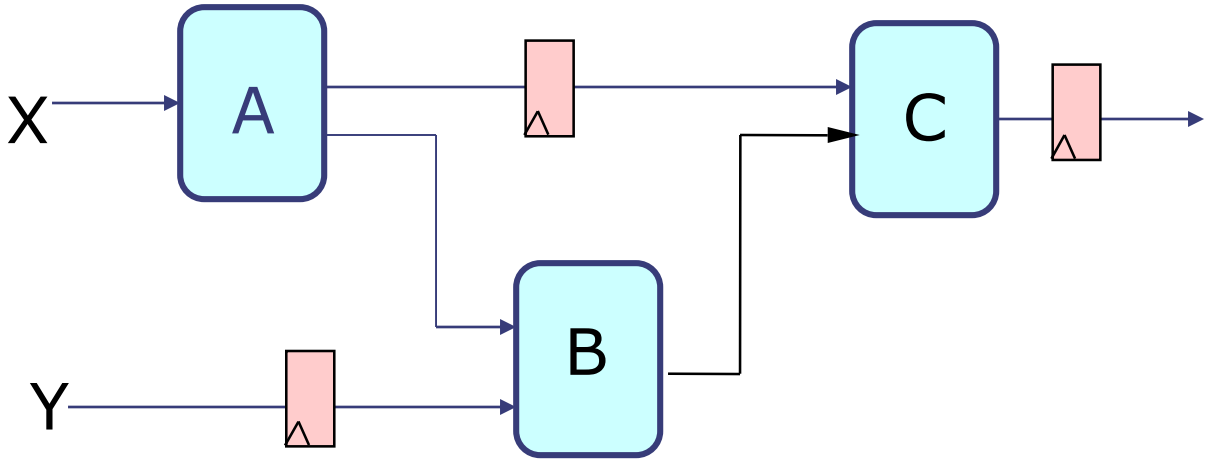
Ill-Formed Pipelines

Consider a BAD job of pipelining:



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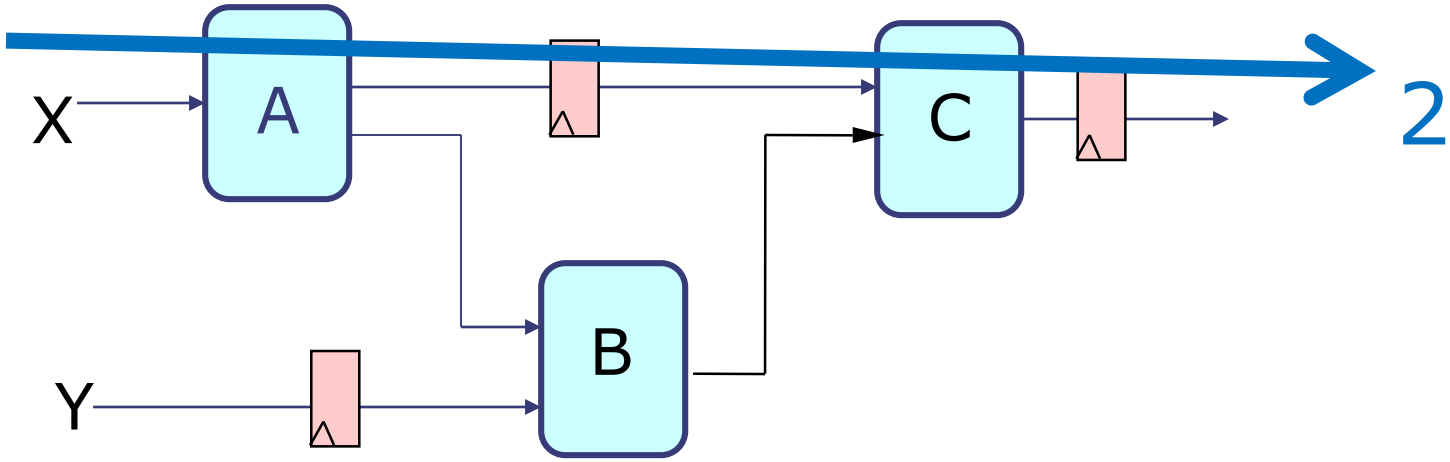

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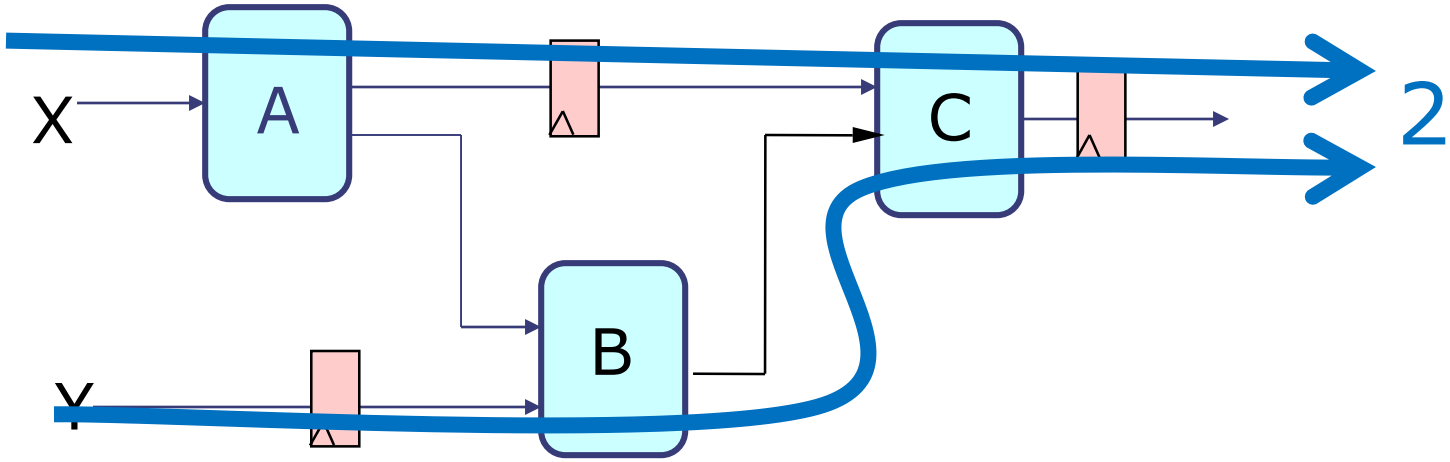

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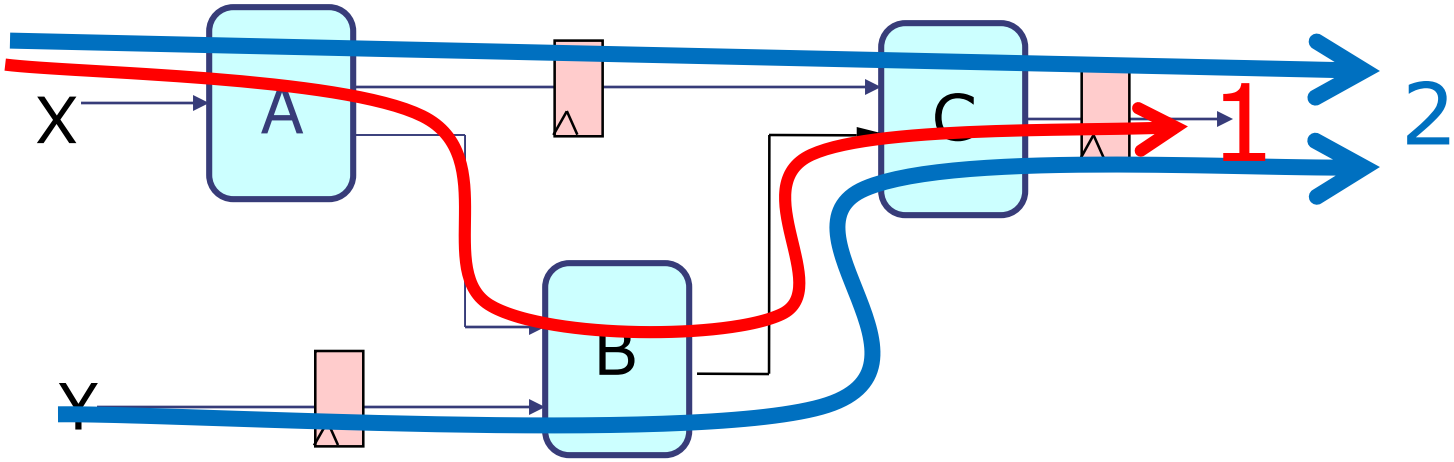

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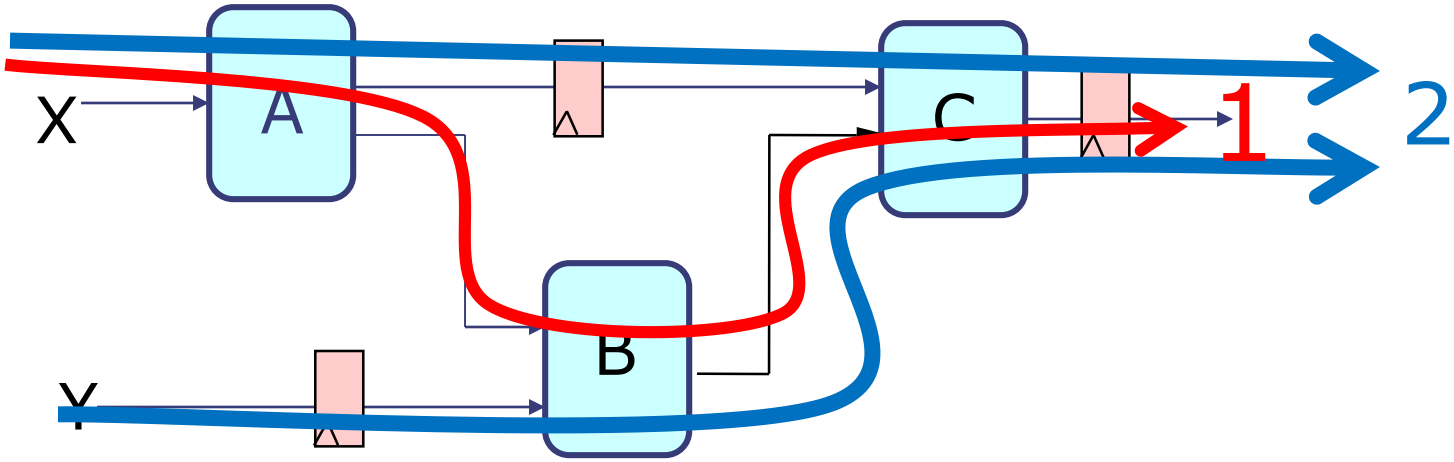

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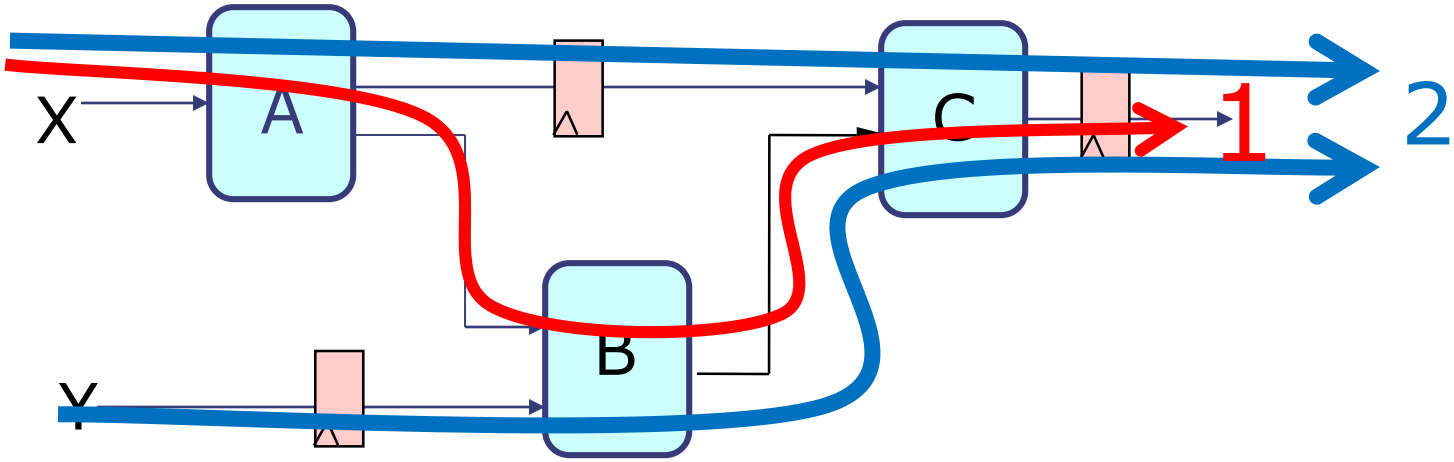

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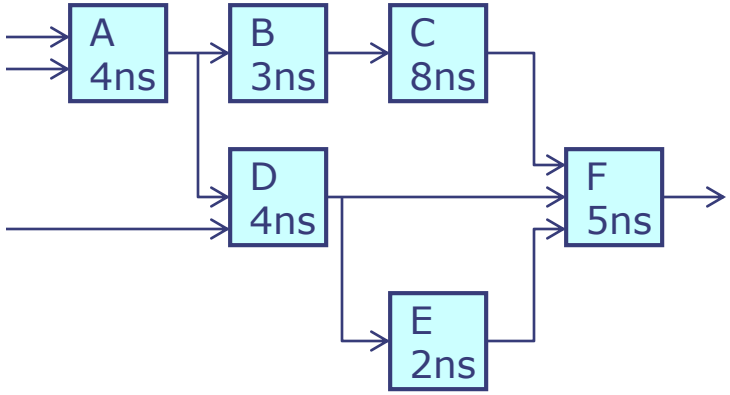
Problem:

Successive inputs get mixed: e.g., $B(A(X_{i+1}), Y_i)$. This happens because some paths from inputs to outputs have 2 registers, and some have only 1!

This can't happen in a well-formed K pipeline!

A Pipelining Methodology



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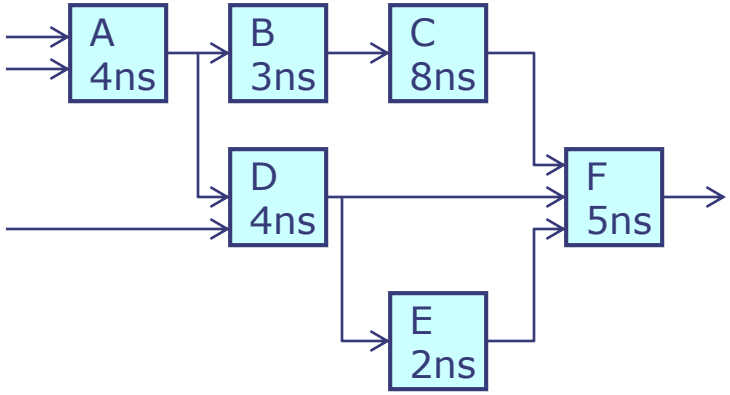

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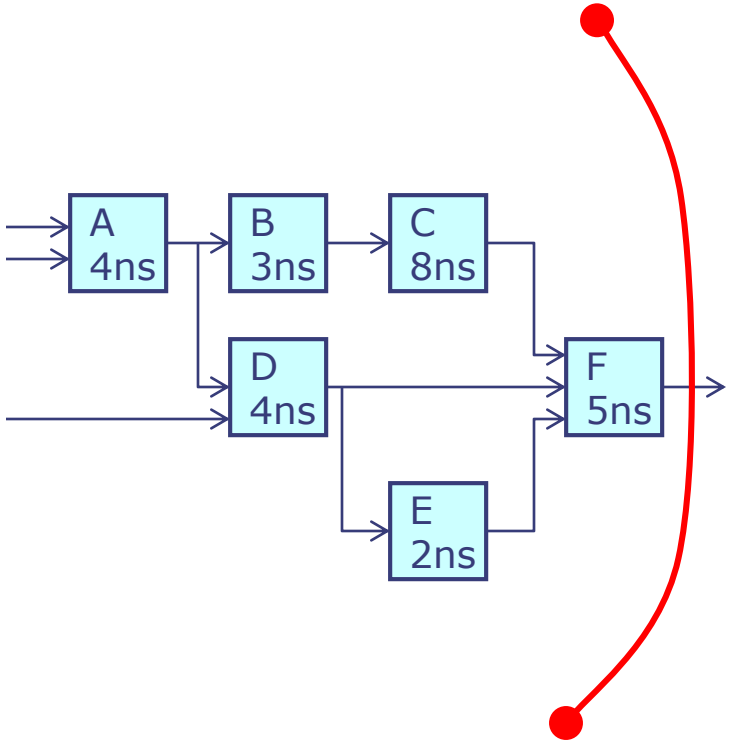

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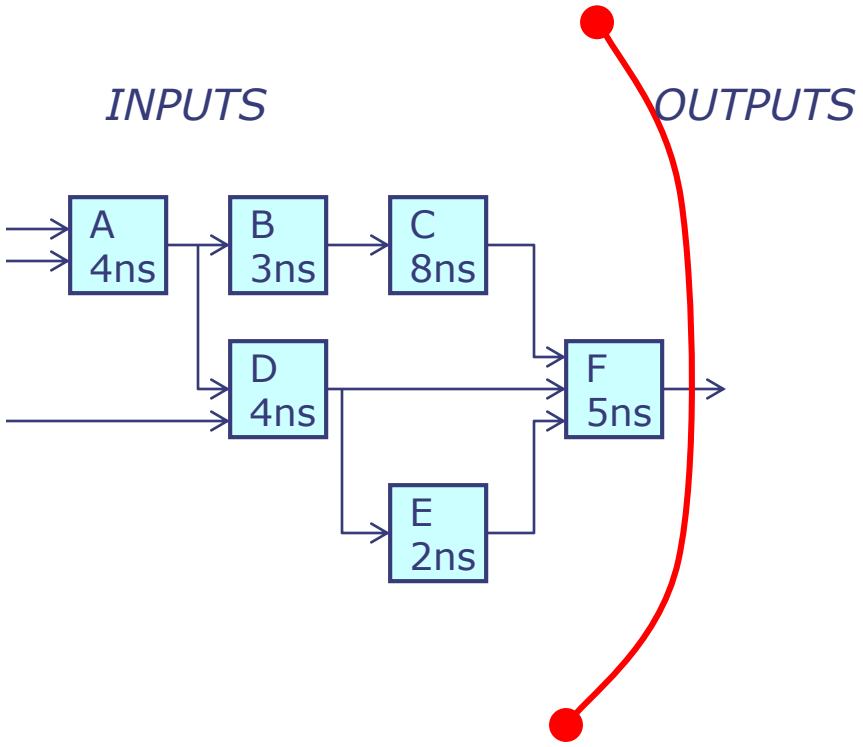

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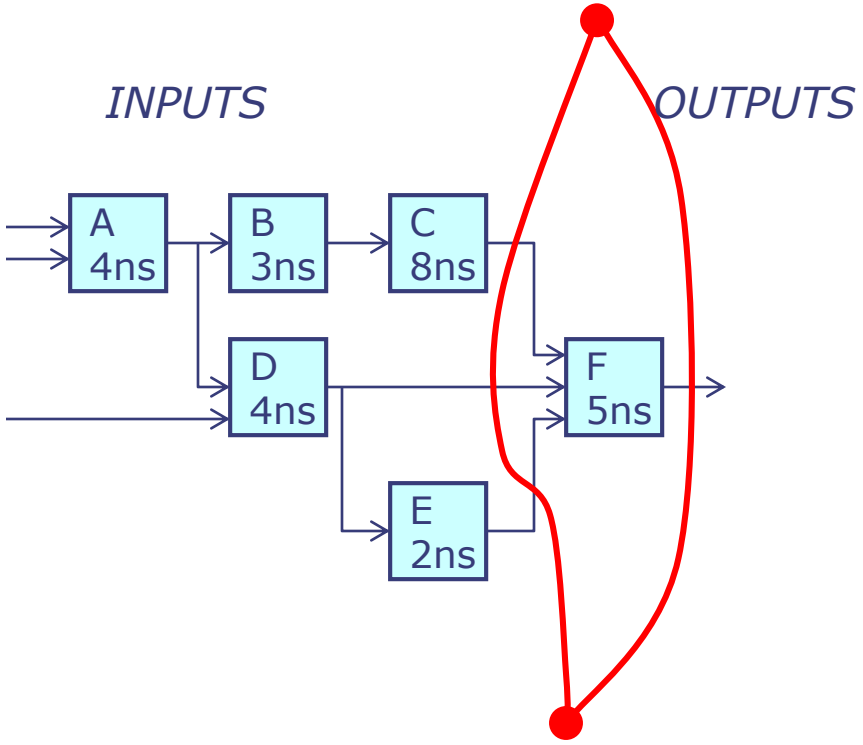

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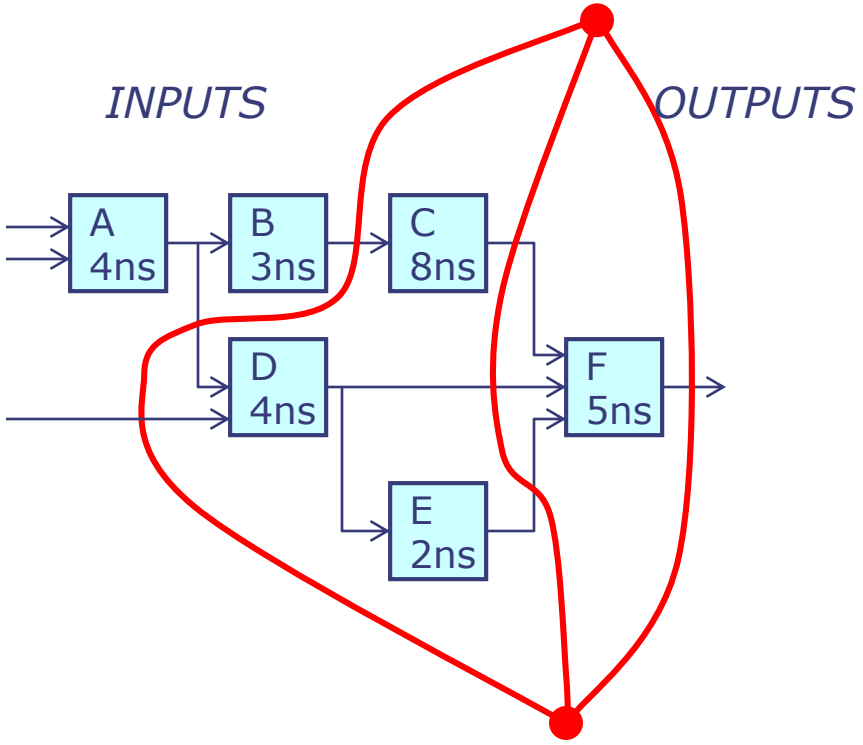

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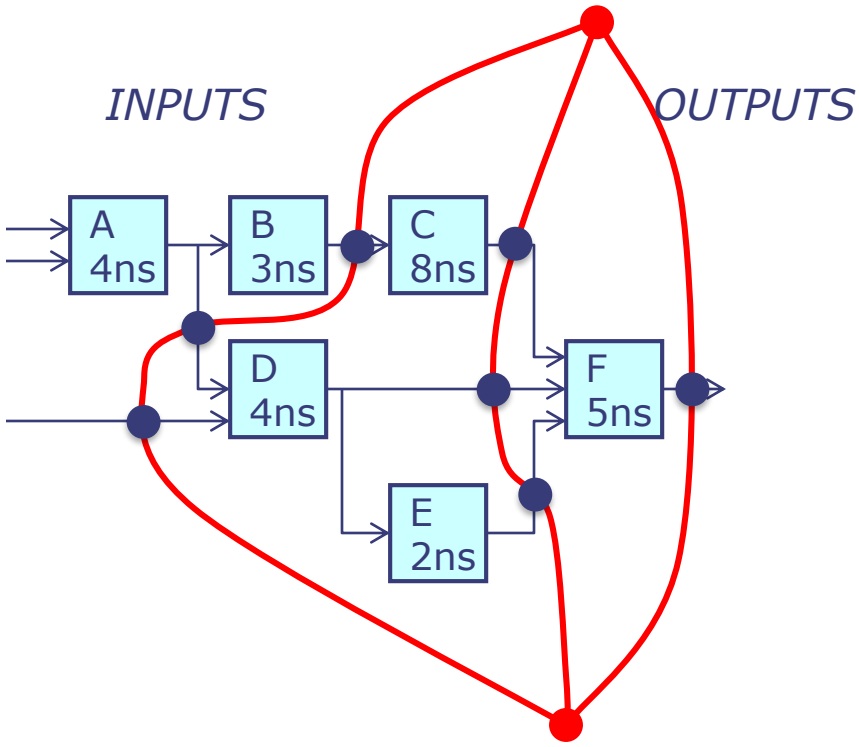
Adding a pipeline register at every point where a separating line crosses a connection will always generate a valid pipeline.



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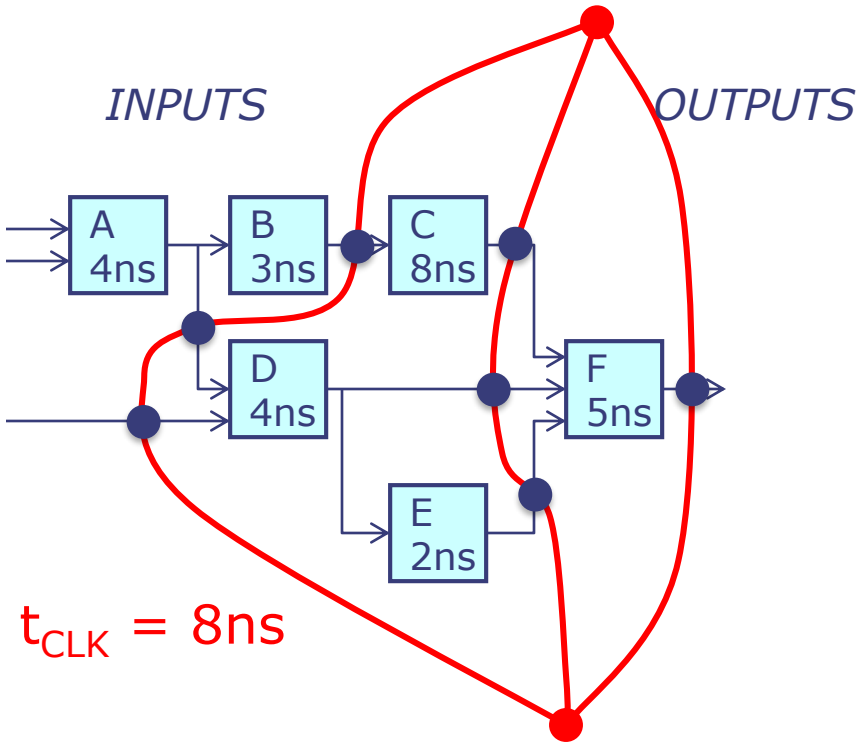

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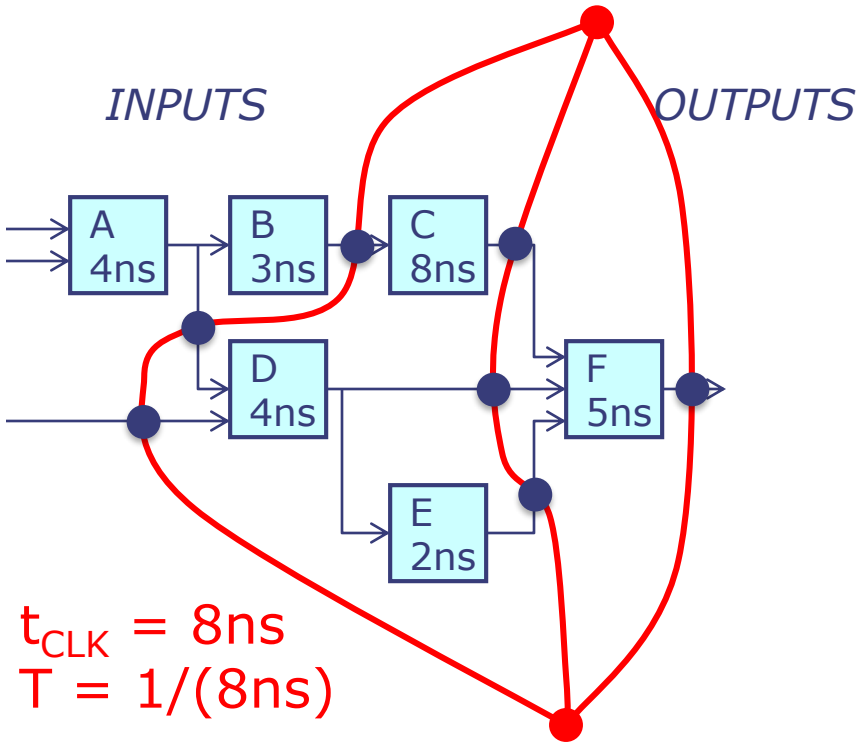

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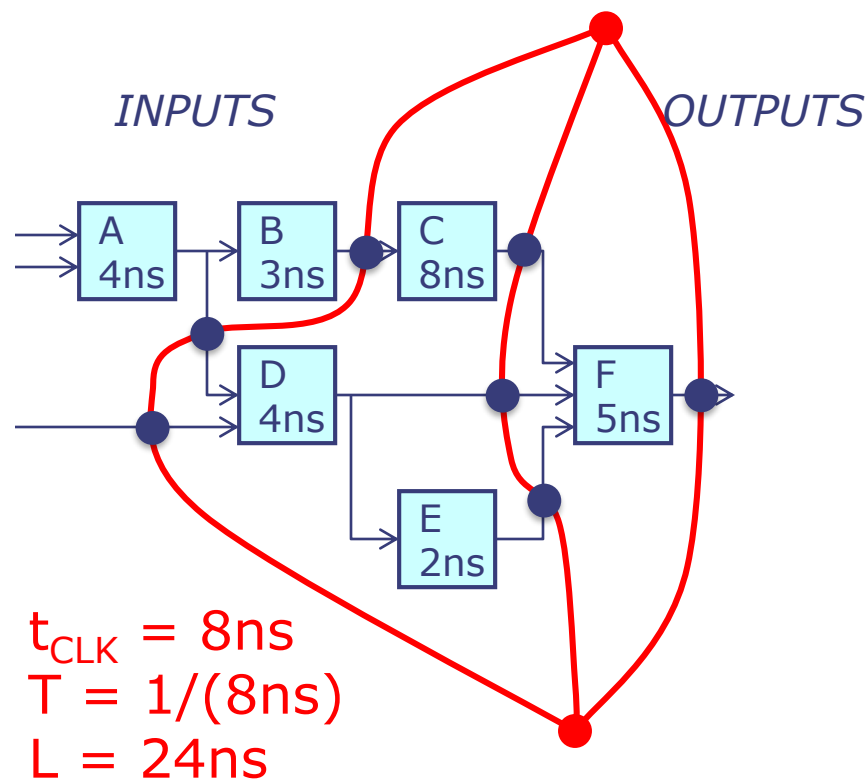

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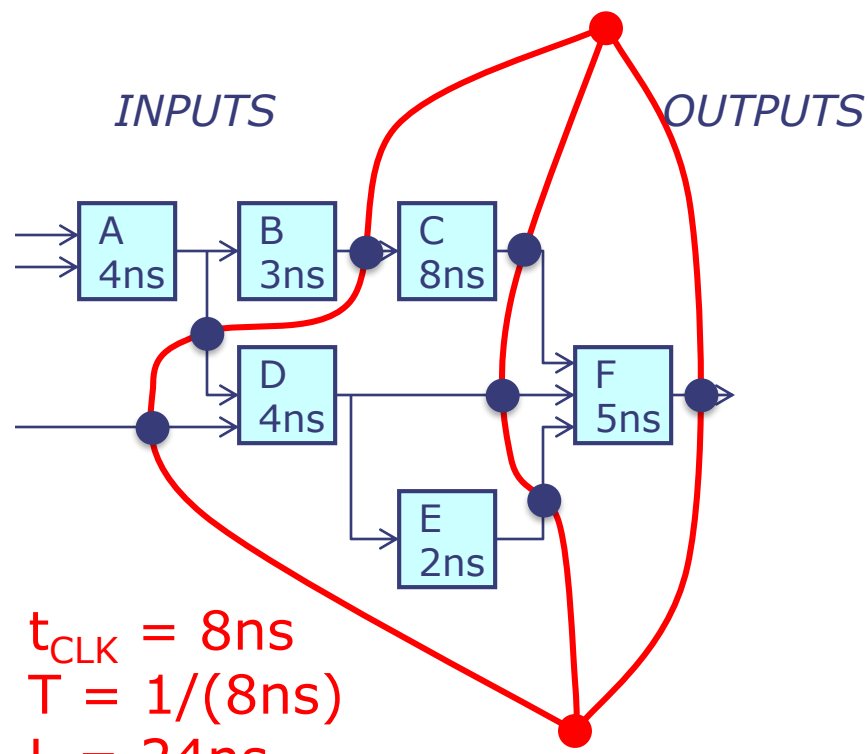
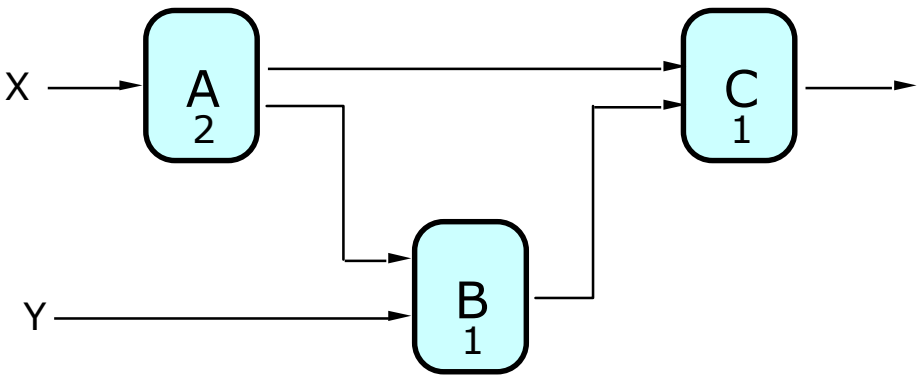
Strategy:

Focus your attention on placing pipelining registers around the slowest circuit elements (*bottlenecks*).



t_{CLK} = 8ns
T = 1/(8ns)
L = 24ns

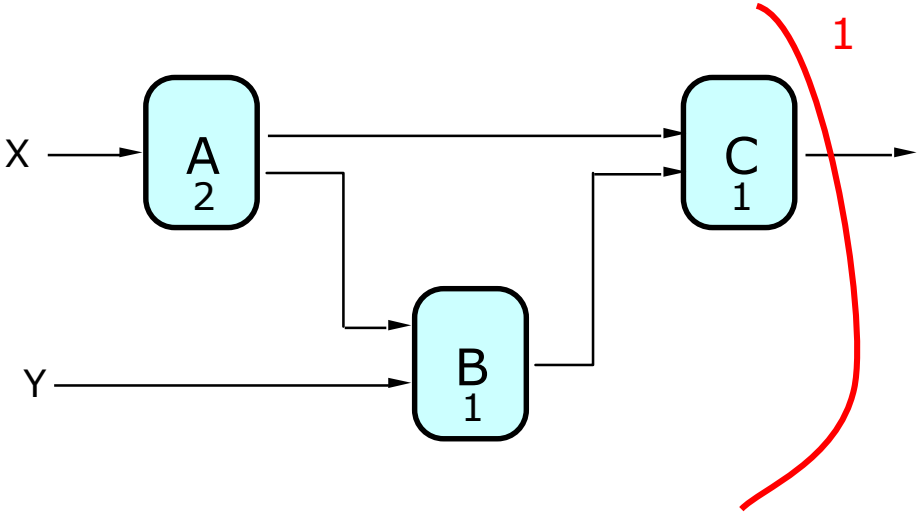
Pipeline Example



OBSERVATIONS:

	LATENCY	THROUGHPUT
0-pipe:	4	1/4
1-pipe:		
2-pipe:		
3-pipe:		

Pipeline Example

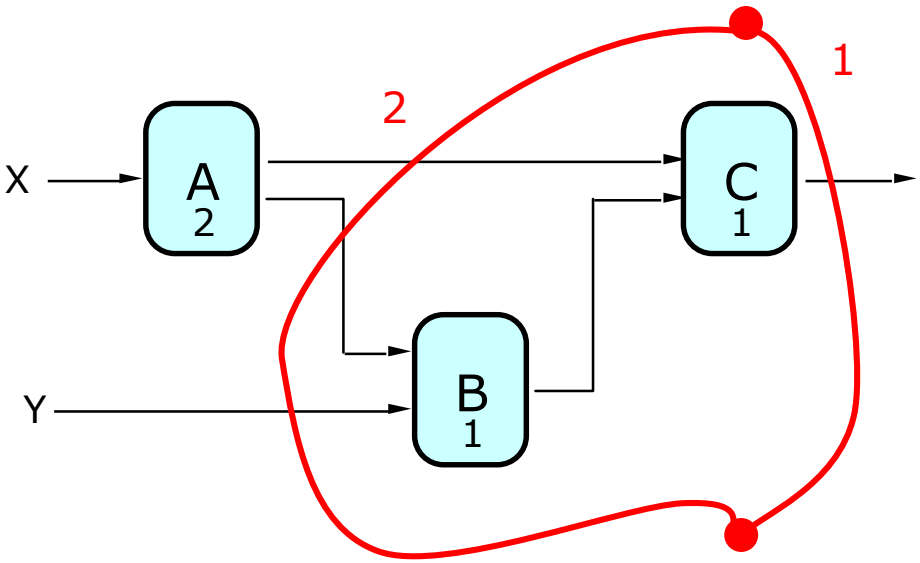


	LATENCY	THROUGHPUT
0-pipe:	4	1/4
1-pipe:	4	1/4
2-pipe:		
3-pipe:		

OBSERVATIONS:

- 1-pipeline improves neither L nor T.

Pipeline Example

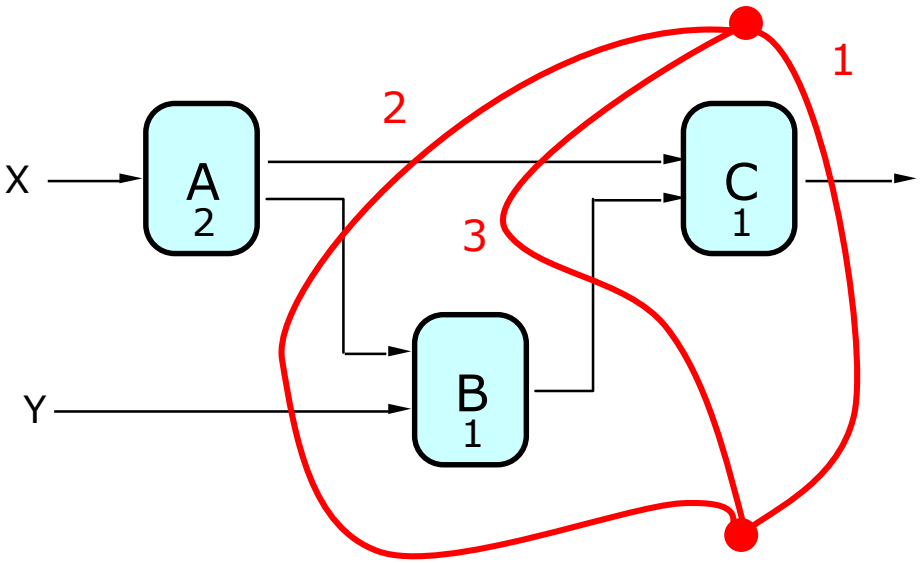


	LATENCY	THROUGHPUT
0-pipe:	4	1/4
1-pipe:	4	1/4
2-pipe:	4	1/2
3-pipe:		

OBSERVATIONS:

- 1-pipeline improves neither L nor T.
- T improved by breaking long combinational paths, allowing faster clock.

Pipeline Example

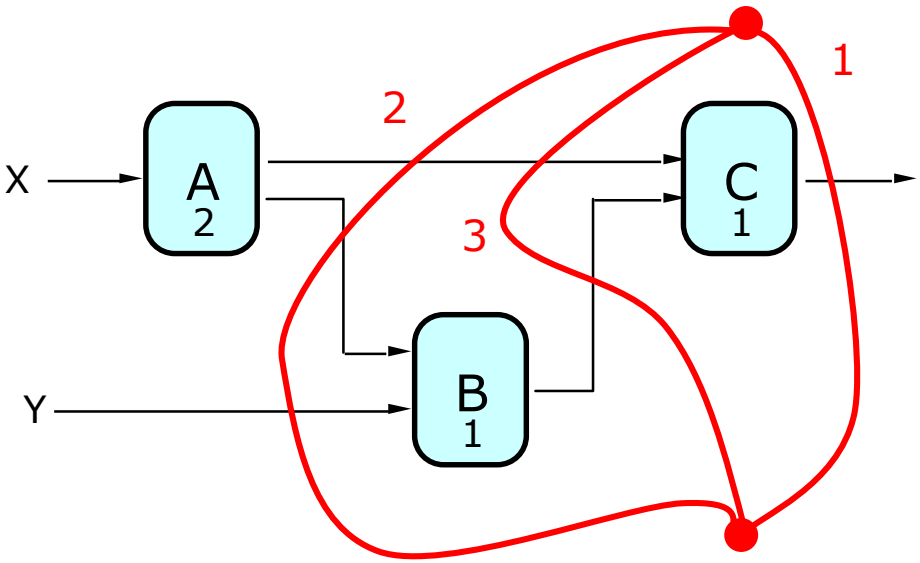


	LATENCY	THROUGHPUT
0-pipe:	4	1/4
1-pipe:	4	1/4
2-pipe:	4	1/2
3-pipe:	6	1/2

OBSERVATIONS:

- 1-pipeline improves neither L nor T.
- T improved by breaking long combinational paths, allowing faster clock.
- Too many stages cost L, don't improve T.

Pipeline Example



	LATENCY	THROUGHPUT
0-pipe:	4	1/4
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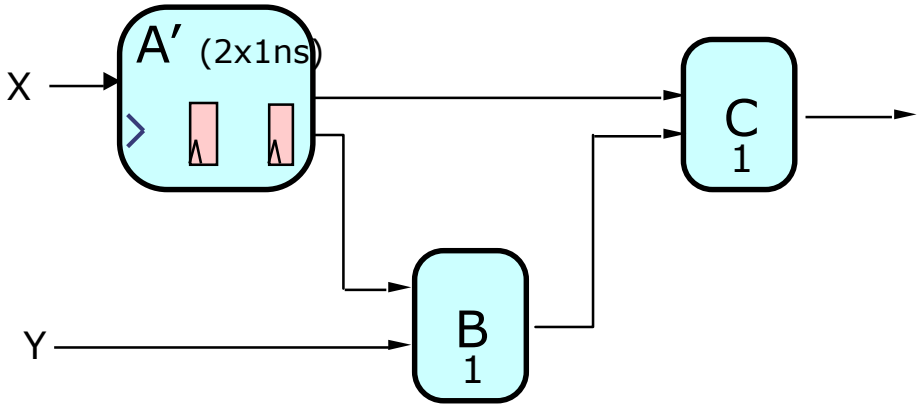
OBSERVATIONS:

- 1-pipeline improves neither L nor T.
- T improved by breaking long combinational paths, allowing faster clock.
- Too many stages cost L, don't improve T.
- Back-to-back registers are sometimes needed to keep pipeline well-formed.

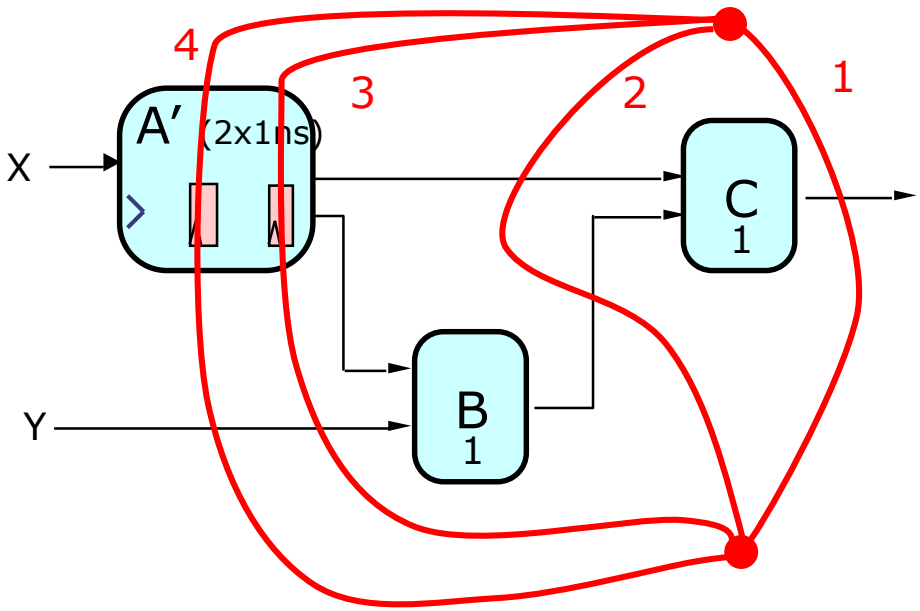
Pipelined Components



Pipelined systems can be hierarchical:

- Replacing a slow combinational component with a k-pipe version may let us decrease the clock period

Pipelined Components



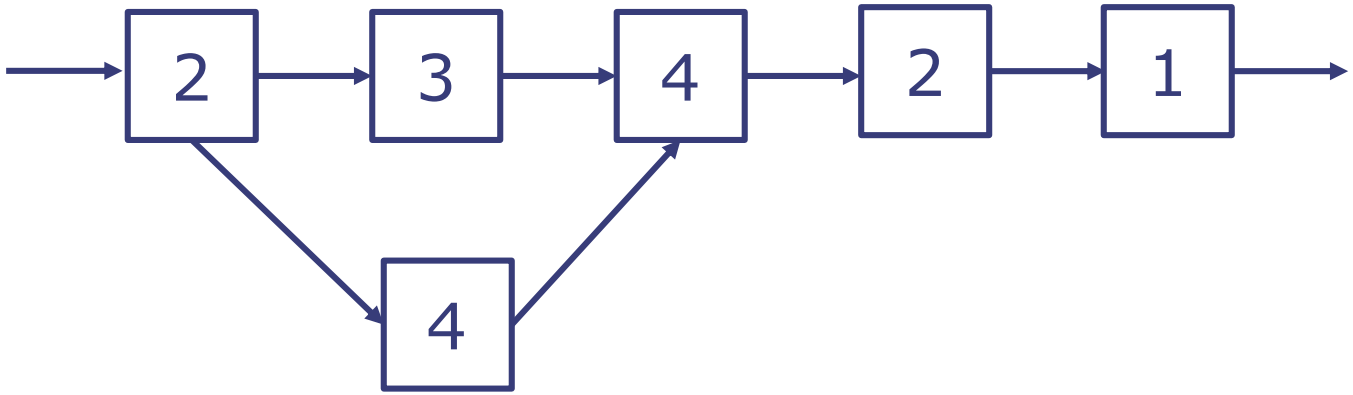
4-stage pipeline, throughput=1

Pipelined systems can be hierarchical:

- Replacing a slow combinational component with a k-pipe version may let us decrease the clock period
- Must account for new pipeline stages in our plan

Sample Pipelining Problem

- Pipeline the following circuit for maximum throughput while minimizing latency. The number in each module is the module's latency.



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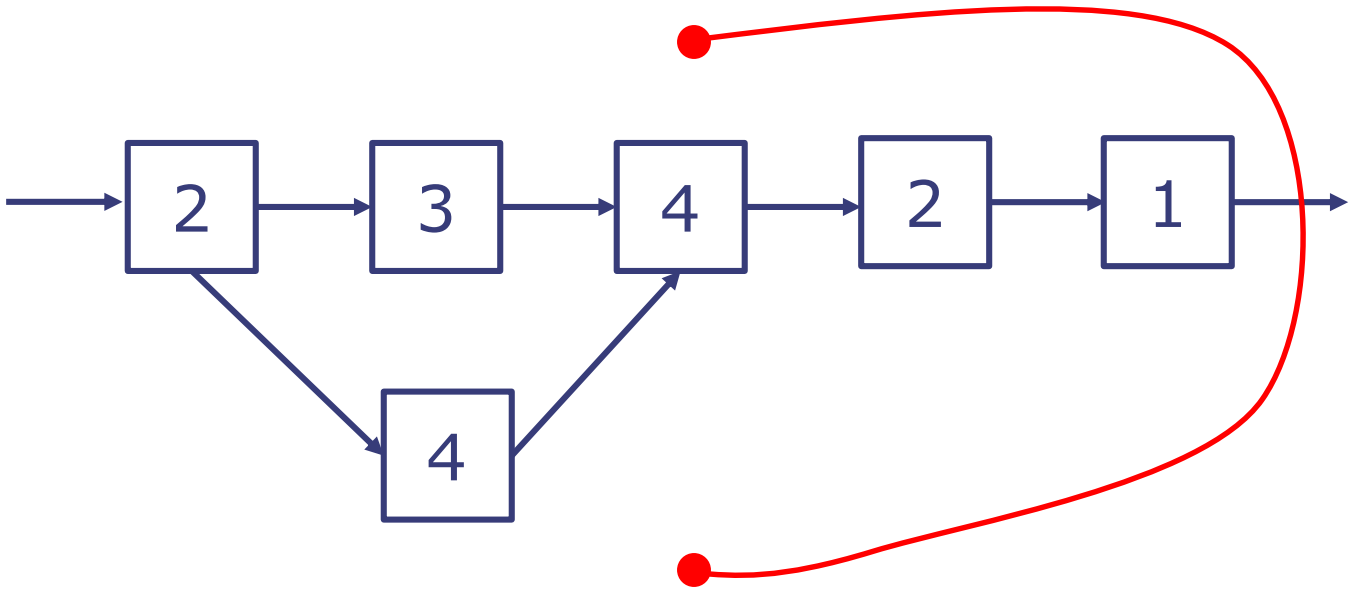

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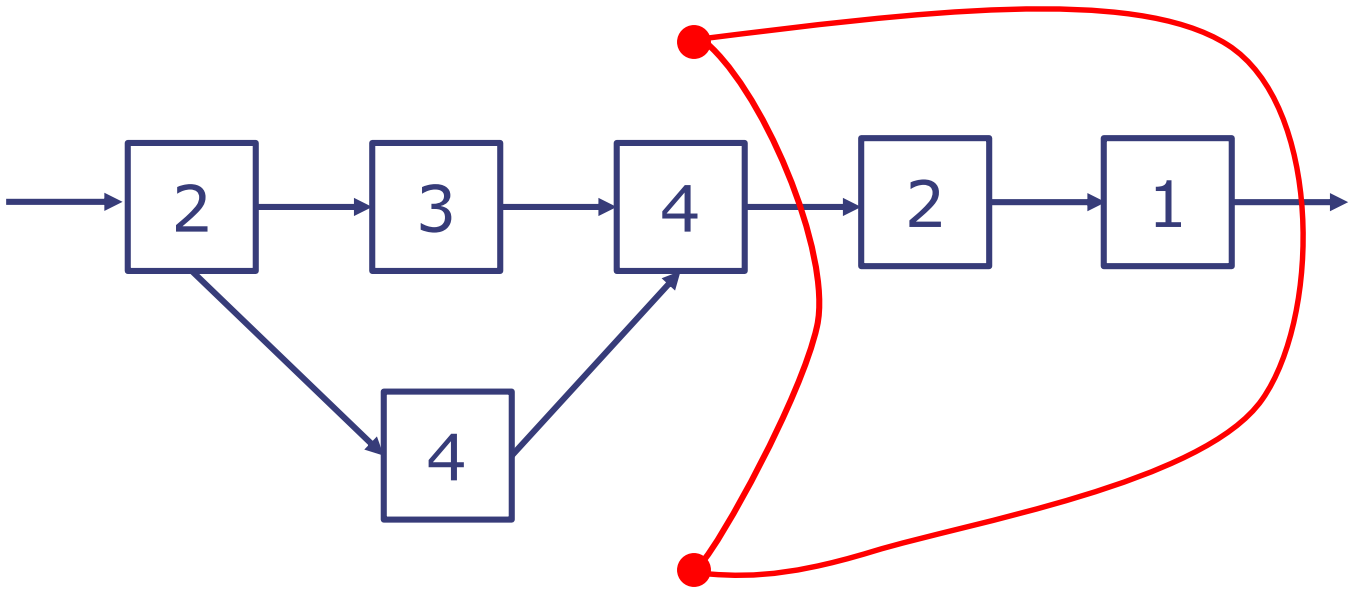

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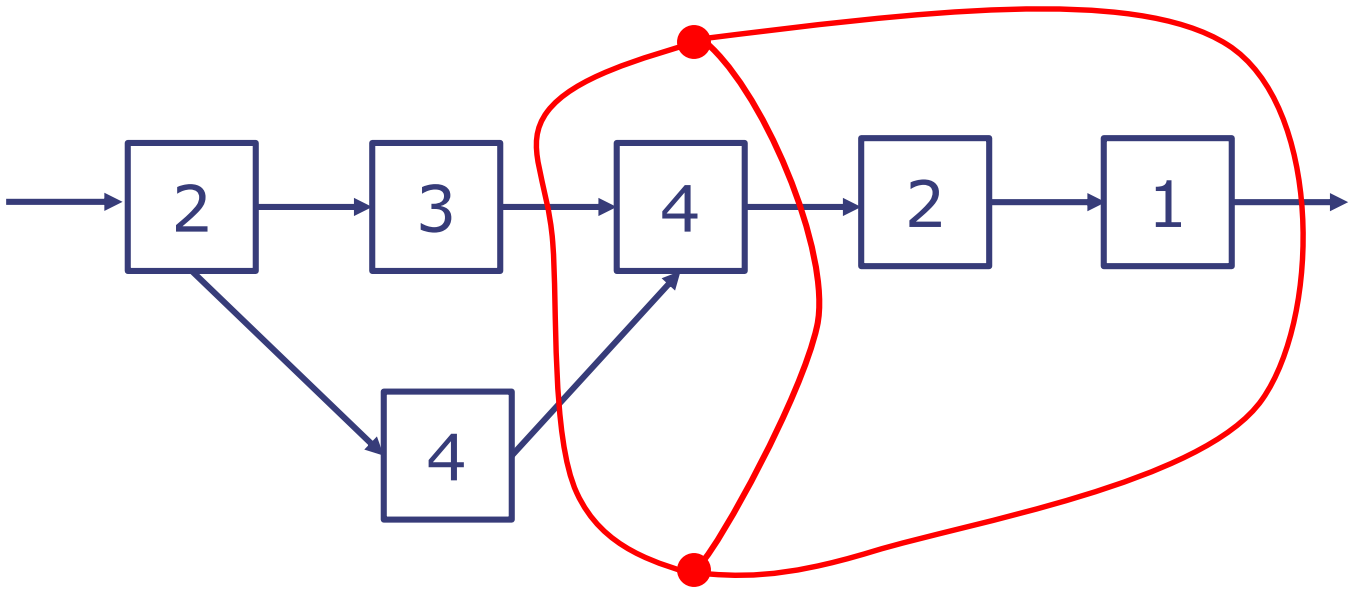

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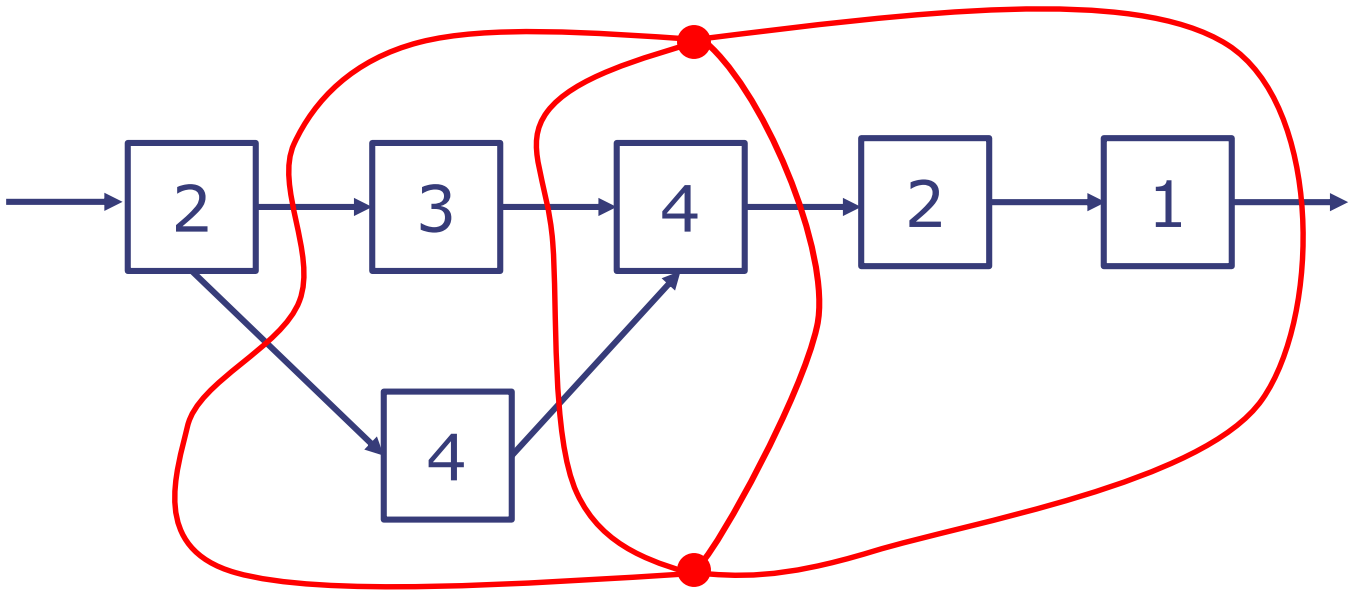

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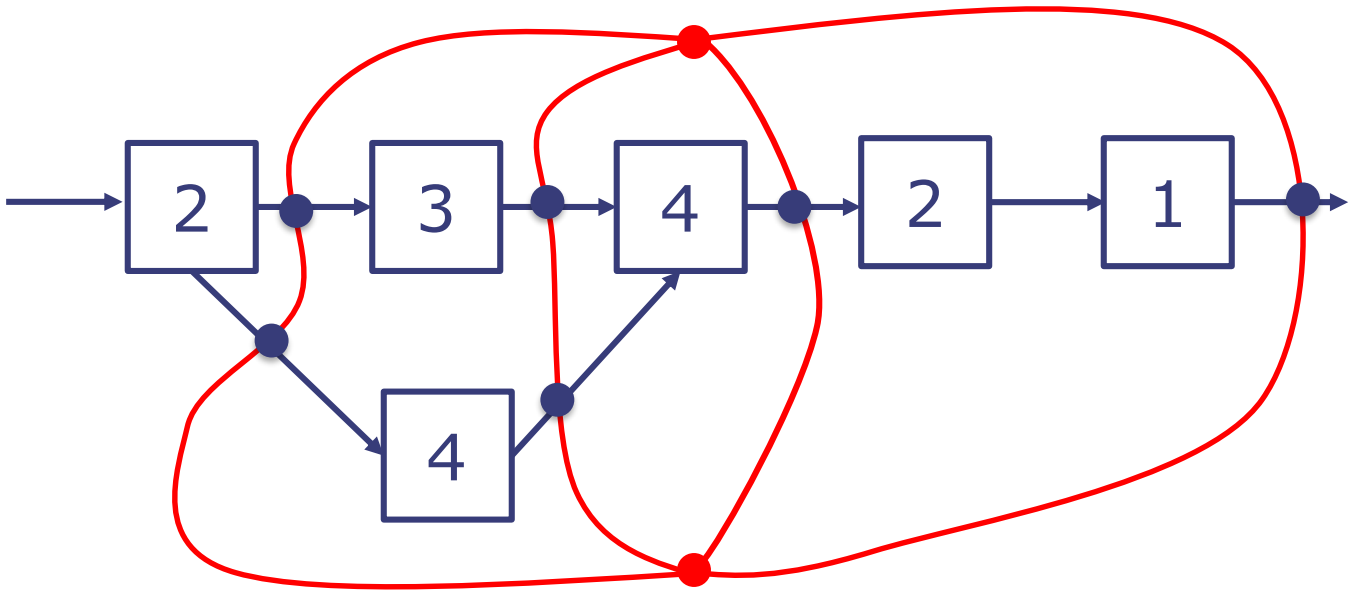

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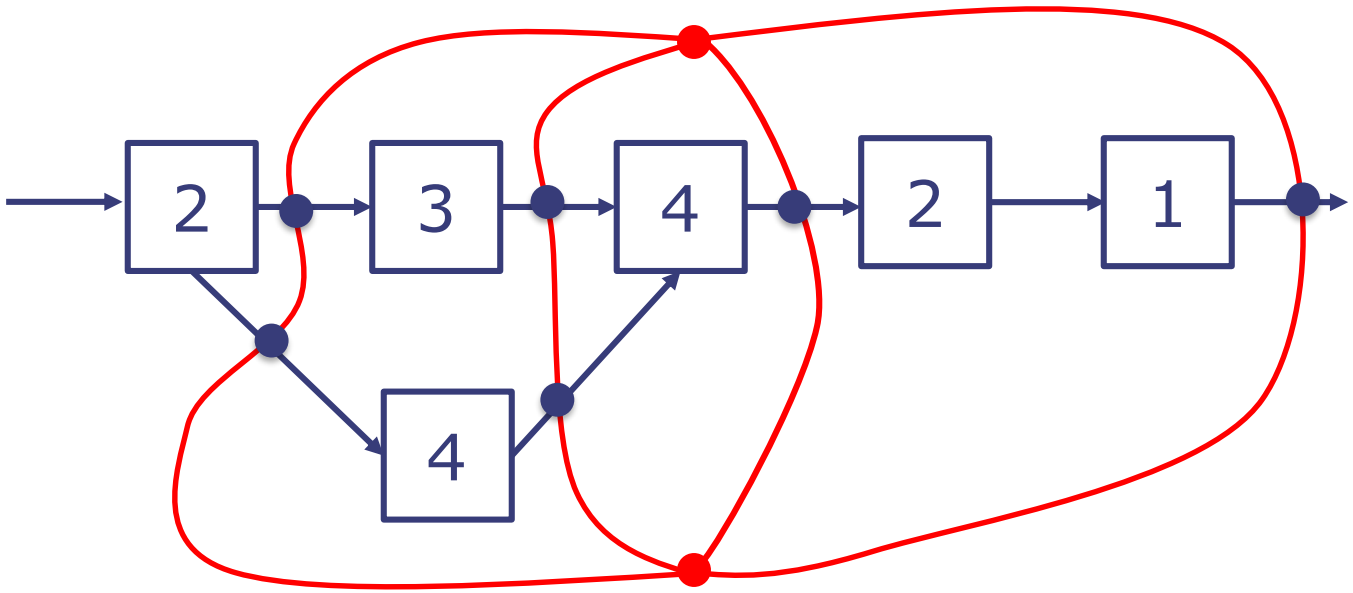

- What is the latency and throughput of your pipelined circuit?

Sample Pipelining Problem

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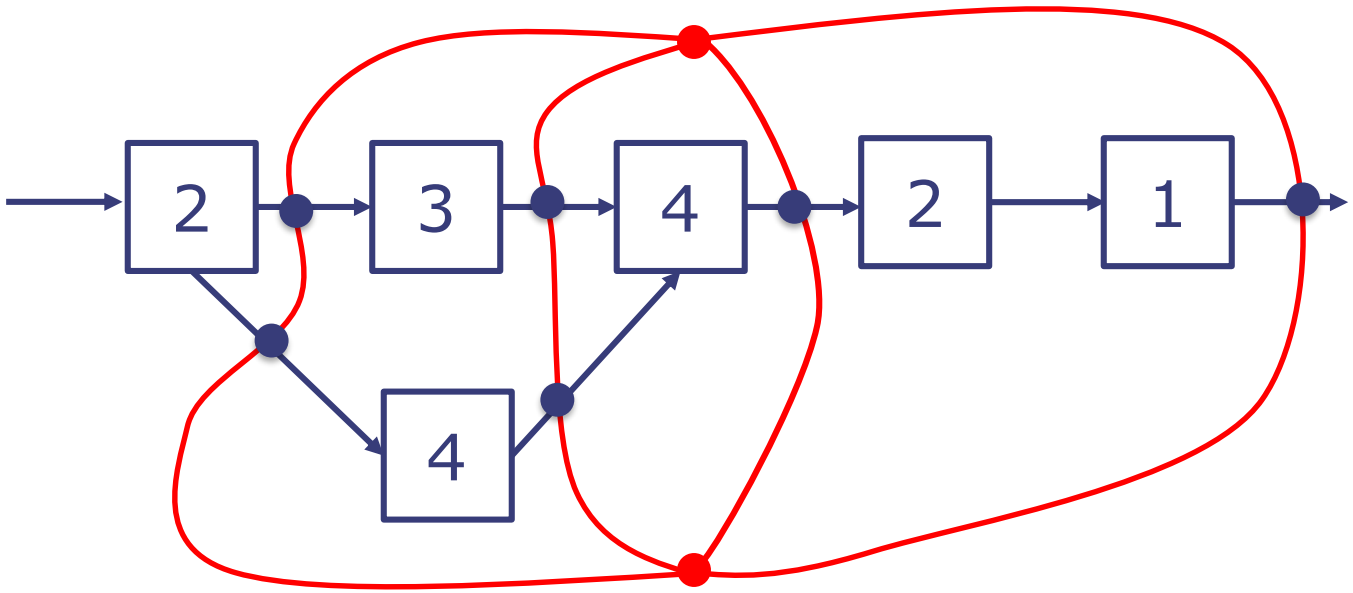

- What is the latency and throughput of your pipelined circuit?

$t_{CLK} = 4$
$T = 1/(4)$
$L = 4*4 = 16$

Design Tradeoffs Introduction:

Multiplier Case Study

Multiplication by repeated addition

```
b Multiplicand   1101   (13)
a Multiplier   * 1011   (11)

tp                0000
m0          +     1101
            ----------------
tp               01101
m1          +    1101
            ----------------
tp              100111
m2          +   0000
            ----------------
tp             0100111
m3          +  1101
            ----------------
tp            10001111   (143)
```

At each step we add either b (1101) or 0 to the result depending upon a bit in the multiplier

Multiplication by repeated addition

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At each step we add either b (1101) or 0 to the result depending upon a bit in the multiplier

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We also shift the result by one position at every step

Multiplication by repeated addition

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Note the first addition is unnecessary because it simply yields m0

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Also note that these are unsigned binary numbers.

Multiplication by repeated addition
Combinational circuit

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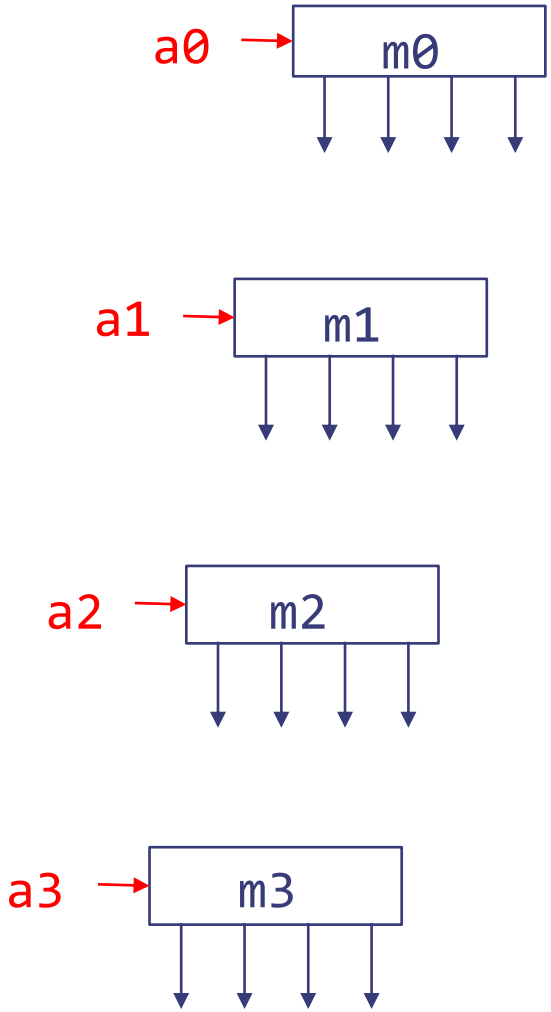


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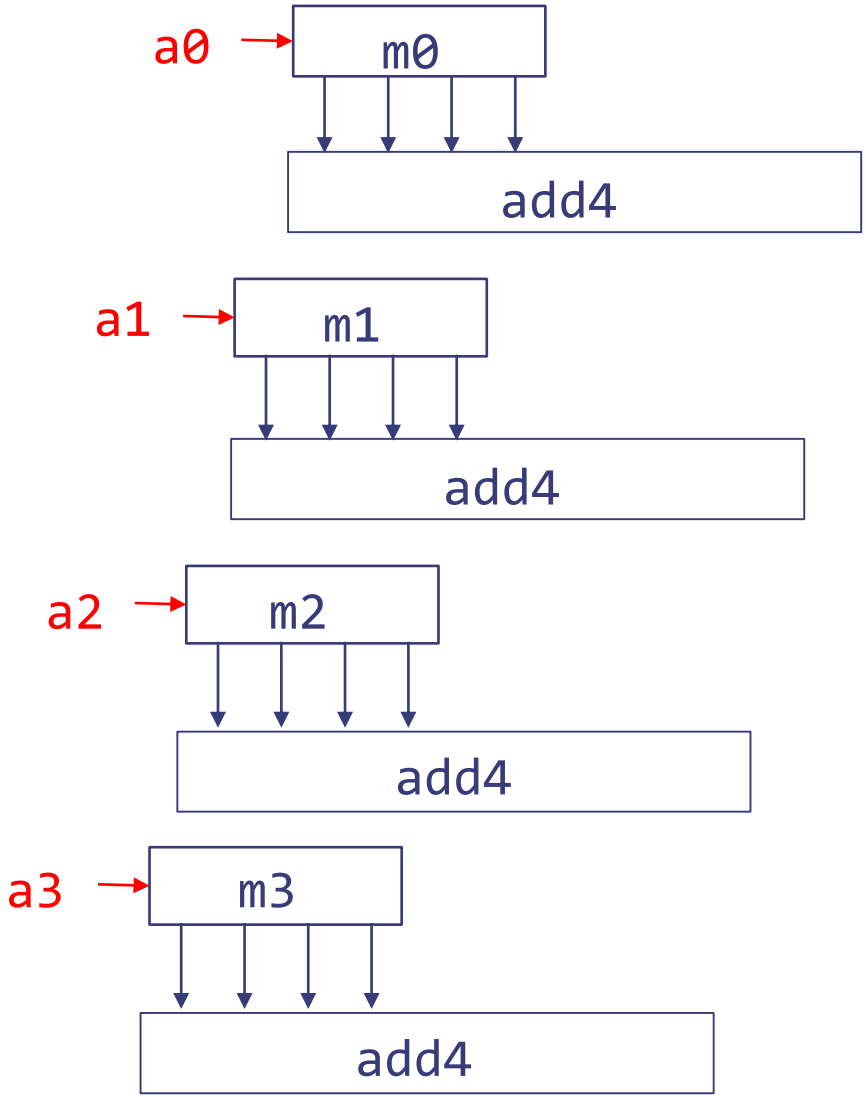


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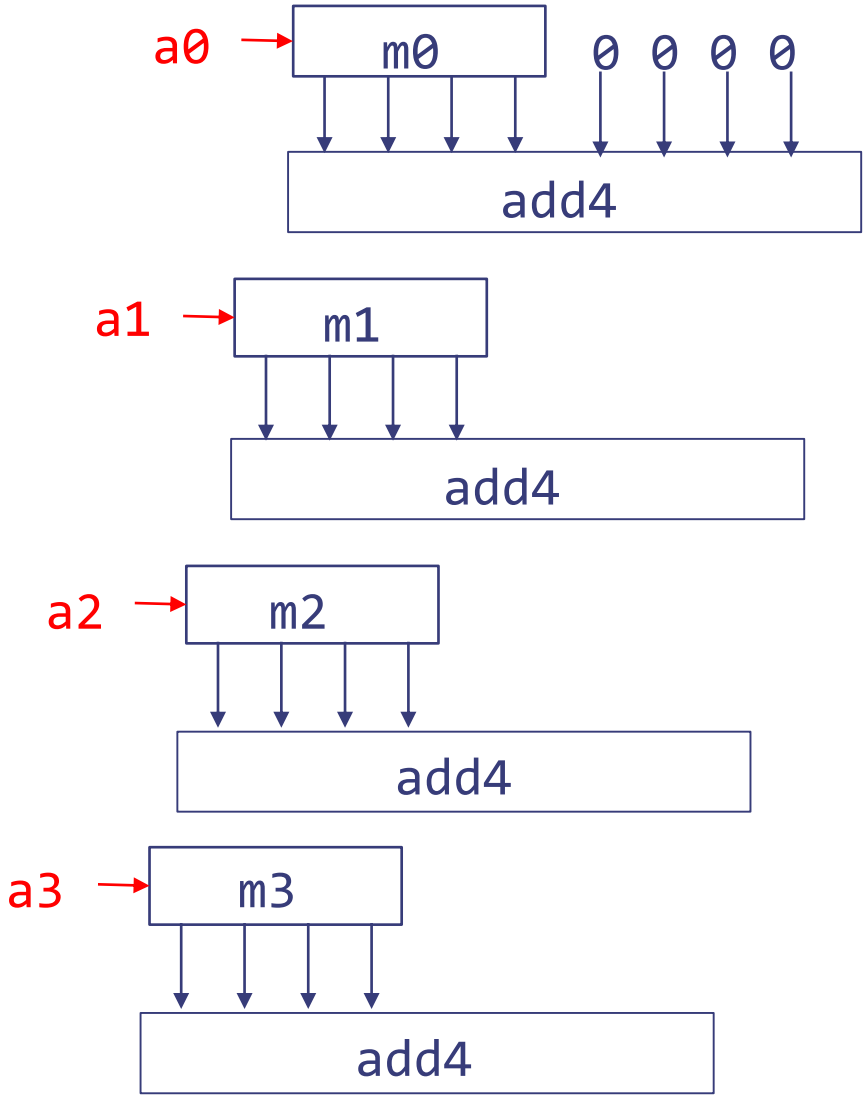


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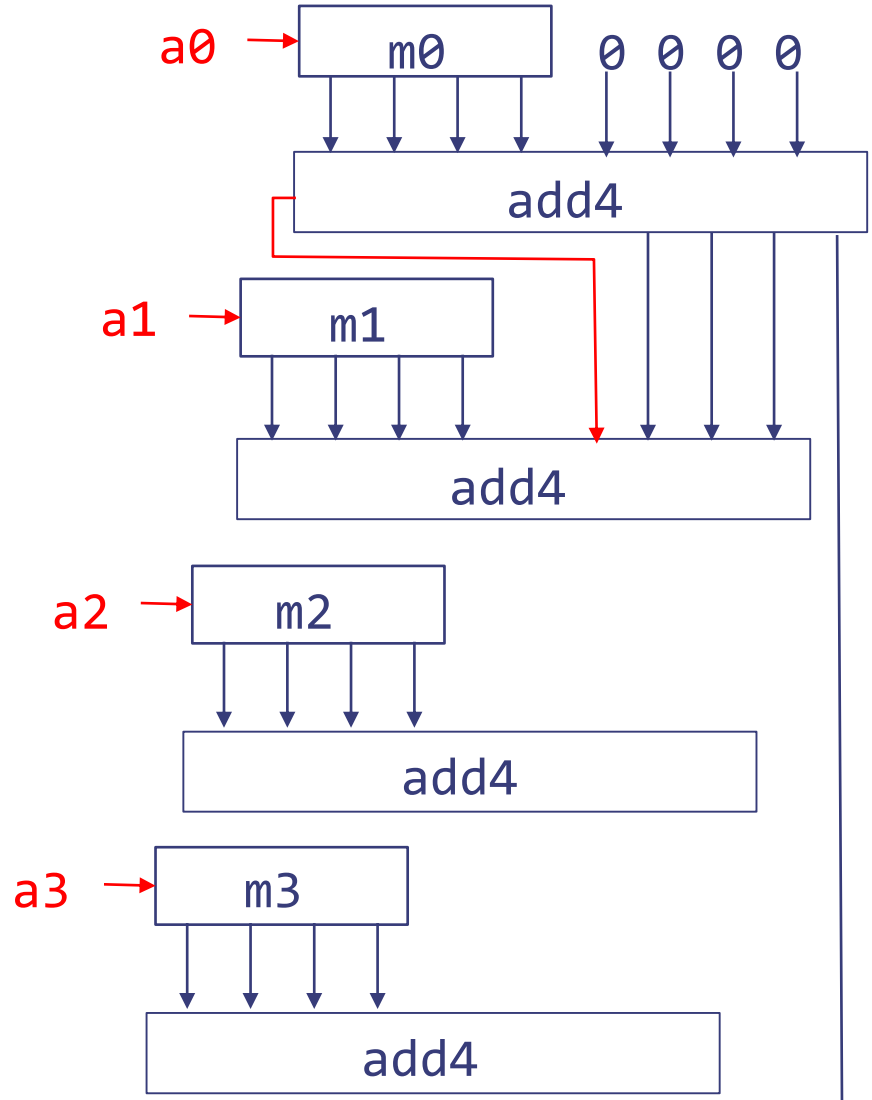


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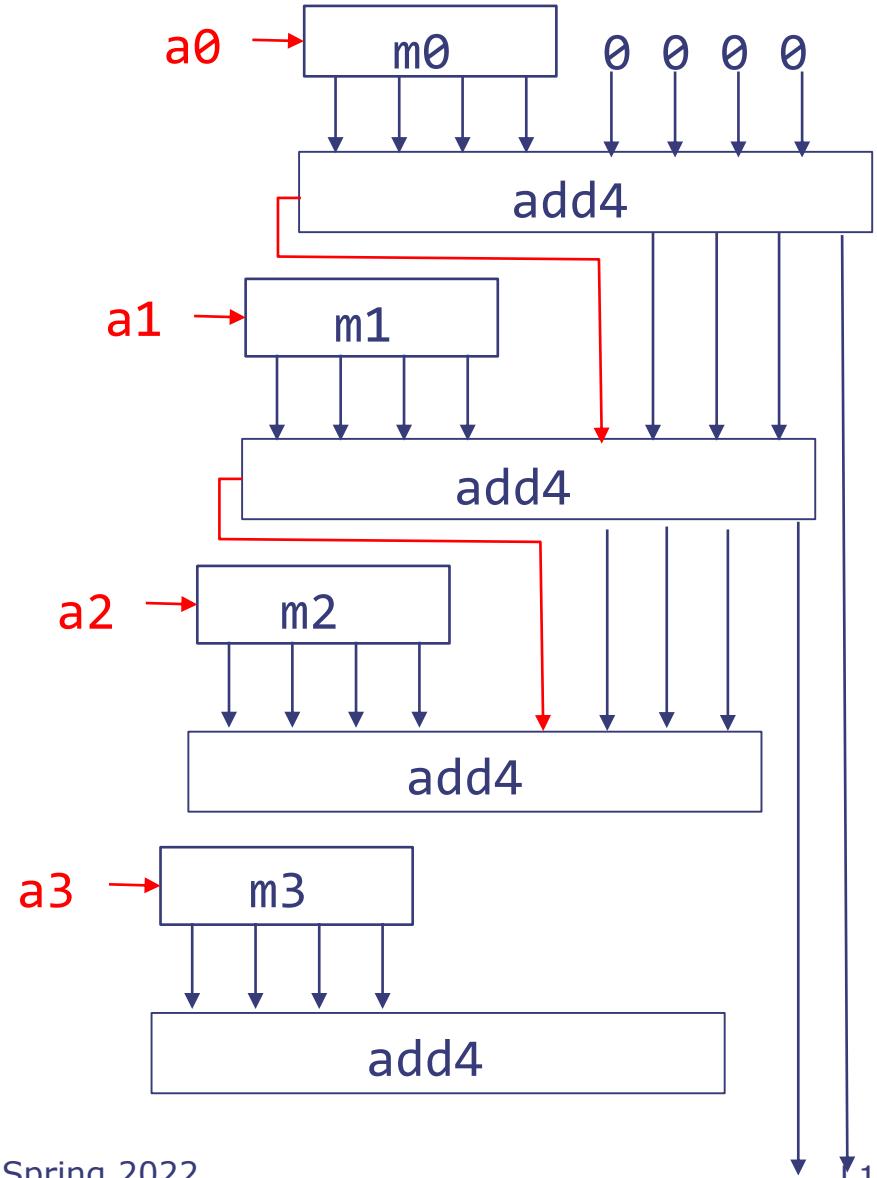


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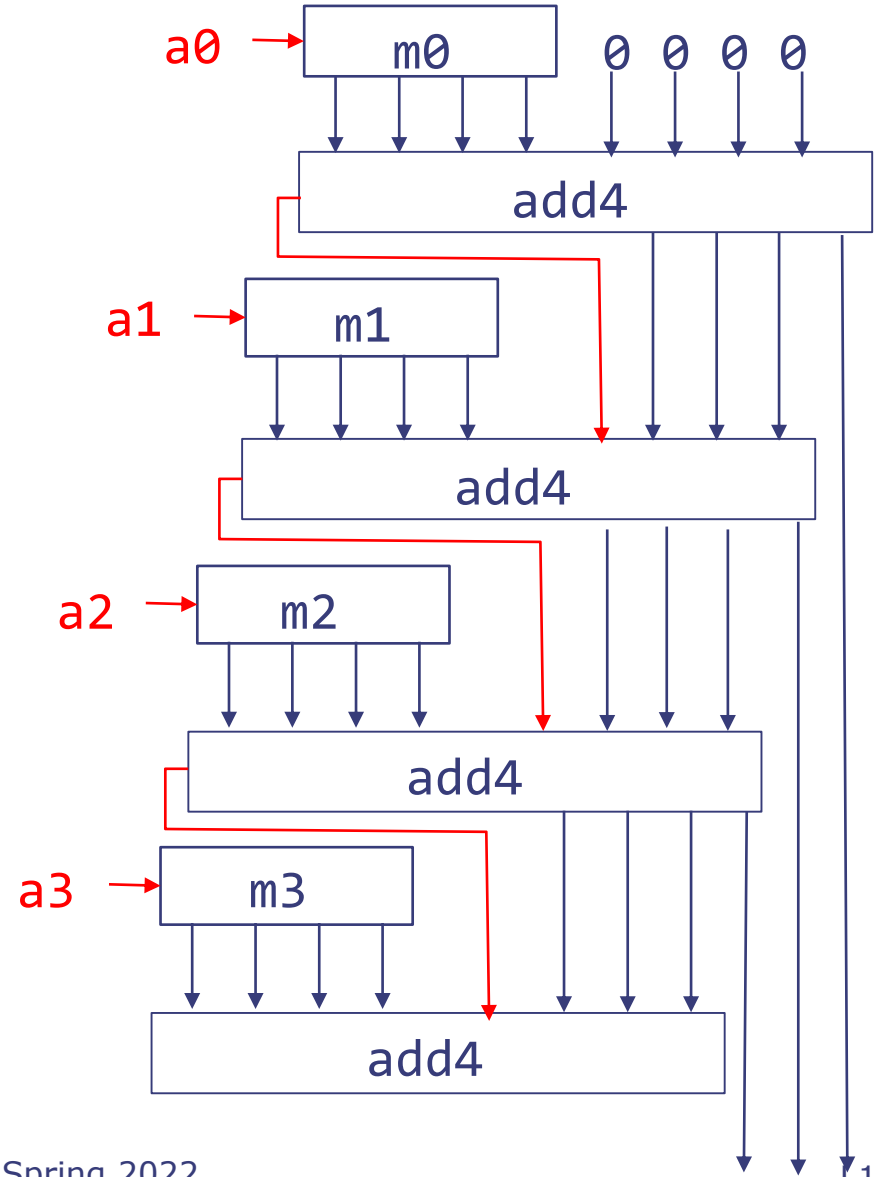

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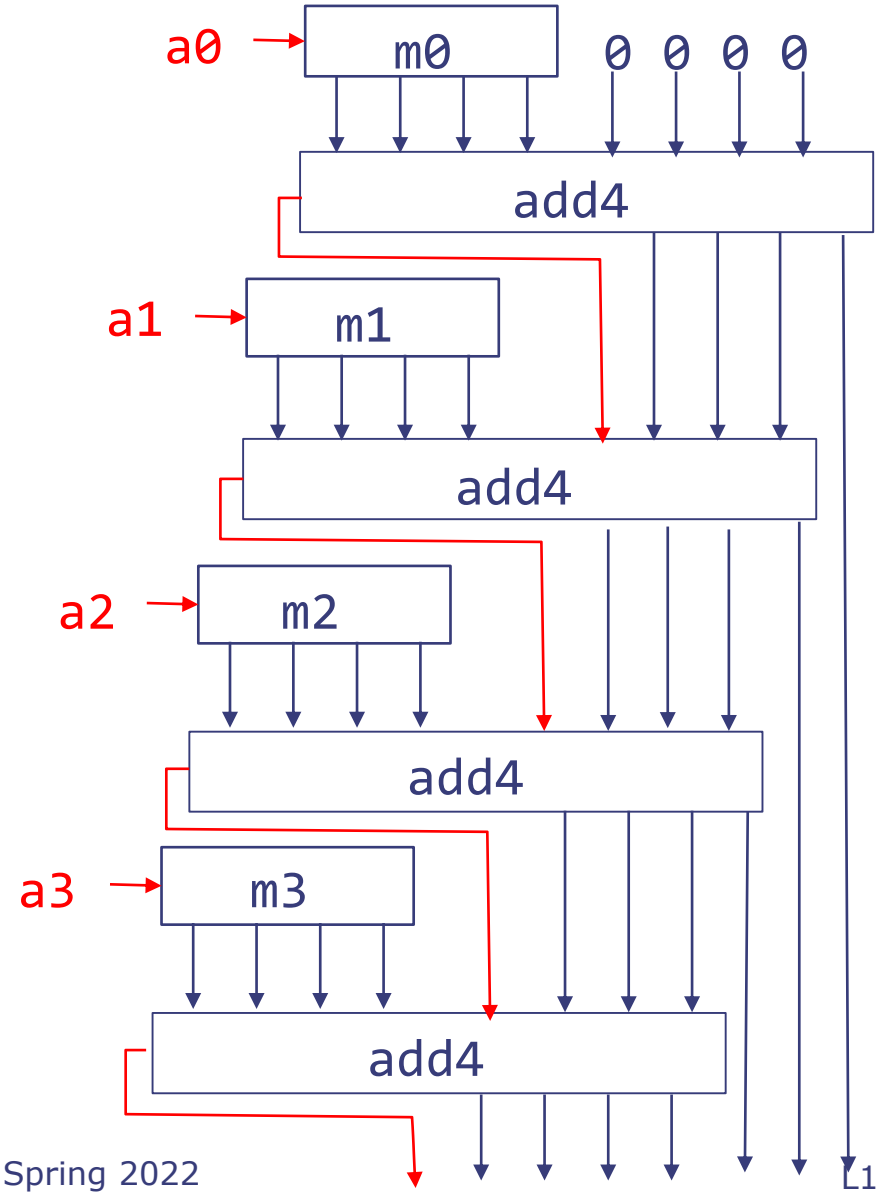


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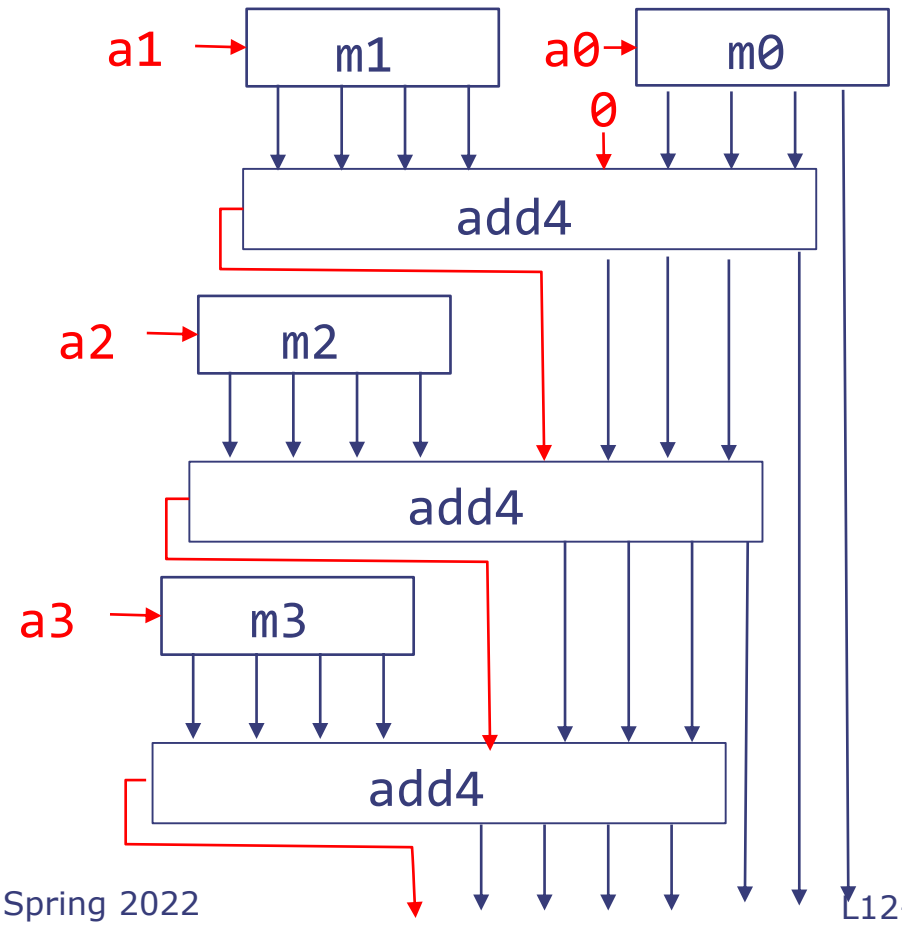

Implementation of mi

$$
\begin{array}{rrrrrrr}
 & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & \times & A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & B_3A_0 & B_2A_0 & B_1A_0 & B_0A_0 \\
 & & & B_3A_1 & B_2A_1 & B_1A_1 & B_0A_1 & \\
 & & B_3A_2 & B_2A_2 & B_1A_2 & B_0A_2 & & \\
+ & B_3A_3 & B_2A_3 & B_1A_3 & B_0A_3 & & & \\
\hline
\end{array}
$$

Implementation of mi

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 & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & \times & A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & B_3A_0 & B_2A_0 & B_1A_0 & B_0A_0 \\
 & & B_3A_1 & & B_2A_1 & B_1A_1 & B_0A_1 & \\
 & B_3A_2 & B_2A_2 & & B_1A_2 & B_0A_2 & & \\
+ & B_3A_3 & B_2A_3 & & B_1A_3 & B_0A_3 & & \\
\hline
\end{array}
$$

m0
m1
m2
m3

Implementation of mi

The "Binary" Multiplication Table

*	0	1
0	0	0
1	0	1

```
mi = (a[i]==0)? 0 : b;
```

$$
\begin{array}{rrrrrrr}
 & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & \times & A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & B_3A_0 & B_2A_0 & B_1A_0 & B_0A_0 \\
 & & B_3A_1 & & B_2A_1 & B_1A_1 & B_0A_1 & \\
 & B_3A_2 & B_2A_2 & & B_1A_2 & B_0A_2 & & \\
+ & B_3A_3 & B_2A_3 & & B_1A_3 & B_0A_3 & & \\
\hline
\end{array}
$$

m0
m1
m2
m3

Implementation of mi

The "Binary" Multiplication Table

*	0	1
0	0	0
1	0	1

= AND

```
mi = (a[i]==0)? 0 : b;
```

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\begin{array}{rrrrrrr}
 & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & & \times\ A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & B_3A_0 & B_2A_0 & B_1A_0 & B_0A_0 \\
 & & & B_3A_1 & B_2A_1 & B_1A_1 & B_0A_1 & \\
 & & B_3A_2 & B_2A_2 & B_1A_2 & B_0A_2 & & \\
+ & B_3A_3 & B_2A_3 & B_1A_3 & B_0A_3 & & & \\
\hline
\end{array}
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m0
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Implementation of mi

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 & & & & \times & A_3 & A_2 & A_1 & A_0 \\
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 & + & B_3A_3 & B_2A_3 & B_1A_3 & B_0A_3 & & & \\
\hline
\end{array}
$$

BA_i called a "partial product" → B_3A_0 B_2A_0 B_1A_0 B_0A_0

m0
m1
m2
m3

Implementation of mi

The "Binary" Multiplication Table

*	0	1
0	0	0
1	0	1

= AND

```
mi = (a[i]==0)? 0 : b;
```

$$
\begin{array}{rrrrrrrr}
 & & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & & \times & A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & & B_3A_0 & B_2A_0 & B_1A_0 & B_0A_0 \\
 & & & & B_3A_1 & B_2A_1 & B_1A_1 & B_0A_1 & \\
 & & & B_3A_2 & B_2A_2 & B_1A_2 & B_0A_2 & & \\
 & + & B_3A_3 & B_2A_3 & B_1A_3 & B_0A_3 & & & \\
\hline
\end{array}
$$

BA_i called a "partial product" → B_3A_0 B_2A_0 B_1A_0 B_0A_0

m0
m1
m2
m3

Multiplying N-digit number by M-digit number gives (N+M)-digit result

Implementation of mi

The "Binary" Multiplication Table

*	0	1
0	0	0
1	0	1

= AND

```
mi = (a[i]==0)? 0 : b;
```

$$
\begin{array}{rrrrrrrr}
 & & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & & \times & A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & & B_3A_0 & B_2A_0 & B_1A_0 & B_0A_0 \\
 & & & & B_3A_1 & B_2A_1 & B_1A_1 & B_0A_1 & \\
 & & & B_3A_2 & B_2A_2 & B_1A_2 & B_0A_2 & & \\
 & + & B_3A_3 & B_2A_3 & B_1A_3 & B_0A_3 & & & \\
\hline
\end{array}
$$

BA_i called a "partial product" → B_3A_0 B_2A_0 B_1A_0 B_0A_0 m0

B_3A_1 B_2A_1 B_1A_1 B_0A_1 m1

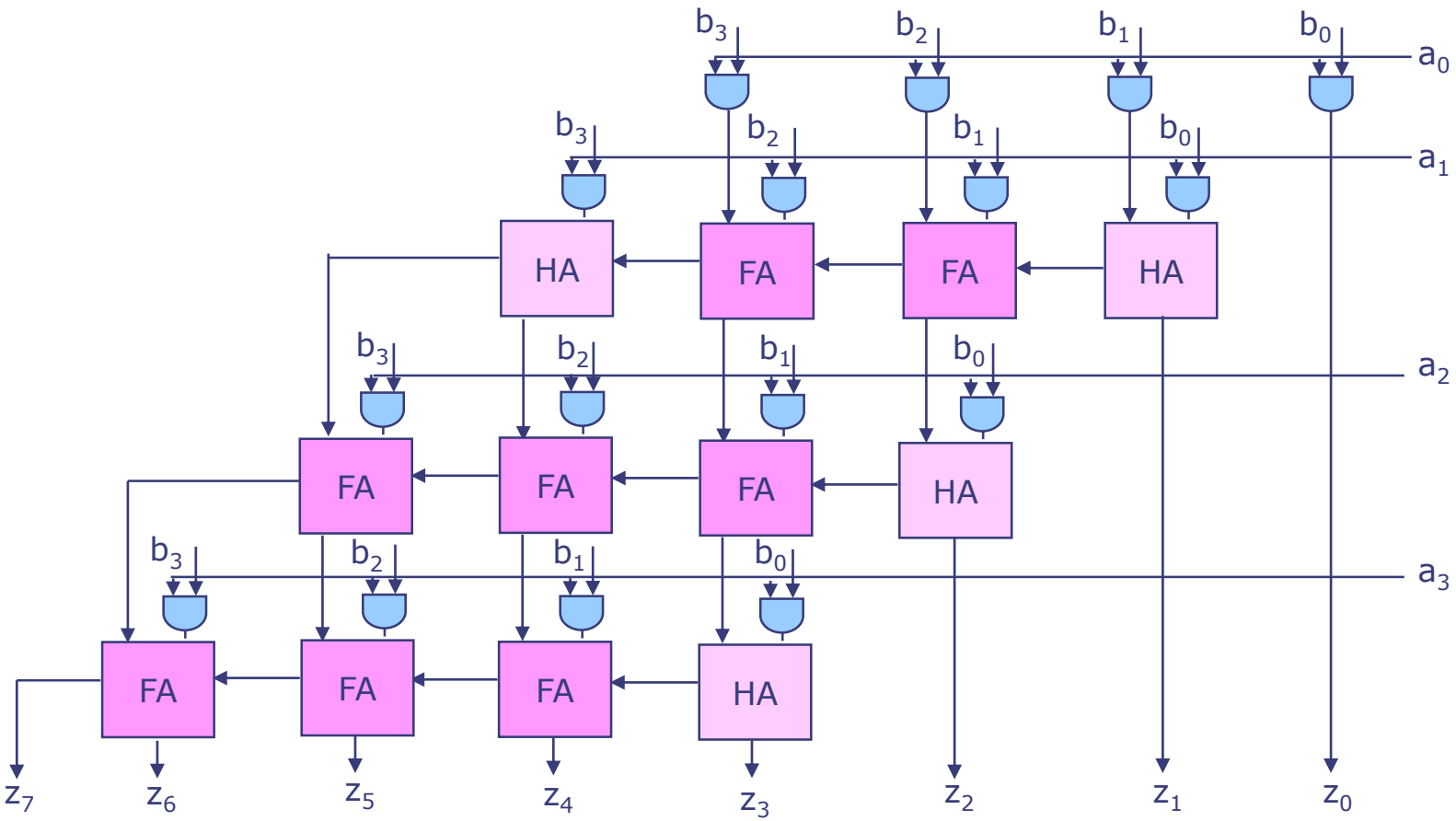
B_3A_2 B_2A_2 B_1A_2 B_0A_2 m2

$+ B_3A_3$ B_2A_3 B_1A_3 B_0A_3 m3

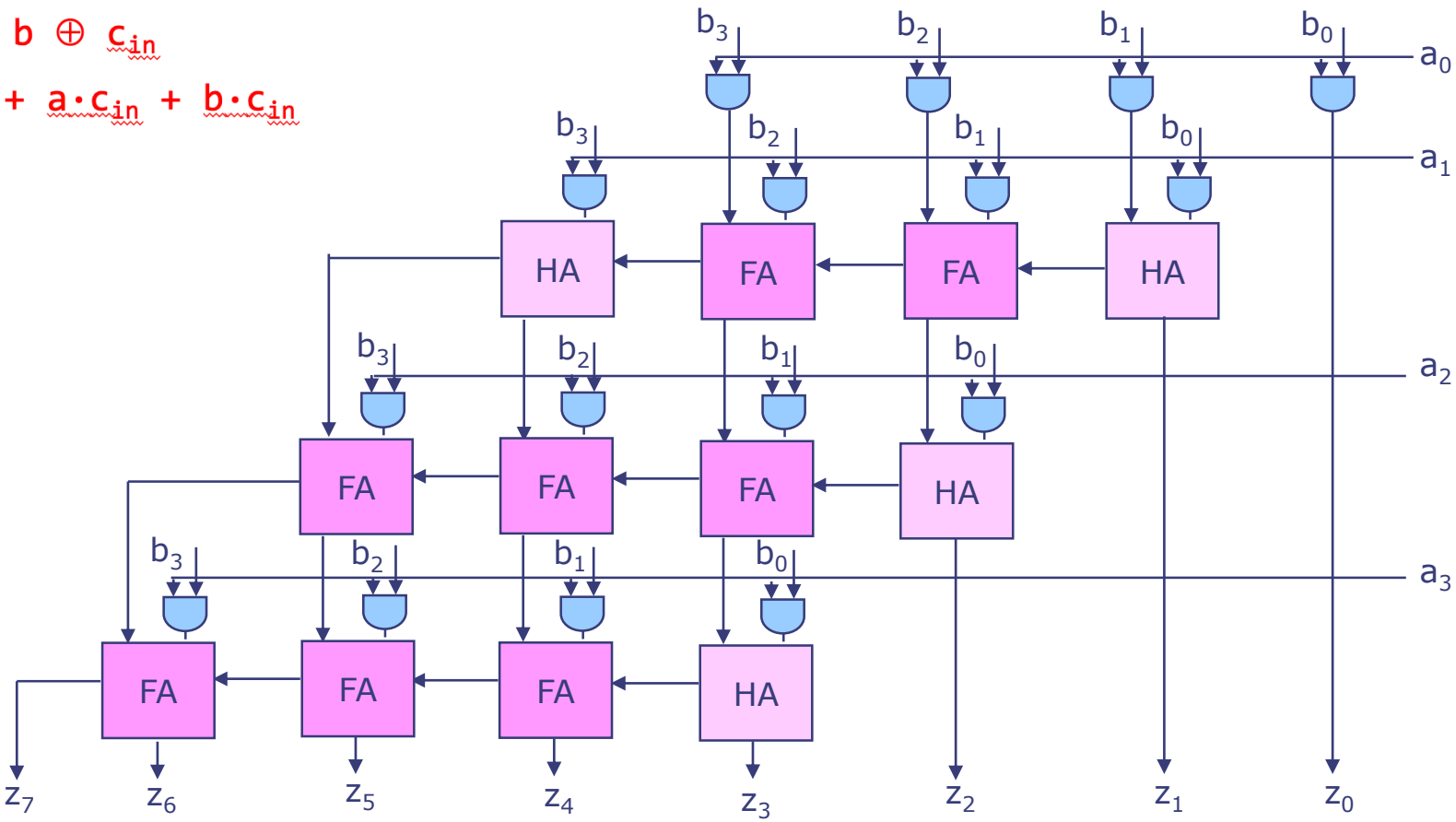
Multiplying N-digit number by M-digit number gives (N+M)-digit result

Easy part: forming partial products (bunch of AND gates)
Hard part: adding M N-bit partial products

Combinational Multiplier Redrawn



Combinational Multiplier Redrawn



Combinational Multiplier Redrawn

FA

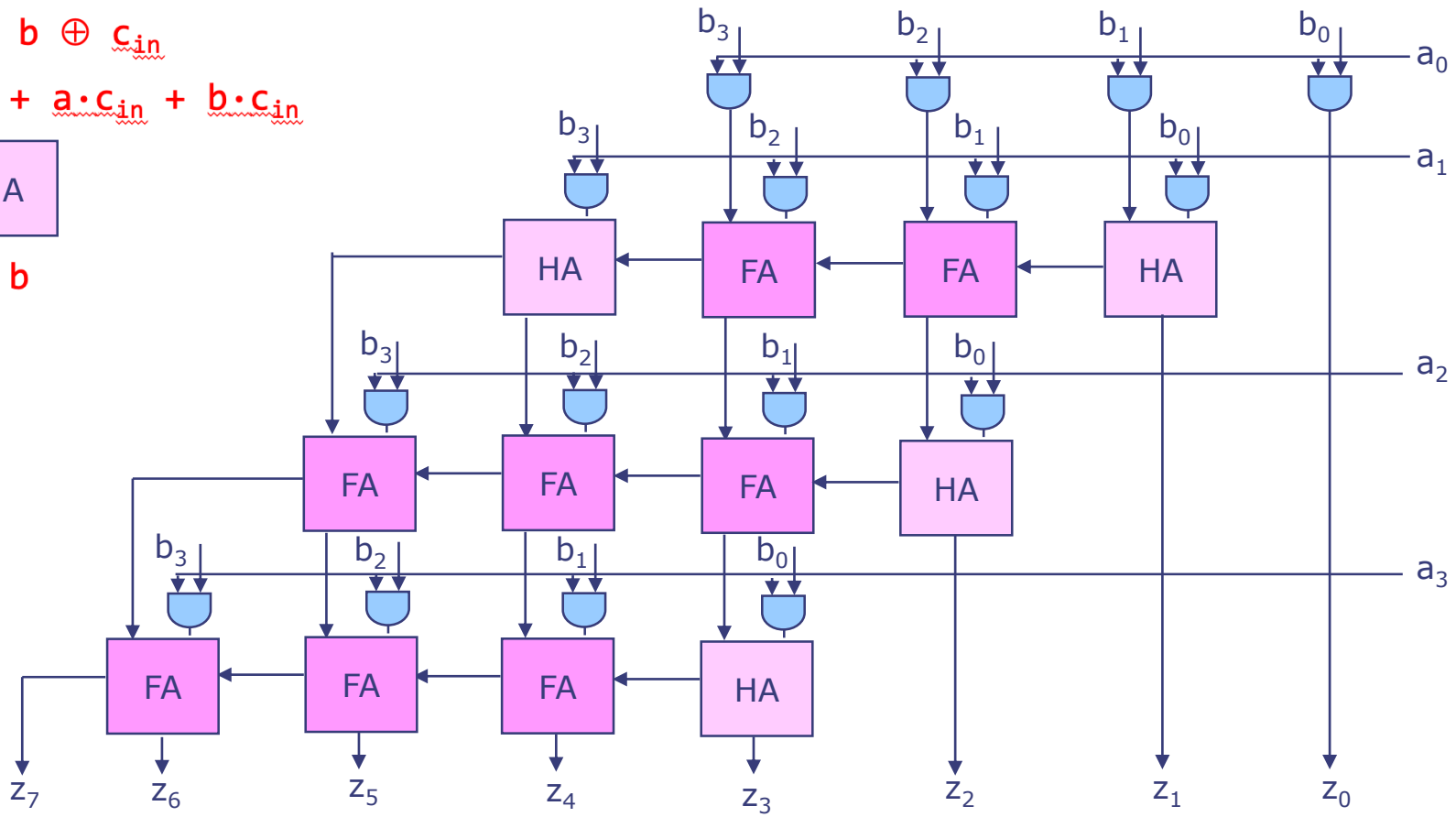
$s = a \oplus b \oplus c_{in}$

$c_{out} = a \cdot b + a \cdot c_{in} + b \cdot c_{in}$

HA

$s = a \oplus b$

$c_{out} = a \cdot b$



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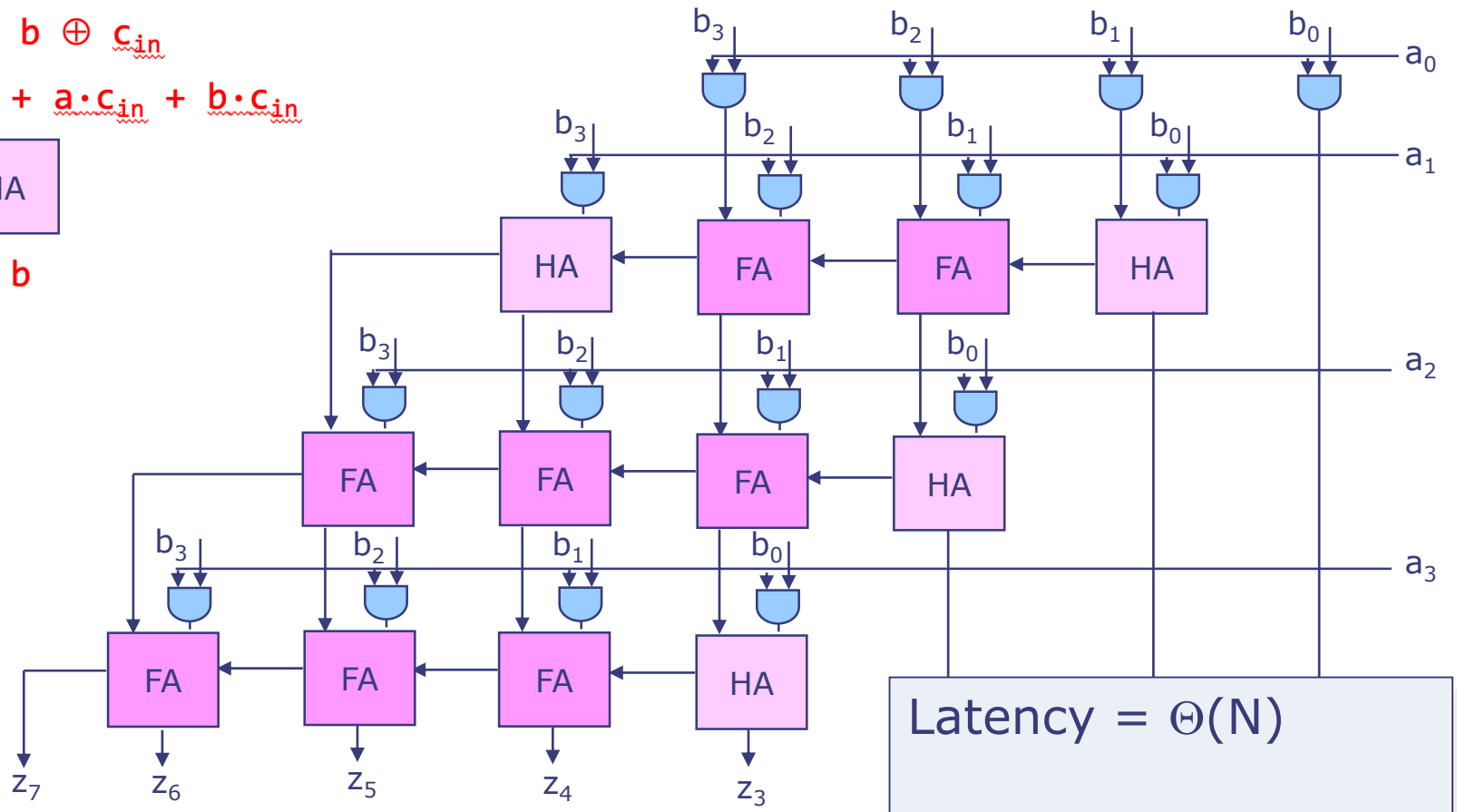

Latency = $\Theta(N)$

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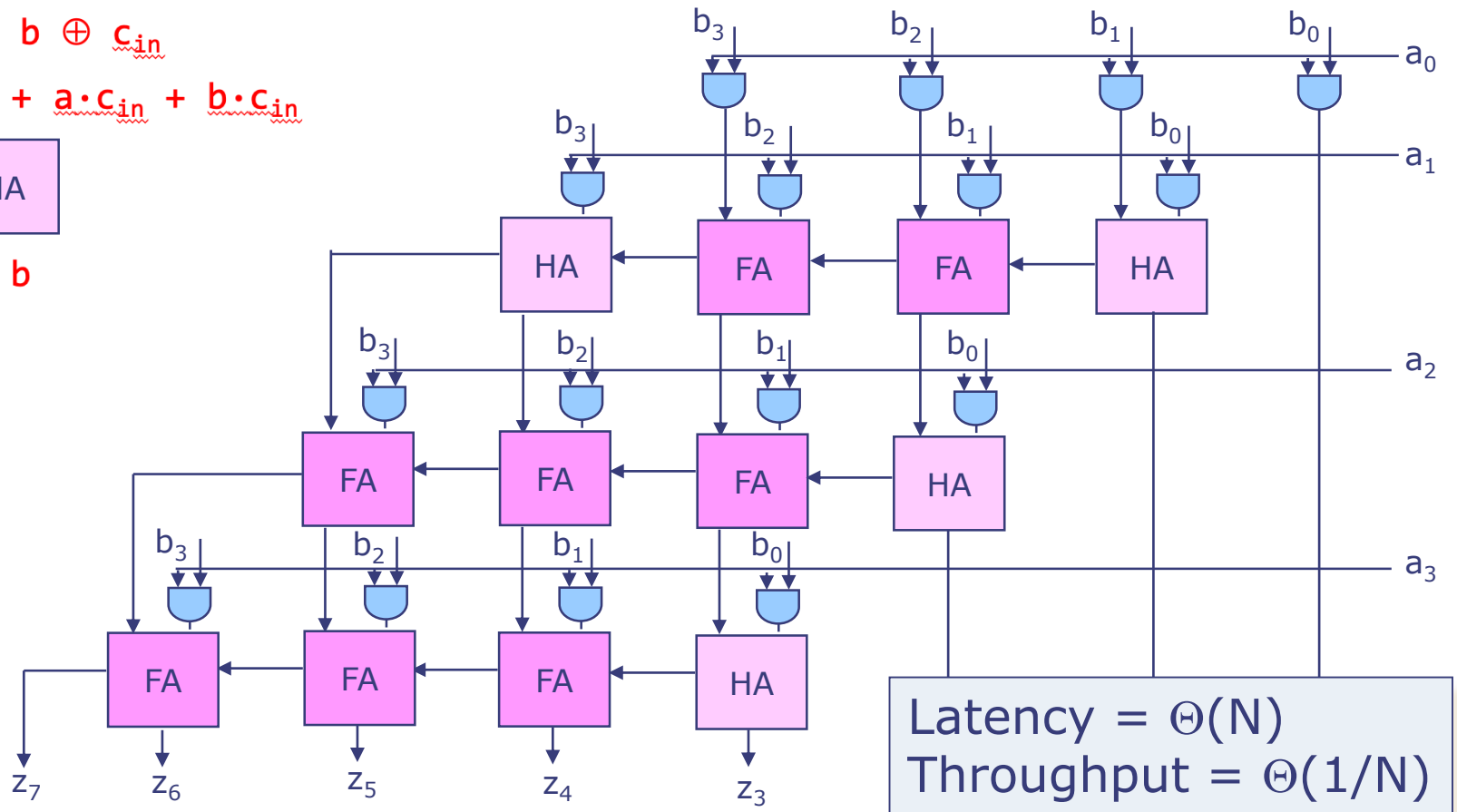

Latency = $\Theta(N)$
Throughput = $\Theta(1/N)$

Combinational Multiplier Redrawn

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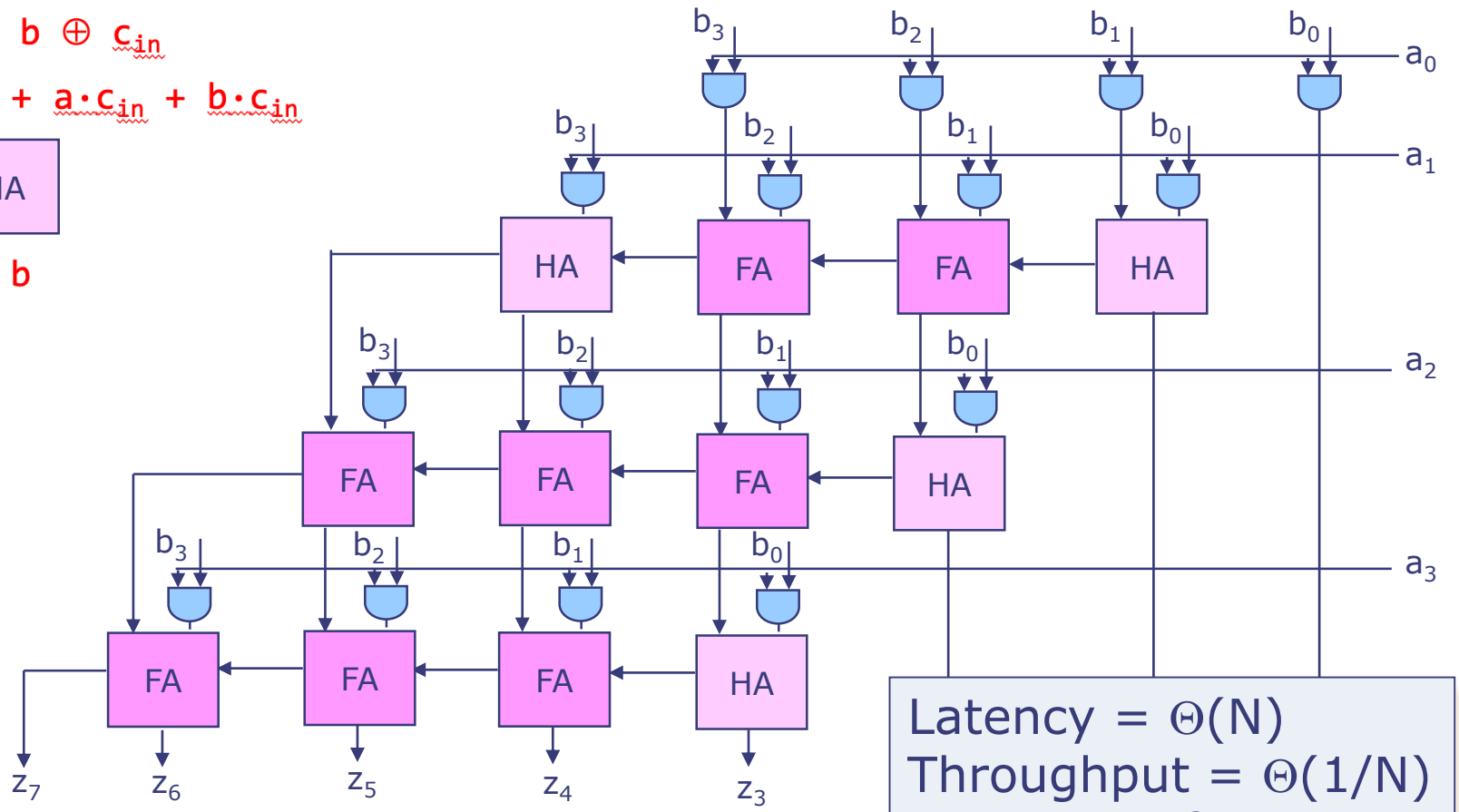
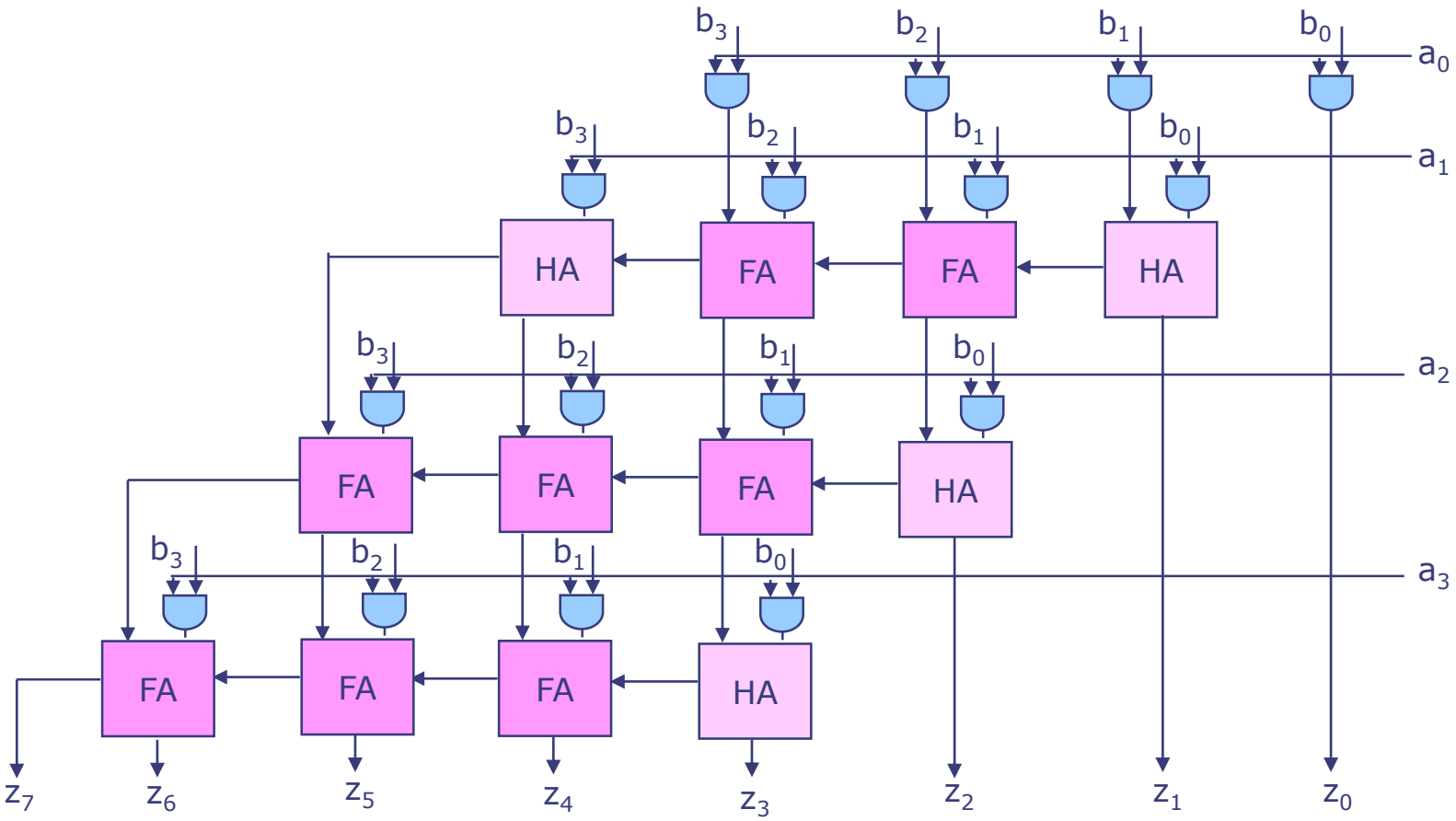
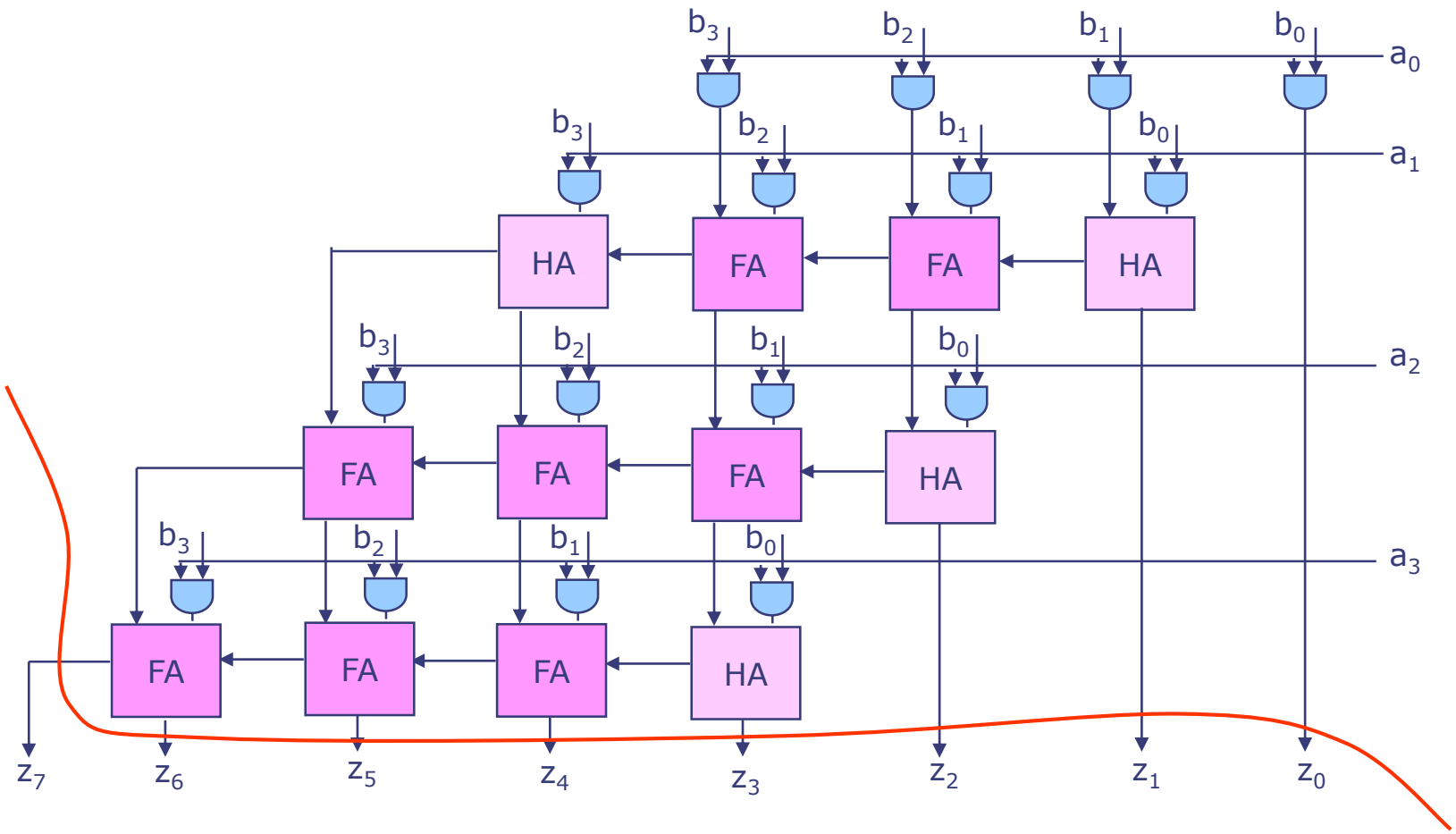


Latency = $\Theta(N)$
Throughput = $\Theta(1/N)$
Area = $\Theta(N^2)$

Pipelining to Increase Throughput
First Attempt



Pipelining to Increase Throughput
First Attempt



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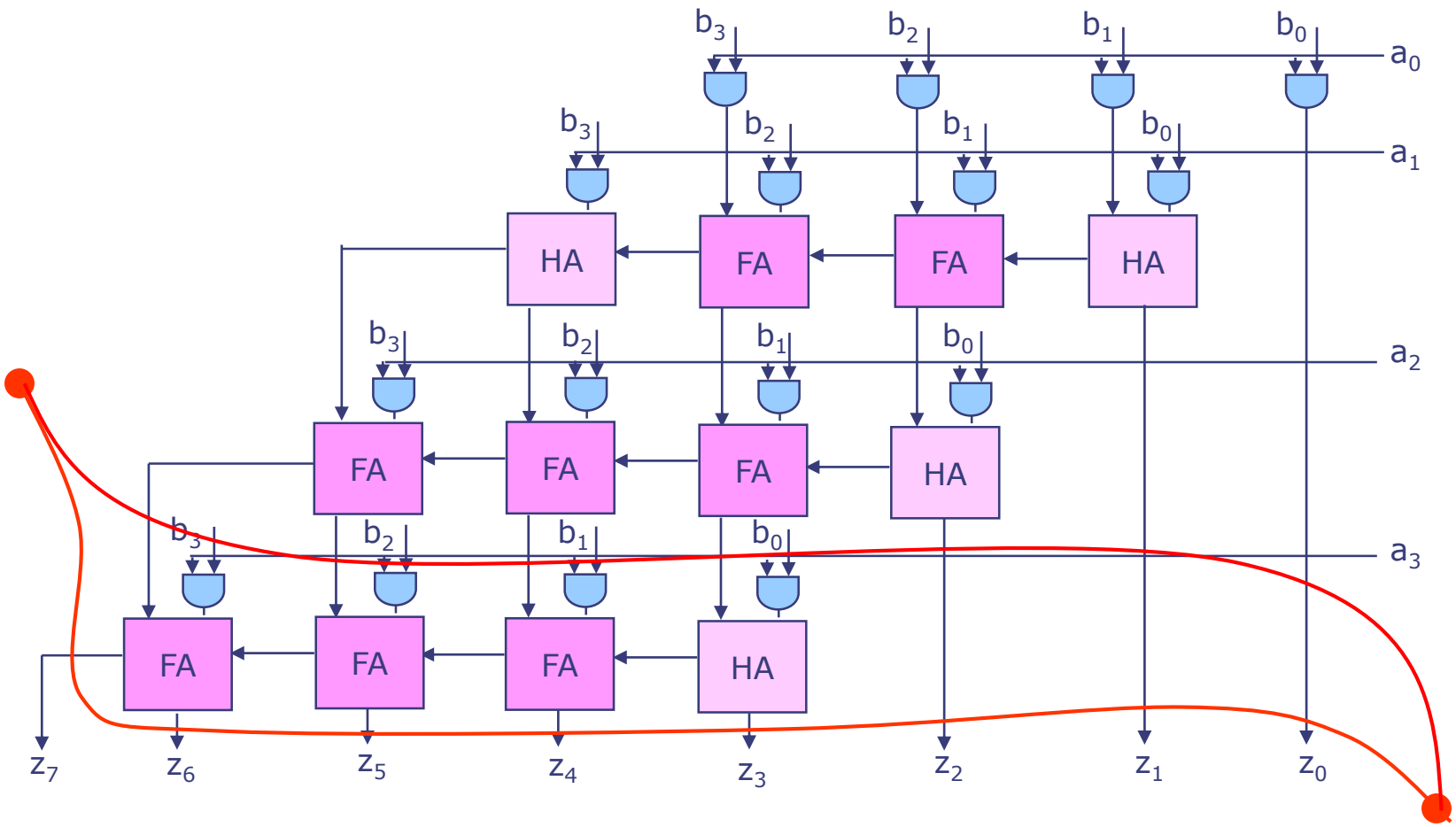

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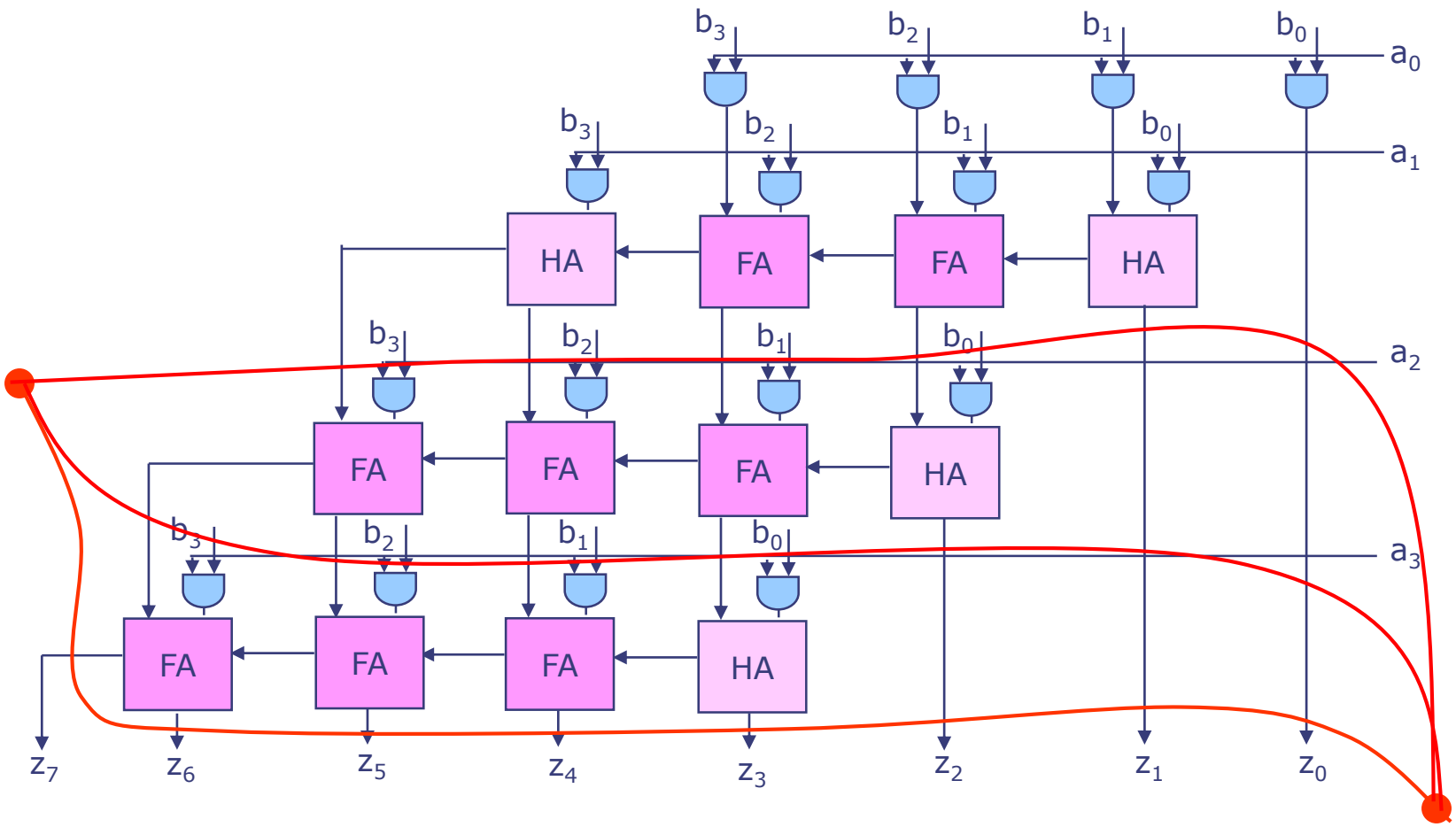
First Attempt



Pipelining to Increase Throughput
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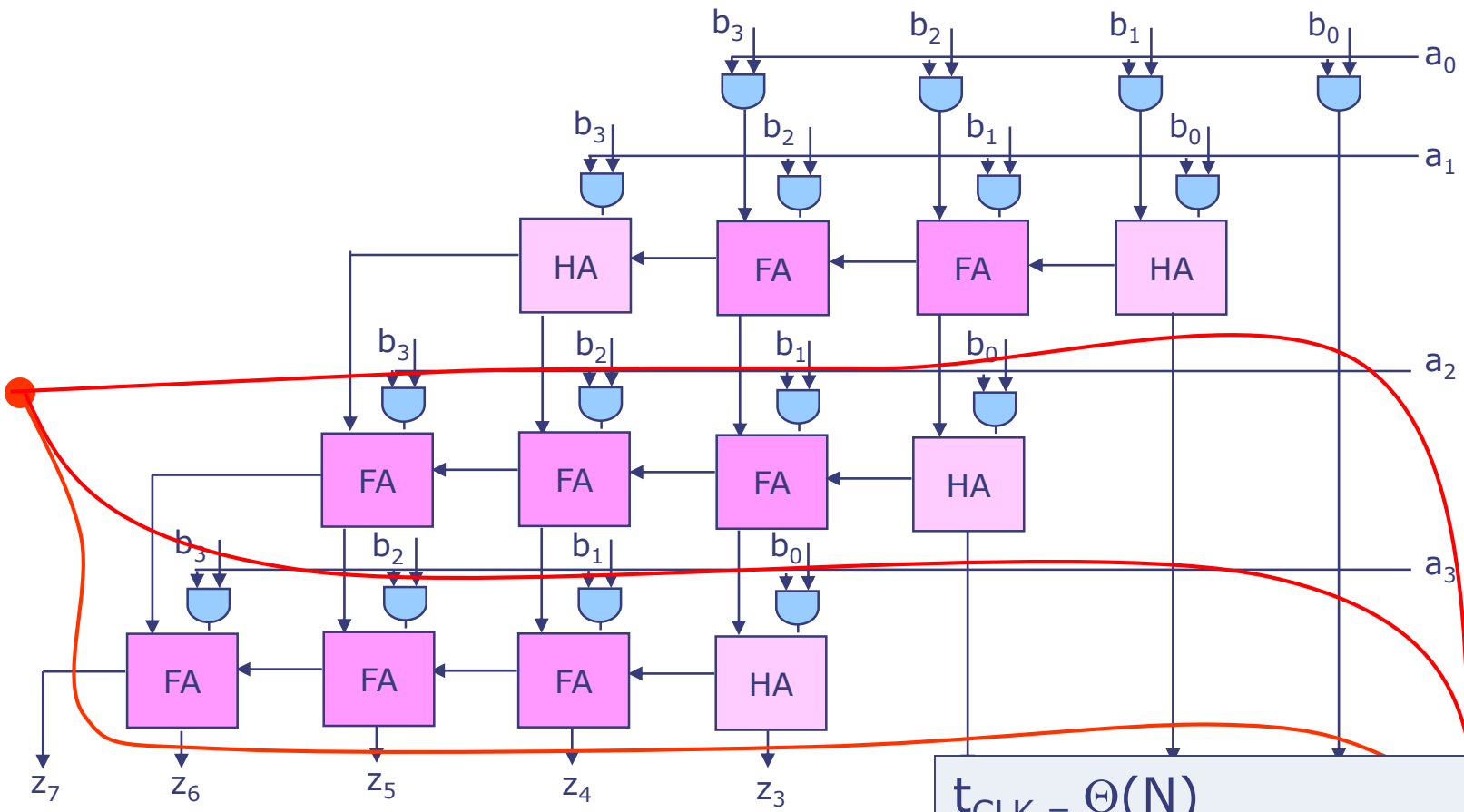
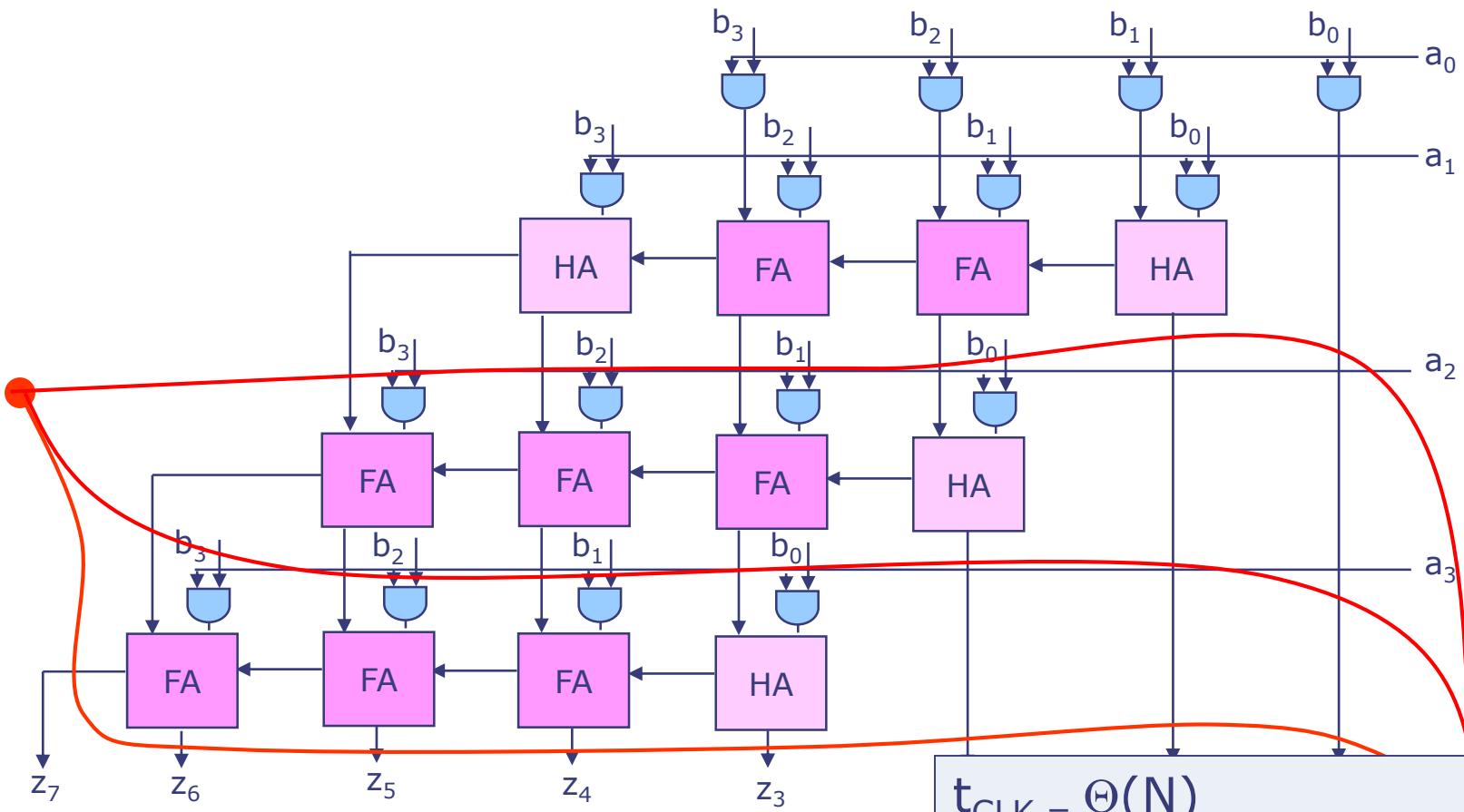


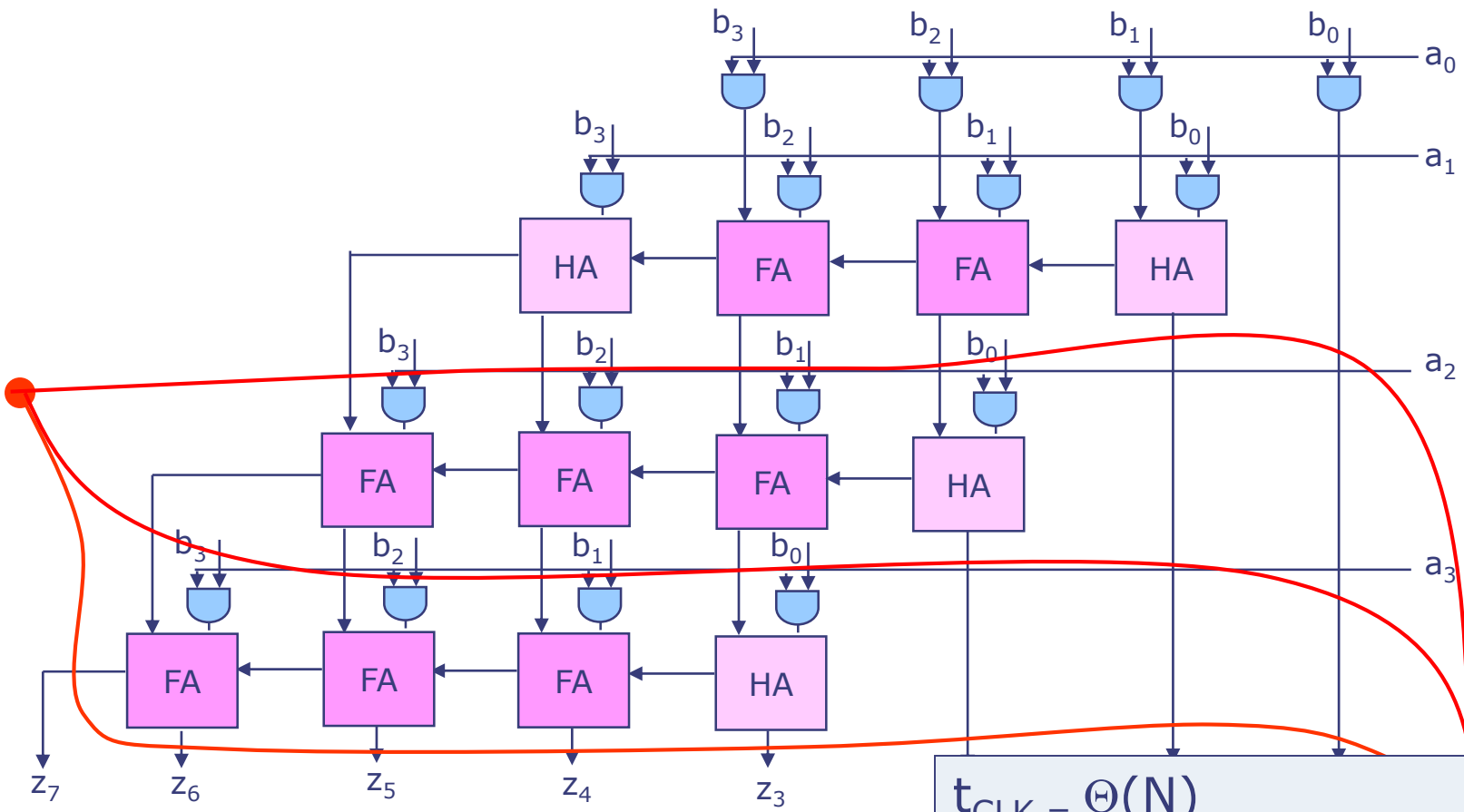
$t_{CLK} = \Theta(N)$

Pipelining to Increase Throughput
First Attempt



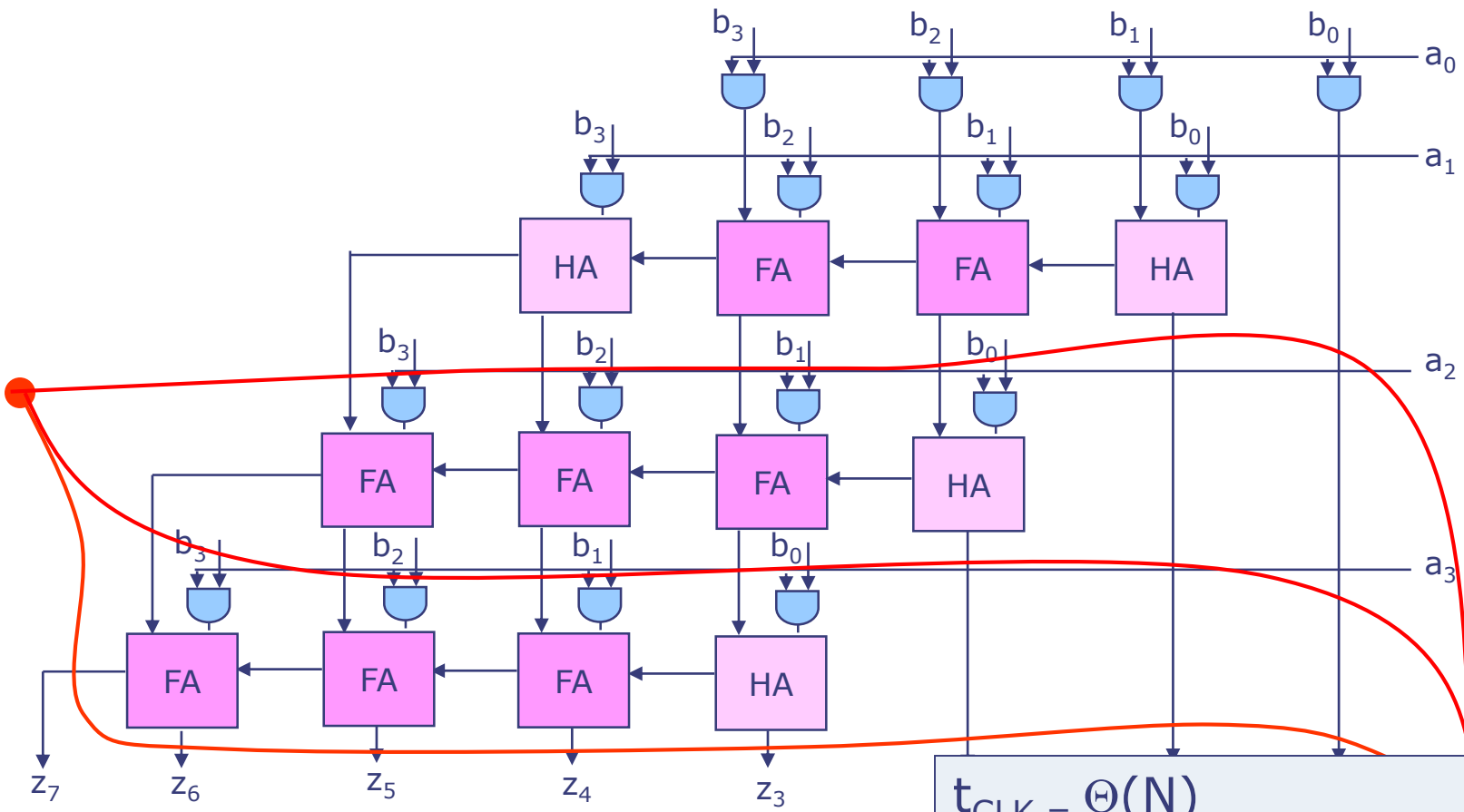
$t_{CLK} = \Theta(N)$
stages = $\Theta(N)$

Pipelining to Increase Throughput
First Attempt



$t_{CLK} = \Theta(N)$
# stages = $\Theta(N)$
Latency = $\Theta(N^2)$

Pipelining to Increase Throughput
First Attempt



$t_{CLK} = \Theta(N)$
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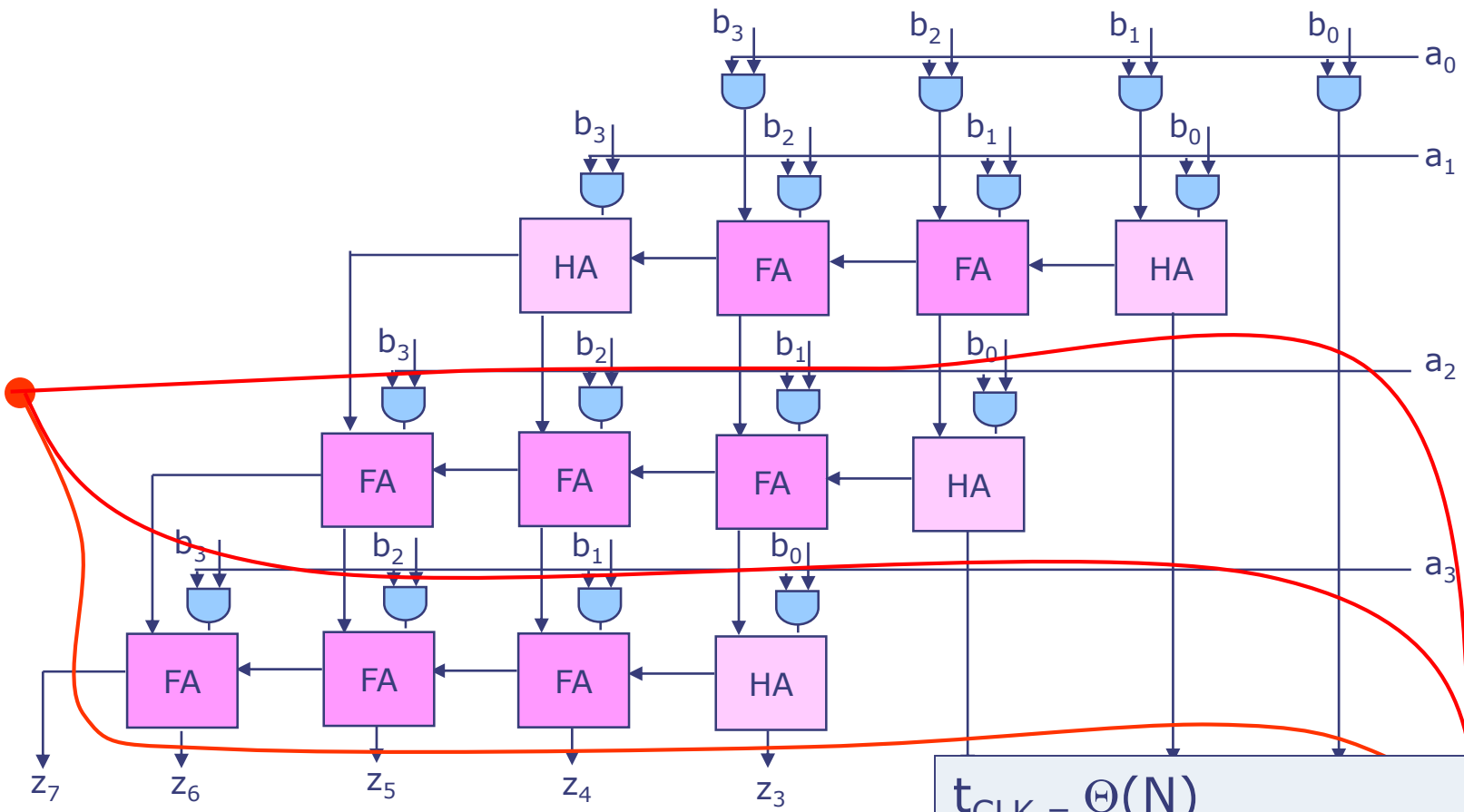

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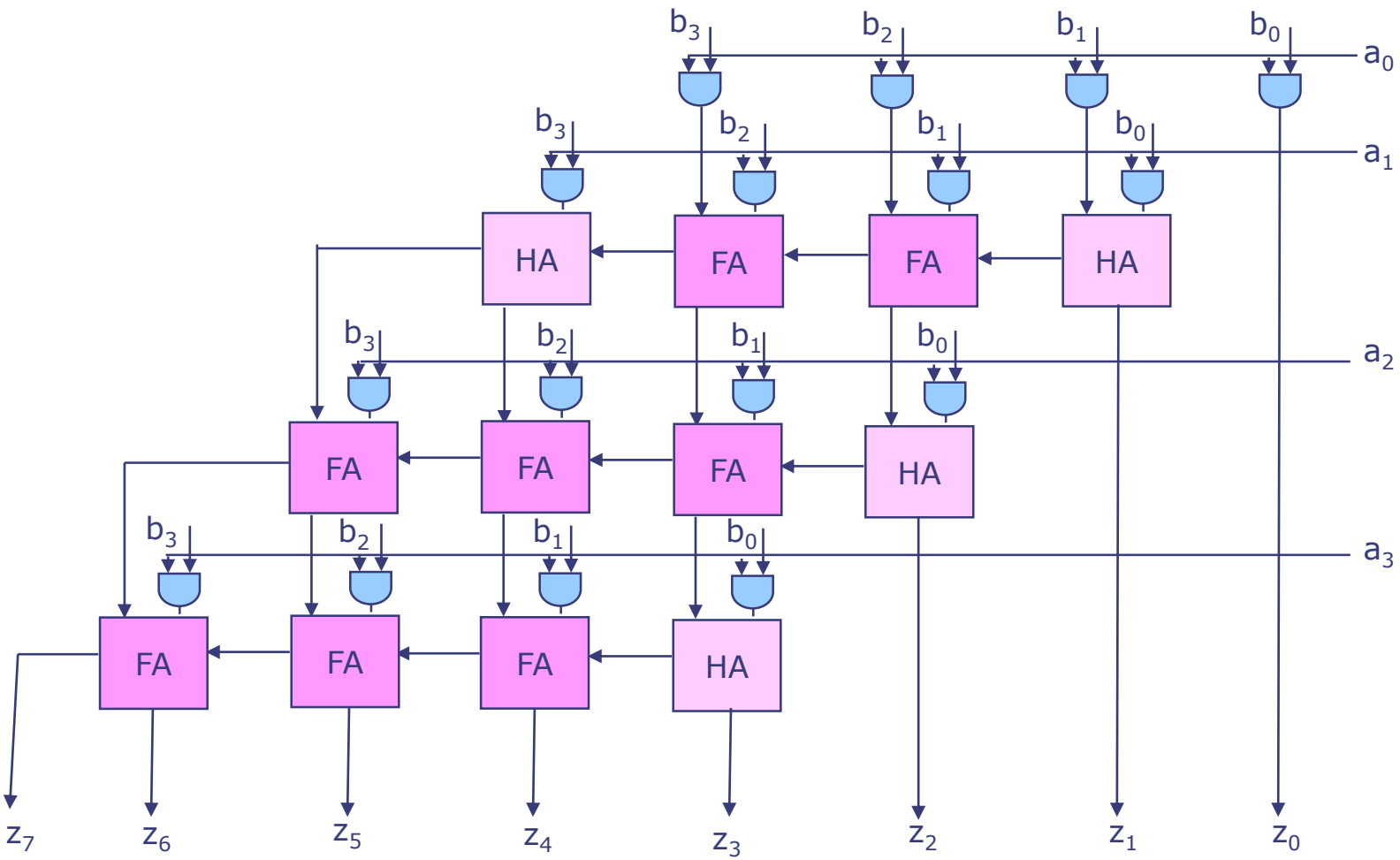
Throughput = $\Theta(1/N)$

Need to break carry chain

Pipelining to Increase Throughput



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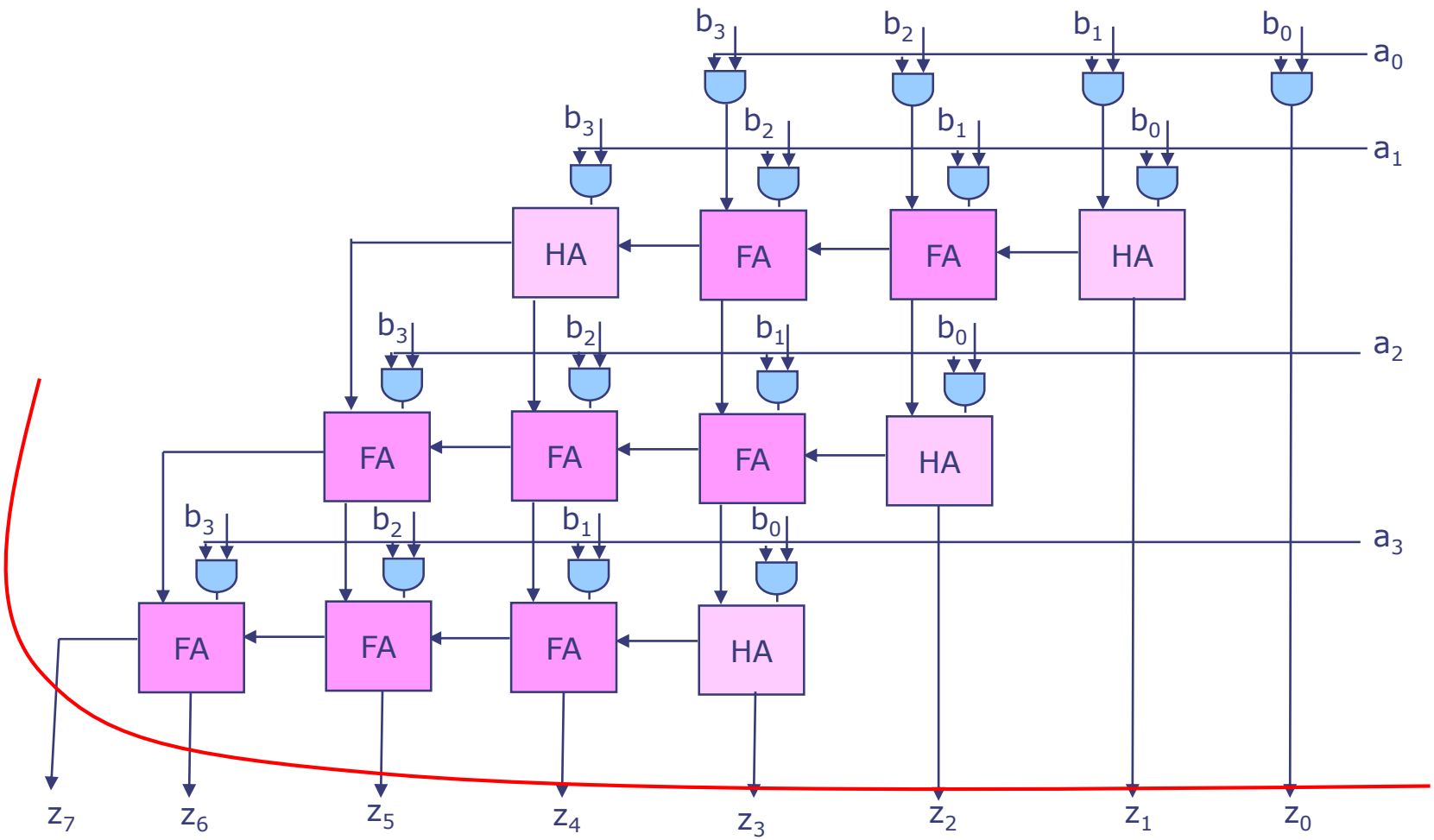

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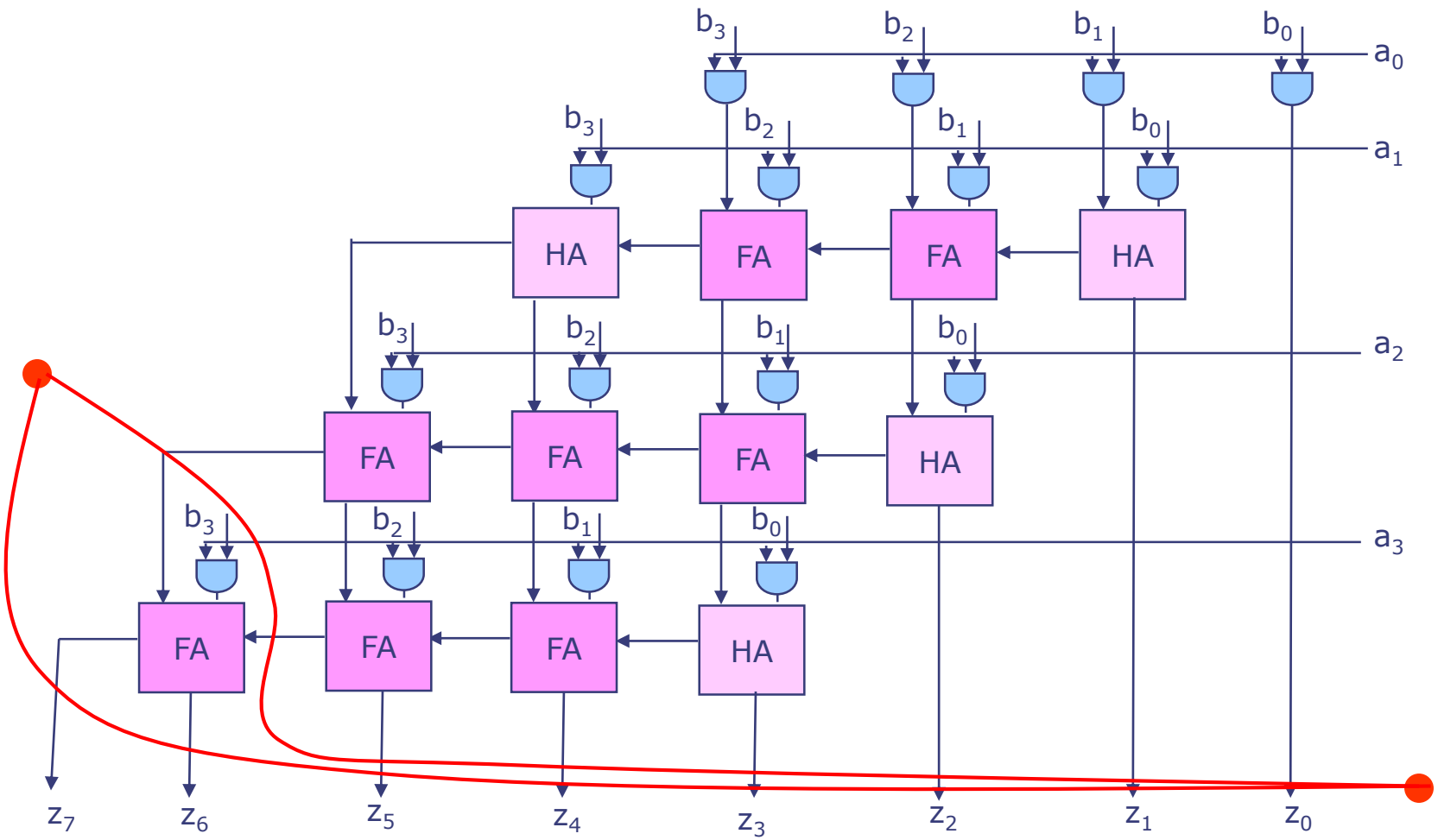

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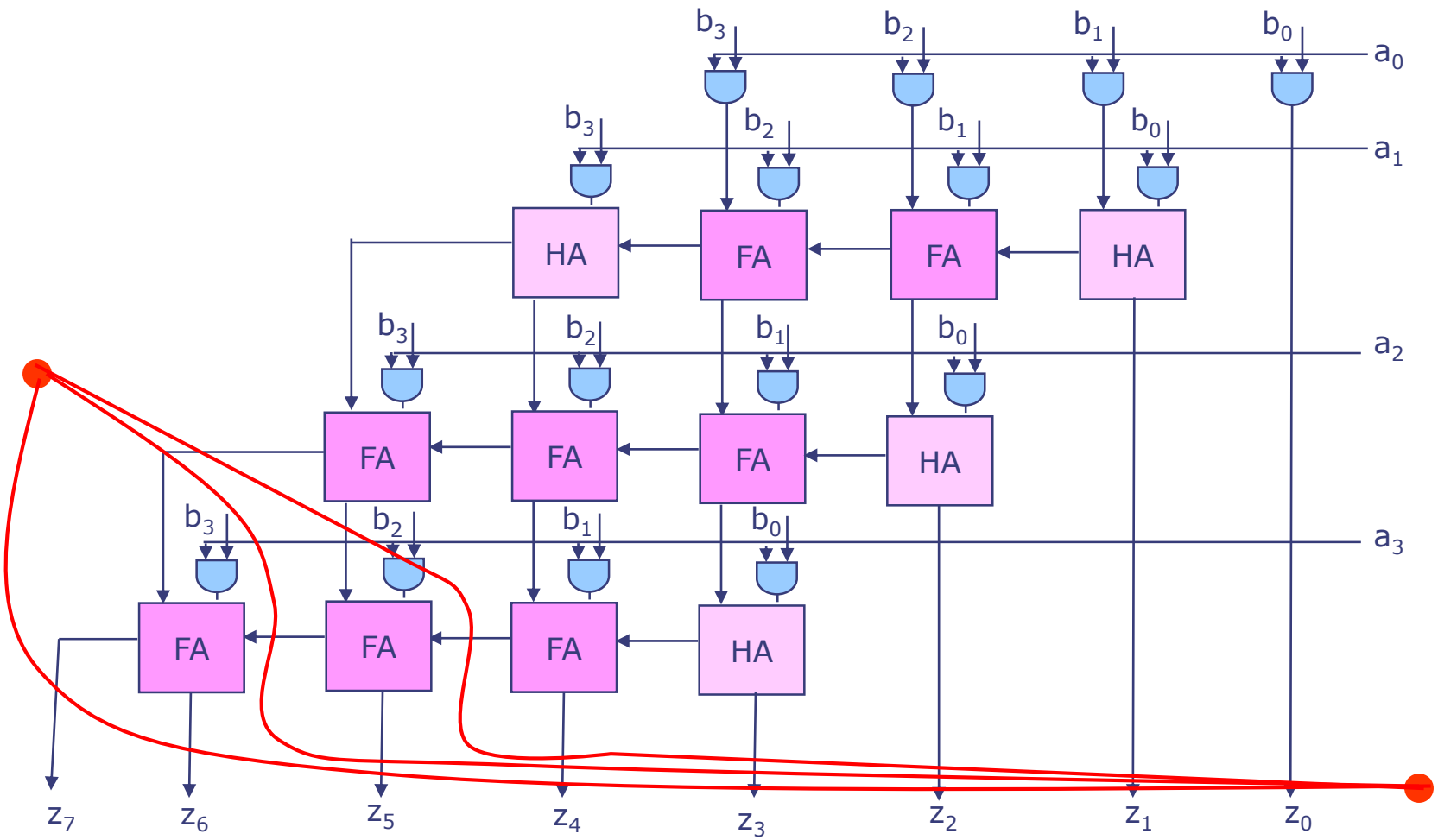

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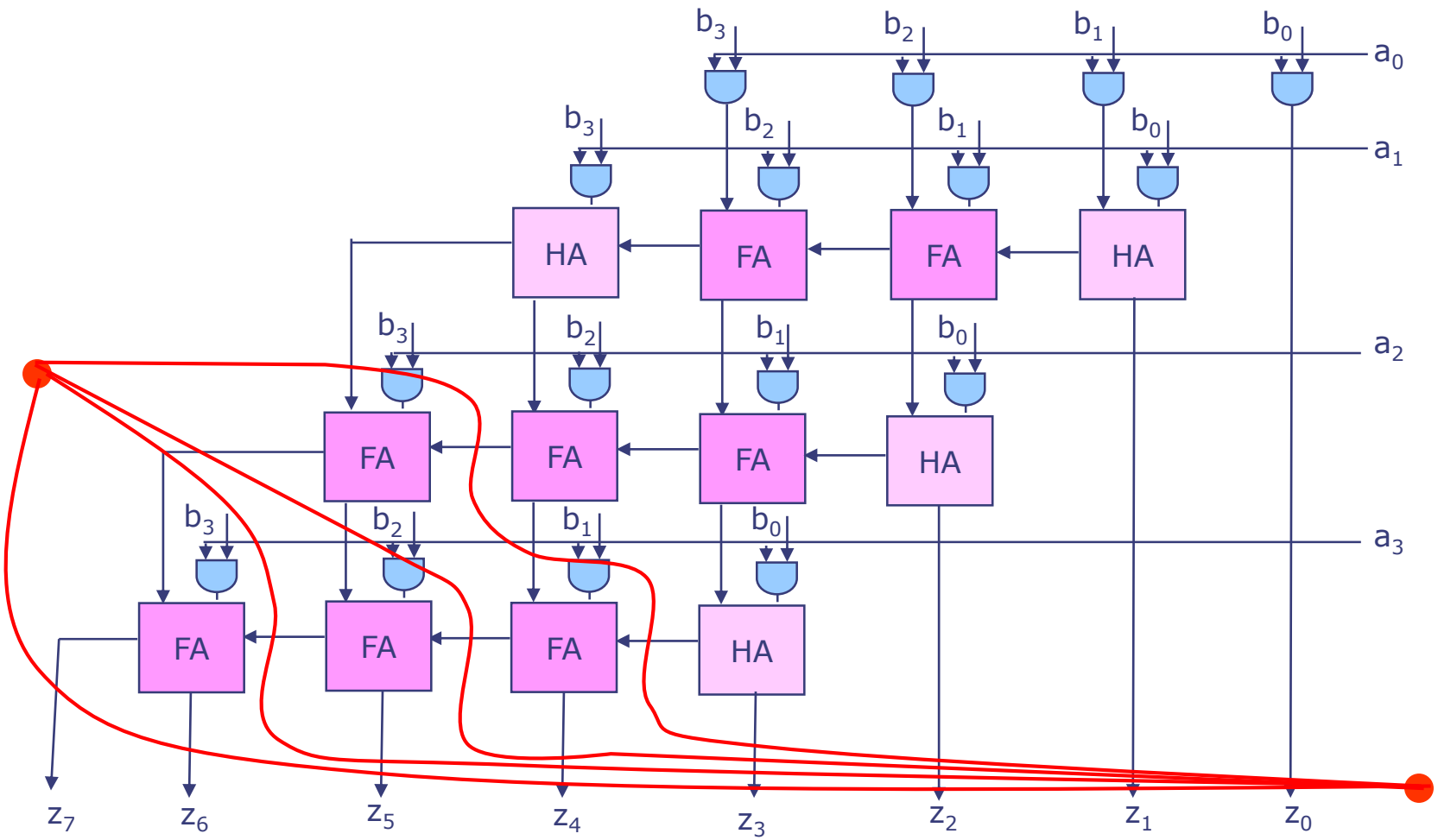

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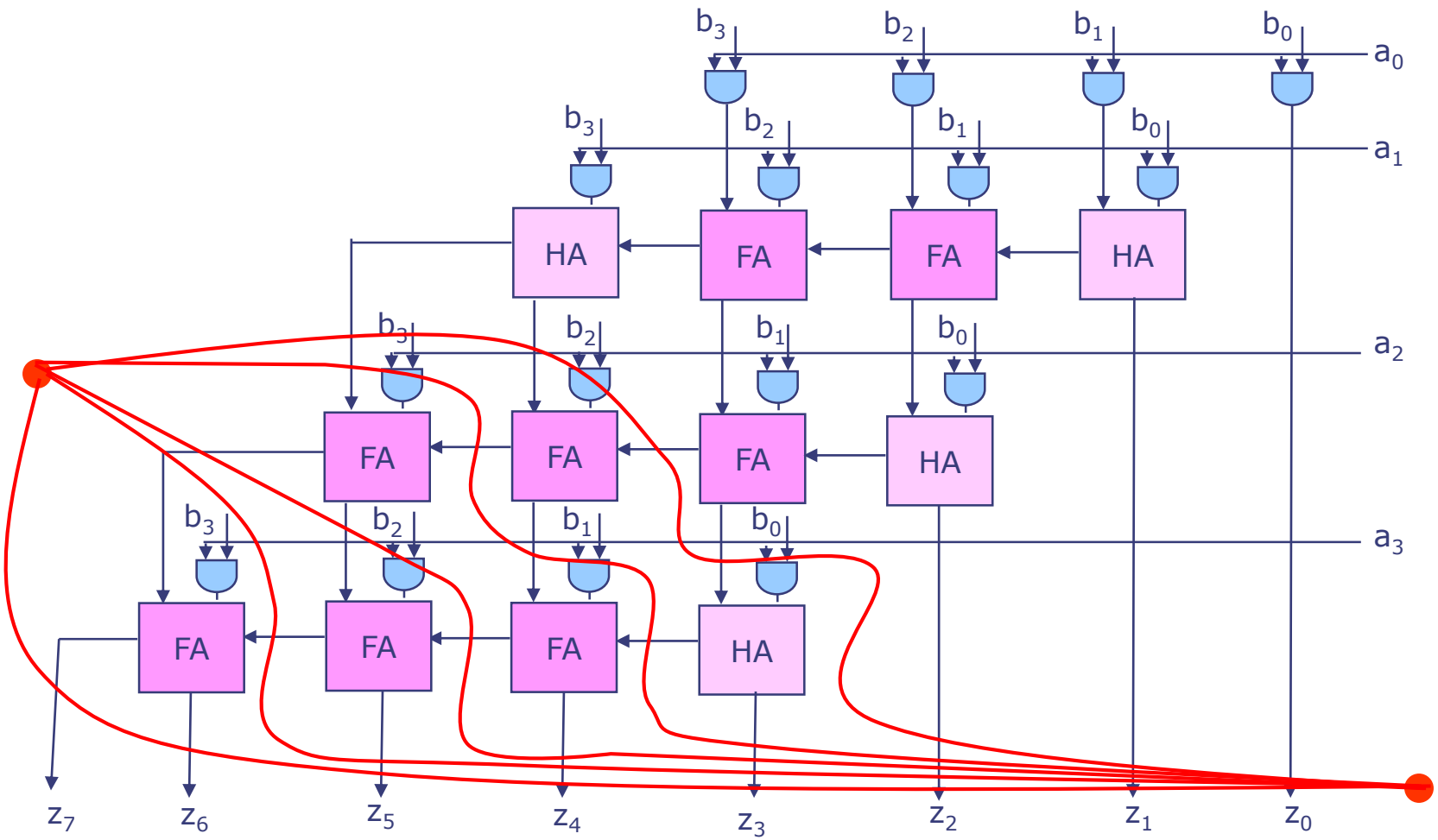

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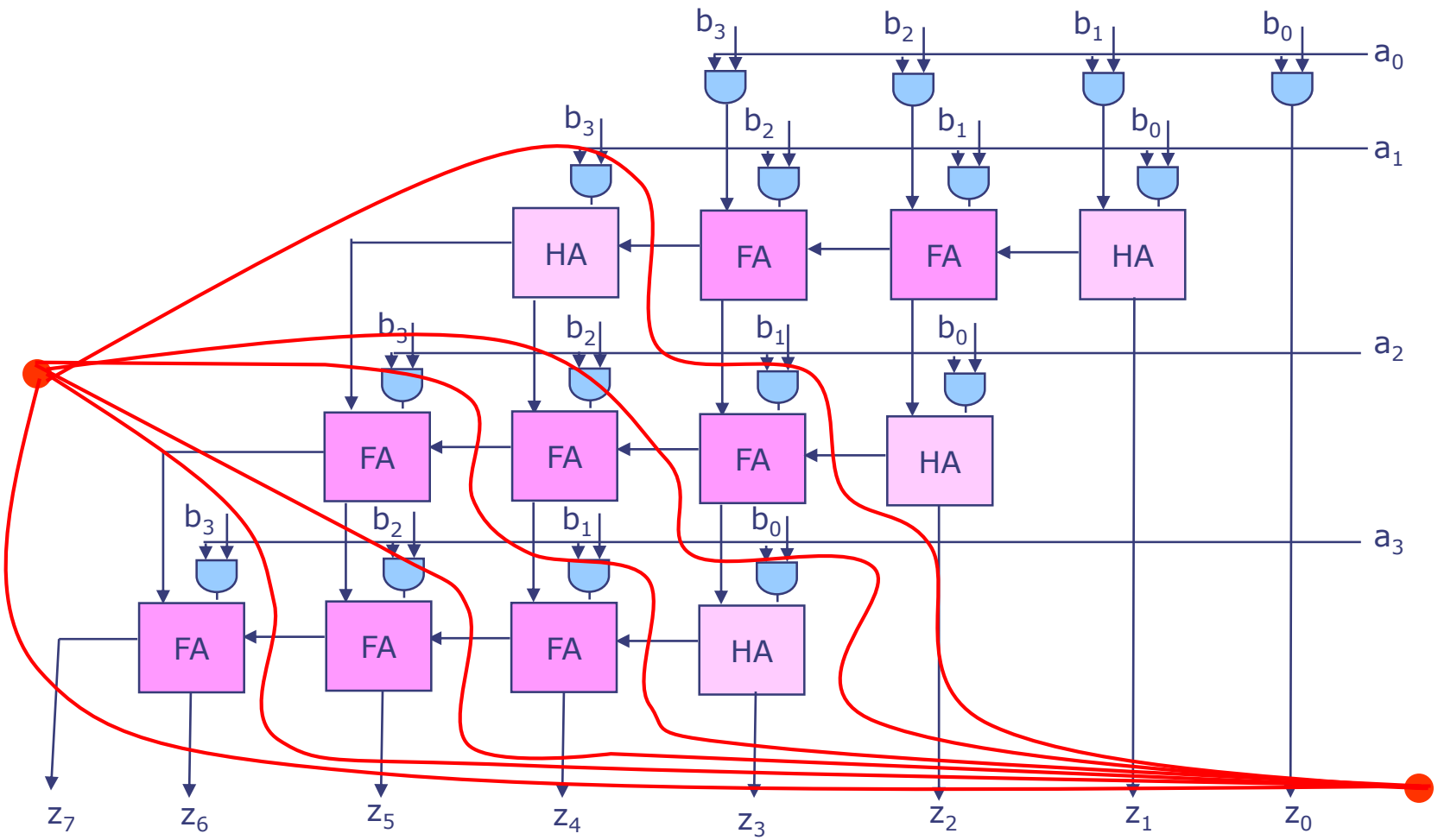

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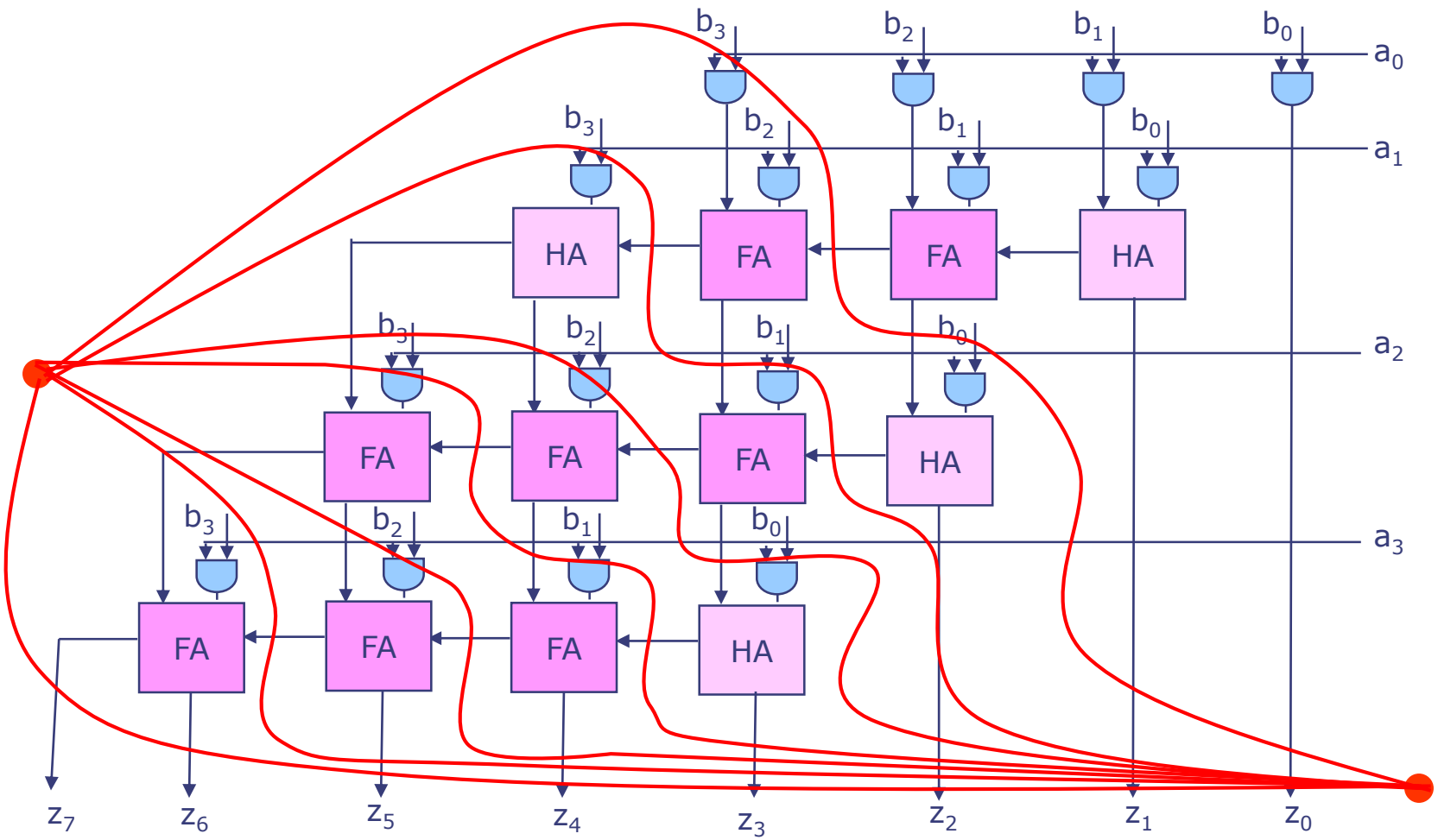

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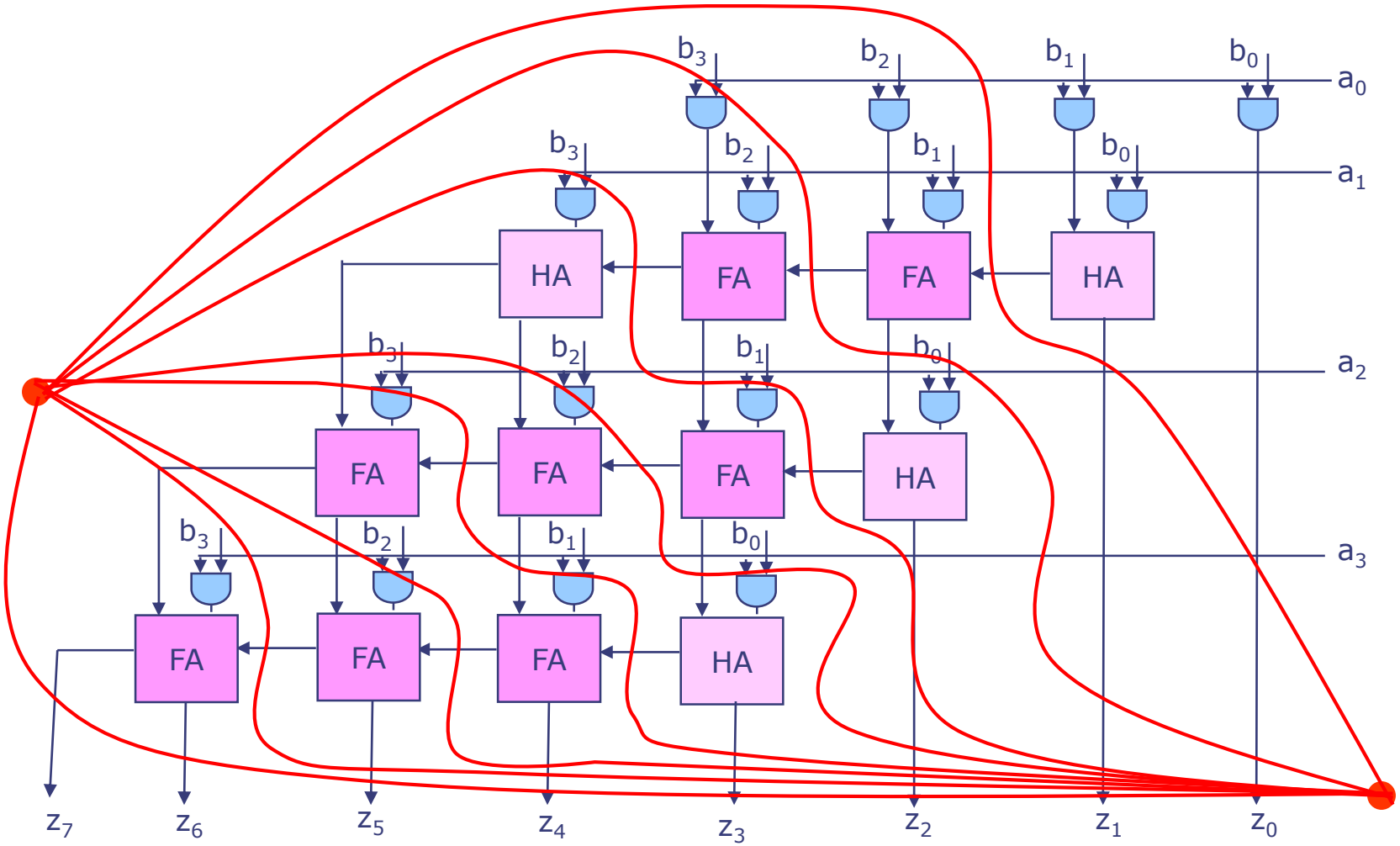

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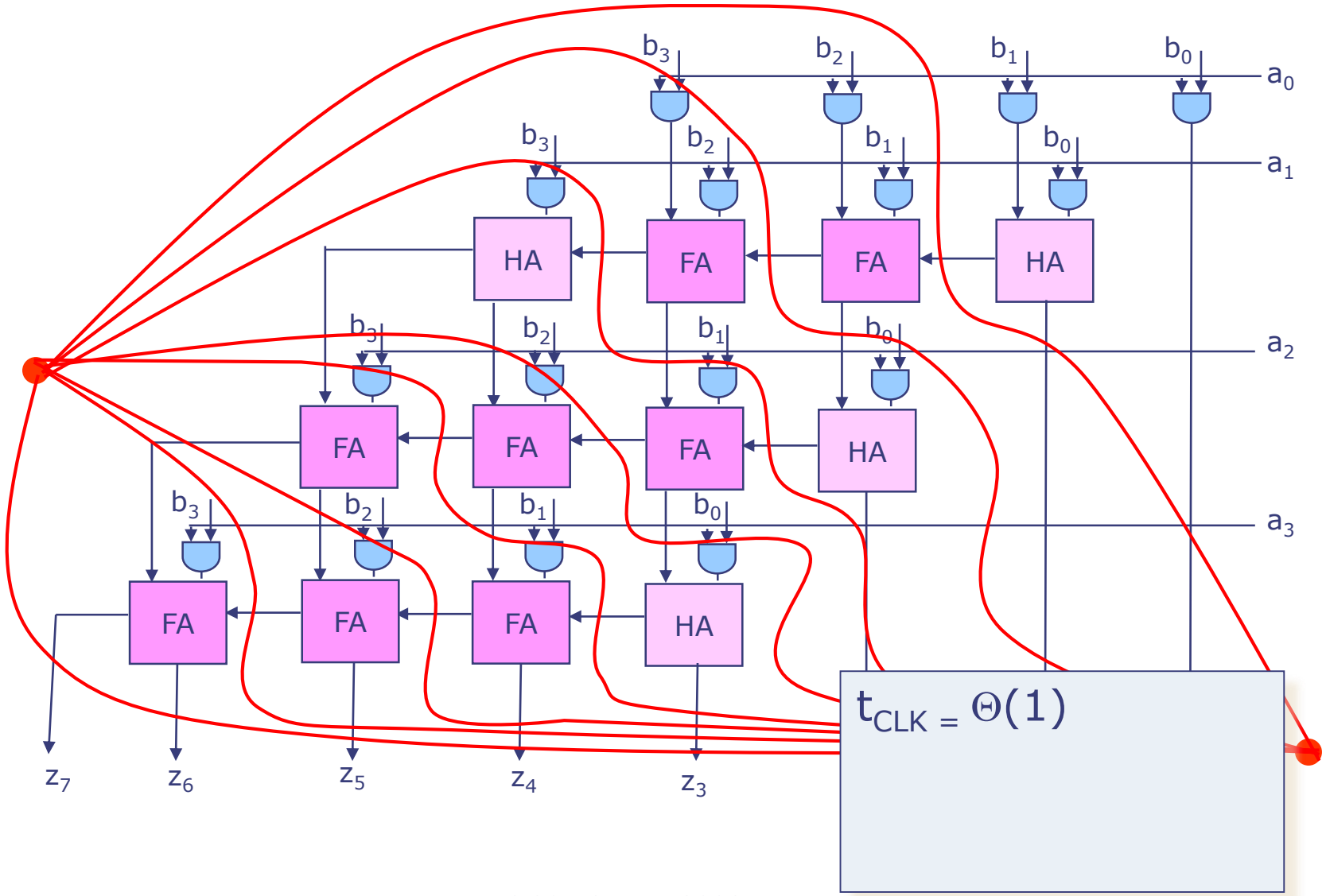

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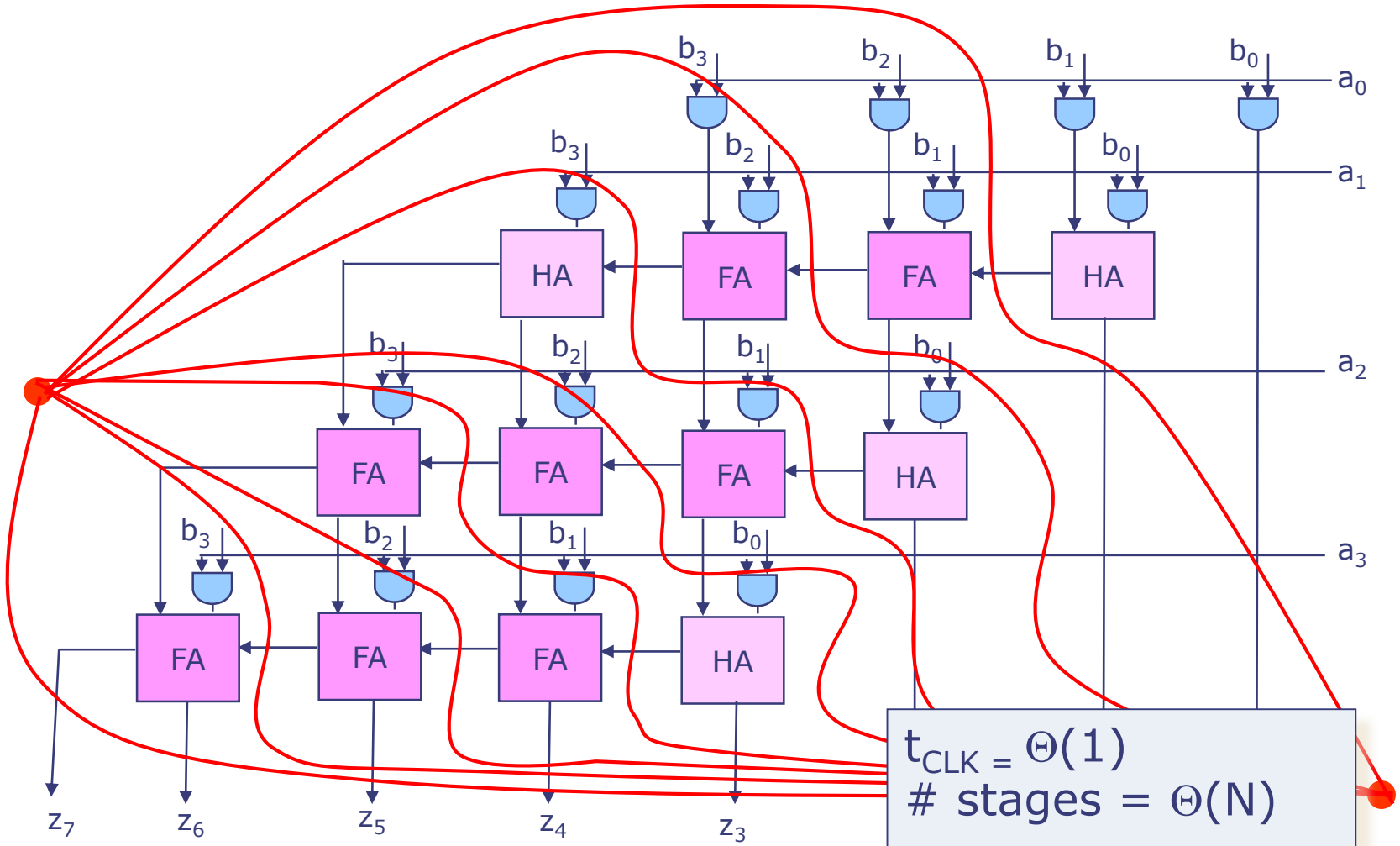
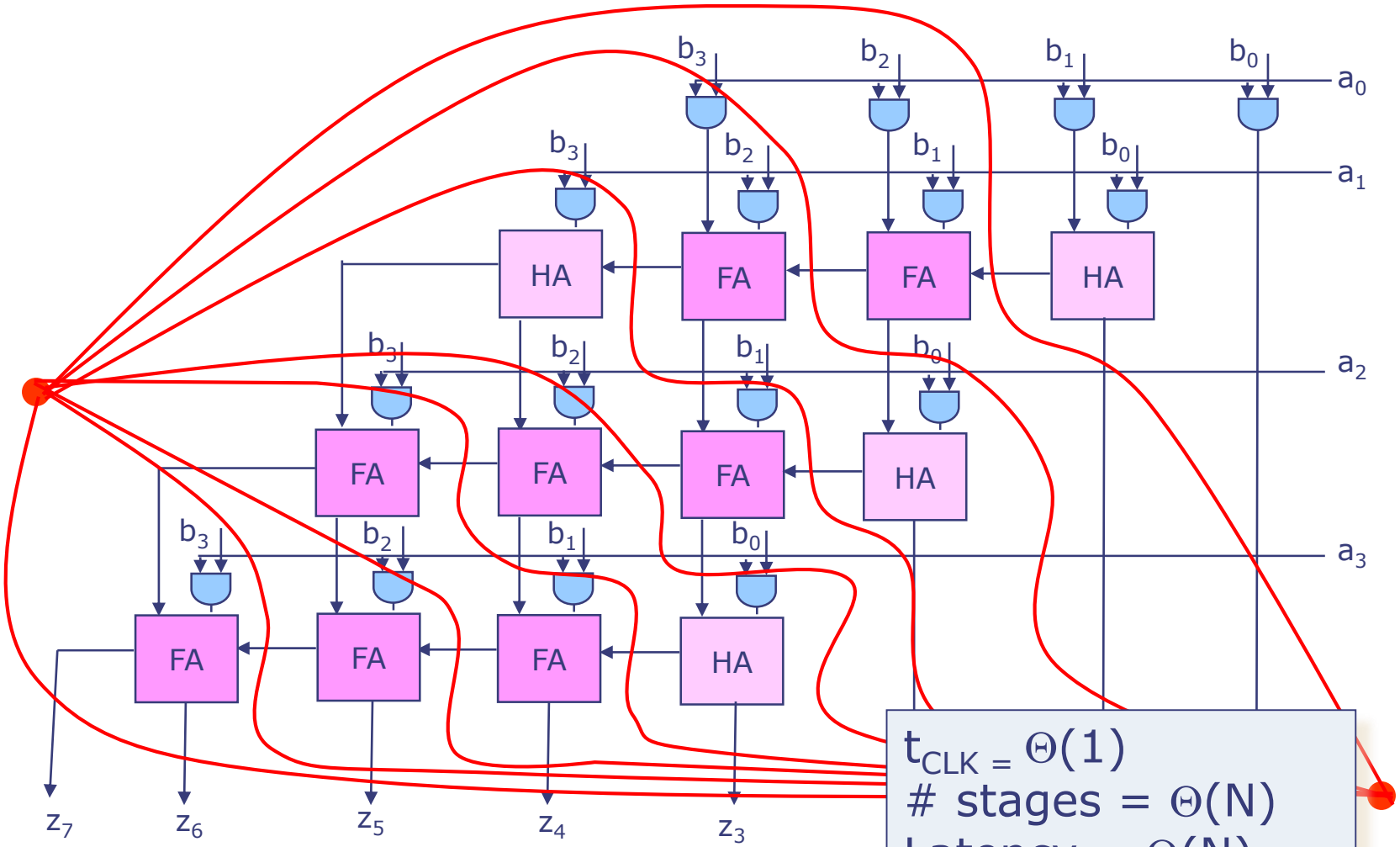


$t_{CLK} = \Theta(1)$

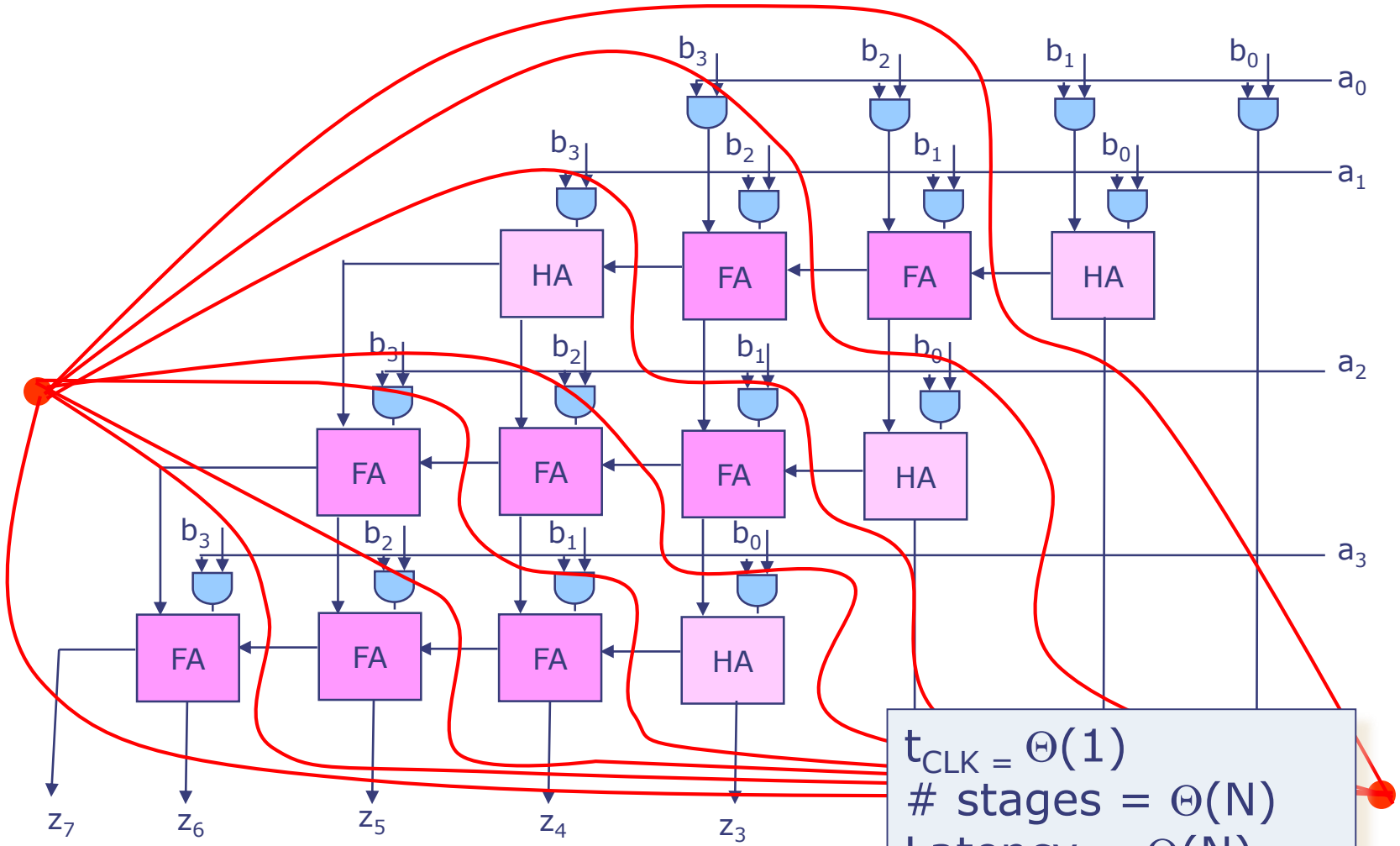
\# stages = $\Theta(N)$

Pipelining to Increase Throughput



$t_{CLK} = \Theta(1)$
# stages = $\Theta(N)$
Latency = $\Theta(N)$

Pipelining to Increase Throughput



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Folded (Multi-Cycle) Multiplier

- Combinational circuits often have repetitive logic
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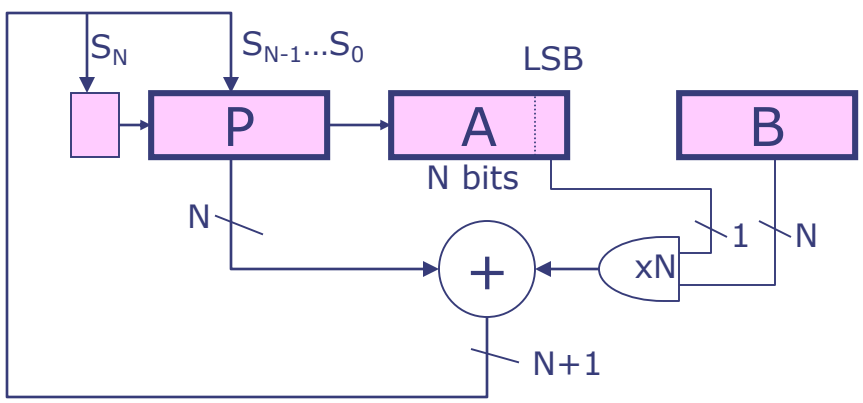


```
Init: P←0, load A&B

Repeat N times {
   P ← P + (A_LSB==1 ? B : 0)
   shift S_N,P,A right one bit
}

Done: 2N-bit result in P,A
```

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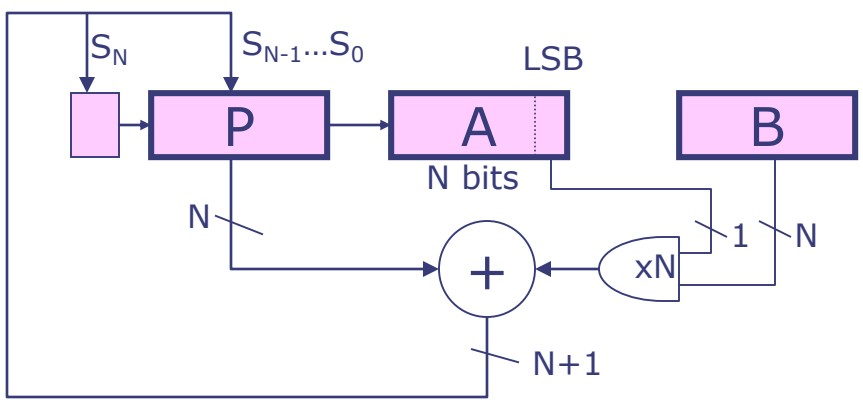


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```
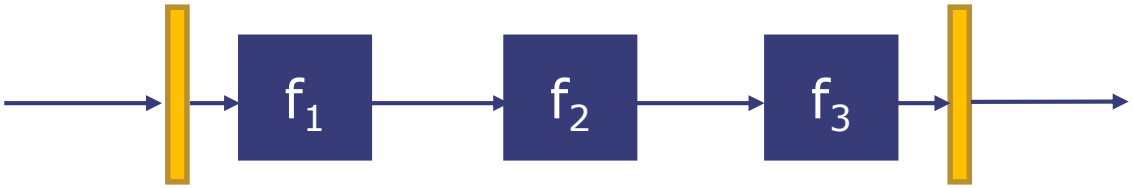
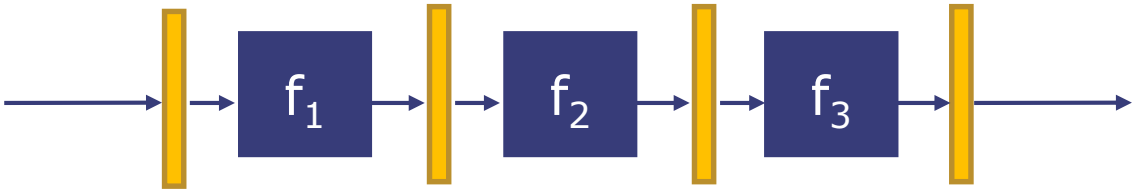

Tradeoff: reduced area, but lower throughput

Summary: Design Alternatives

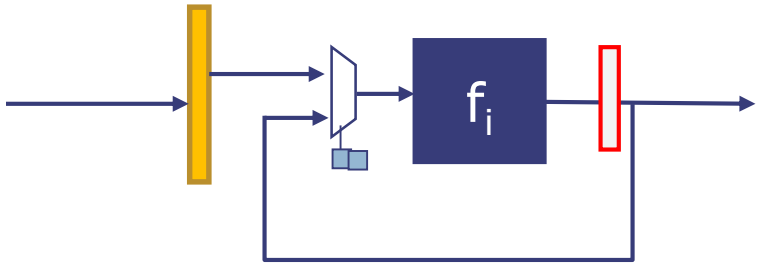
Several combinational modules in one pipeline stage (A)



One module per pipeline stage (B)



Folded reuse a block, multi-cycle (C)



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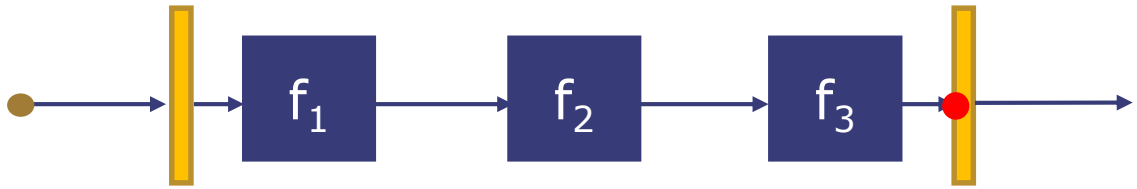

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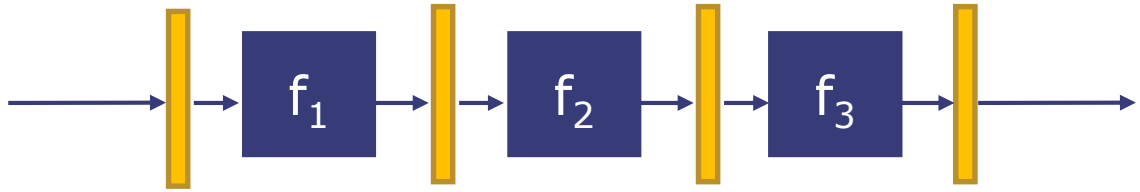

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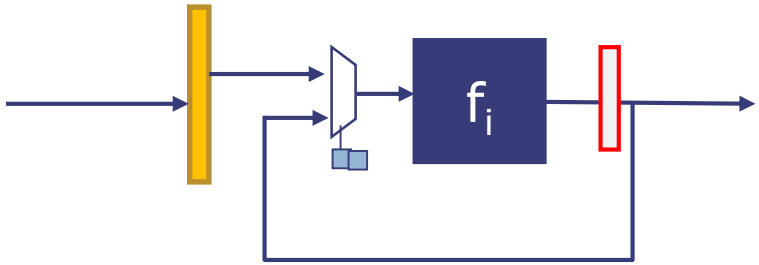

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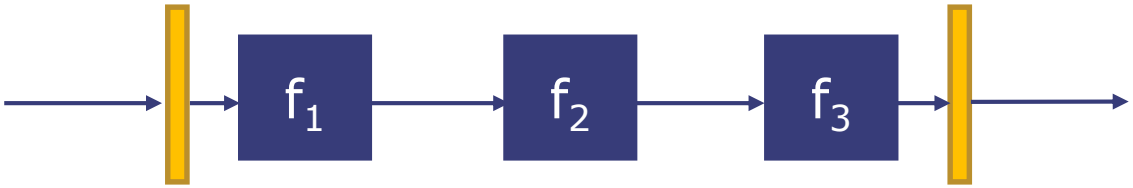

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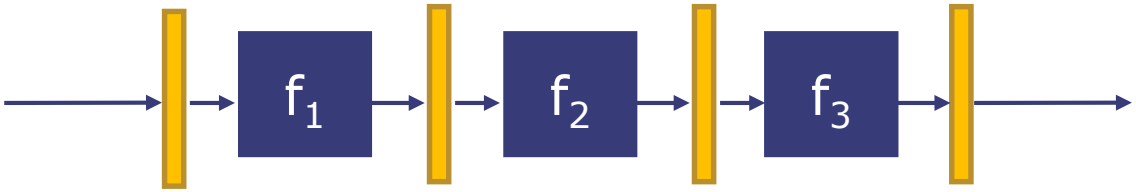

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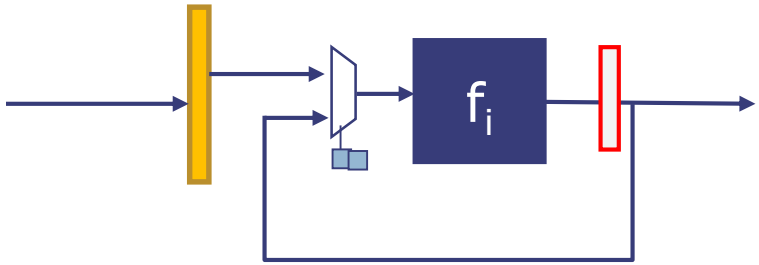

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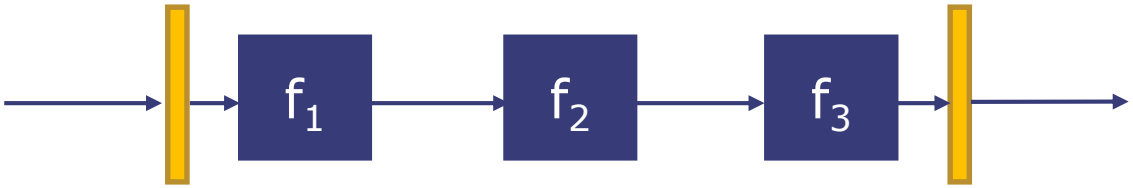
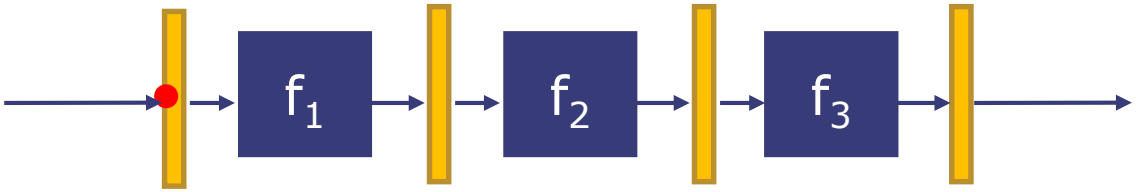
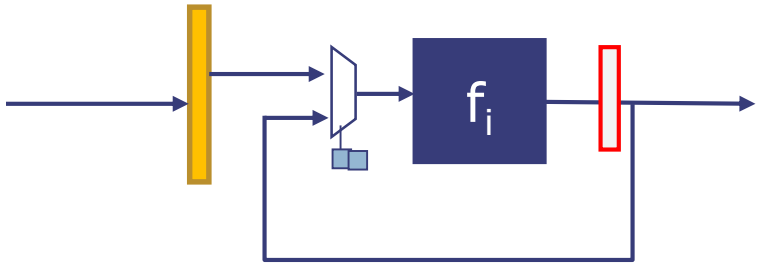


One module per pipeline stage (B)



Folded reuse a block, multi-cycle (C)



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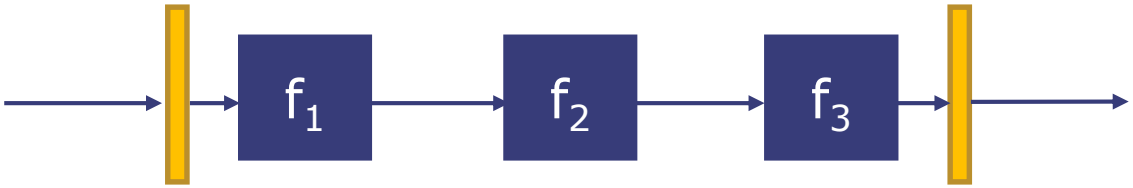

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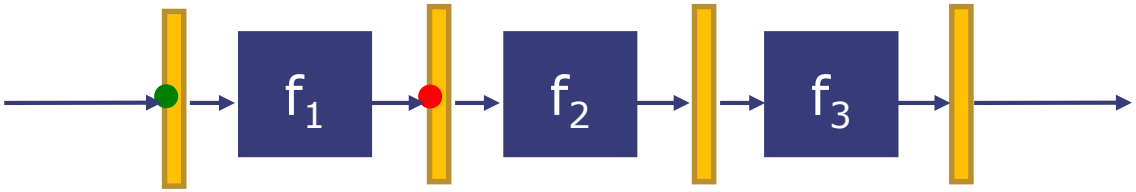

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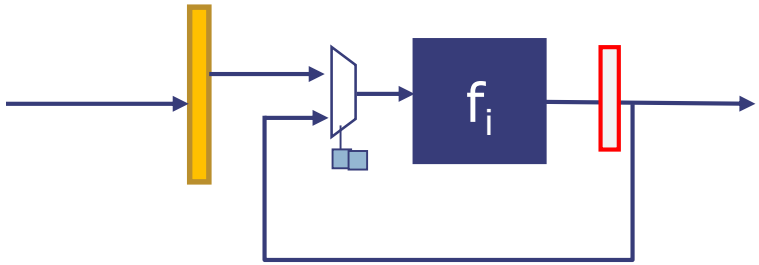

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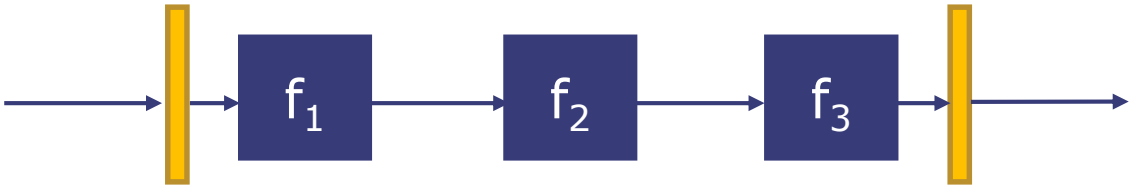
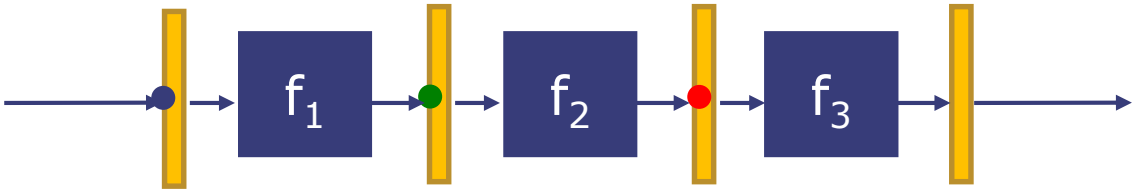
Several combinational modules in one pipeline stage (A)



One module per pipeline stage (B)



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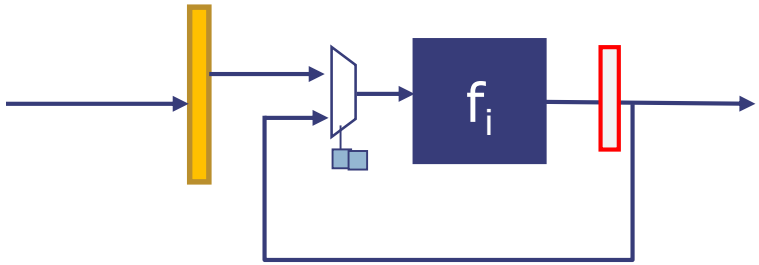

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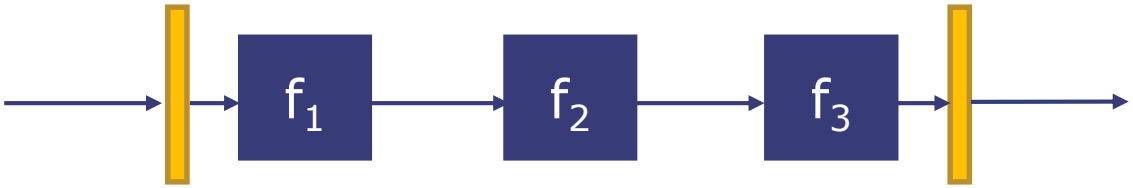

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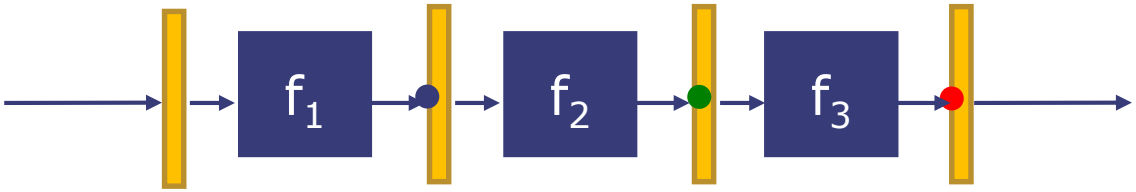

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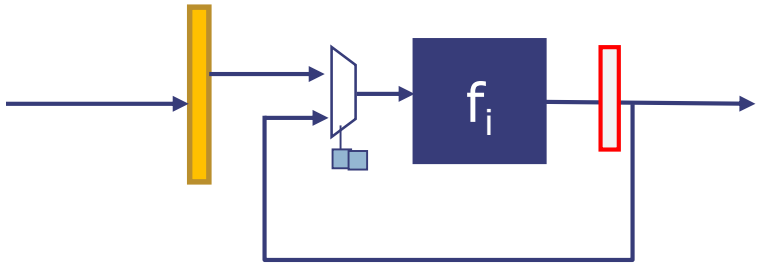

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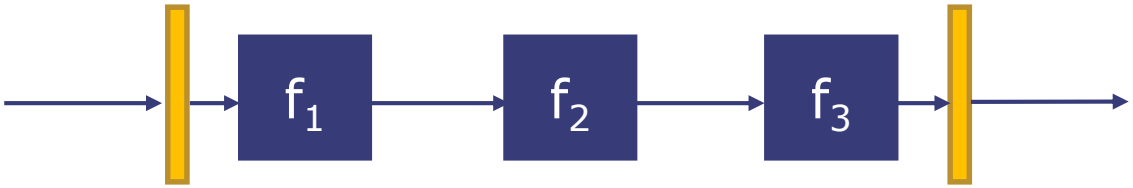

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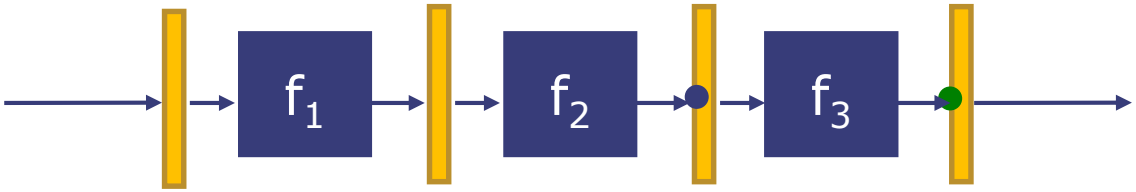

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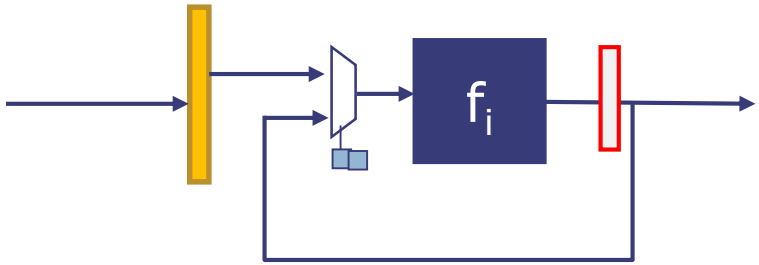

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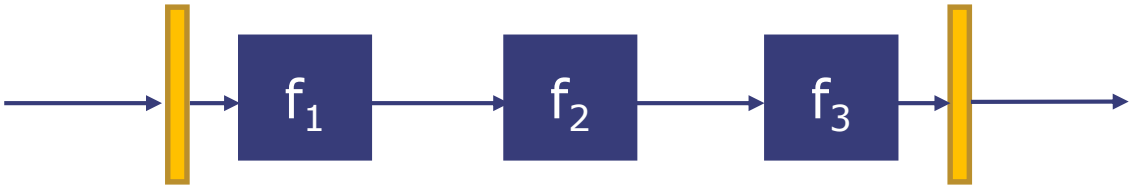

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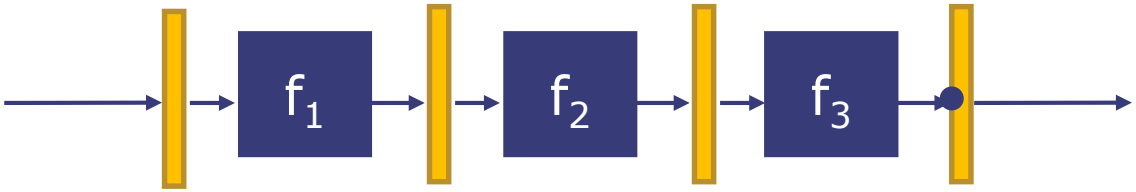

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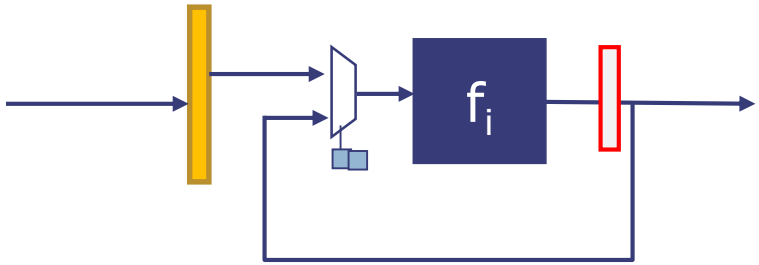

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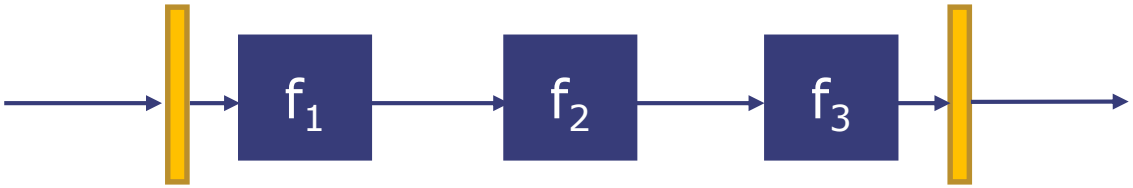

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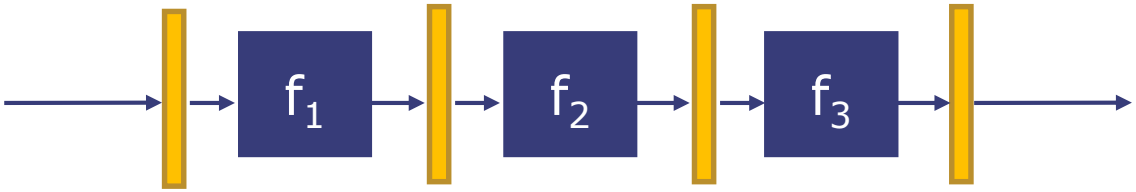

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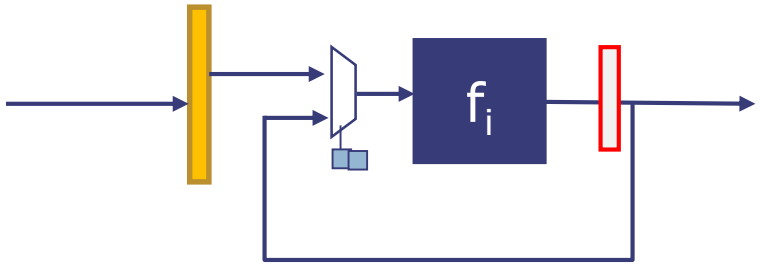

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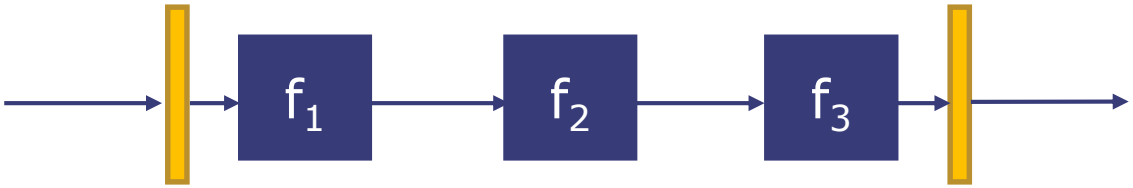

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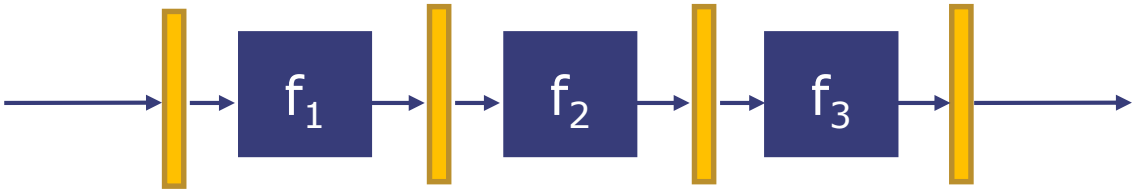

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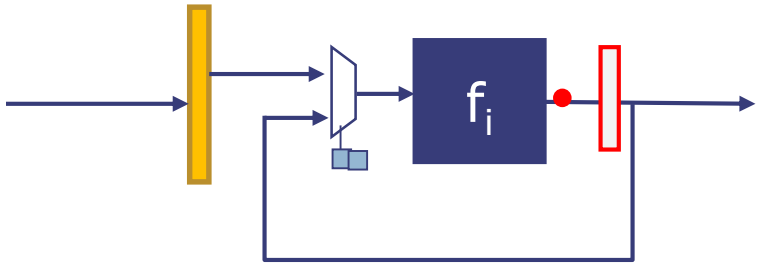

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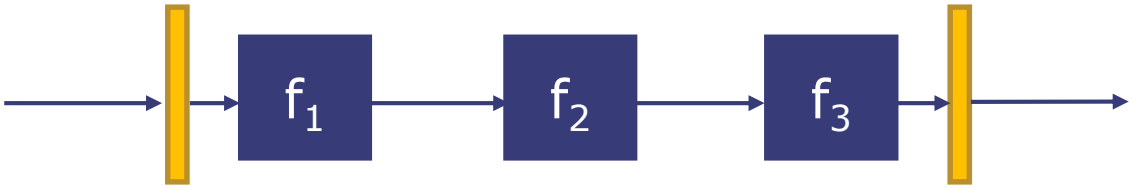

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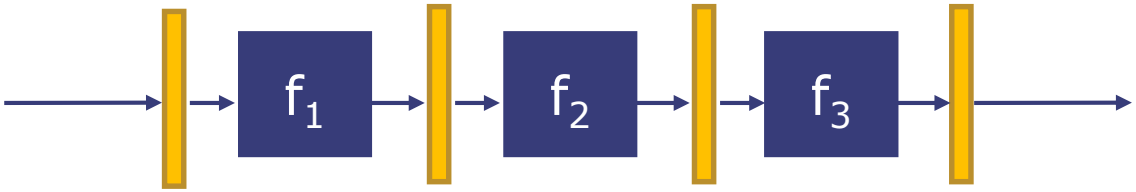

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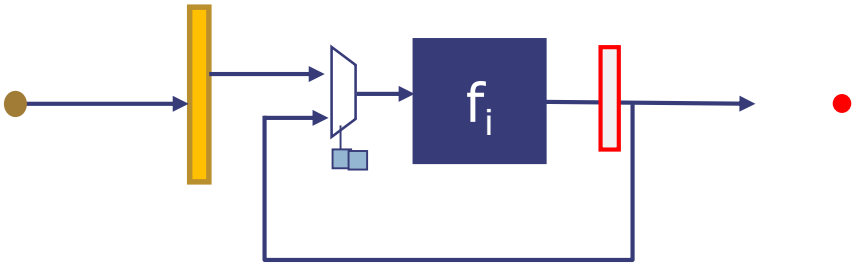

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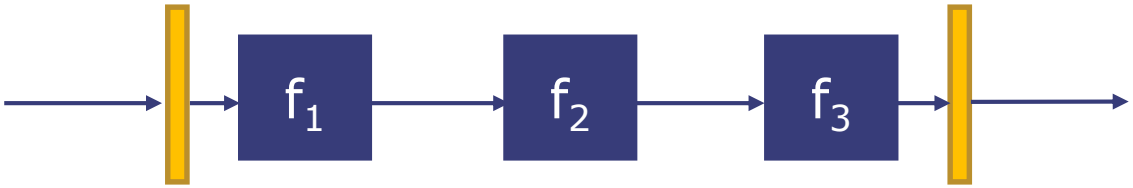

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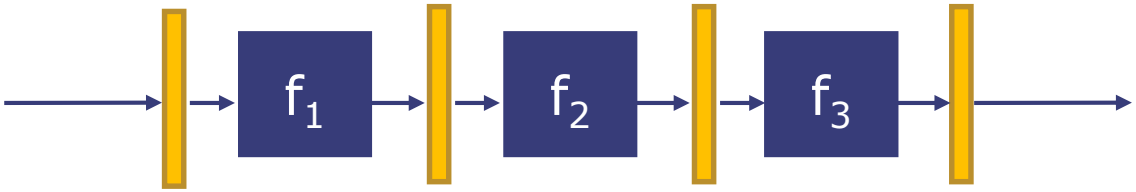

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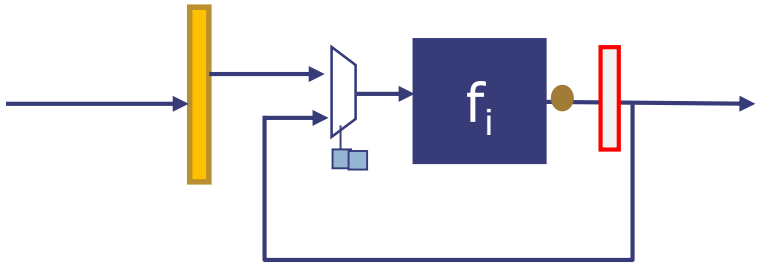

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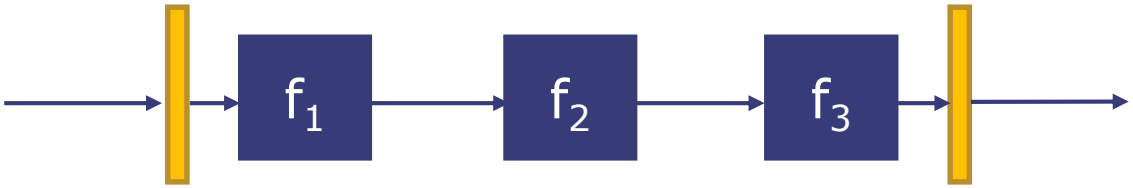

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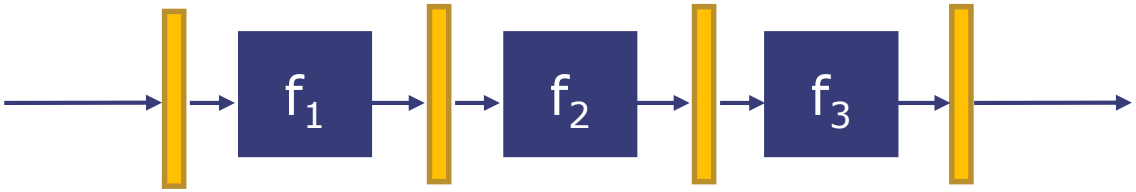

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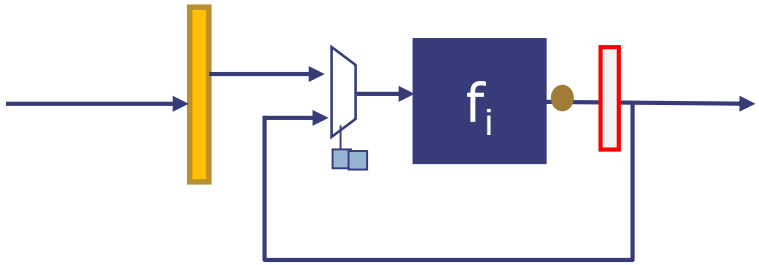

Clock?

Latency?

Area?

Throughput?

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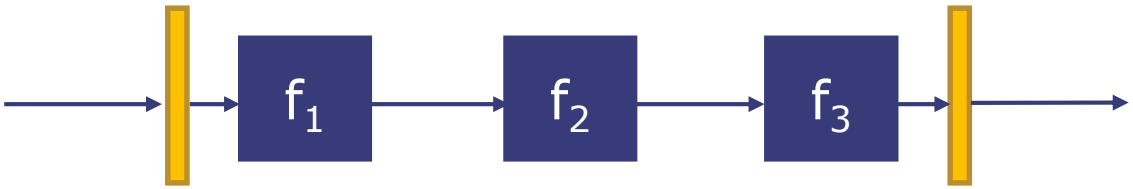

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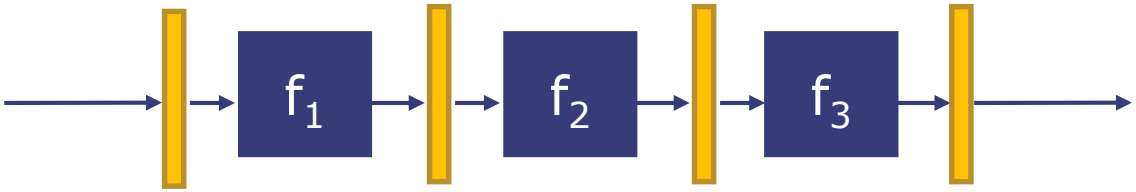

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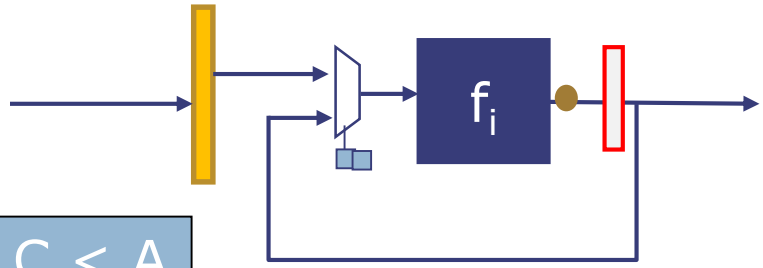

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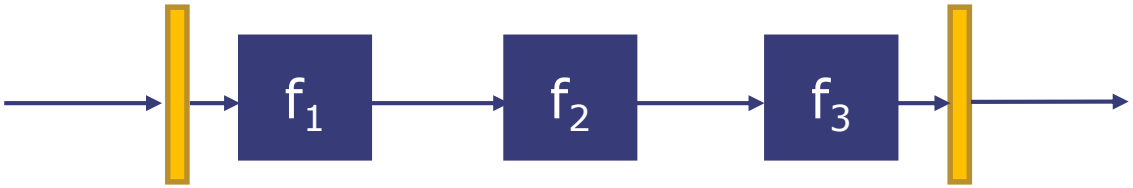

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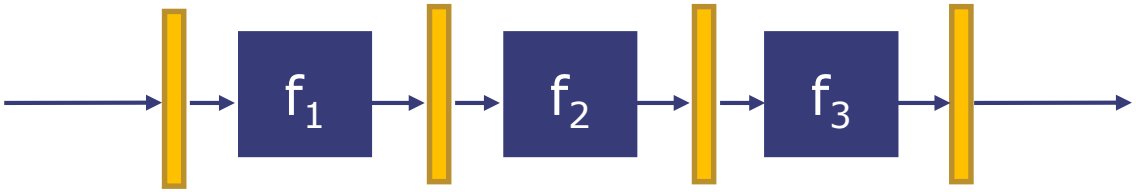

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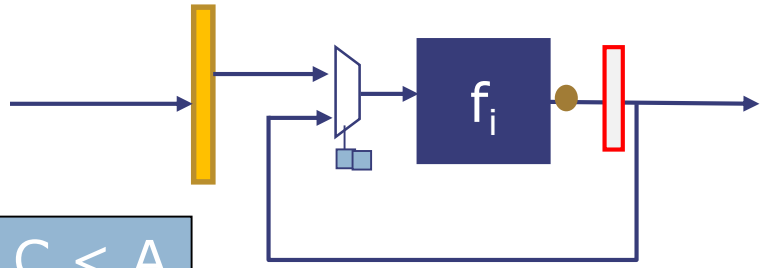

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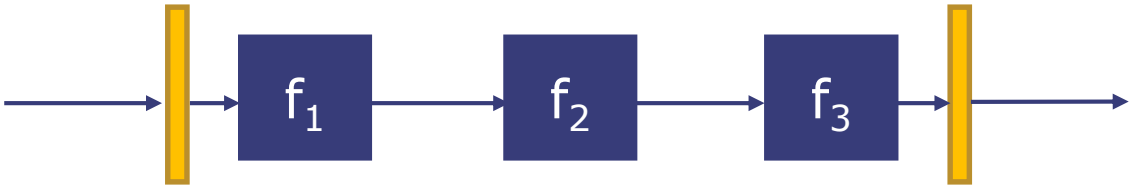

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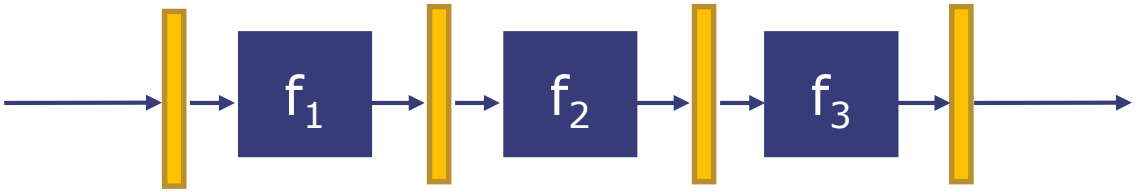

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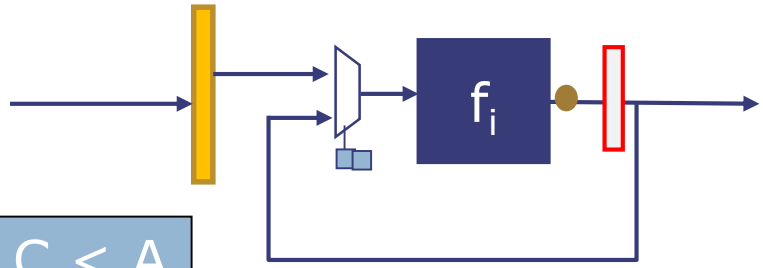

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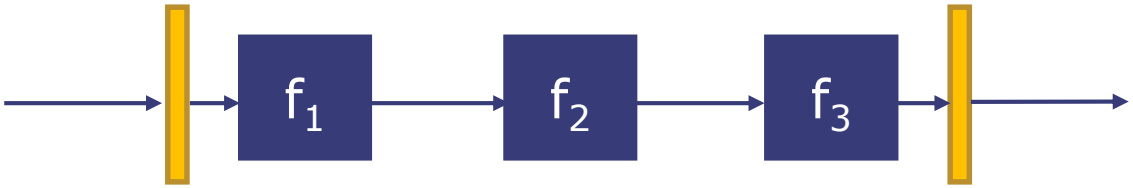

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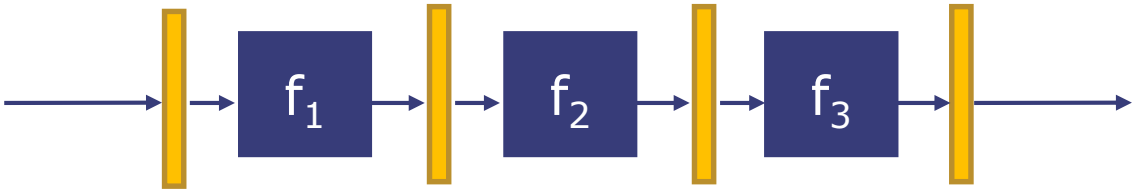

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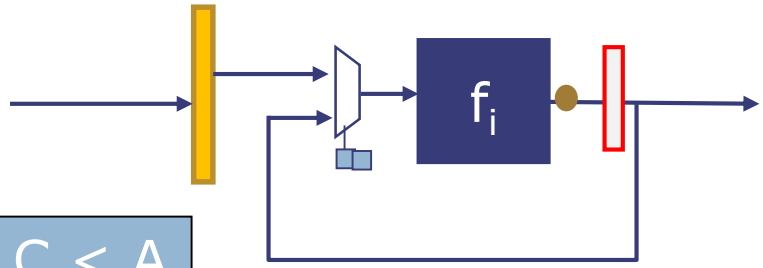

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Thank You!

Next Lecture:
Design Tradeoffs in Sequential Circuits