Modern Processor Architecture

Lecture Goals

- Learn about the key techniques that modern processors use to achieve high performance

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- Emphasize the techniques that may help you in the design project (e.g., simple branch prediction)

Reminder: Processor Performance

$$\frac{\text{Time}}{\text{Program}} = \frac{\text{Instructions}}{\text{Program}} \cdot \frac{\text{Cycles}}{\text{Instruction}} \cdot \frac{\text{Time}}{\text{Cycle}}$$

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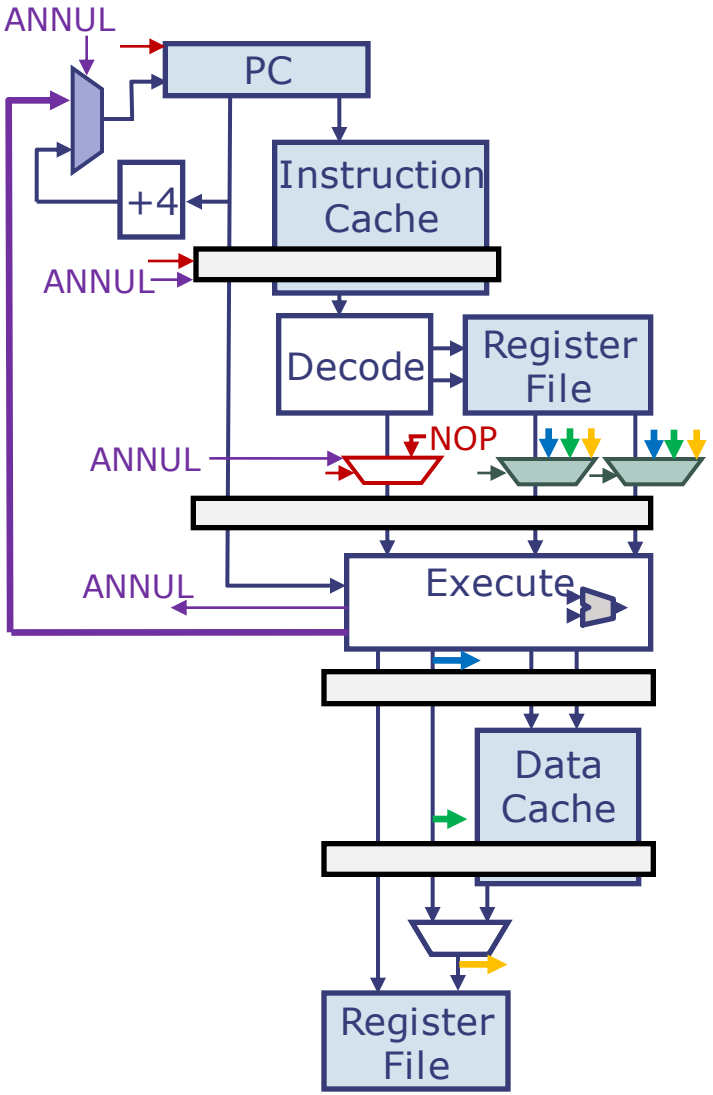
- CPI_{hazard} contributors
  - Data hazards: long operations, cache misses
  - Control hazards: branches, jumps, exceptions

Standard 5-Stage Pipeline

- Assume full bypassing



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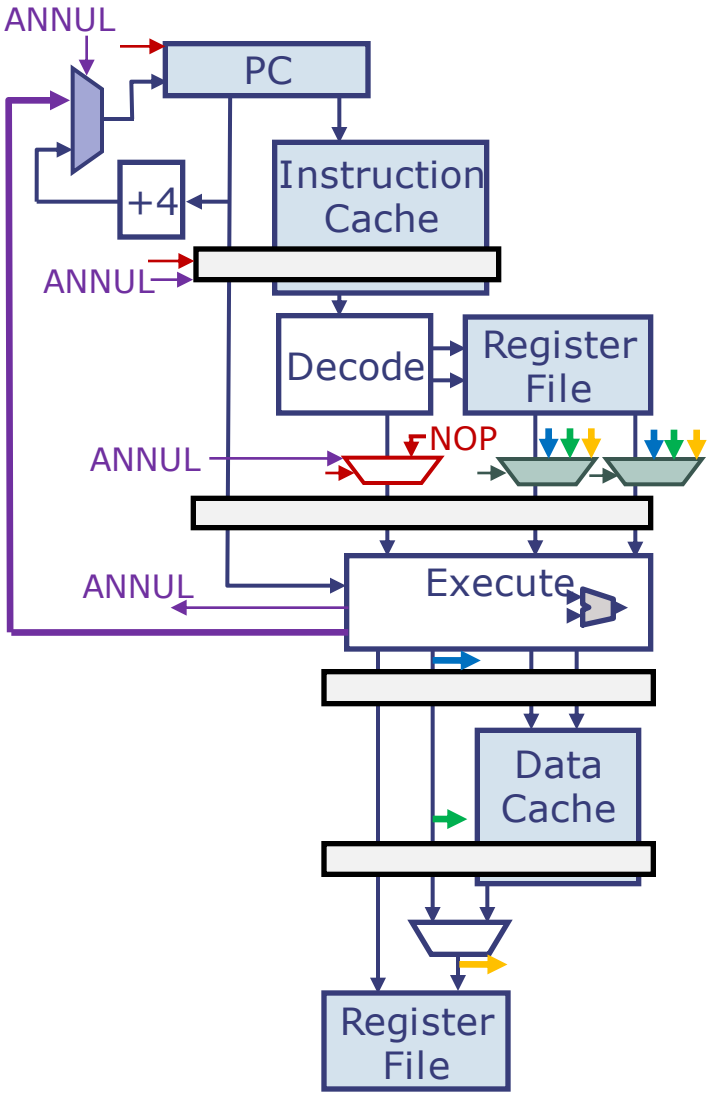

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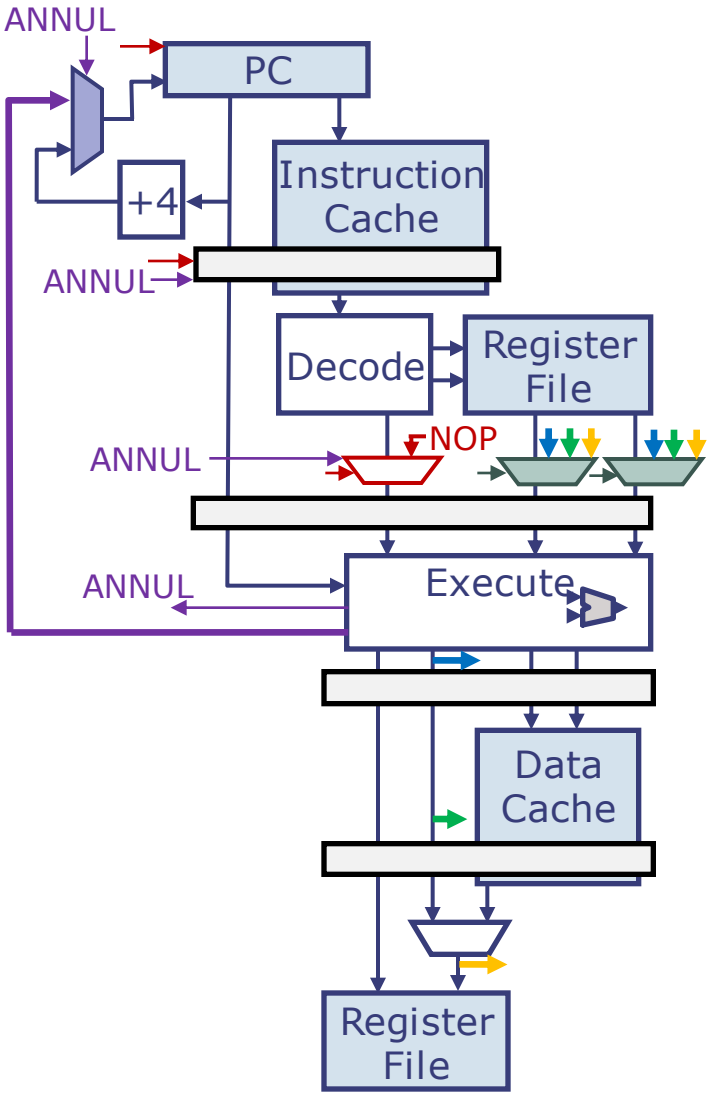

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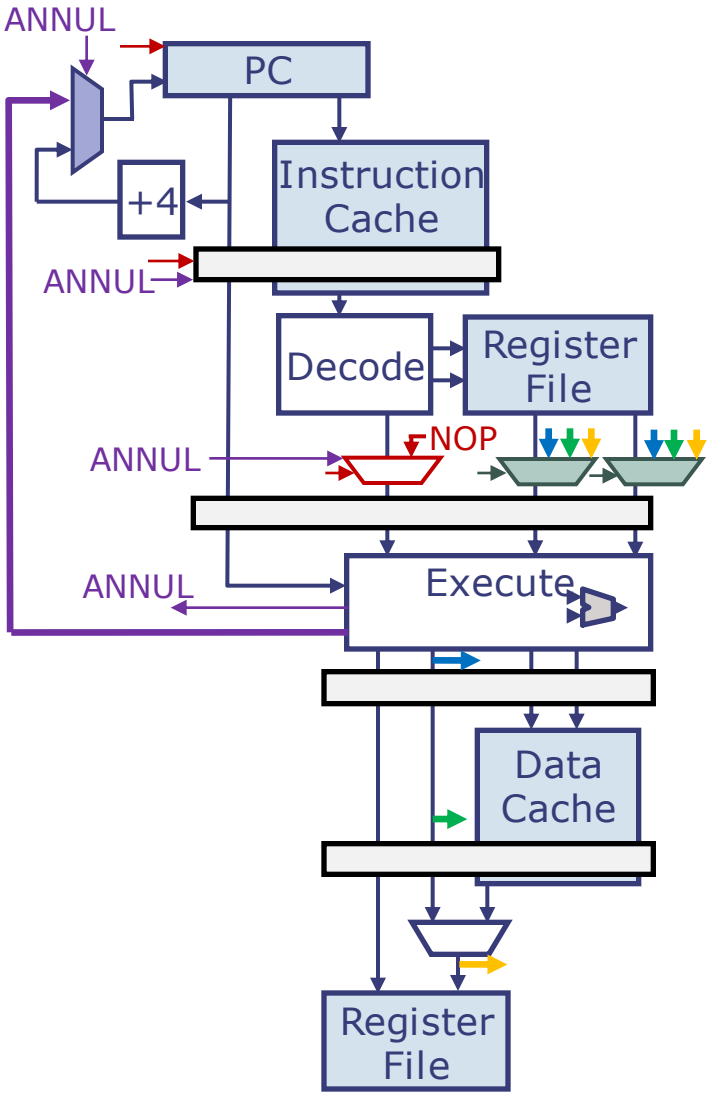

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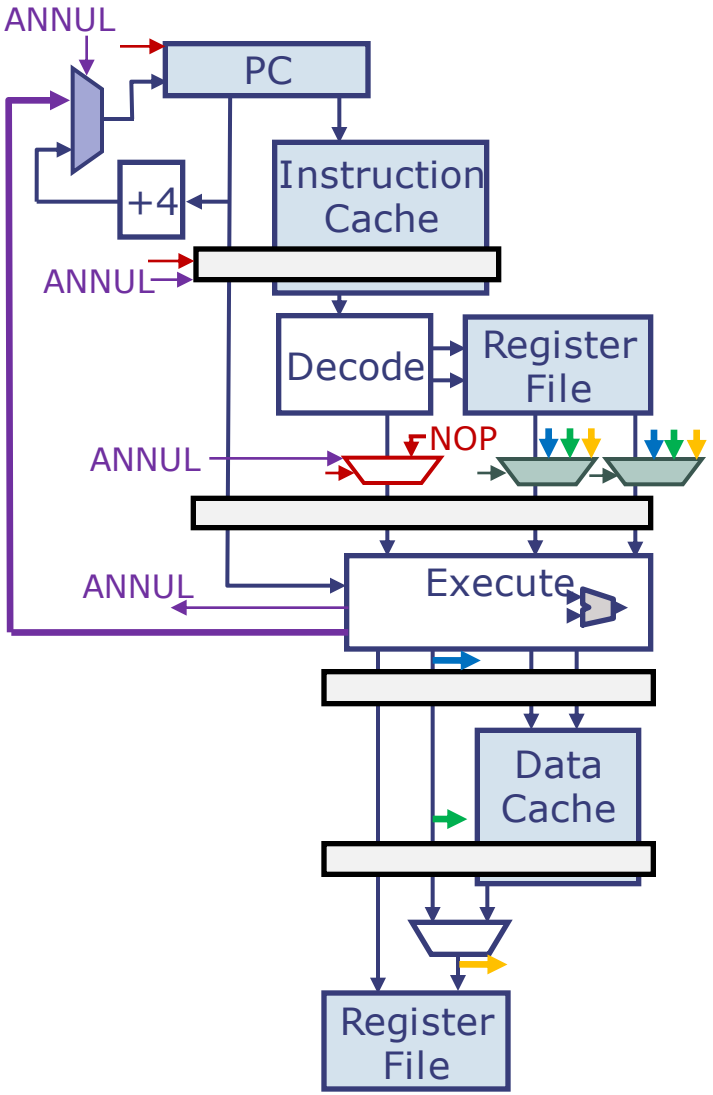

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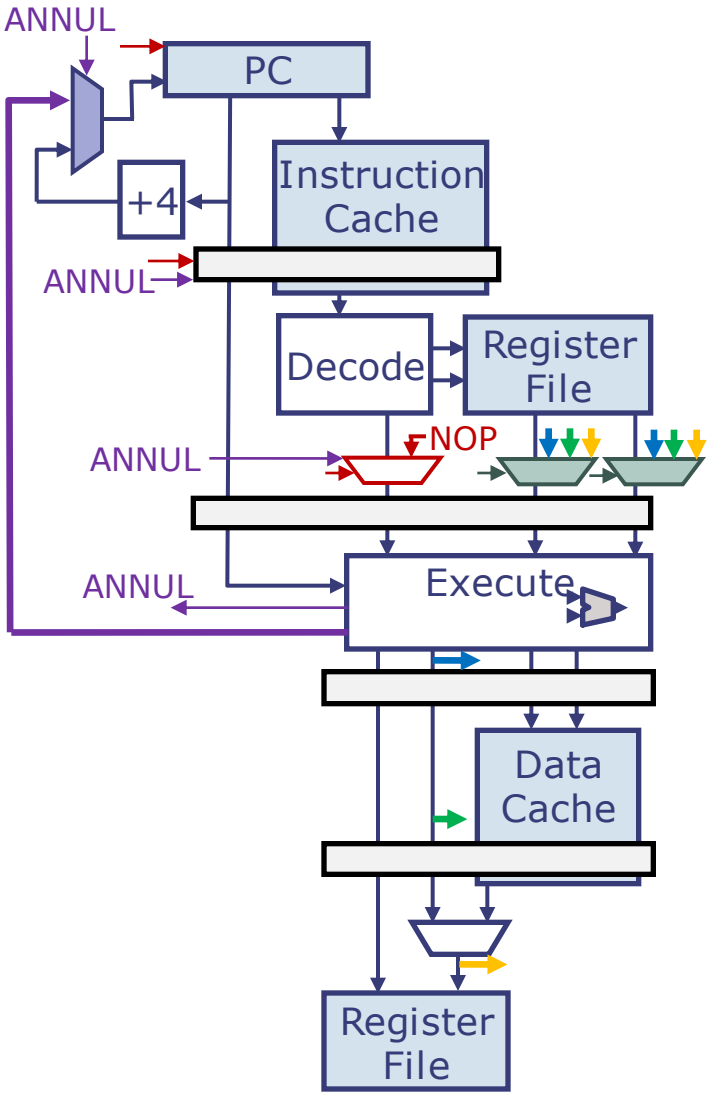

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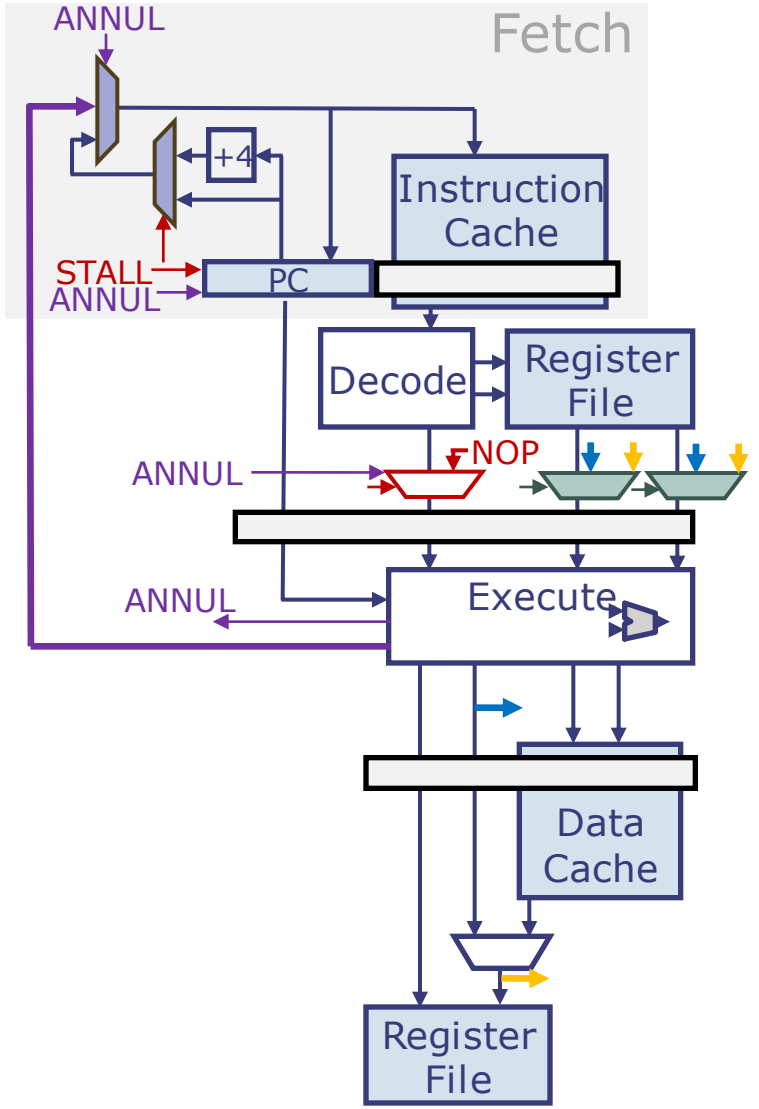

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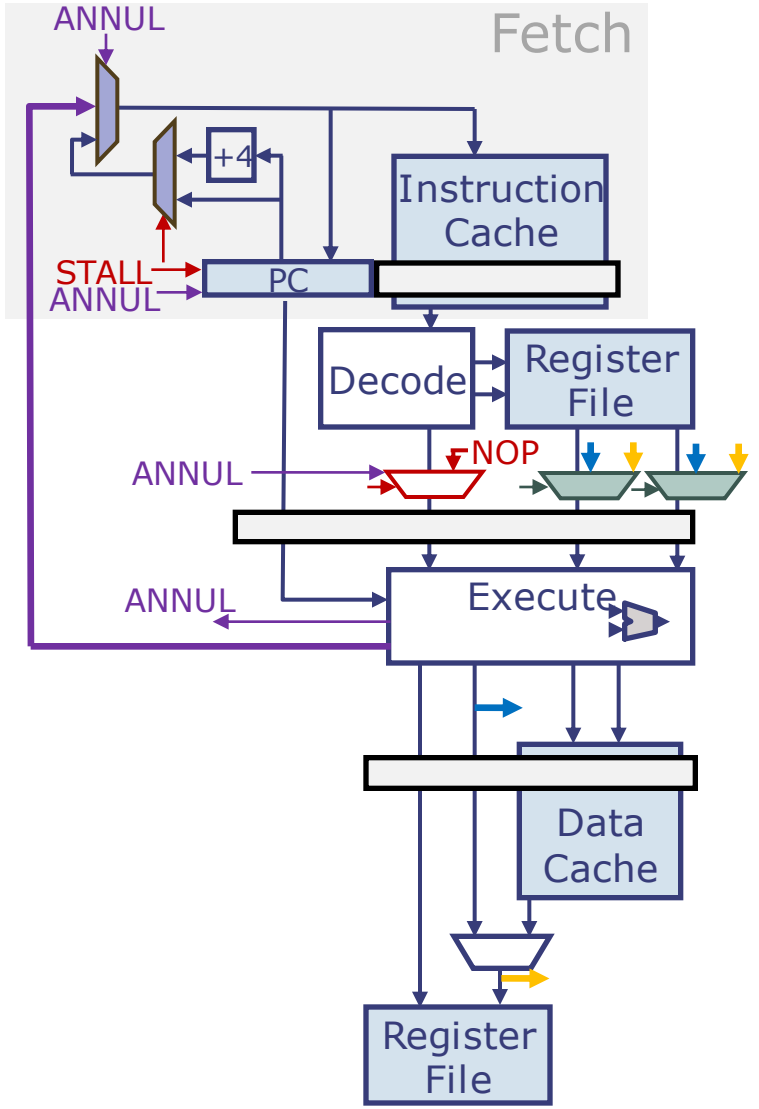

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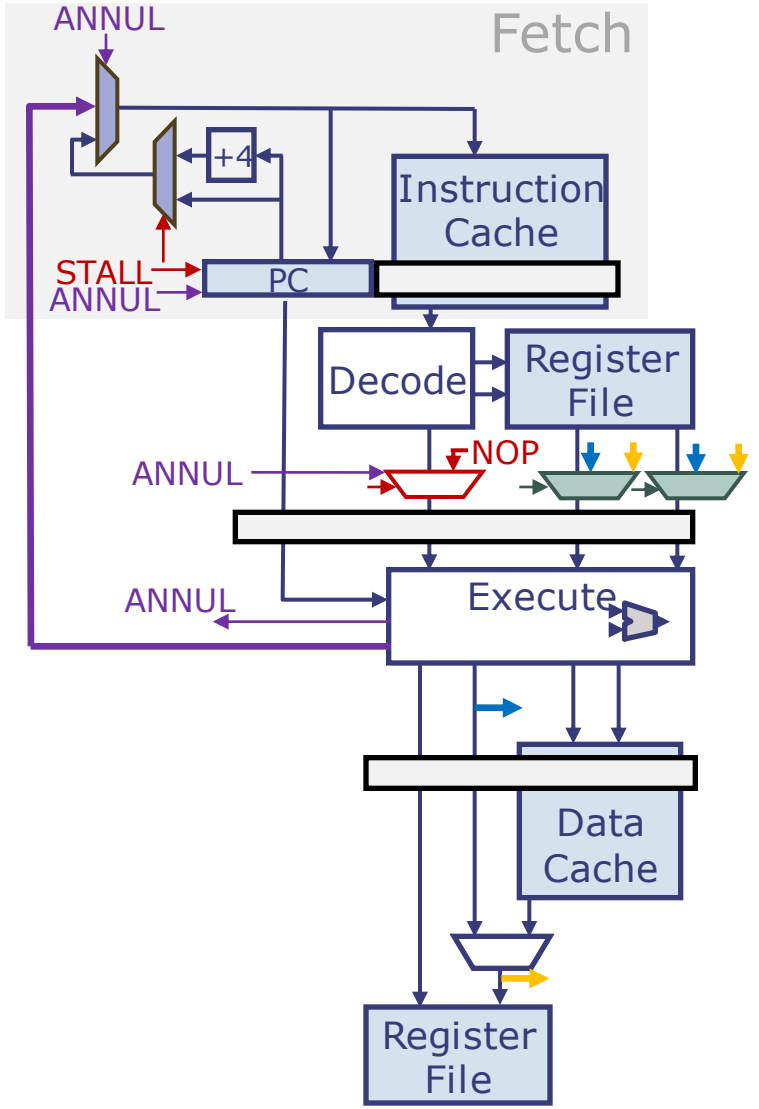

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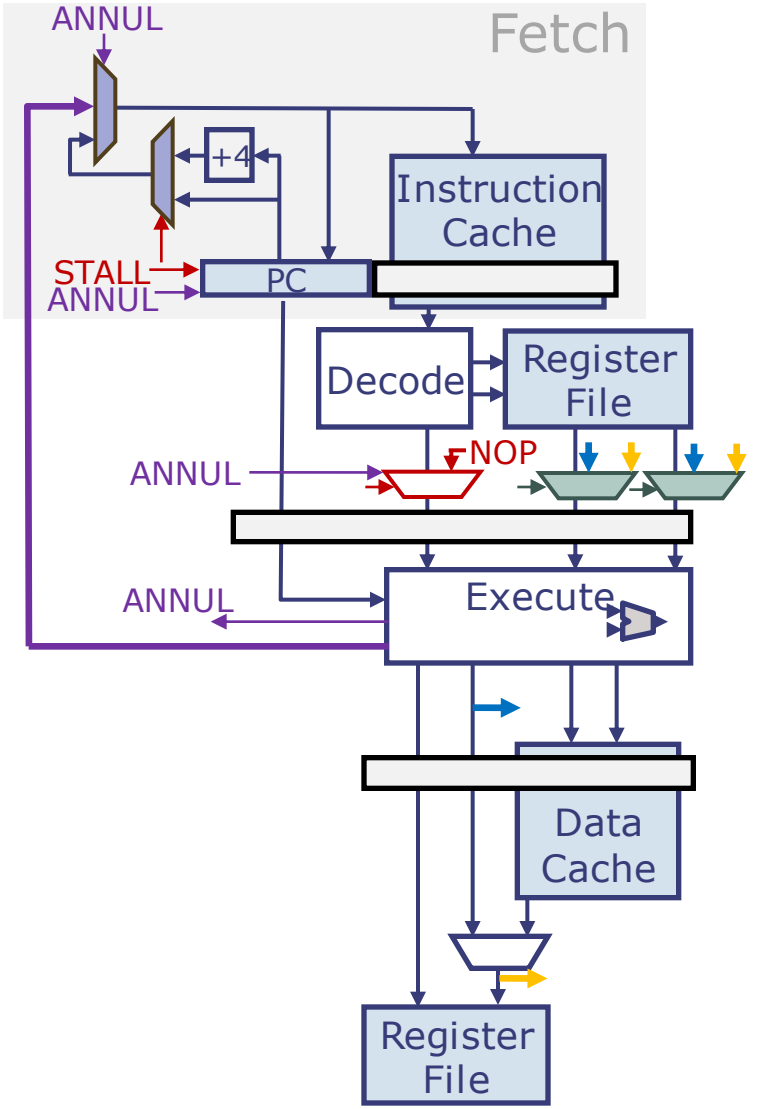

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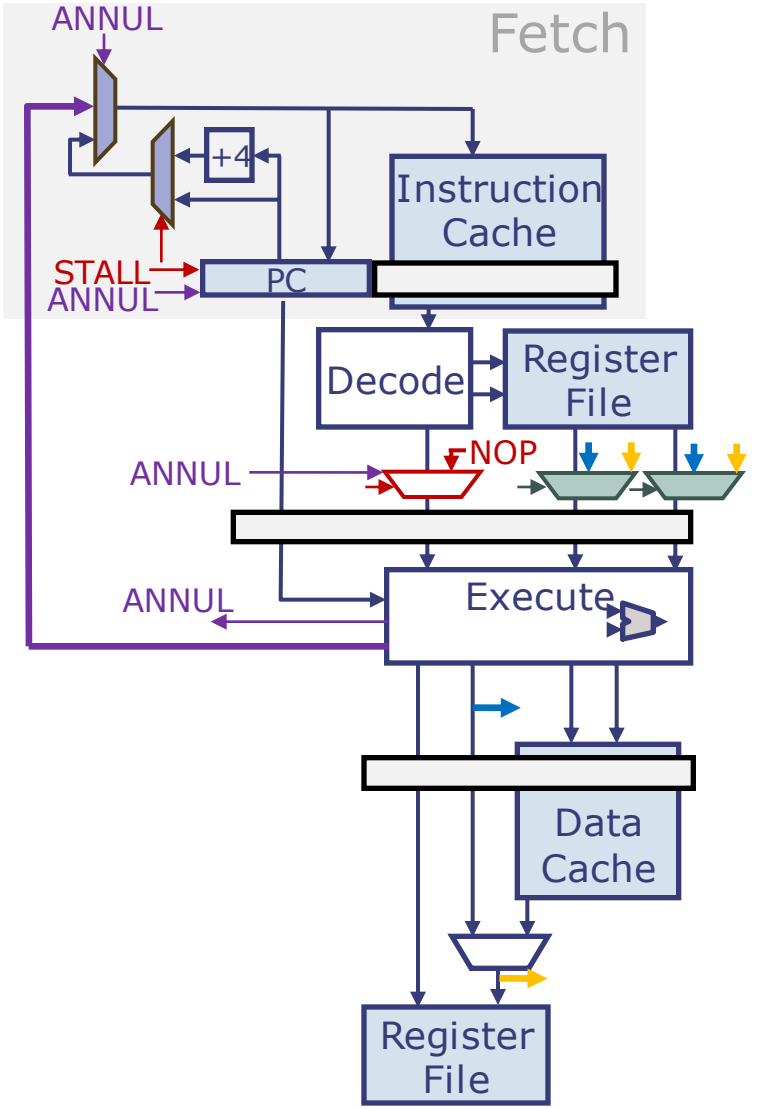

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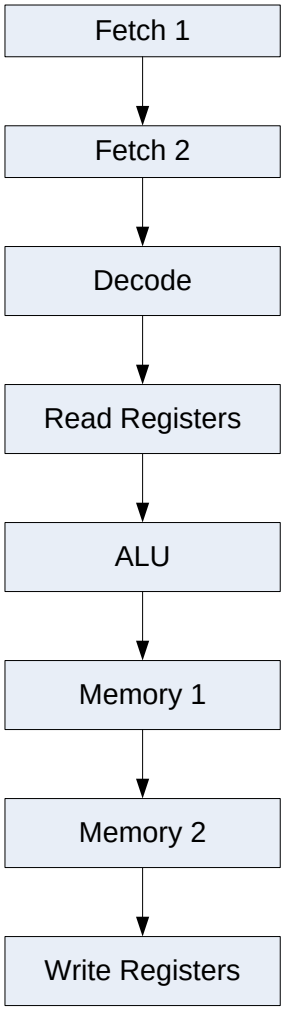
- Reduce impact of control hazards: branch prediction
  - Predict both direction and target of branches and jumps

Deeper Pipelines



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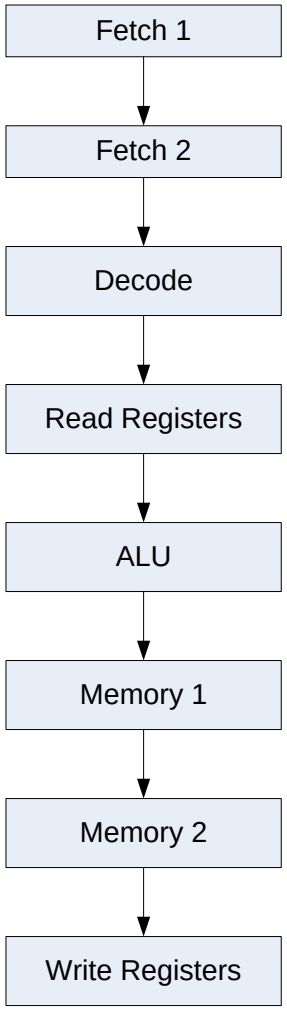

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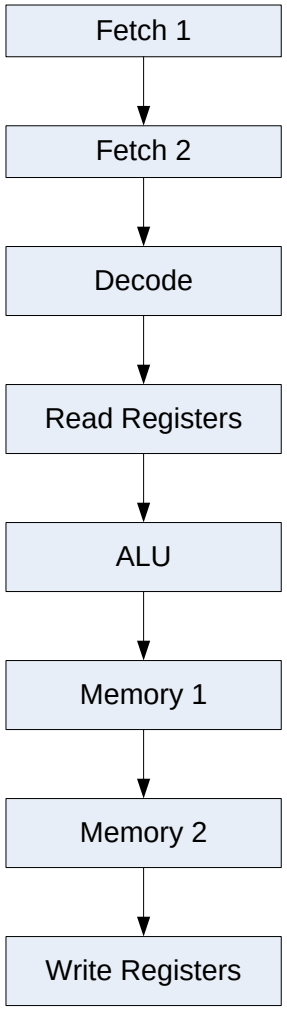

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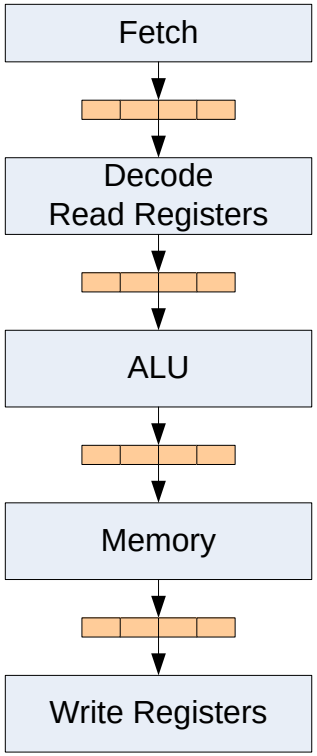
- Disadvantages
  - More overlapping ⇒ more dependencies
    - CPI_{hazard} grows due to data and control hazards
  - Pipeline registers add area & power

Wider (aka Superscalar) Pipelines

- Each stage operates on up to W instructions each clock cycle



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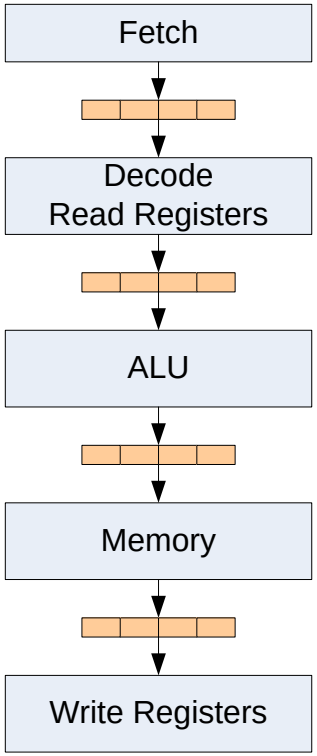

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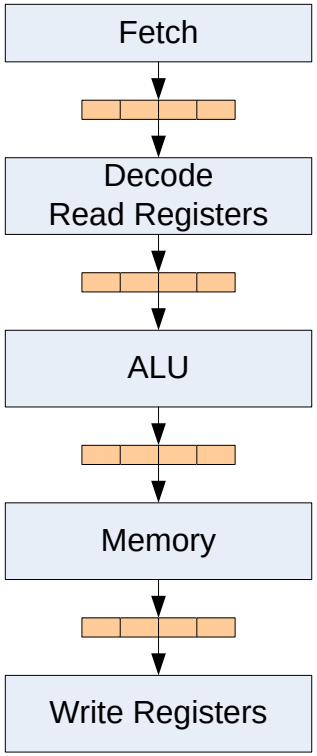

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  - Parallel execution ⇒ more dependencies
    - CPI_{hazard} grows due to data and control hazards
  - Much higher cost & complexity
    - More ALUs, register file ports, …
    - Many bypass & stall cases to check

Resolving Hazards

- Strategy 1: Stall. Wait for the result to be available by freezing earlier pipeline stages
- Strategy 2: Bypass. Route data to the earlier pipeline stage as soon as it is calculated
- Strategy 3: Speculate
  - Guess a value and continue executing anyway
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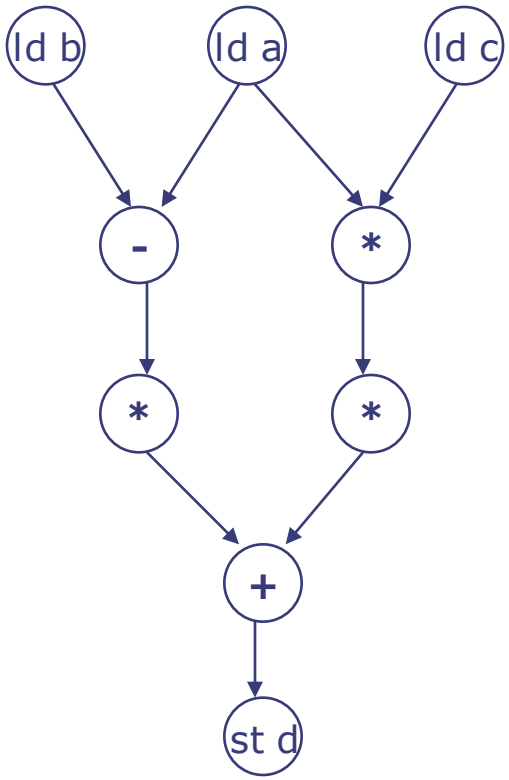

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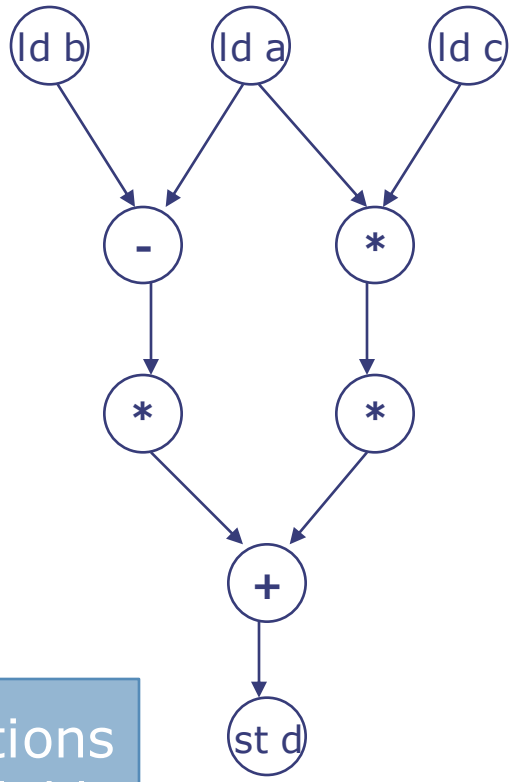

Out-of-order execution runs instructions as soon as their inputs become available

Out-of-Order Execution Example

- If `ld b` takes a few cycles (e.g., cache miss), can execute instructions that do not depend on b

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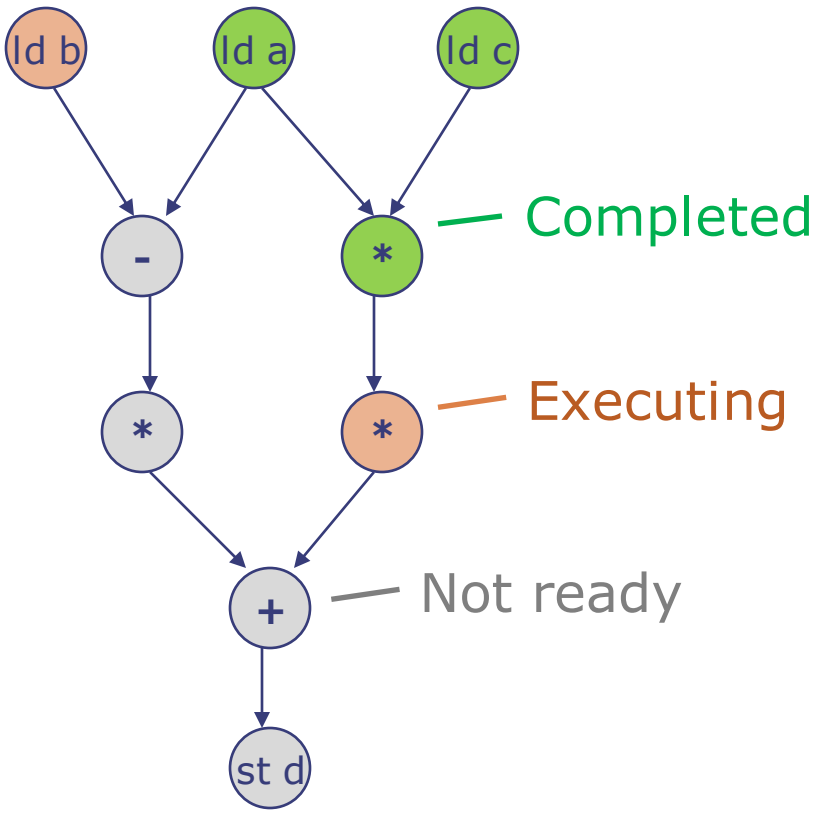

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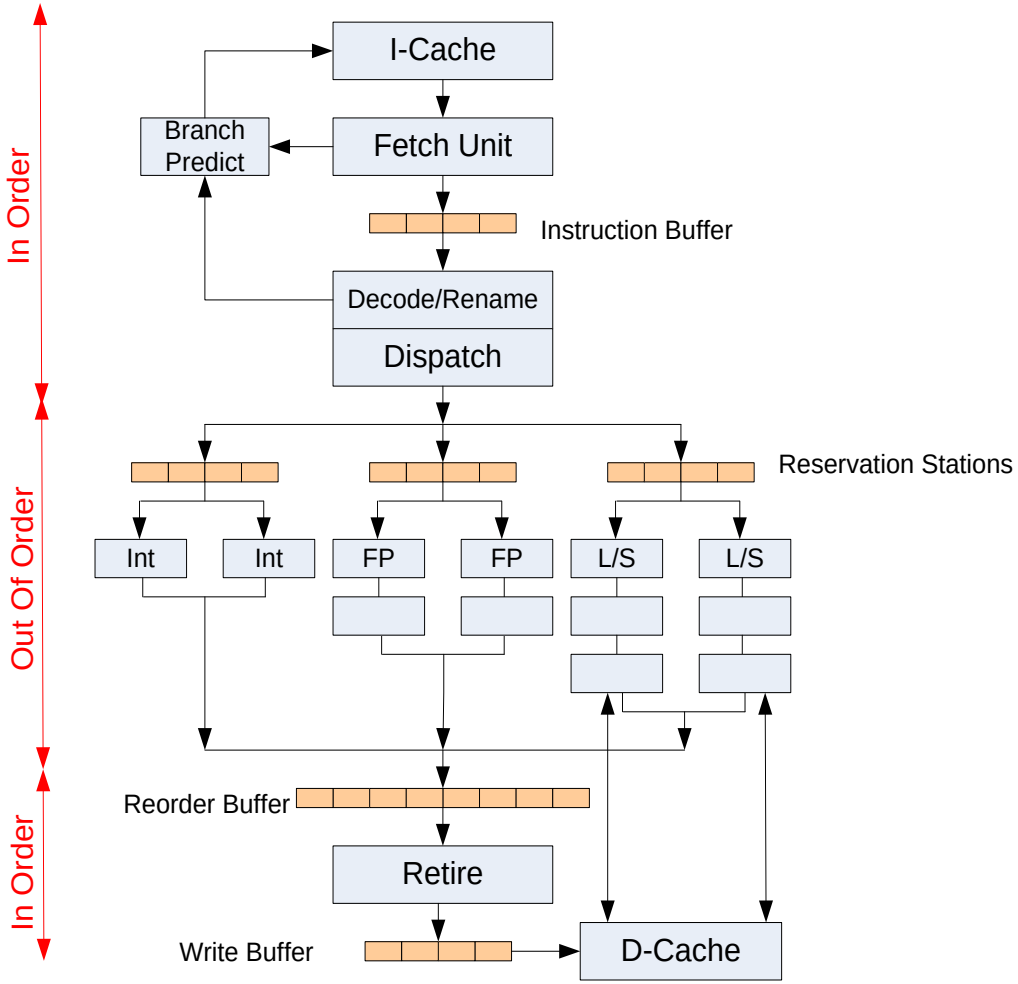

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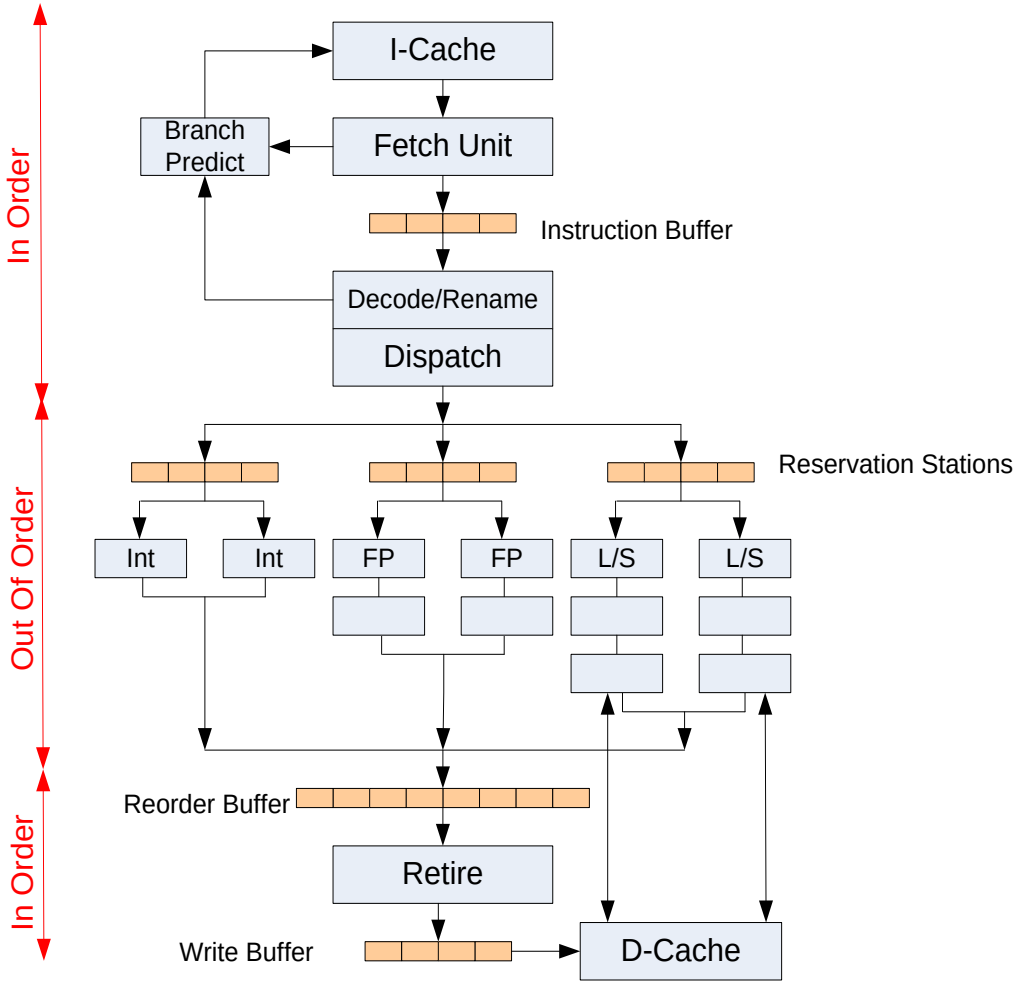

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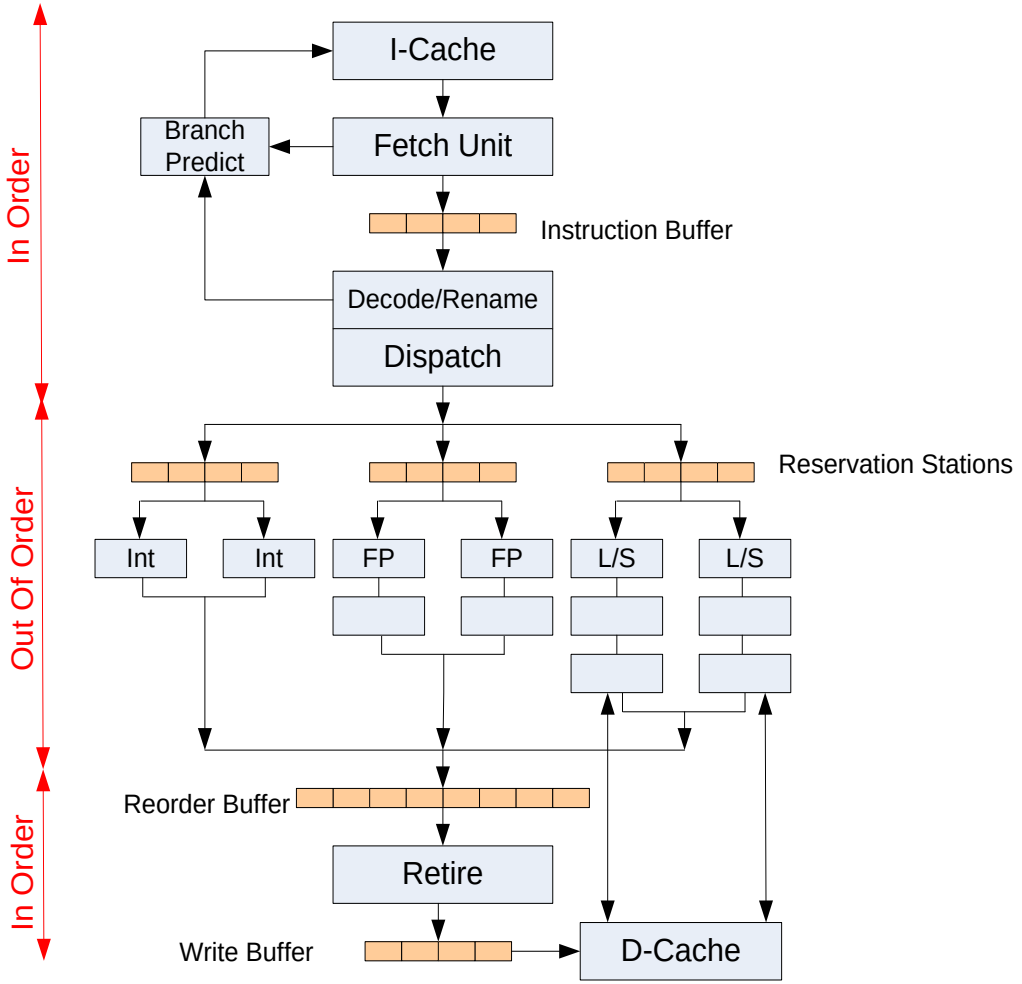

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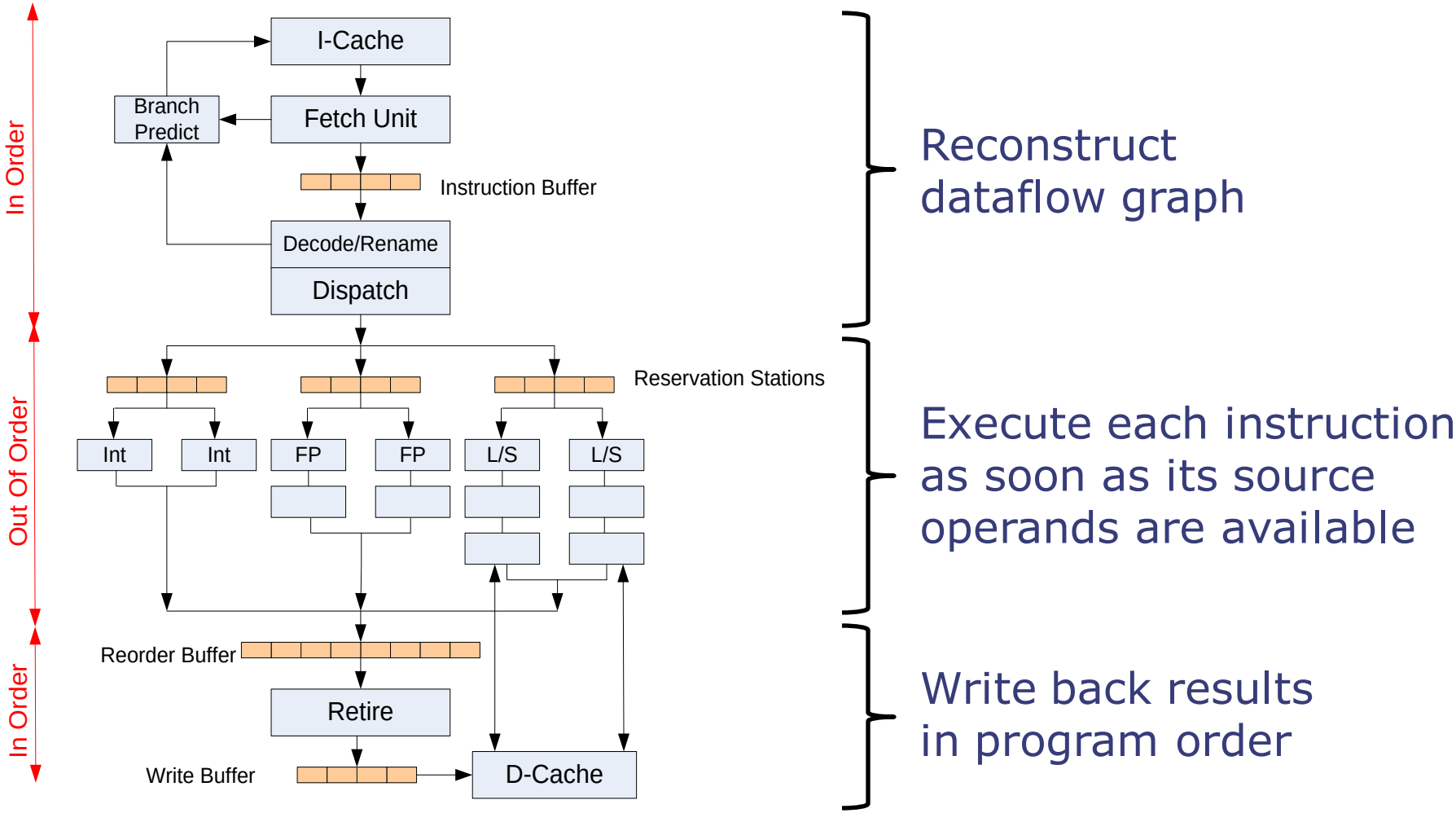

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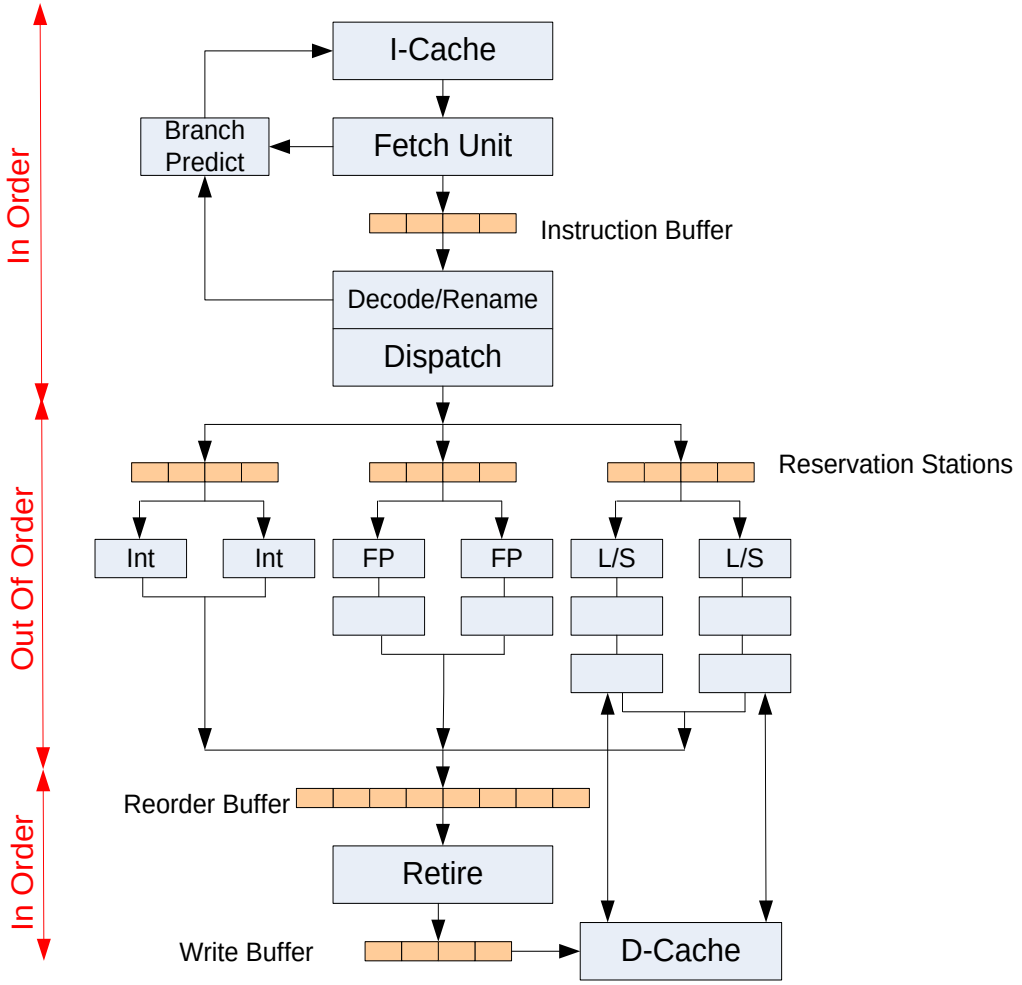

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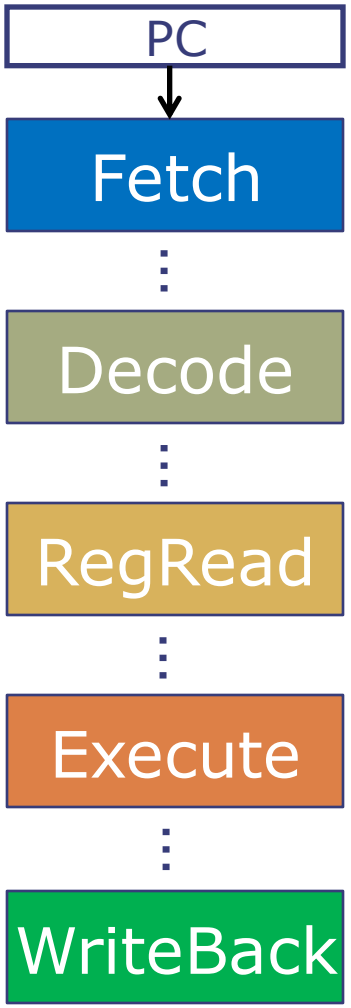
Write back results in program order

Why is this needed?

Control Hazard Penalty

- Modern processors have >10 pipeline stages between next PC calculation and branch resolution!



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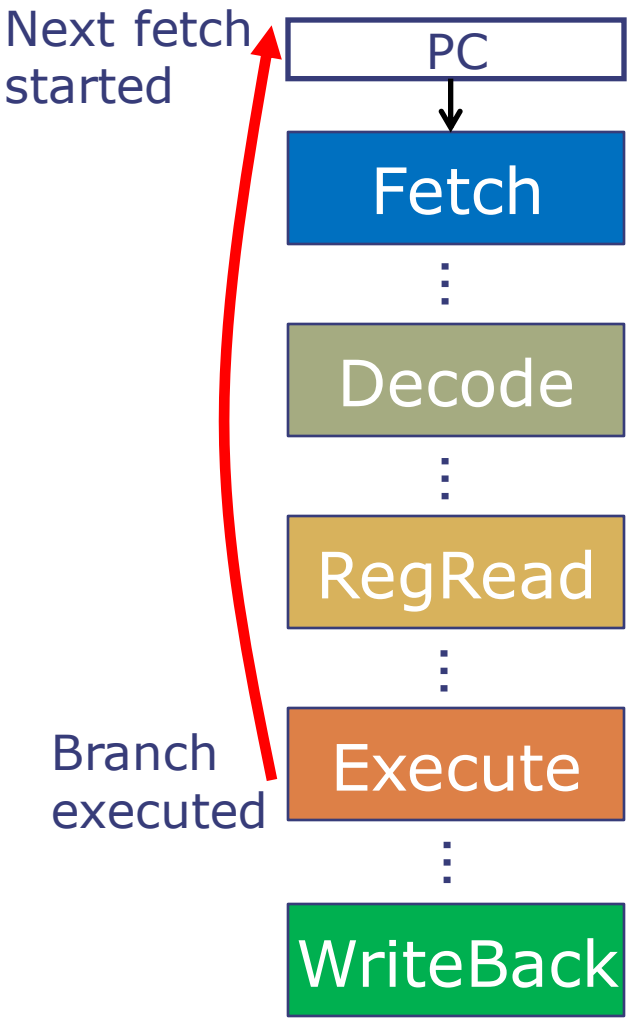

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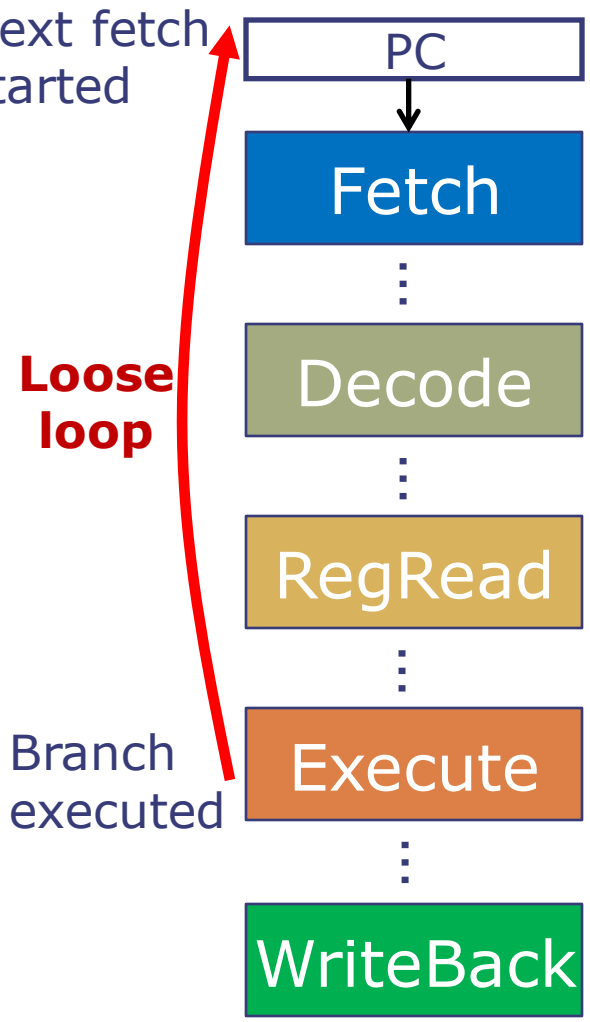

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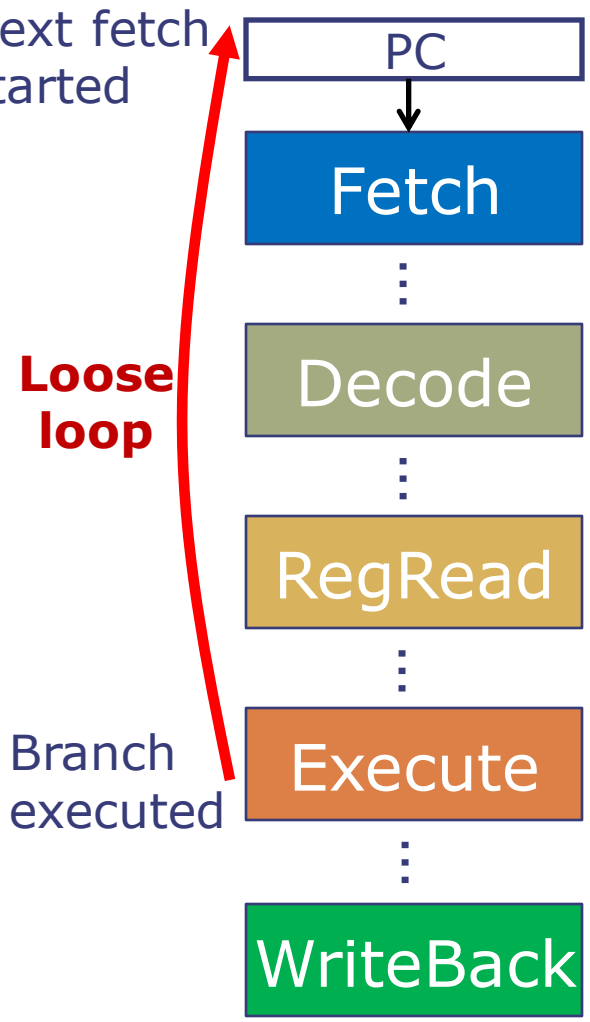

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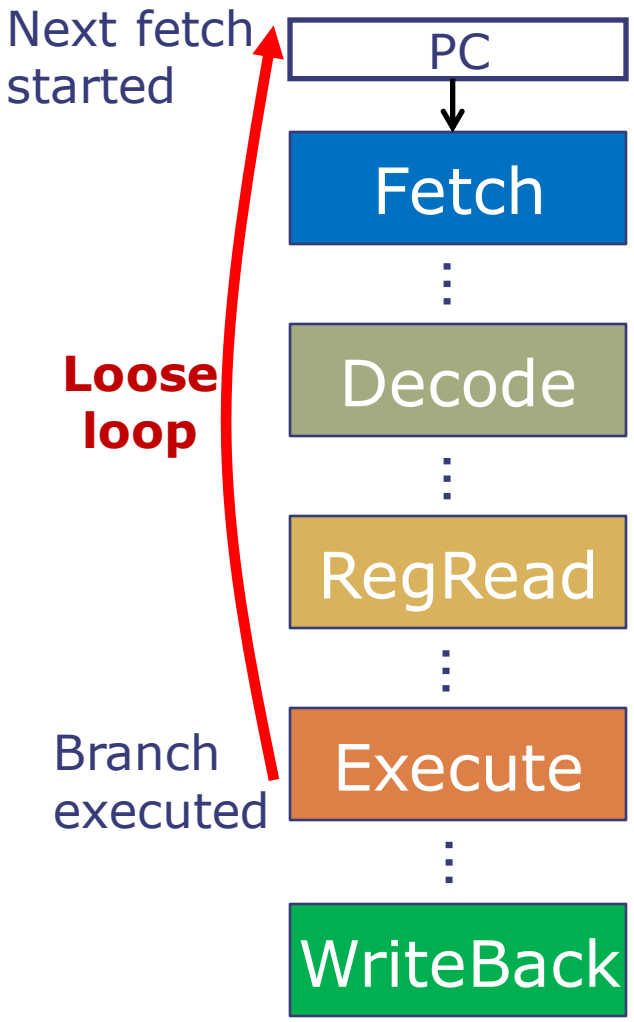

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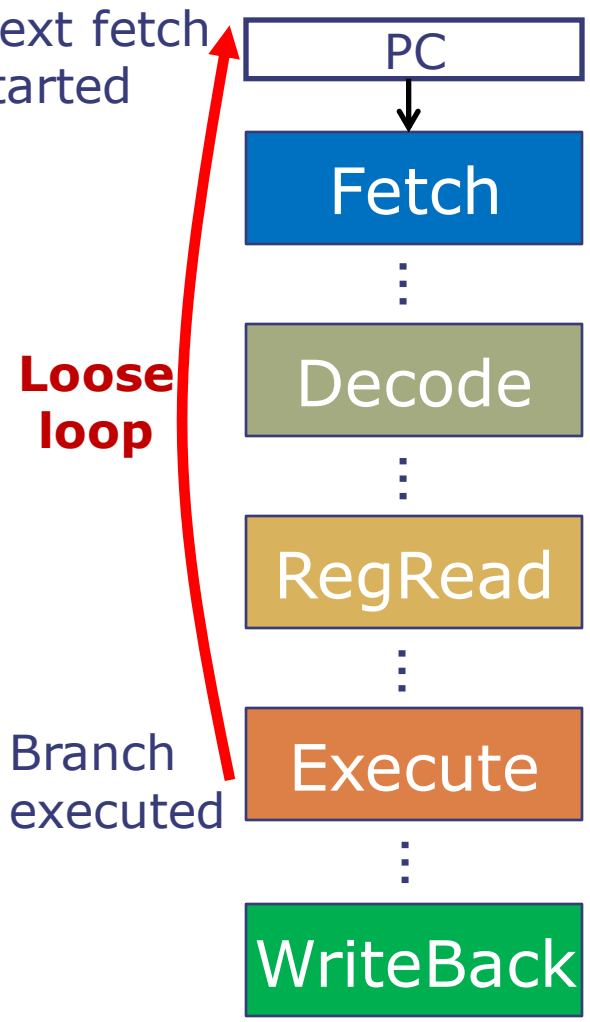
- One branch every 5-20 instructions… performance impact of mispredictions?



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  1) Is the preceding instruction a taken branch or jump?
  2) If so, what is the target address?

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Resolving Hazards

- Strategy 1: Stall. Wait for the result to be available by freezing earlier pipeline stages
- Strategy 2: Bypass. Route data to the earlier pipeline stage as soon as it is calculated
- Strategy 3: Speculate
  - Guess a value and continue executing anyway
  - When actual value is available, two cases
    - Guessed correctly → do nothing
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Predict jump/branch target and direction

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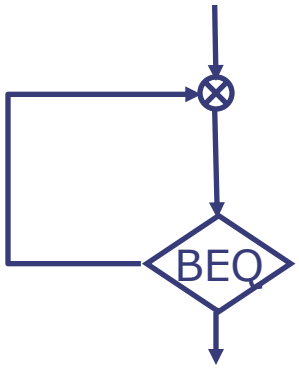
Static Branch Prediction

- Probability a branch is taken is ~60-70%, but:

backward
90%



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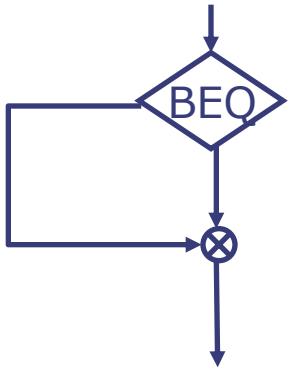
50%



- Some ISAs attach preferred direction hints to branches, e.g., Motorola MC88110
  - bne0 *(preferred taken)* beq0 *(not taken)*
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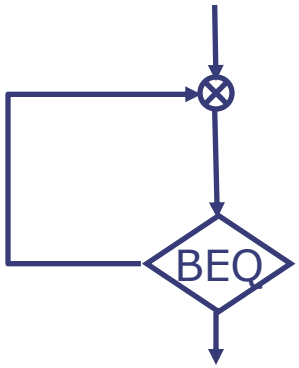

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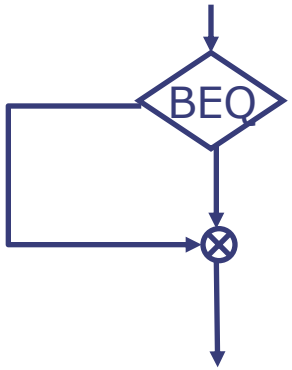

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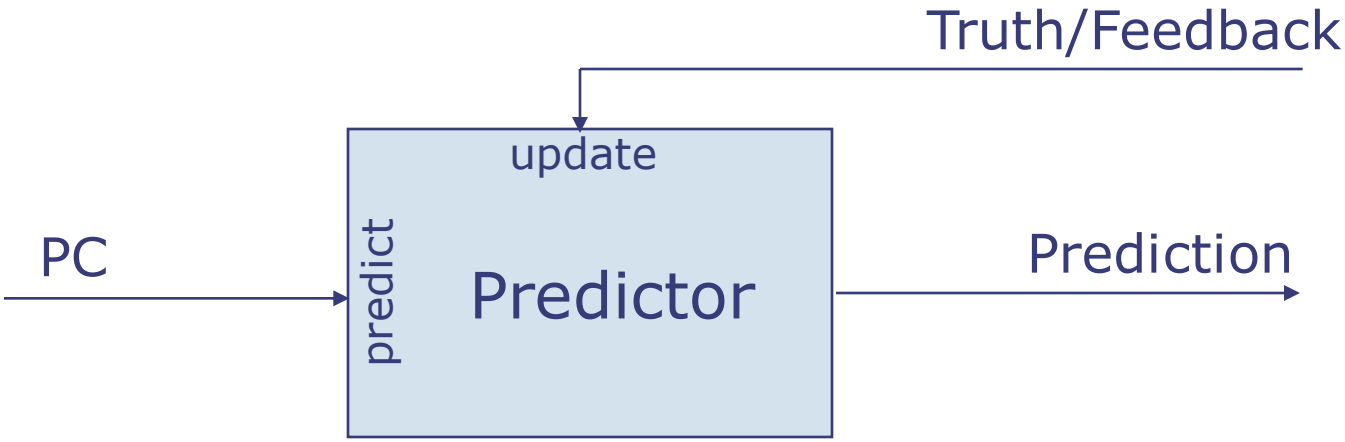
Good way to improve CPI on part 3 of the design project if you use a 4-stage pipeline

Dynamic Branch Prediction

Learning from past behavior



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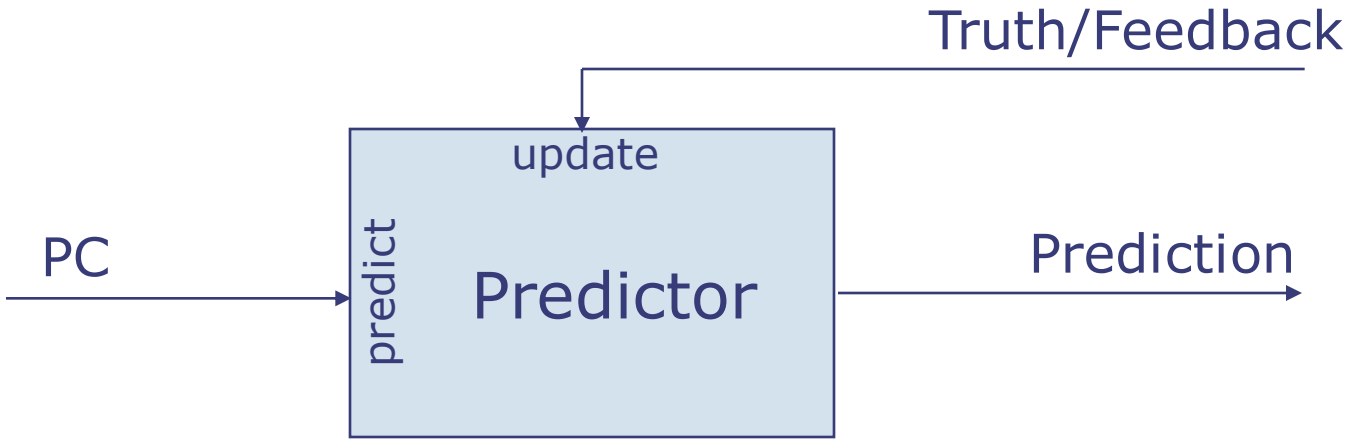

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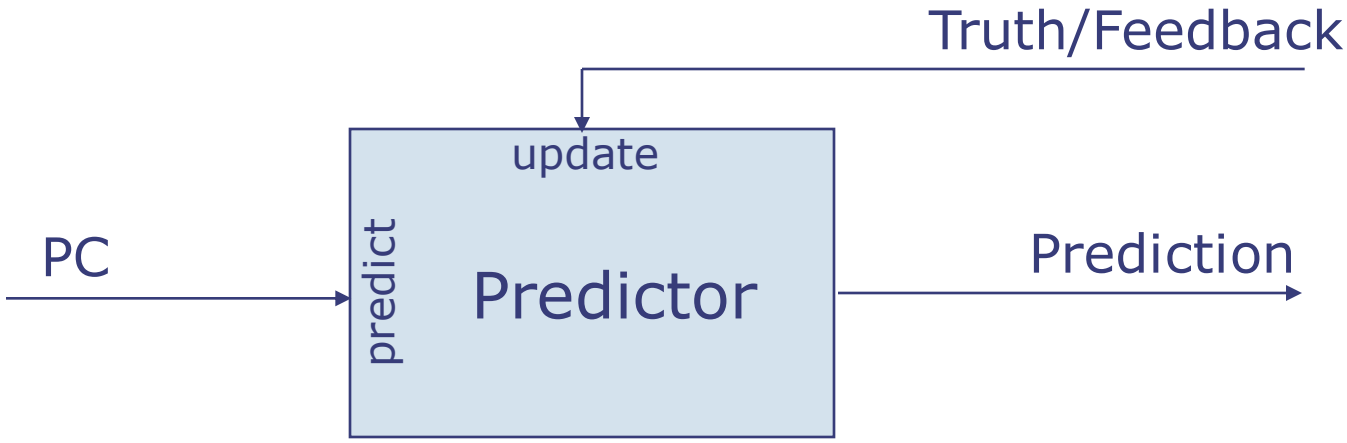
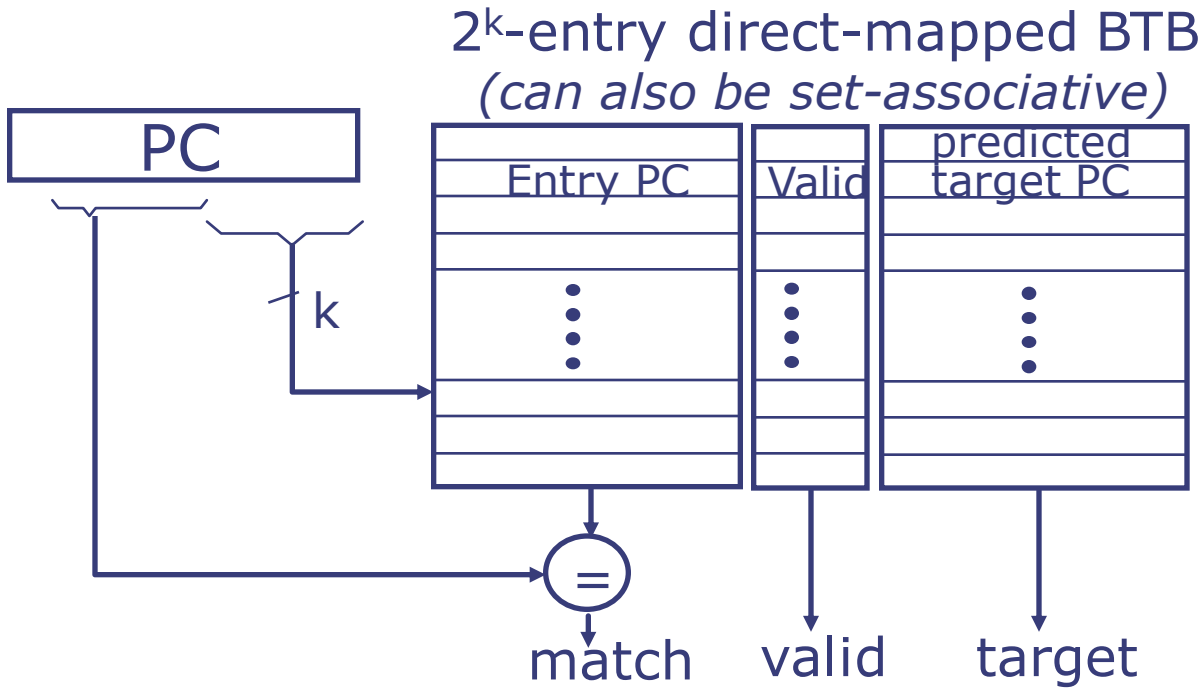


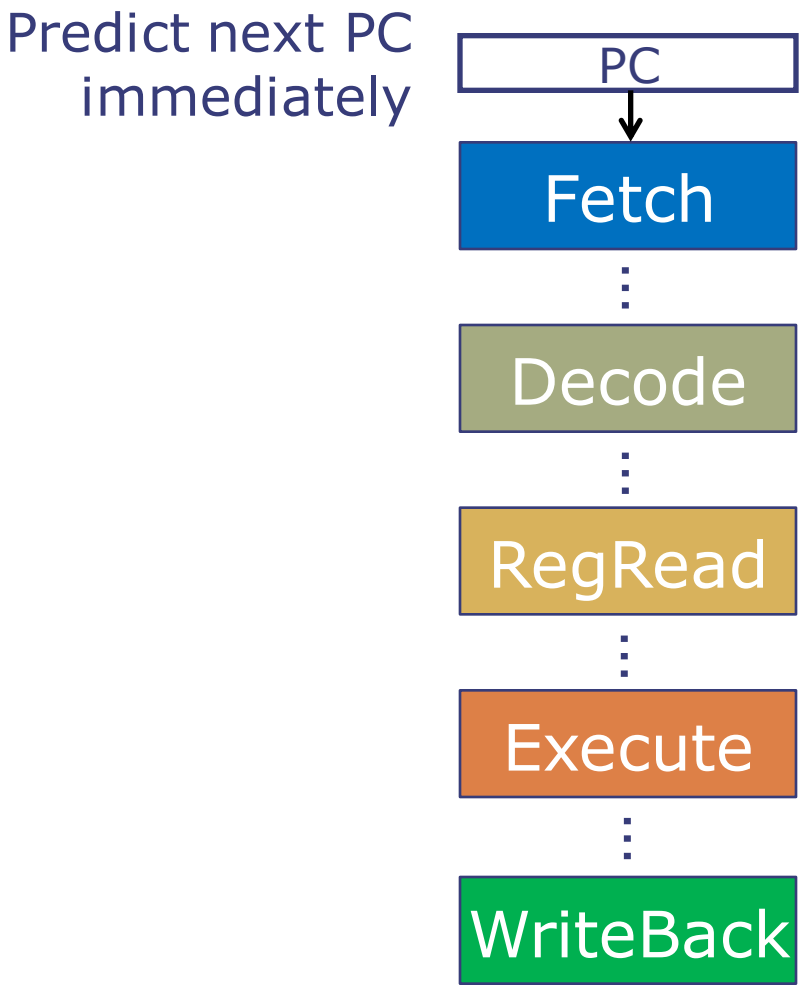
- Temporal correlation
  - The way a branch resolves may be a good predictor of the way it will resolve at the next execution
- Spatial correlation
  - Several branches may resolve in a highly correlated manner (a preferred path of execution)

Predicting the Target Address: Branch Target Buffer (BTB)



- BTB is a cache for targets: Remembers last target PC *for taken branches and jumps*
  - If hit, use stored target as predicted next PC
  - If miss, use PC+4 as predicted next PC
  - After target is known, update if prediction is wrong

Integrating the BTB in the Pipeline



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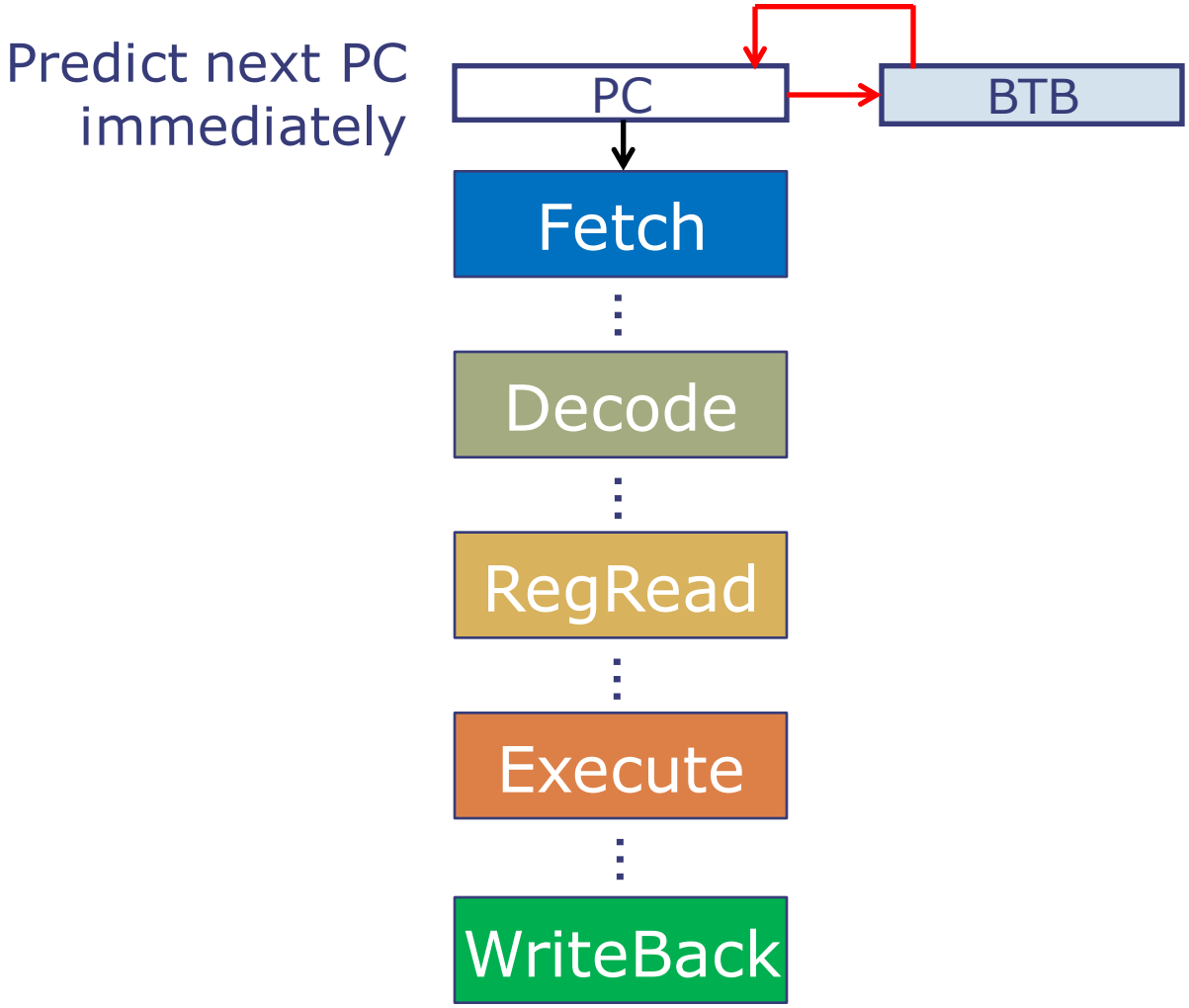

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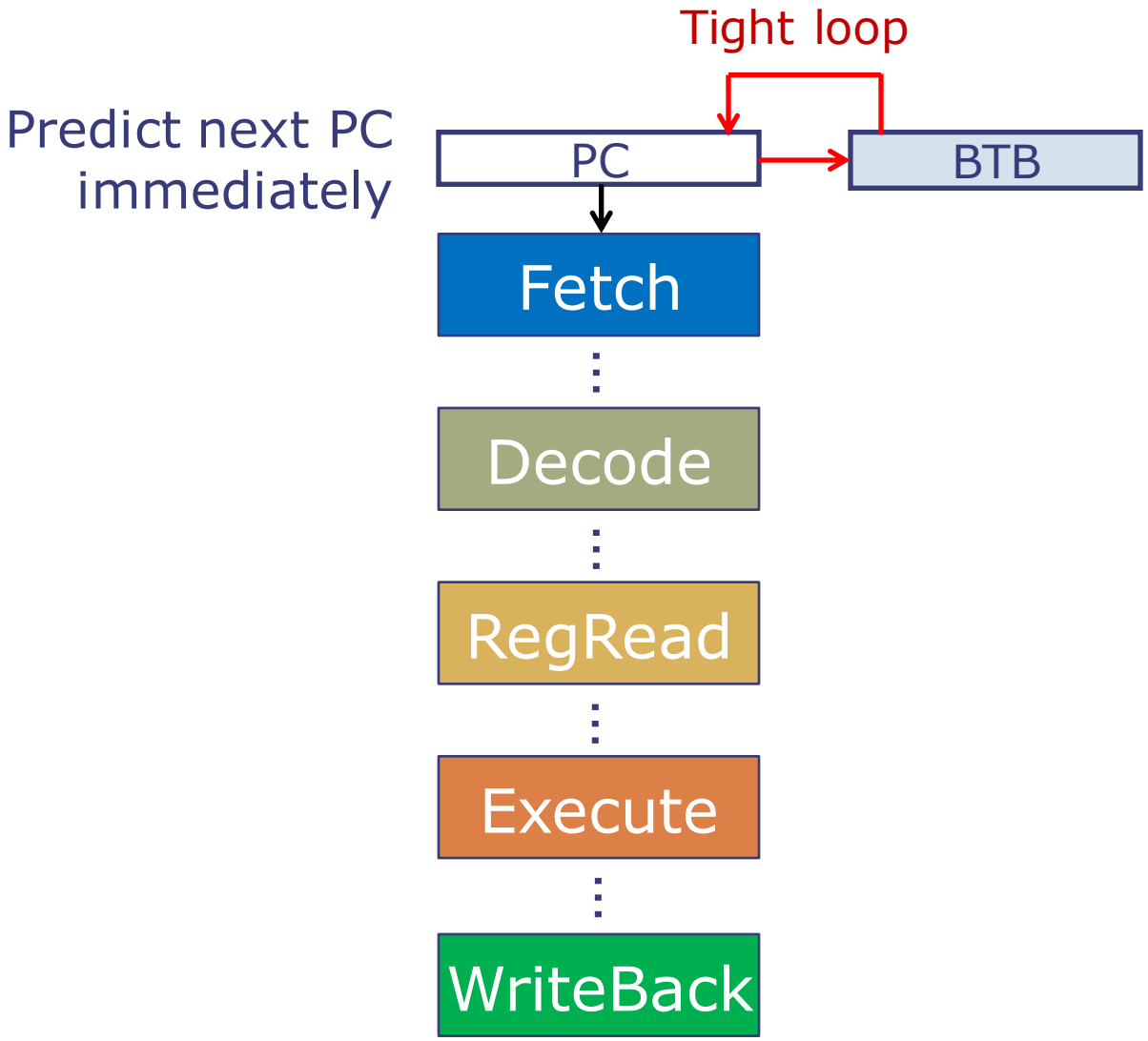

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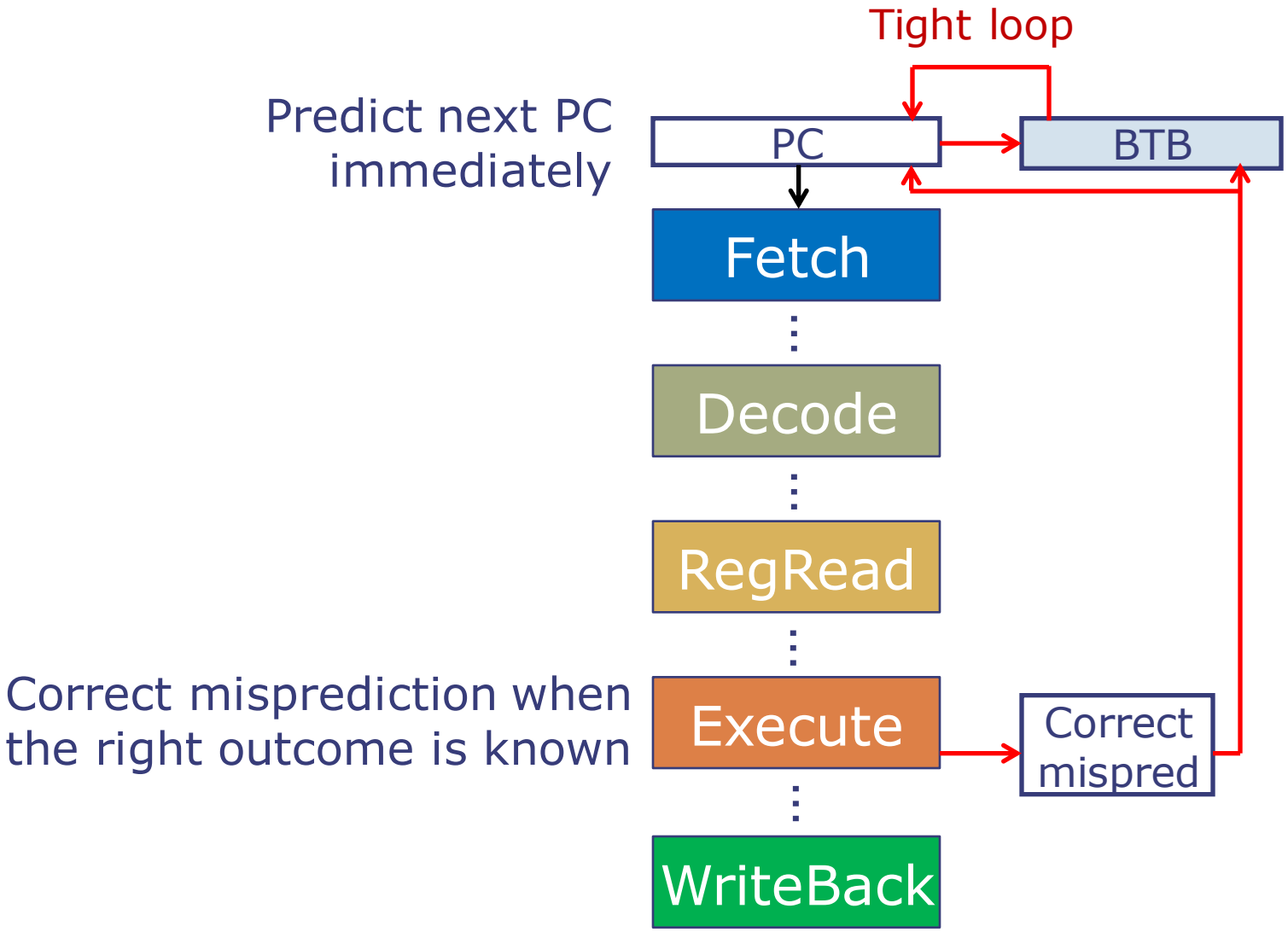

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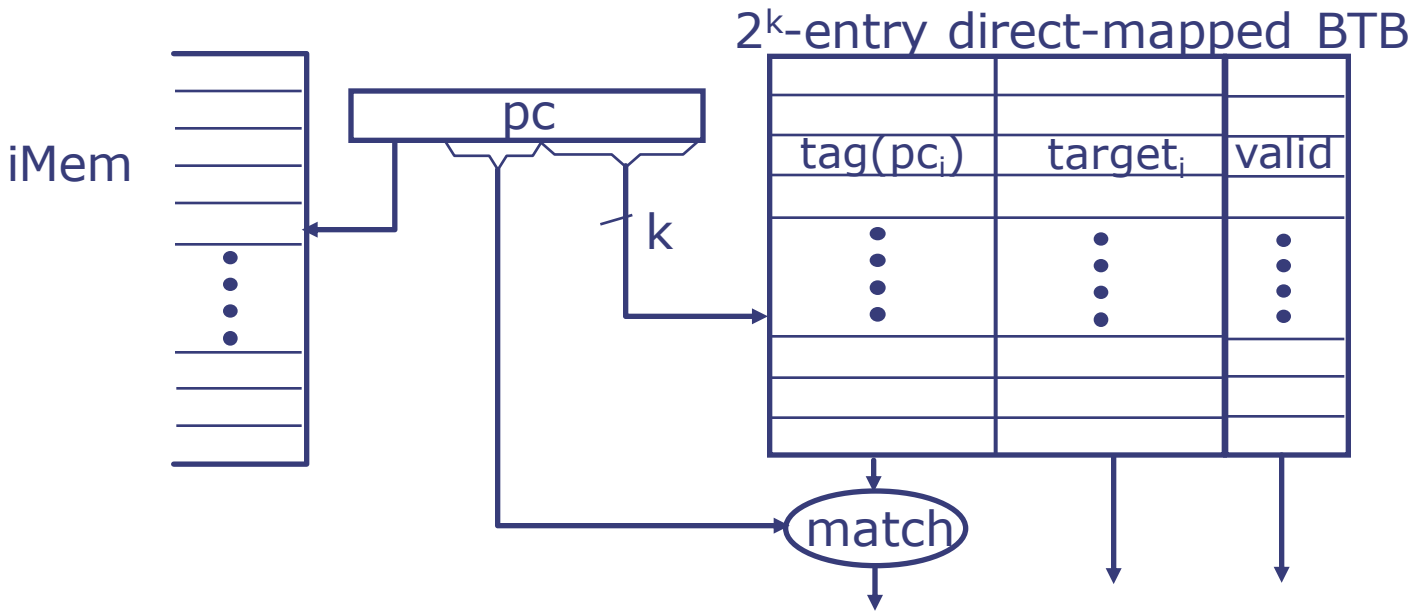

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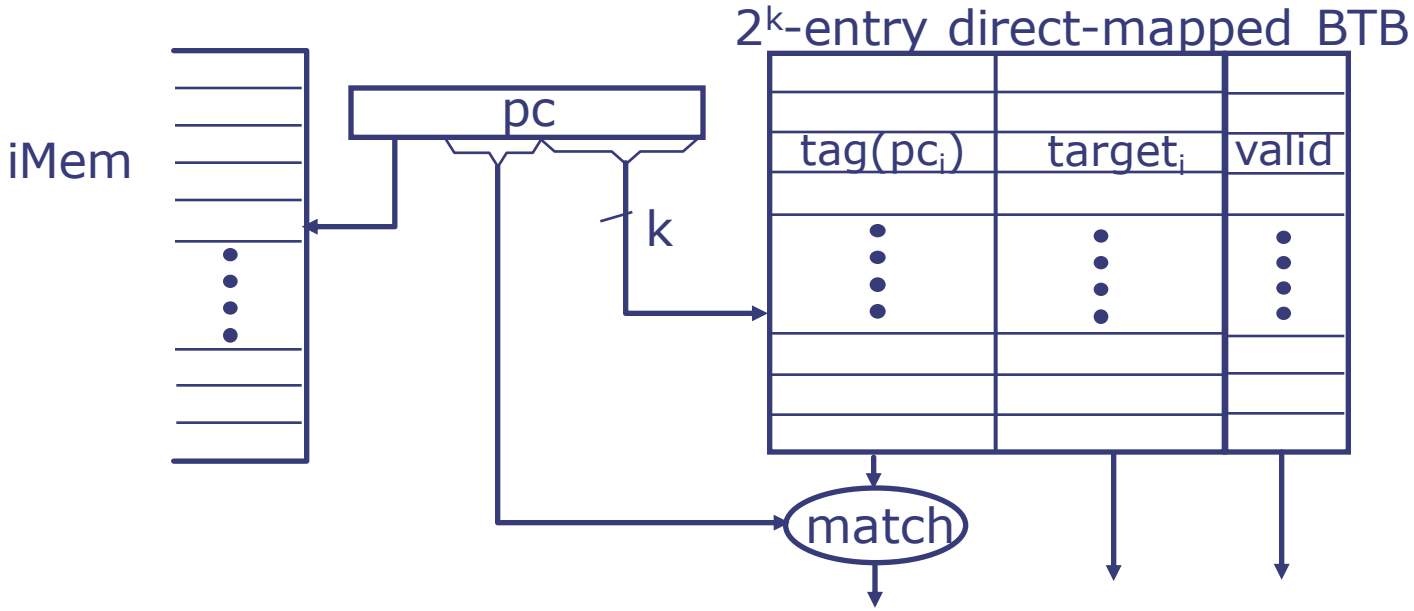

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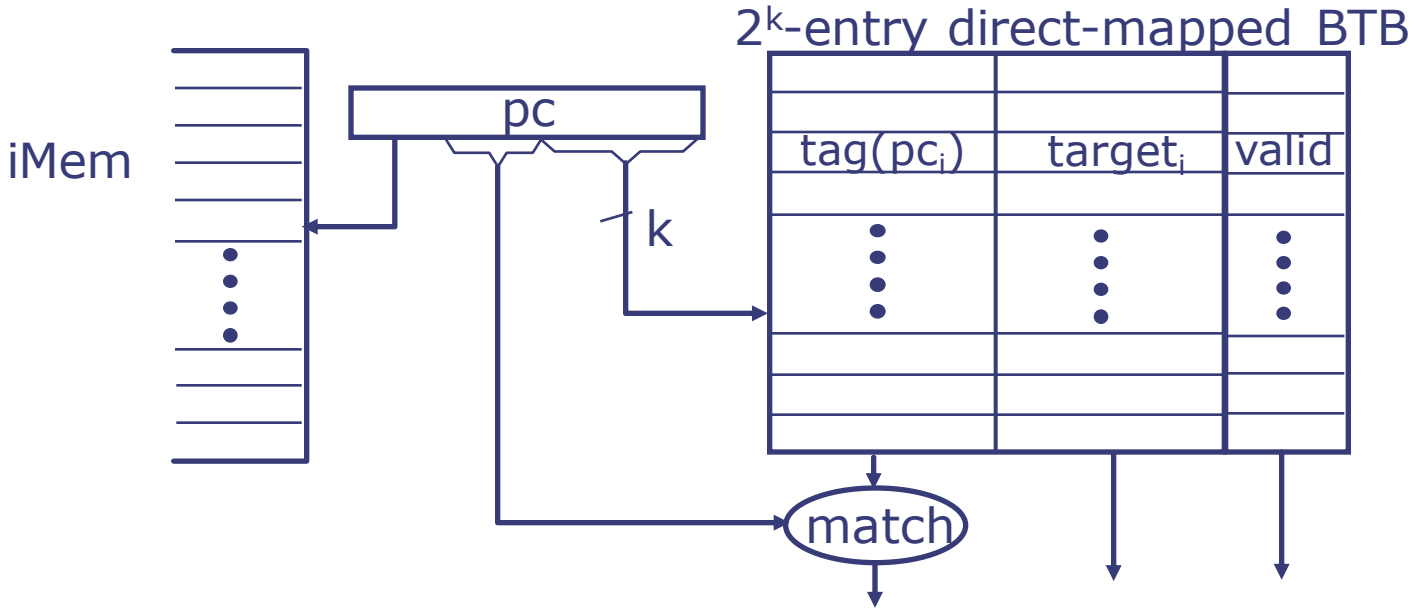

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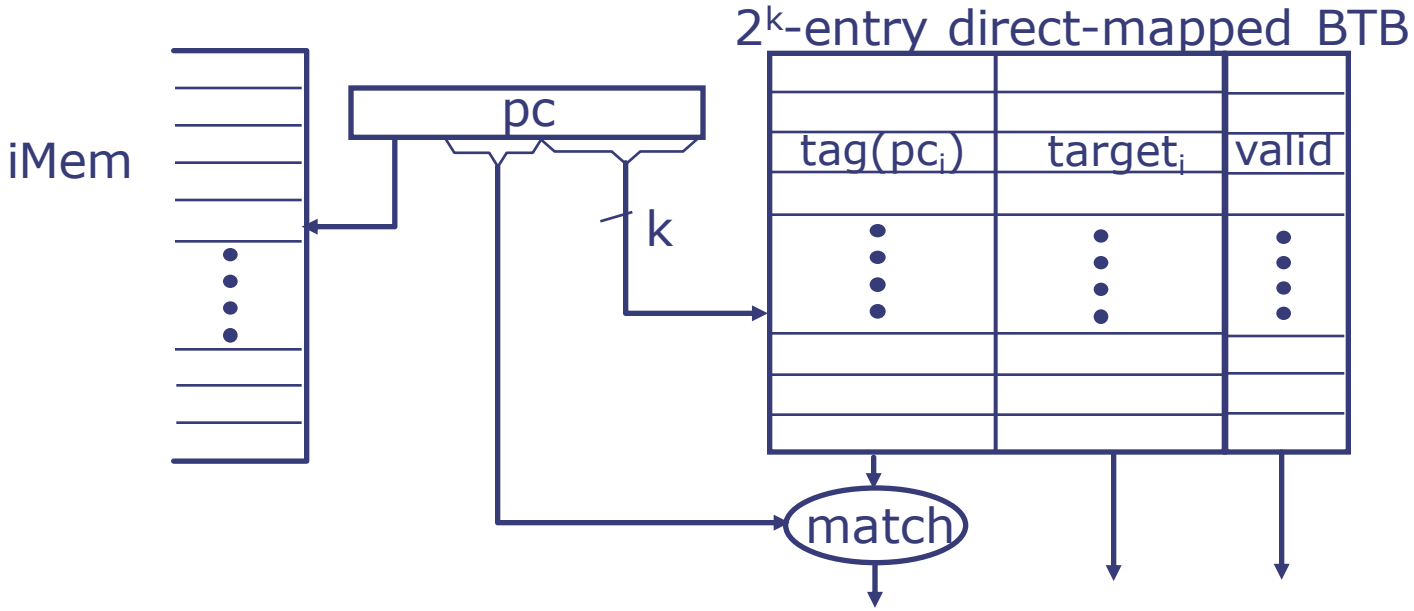

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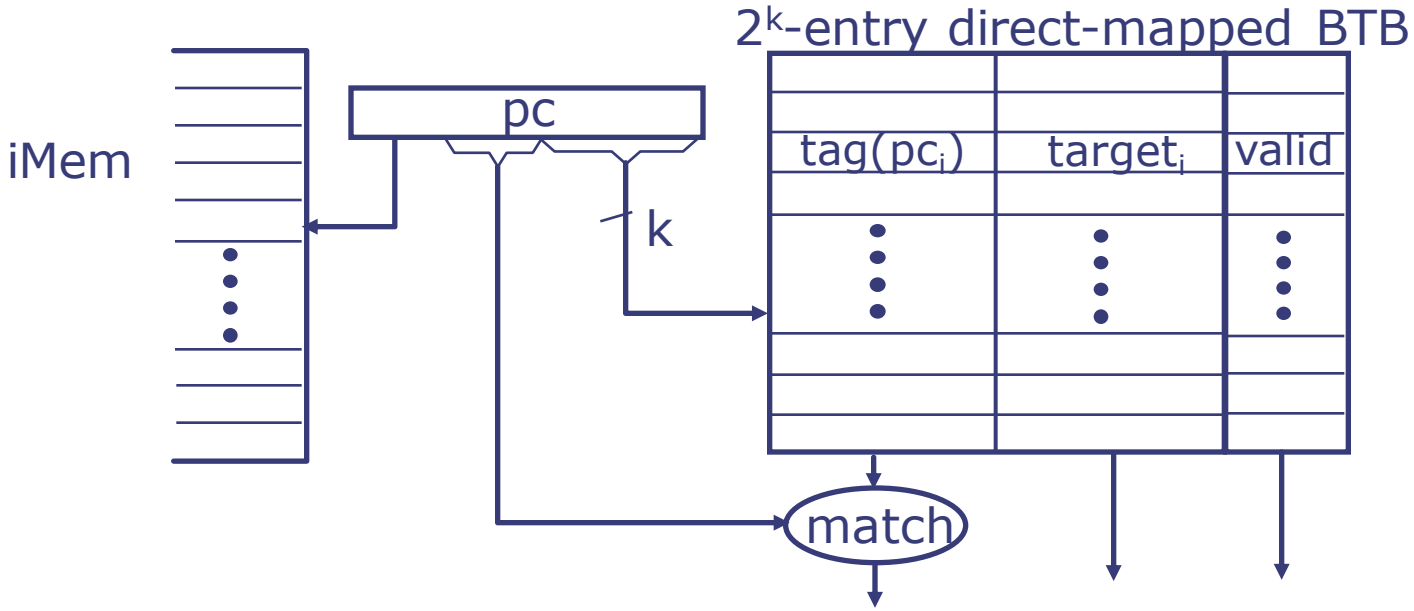

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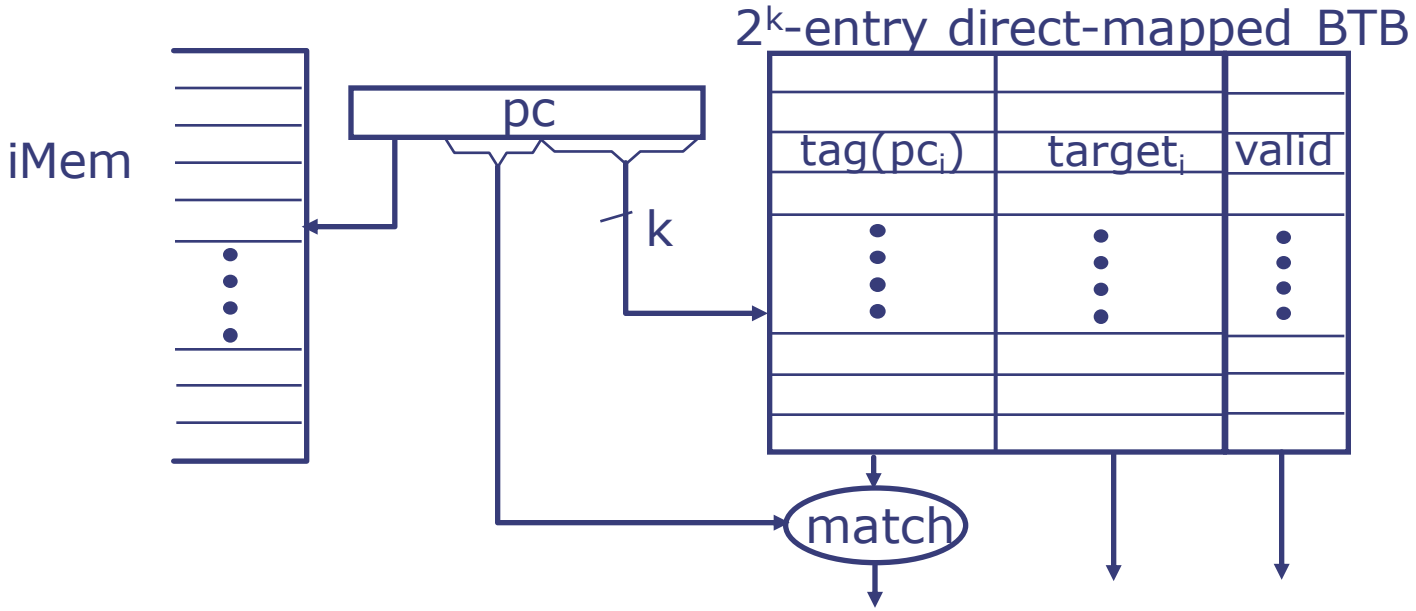

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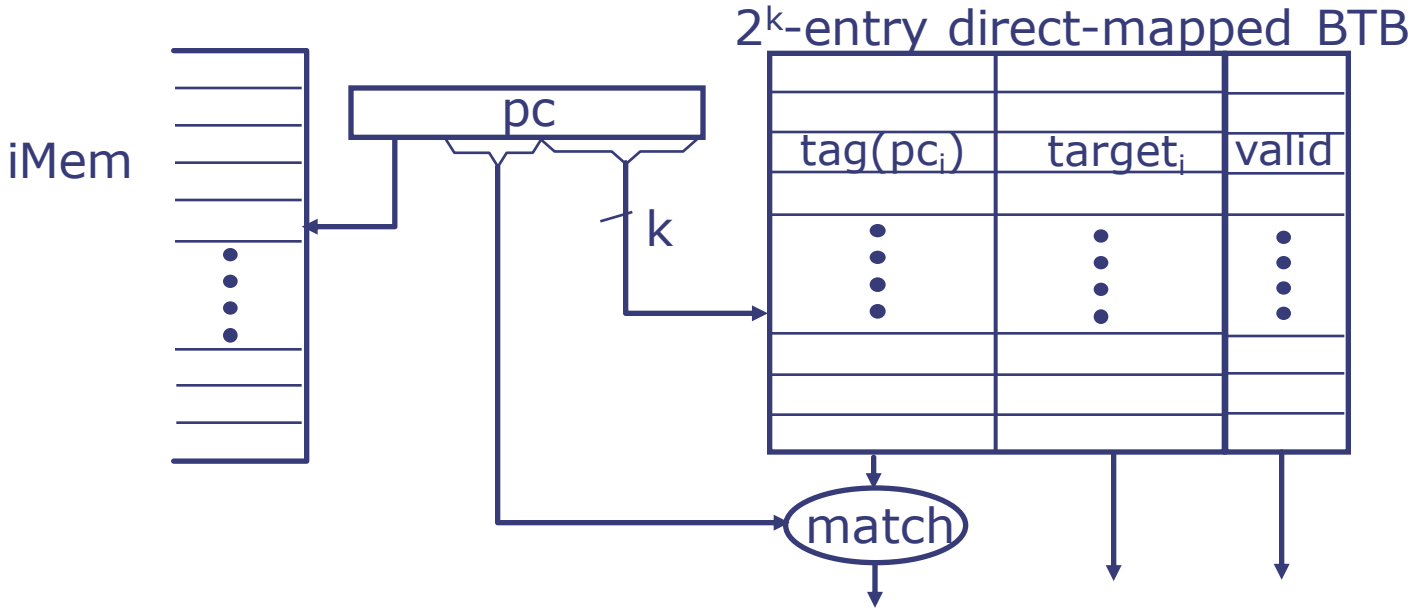

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- Even small BTBs are very effective!

BTB Interface

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  { Word pc; Word nextPc; Bool taken; } UpdateArgs;
module BTB;
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on part 3 of the design project
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Two-Bit Direction Predictor
Smith 1981

- Use two bits per BTB entry instead of one valid bit
- Manage them as a saturating counter:

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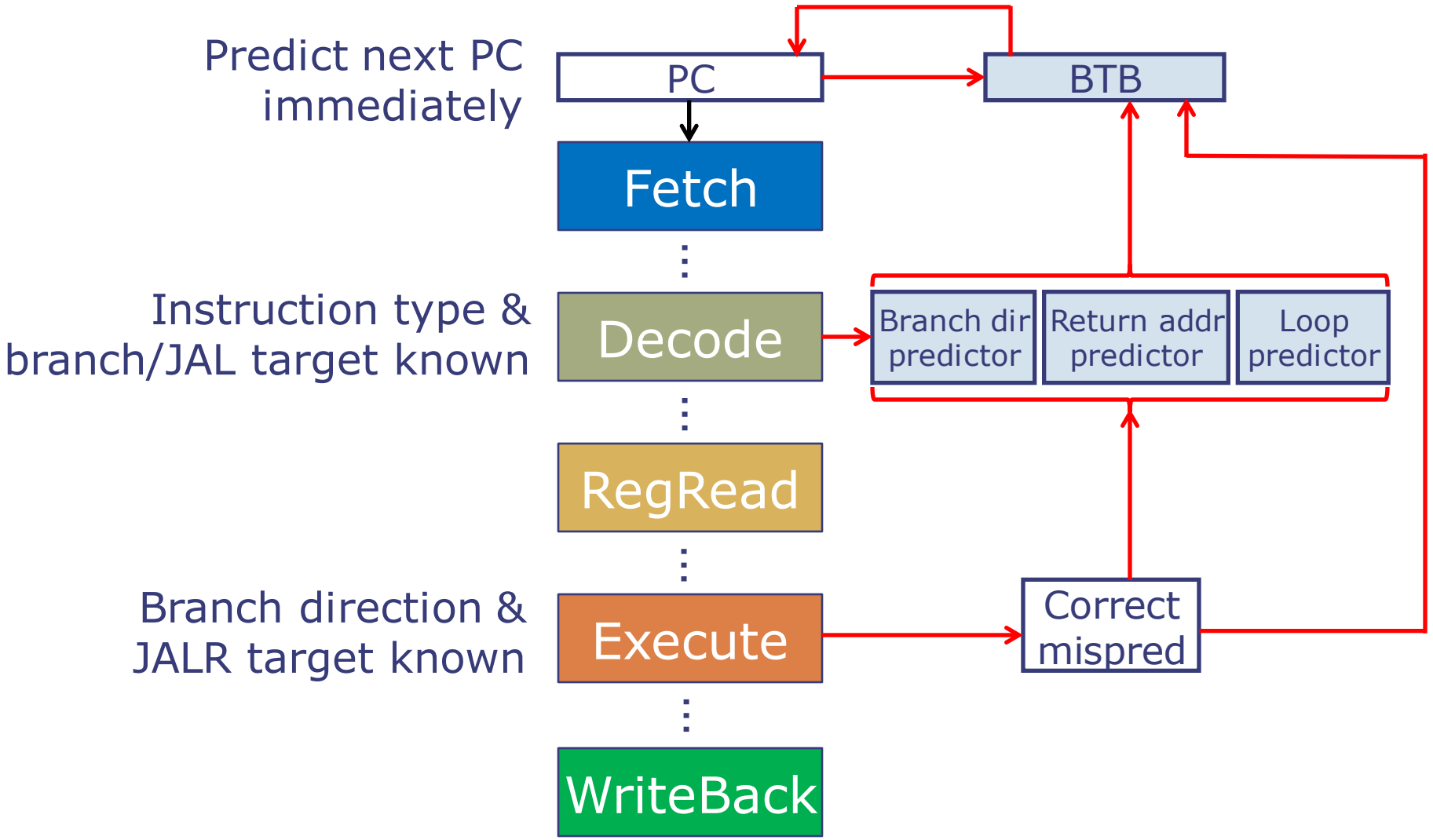
Modern Processors Combine Multiple Specialized Predictors



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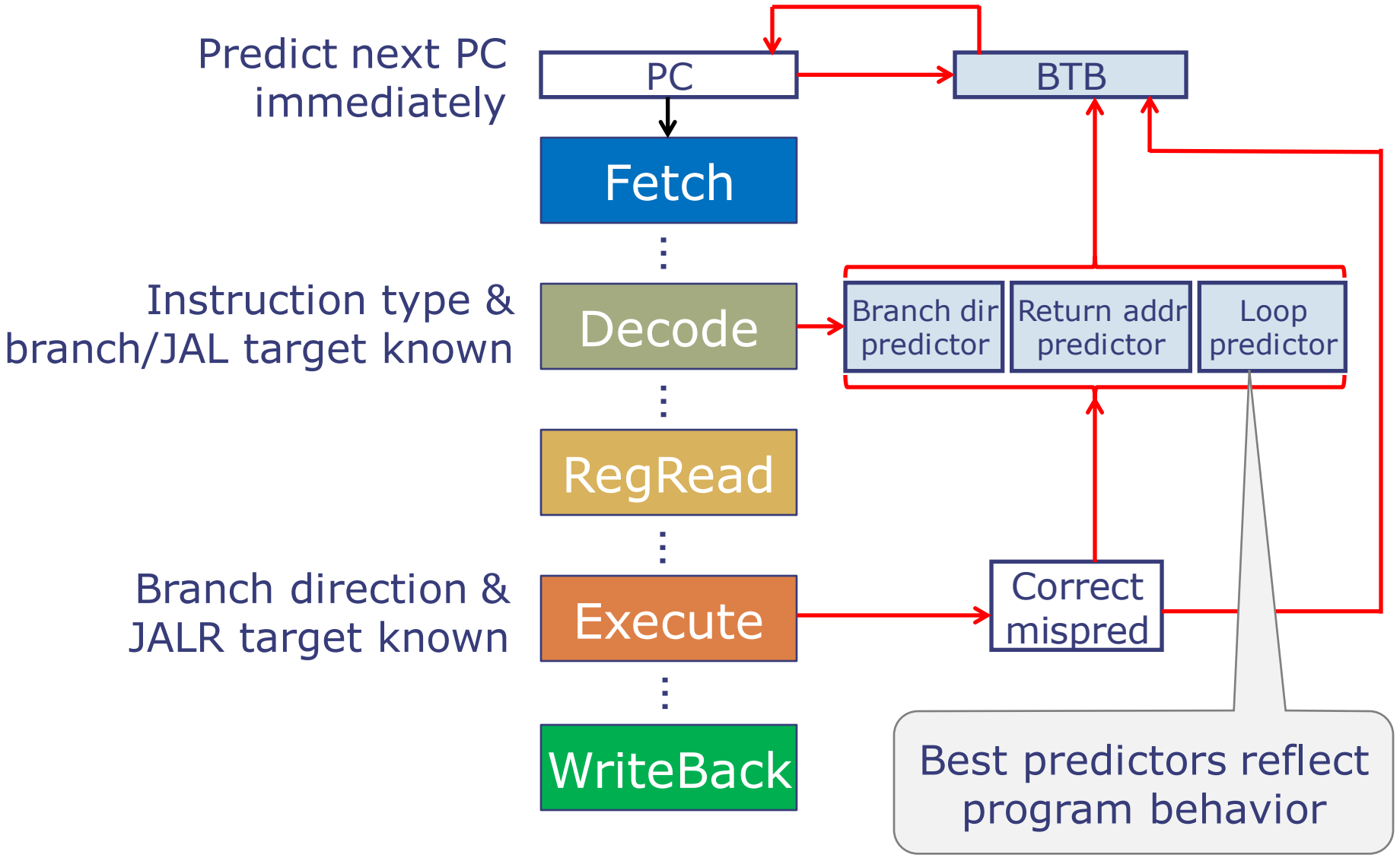

Putting It All Together: Intel Core i7 (Skylake)

- Each core has 19 pipeline stages, ~4GHz
- 6-wide superscalar
- Out of order execution
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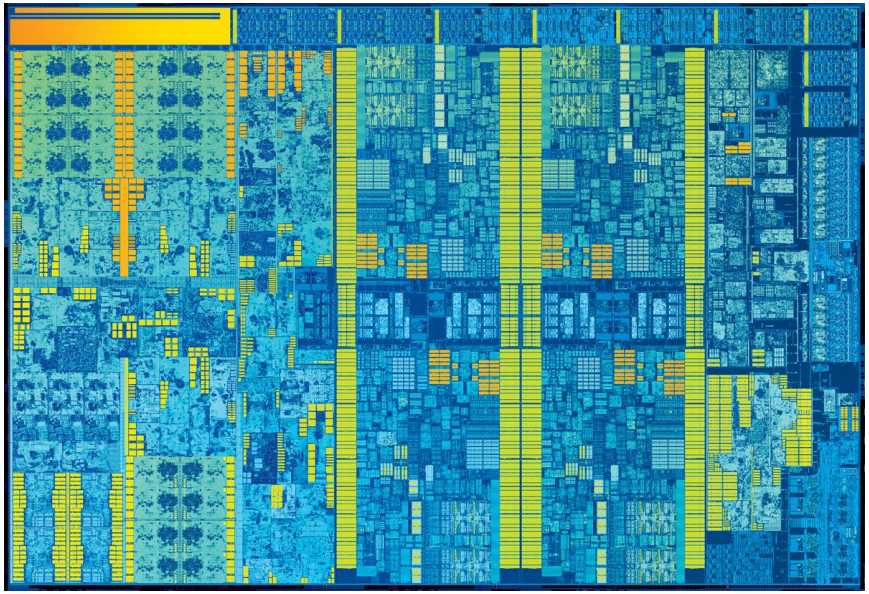

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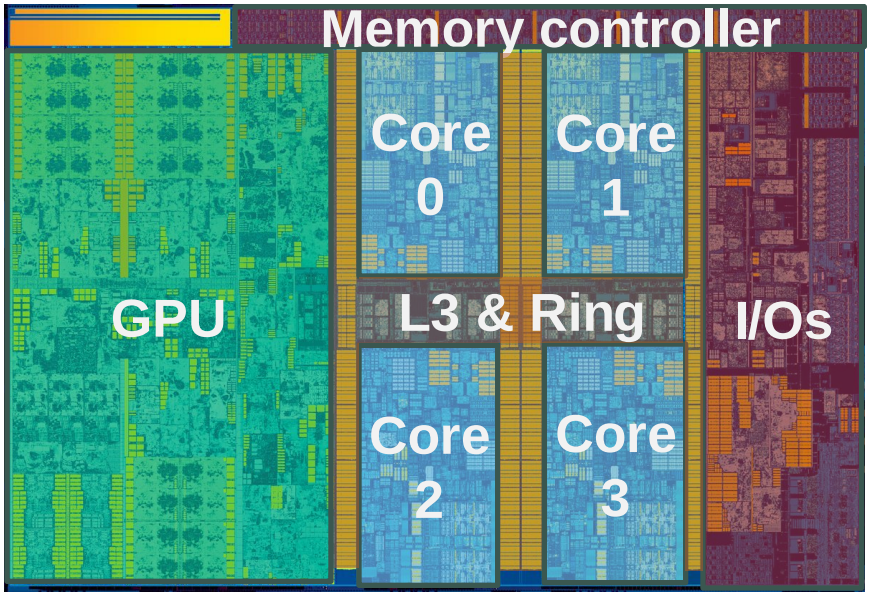

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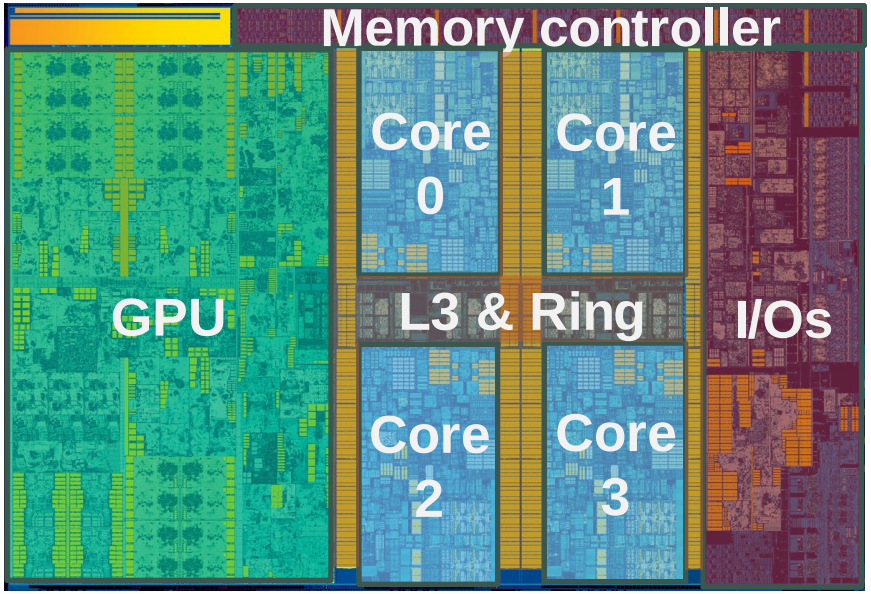

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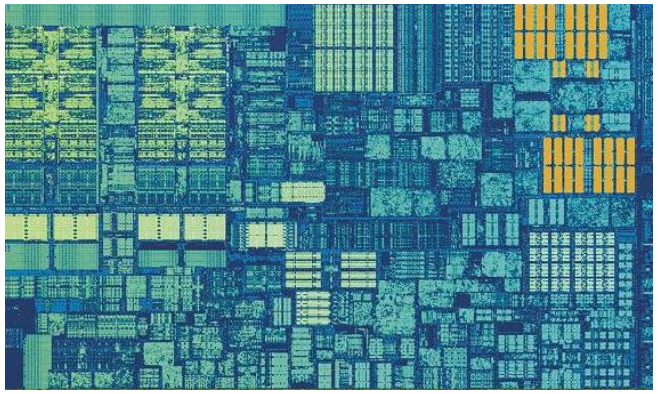

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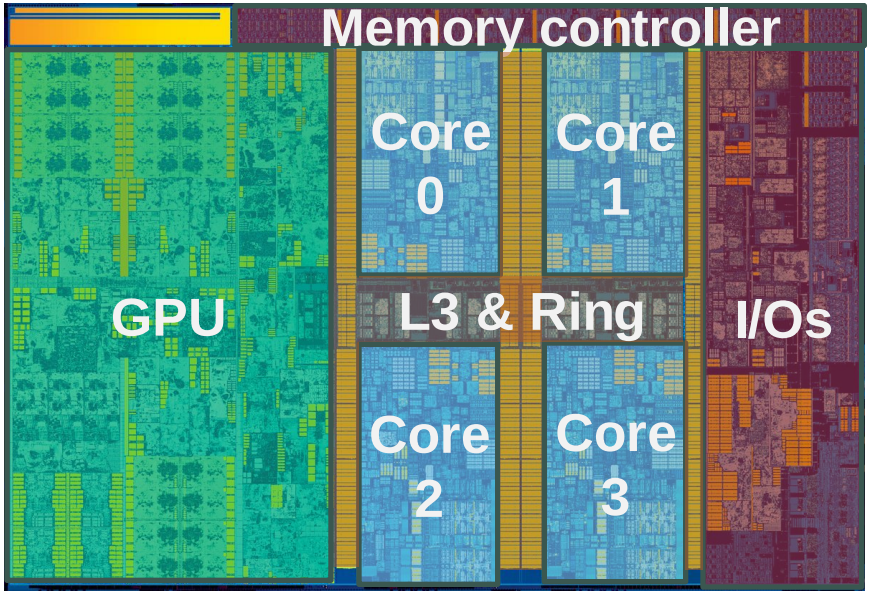

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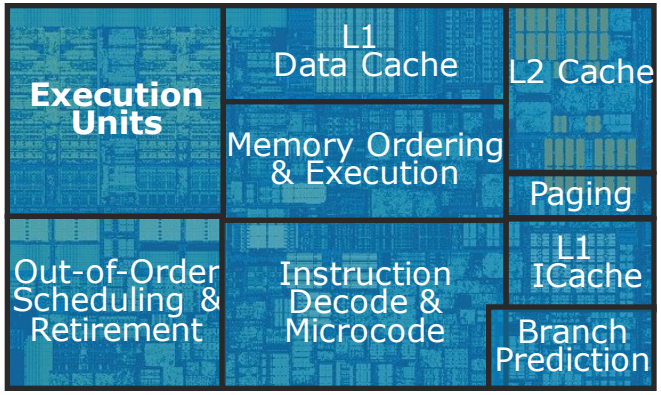

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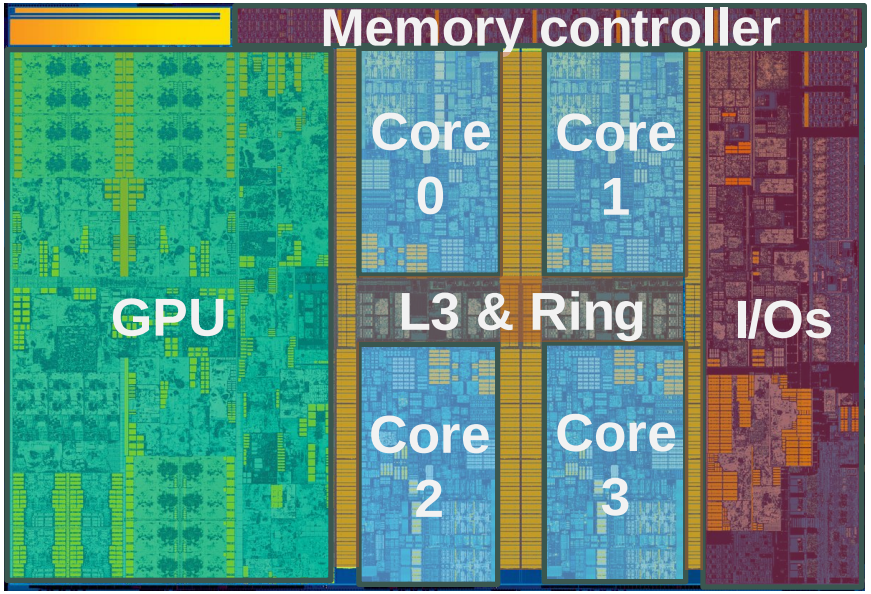

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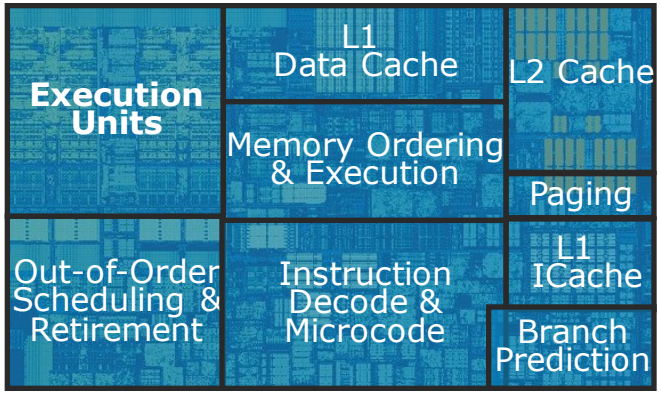

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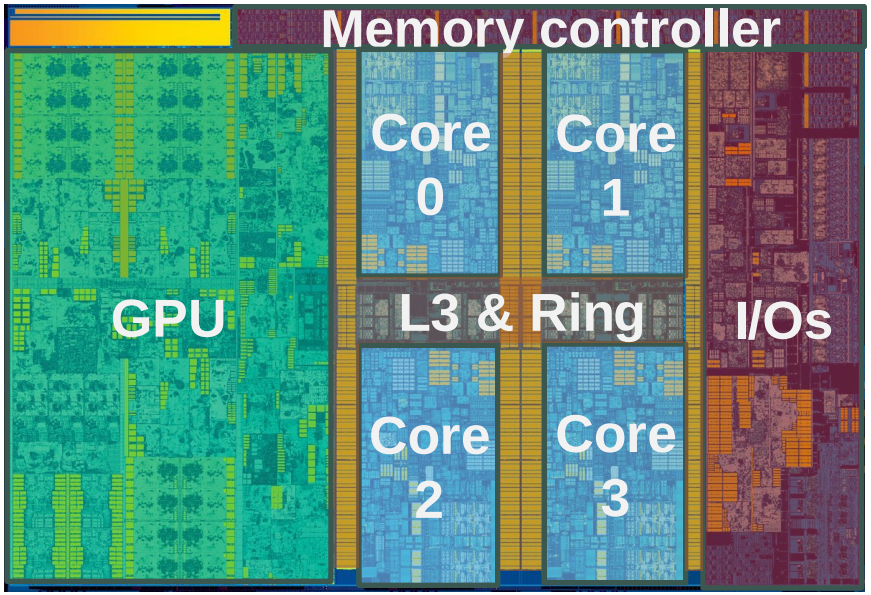

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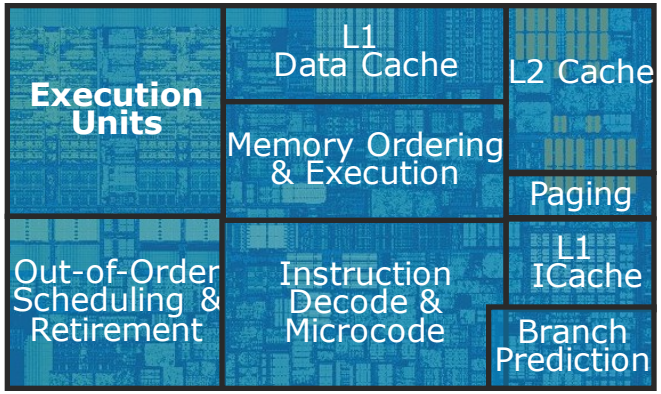

- Your RISC-V core

Thank you!

Good luck on Quiz 3 ☺