Complex Combinational Logic: Implementation and Design Tradeoffs

Lecture Goals

- Learn some advanced Minispec features that enable implementing large circuits succinctly
  - Parametric functions
  - Type inference and user-defined types
  - Loops and control-flow statements

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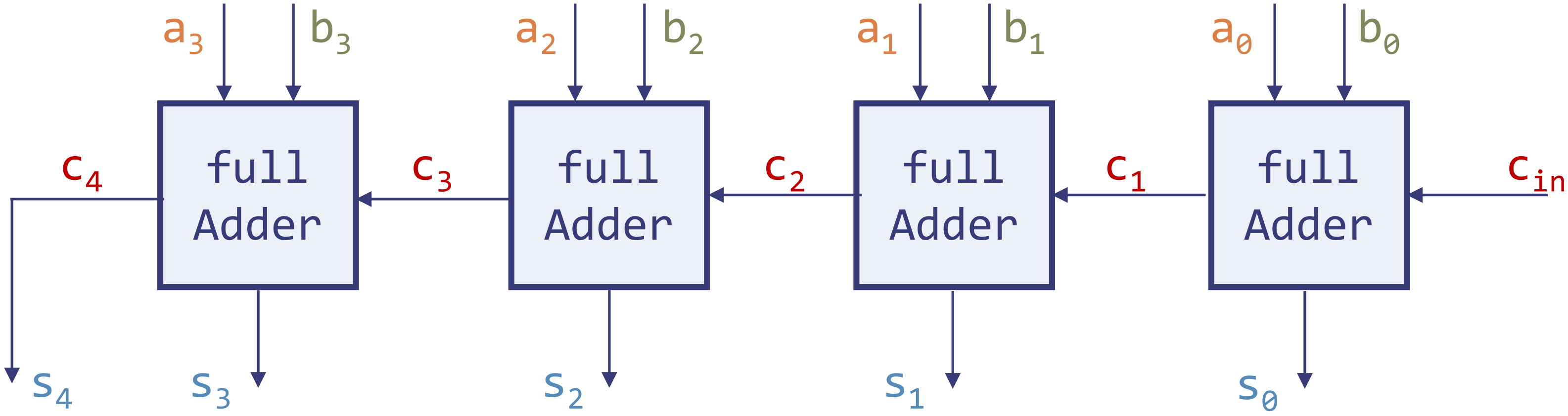
  - Parametric functions
  - Type inference and user-defined types
  - Loops and control-flow statements

- Study design tradeoffs in combinational logic by analyzing different adder implementations

Reminder: 4-bit Ripple-Carry Adder



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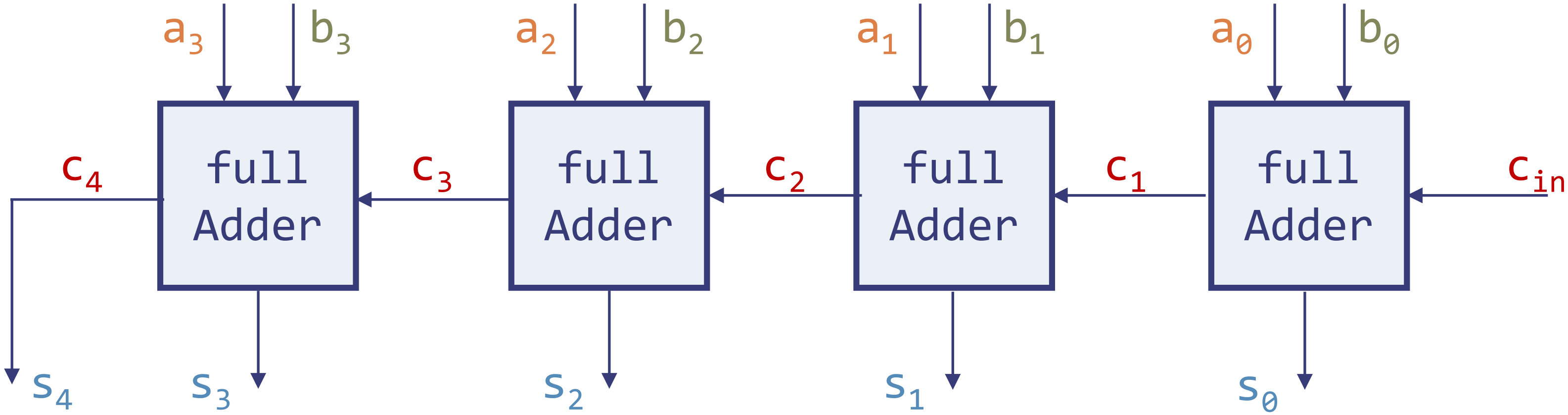


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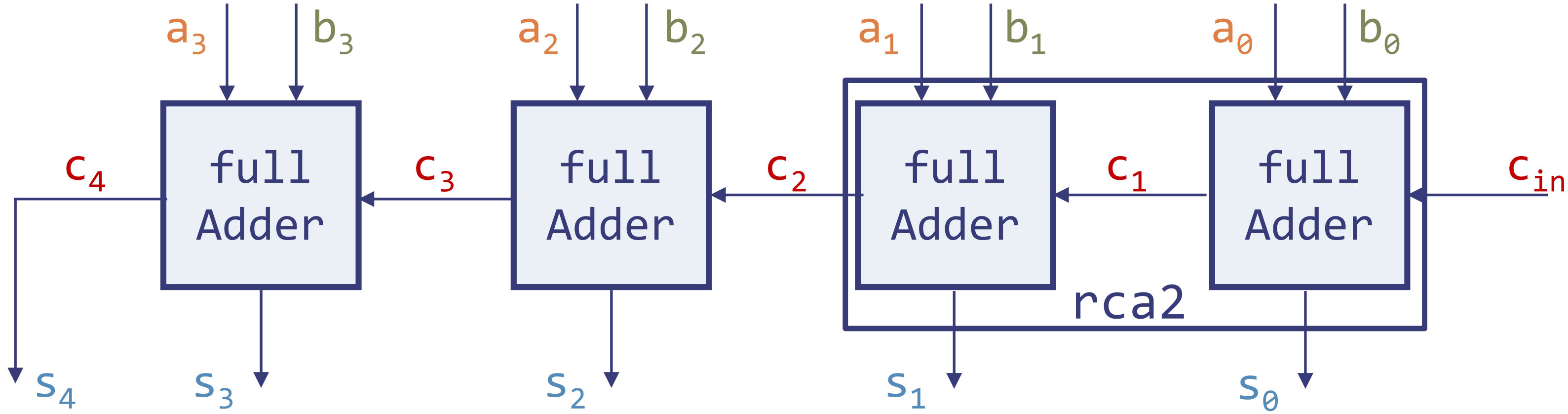


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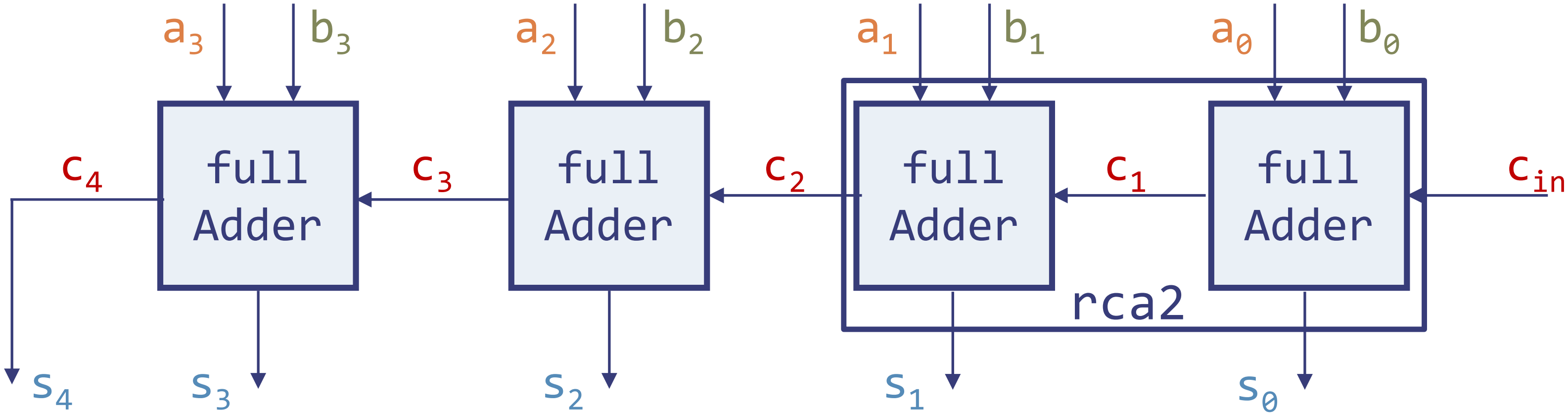


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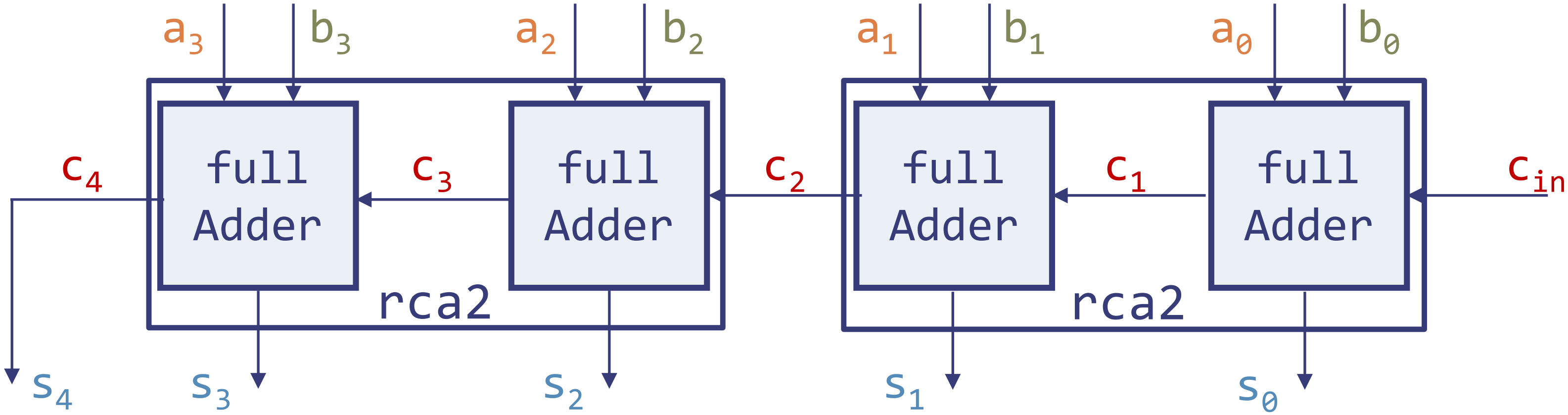


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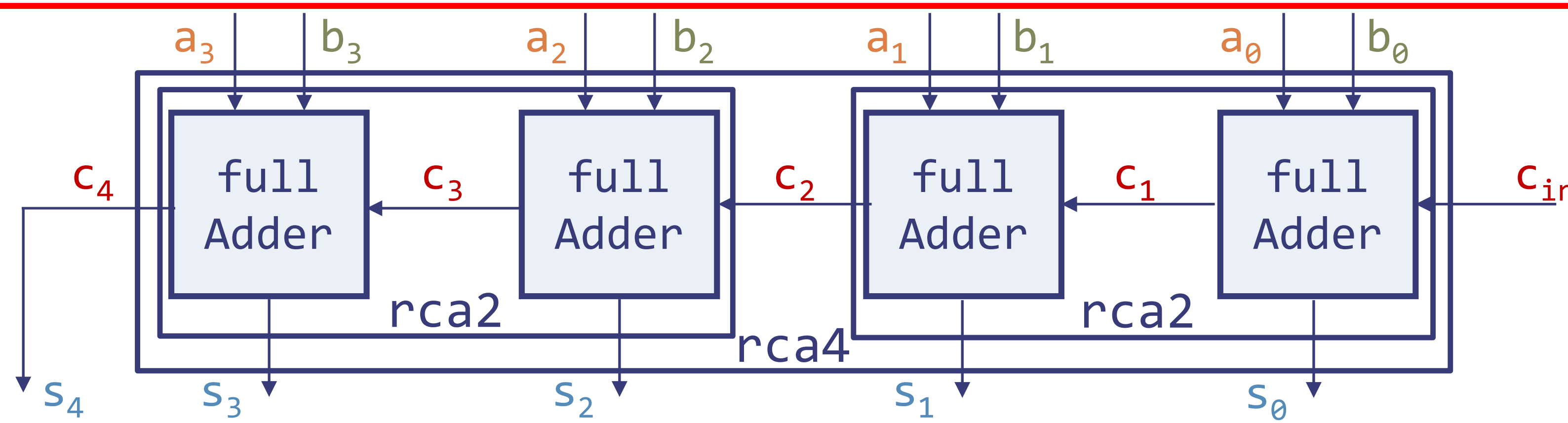


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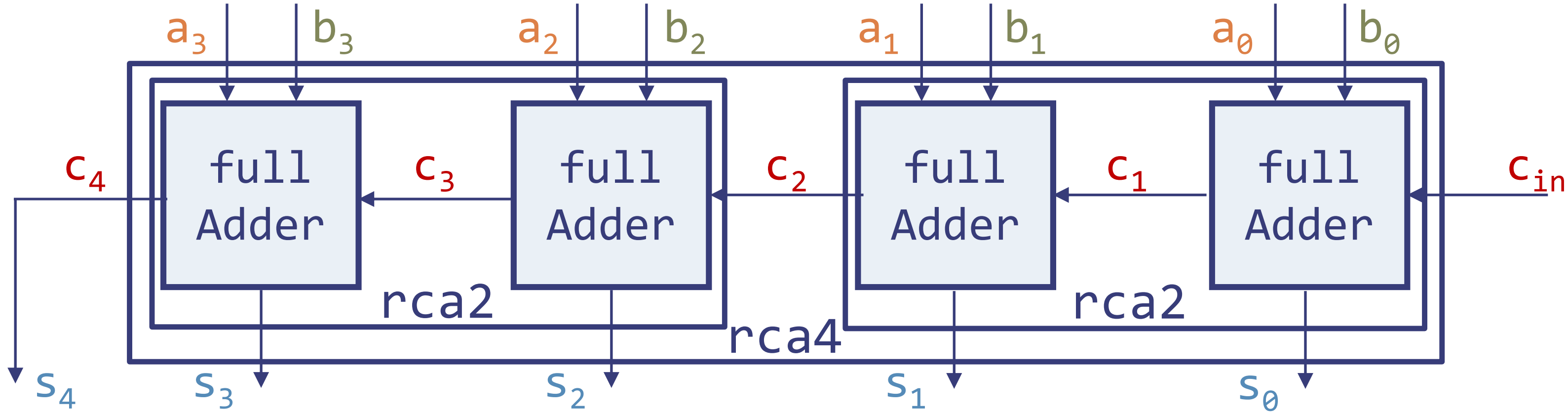


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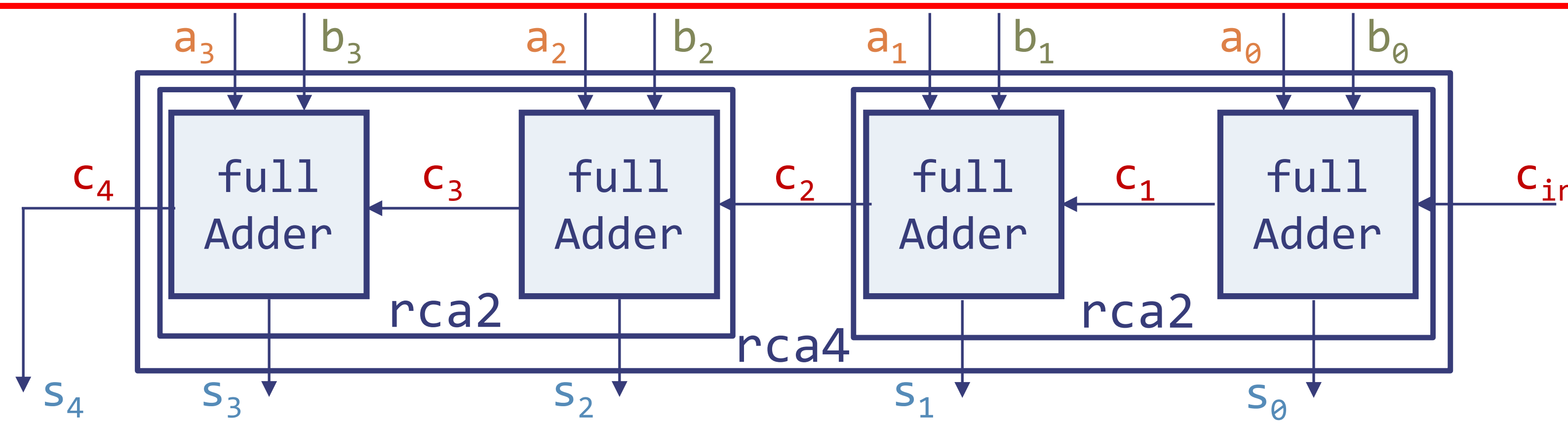


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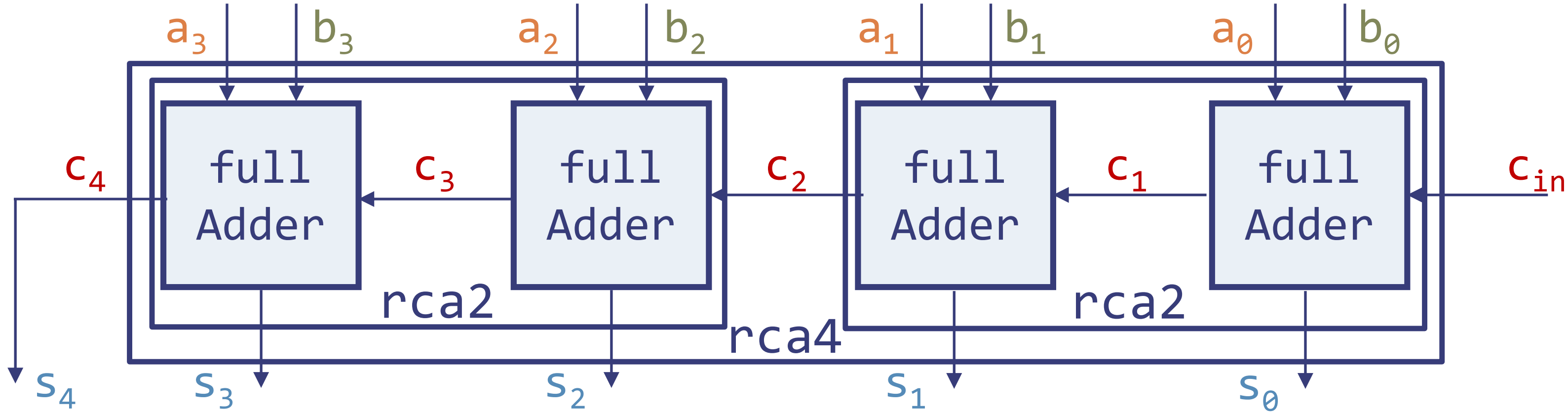


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- Problem 1: Have to write a function for every bit width
- Problem 2: If we build large functions from smaller ones, have to write many functions!

Parametric Types

- Bit#(n), an n-bit value, is a parametric type
  - n is the parameter (an Integer value)
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- Parameters can be Integers or types
  - Example: Vector#(n, T) is an n-element vector of T's
    (e.g., Vector#(4, Bit#(8)) = 4-elem vector of 8-bit values)

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  - Example: `rca#(n)`, an n-bit ripple-carry adder
- A parametric function must be invoked with fixed parameters, which instantiates a *concrete* function
  - Example: Calling `rca#(32)` instantiates a 32-bit adder

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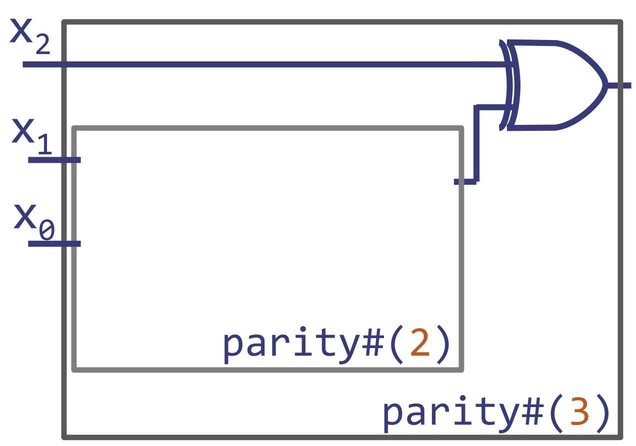

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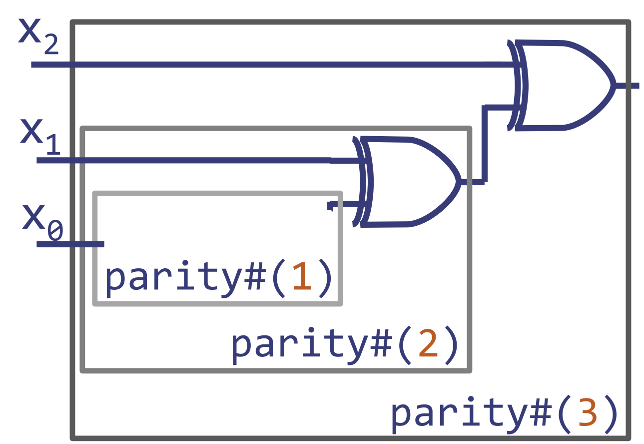

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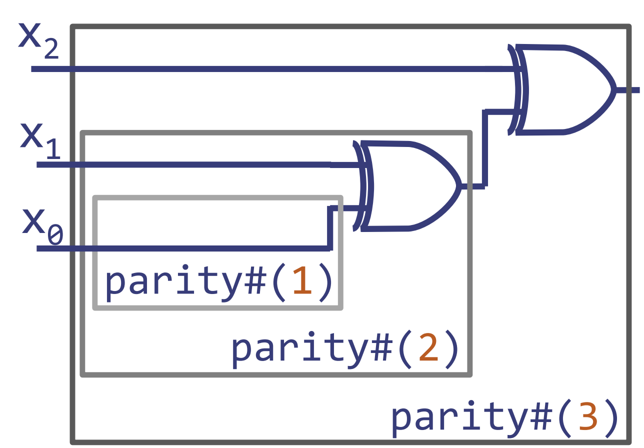

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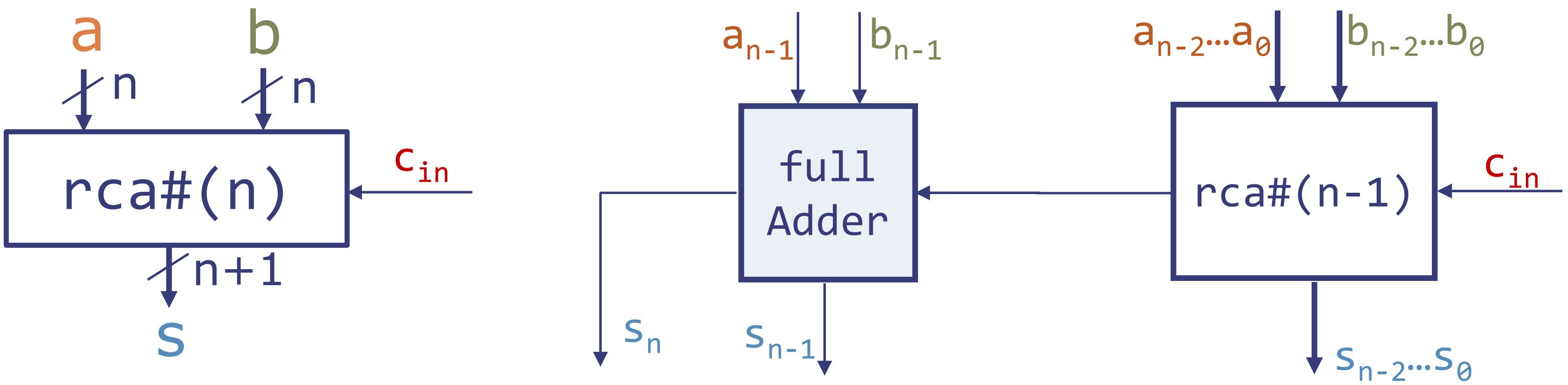
  - If the compiler cannot evaluate an Integer expression, it throws an error
- Integer supports the same operations as Bit#(n), (arithmetic, logical, comparisons, etc.)
  - But evaluated by compiler → operations on Integers never produce any hardware

N-bit Ripple-Carry Adder



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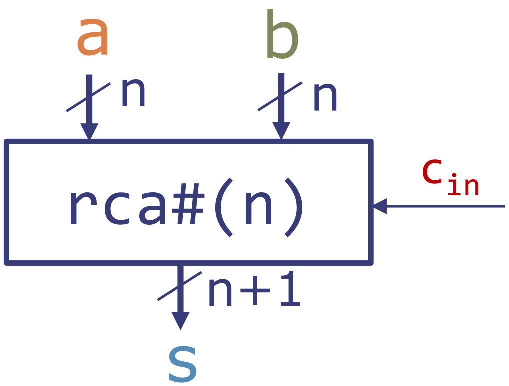

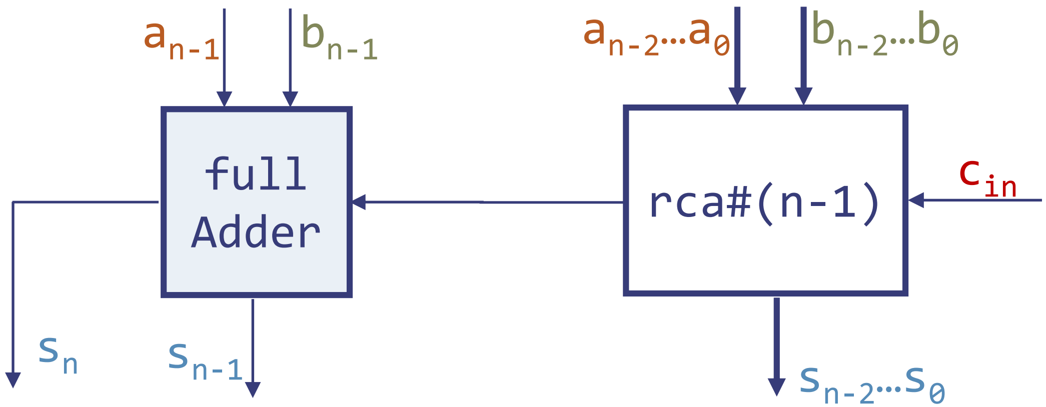


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function Bit#(n+1) rca#(Integer n)(Bit#(n) a, Bit#(n) b, Bit#(1) cin);


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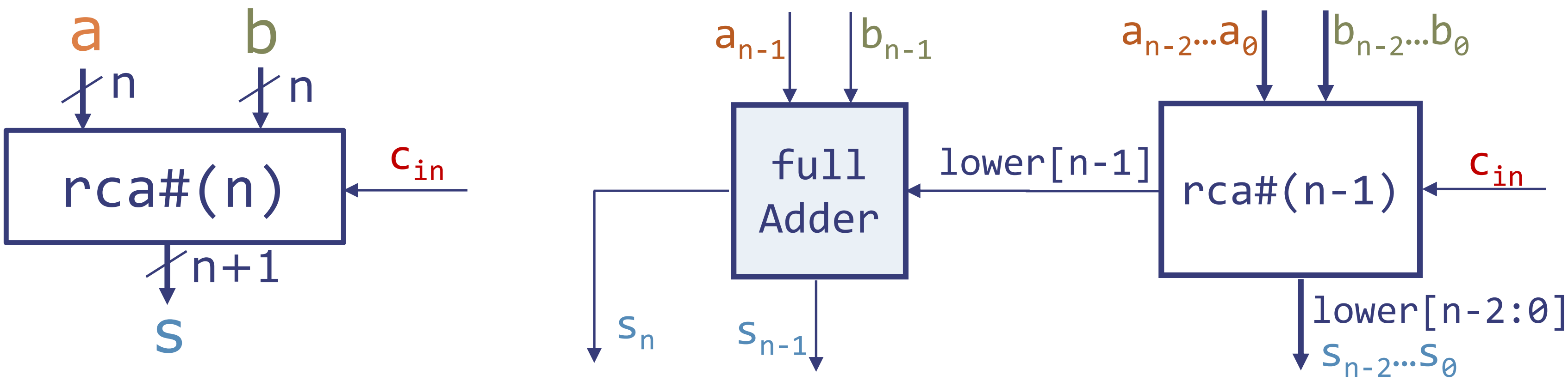


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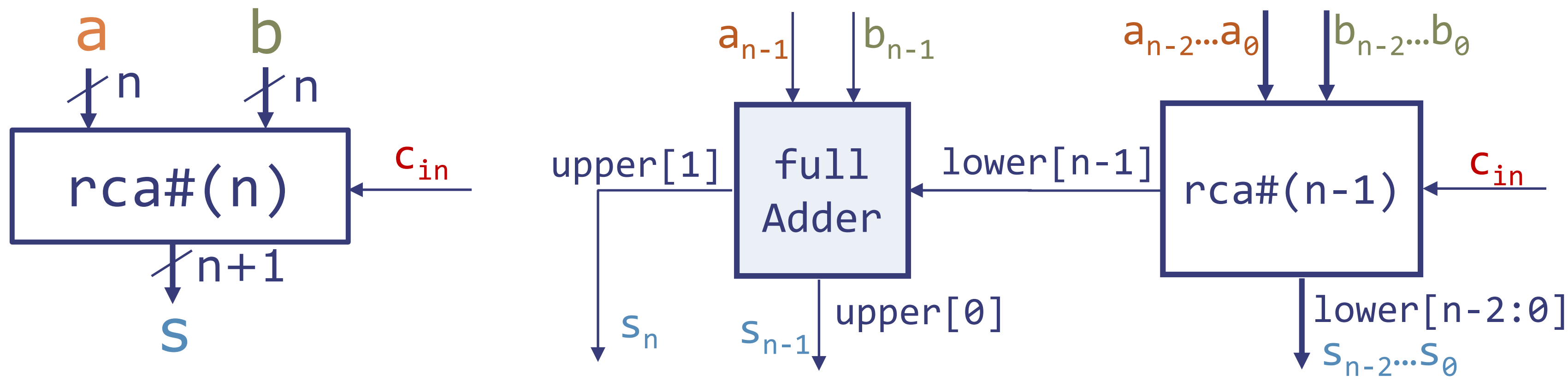


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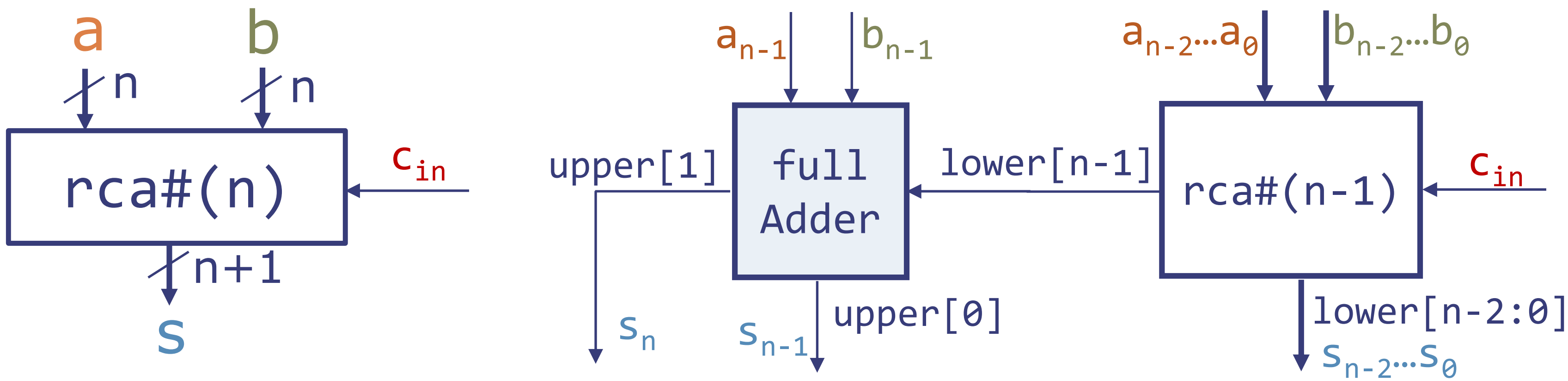


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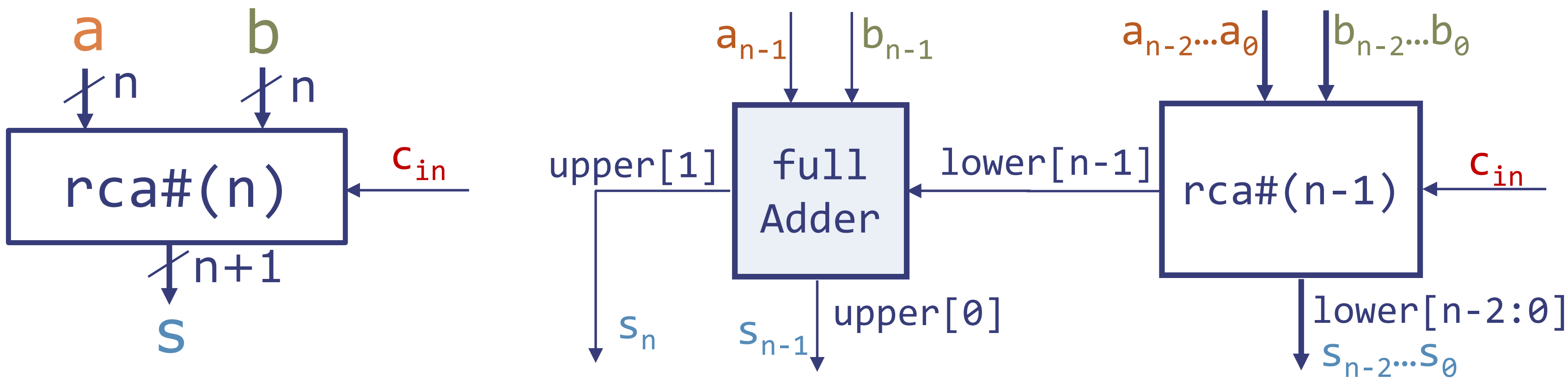


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endfunction

// Base case
function Bit#(2) rca#(1)(Bit#(1) a, Bit#(1) b, Bit#(1) cin);
    return fullAdder(a, b, cin);
endfunction
```

Type Inference

- You can omit the type of a variable by declaring it with the let keyword
- The compiler infers the variable's type from the type of the expression assigned to the variable

```
Bit#(4) x = 4'b0011;
let y = x;         // y has type Bit#(4)
let z = {x, x};    // z has type Bit#(8)
let w = 2'b11;     // w has type Bit#(2)
let n = 42;        // n has type Integer
```

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Pixel p;
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- Structs represent a group of member values with different types
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- Structs and enums are much clearer than using raw bits!
  - e.g., `Bit#(24) pixel; pixel[15:8]` versus `Pixel pixel; pixel.green`

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State state = Ready;
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For Loops

Use with care

- For loop statements allow compactly expressing a sequence of similar statements

```
Bit#(6) w = 0;
for (Integer i = 0; i < 6; i = i + 1)
    w[i] = z[i / 2];
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Use with care

- For loop statements allow compactly expressing a sequence of similar statements

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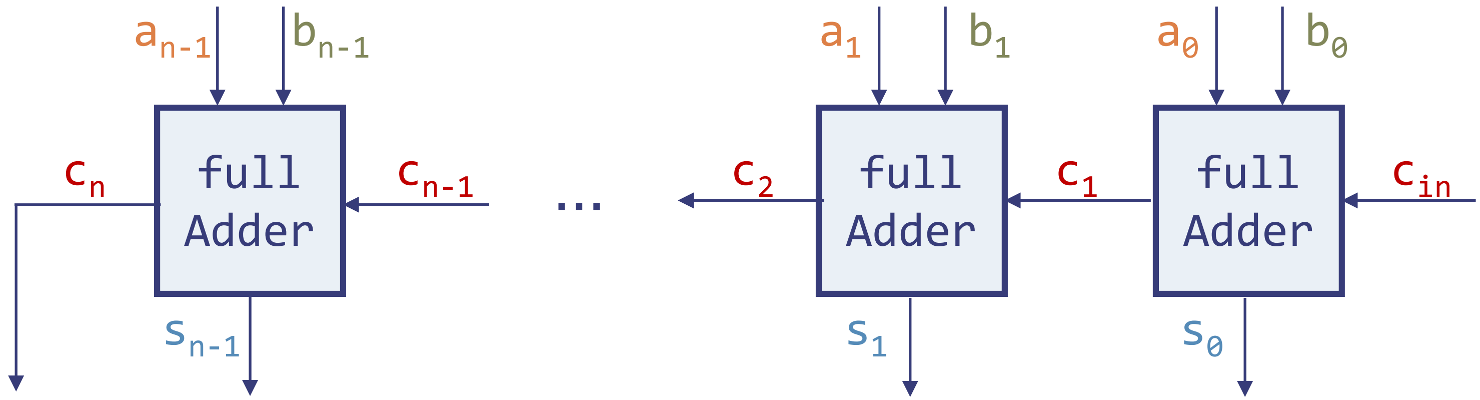
- Example: The loop above is translated into this sequence:

```
w[0] = z[0];
w[1] = z[0];
w[2] = z[1];
w[3] = z[1];
w[4] = z[2];
w[5] = z[2];
```

N-bit Ripple-Carry Adder with Loop




```
function Bit#(n+1) rca#(Integer n)(Bit#(n) a, Bit#(n) b, Bit#(1) cin);
    Bit#(n) s = 0;
    Bit#(n+1) c = {0, cin};
    for (Integer i = 0; i < n; i = i + 1) begin
        let x = fullAdder(a[i], b[i], c[i]);
        s[i] = x[0];
        c[i+1] = x[1];
    end
    return {c[n], s};
endfunction
```

Conditional Statements

Use with care

- If statements have a syntax similar to software:

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function Bit#(4) max(Bit#(4) a,
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- Minispec also has case statements (see tutorial)

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Never forget that you're designing hardware

Design Tradeoffs in Combinational Circuits

Algorithmic Tradeoffs in Hardware Design

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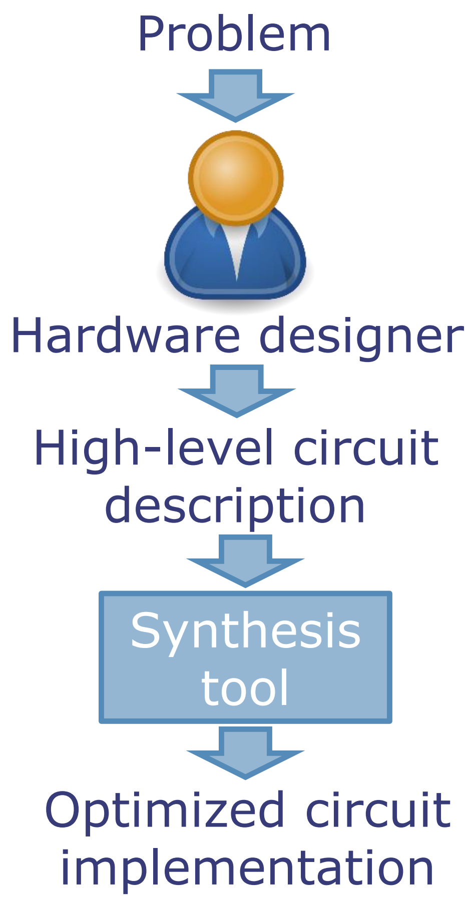

Algorithmic Tradeoffs in Hardware Design

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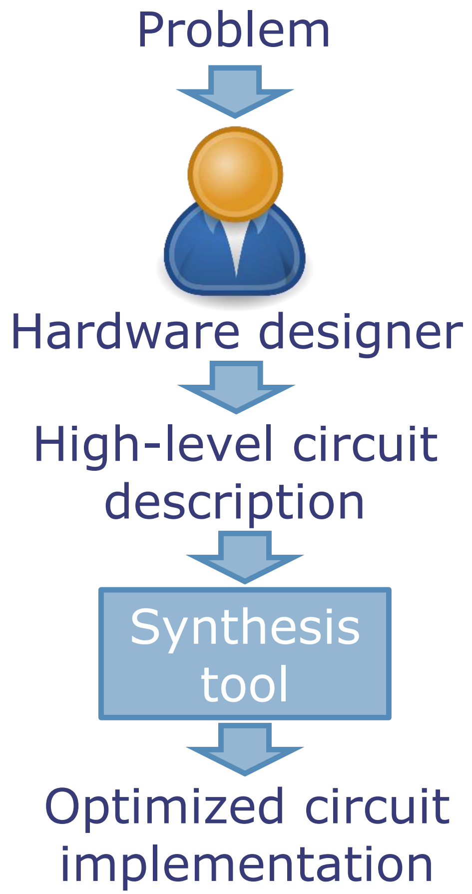

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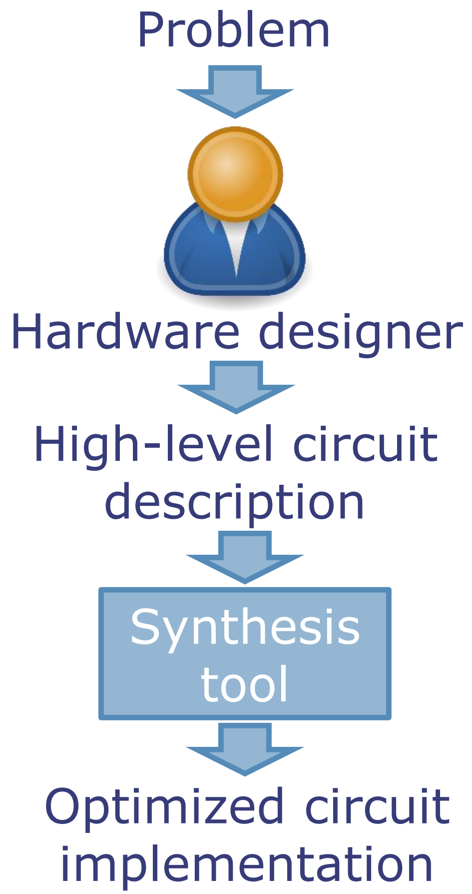

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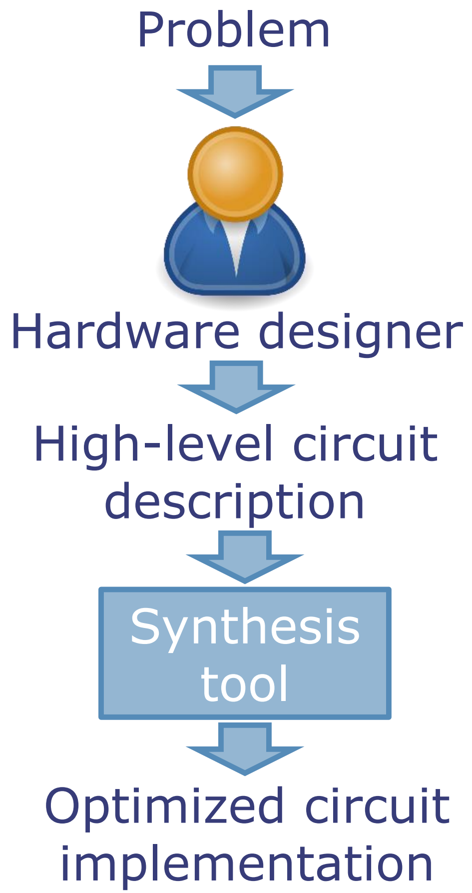
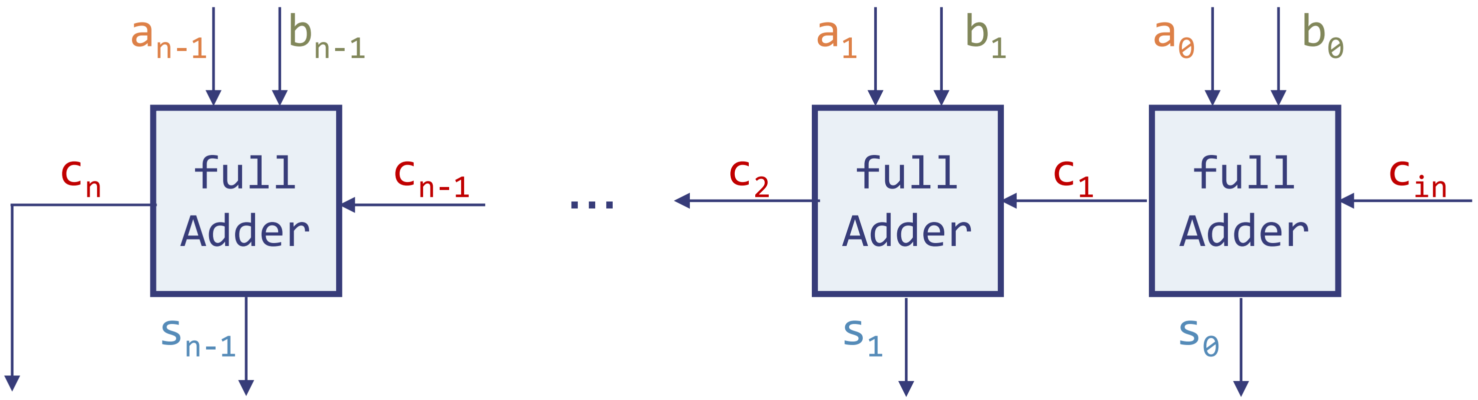
- Case study: Building a better adder



Ripple-Carry Adder: Simple but Slow



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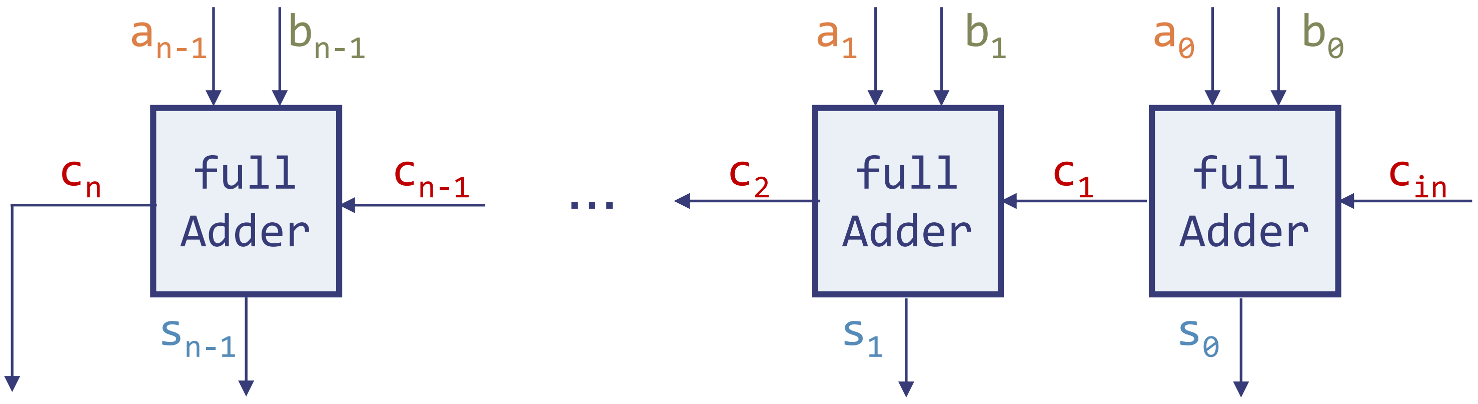

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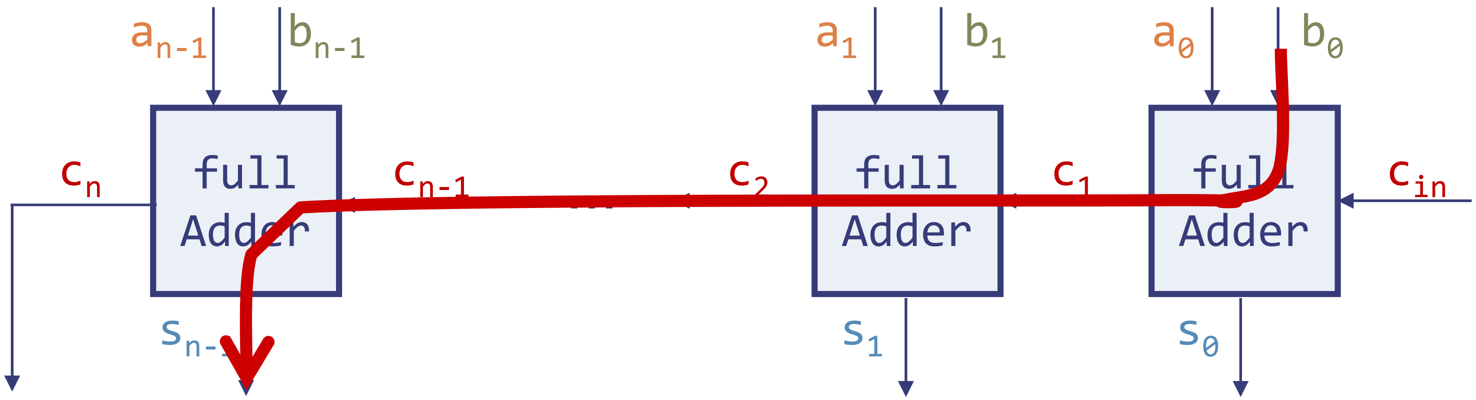

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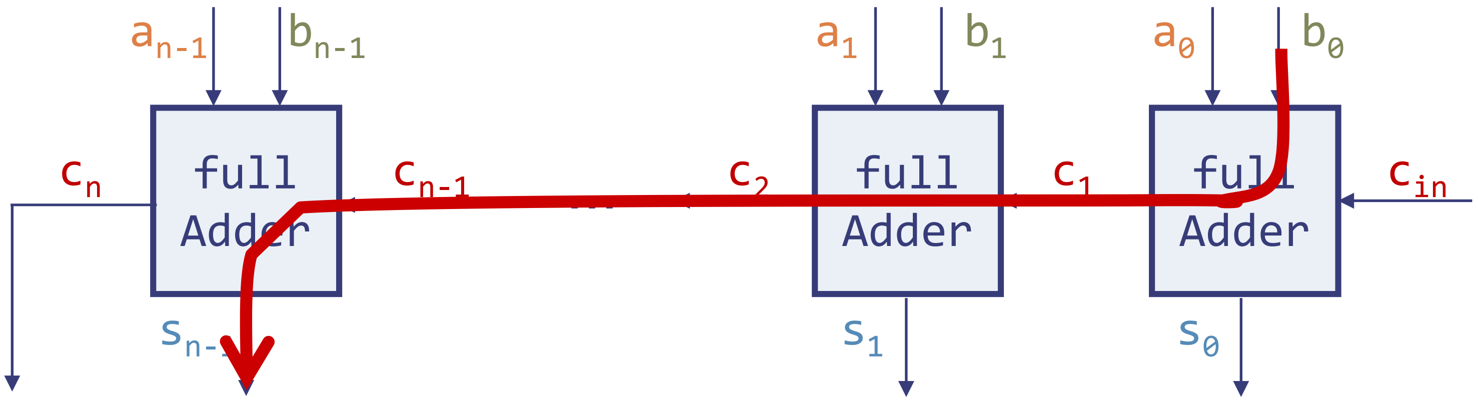

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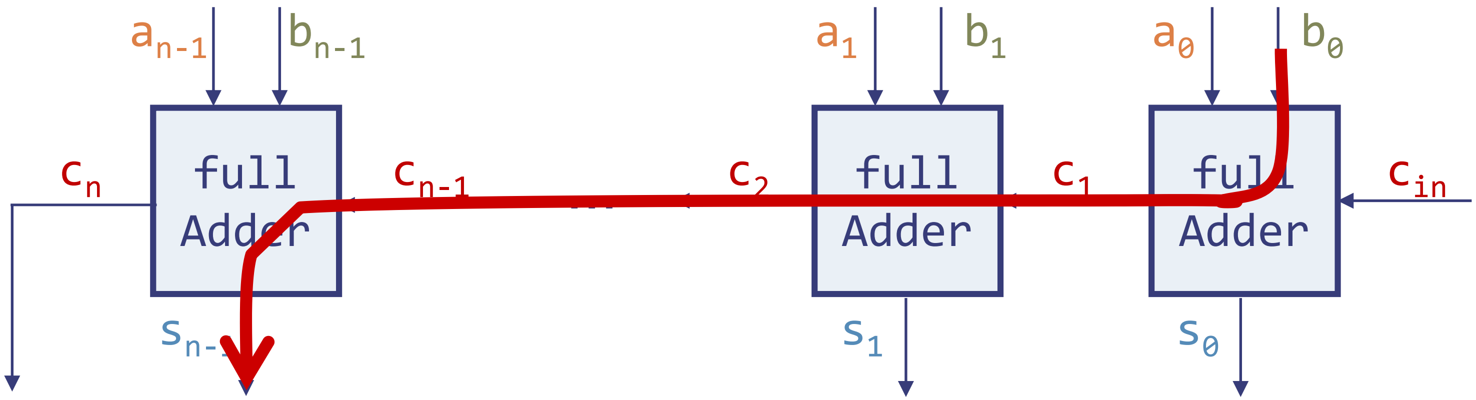

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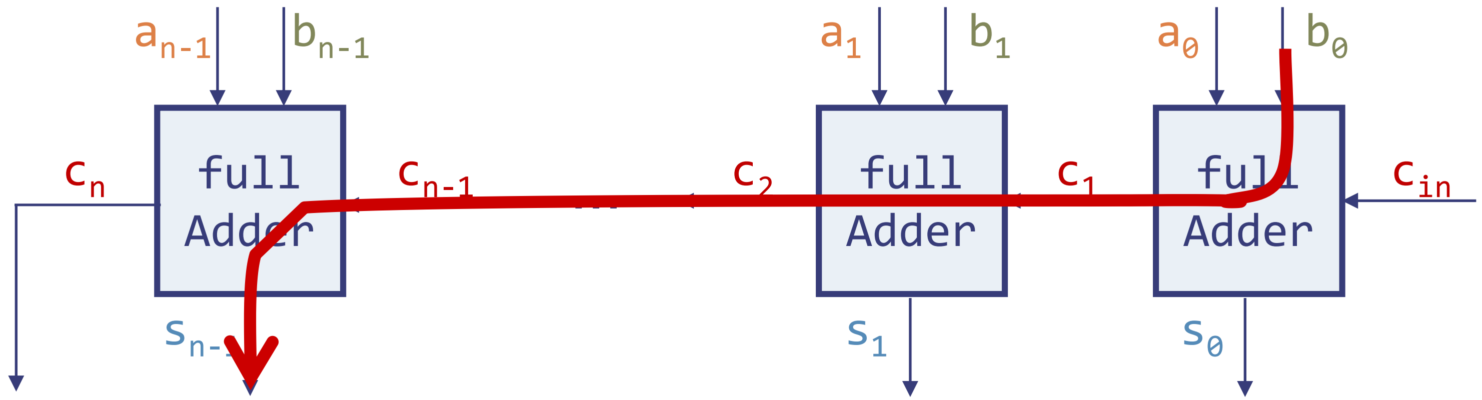

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- Θ(n) is read "order n" and tells us that the latency of our adder grows linearly with the number of bits of the operands

Asymptotic Analysis

- Formally, $g(n)=\Theta(f(n))$ iff there exist $C_2 \geq C_1 > 0$ such that for all but *finitely many* integers $n \geq 0$,

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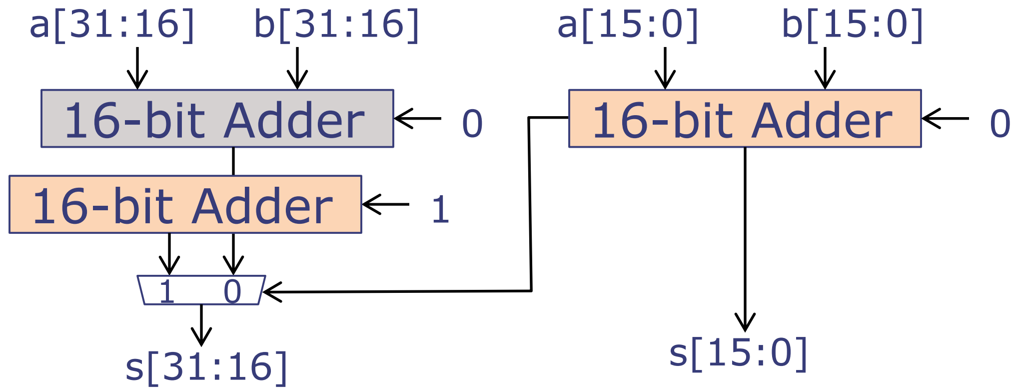
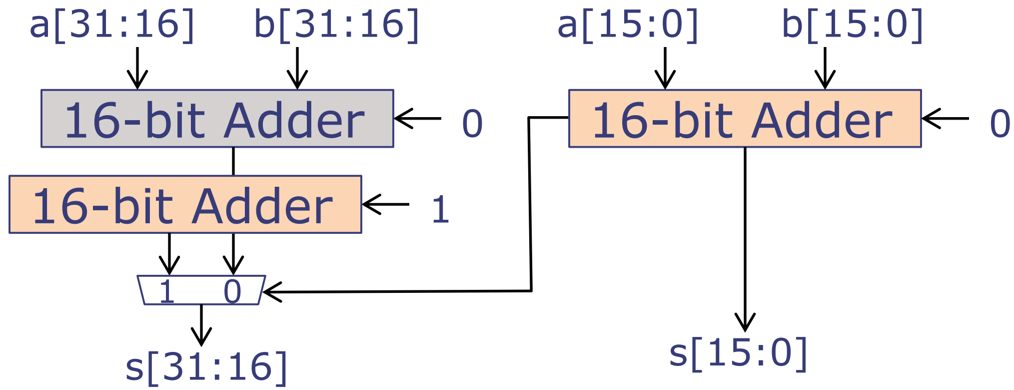
Carry-Select Adder Trades Area for Speed



Carry-Select Adder Trades Area for Speed

Two copies of the high half of the adder: one assumes carry-in of “0”, the other carry-in of “1”



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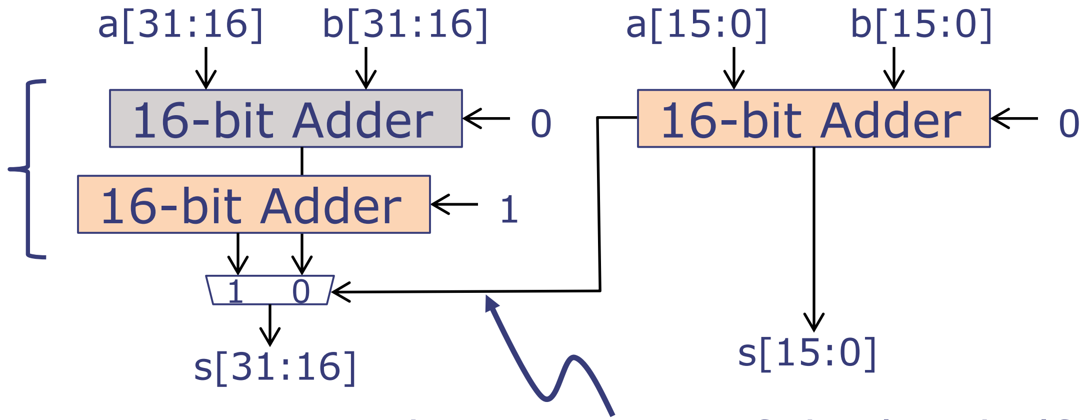

The carry-out of the low half selects the correct version of the high-half addition.

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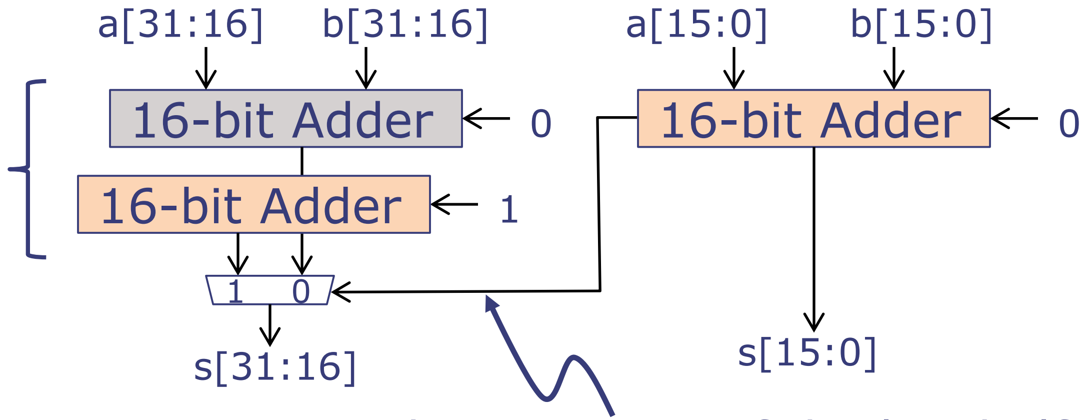

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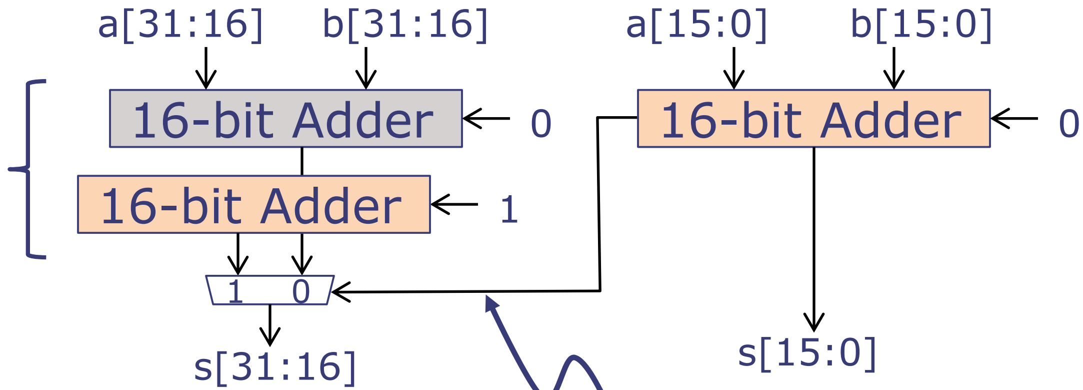

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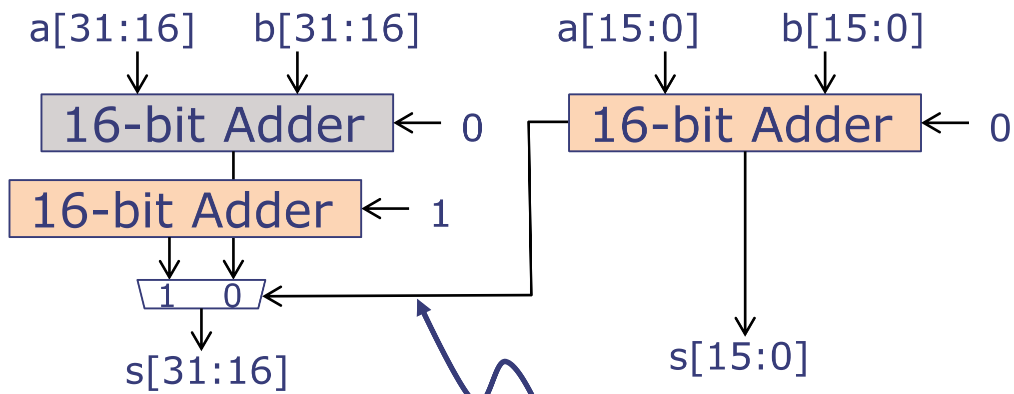

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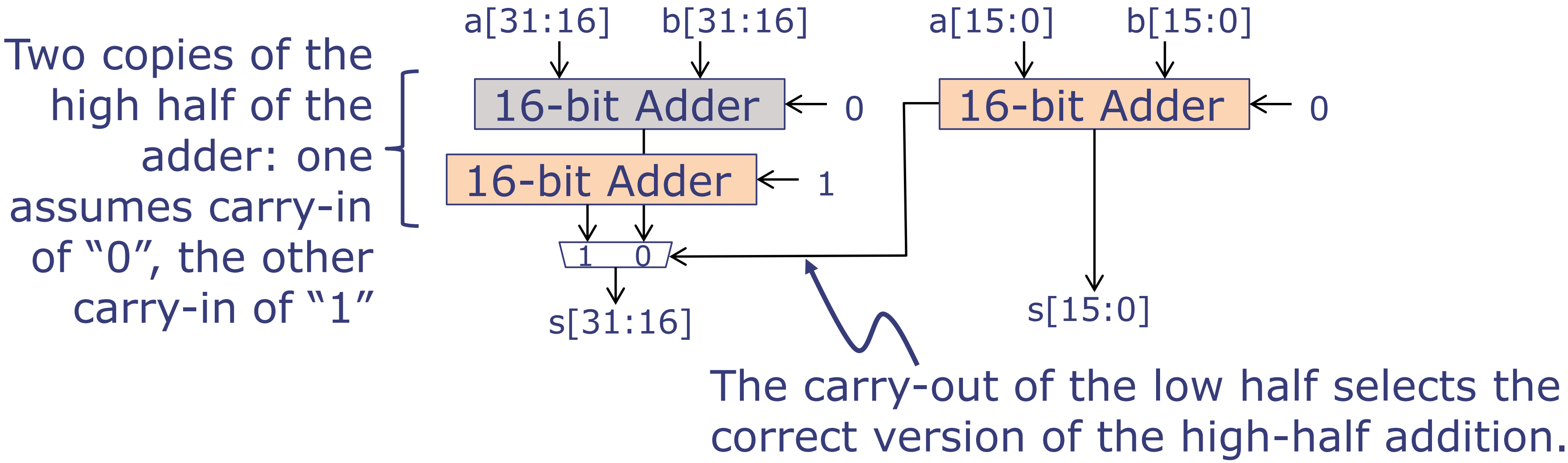

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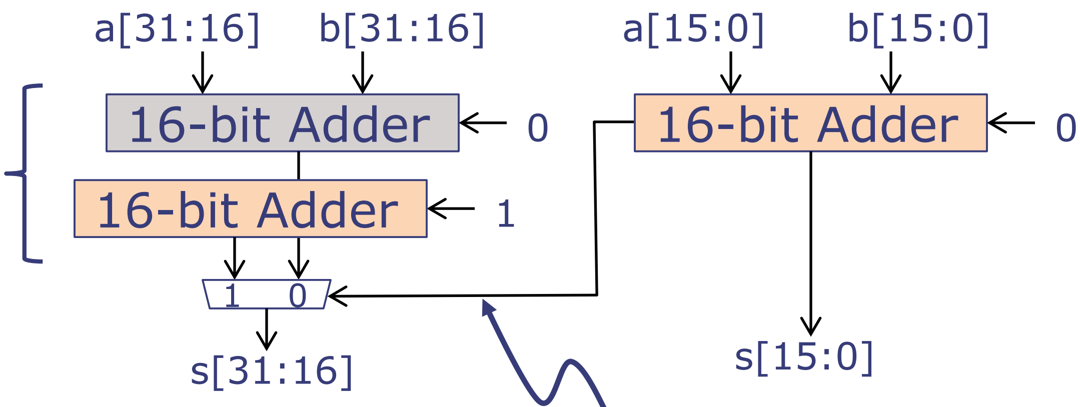

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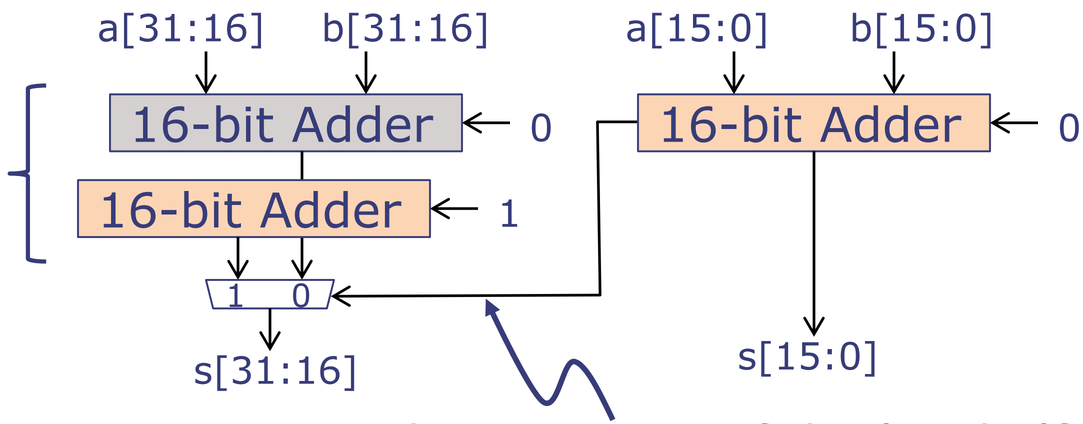

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Wide mux adds significant delay (lab 4)

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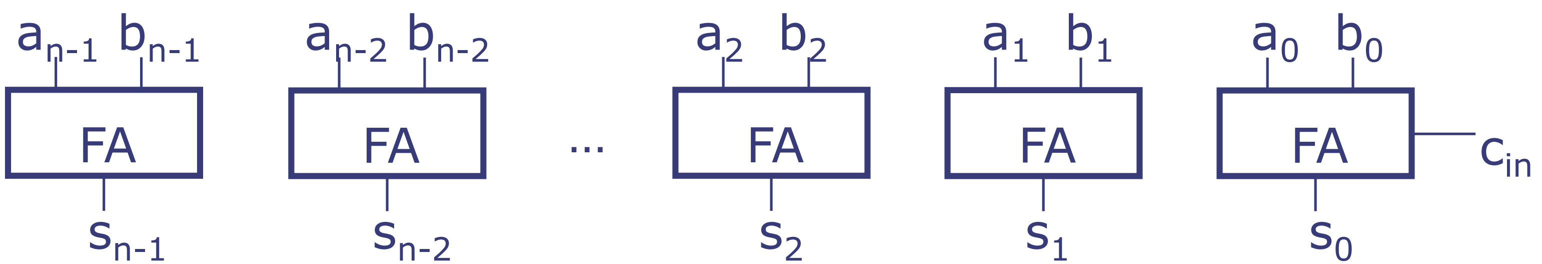

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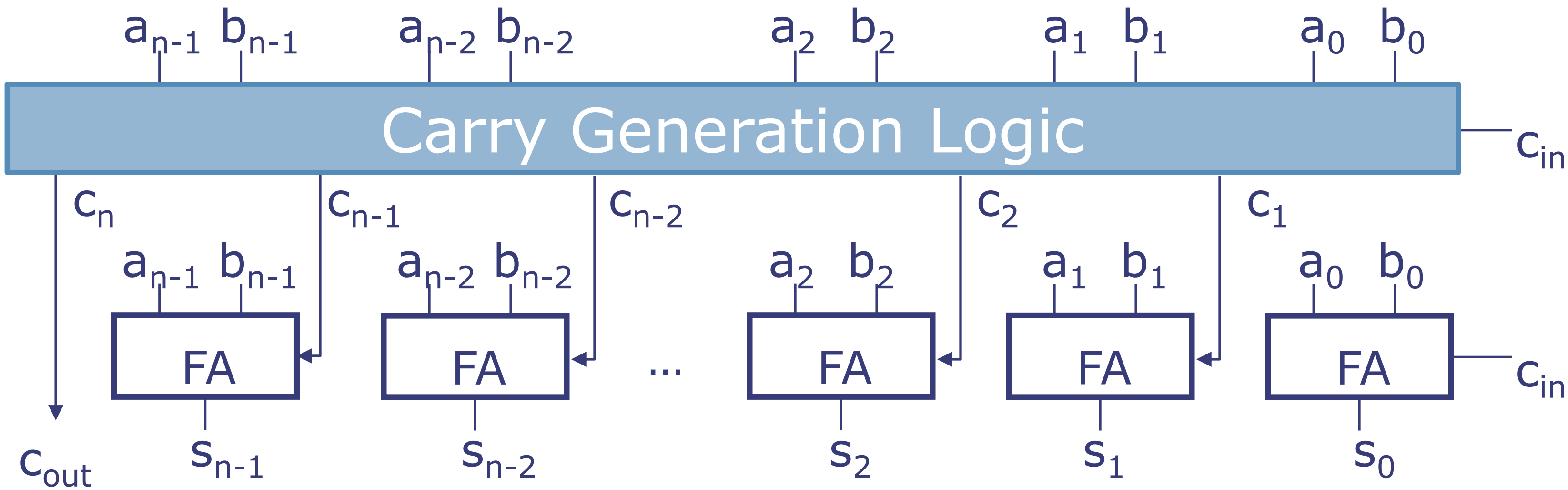

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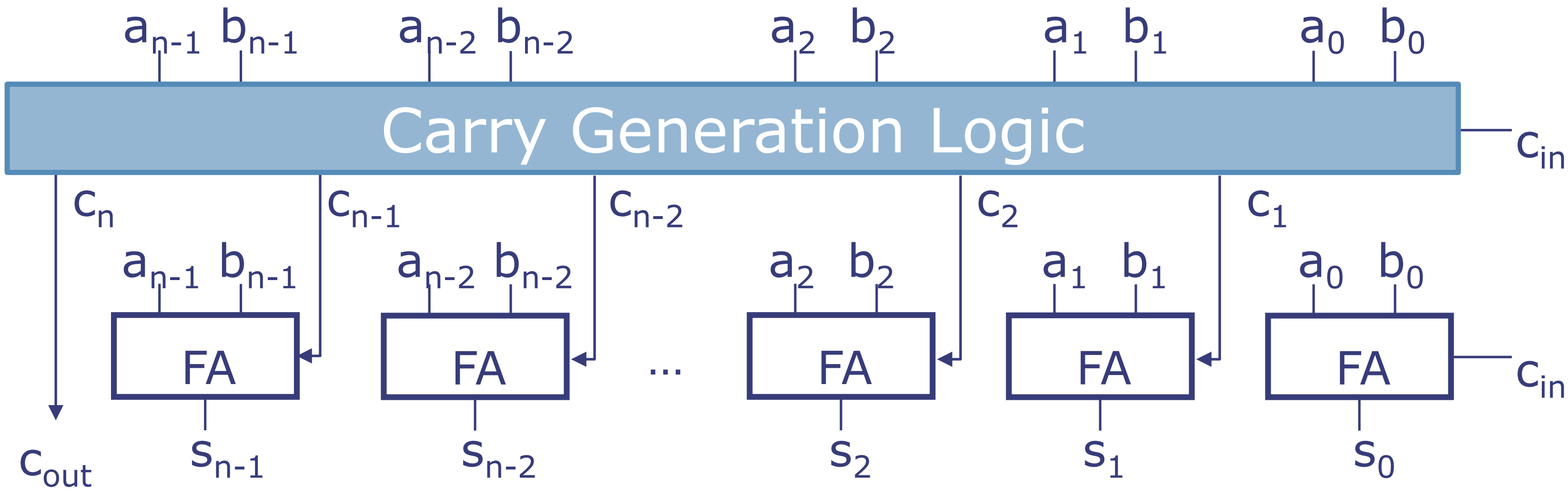

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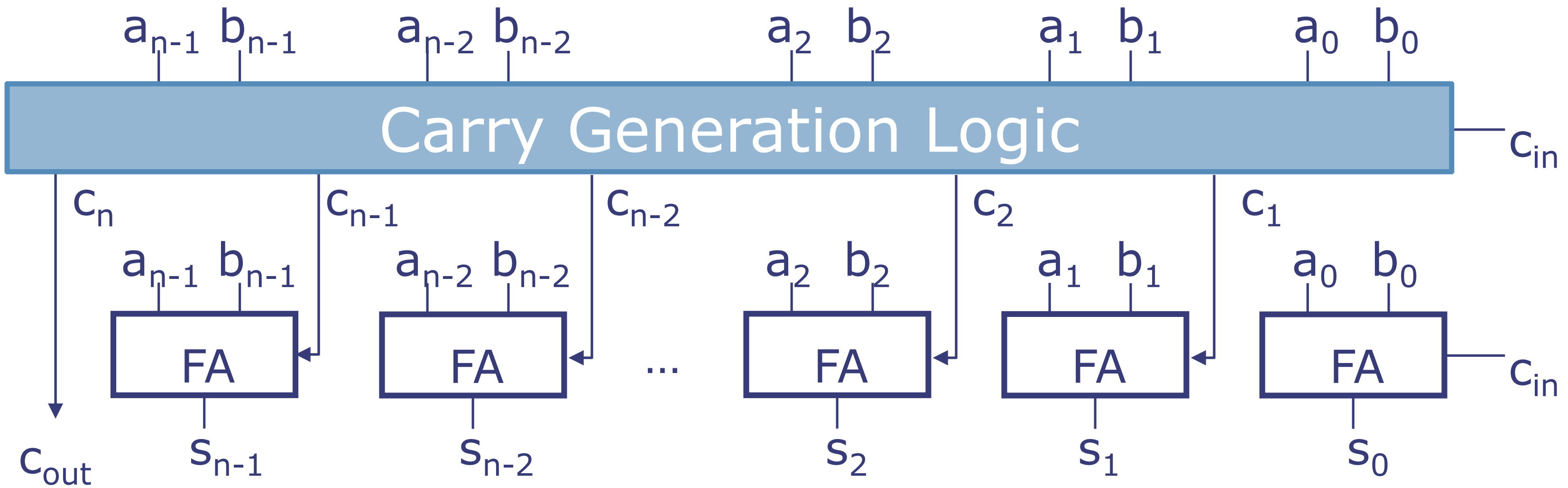

- Key idea: Transform chain of carry computations into a tree
  - Transforming a chain of associative operations (e.g., AND, OR, XOR) into a tree is easy
  - But how to do this with carries?

Carry-Lookahead Adder Details

NOTE: Remaining slides are optional material that will not be on a quiz but will be helpful for Lab 4 and the Design Project

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  - Step 2 uses the parallel scan (a.k.a. parallel prefix) algorithm

Function composition is associative
Basic math reminder ☺

Function compo

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Fu $f 1 \circ f 2 \circ f 3 = (f 1 \circ f 2) \circ f 3 = f 1 \circ (f 2 \circ f 3$
$)$

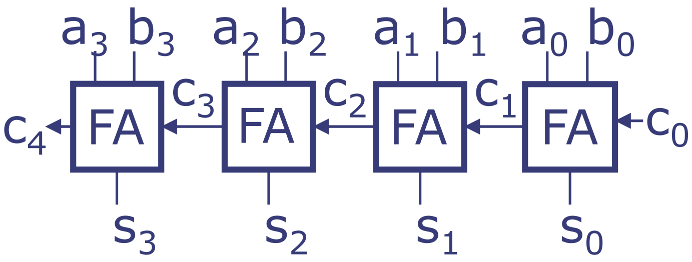
3 3 3 2 2 2 1 1 3 3 3 2 2 1 1 1 3 3 2 2 2 1 1 1

- Function composition is always associative:

$\circ f_2 \circ f_3 = (f_1 \circ f_2) \circ f_3 = f_1 \circ (f_2 \circ f_3$

Deriving carry-out in Θ(log n) delay

- Consider a ripple-carry adder:



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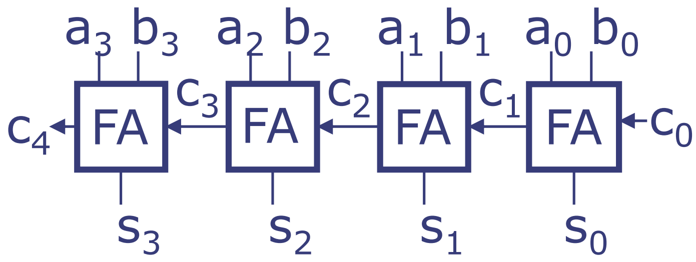

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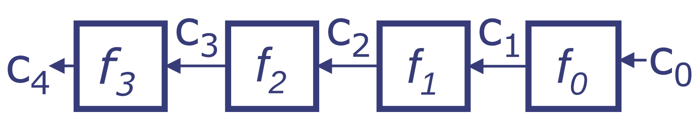

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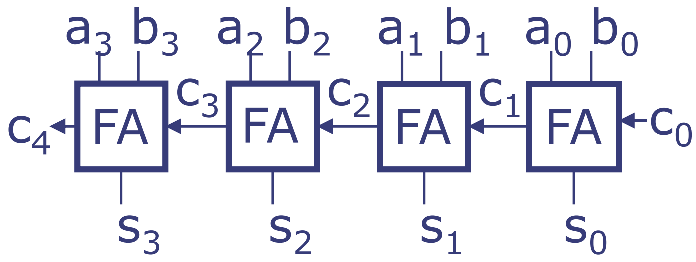

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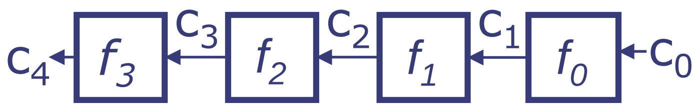

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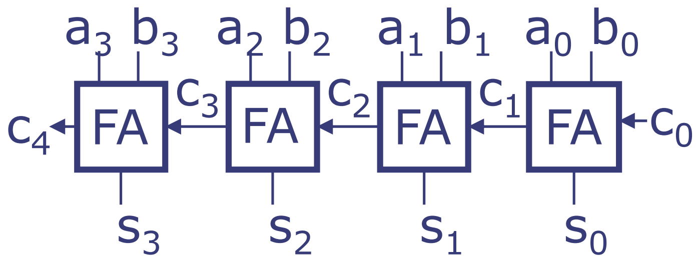

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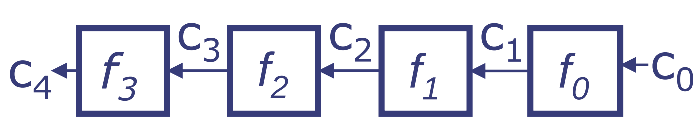
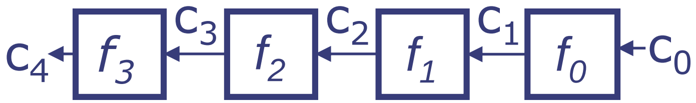


  - A chain of functions f_i , each with 1-bit input and output
  - Each f_i is determined by the values of a_i and b_i

Turning function chains into trees

- Because function composition is associative, we can turn a chain of functions into a tree by first composing the functions…



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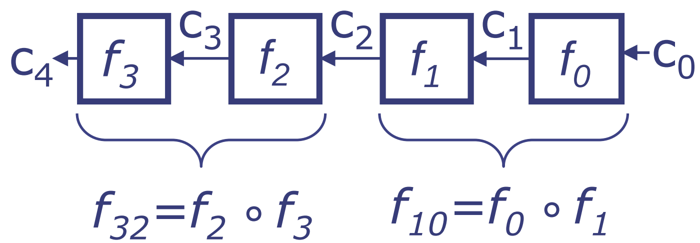
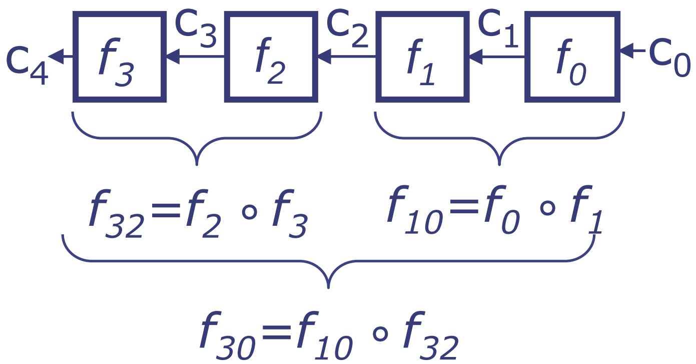


Turning function chains into trees

- Because function composition is associative, we can turn a chain of functions into a tree by first composing the functions…



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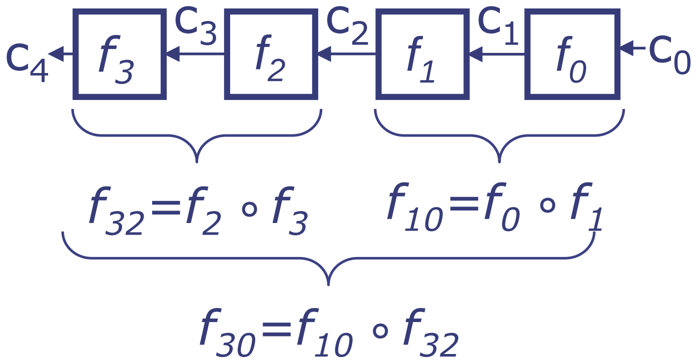

…and then evaluating the final function: $c_4=f_{30}(c_0)$

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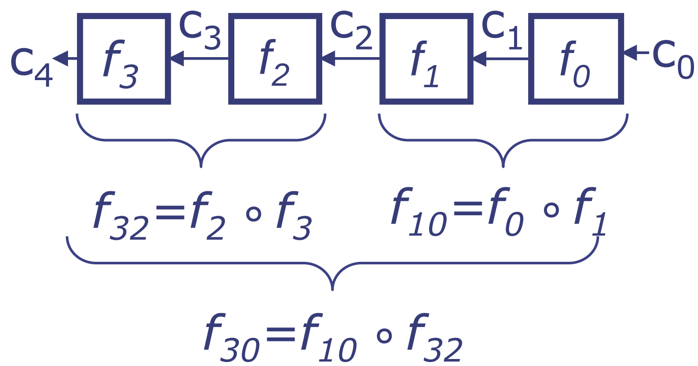

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How does delay grow with chain length n?

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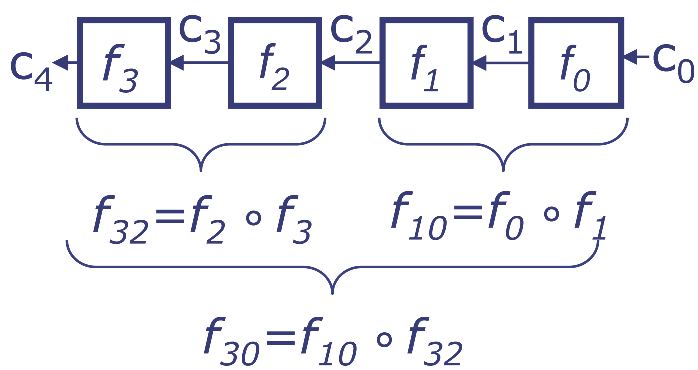

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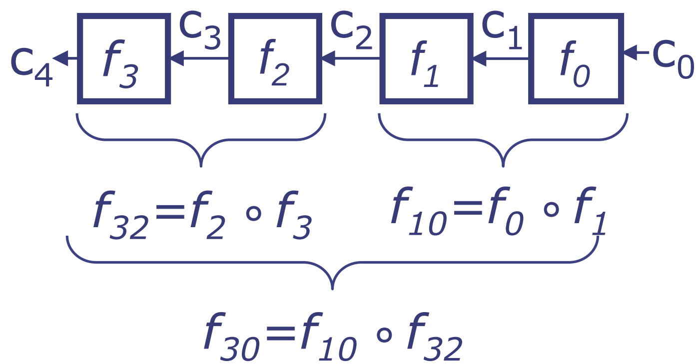

…and then evaluating the final function: $c_4=f_{30}(c_0)$

How does delay grow with chain length n? $\Theta(\log n)$

- Very general trick: Can turn any chain of functions into a tree, *if you can compose them efficiently*

1-bit input, 1-bit output functions

in	out
0	0
1	0

in	out
0	0
1	1

in	out
0	1
1	1

in	out
0	1
1	0

1-bit input, 1-bit output functions

kill

in	out
0	0
1	0

in	out
0	0
1	1

in	out
0	1
1	1

in	out
0	1
1	0

1-bit input, 1-bit output functions

kill

in	out
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1	0

in	out
0	0
1	1

generate

in	out
0	1
1	1

in	out
0	1
1	0

1-bit input, 1-bit output functions

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in	out
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1	0

propagate

in	out
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invert

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in	out
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- *How many bits do we need to enumerate these functions?*

1-bit input, 1-bit output functions

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in	out
0	0
1	0

propagate

in	out
0	0
1	1

generate

in	out
0	1
1	1

invert

in	out
0	1
1	0

- *How many bits do we need to enumerate these functions?* 2 bits (only 4 choices!)

Composing 1-bit functions

f	g	f ∘ g
kill	kill	
kill	generate	
kill	propagate	
kill	invert	
generate	kill	
generate	generate	
generate	propagate	
generate	invert	
propagate	kill	
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This is just a combinational function with two 2-bit inputs and one 2-bit output!

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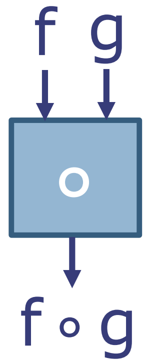
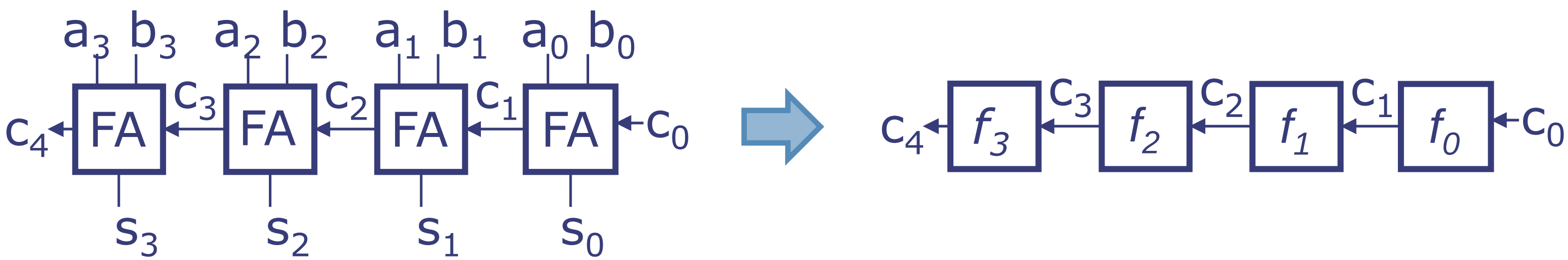


Deriving the initial functions

- Remember, to derive the carry-out, a ripple-carry adder can be seen as a chain of functions f_i , each determined by the values of a_i and b_i



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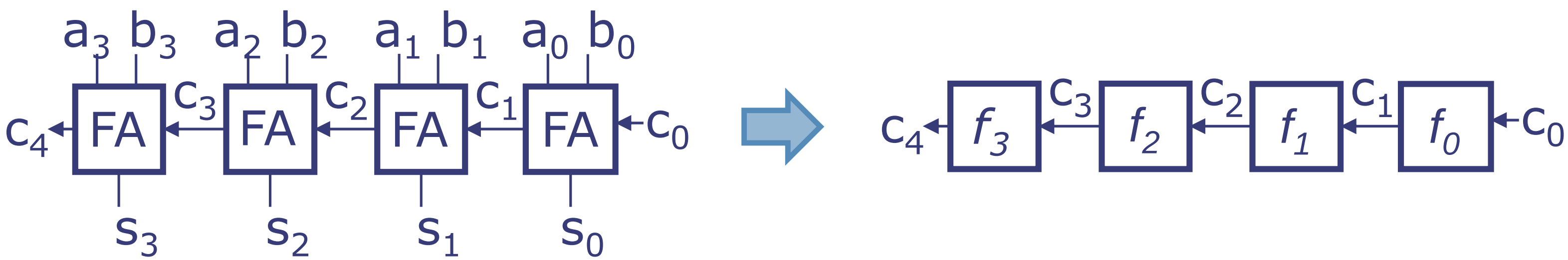

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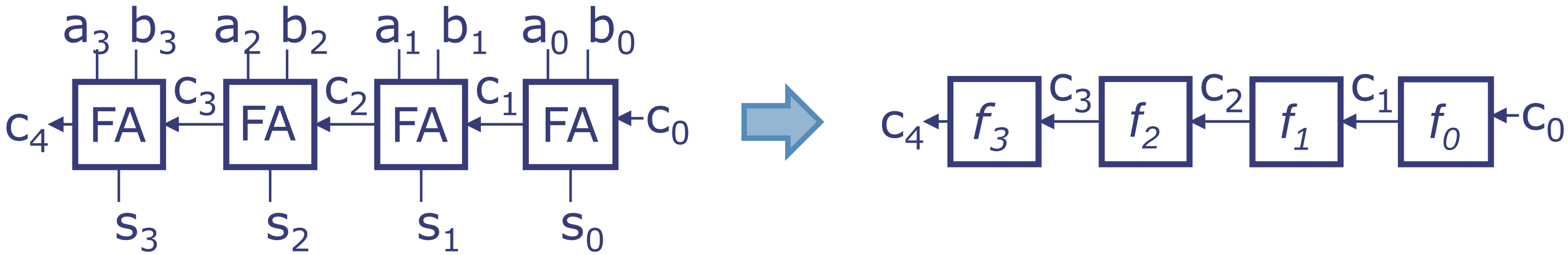

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a	**b**	**c_{in}**	**c_{out}**
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
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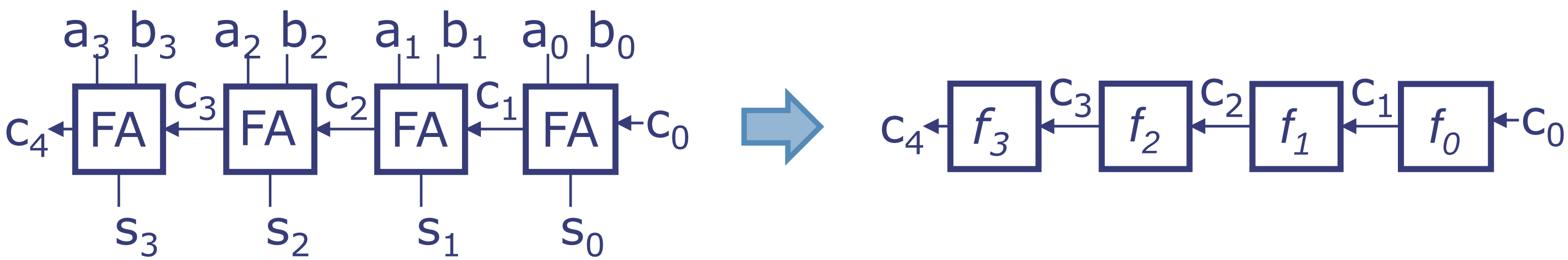

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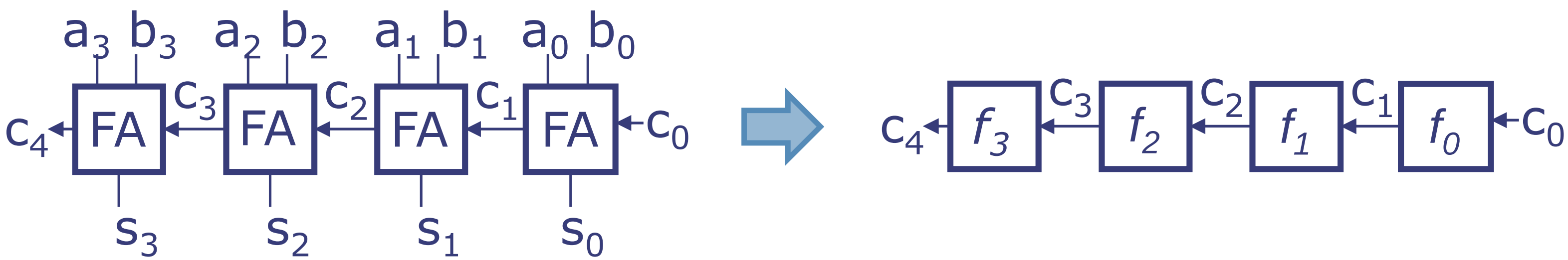

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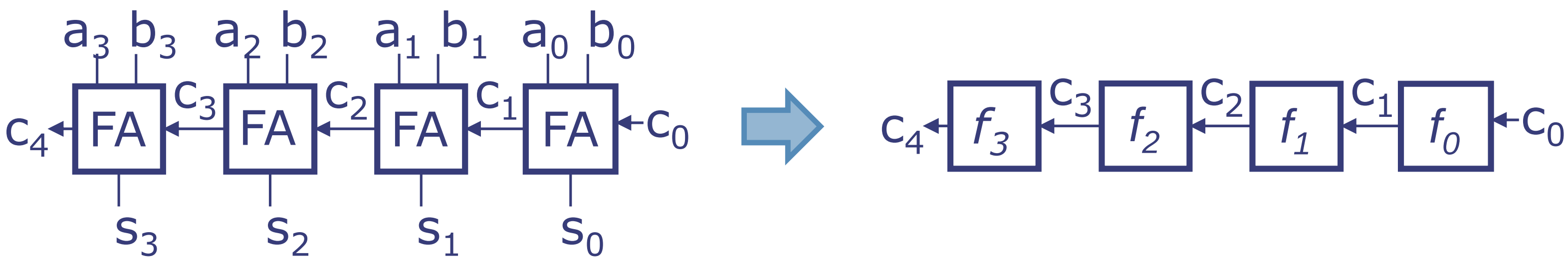

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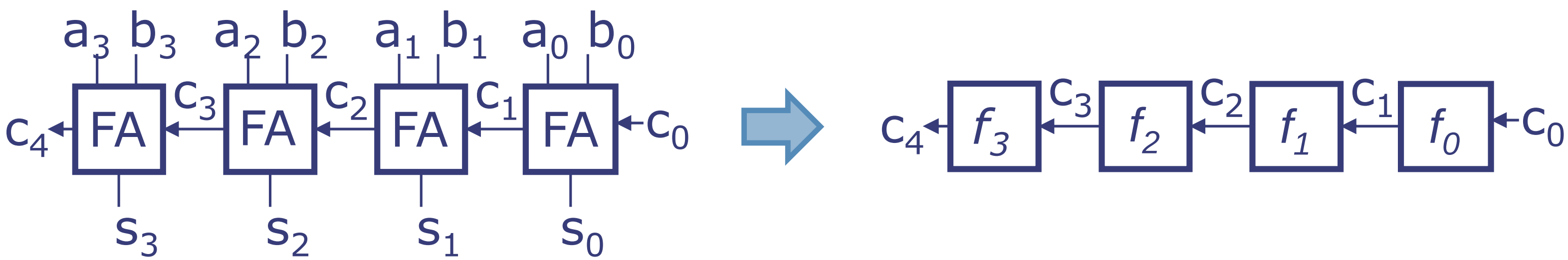

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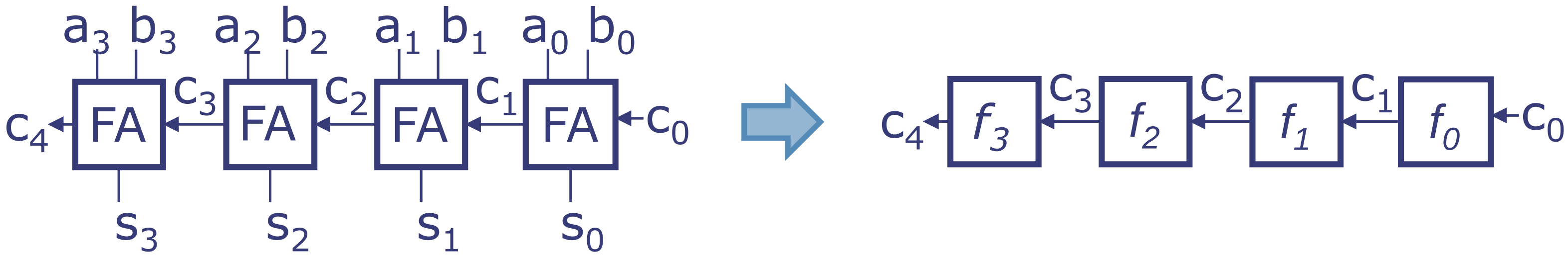

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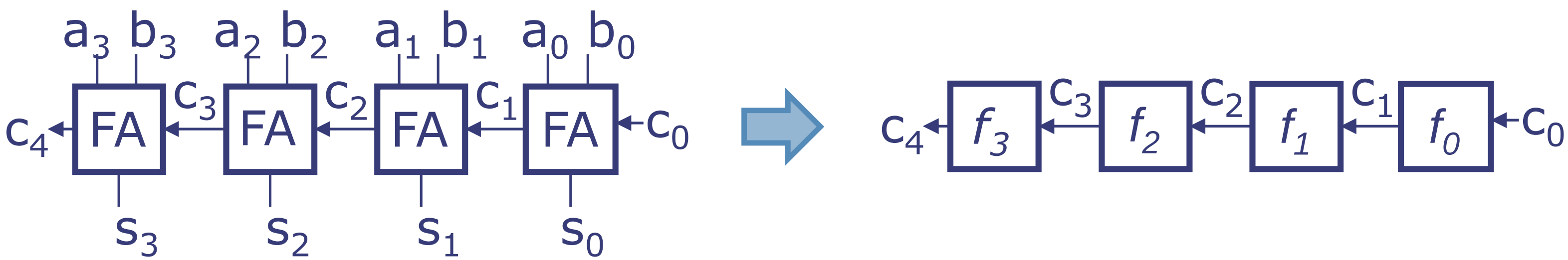

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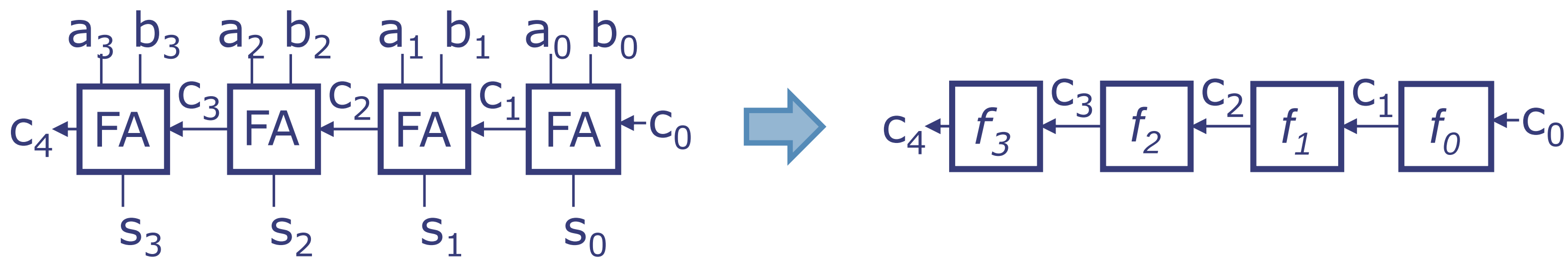

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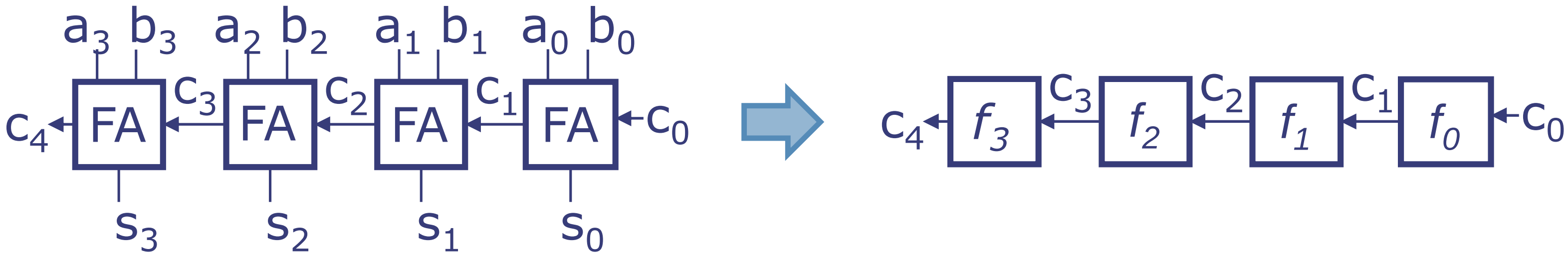

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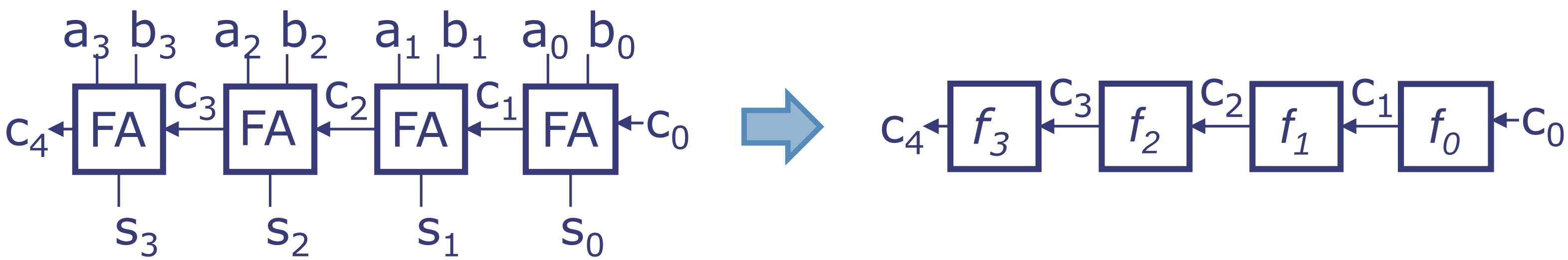

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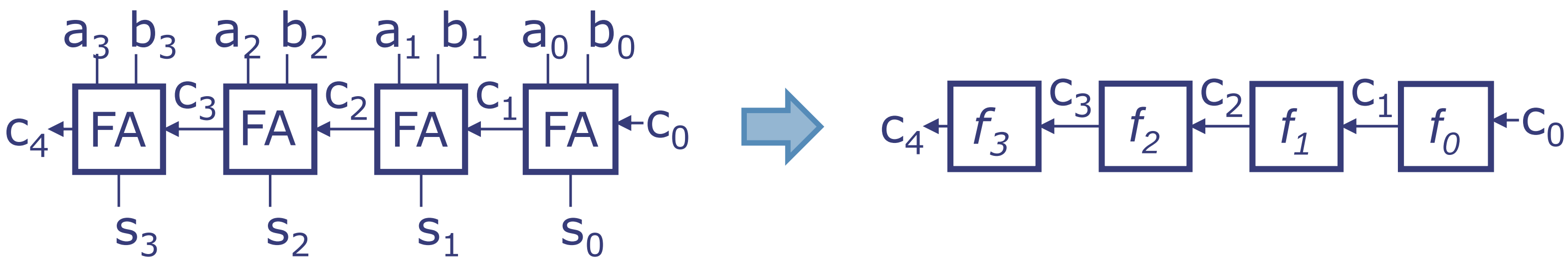

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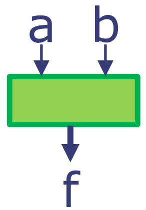

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generate	0	1
generate	1	1
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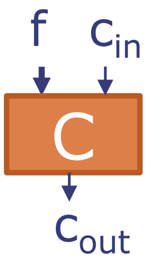
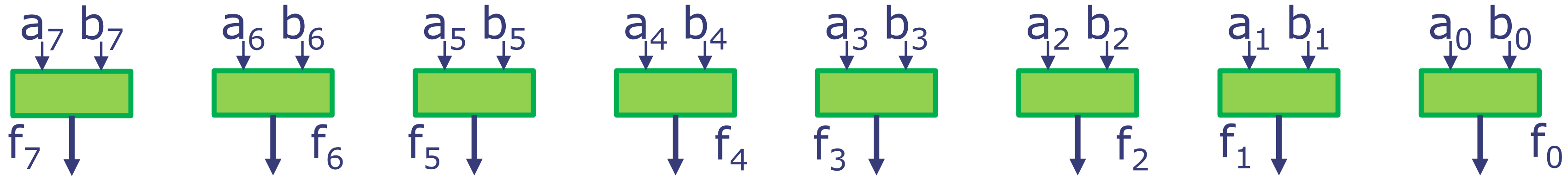


Step 1: Generating the output carry
Putting it all together



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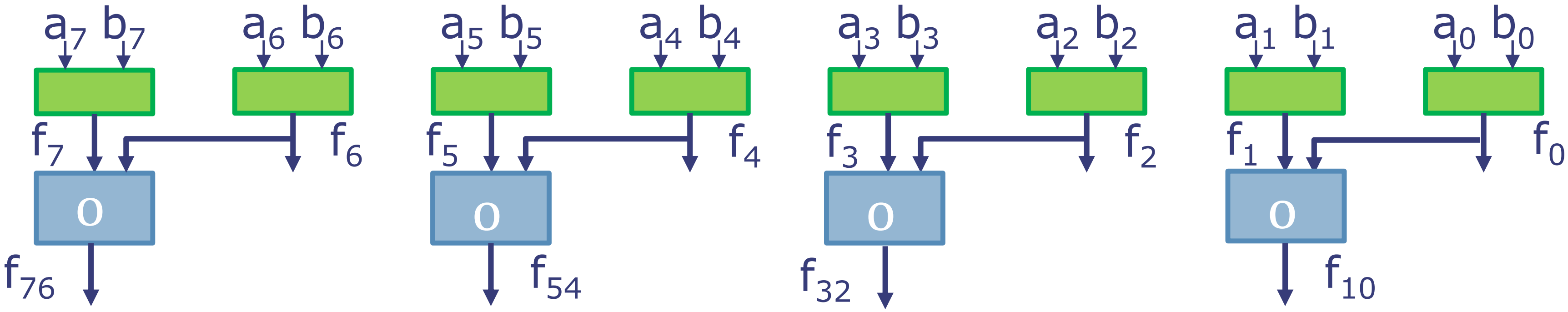

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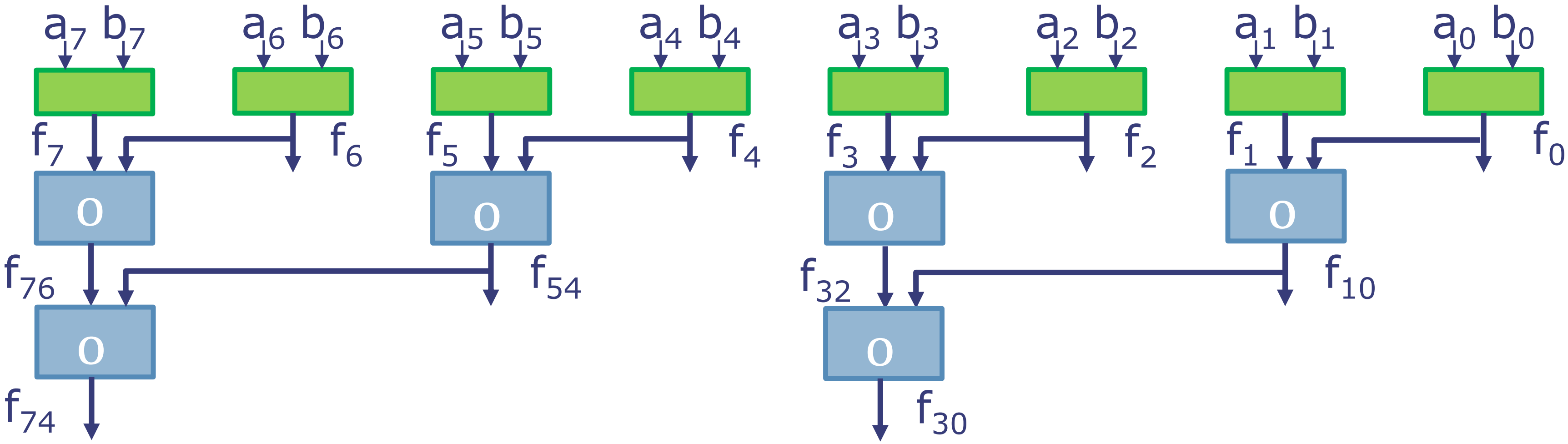

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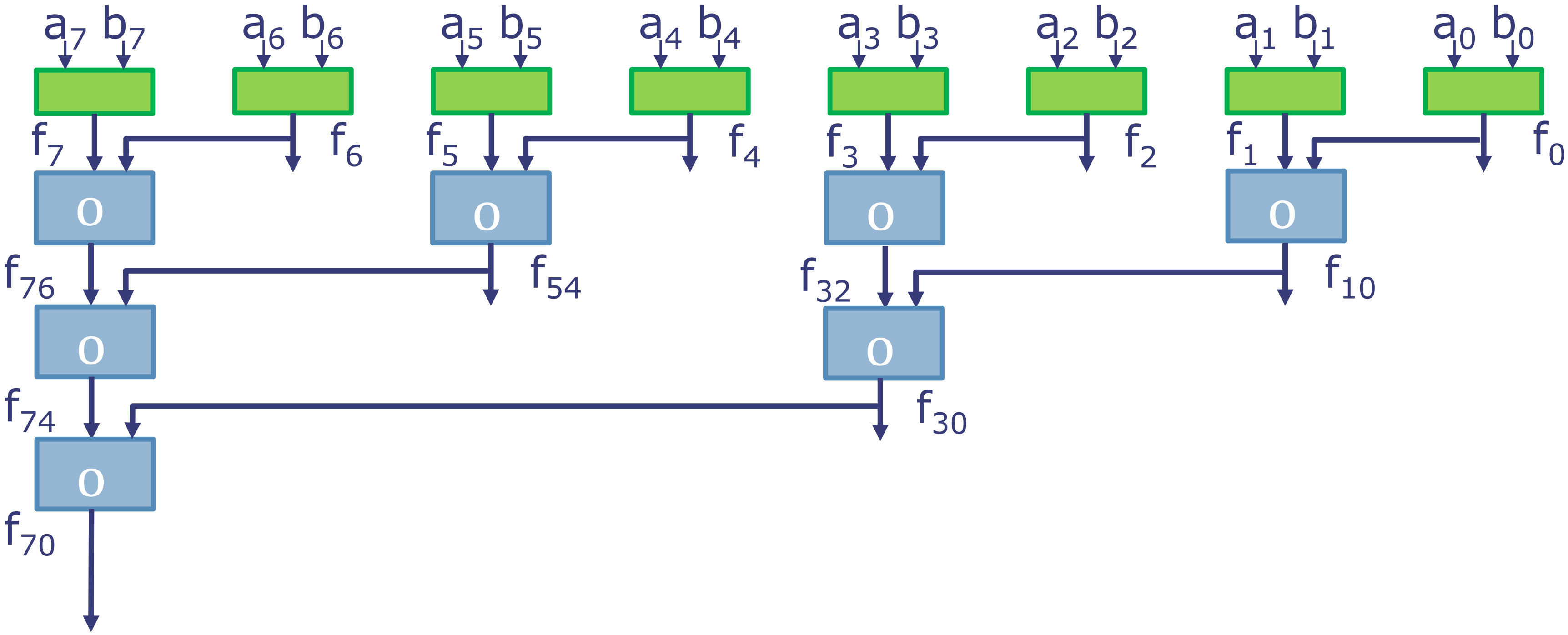

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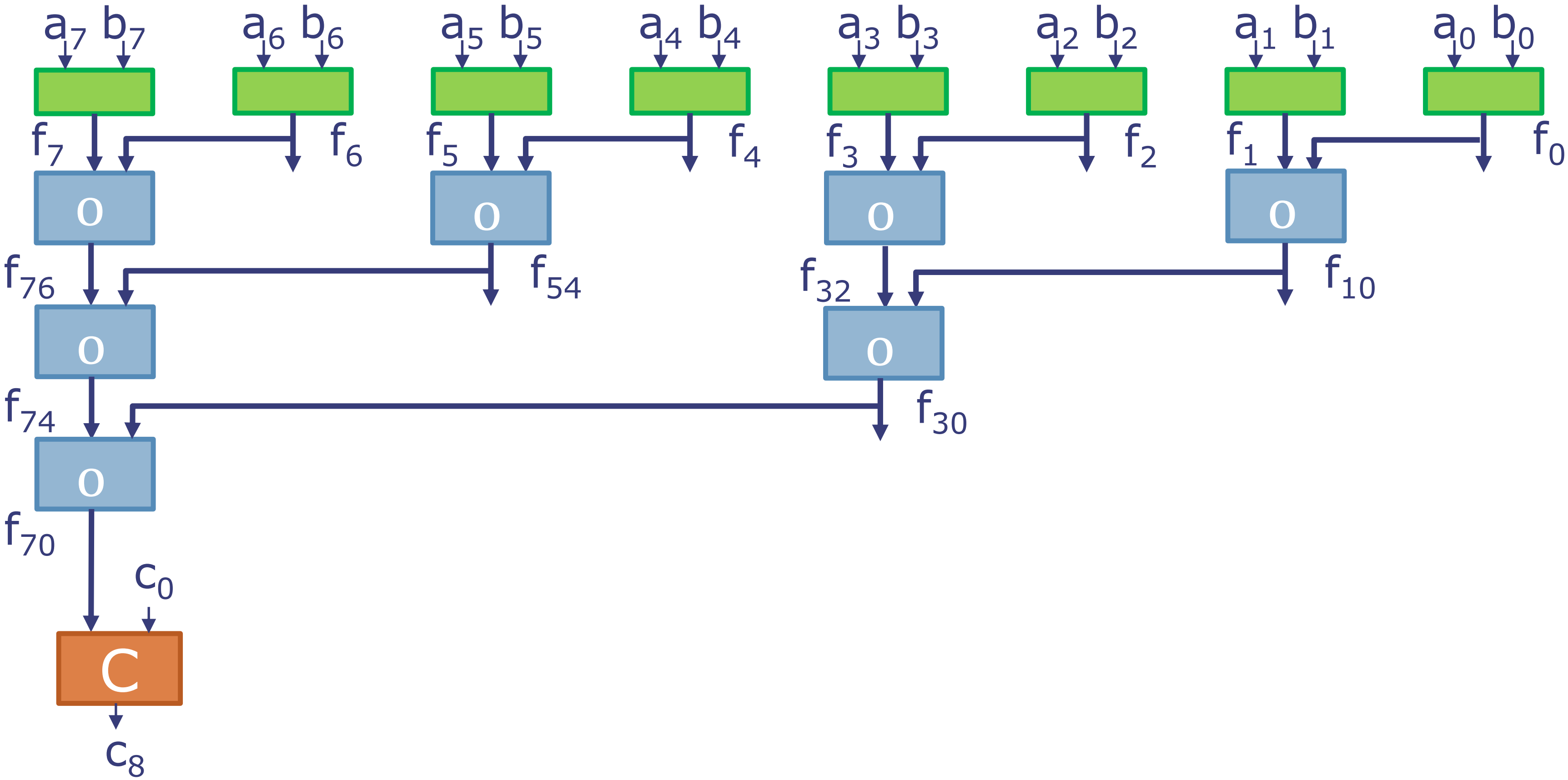

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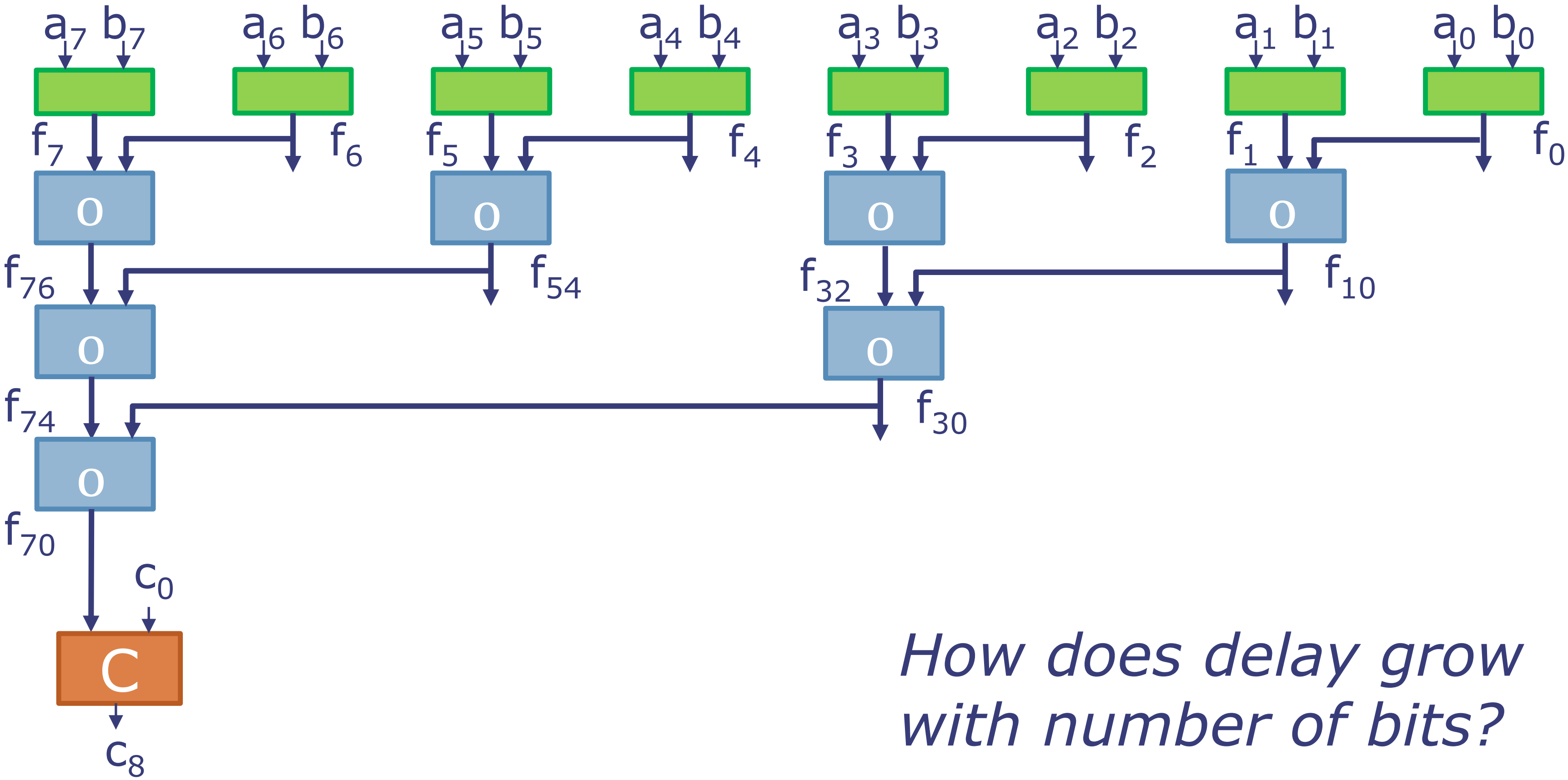

How does delay grow with number of bits?

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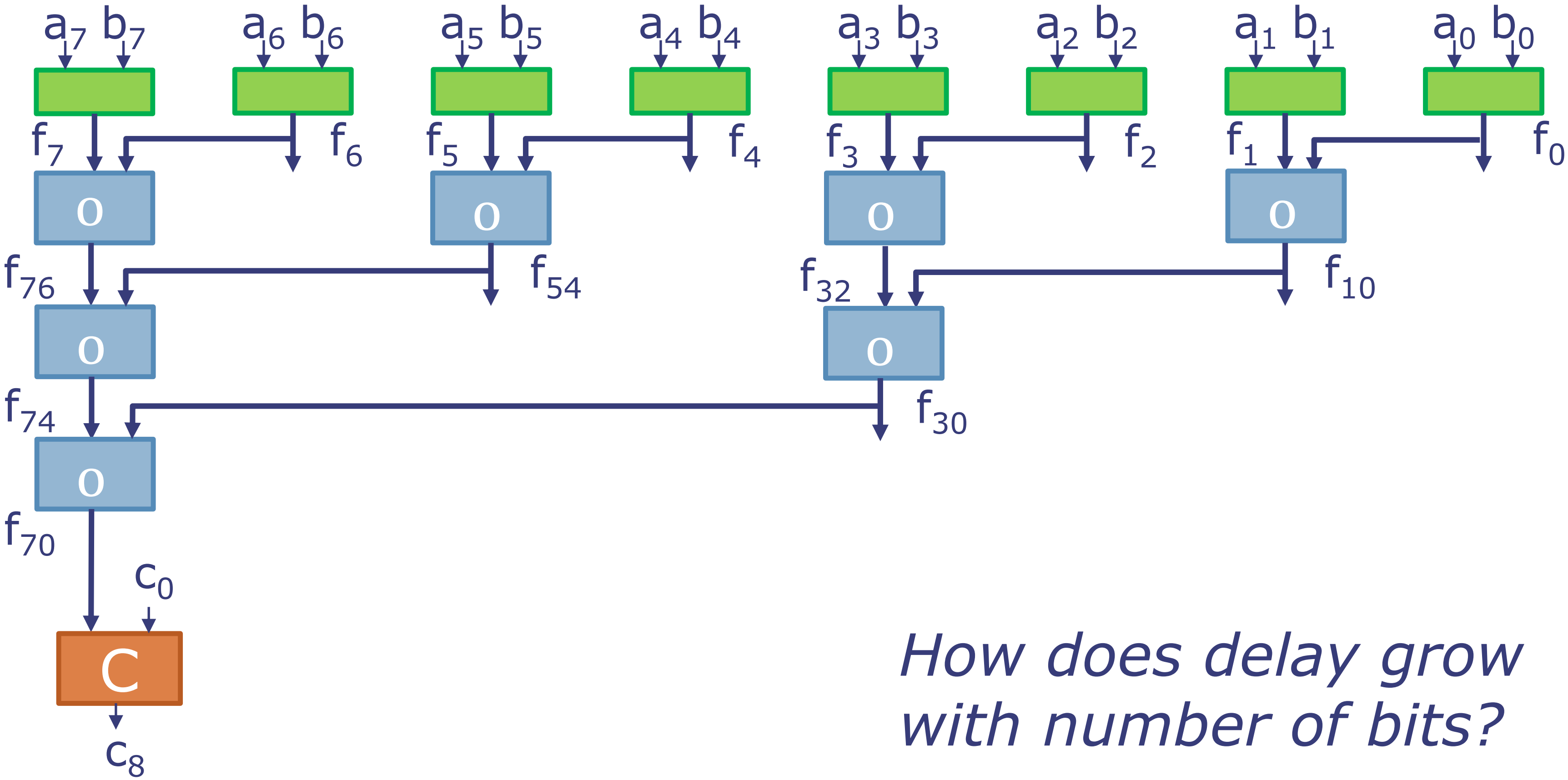

How does delay grow with number of bits?

Θ(log n)

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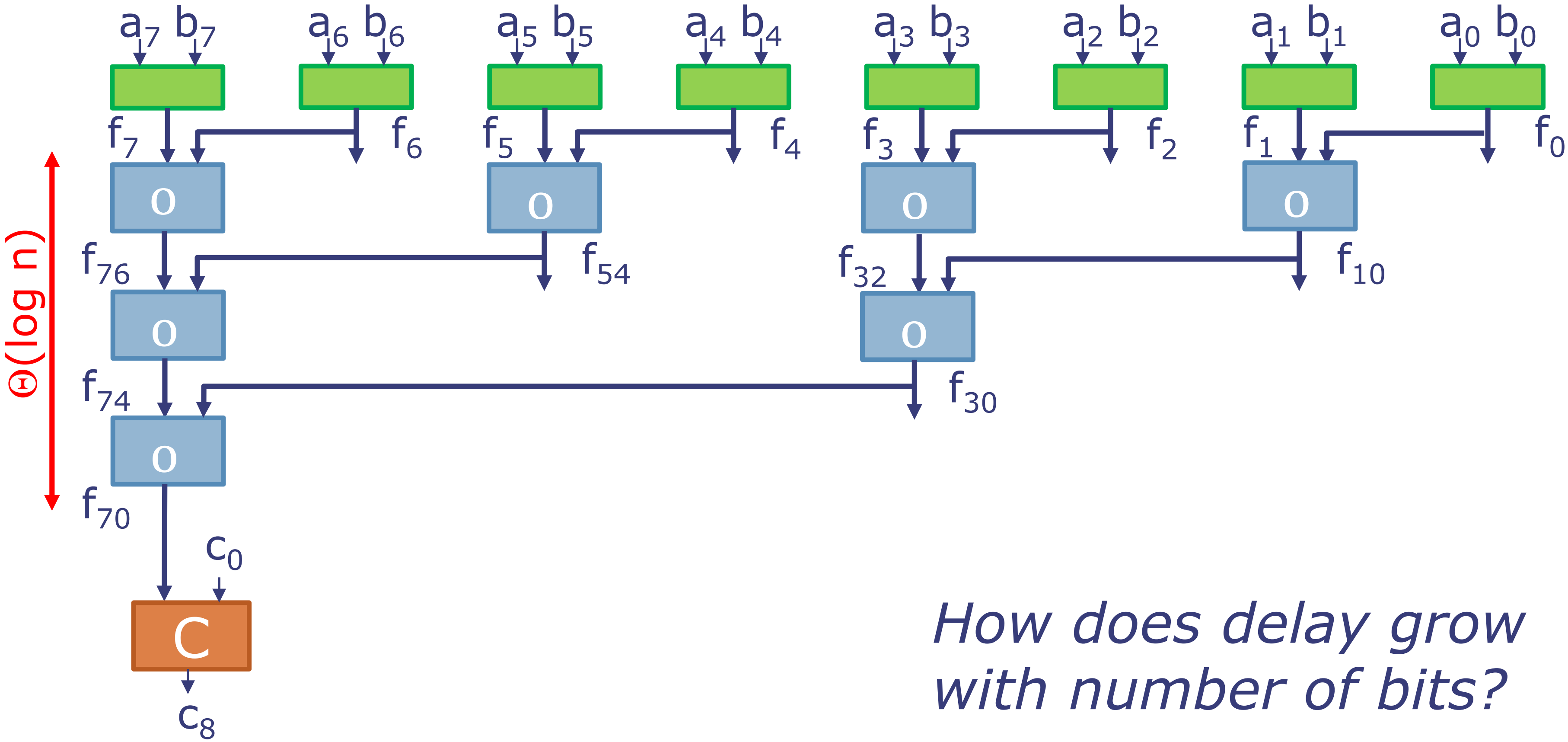

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- So far we have seen how to generate a single output carry, but we need all intermediate ones too
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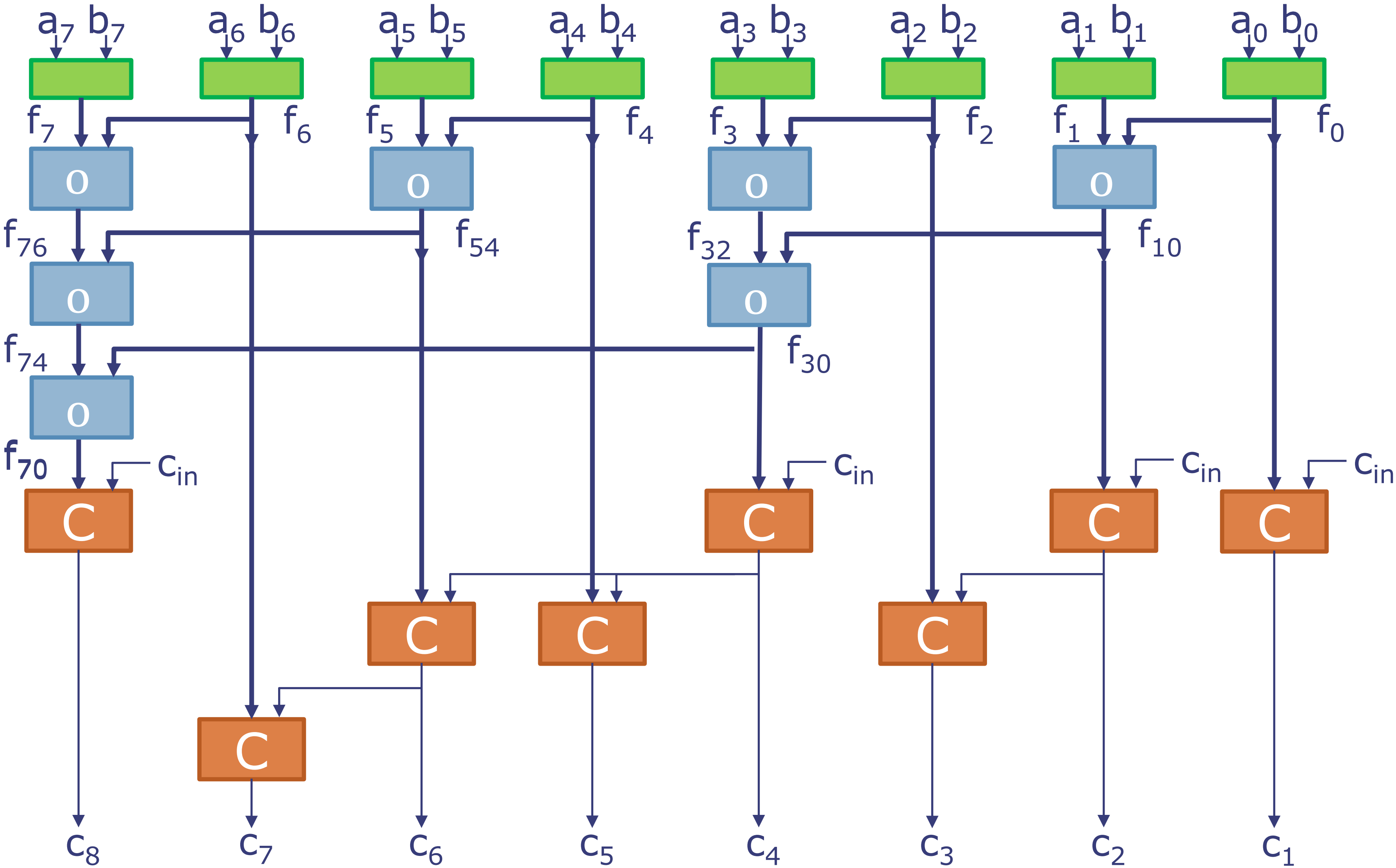
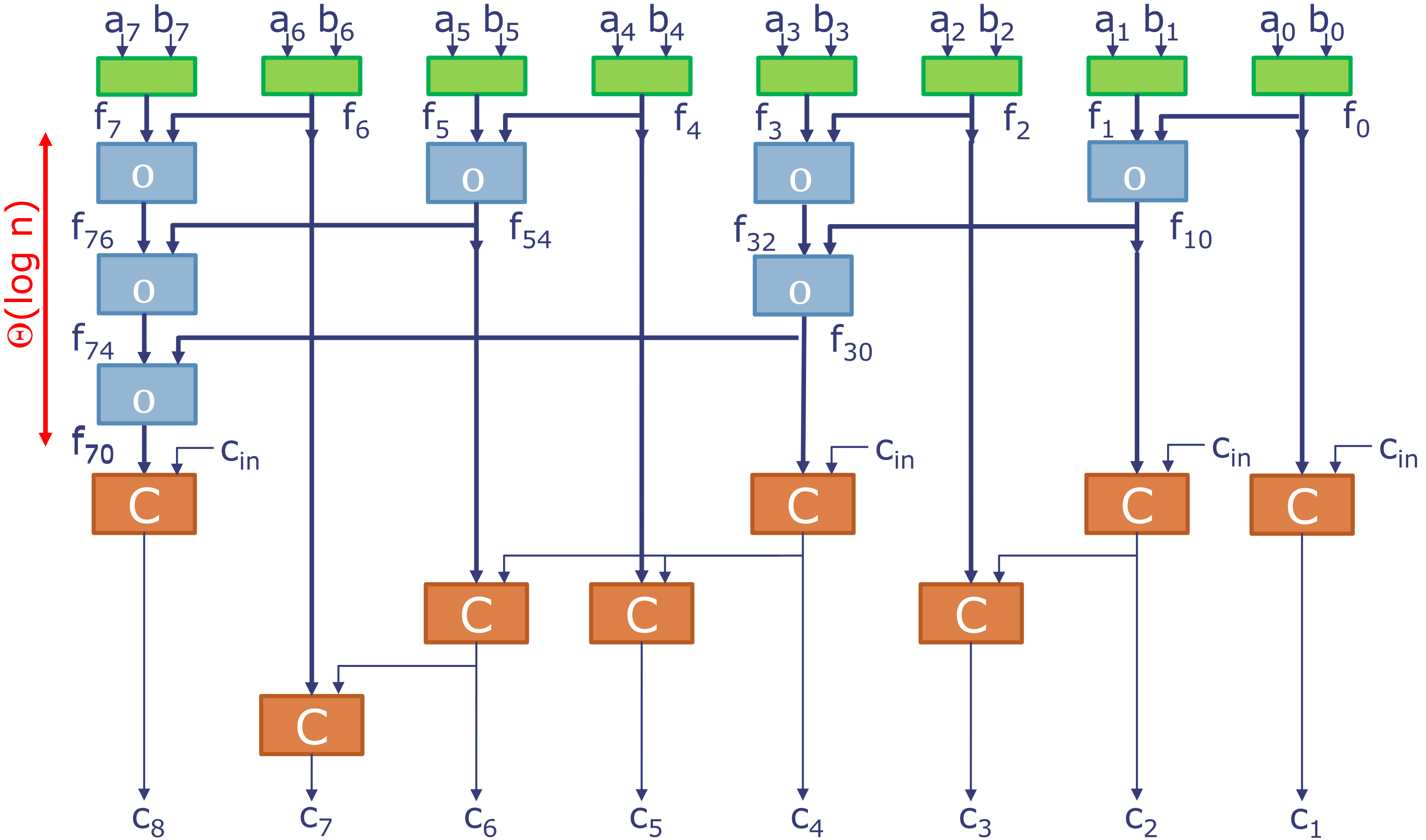
- Two main options:
  - Brent-Kung CLA: Low area but some extra delay
  - Kogge-Stone CLA: High area but lower delay

Option 1: Brent-Kung CLA



Option 1: Brent-Kung CLA



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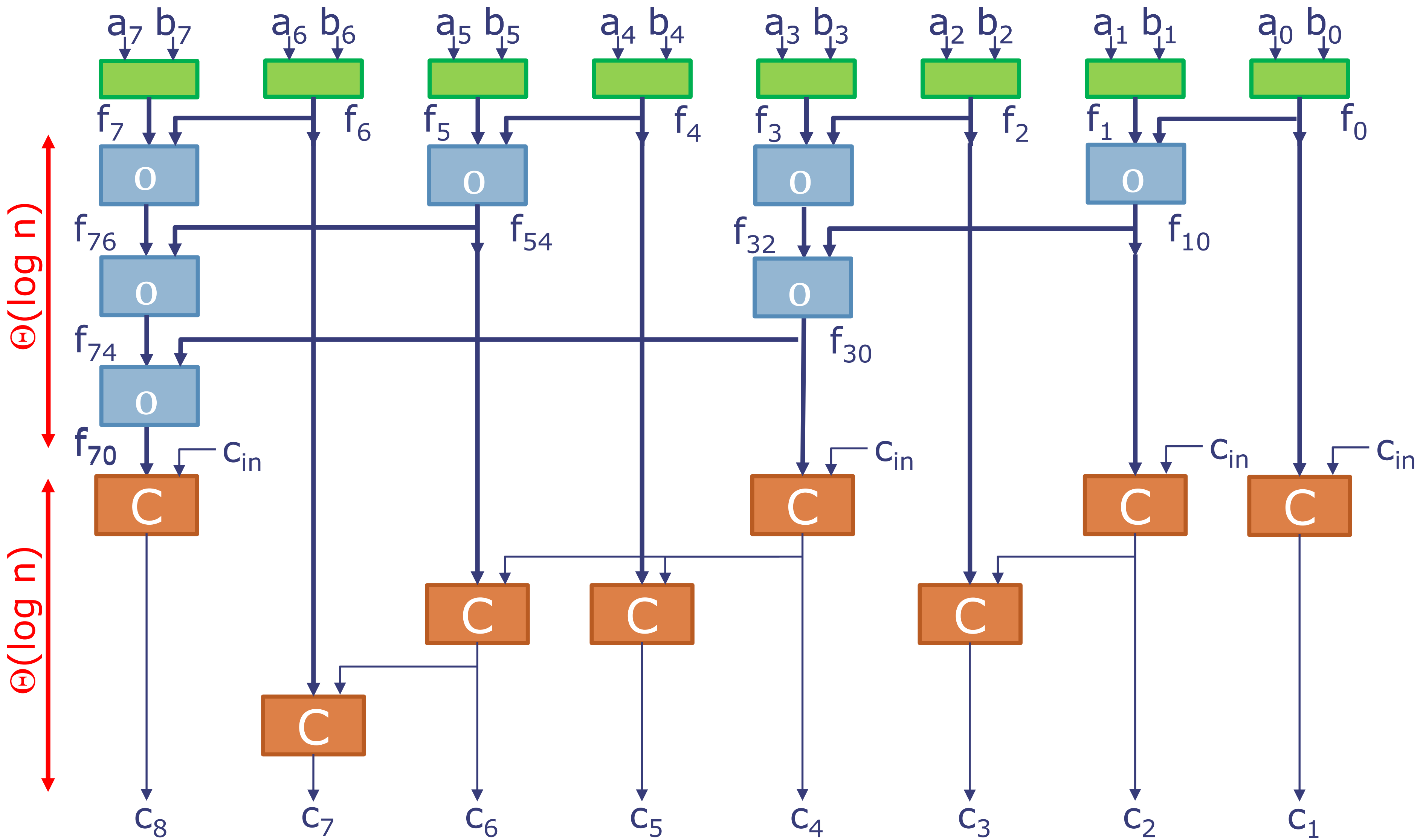
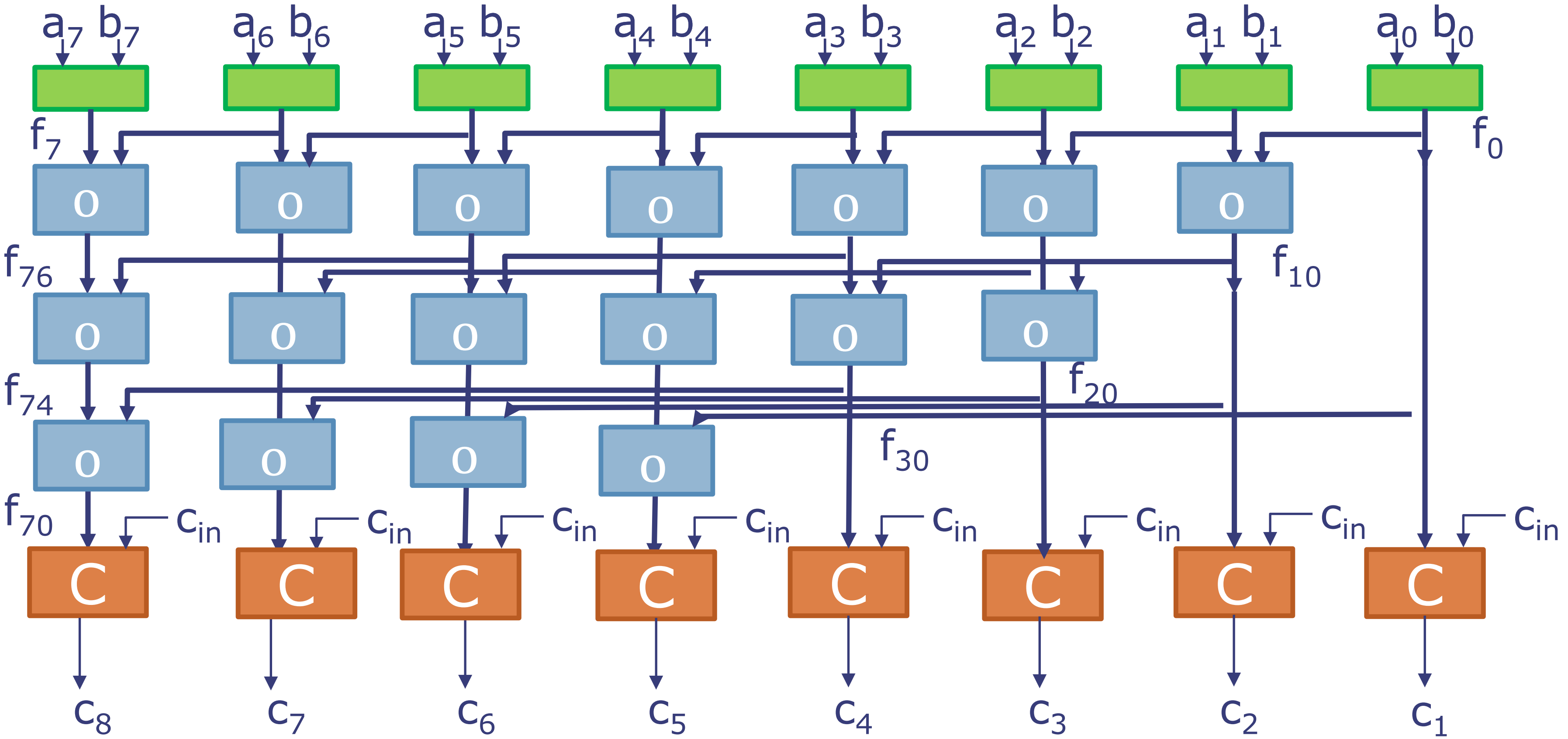


Option 2: Kogge-Stone CLA



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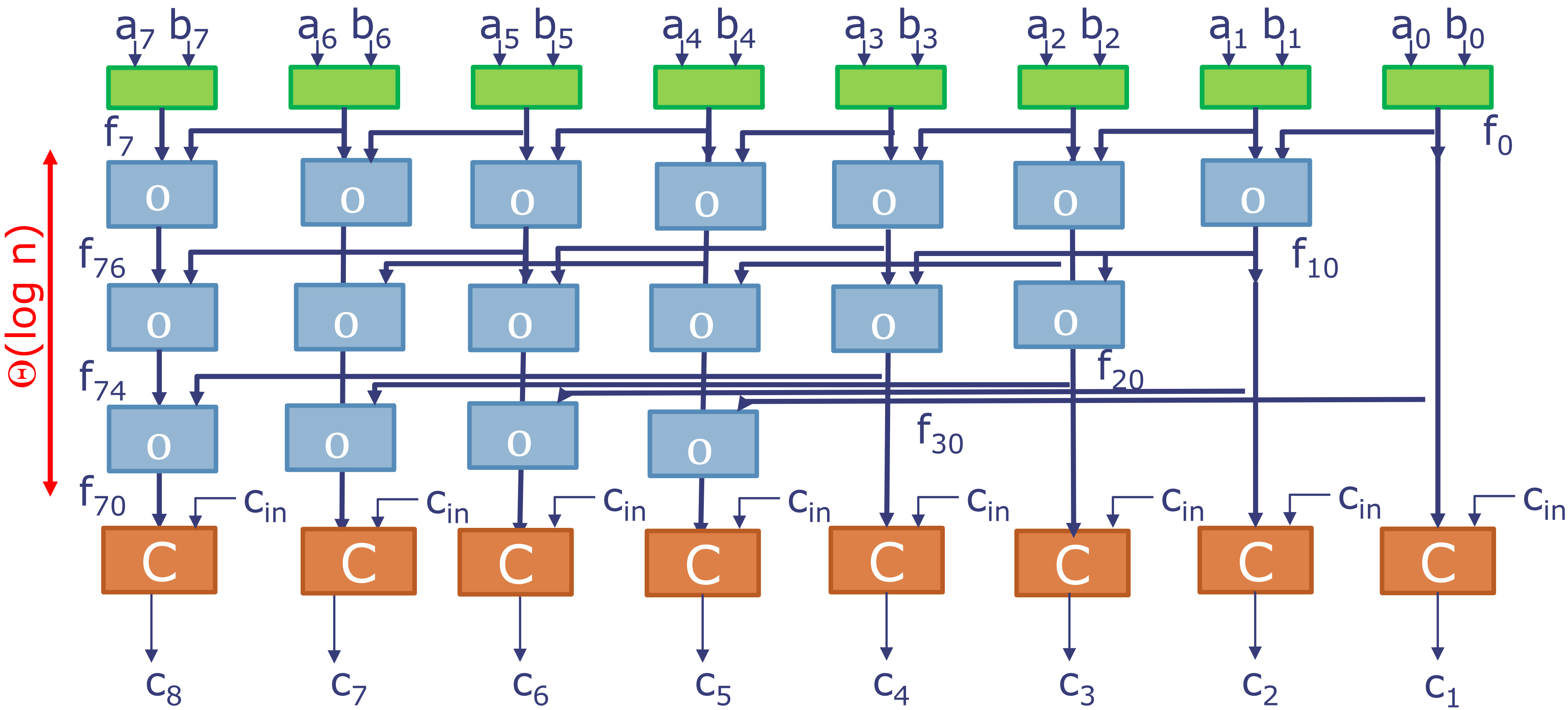

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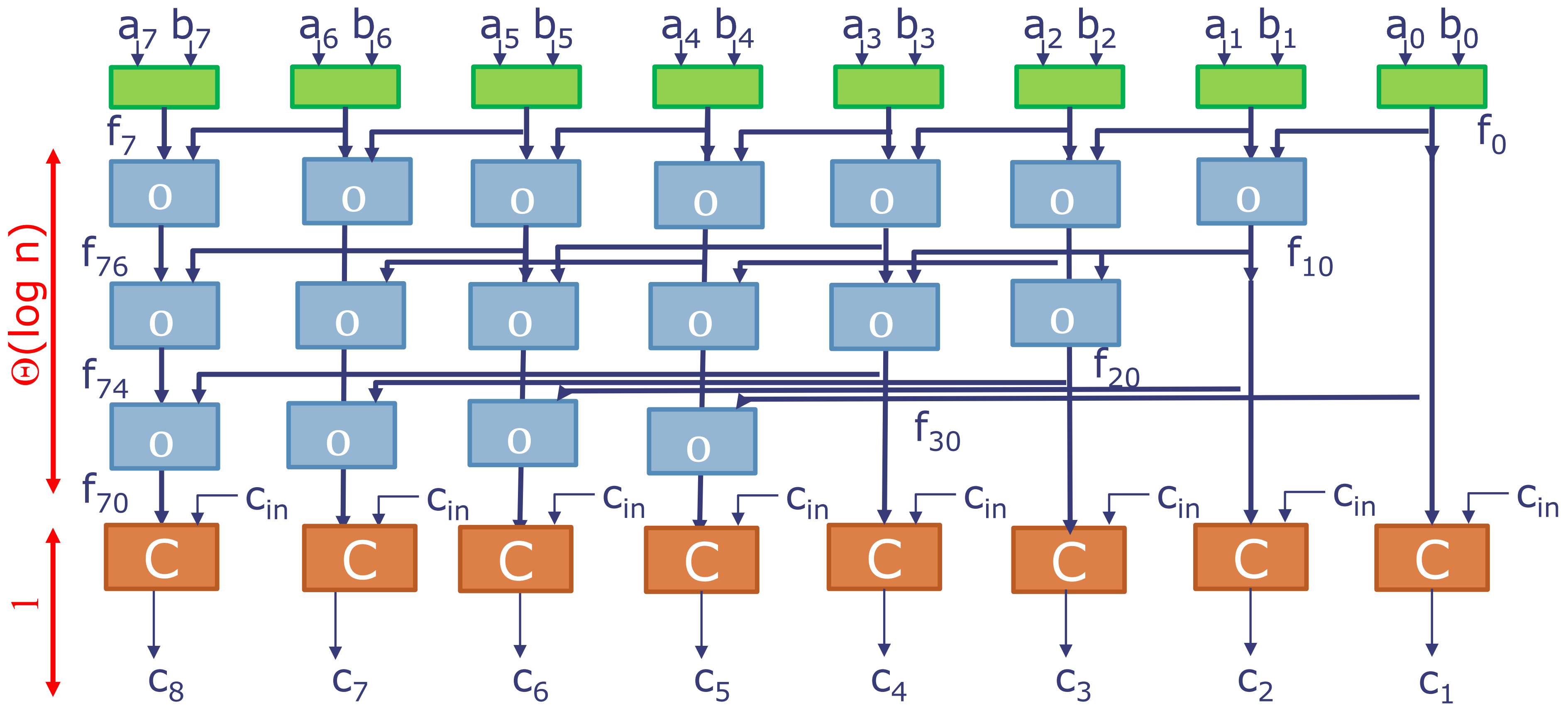

CLA Nitty-Gritty: Choosing a good encoding for functions

- CLAs need to encode three possible functions: kill, propagate, generate (invert is not used)
- 2-bits required per function, but 3 values, so how they are encoded can affect logic cost

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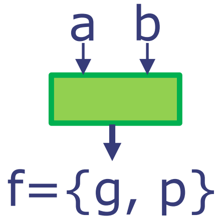
- A common encoding is f = {g, p}, where:
  - g = ab   (generate bit)
  - p = a+b (propagate bit)

- With this encoding,
  - g = 0, p = 0 → kill
  - g = 0, p = 1 → propagate
  - g = 1, p = X → generate

CLA Building Blocks
with f ={g, p} encoding

- Produce initial f signals



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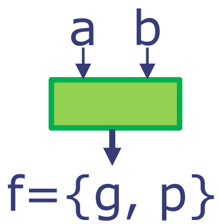

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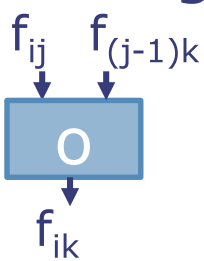

$$g_{ik} = g_{ij} + p_{ij}g_{(j-1)k}$$
$$p_{ik} = p_{ij}p_{(j-1)k} \qquad (i \geq j > k)$$

CLA Building Blocks
with f ={g, p} encoding

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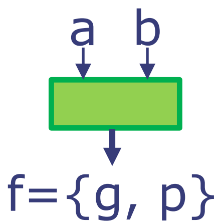

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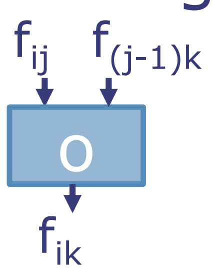

$$g_{ik} = g_{ij} + p_{ij}g_{(j-1)k}$$
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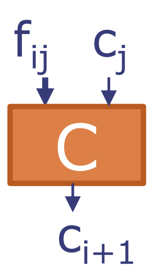
- Produce individual carries



$$c_{i+1} = g_{ij} + p_{ij}c_j$$

Carry-Lookahead Adder Takeaways

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  - We’ve seen Brent-Kung and Kogge-Stone CLAs
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- There are many CLA designs
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- This technique is useful beyond adders: computes any one-dimensional recurrence in $\Theta(\log n)$ delay
  - e.g., comparators, priority encoders, etc.

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- Parametric functions let us write a generic description of a function that is then instantiated on demand
- Use for loops and if-else statements with care: their similarity to software can be confusing and they can lead to poor circuits
- Choosing the right algorithms is crucial to design good digital circuits—tools can only do so much!
- Carry-select and carry-lookahead adders achieve $\Theta(\log n)$ delay, but at the cost of extra area

Thank you!

Next lecture: Sequential Circuits