Design Tradeoffs in Sequential Circuits

Why Study Hardware Design?

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  - Past 50+ years: Exponential growth in transistors per chip (~2x/2 years)
  - Now/soon: How to improve performance without more or faster transistors?

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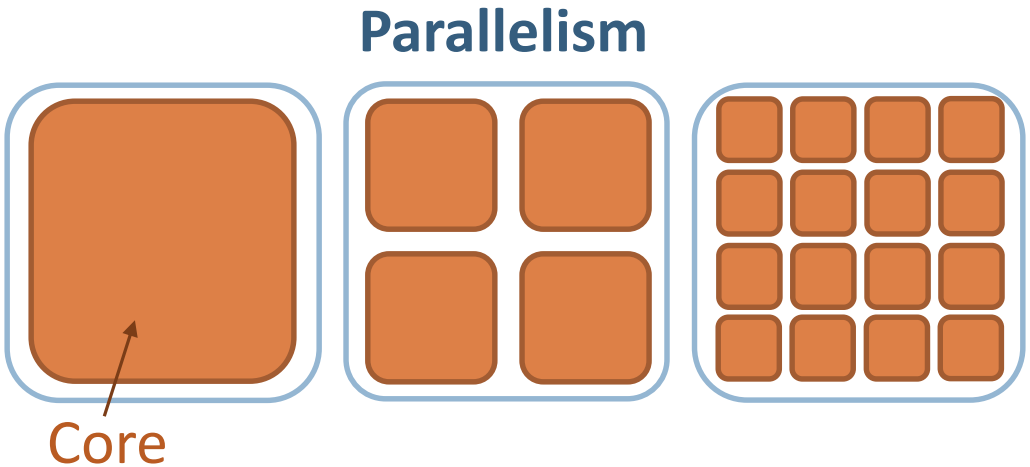

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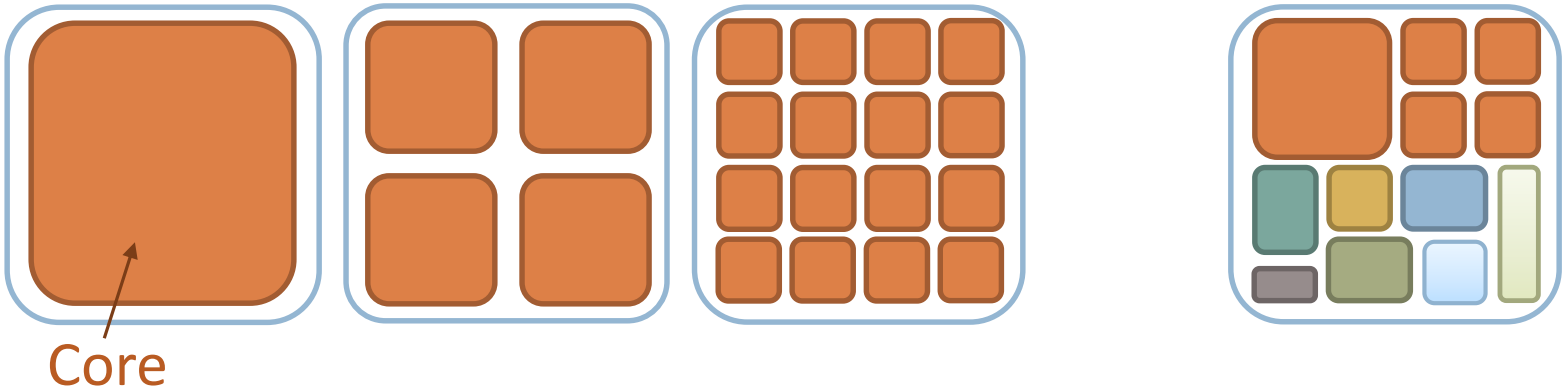

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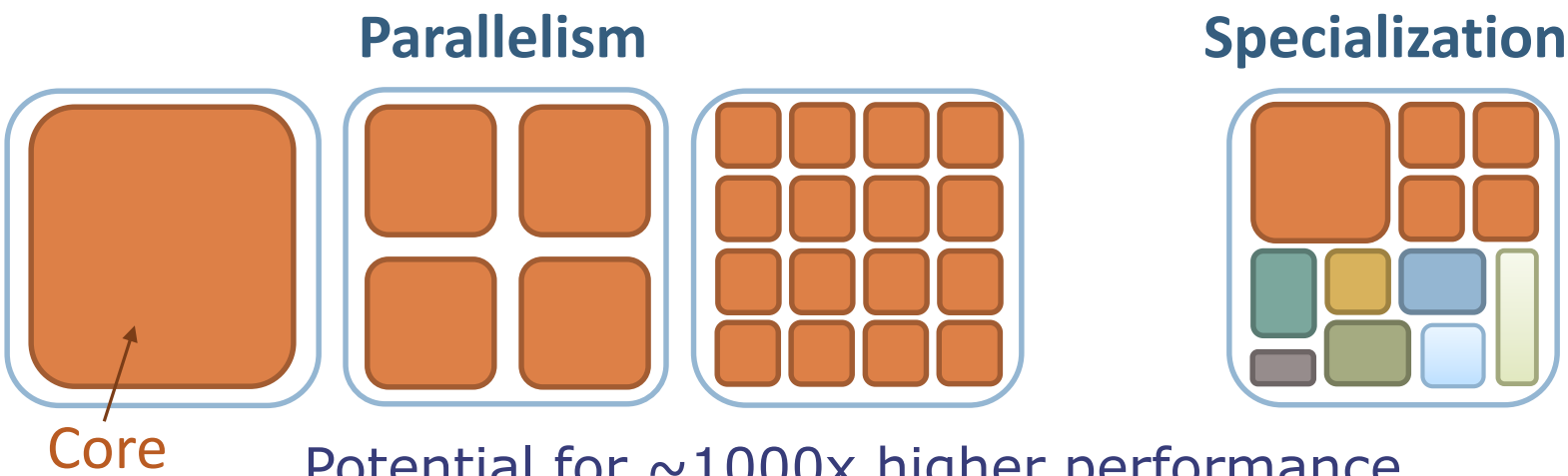

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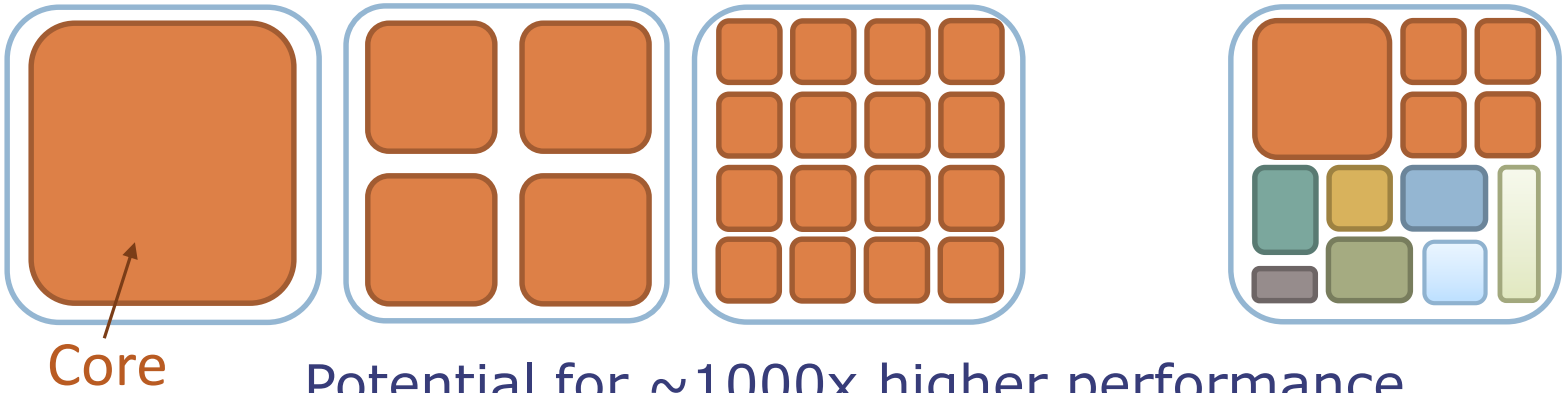

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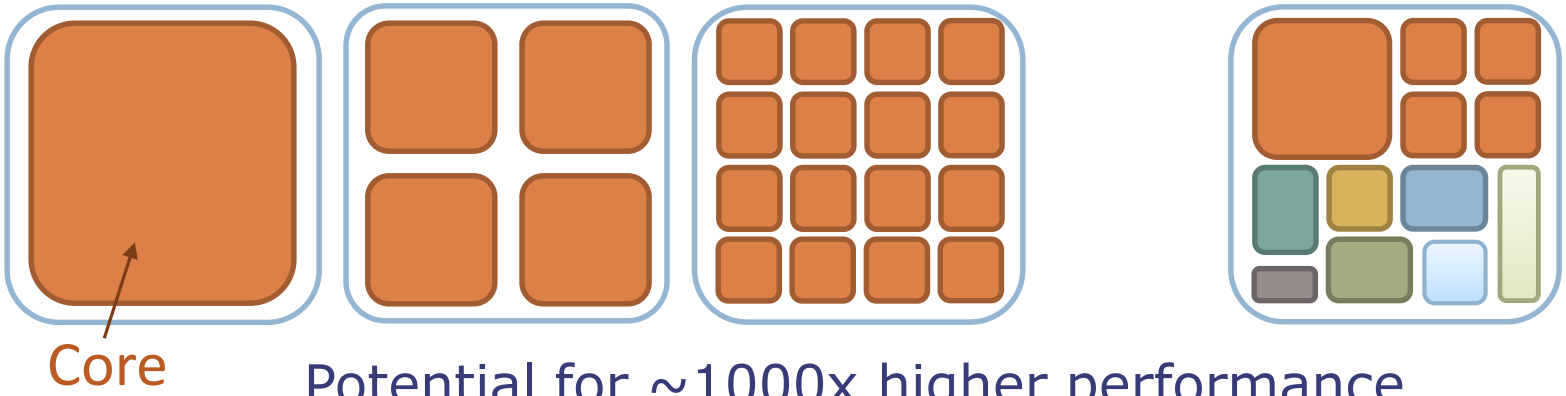

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You are likely to build or interact closely with specialized hardware in your career!

The Trend Towards Specialization

- Most of the area in modern processors is spent on specialized units, not general-purpose cores

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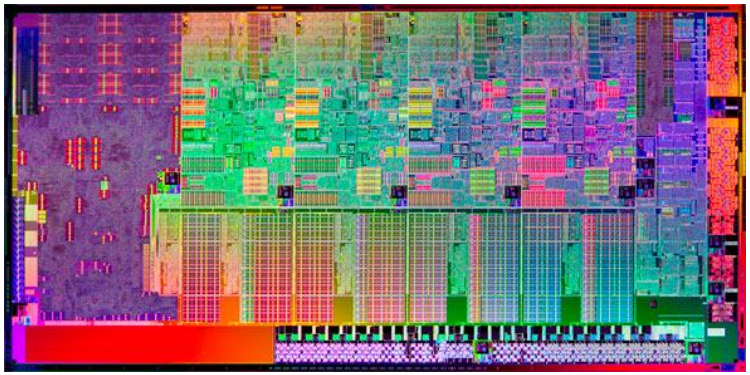

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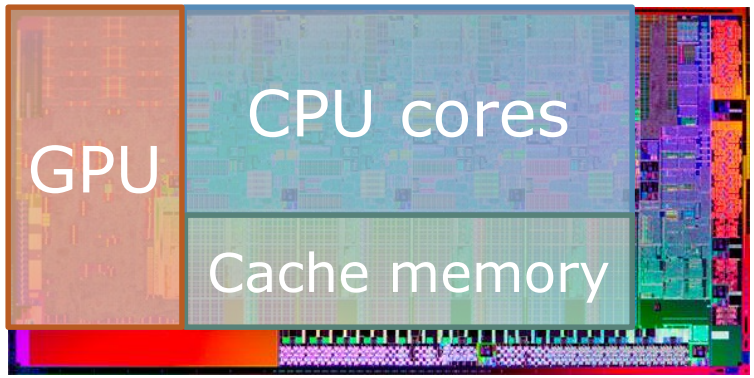

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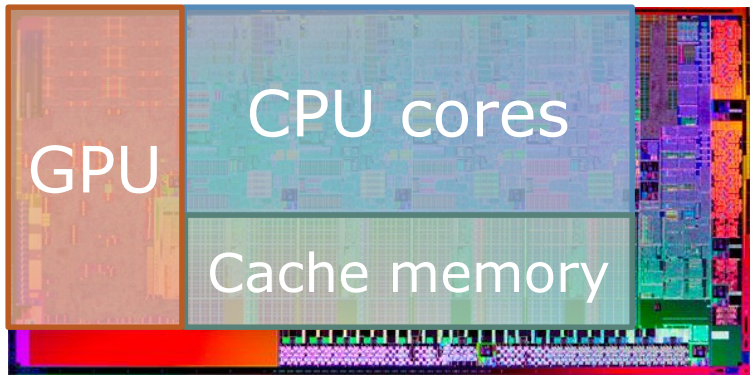

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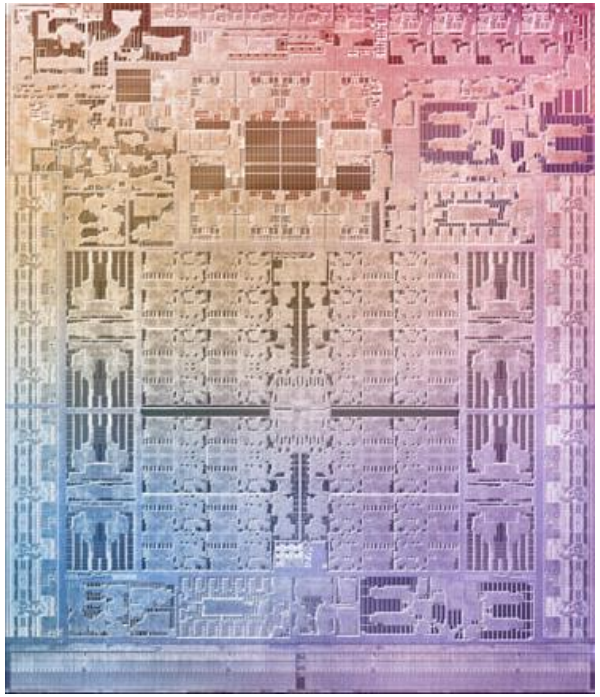

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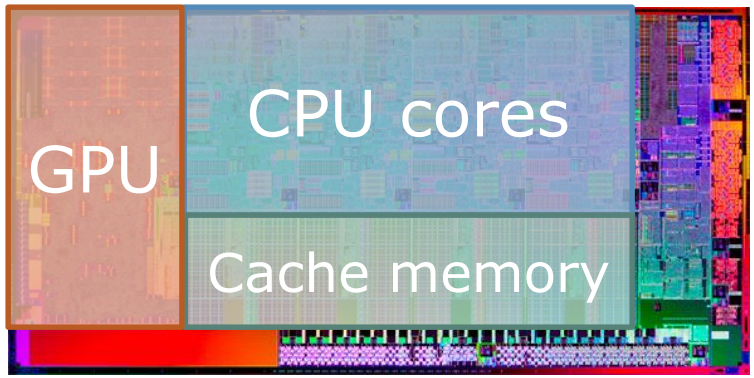

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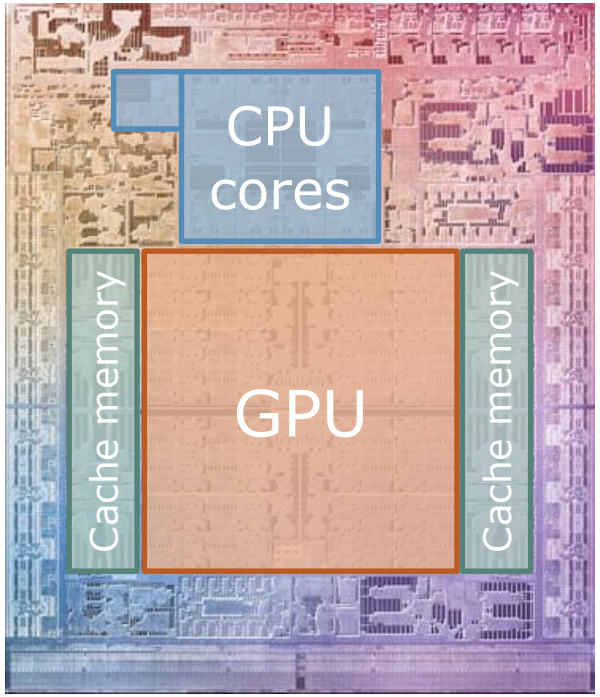

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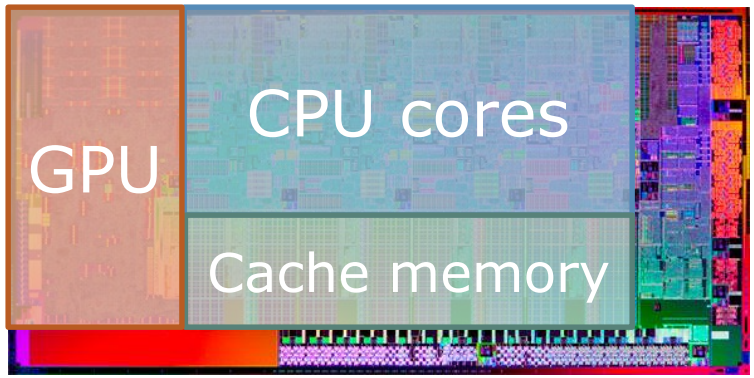

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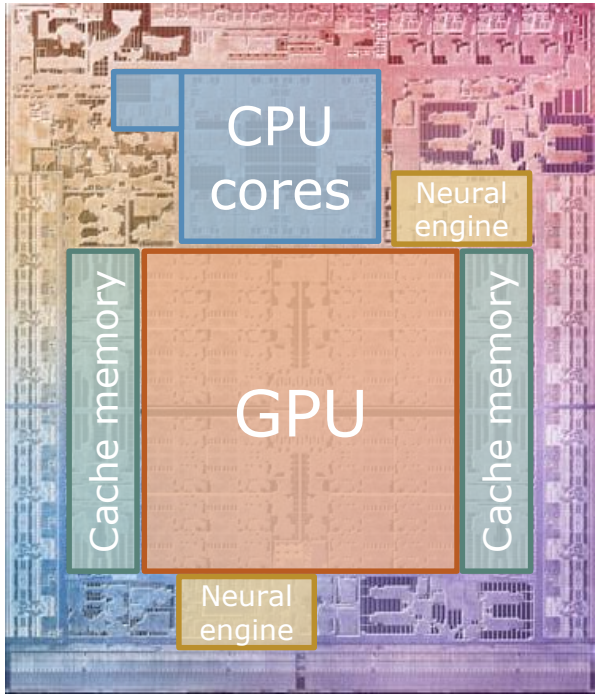

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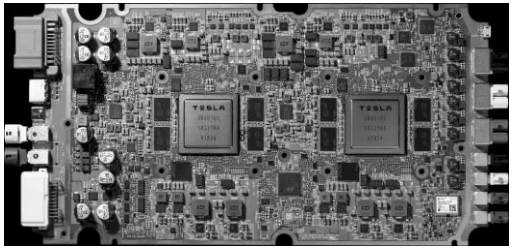

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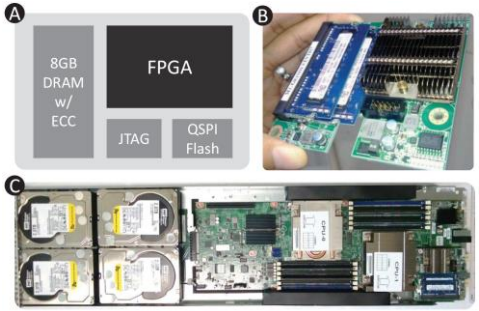

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[Catapult ISCA 2014]

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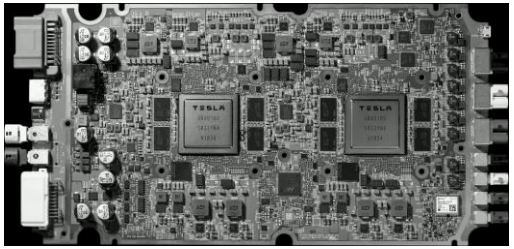

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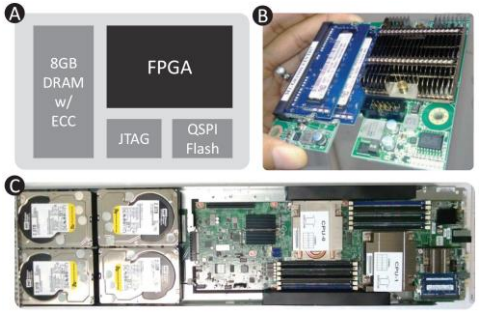

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- It is likely that you will build or closely interact with specialized hardware
  - Limited abstraction
  - Using these systems well requires understanding hardware design

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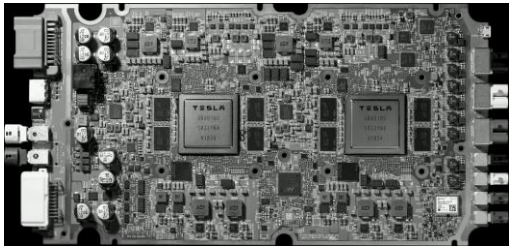

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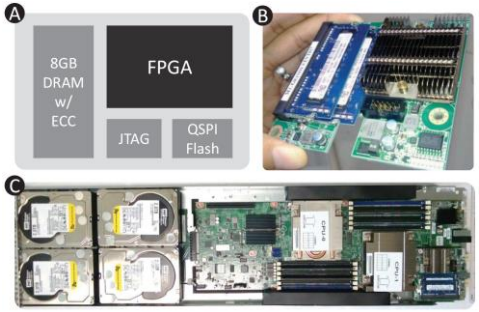

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Lecture Outline

- Examine design tradeoffs in digital logic: throughput, latency, and area
  - Power & energy are important, but out of scope for 6.004
  - Case study: Multiplier

- Study how to generalize an FSM to solve multiple problems
  - First step towards building a general-purpose processor!

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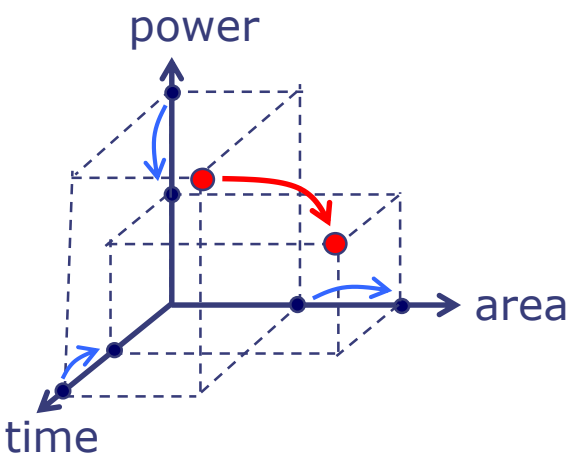

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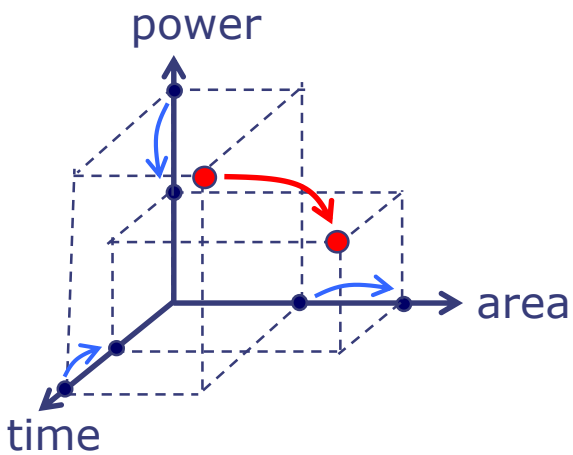

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Benefits of Sequential Logic

- Sequential circuits can implement more computations than combinational circuits
  - Variable amount of input and/or output
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- Even when combinational circuits suffice, sequential circuits allow more design tradeoffs
  - Pipelined circuits *improve throughput* by decreasing clock period and overlapping multiple computations
  - Multi-cycle / folded circuits *reduce area* by reusing a small amount of combinational logic over multiple cycles

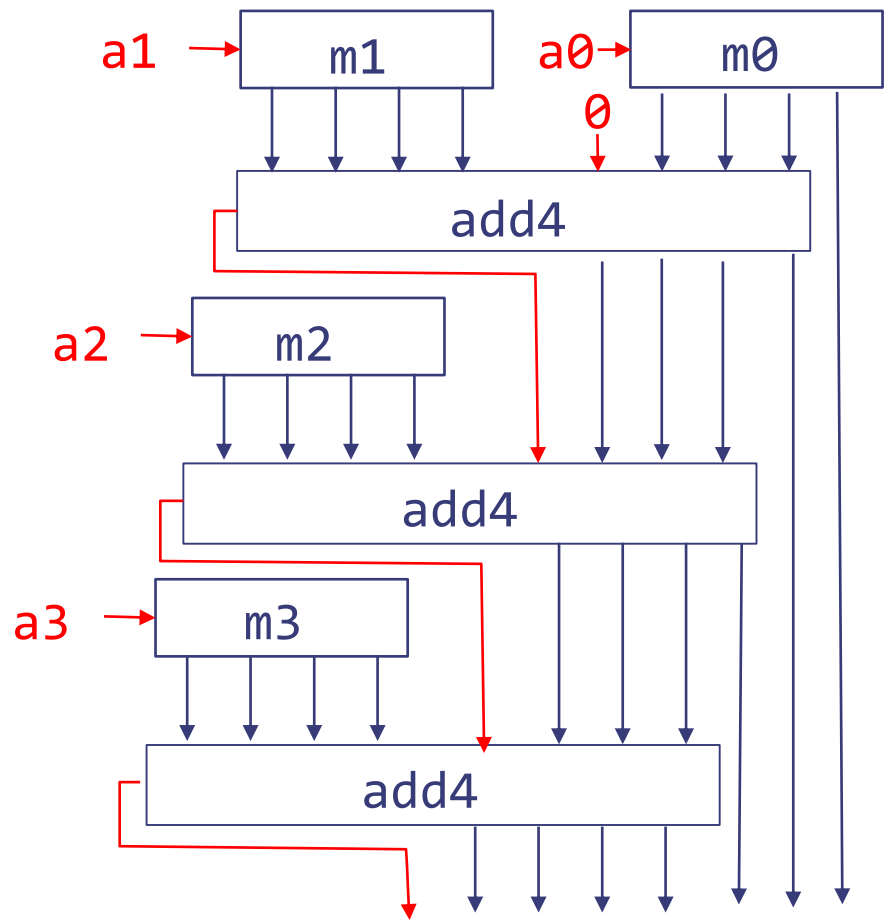
Reminder: Multiplication by repeated addition

```
b Multiplicand   1101   (13)
a Multiplier   * 1011   (11)

tp                0000
m0          +     1101
            ------------
tp               01101
m1          +    1101
            ------------
tp              100111
m2          +   0000
            ------------
tp             0100111
m3          + 1101
            ------------
tp            10001111   (143)
```

```
mi = (a[i]==0)? 0 : b;
```

Implementation: Cascade of N-1 N-bit adders



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The "Binary" Multiplication Table

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\begin{array}{rrrrrrr}
 & & & & B_3 & B_2 & B_1 & B_0 \\
 & & & & \times\ A_3 & A_2 & A_1 & A_0 \\
\hline
 & & & & B_3A_0 & B_2A_0 & B_1A_0 & B_0A_0 & \text{m0} \\
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BA_i called a "partial product" → B_3A_0 B_2A_0 B_1A_0 B_0A_0

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Multiplying N-digit number by M-digit number gives (N+M)-digit result

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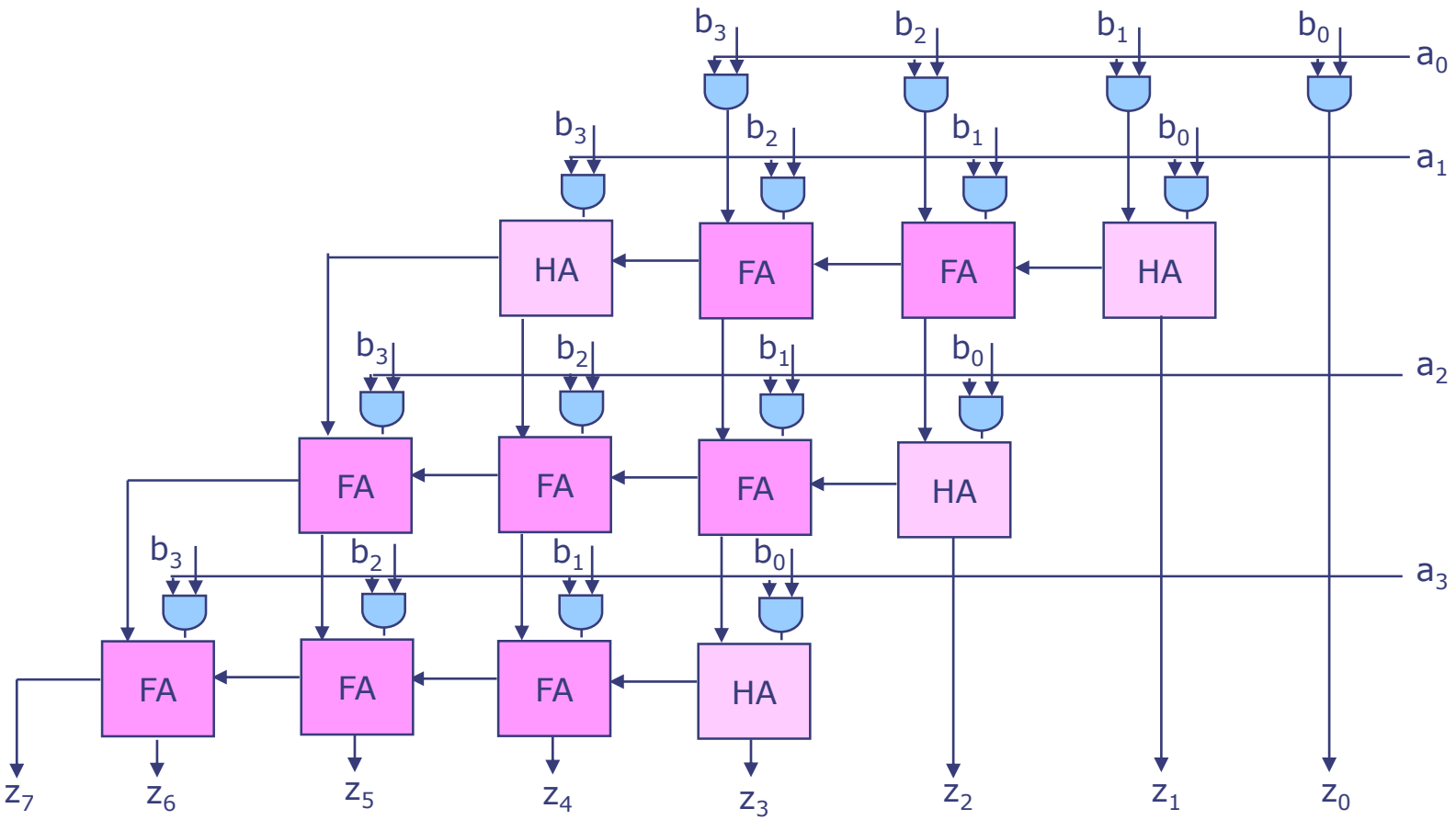
Easy part: forming partial products (bunch of AND gates)
Hard part: adding M N-bit partial products

Combinational Multiplier Redrawn

Using ripple-carry adders



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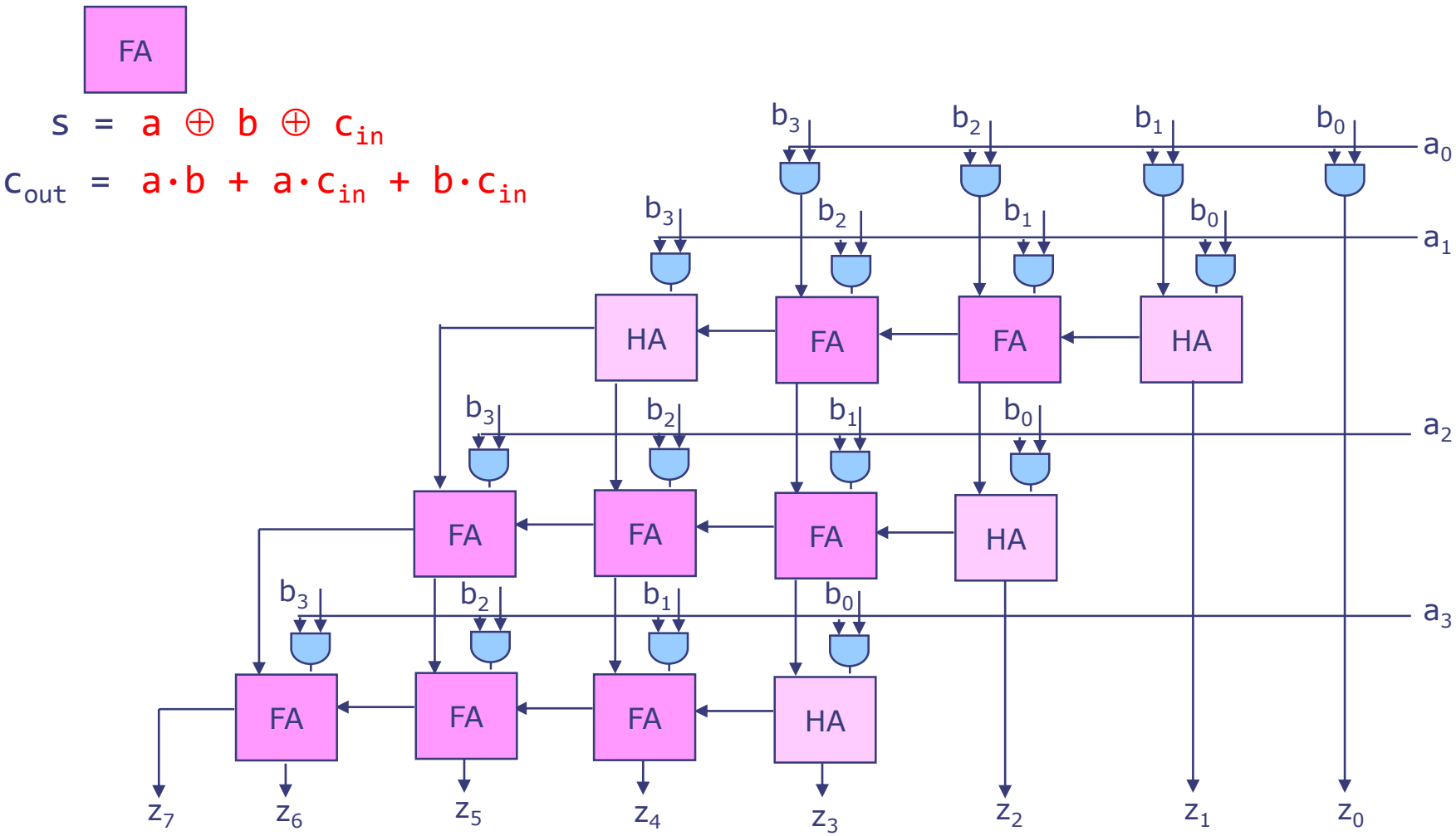

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Using ripple-carry adders

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$s = a \oplus b \oplus c_{in}$

$c_{out} = a \cdot b + a \cdot c_{in} + b \cdot c_{in}$

HA

$s = a \oplus b$

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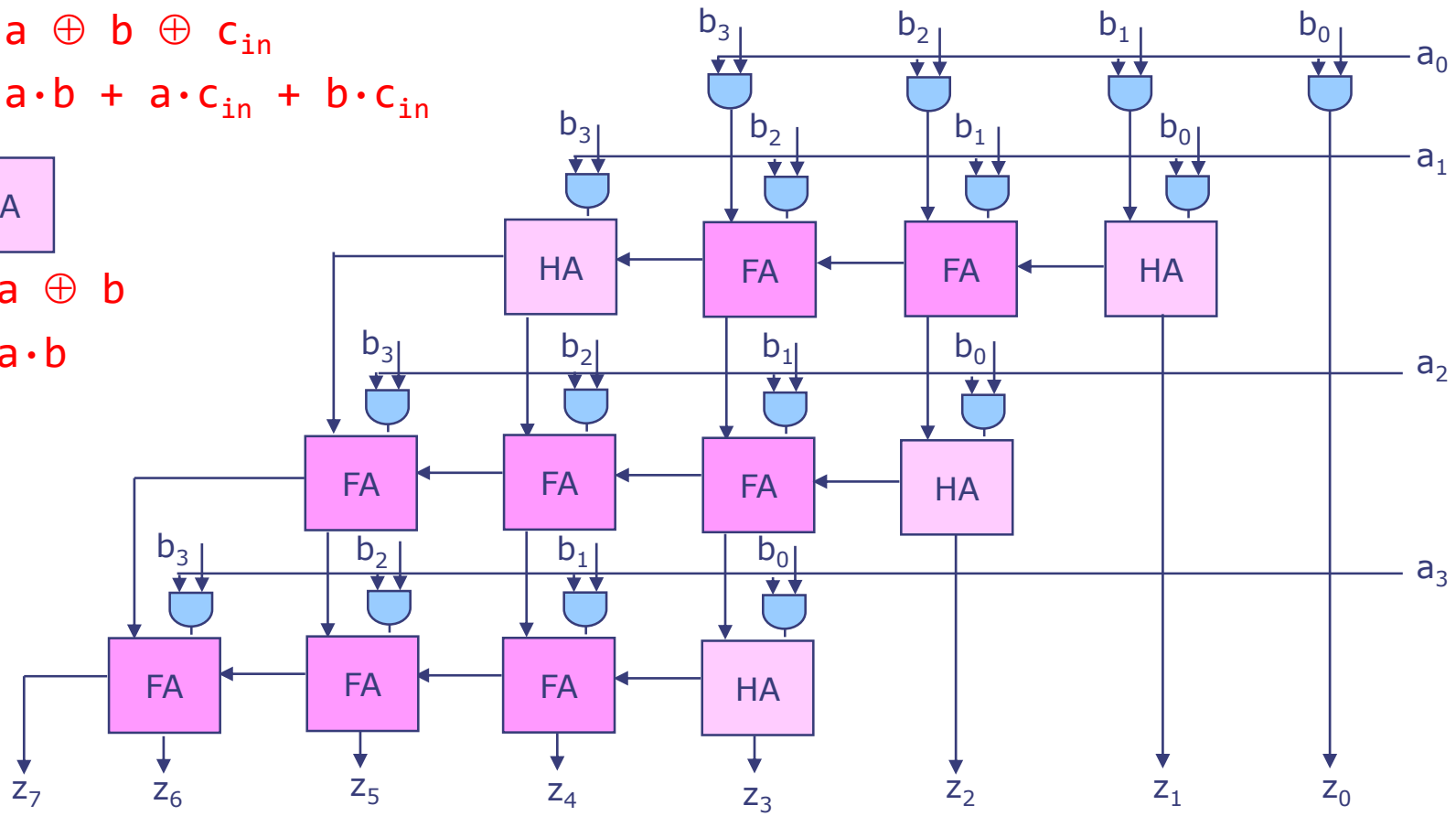

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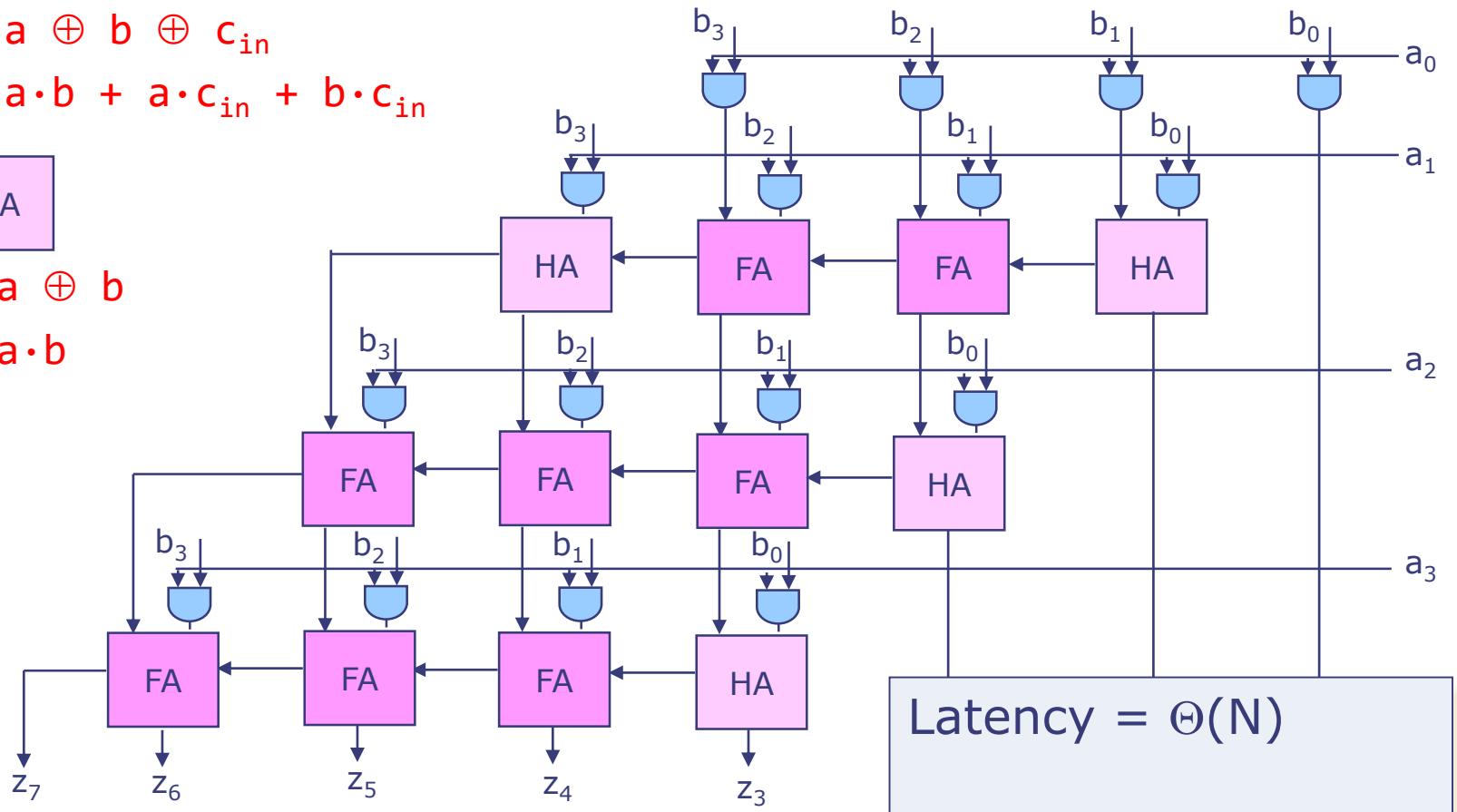

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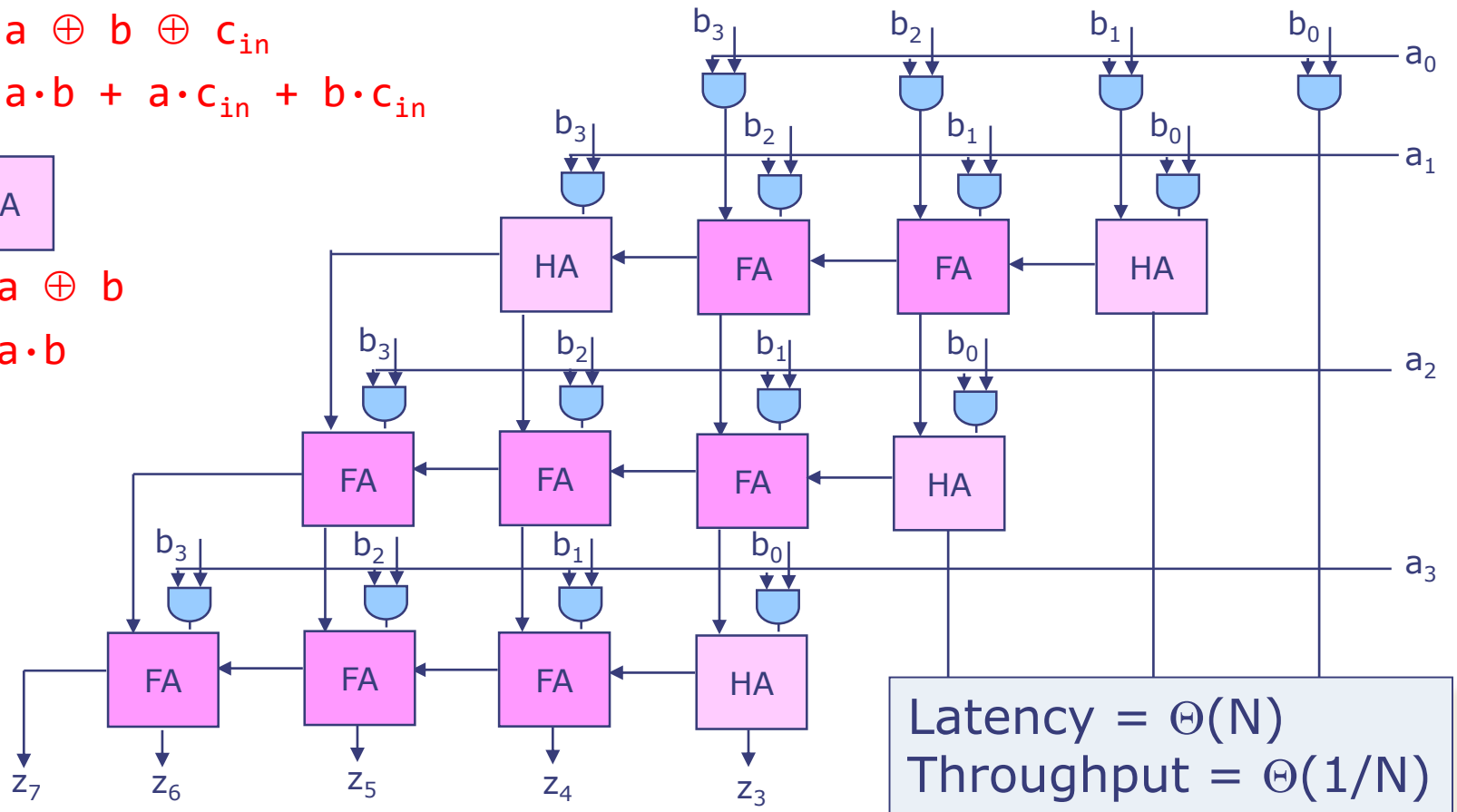

Latency = $\Theta(N)$
Throughput = $\Theta(1/N)$

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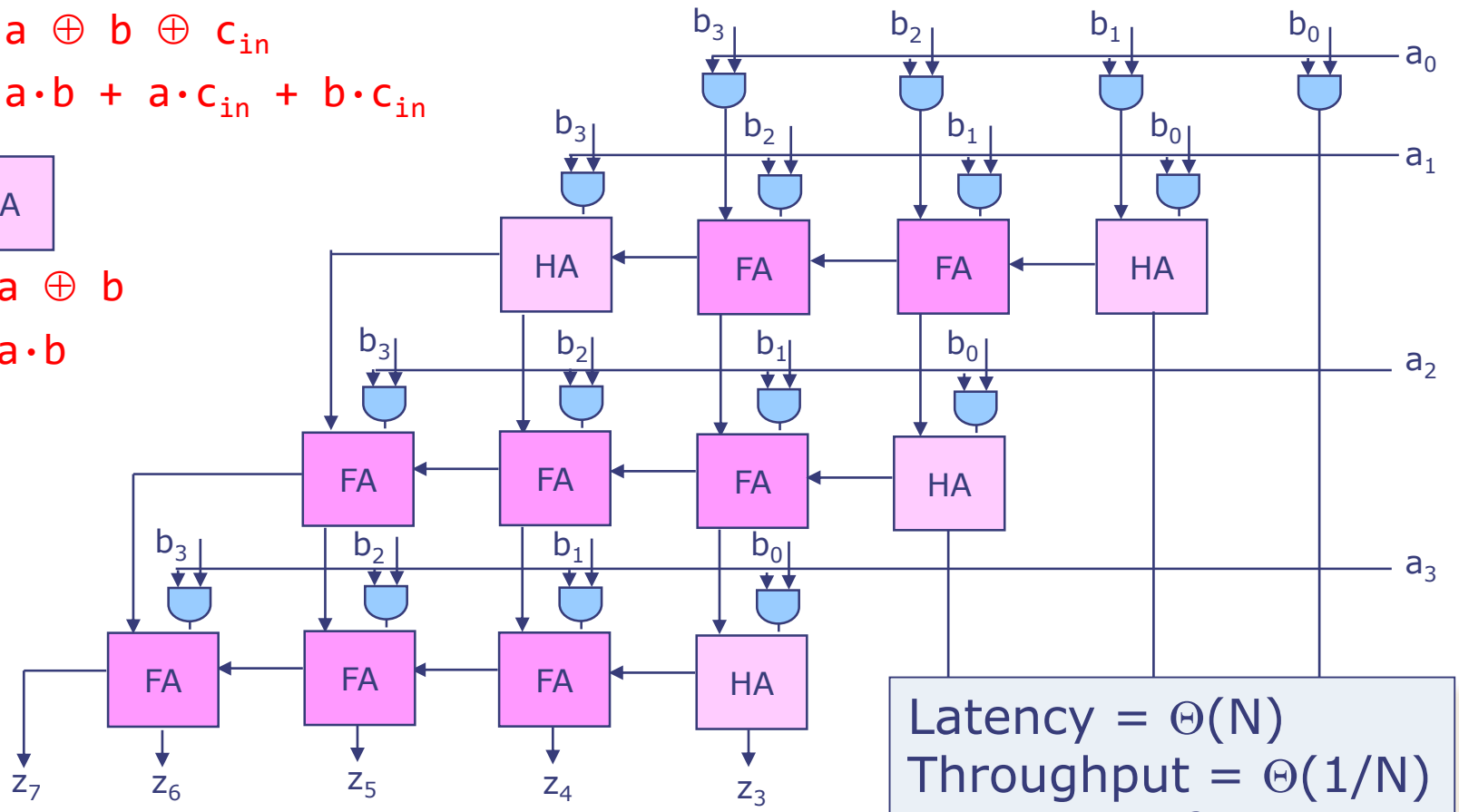
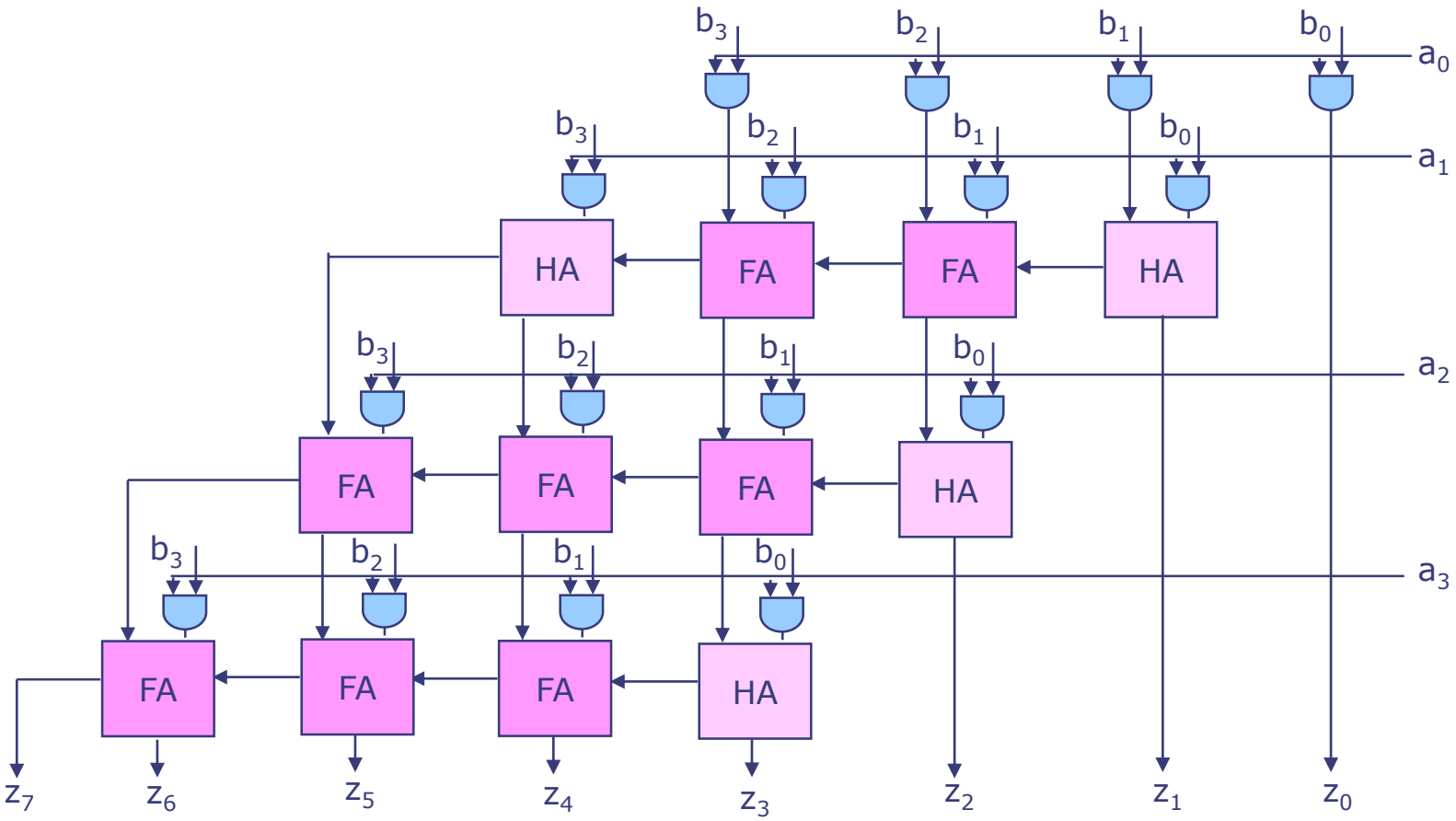


Latency = $\Theta(N)$
Throughput = $\Theta(1/N)$
Area = $\Theta(N^2)$

Pipelining to Increase Throughput
First Attempt



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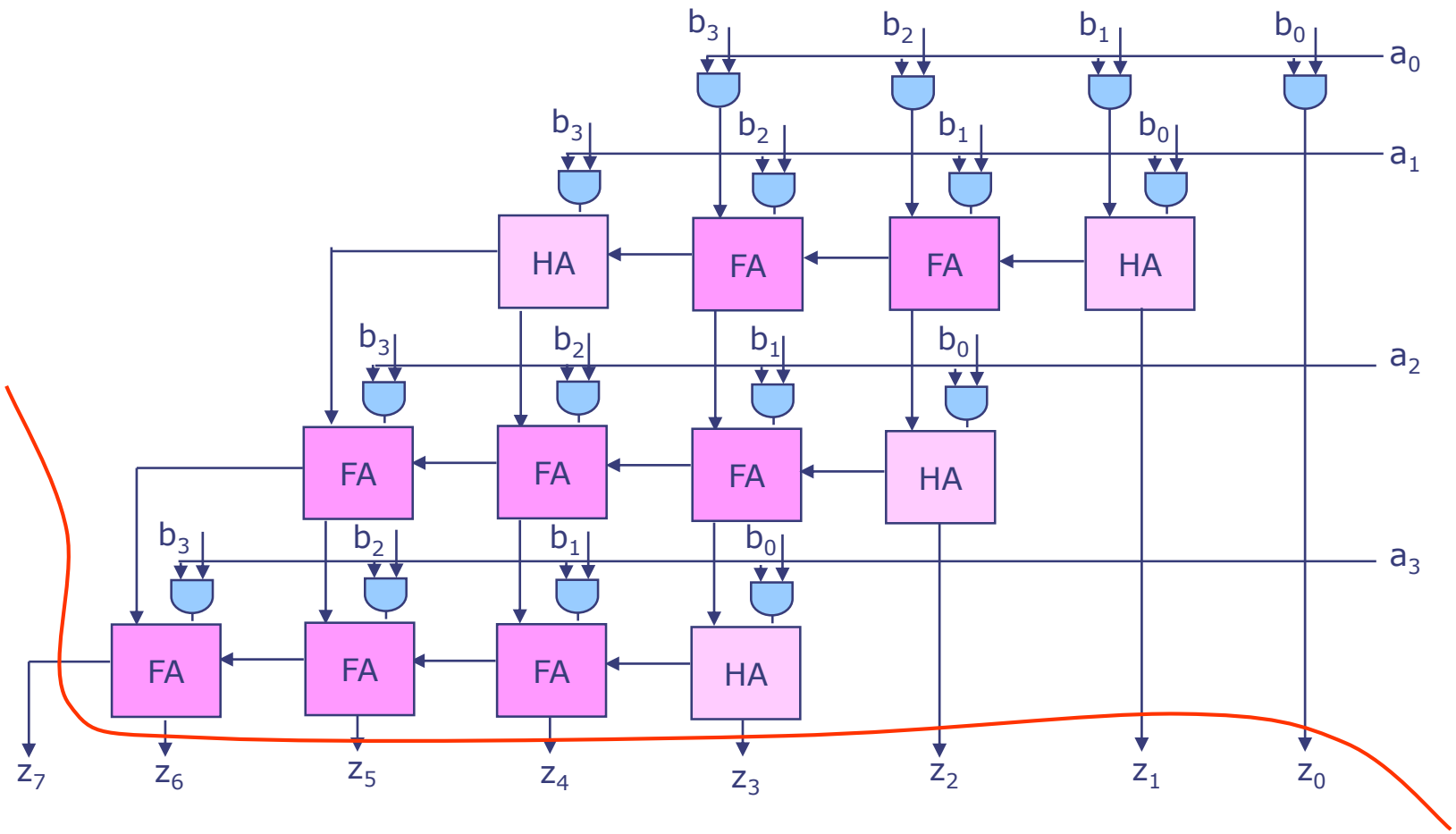

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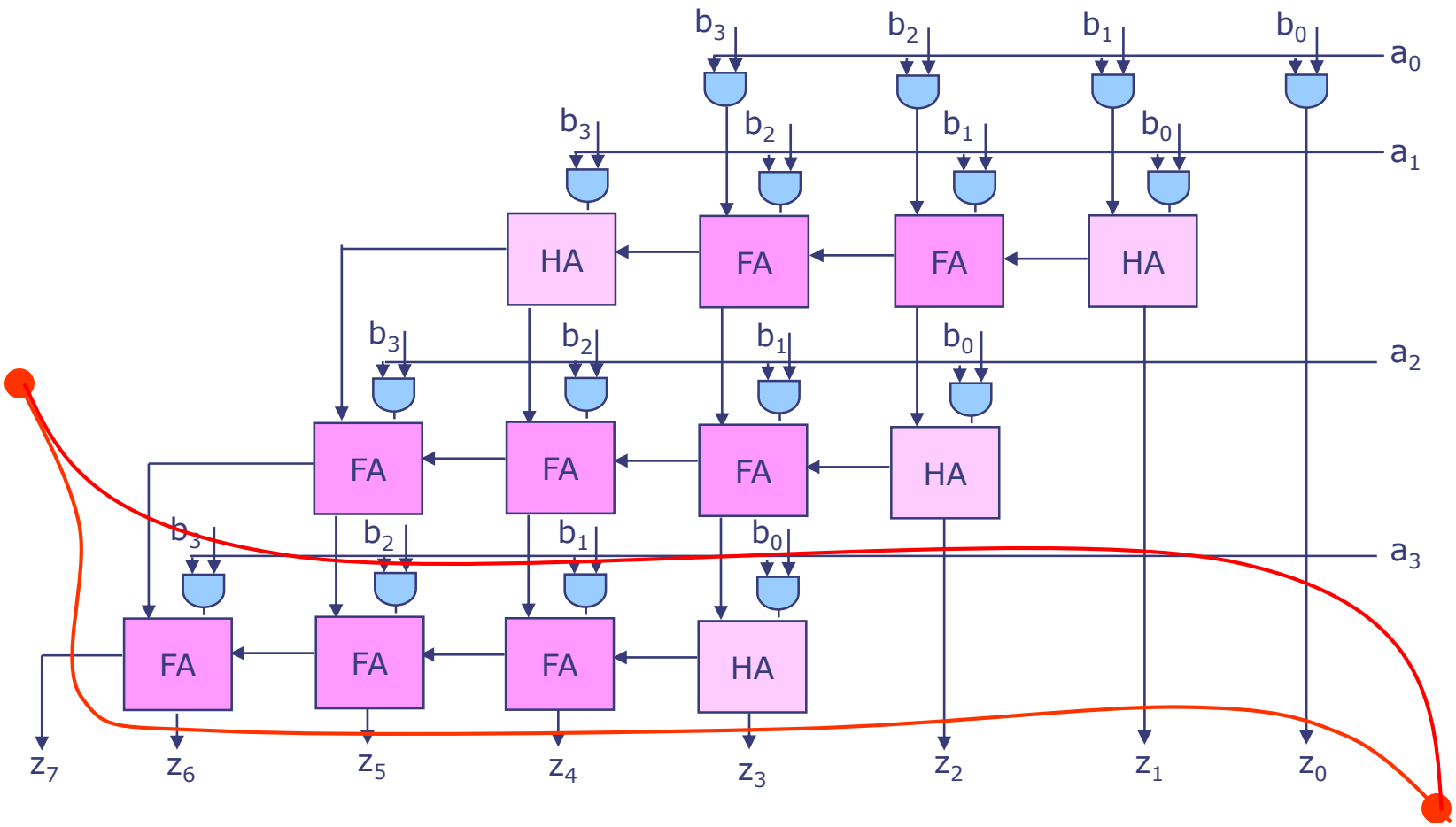

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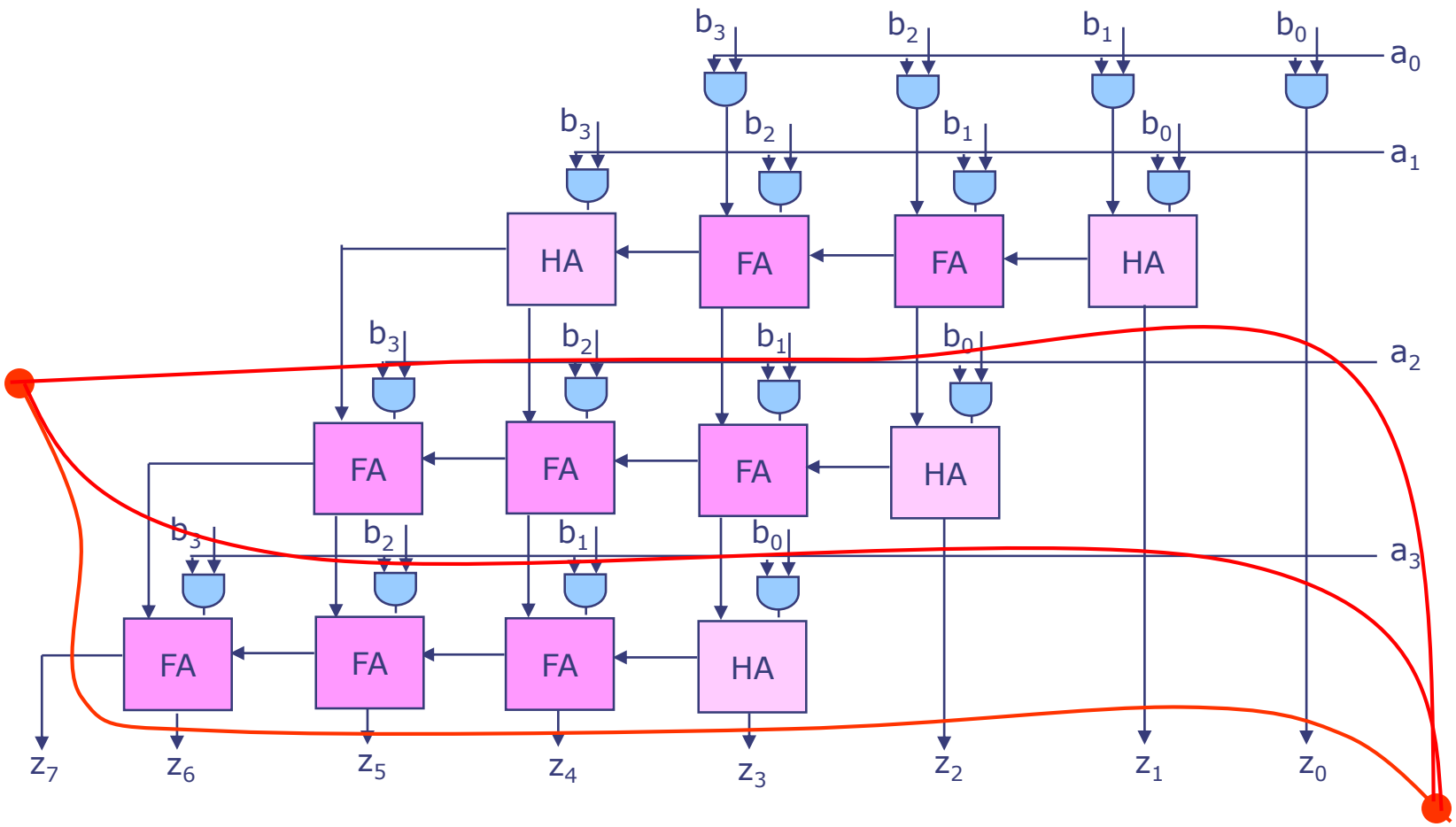

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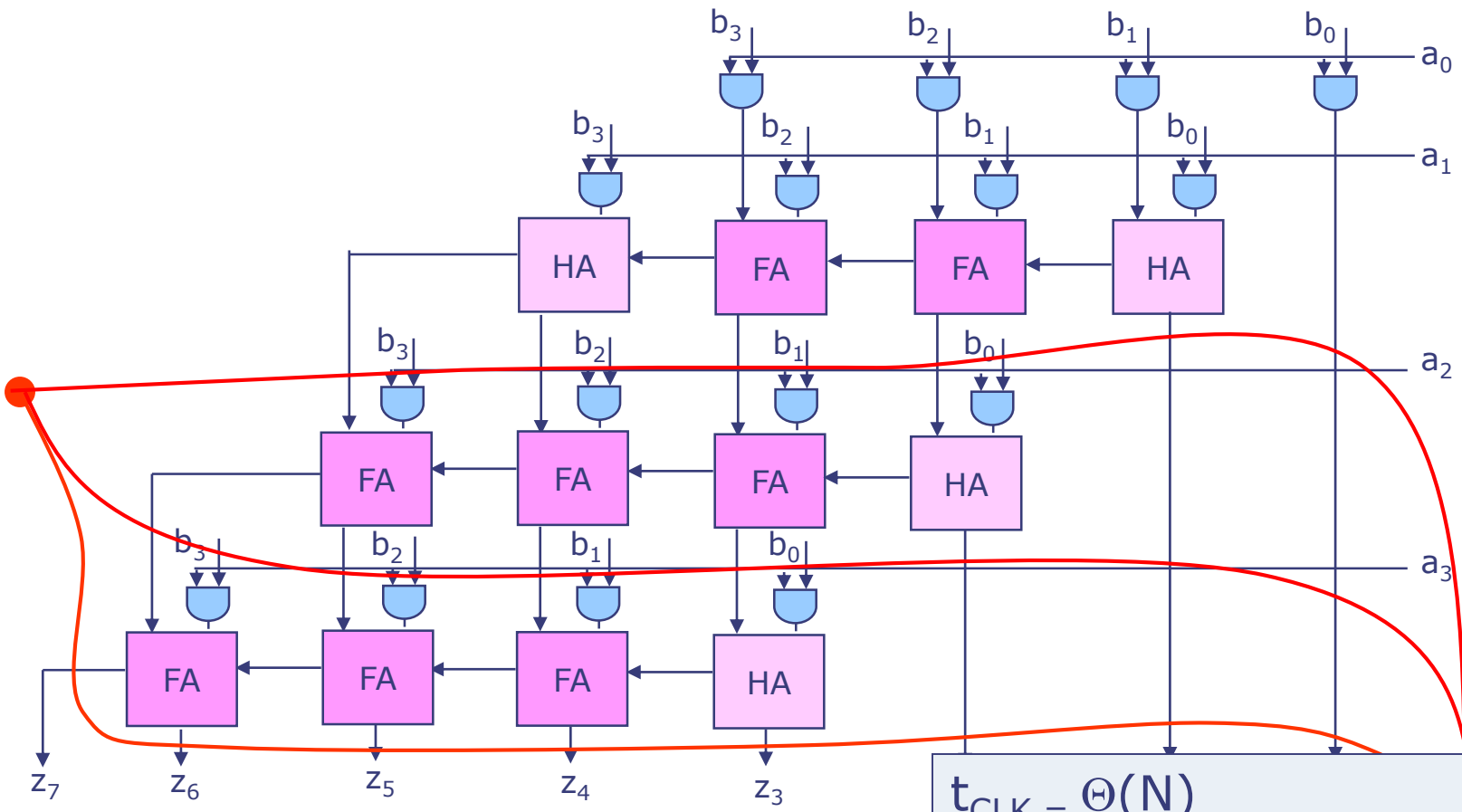

$t_{CLK} = \Theta(N)$

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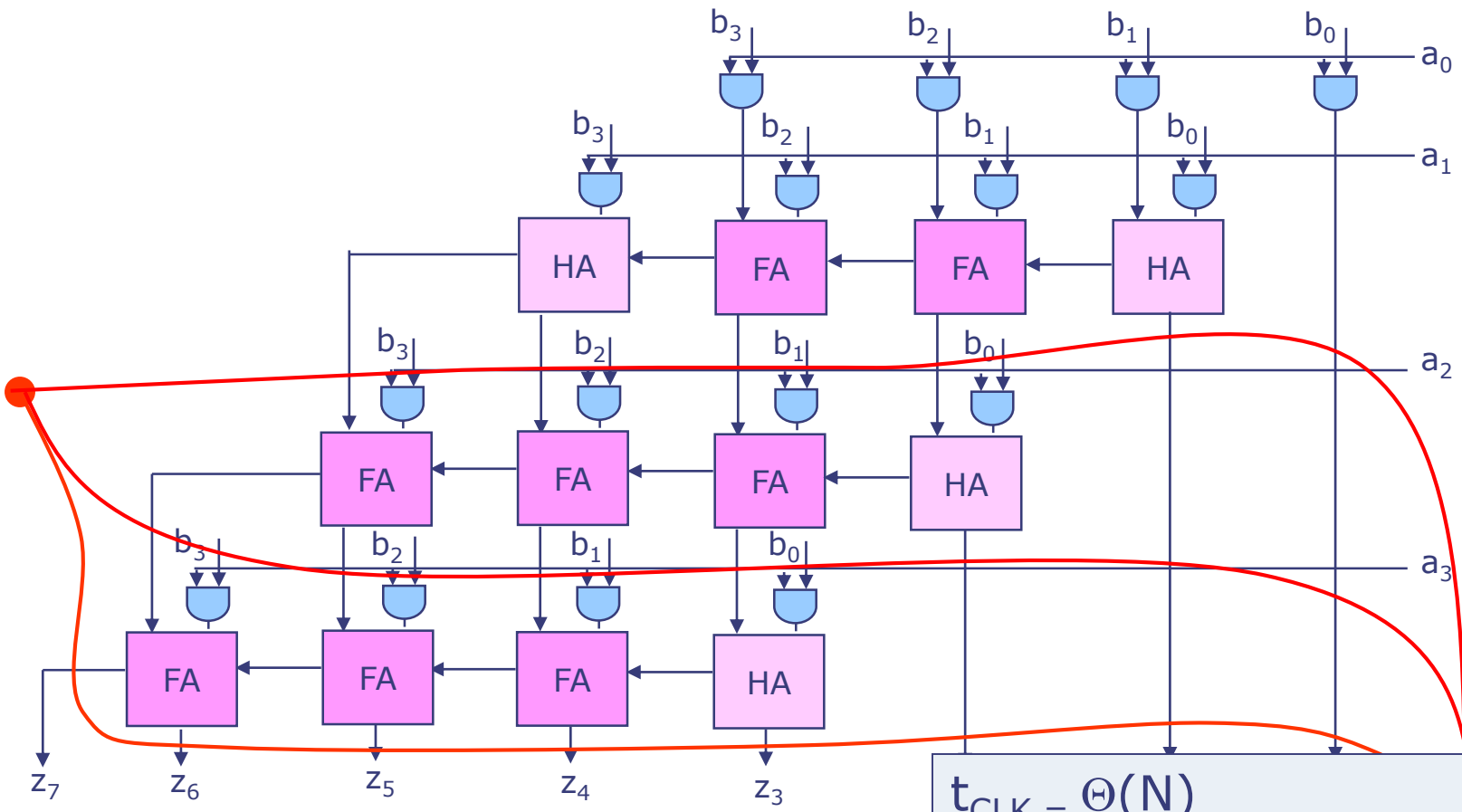

$t_{CLK} = \Theta(N)$
stages = $\Theta(N)$

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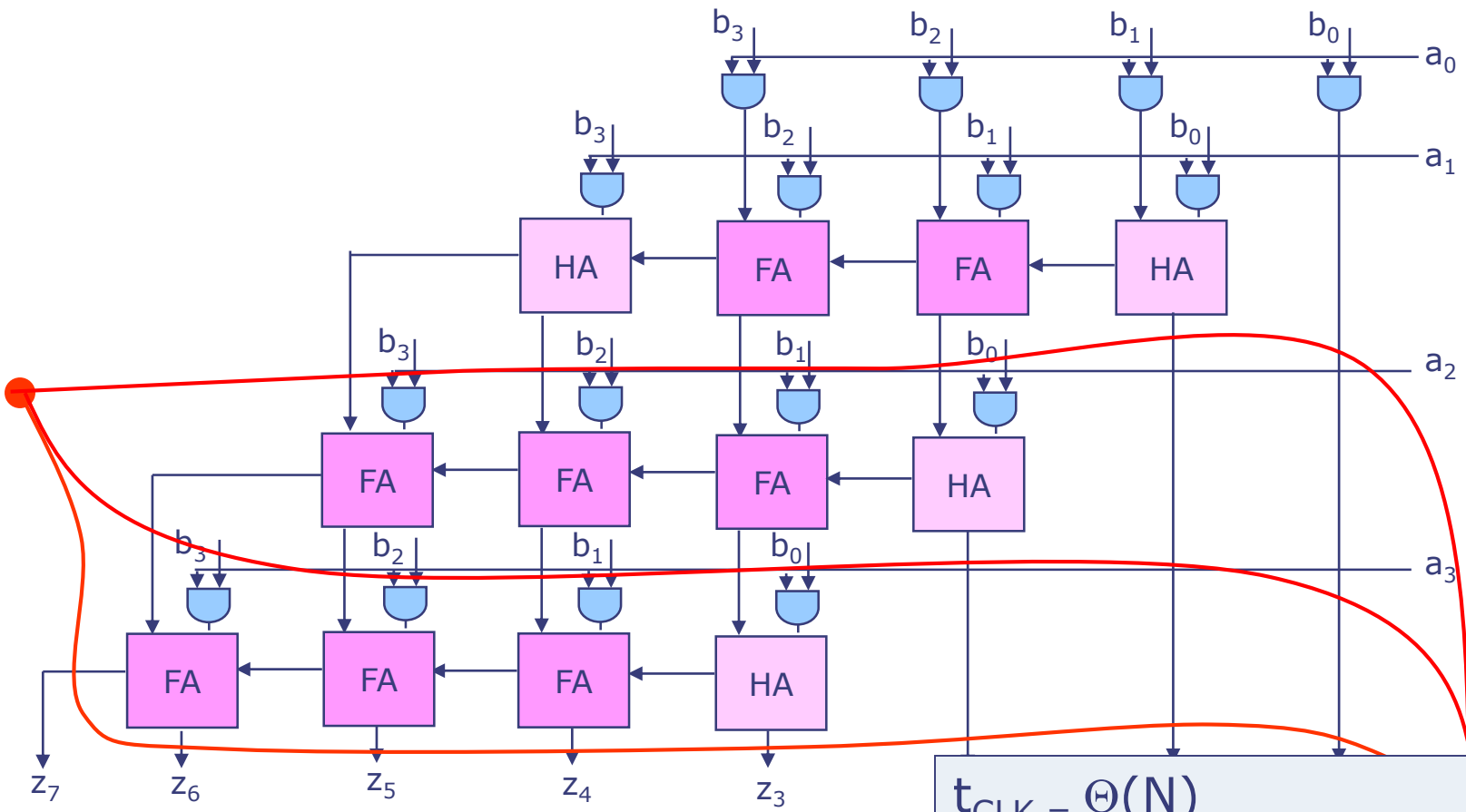
First Attempt



$t_{CLK} = \Theta(N)$
# stages = $\Theta(N)$
Latency = $\Theta(N^2)$

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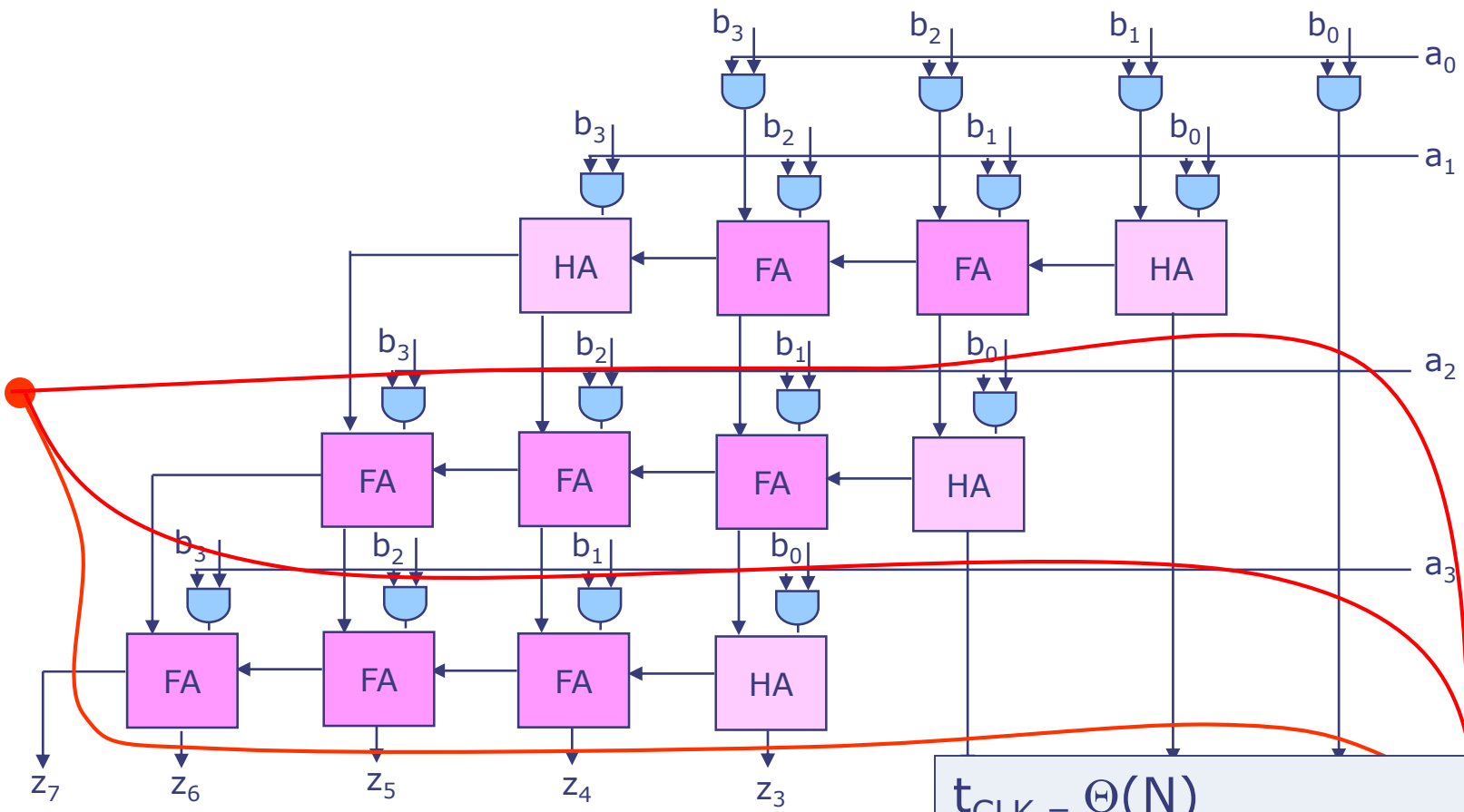

$t_{CLK} = \Theta(N)$
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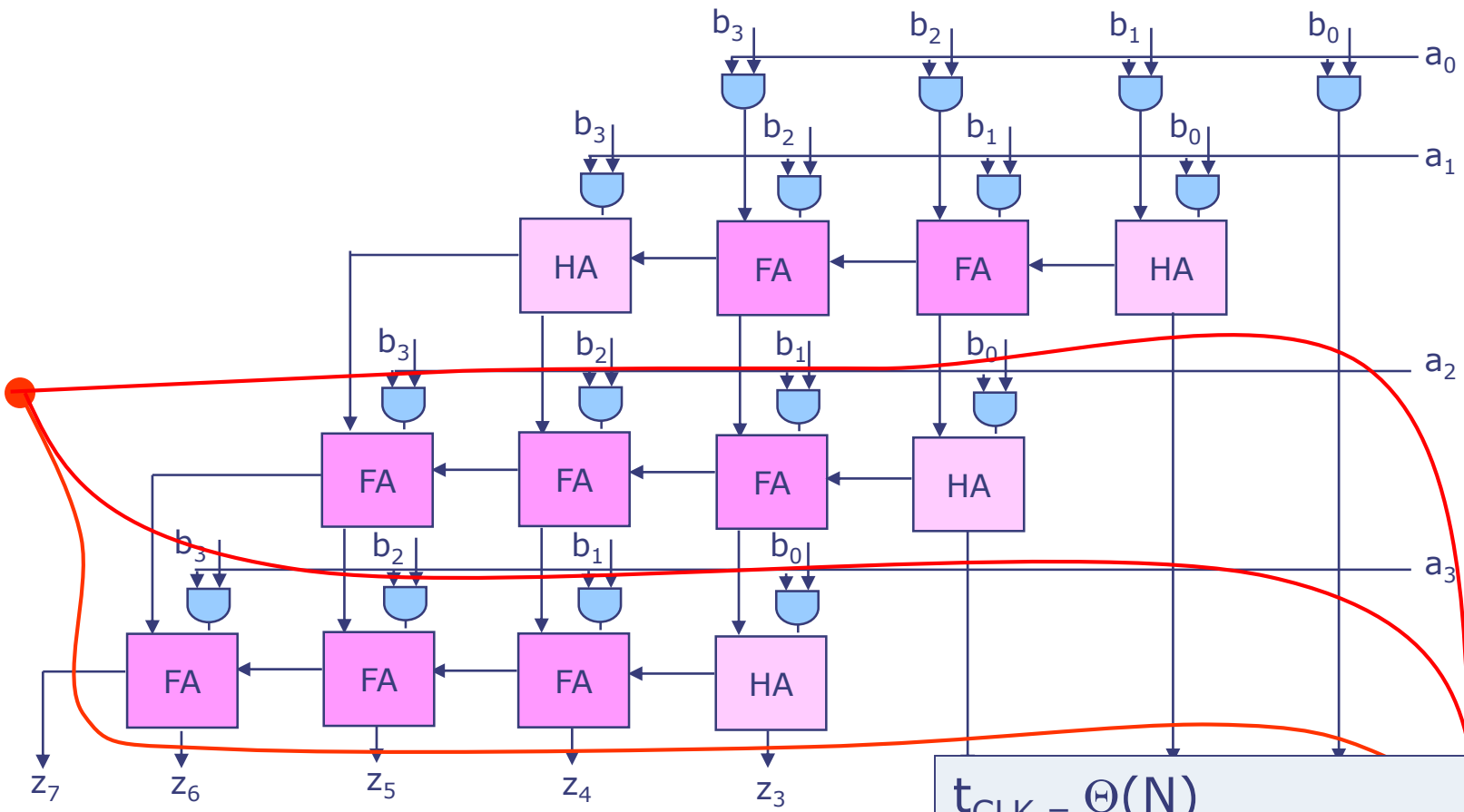

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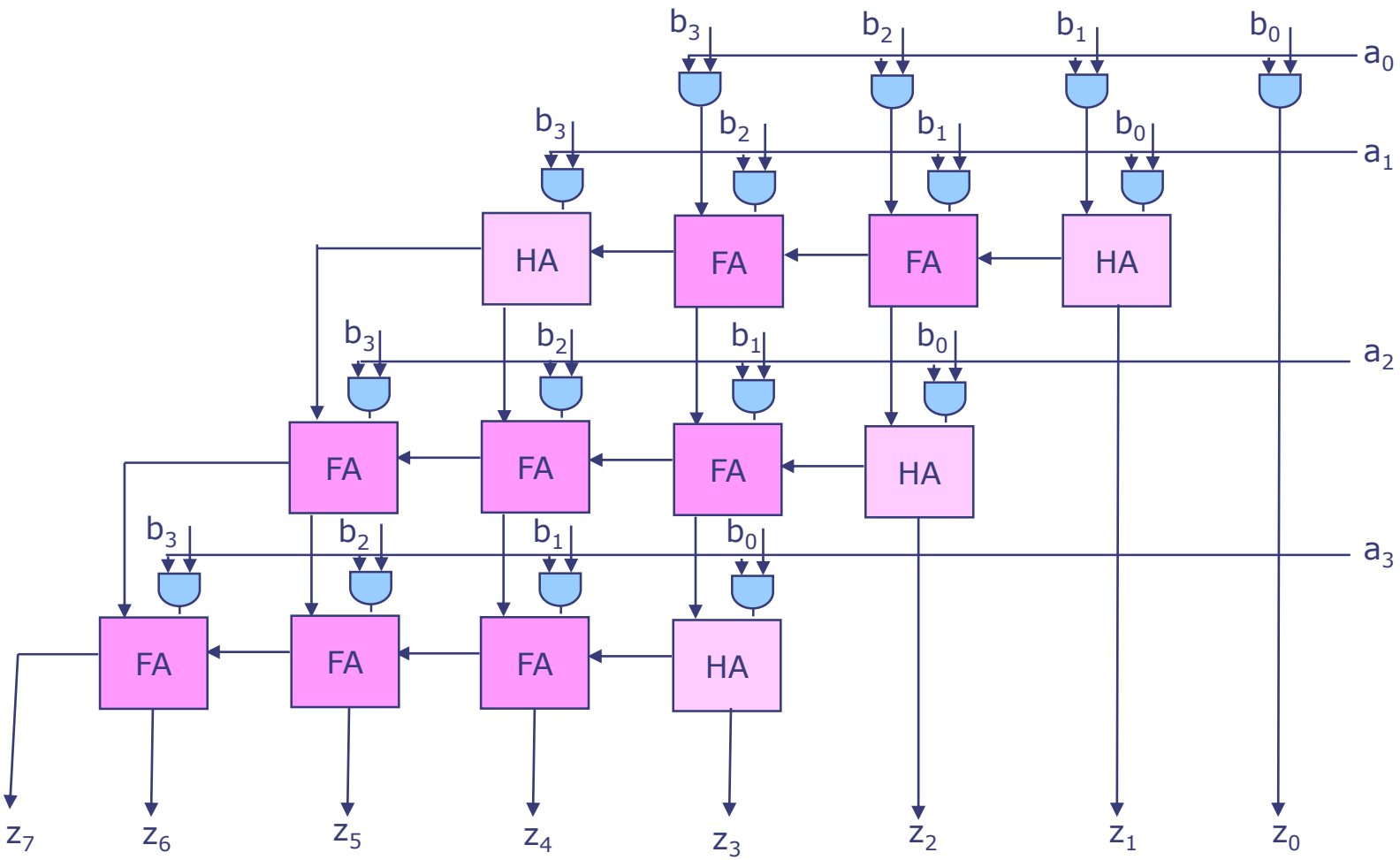
Need to break carry chain

Pipelining to Increase Throughput



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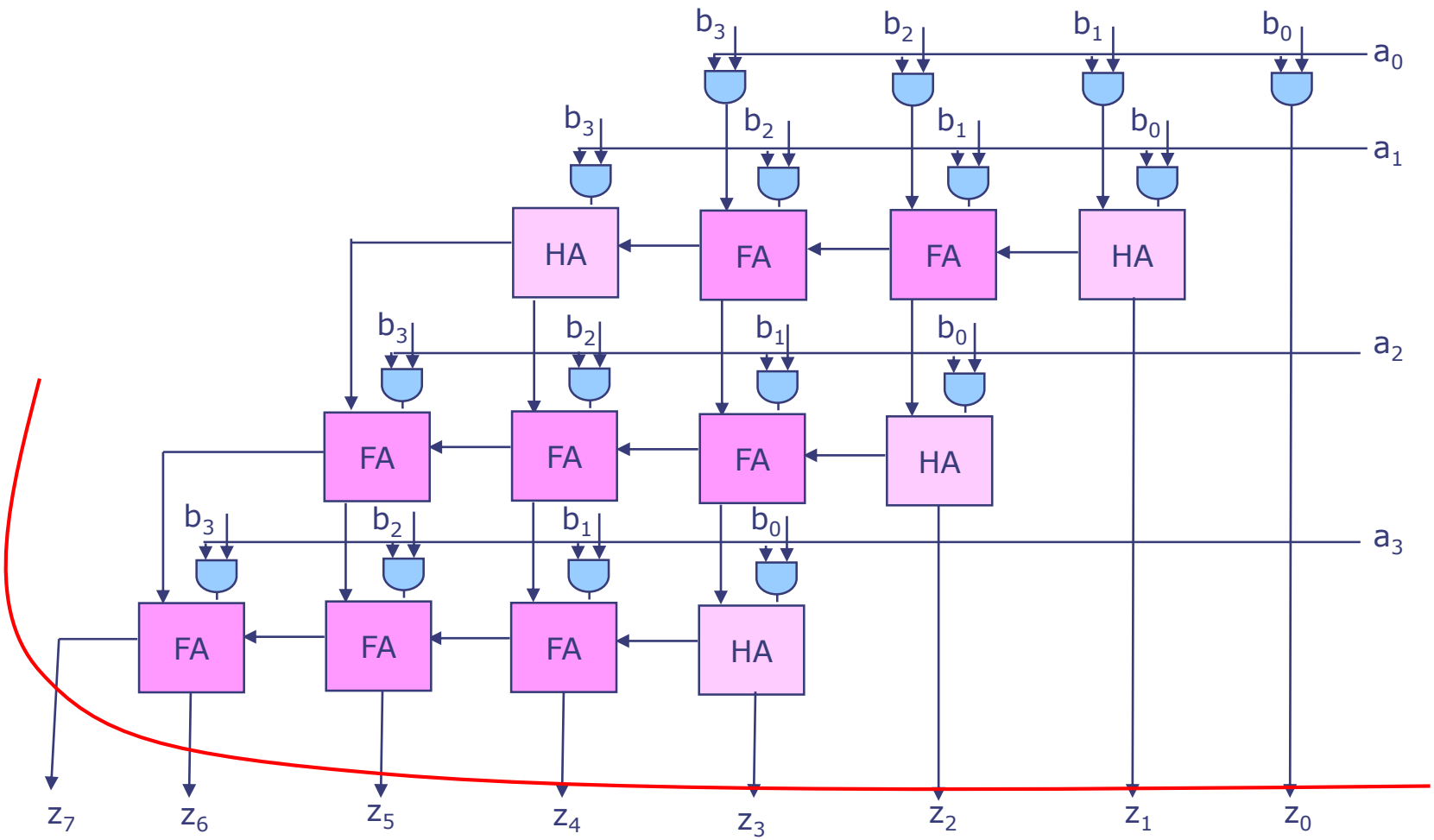

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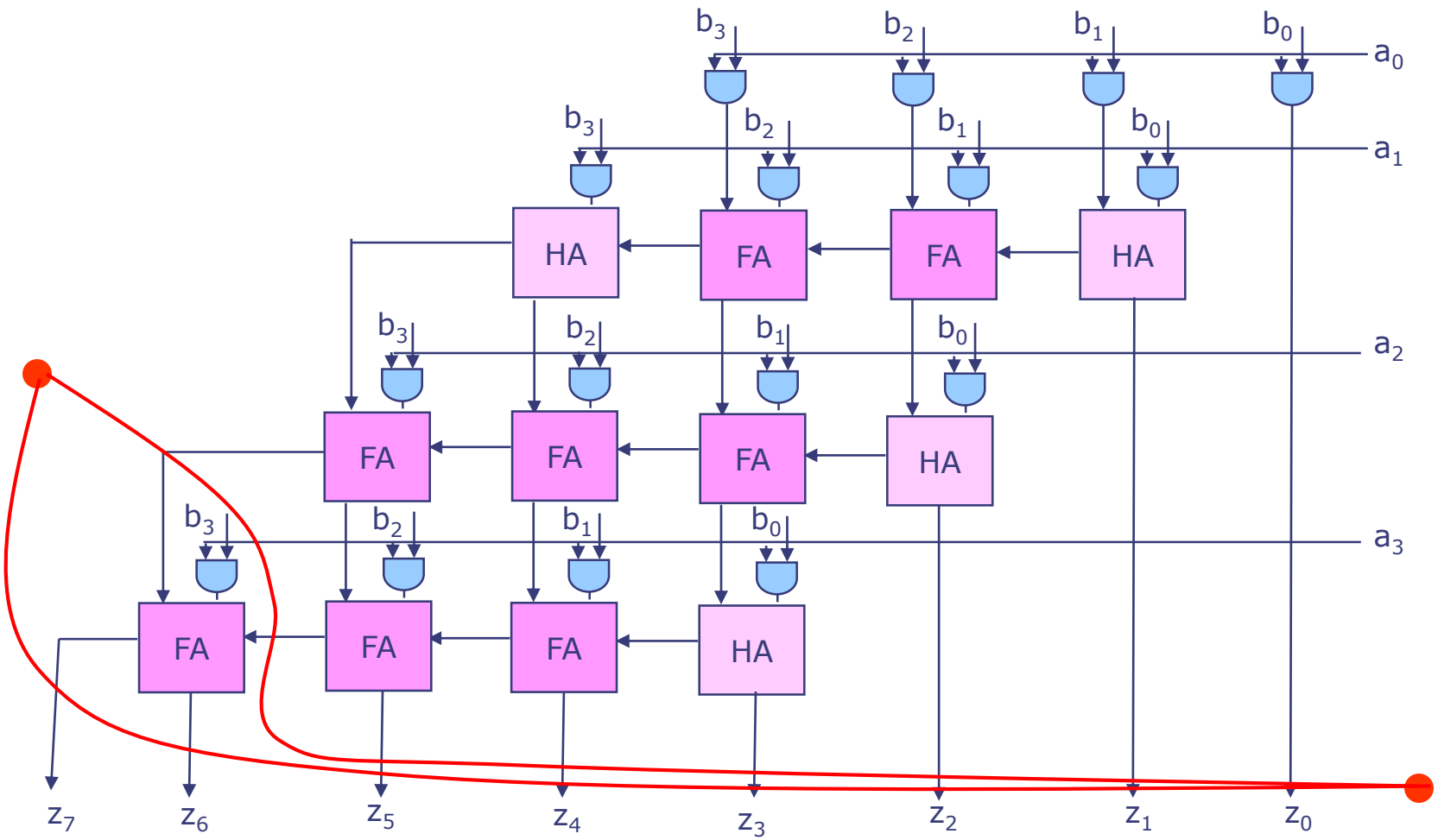

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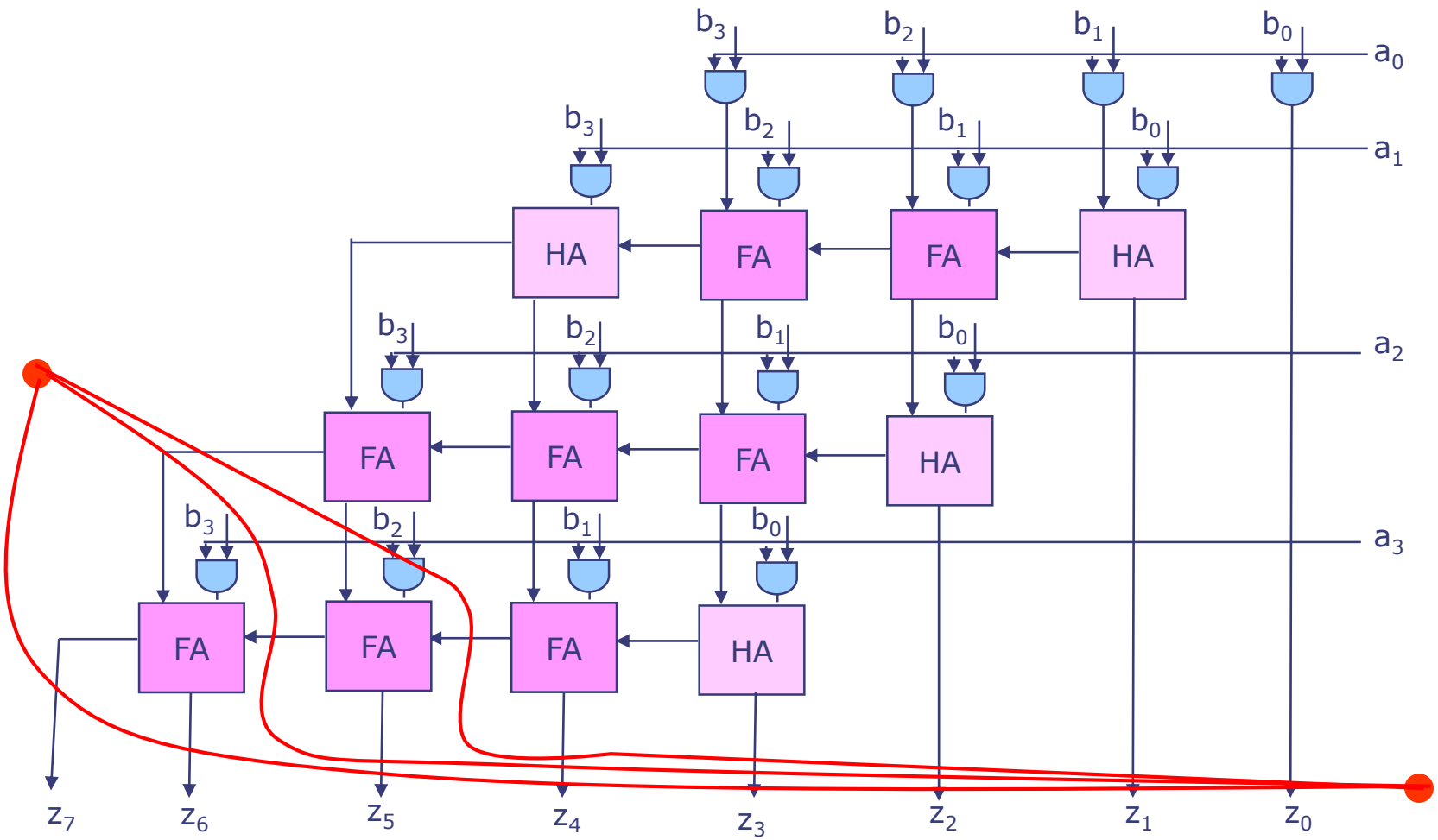

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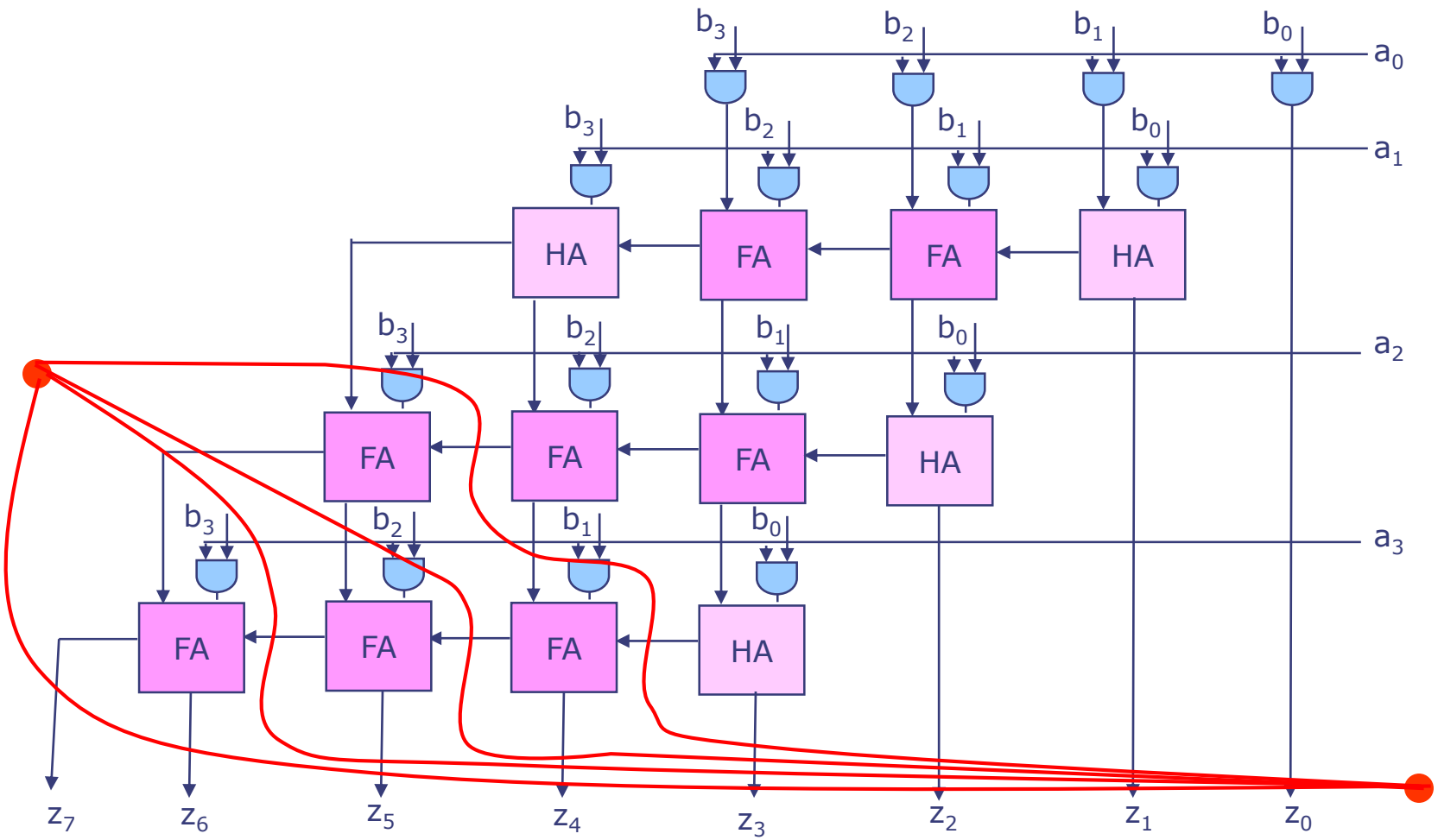

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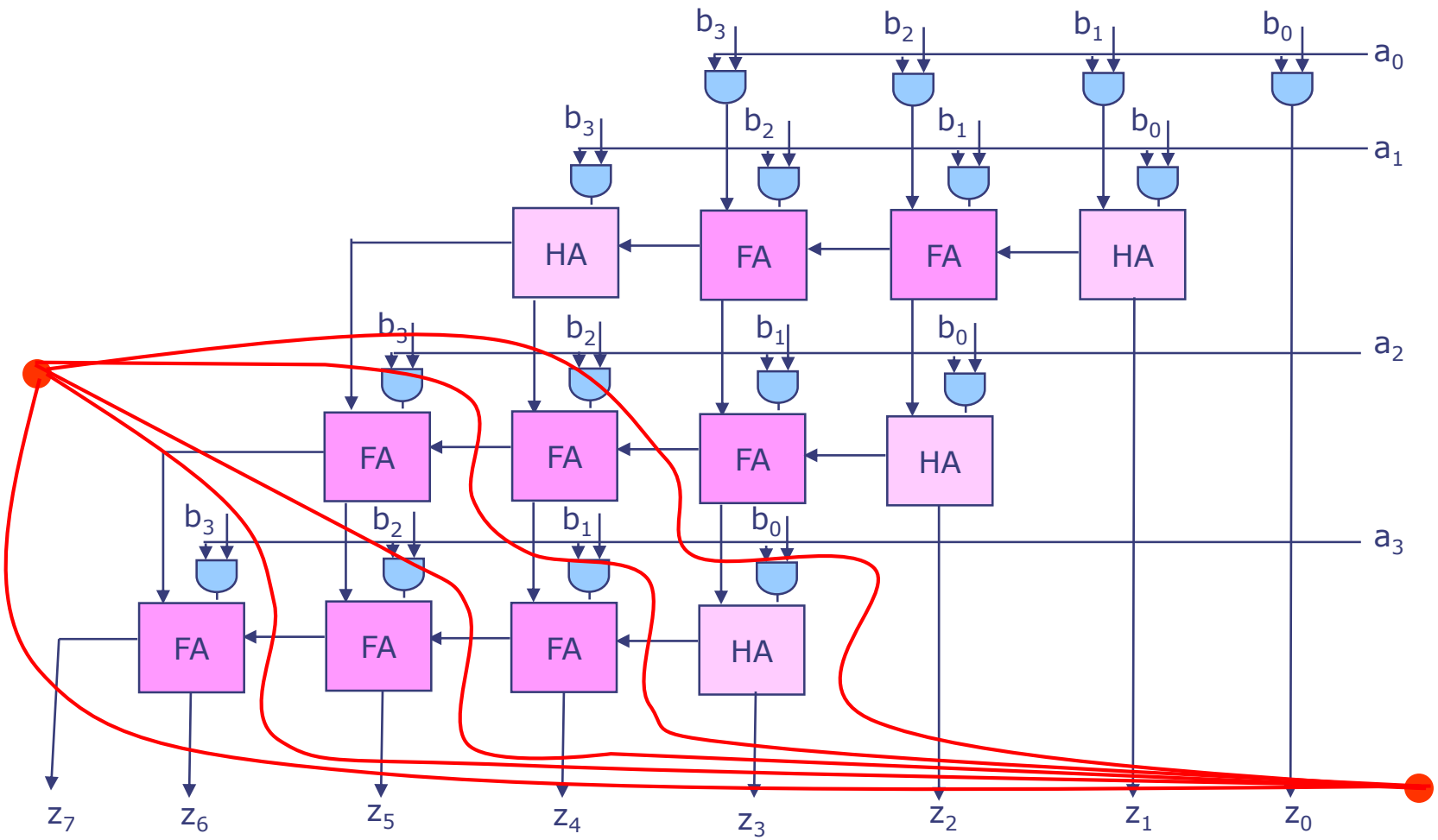

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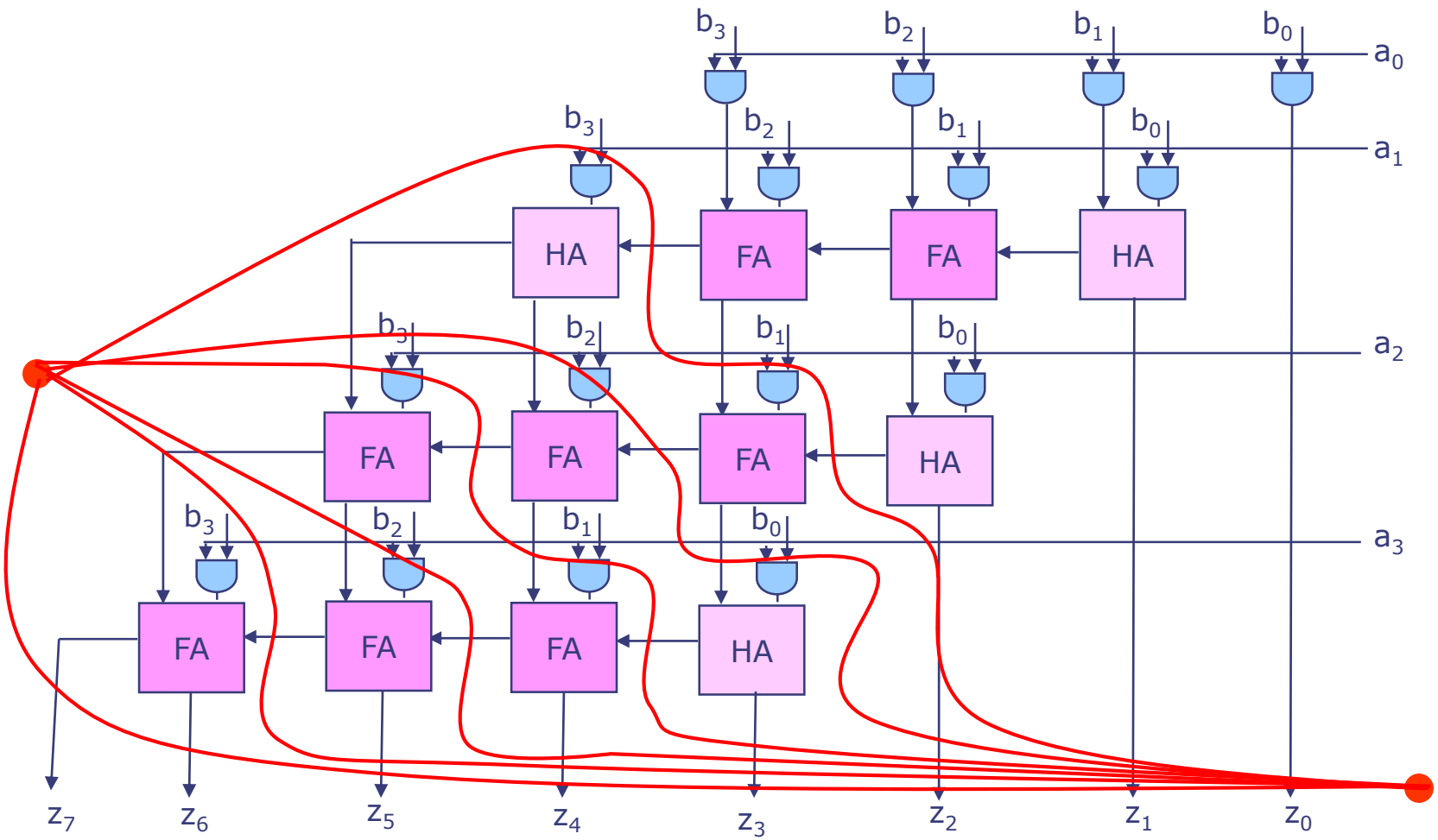

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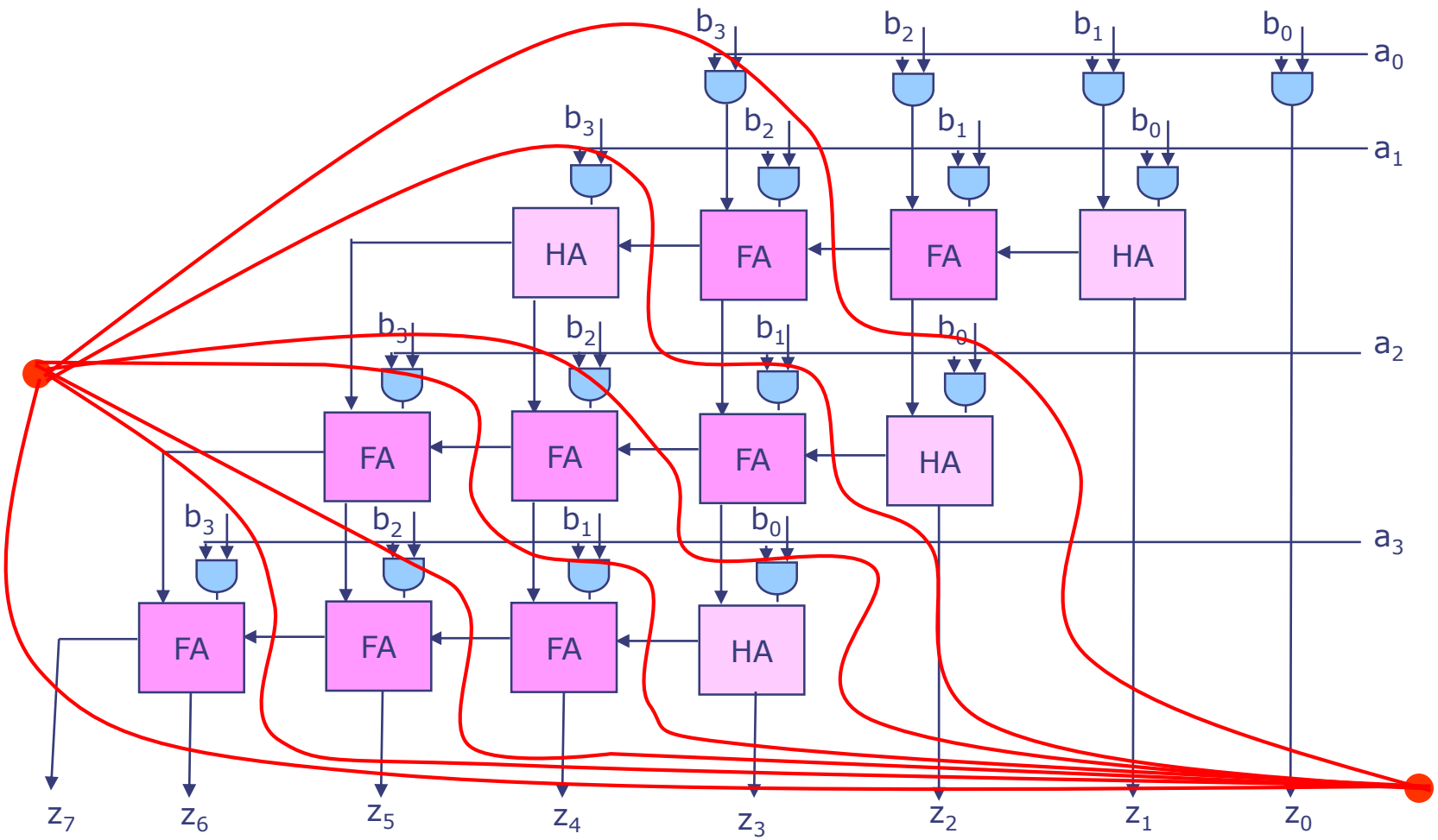

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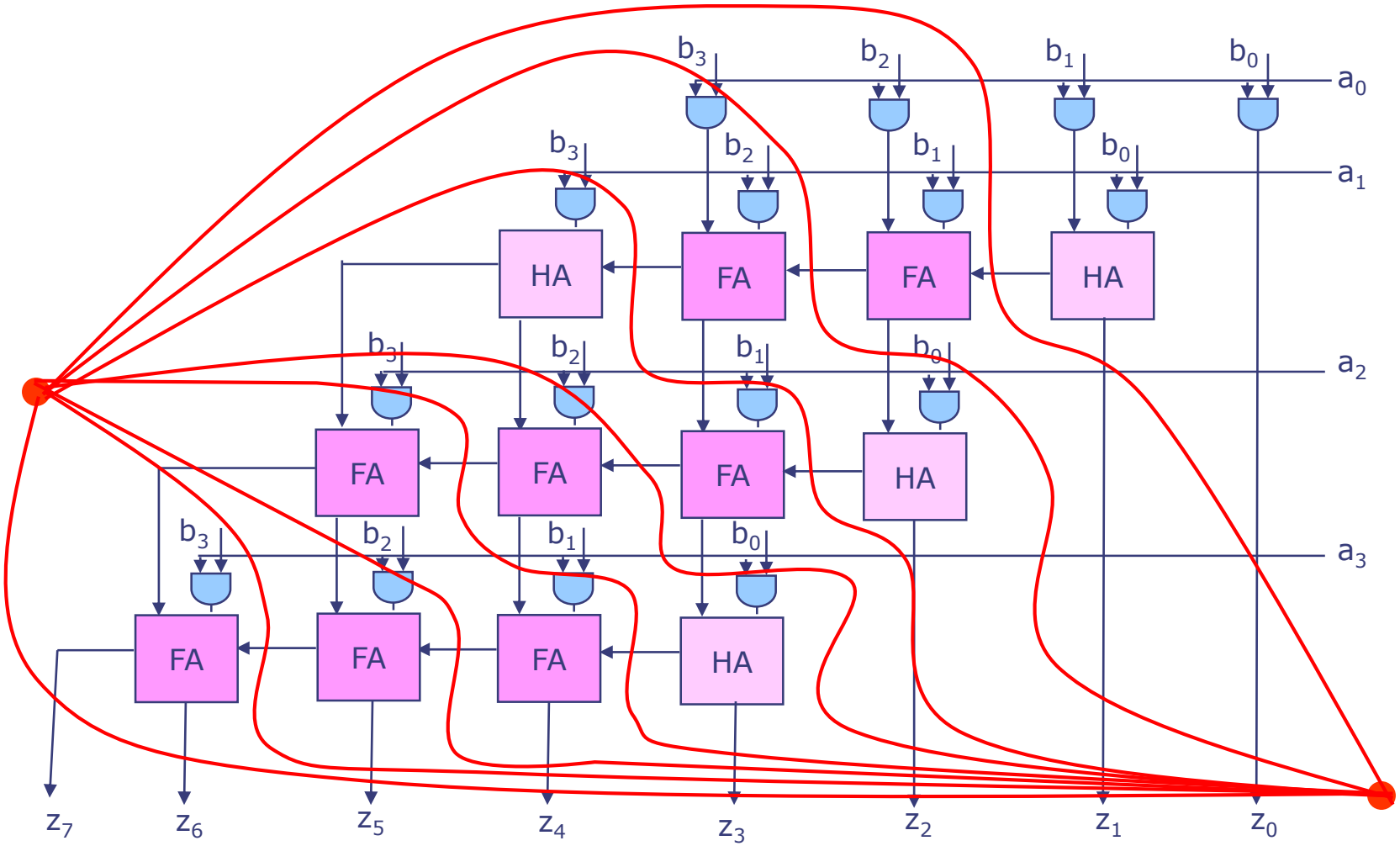

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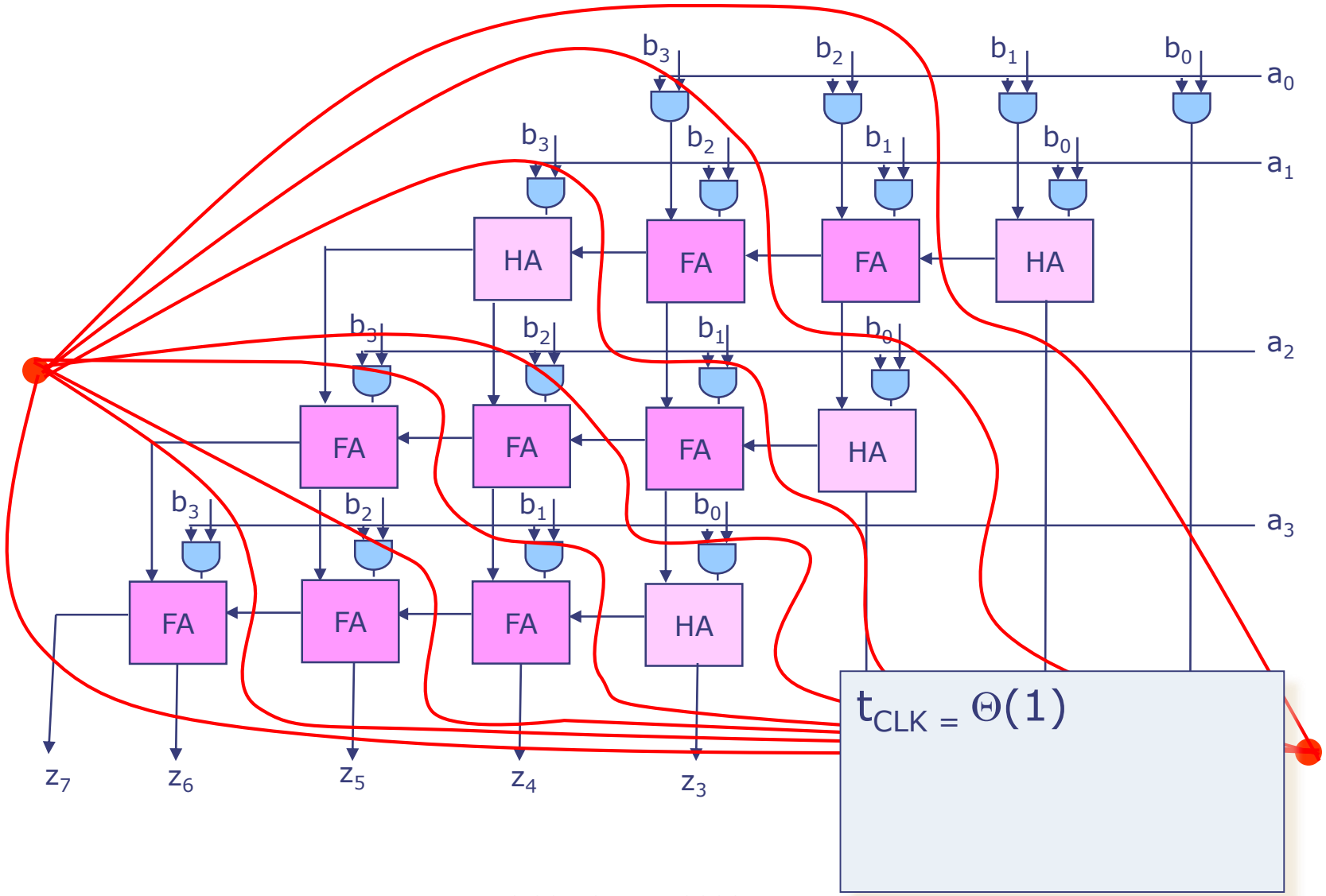

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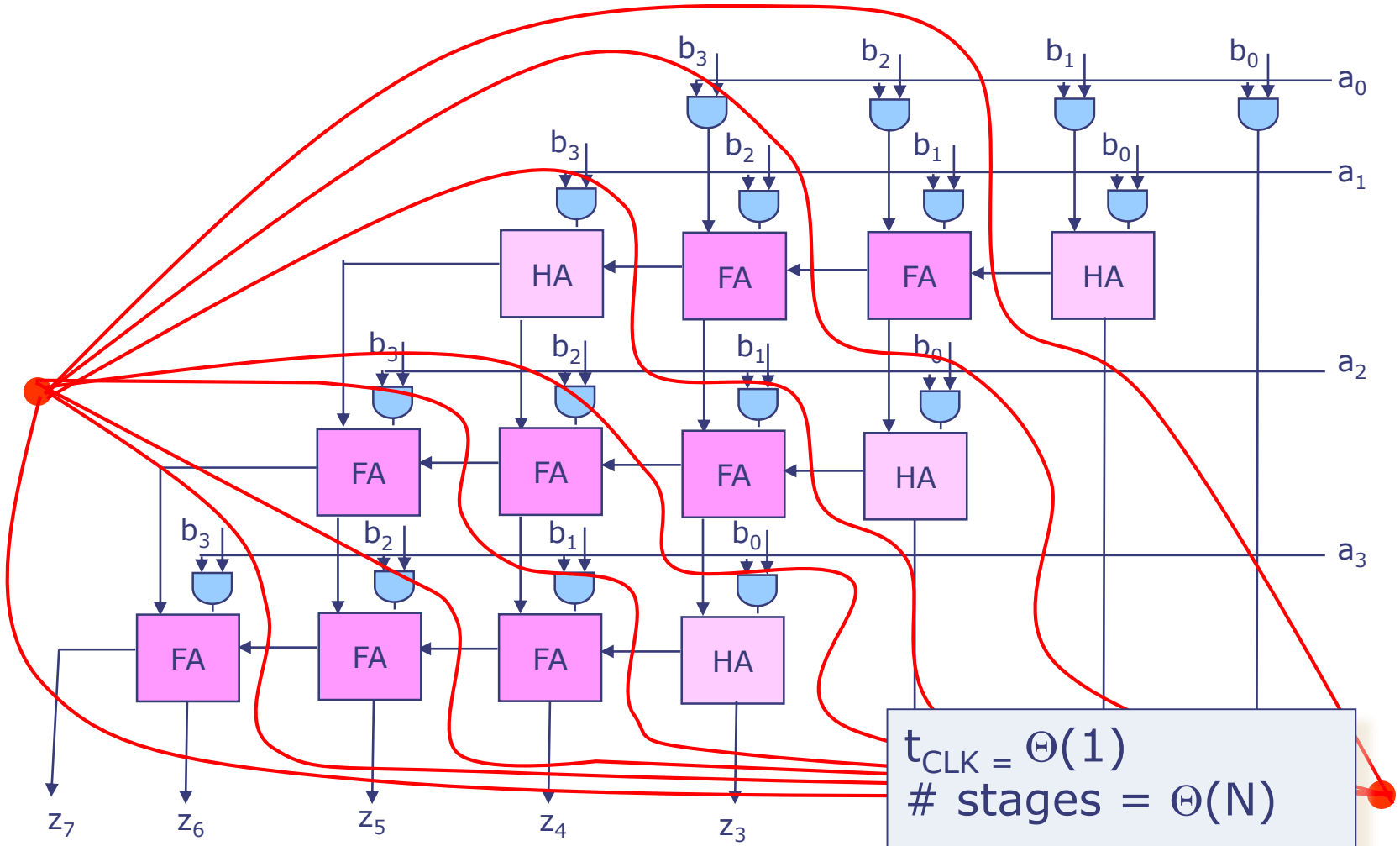

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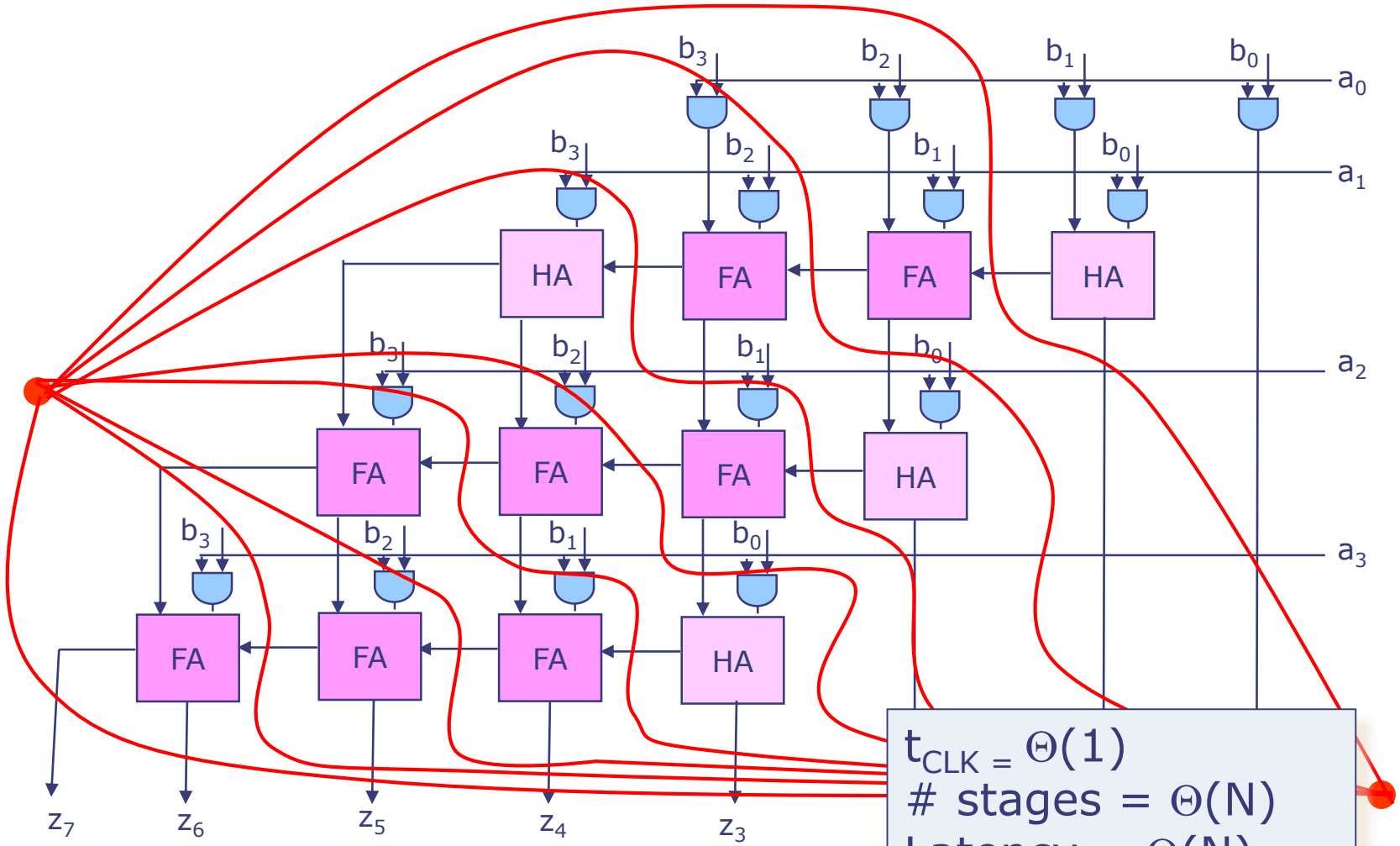

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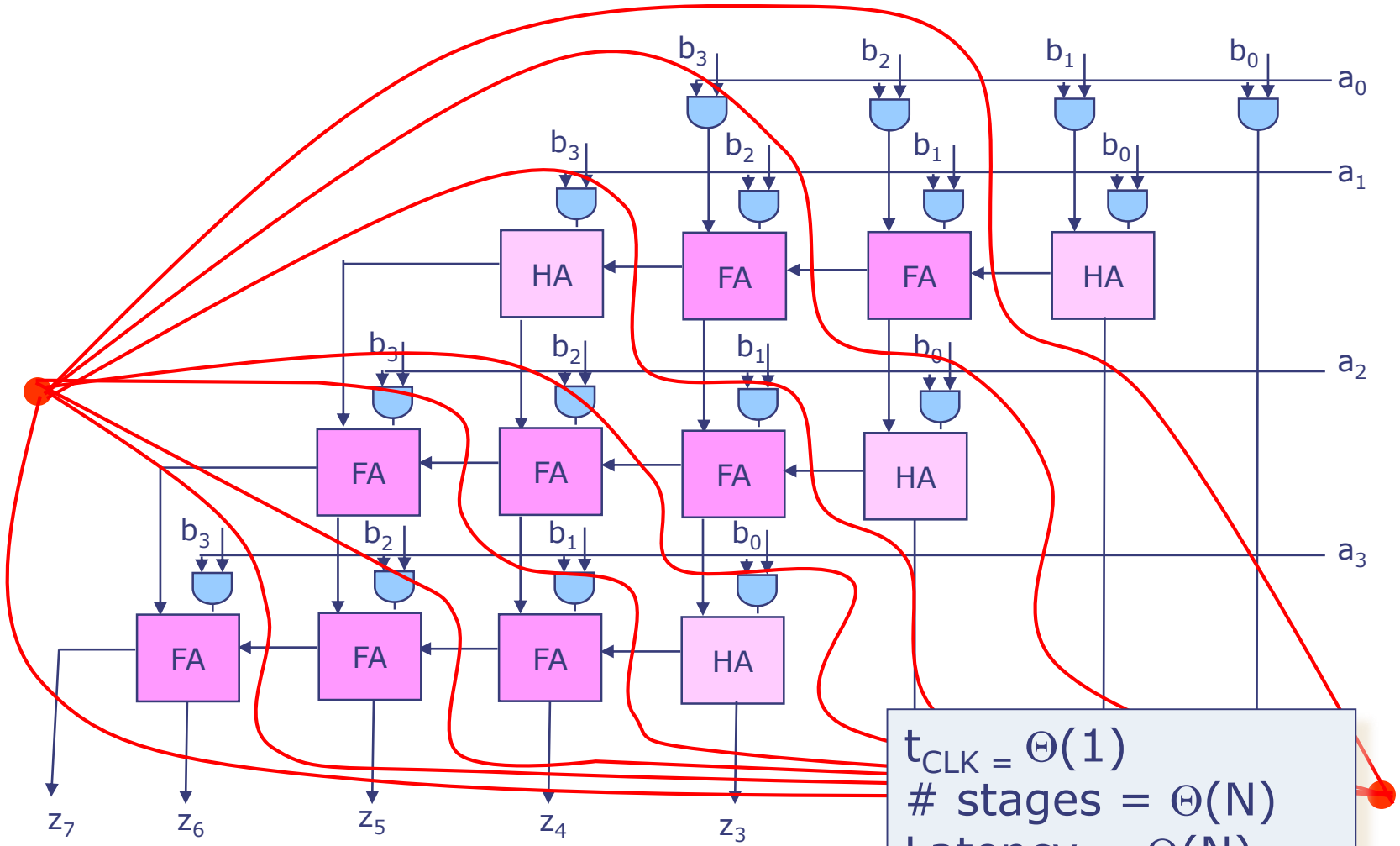

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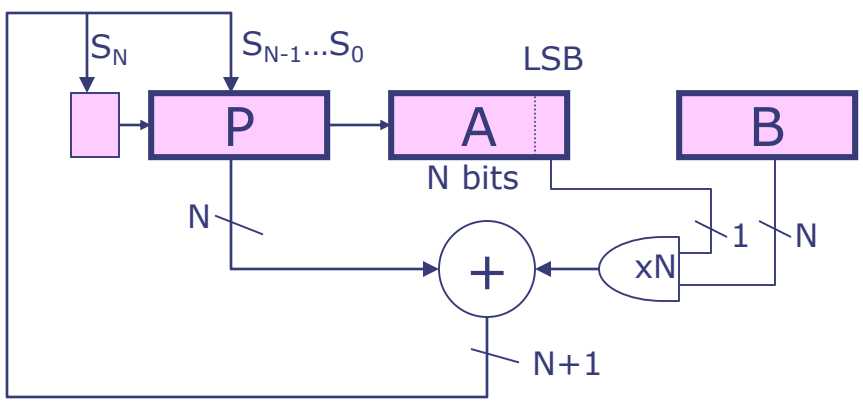


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Init: P←0, load A&B

Repeat N times {
   P ← P + (A_LSB==1 ? B : 0)
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Done: 2N-bit result in P,A
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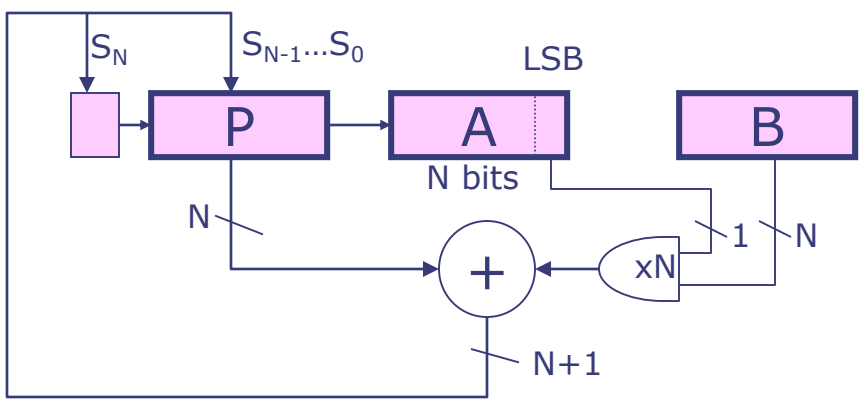


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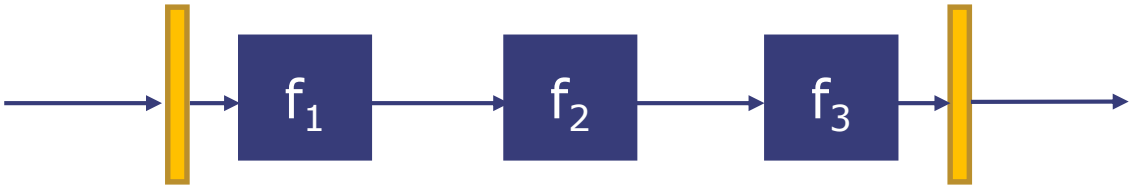
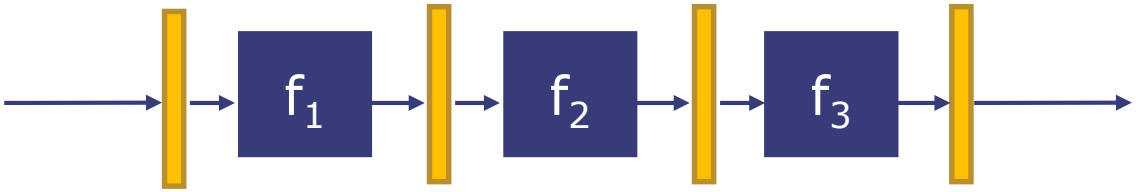
Tradeoff: reduced area, but lower throughput

Summary: Design Alternatives

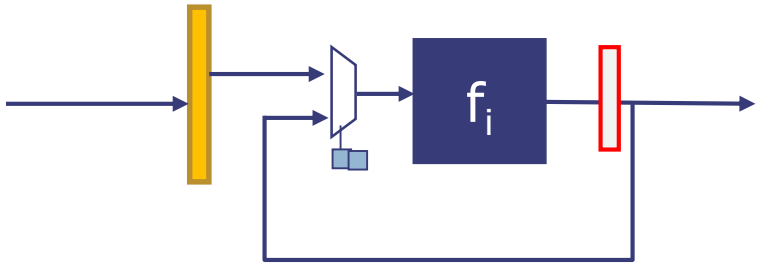
Several combinational modules in one pipeline stage (A)



One module per pipeline stage (B)



Folded reuse a block, multi-cycle (C)



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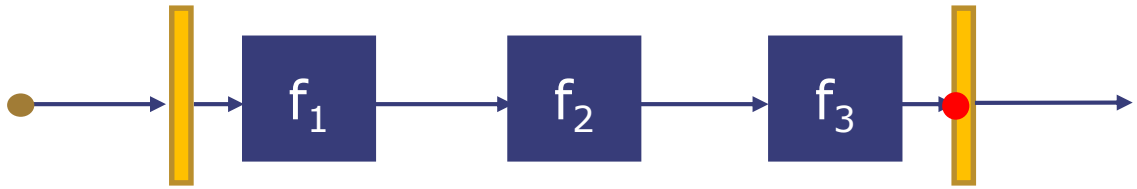

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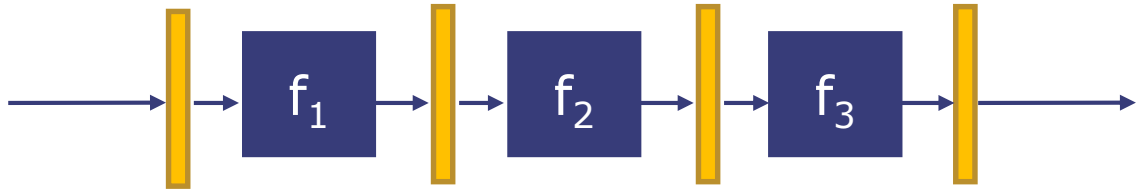

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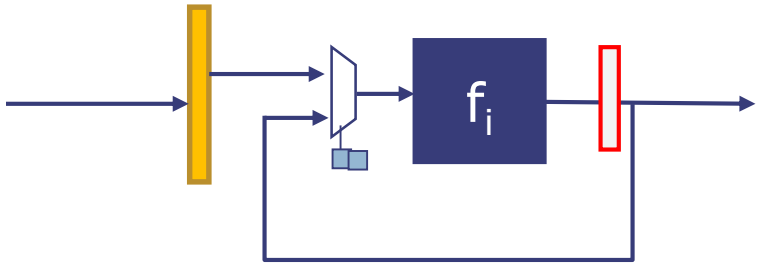

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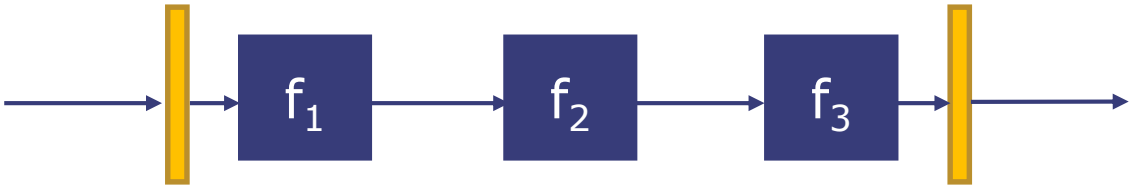

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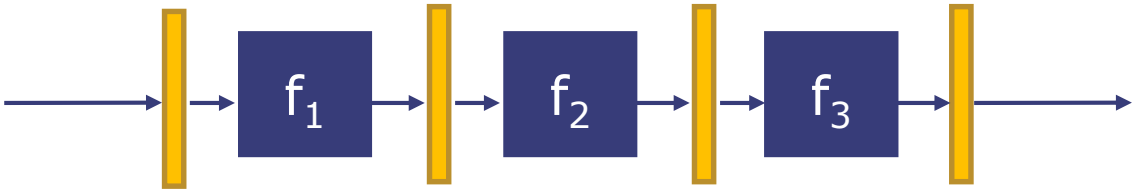

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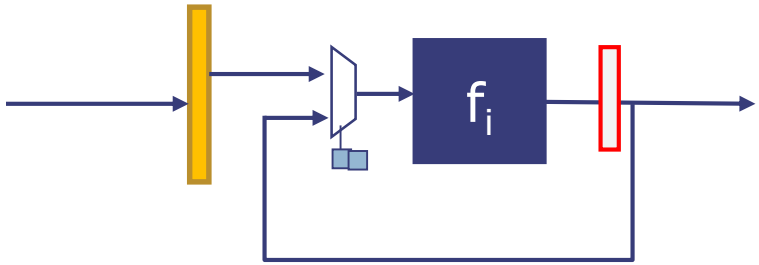

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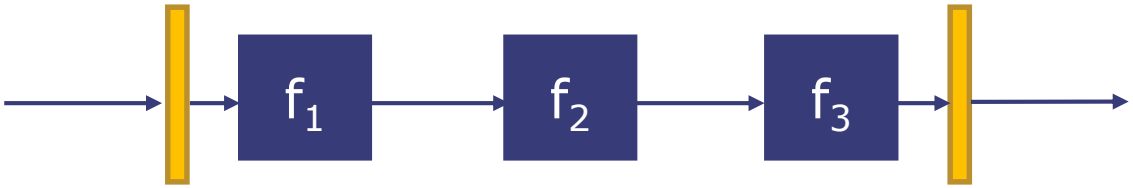

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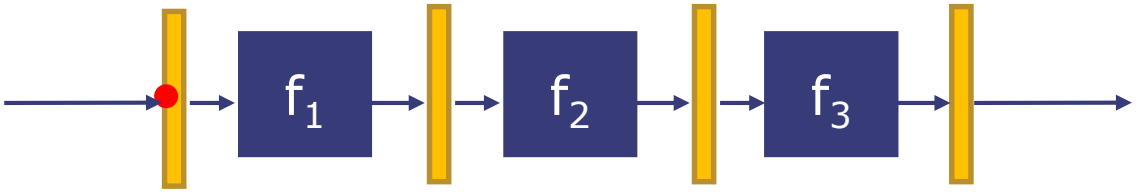

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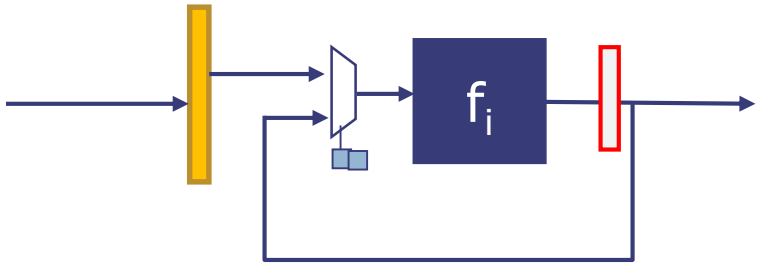

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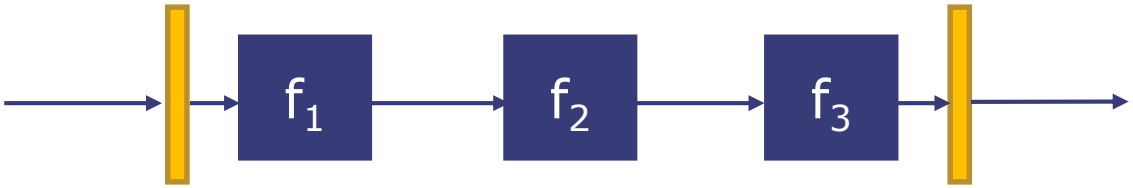

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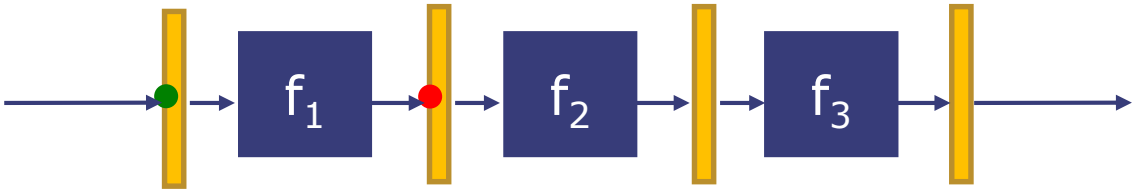

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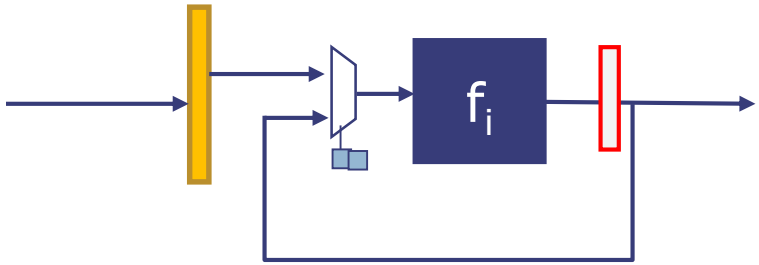

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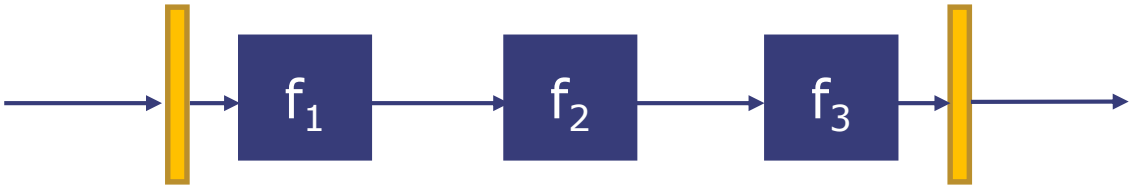

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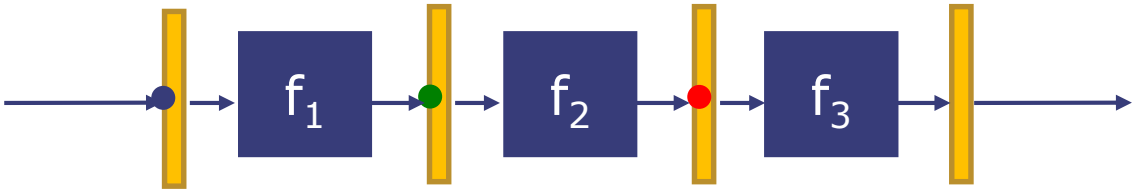

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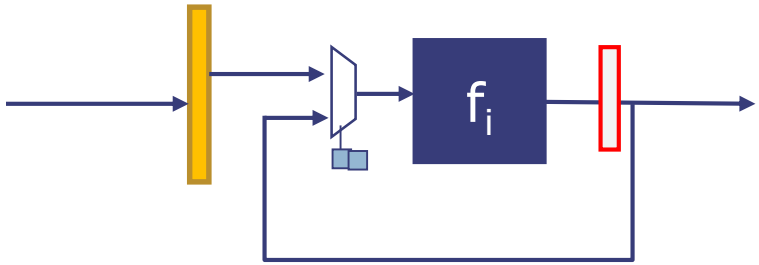

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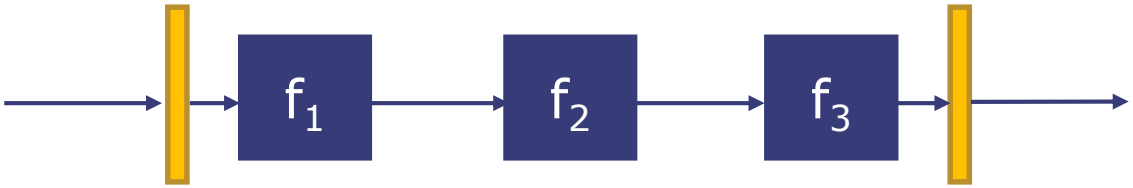

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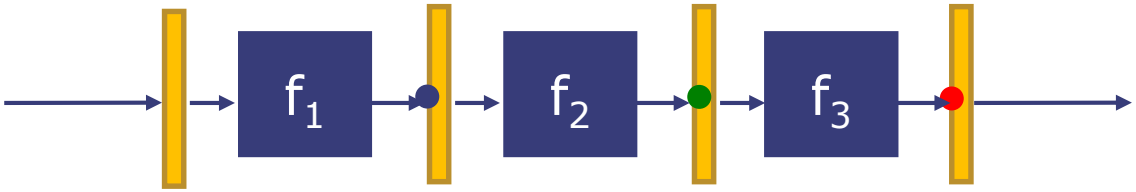

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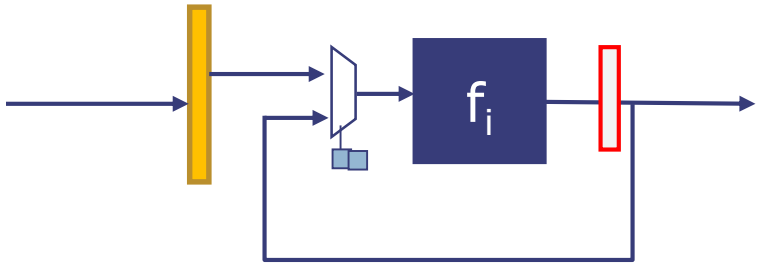

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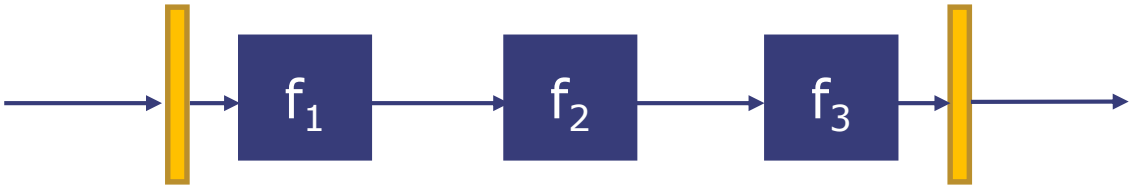

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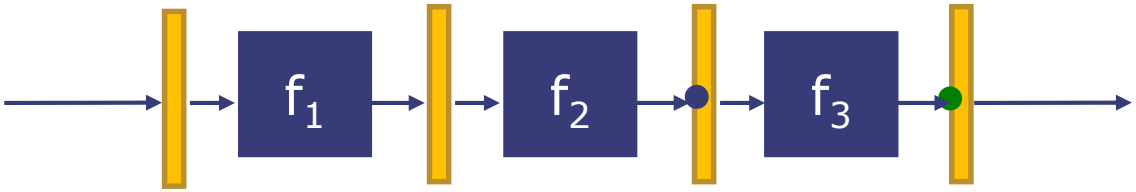

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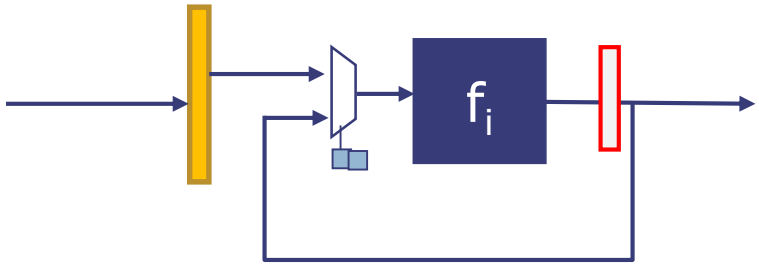

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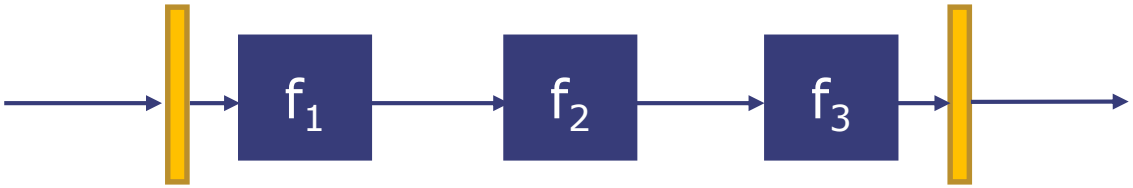

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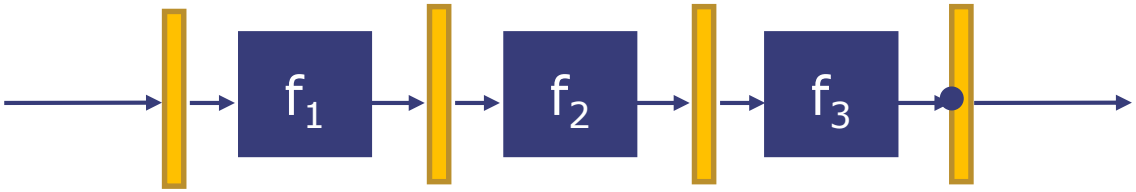

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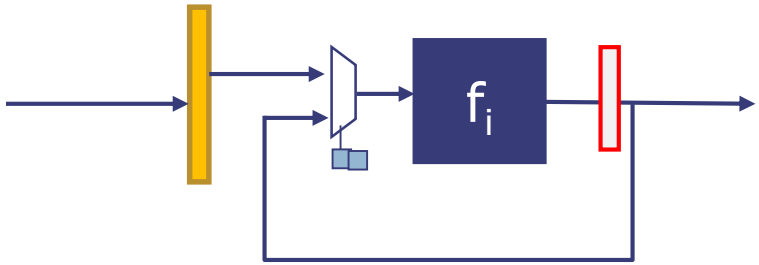

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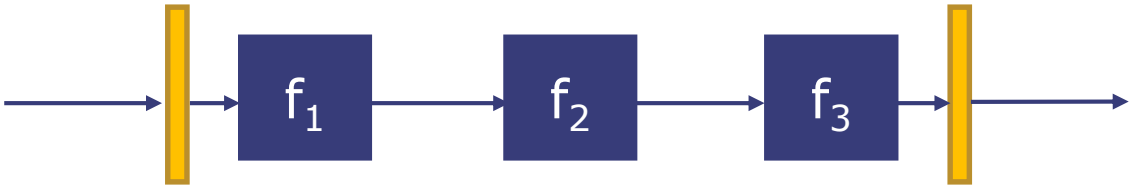

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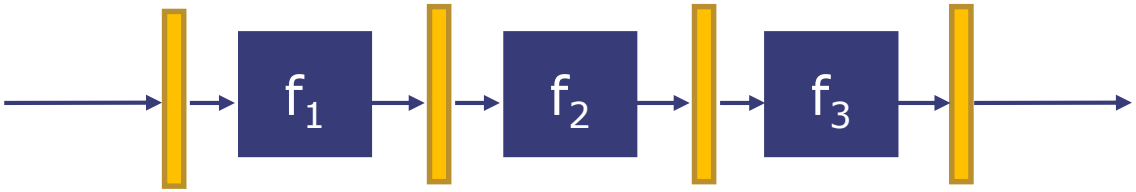

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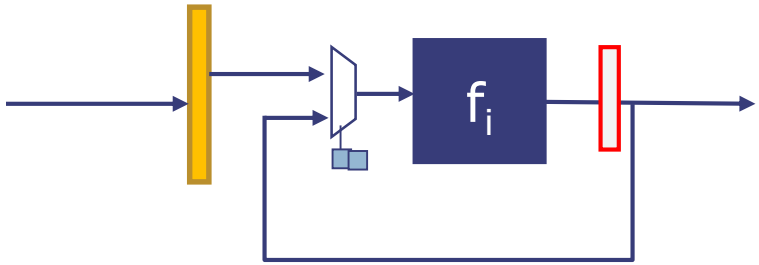

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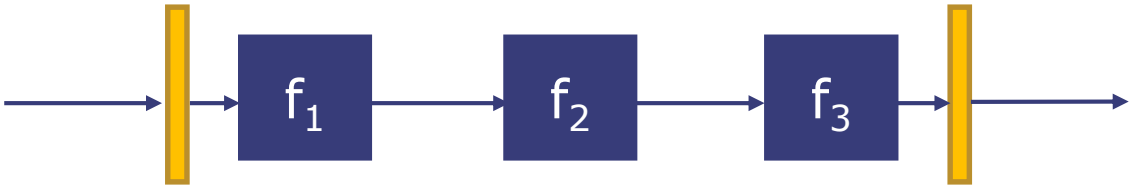

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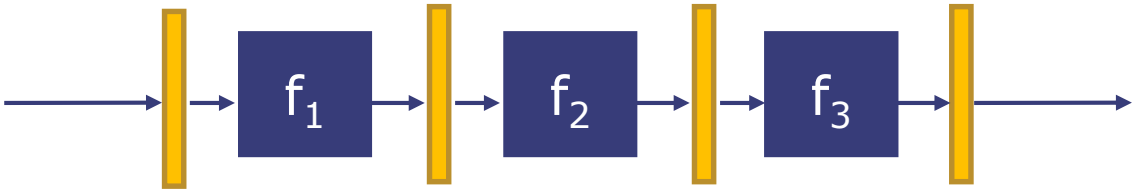

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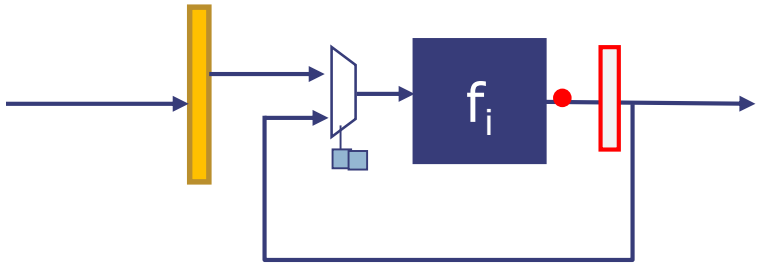

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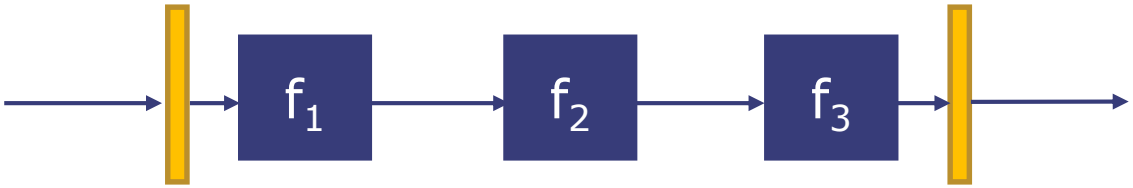

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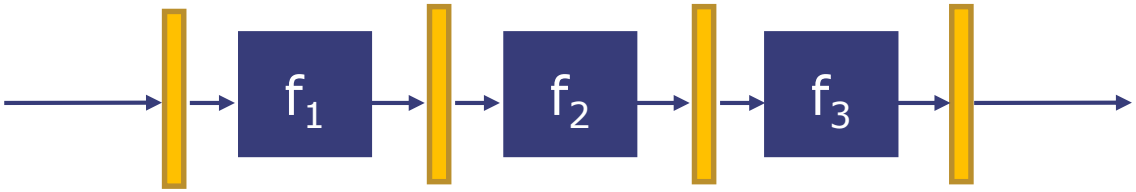

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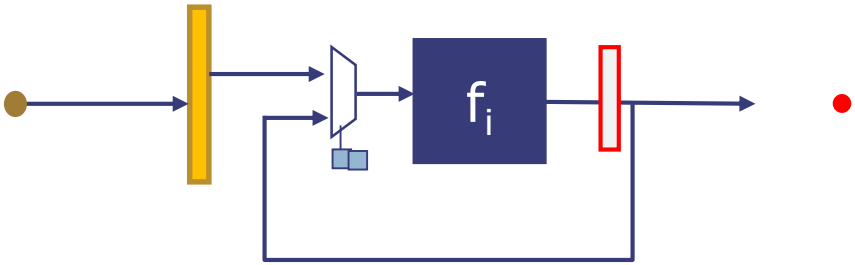

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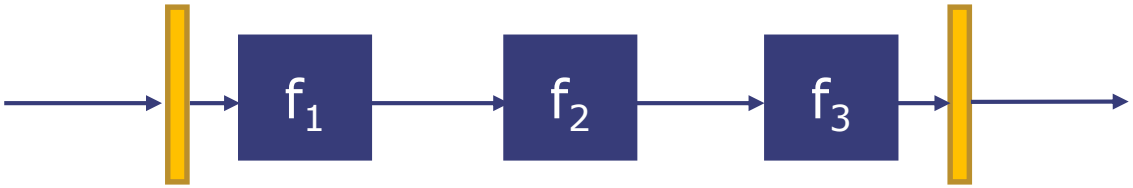

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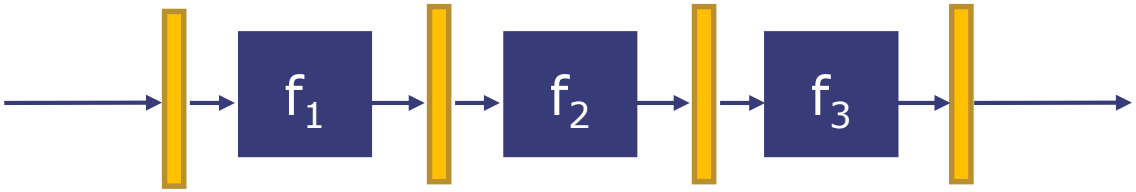

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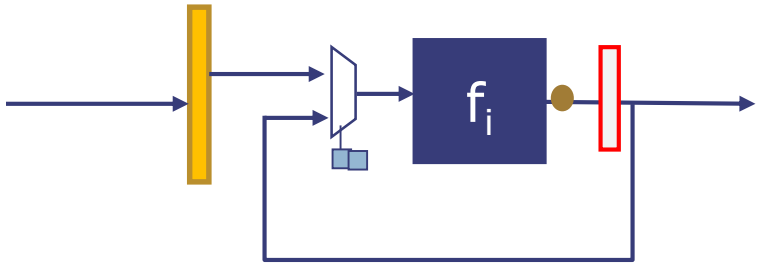

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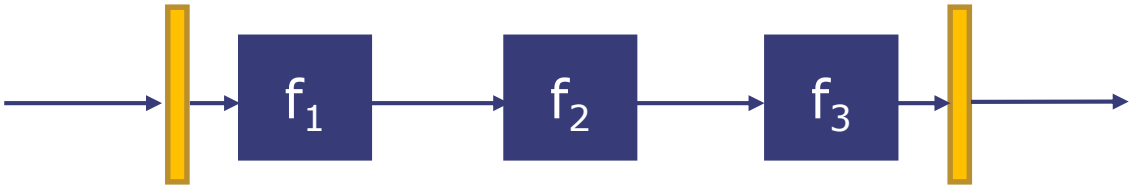

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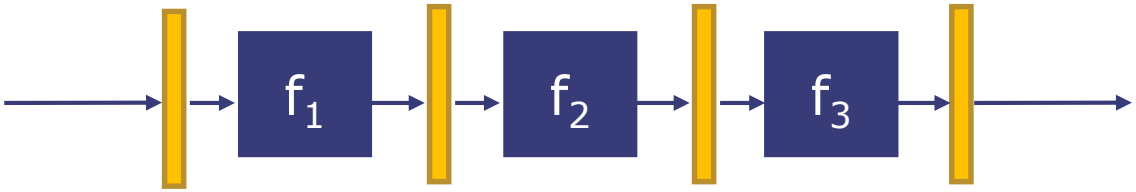

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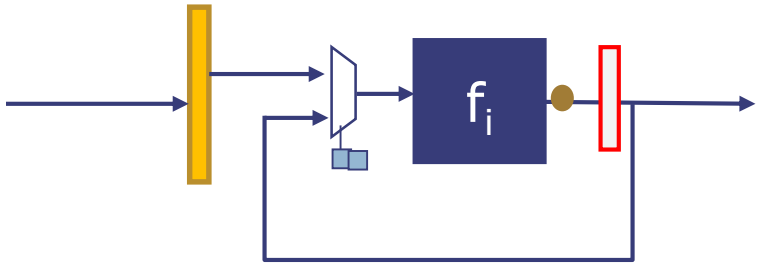

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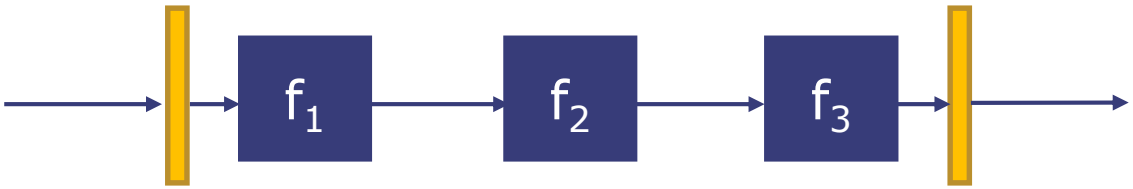

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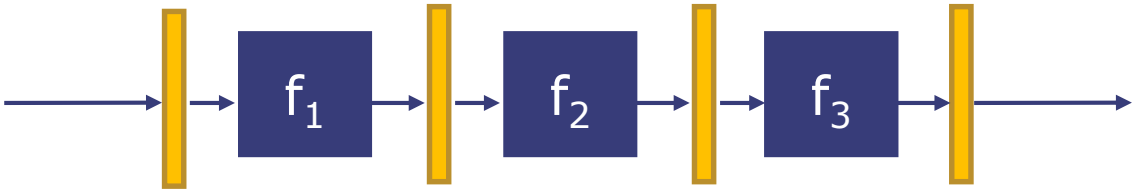

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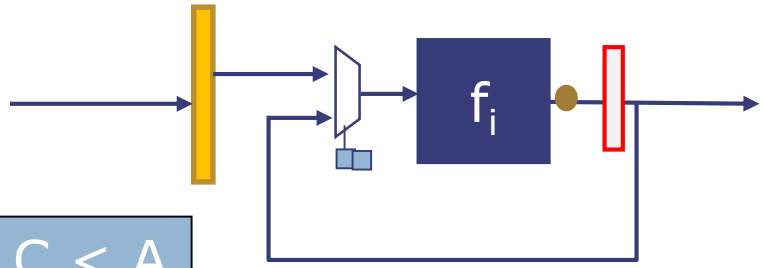

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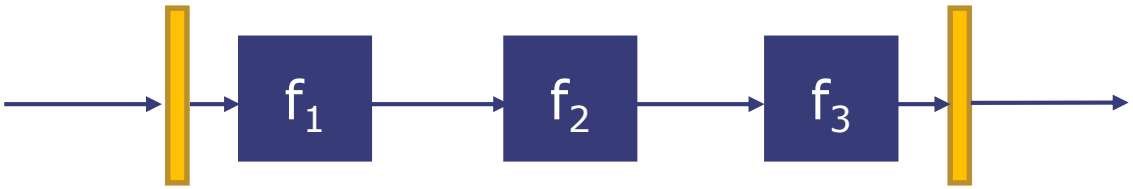

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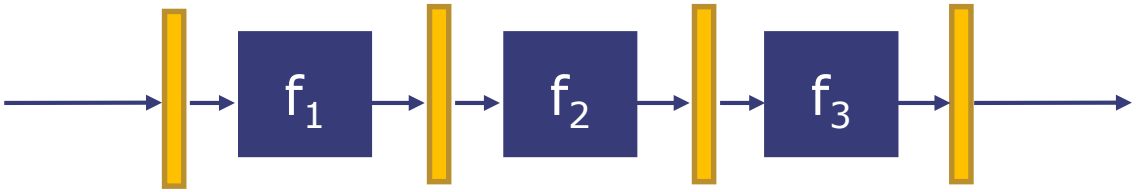

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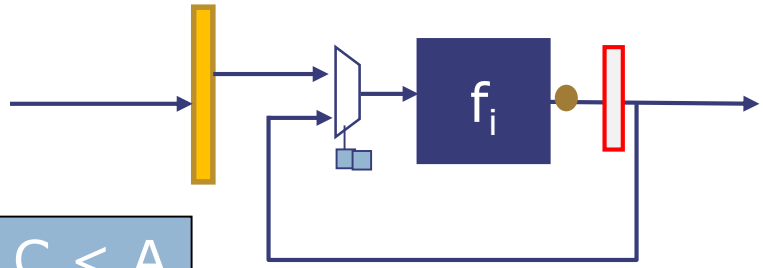

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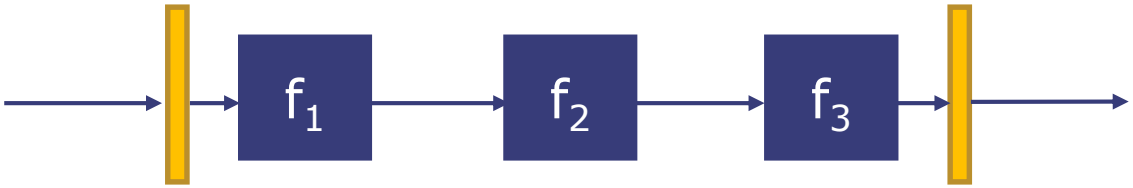

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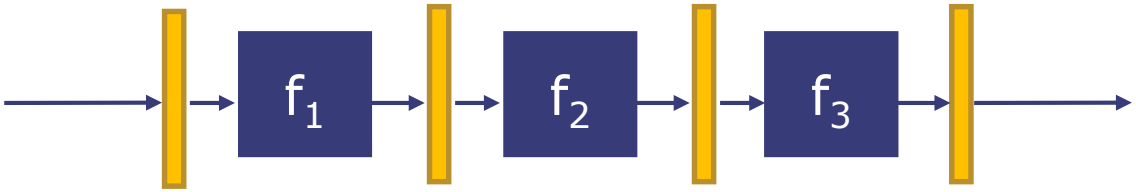

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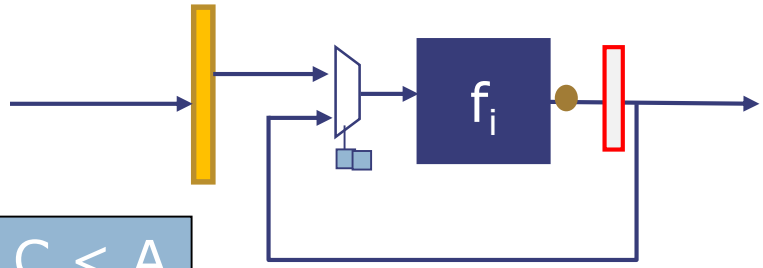

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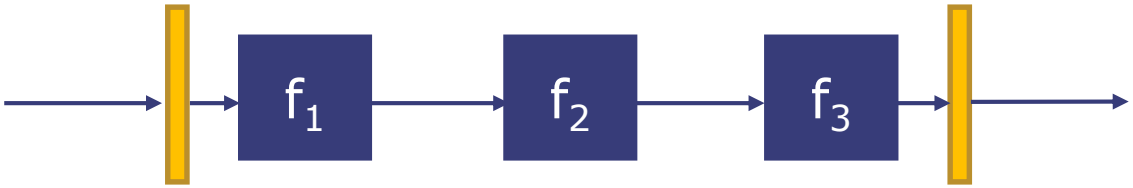

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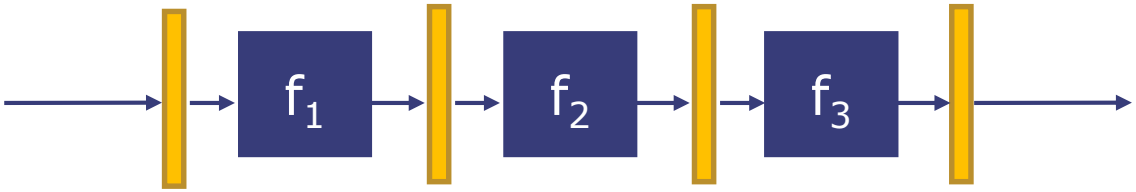

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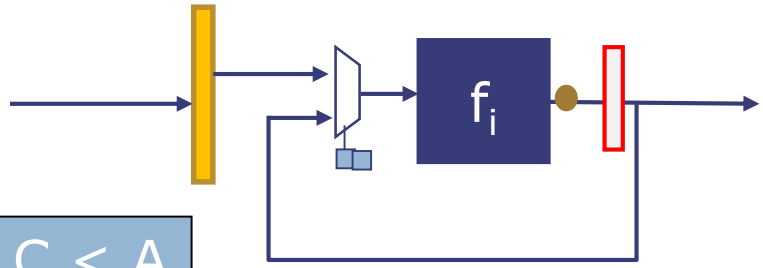

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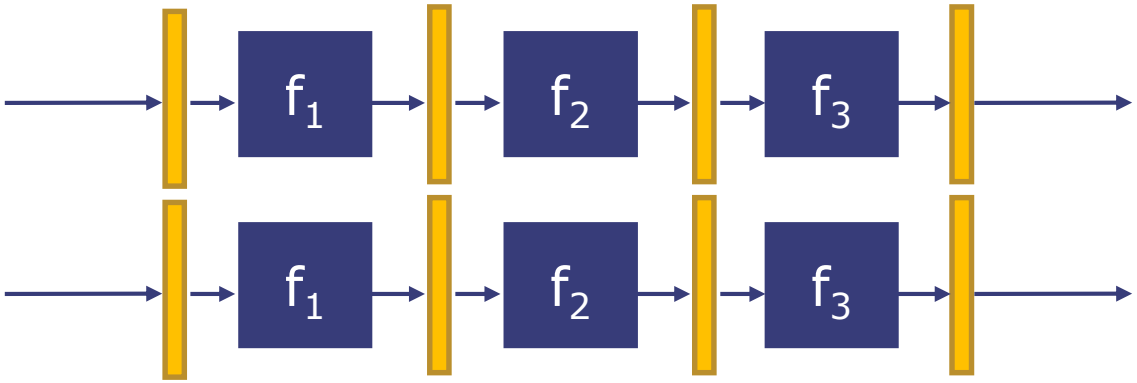

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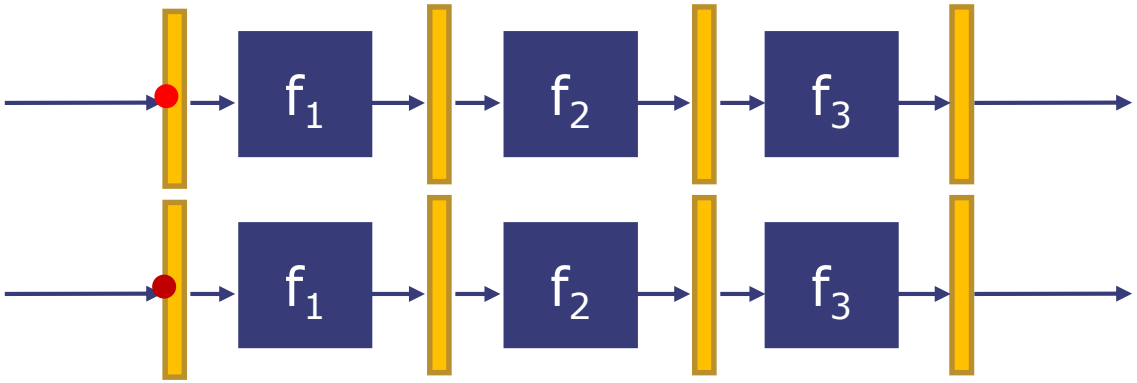

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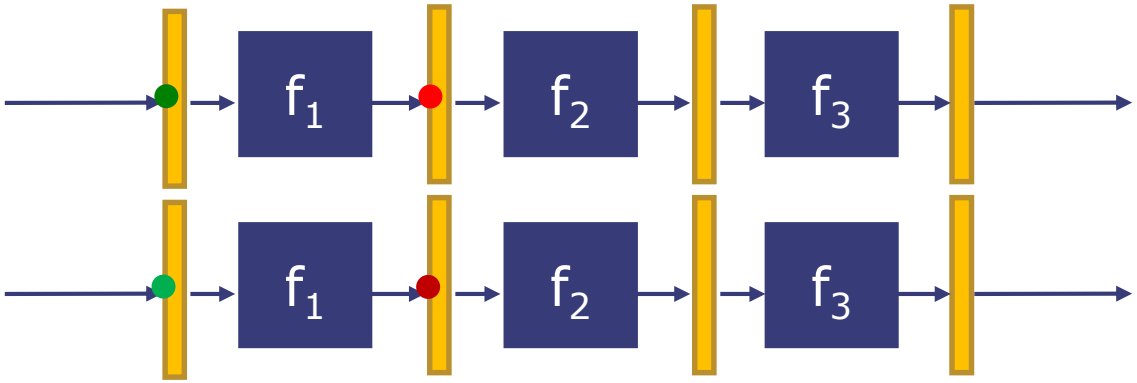

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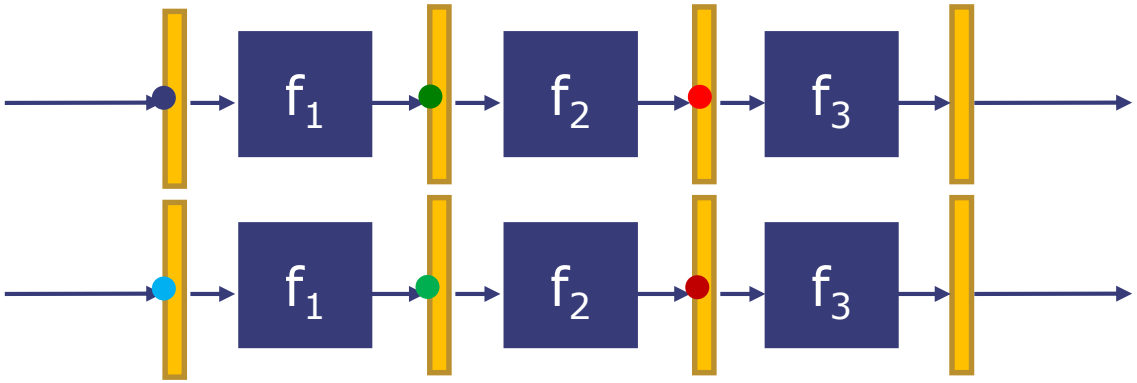

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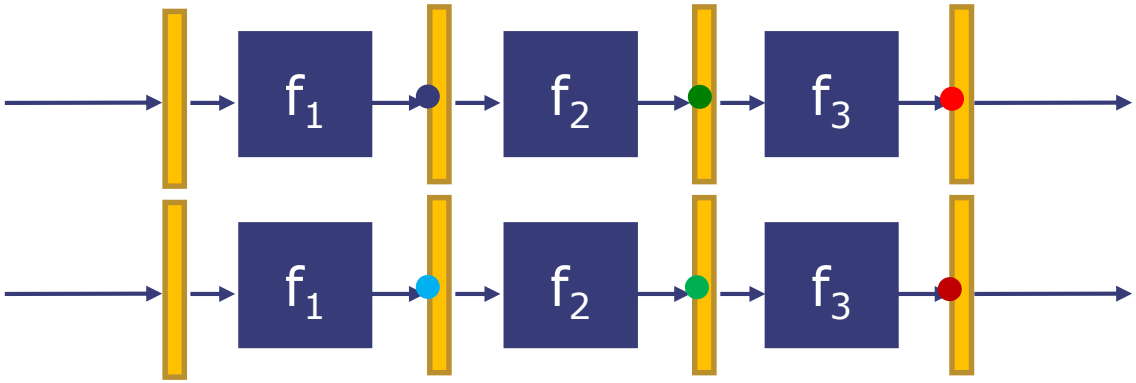

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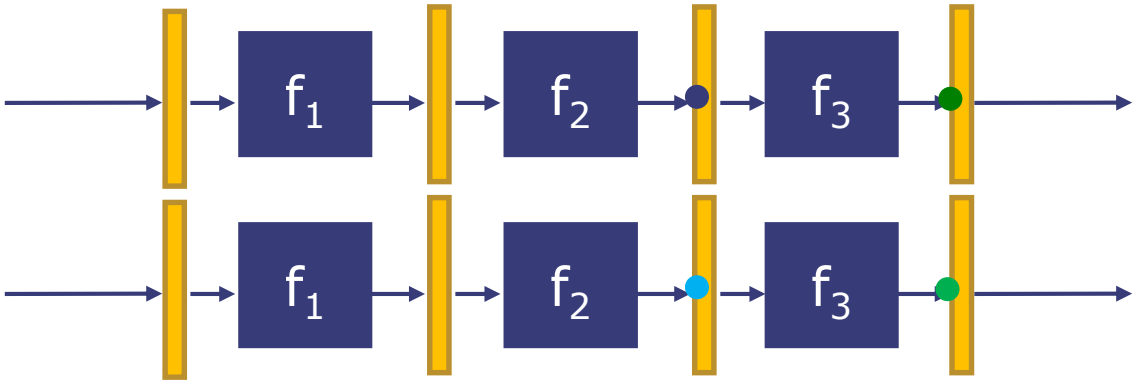

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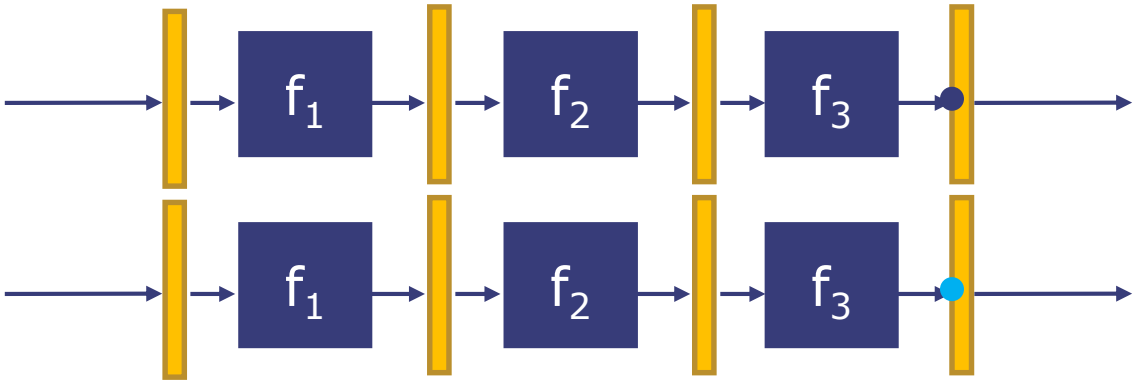

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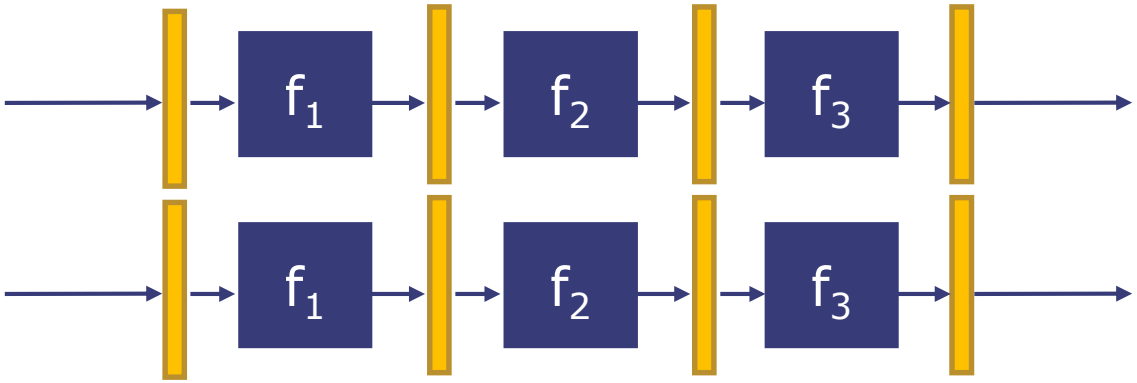

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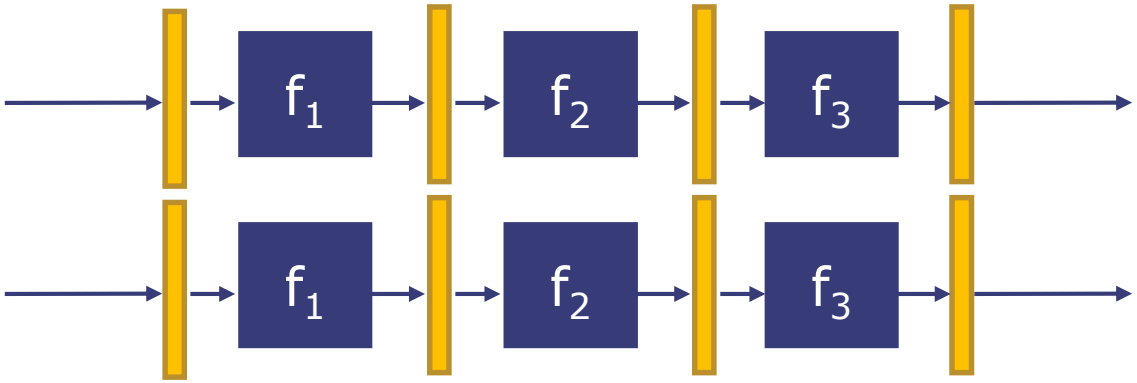

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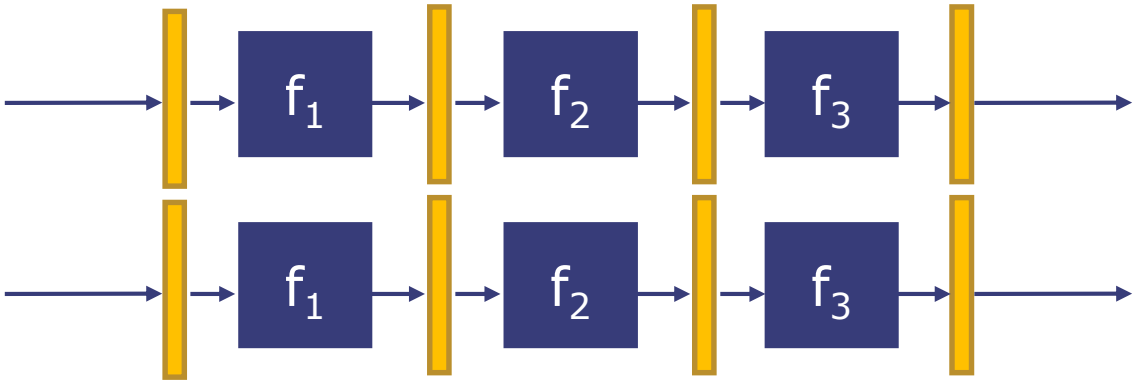

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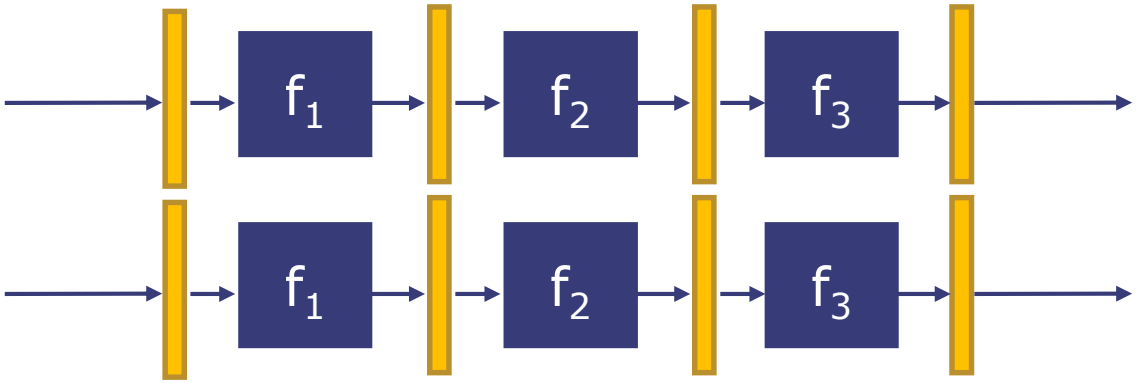

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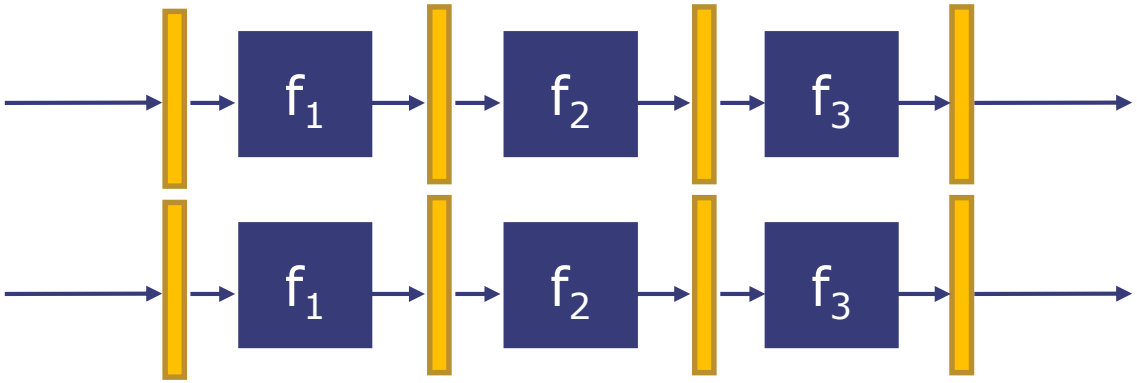

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Throughput = $1/t_{CLK}$

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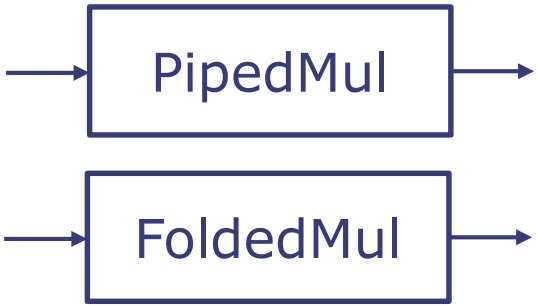

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Similar t_{CLK} vs. PipedMul, lower area

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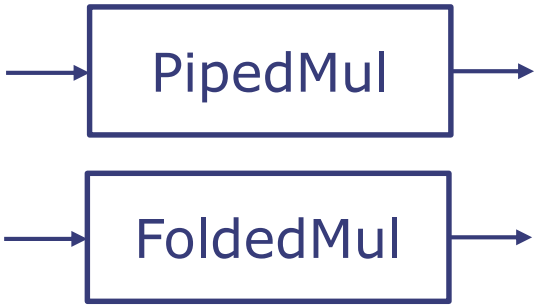

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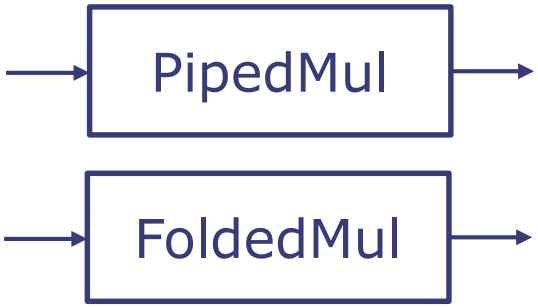

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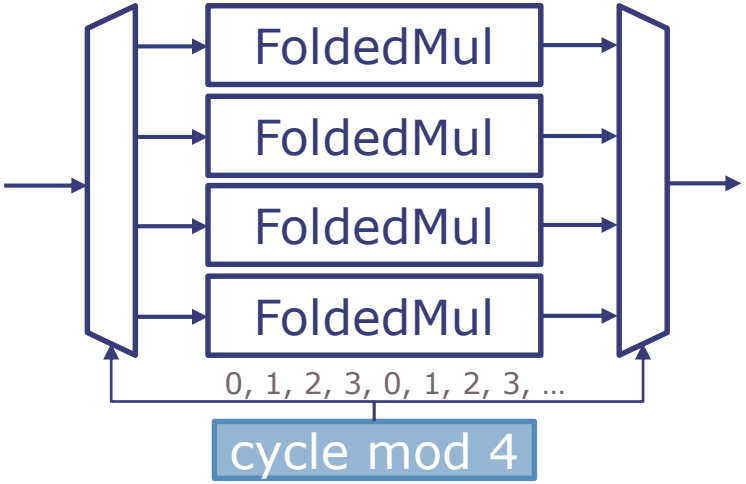

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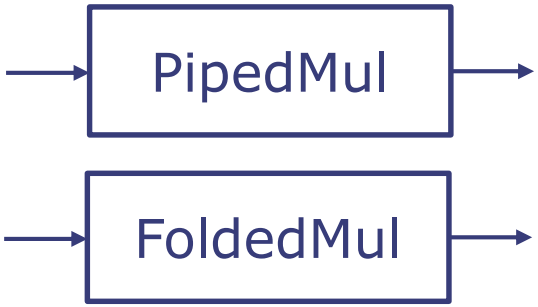

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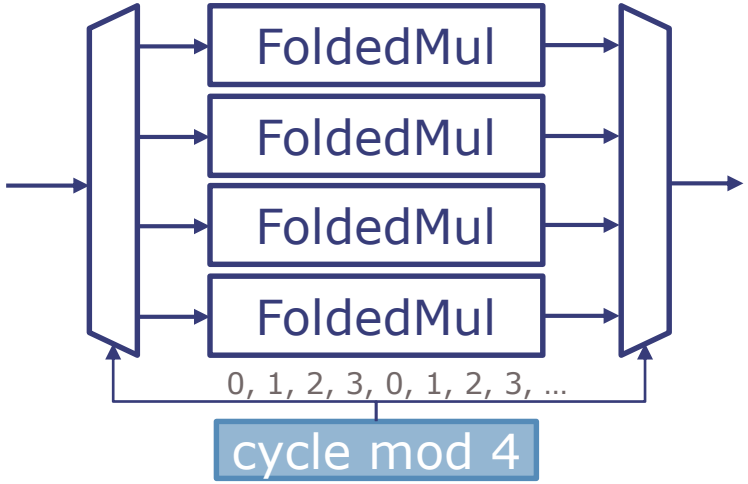

Replicate FoldedMul 4 times
Each FoldedMul produces an output and takes a new input every 4 cycles
Throughput = $4*1/(4t_{CLK}) = 1/t_{CLK}$

Software vs. Hardware Design
Timing is the key difference

1. Software interfaces (even instructions) are timing-independent
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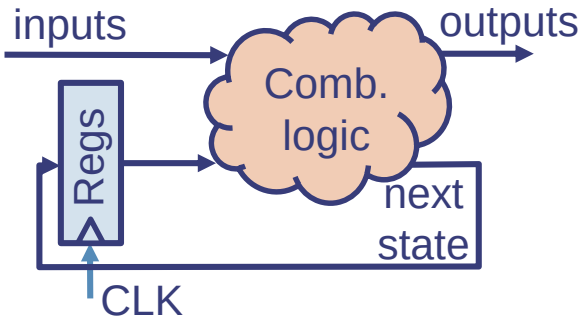
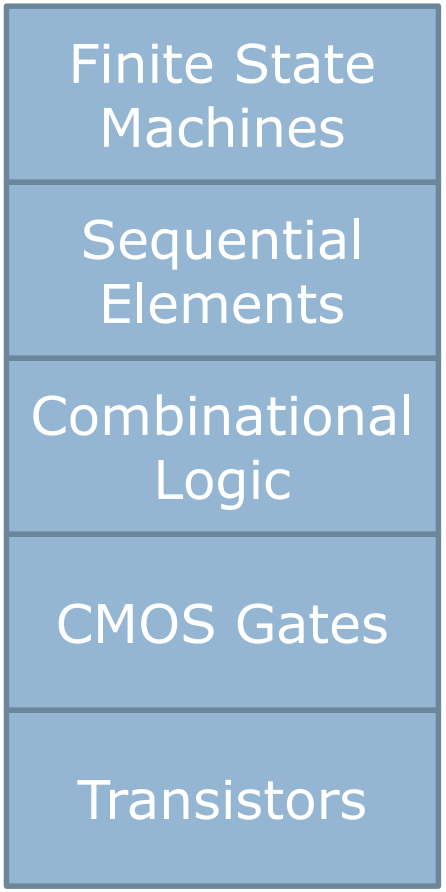
2. Hardware design is all about timing
   - Specify what happens on every clock cycle…
   - …which itself determines the length of the clock cycle

```
module Factorial;
  Reg#(Word) a(0);
  Reg#(Word) b(0);
  rule step;
    …
```



From Special-Purpose FSMs to General-Purpose Processors

6.004 So Far


Finite State Machines
Sequential Elements
Combinational Logic
CMOS Gates
Transistors

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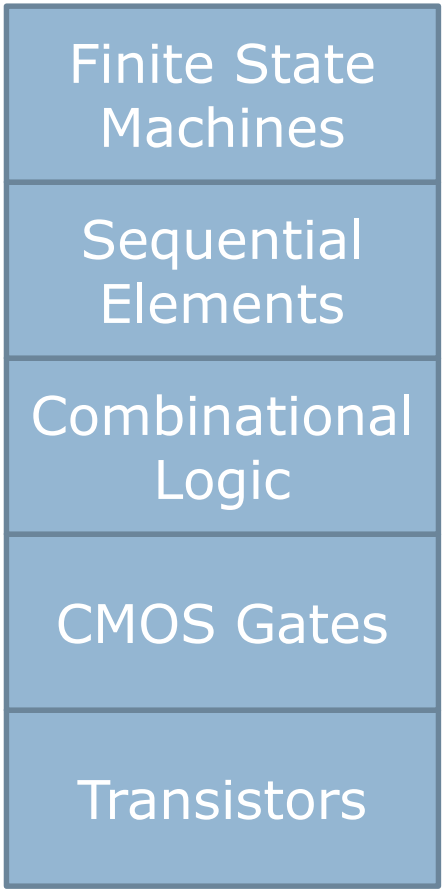

- What can you do with these?
  - Take a (solvable) problem
  - Design a procedure (recipe) to solve the problem
  - Design a finite state machine that implements the procedure and solves the problem

6.004 So Far

Finite State Machines
Sequential Elements
Combinational Logic
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Transistors

- What can you do with these?
  - Take a (solvable) problem
  - Design a procedure (recipe) to solve the problem
  - Design a finite state machine that implements the procedure and solves the problem
- What you'll be able to do after this week:
  - Design a machine that can solve any solvable problem, given enough time and memory (a general-purpose computer)

Example: Factorial FSM

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Let’s design a circuit to compute factorial(N)

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Python:

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a = 1
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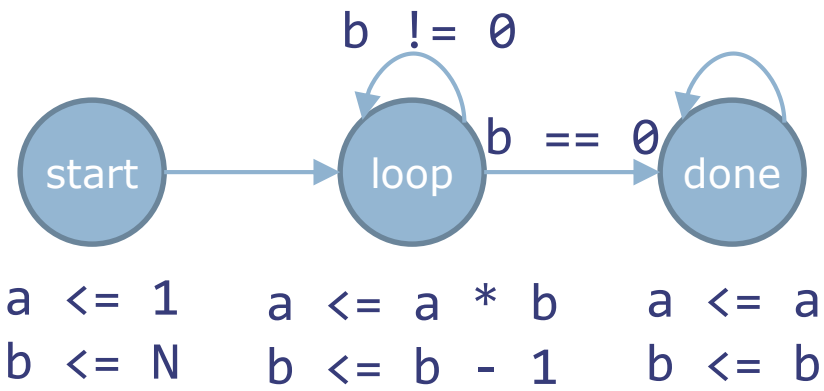
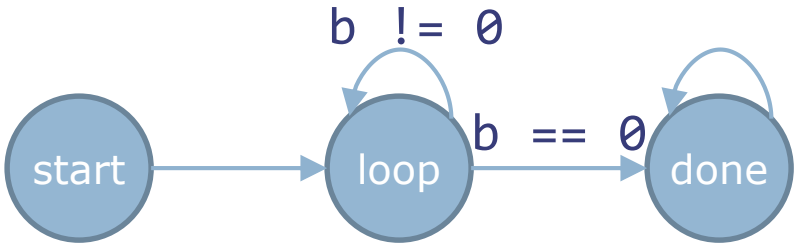
High-level FSM:



- Describes cycle-by-cycle behavior
- Registers (a, b)
- States (start, loop, done)
- Boolean transitions (b==0, b!=0)
- Register assignments in states (e.g., a ← a * b)

Datapath for Factorial

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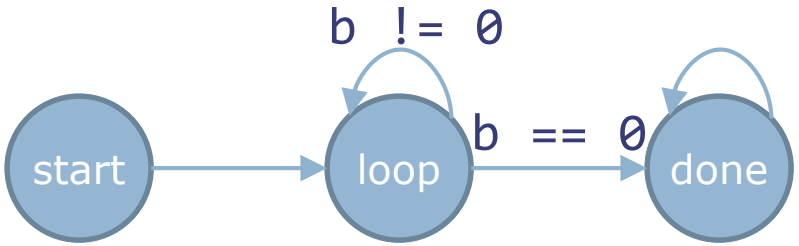


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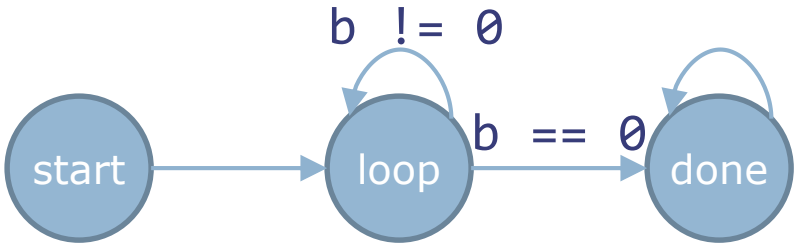


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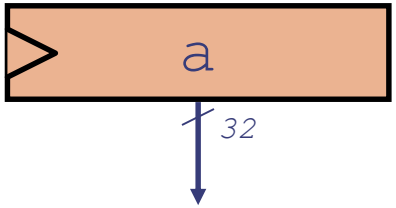

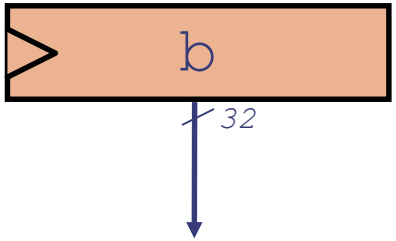

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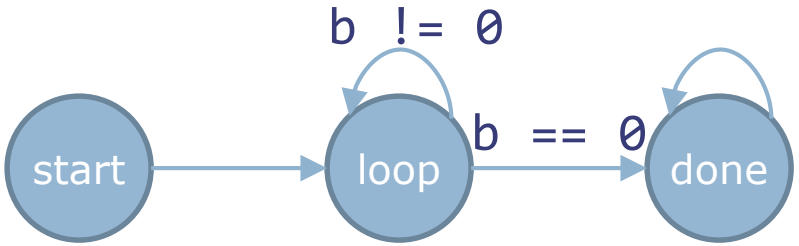


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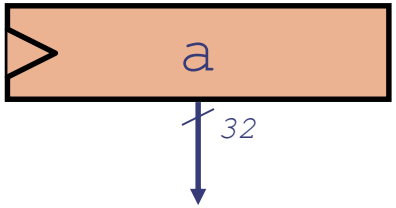

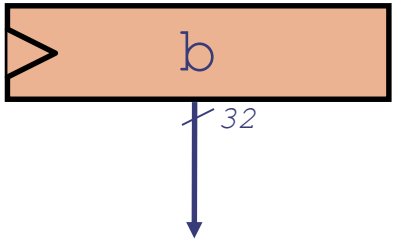

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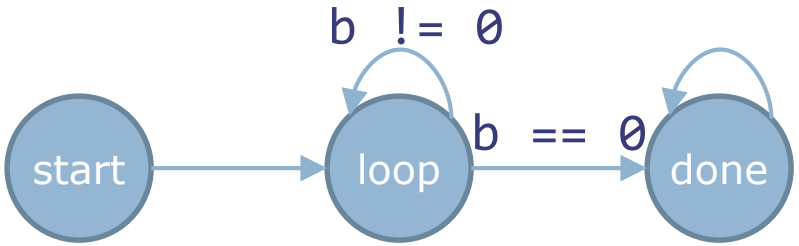


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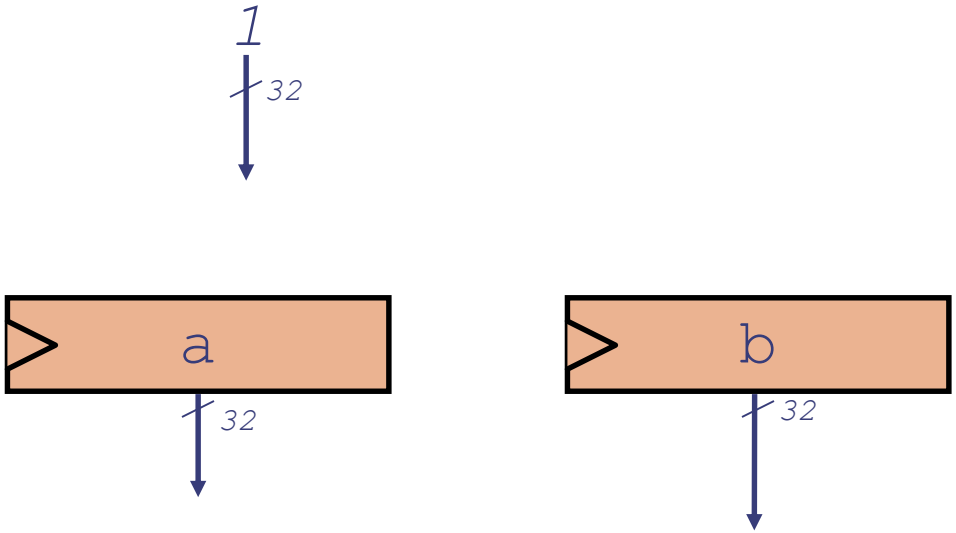

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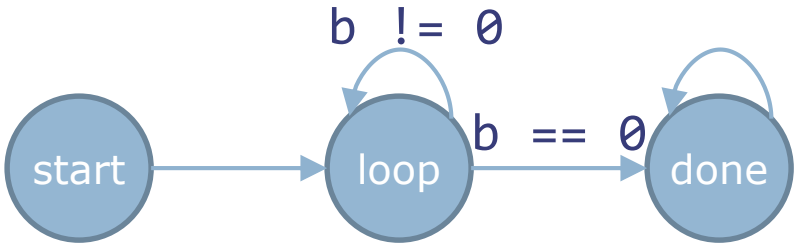


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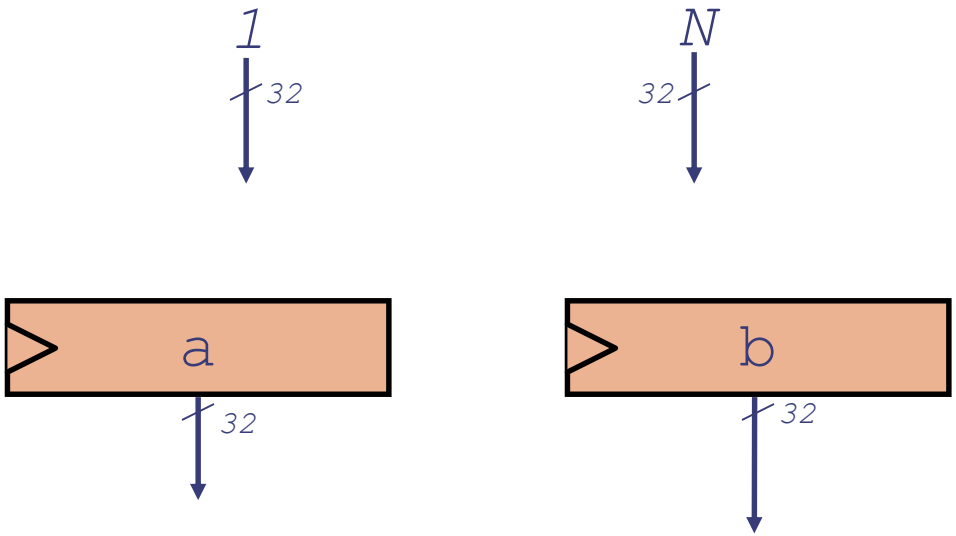

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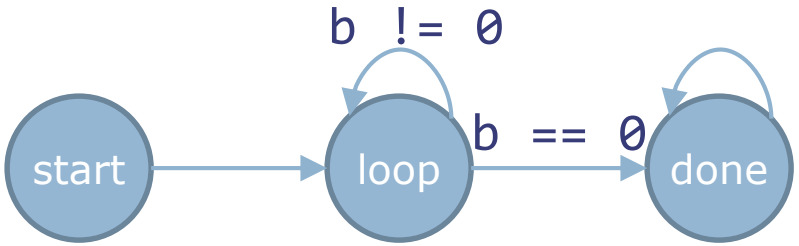


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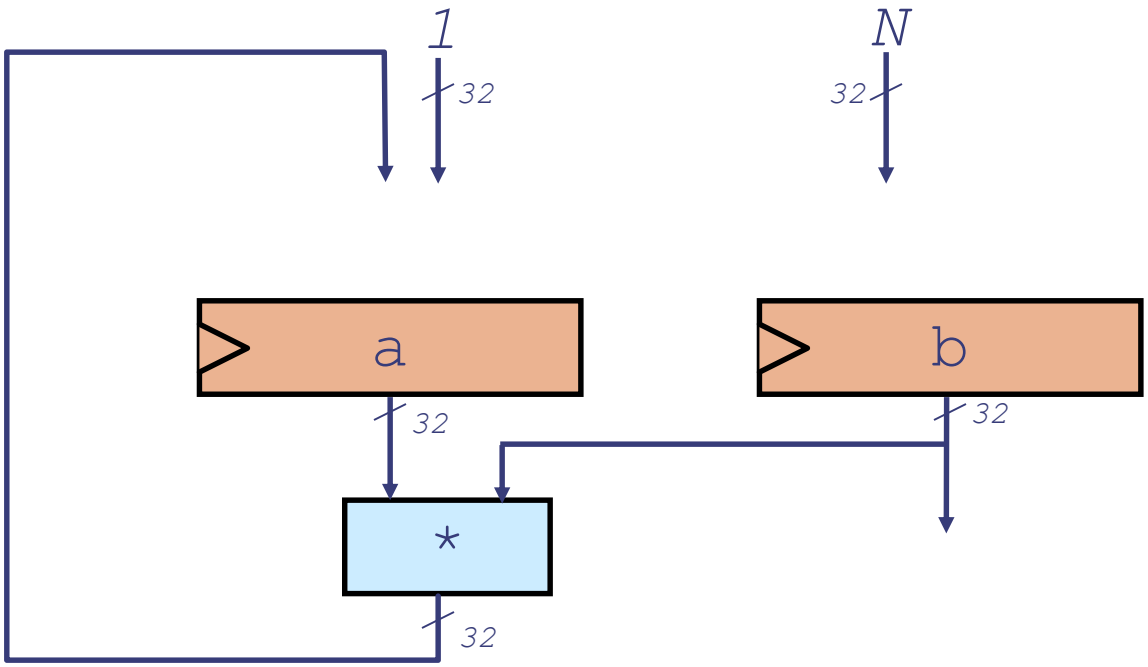

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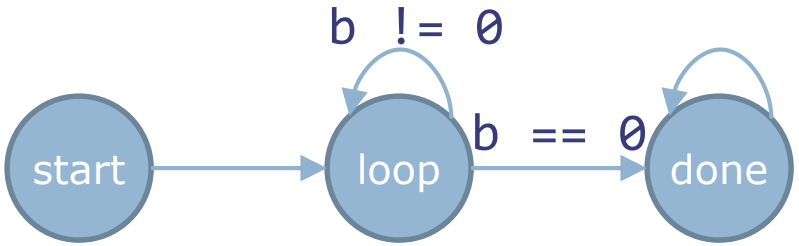


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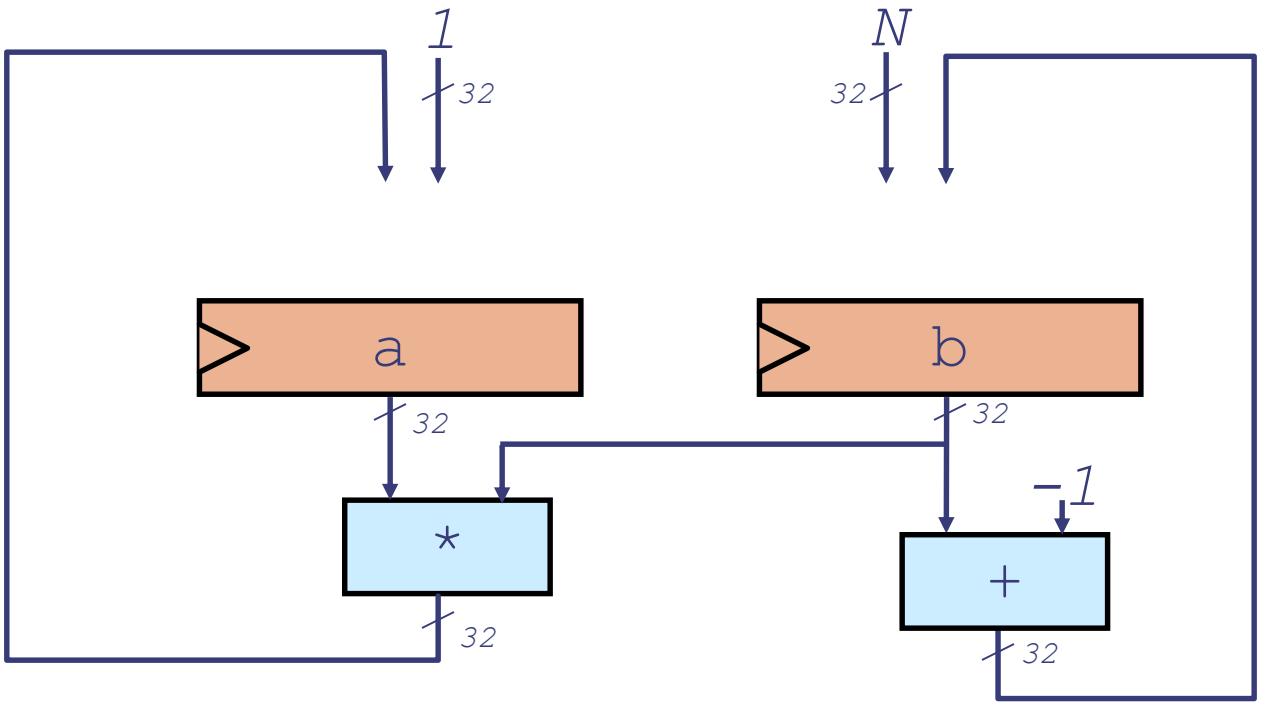

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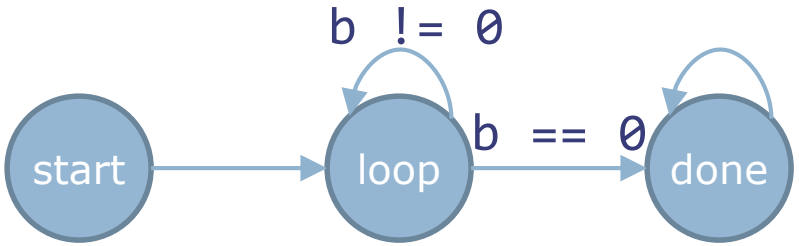


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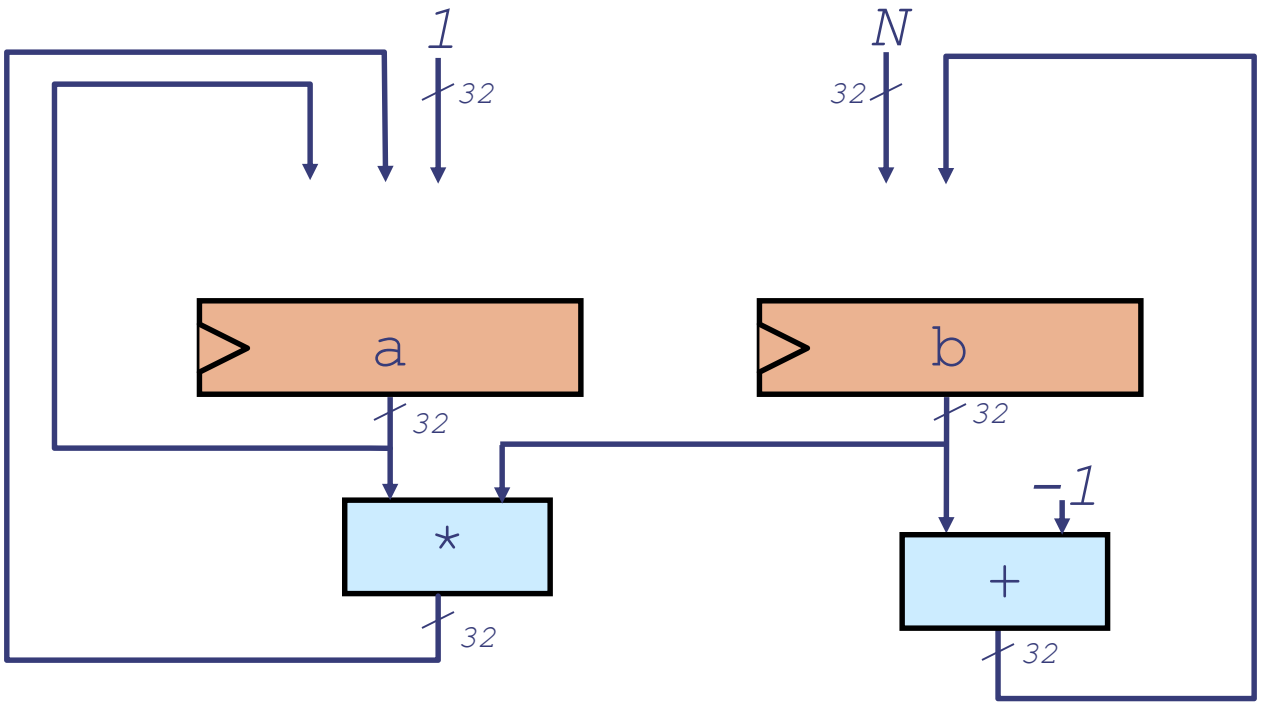

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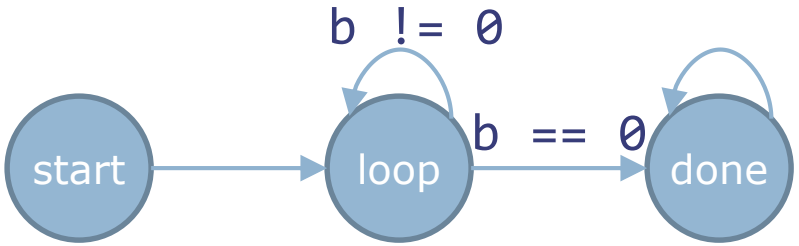


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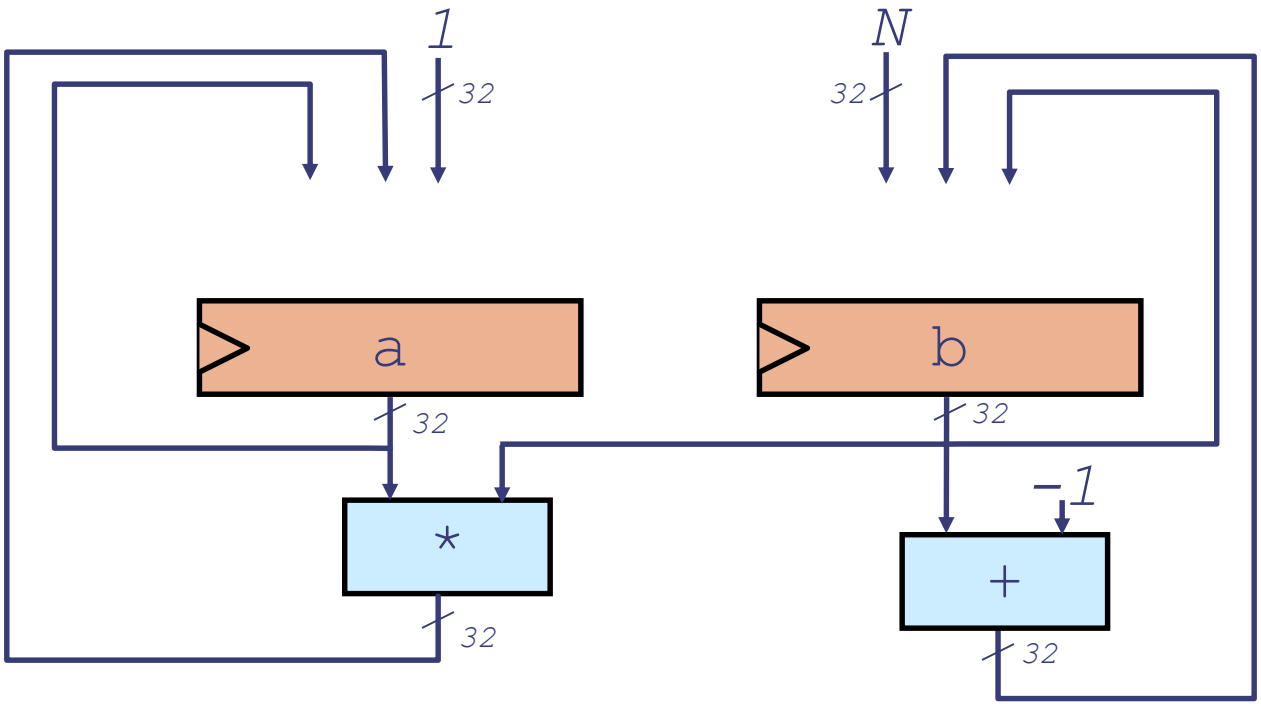

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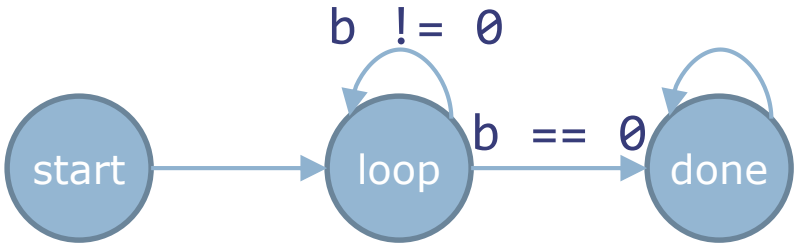


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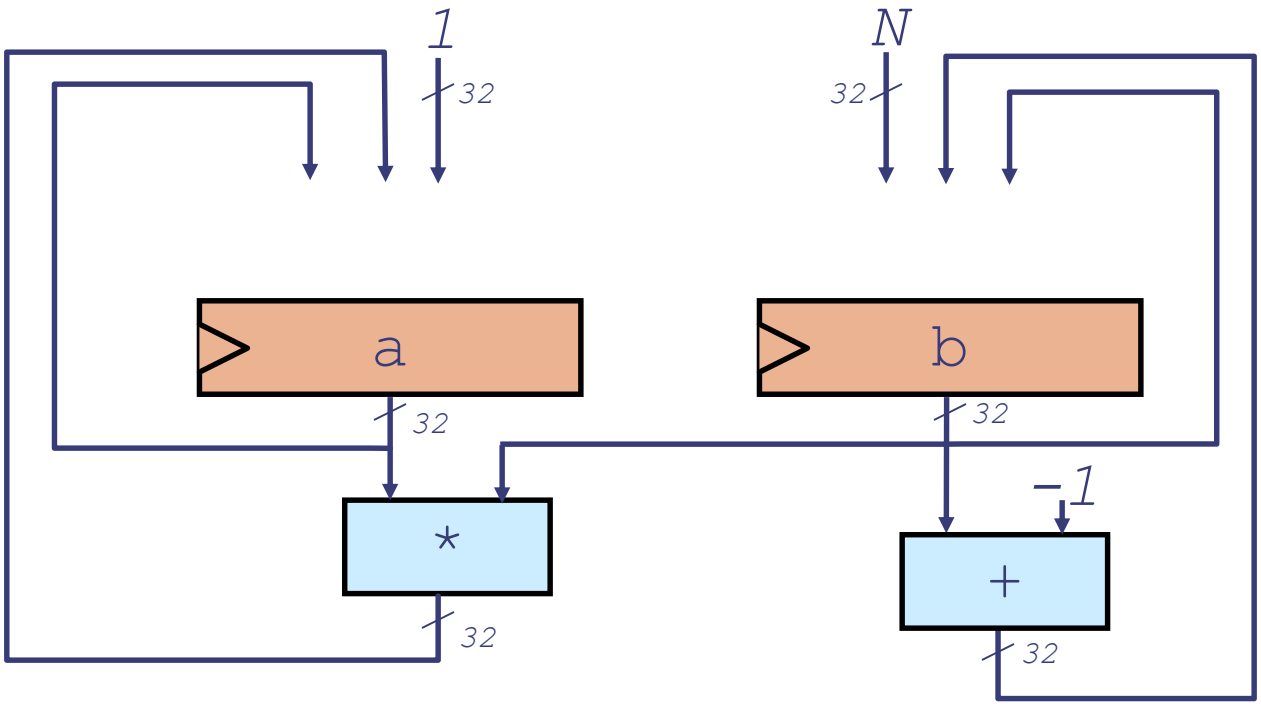

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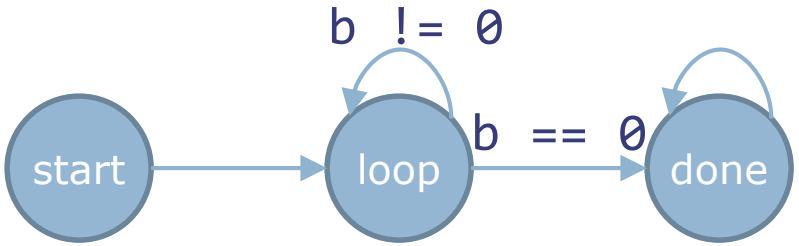


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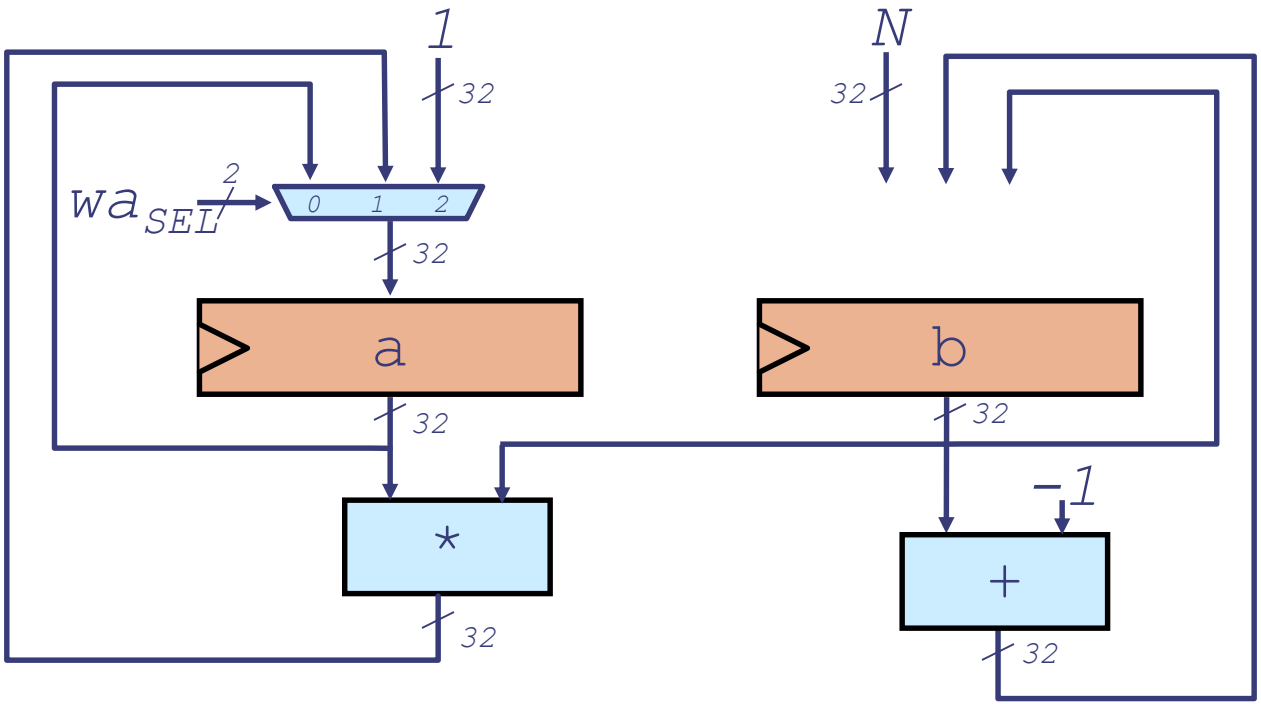

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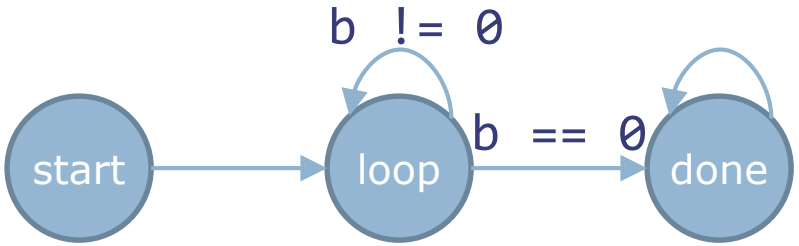


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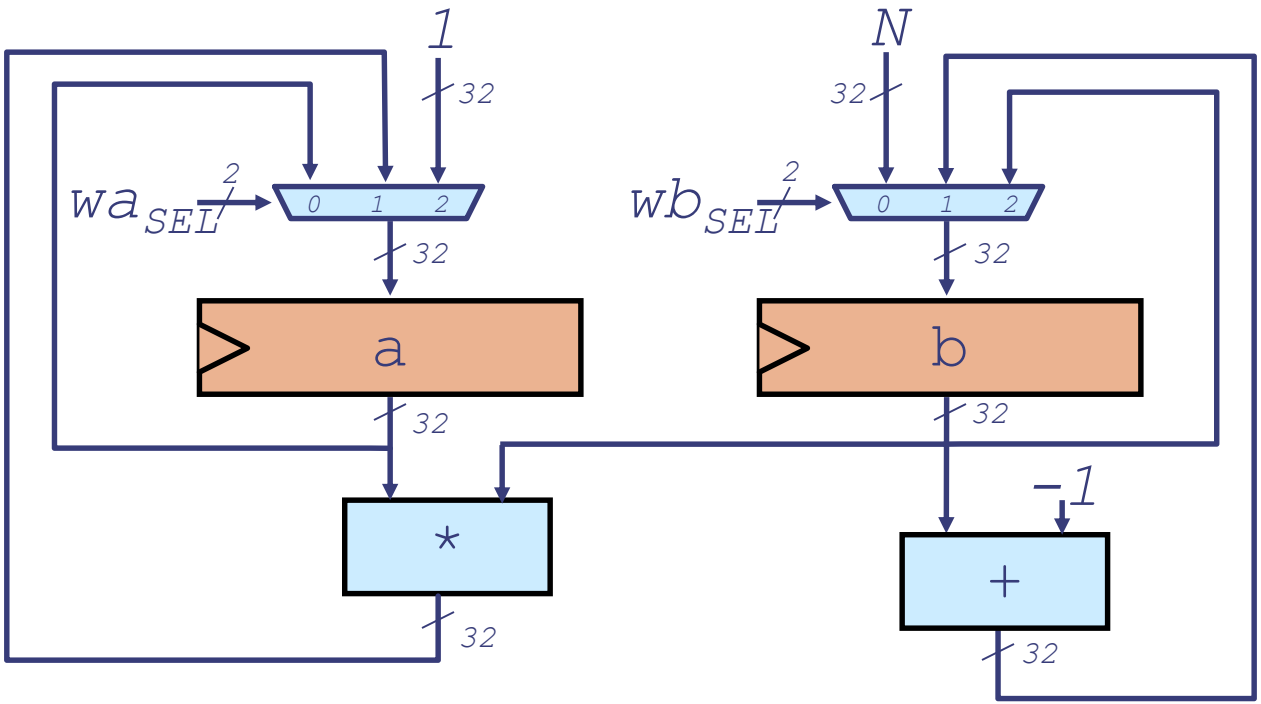
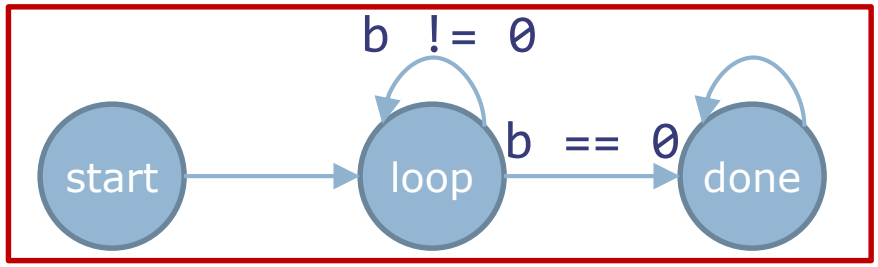


Control FSM for Factorial

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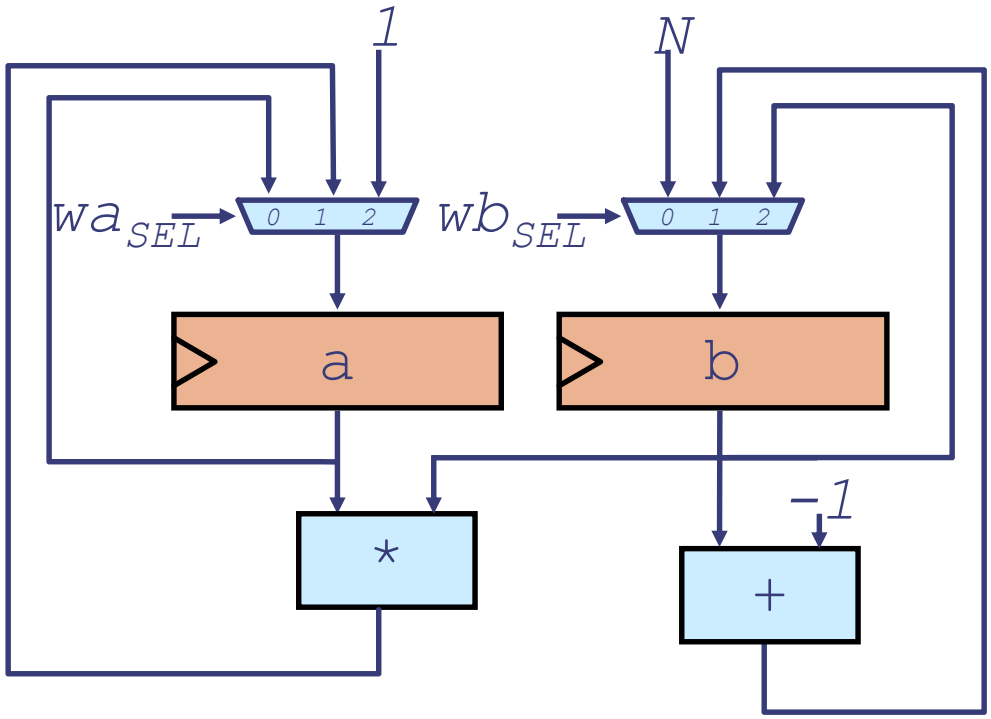

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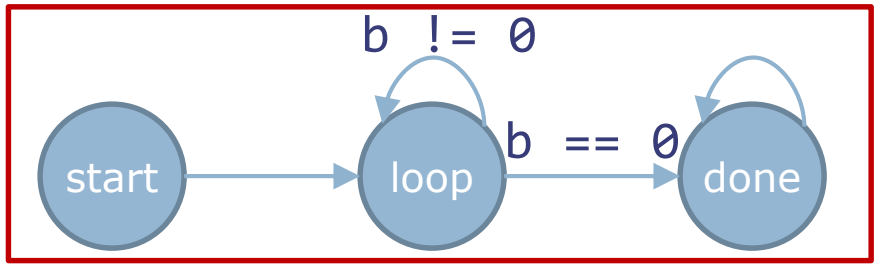


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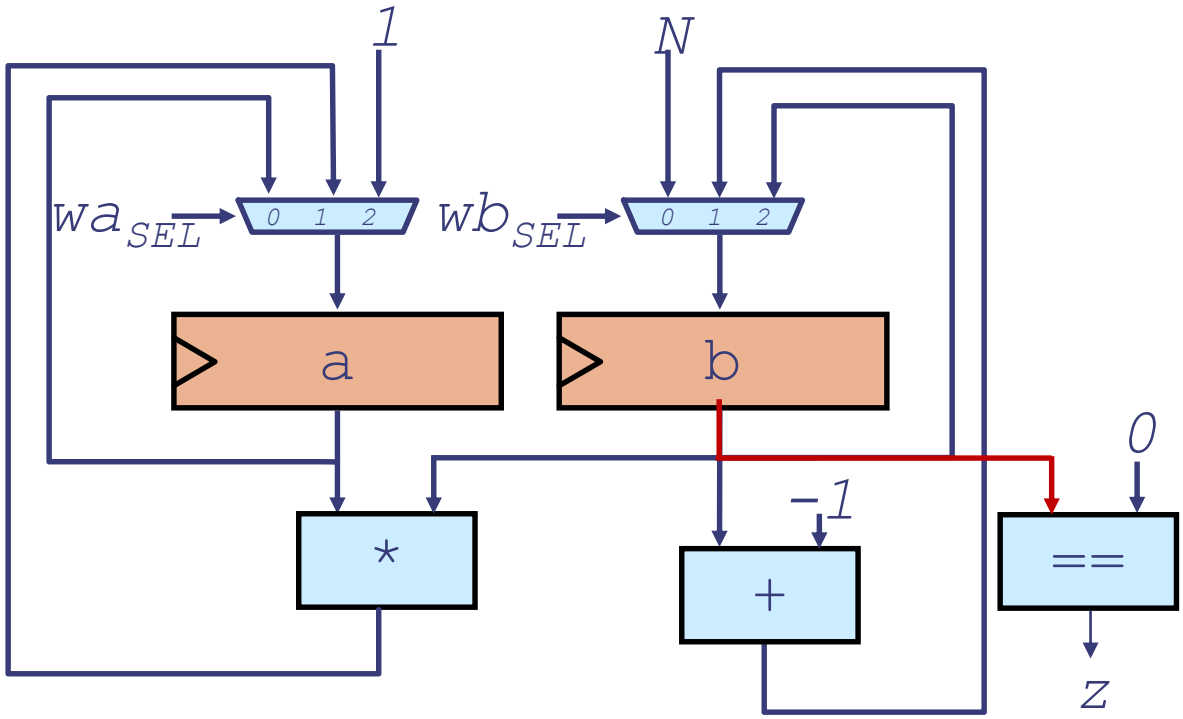

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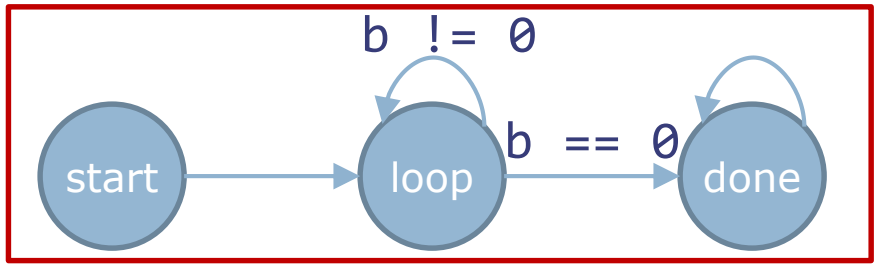


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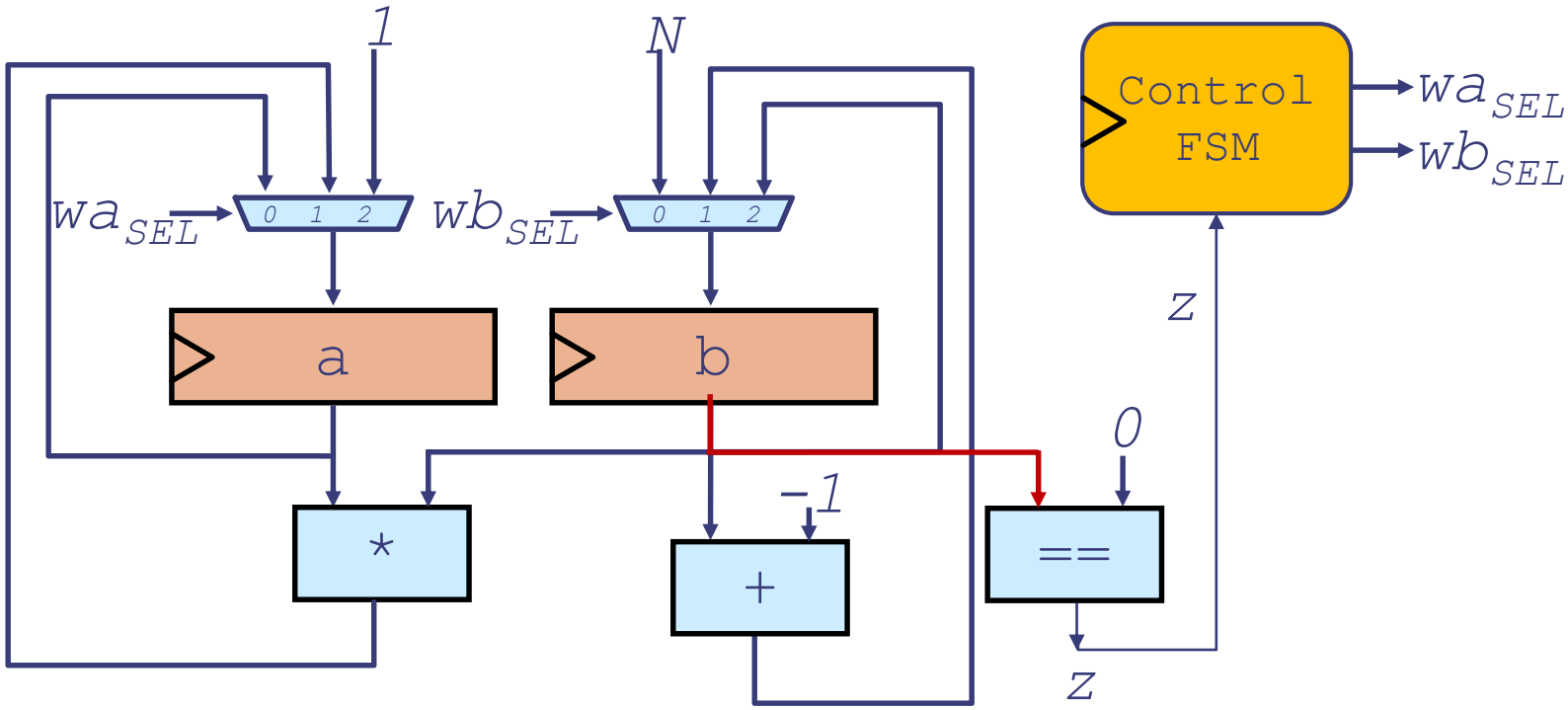

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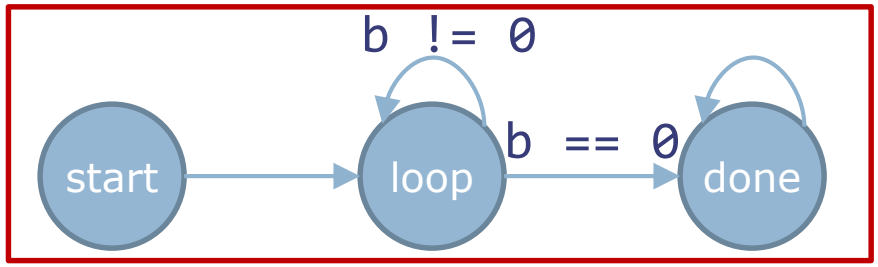


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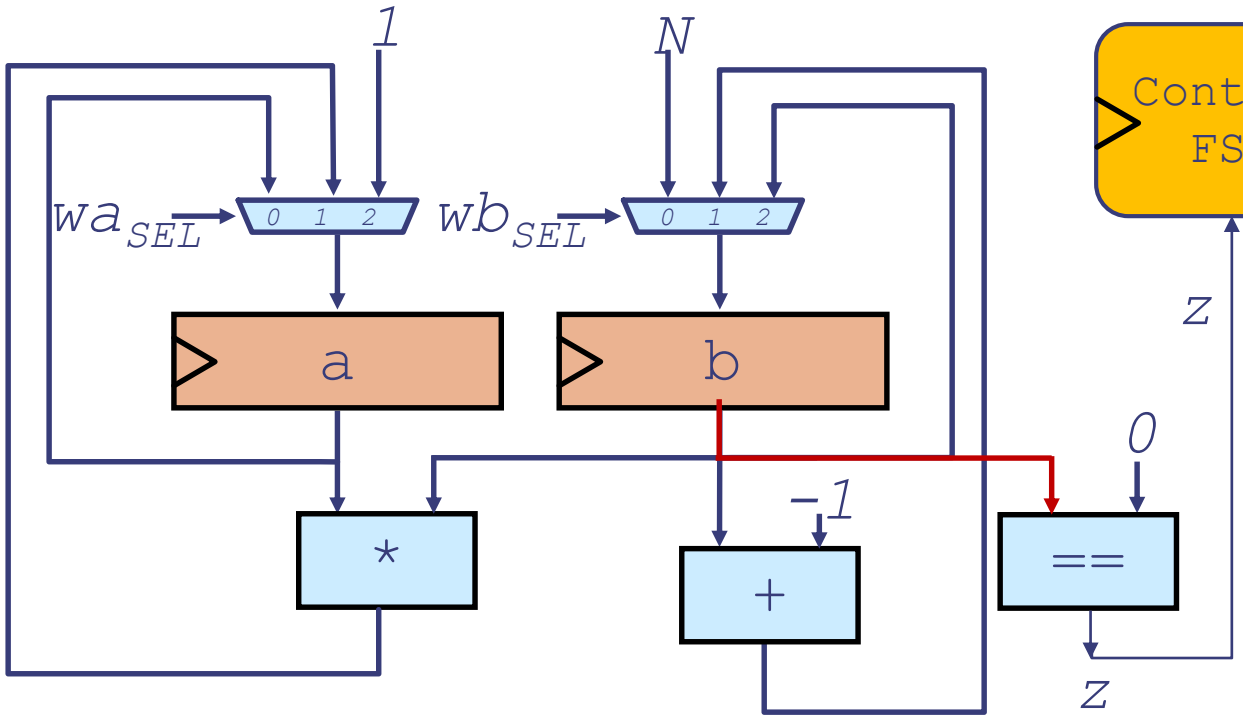
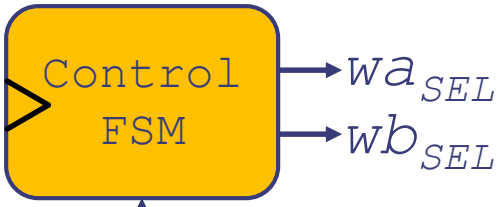




S	z	wa_{SEL}	wb_{SEL}	S′
0	0	2	0	1
0	1	2	0	1
1	0	1	1	1
1	1	1	1	2
2	0	0	2	2
2	1	0	2	2

Programming the Datapath

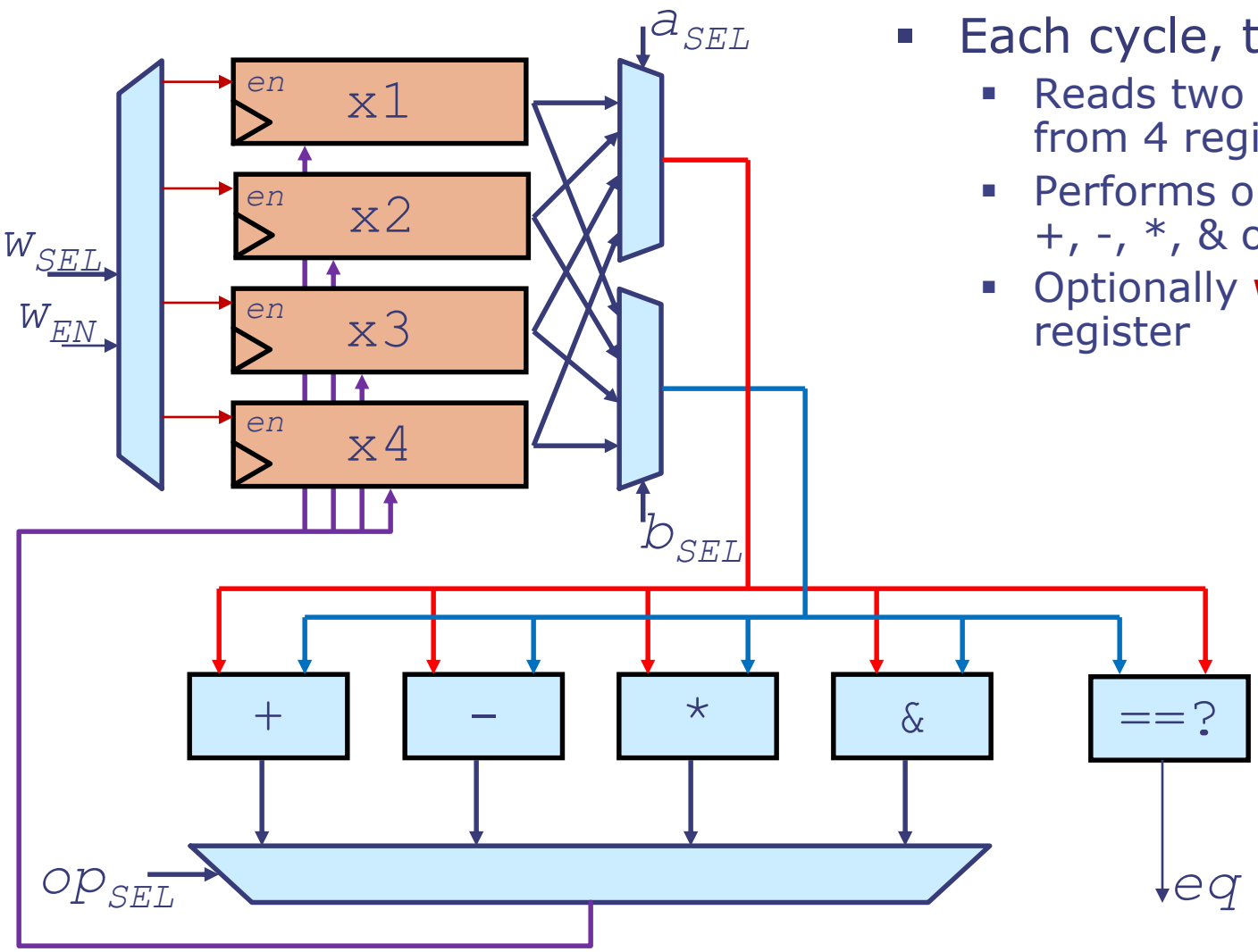
- We can use our factorial datapath and change the control FSM to solve other problems! Examples:
  - Multiplication
  - Squaring

Programming the Datapath

- We can use our factorial datapath and change the control FSM to solve other problems! Examples:
  - Multiplication
  - Squaring

- But very limited problems. Reasons:
  - Limited storage (only two registers!)
  - Limited set of operations, and inputs to those operations
  - Limited inputs to the control FSM

A Simple Programmable Datapath



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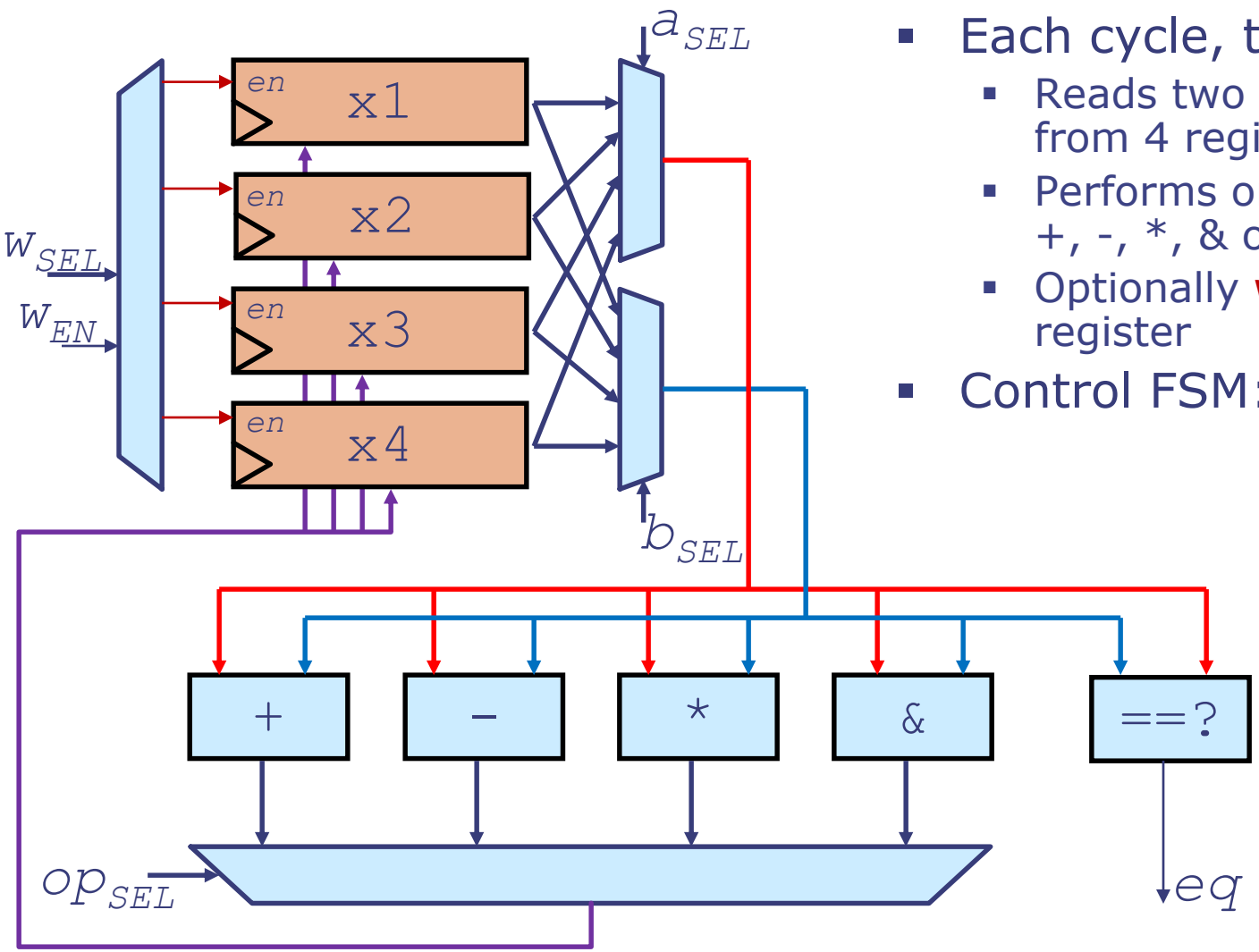

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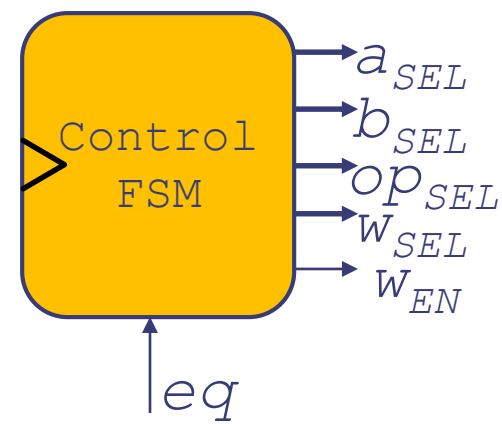
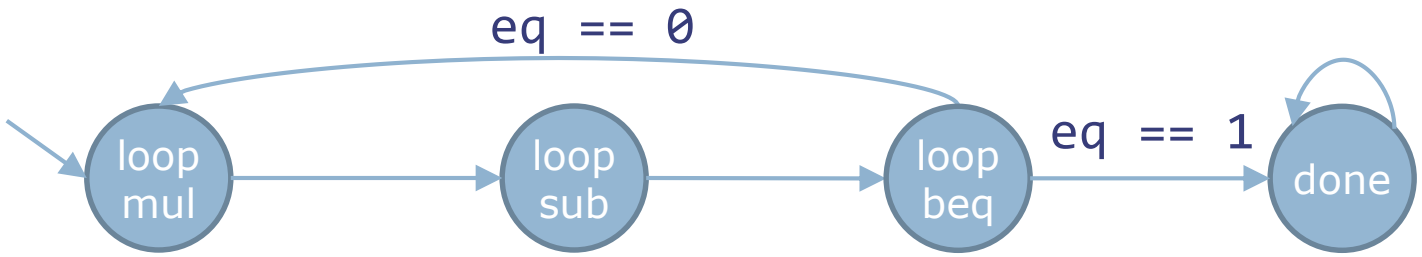


A Control FSM for Factorial

- Assume initial register contents:

```
x1 value = 1
x2 value = N
x3 value = -1
x4 value = 0
```

- Control FSM:



loop mul	loop sub	loop beq	done
asel = x1	asel = x2	asel = x2	asel = X
bsel = x2	bsel = x3	bsel = x4	bsel = X
opsel = 2 (*)	opsel = 0 (+)	opsel = X	opsel = X
wen = 1	wen = 1	wen = 0	wen = 0
wsel = x1	wsel = x2	wsel = X	wsel = X

A Control FSM for Factorial

- Assume initial register contents:

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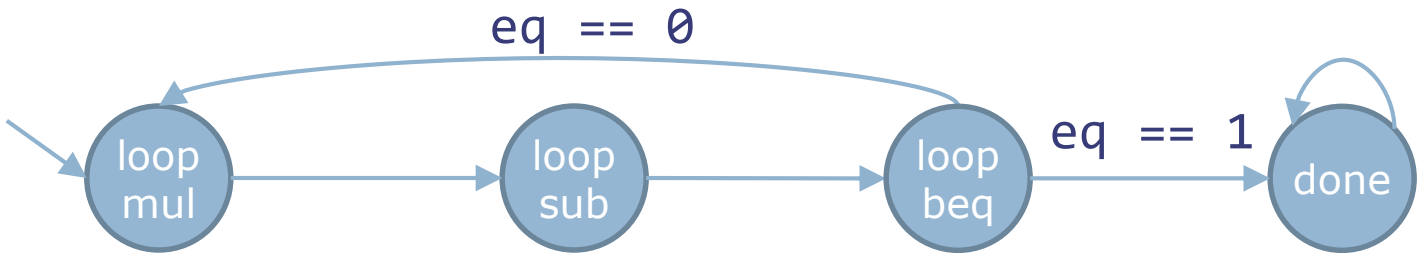

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x1 <= x1 * x2	x2 <= x2 + x3		N! in x1

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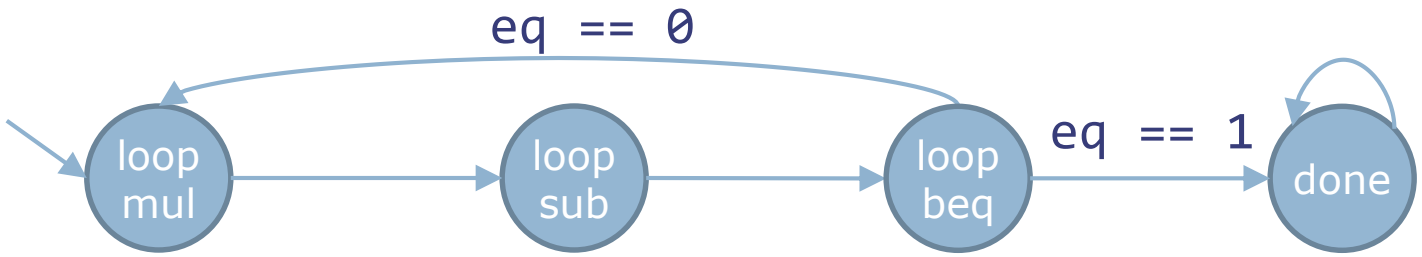

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```
mul x1, x1, x2
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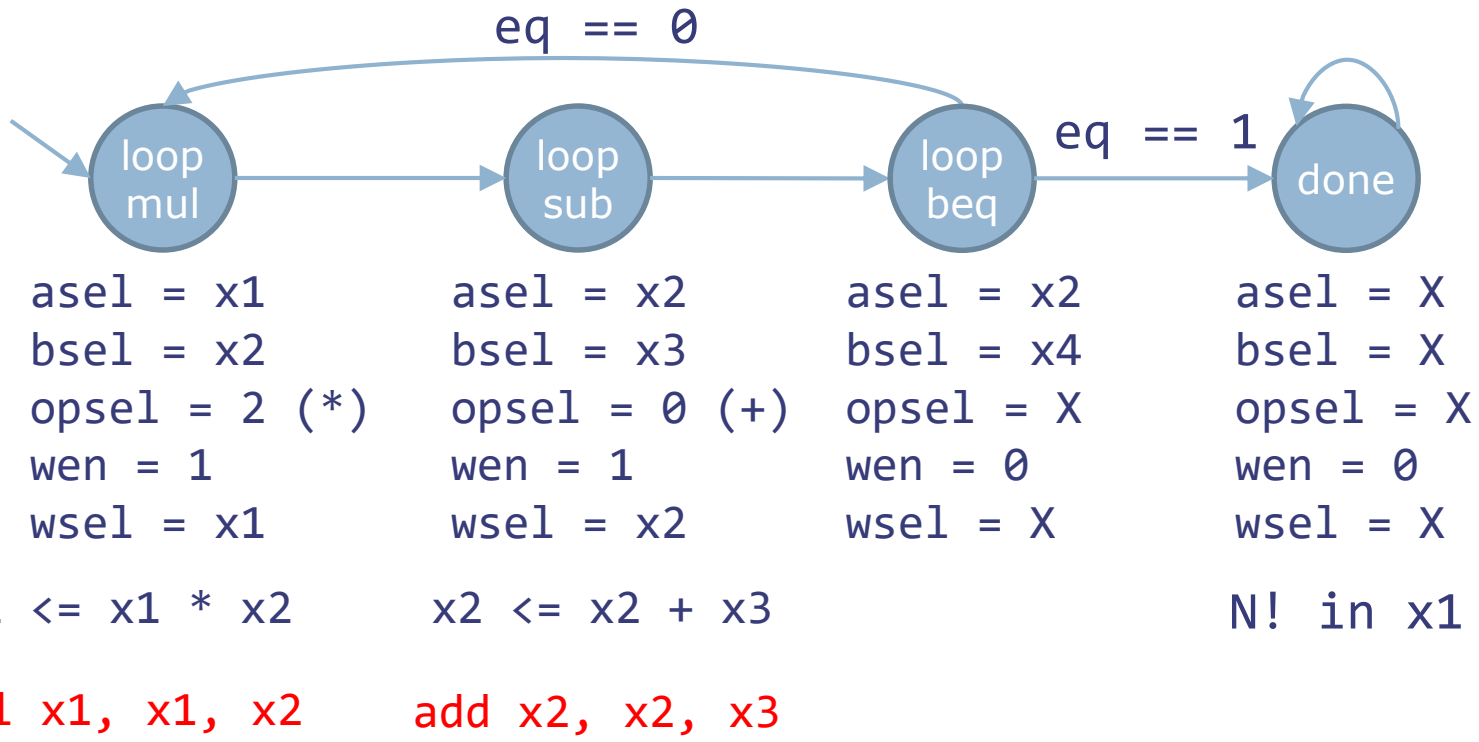

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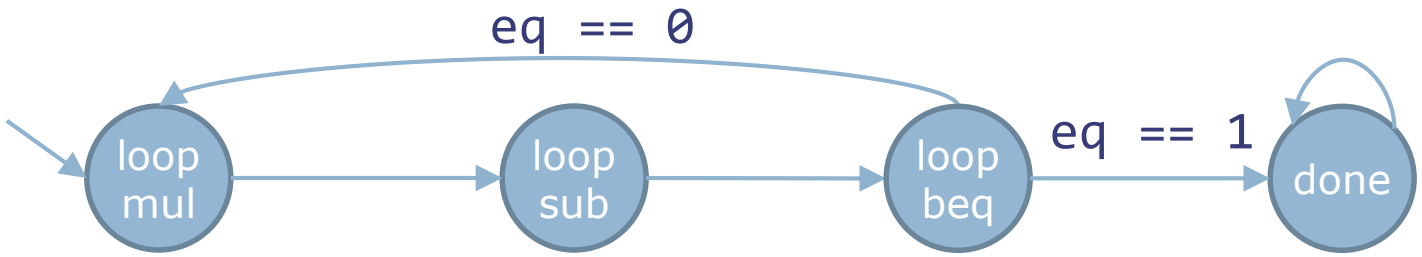

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mul x1, x1, x2	add x2, x2, x3	beq x2, x4, loopmul	

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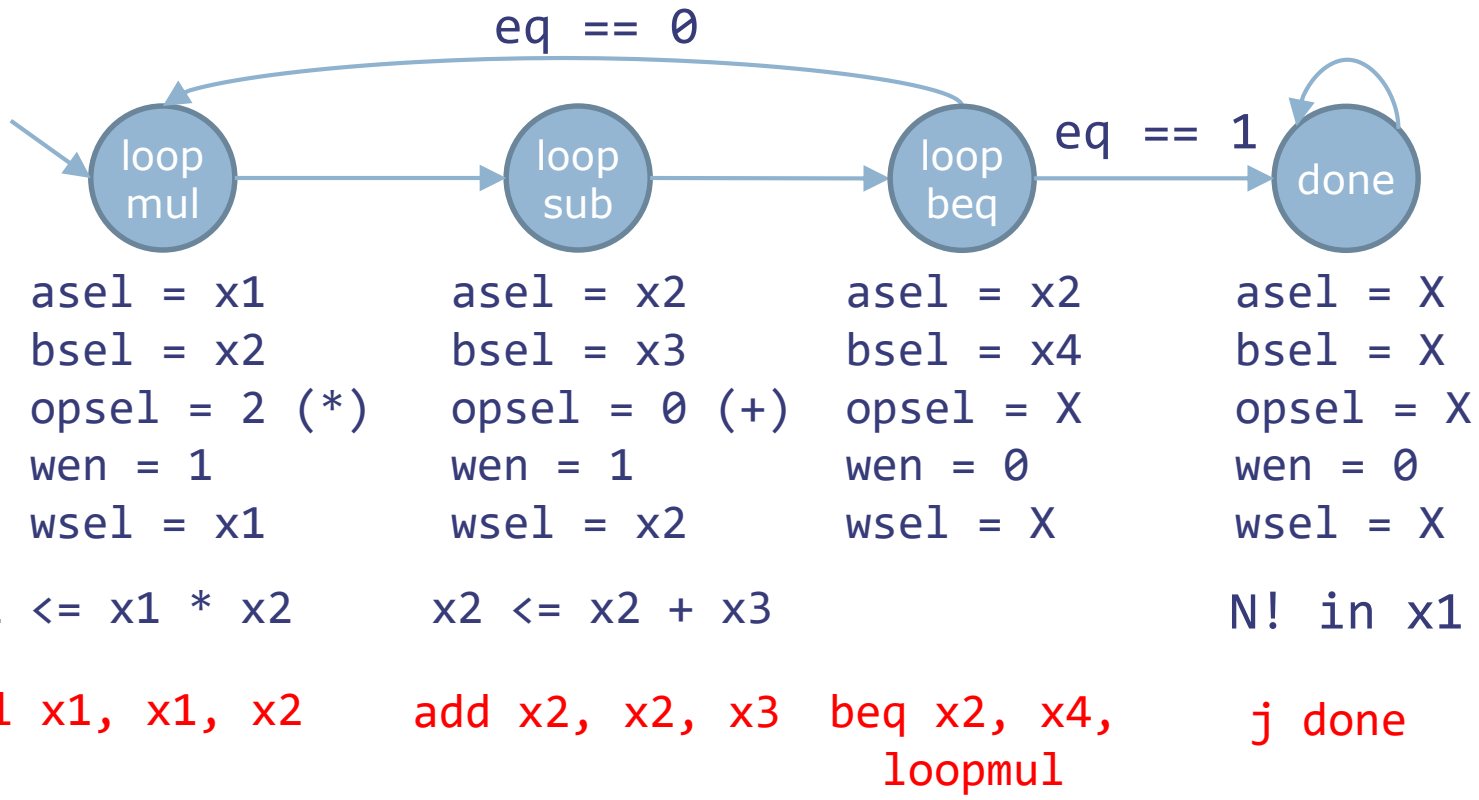

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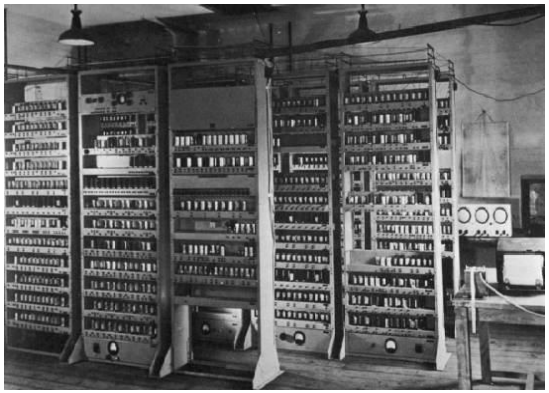
    - Reprogramming it took about 3 weeks



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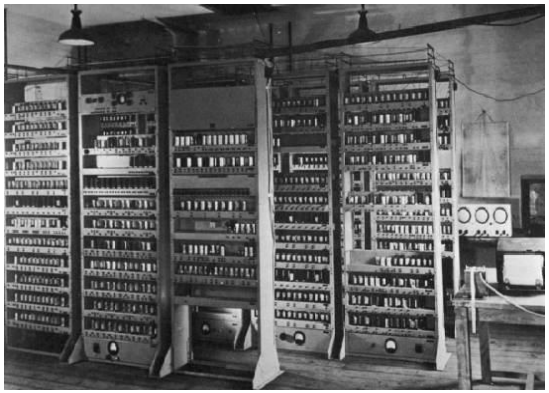

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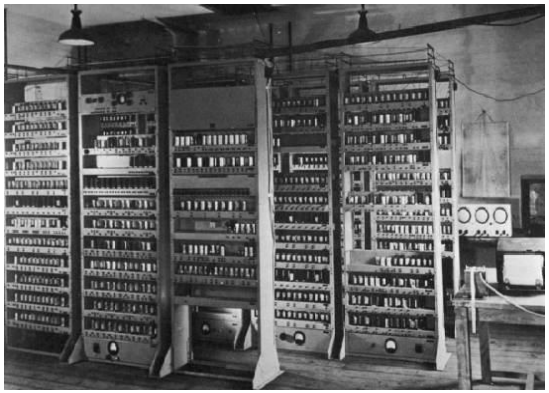

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more on next lecture…

Thank you!

Next lecture: Building a RISC-V processor