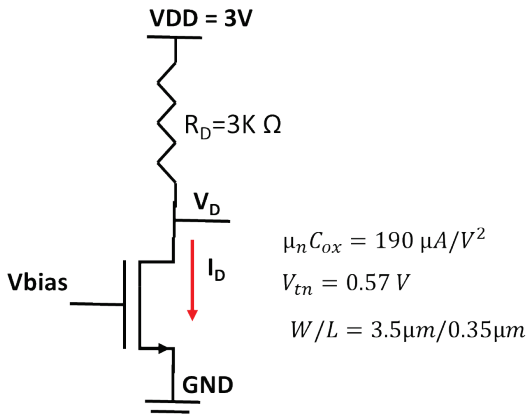
ECSE 4030 Analog IC Design

Class Activity – 1 (review on MOSFET biasing, Regions of Operation)

Drain current (I_D) in the different operating modes for NMOS (NFET) transistor

Off region	$I_D = 0$
Linear Region	$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{tn})V_{DS} - \frac{1}{2}{V_{DS}}^2\right)$ (deep triode) $I_D \approx \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{tn})V_{DS}$
Saturation Region	$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{tn})^2$

Q1: For the circuit below, fill in Table 1



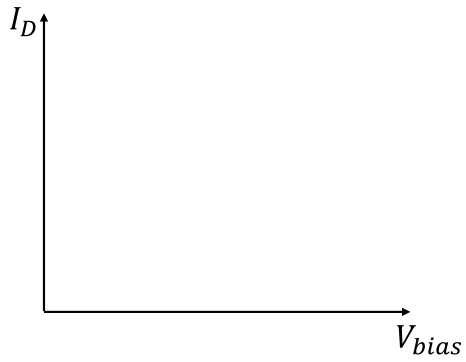
V_{bias}	MOSFET oper. Mode Off/SAT/Linear	I_D(mA)	V_D(V)
0.5V			
1.0V			
1.2V			
1.5V			
2V			
3V			

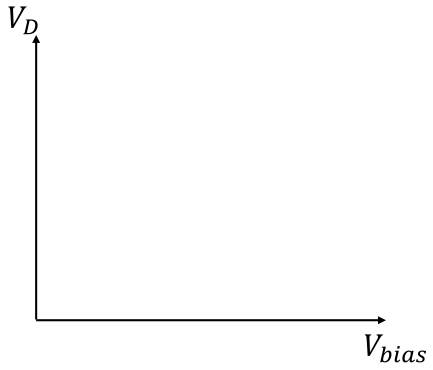
Note that by solving KVL, the total voltage VDD is divided between the voltage drop on the drain resistance and the drop across the drain-source of the transistor such that

$$V_{DD} = V_{DS} + I_D R_D$$

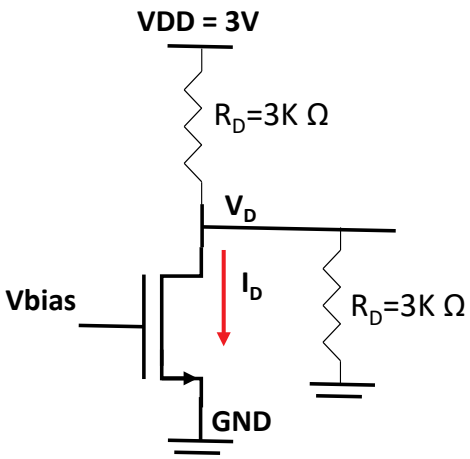
$$V_{DS} = V_{DD} - I_D R_D$$

--After filling the table, Plot I_D versus V_{bias}& plot V_D versus V_{bias}



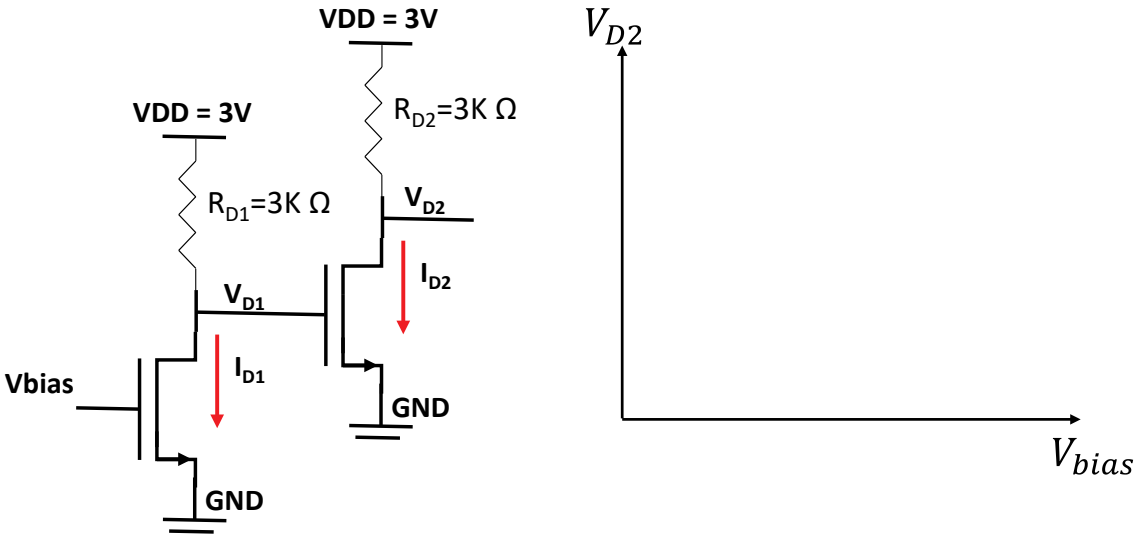


Q2: Repeat Q1 for the circuit shown below.



V_{bias}	MOSFET oper. Mode Off/SAT/Linear	I_D(mA)	V_D(V)
0.5V			
1.0V			
1.2V			
1.5V			
2V			
3V			

Q3: Without doing the math, and based on your answer from the previous two questions, what do you expect the voltage at the drain of the second transistor to look like as a function of the bias voltage of the first transistor?



Q4:

Drain current (I_D) in the different operating modes for PMOS (PFET) transistor

Off region	$I_D = 0$
Linear Region	$I_D = \mu_p C_{ox} \frac{W}{L}\left((V_{SG} - \lvert V_{tp}\rvert)V_{SD} - \frac{1}{2}{V_{SD}}^2\right)$ (deep triode) $I_D \approx \mu_p C_{ox} \frac{W}{L}(V_{SG} - \lvert V_{tp}\rvert)V_{SD}$
Saturation Region	$I_D = \frac{1}{2}\mu_p C_{ox} \frac{W}{L}(V_{SG} - \lvert V_{tp}\rvert)^2$

For the circuit shown in Fig. P4(a), find the voltage at the drain V_D at Vbias =1V? Assume all transistors are in Saturation

If the wire connecting the gate with the drain for transistor M2 is disconnected as shown in Fig. P4(b), can you still find the voltage V_D

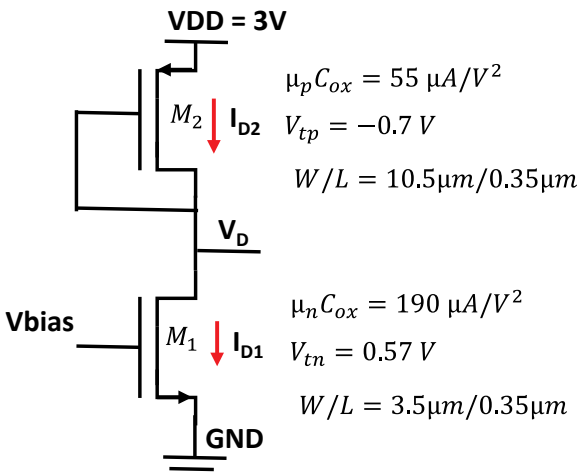


Fig. P4(a)

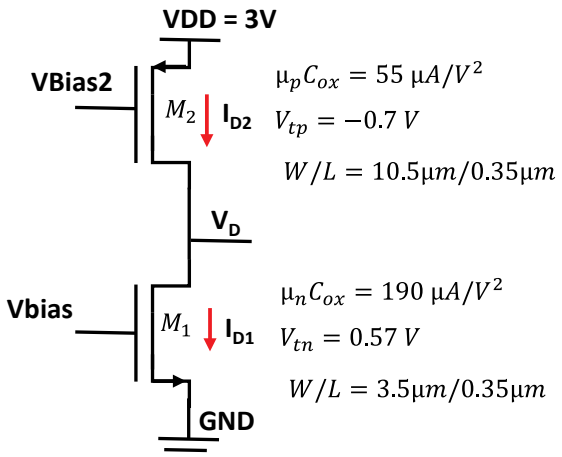


Fig. P4(b)

Q5: Something to think about……

For the circuit shown below, and based on your answer to Q1, Can you guess the value of Vbias2 if Vbias1 = 1V? Assume both NMOS transistors are in the saturation region