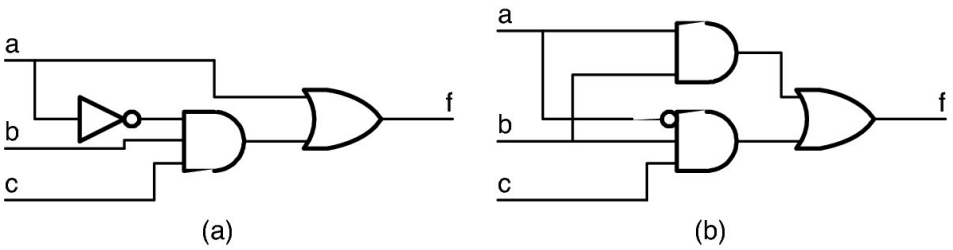
HW3

1. Fix the hazard that may occur in the following figures:



2. Design a combinational circuit with three inputs, x (MSB), y, and z (LSB), and three outputs, A (MSB), B, and C (LSB). When the binary input is 0, 1, or 2, the binary output is three greater than the input (xyz=001 (1) => ABC=100 (4), xyz=010 (2) => ABC=101 (5).). When the binary input is 3, 4, 5, 6, or 7, the binary is two less than the input (xyz=110(6) => ABC=100 (4), xyz=100 (4) => ABC=010(2)).
   (a) Derive the truth table.
   (b) Derive the simplified Boolean expressions for A, B, and C using maps.
   (c) Draw the related logic diagram.

3. Design an excess-3-to-binary decoder using the unused combinations of the code as don't-care conditions.

4. Simplify the following Boolean expressions to a minimum number of literals, and implement with two-level NAND-NAND, NOR-NOR, AND-OR-Invert, and OR-AND-Invert gates, respectively.
   (a) xy'z+xy'z'+xyz',
   (b) (y'z+xw')(xw+y'z).

5. A half adder is a circuit that takes in one-bit binary numbers a and b, and outputs a sum s and a carry out co. The concatenation of xo and s, is the two-bit value that results from adding a and b (e.g. if a=1, b=1, s=0, and co=1).
   (a) Derive the truth table of a half adder.
   (b) Derive the Boolean expression of co and s in the simplest sum-of-product form.
   (c) Find the prime implicants and essential prime implicants of co and s.

6. Use Verilog to simulate the half adder in problem 5.

