

CS 570 HW2 Zhuoling Chen 933341319

1.

a)

	Processor 1	Processor 2	Processor 3	
1	R _A			→ cold miss
2		R _B		→ cold miss
3			R _C	→ cold miss
4	W _A			
5			R _C	→ false sharing miss
6		R _A		→ true sharing miss
7	W _B			
8			R _A	→ true sharing miss
9			R _B	→ hit

Time step 1, 2, 3 \Rightarrow first access to the block

Time step 4: $p1 \xrightarrow{W_A} M$; $p2 = I$; $p3 = I$

Time step 5 \Rightarrow miss but c did not be changed

$p1 = S$, $p2 = I$, $p3 = I \xrightarrow{R_C} S$,

Time step 6 \Rightarrow miss but be changed by P1

$p1 = S$; $p2 = S$; $p3 = S$

Time step 7 \Rightarrow $p1 = S \xrightarrow{W_B} M$; $p2 = I$; $p3 = I$

Time step 8 \Rightarrow miss and change by P1

$p1 = S$, $p2 = I$, $p3 = I \xrightarrow{R_A} S$

b)

False sharing miss will not send the processor new data to cache. Therefore, it can be ignored

c)

	Processor 1	Processor 2	Processor 3
1	R _A		
2		R _B	
3			R _C
4	W _A		
5			R _C
6		R _A	
7	W _B		
8			R _A
9			R _B

$$70 \times 3 + 10 + 70 + 70 + 10 + 70 + 0 = 440$$

↓
Read
from
memory

↓
BusUpgr

↓
Read-
exclusive
by cache

↓
Read-
exclusive
by next level

↓
BusUpgr

↓
Read-
exclusive
by next level

↓
read hit

$$\frac{440 - 70}{440} \times 100\% = 84\%$$

2.

a) home node = requesting node; memory = clean
 Cycle = $50 + 1 = 51$ cycle

Traffic: N/A

b) home node = requesting node; memory = dirty
 Cycle = $50 + 20 + 50 + 100 + 50 + 1 = 271$ cycle

Traffic = $6 + 6 + 32 = 44$ byte

c) home node \neq requestion node; memory = clean
 Cycle = $20 + 50 + 100 + 50 + 1 = 221$ cycle

Traffic = $6 + 6 + 32 = 44$ byte

d) home node \neq requestion node; memory = dirty
 home node = remote node

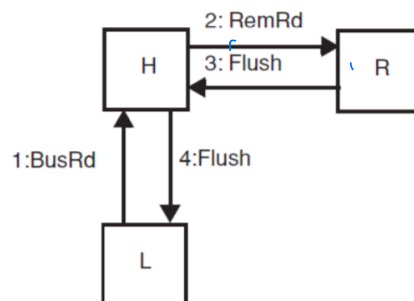
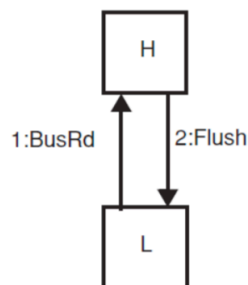
Cycle = $20 + 50 + 100 + 50 + 1 = 221$ cycle

Traffic = $6 + 6 + 32 = 44$ byte.

e) home node \neq requesting node; memory = dirty
 remote node \neq home node

Cycle = $20 + 50 + 20 + 50 + 100 + 50 + 100 + 50 + 1 = 441$

Traffic = $6 + 6 + 6 + 32 + 6 + 32 = 88$



3.

P1	P2	P3
A=1	R1=A	R2=B
	B=1	R3=A

there has 8 conditions total.

if do

↓	P1	A=1
	P2	R1=A=1
	P3	R2=B=1 R3=A=1

In the conclusion, R3 is not be 0. Therefore, 1,1,0 will not be sequentially consistent.

4.

a)

$$\begin{aligned}
 n=1 & \quad (K-1) \times 2 \\
 n=2 & \quad (K-1) \times 2 \times 2 \times K \\
 n=3 & \quad (K-1) \times 2 \times 3 \times K^2
 \end{aligned}$$

$$\Downarrow \\
 2 \times n \times K^{n-1} (K-1)$$

b)

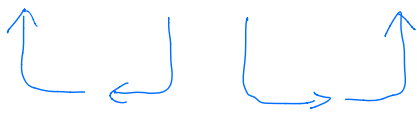
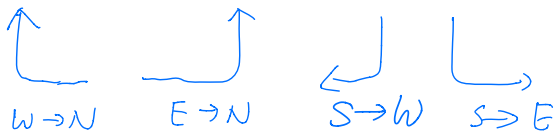
$$\text{bandwidth} = K^{n-1} \quad \text{uni-directional} = 2K^{n-1}$$

c)

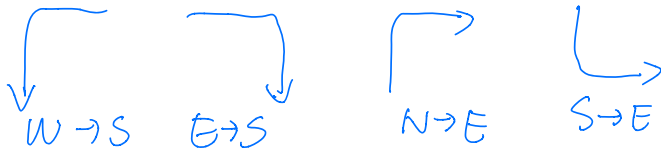
$$\text{max channel load} = \frac{K^{n-1}}{2}$$

5.

a) it is connected but not dead-lock

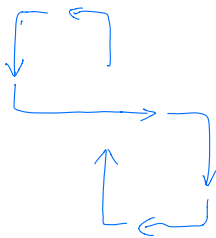
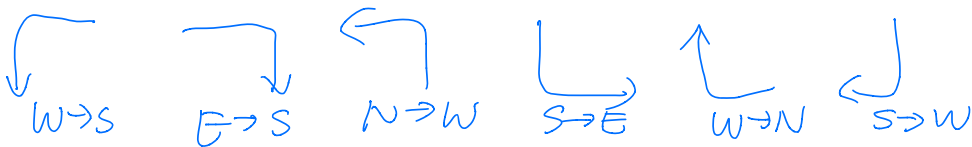


b)



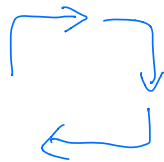
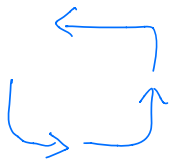
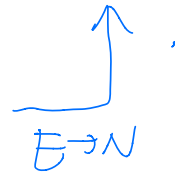
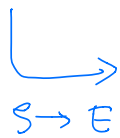
it is not connected and
not dead-lock

c)



it 's not connected and dead-lock

d)



it's connected and
not dead-lock