S32K3_S32M27x Real-Time Drivers AUTOSAR R21-11

Version 6.0.0

17 June 2025 **Release notes**

1 Getting Started

1.1 Package content

This release contains the NXP S32K3_S32M27x Real-Time Drivers Version 6.0.0:

- "eclipse/plugins/<mod>_TS_T40D34M60I0R0" directories - Tresos Plugins, 1 per module.
- "SW32K3_S32M27x_RTD_R21-11_6.0.0_D2506.exe"
- "SW32K3_S32M27x_RTD_R21-11_6.0.0_D2506_ReleaseNotes.pdf" - This file.
- "SW32K3_S32M27x_RTD_R21-11_6.0.0_D2506_SCR.txt"
- "SW32K3_S32M27x_RTD_R21-11_6.0.0_D2506_DesignStudio_updatesite.zip"
- "SW32K3_S32M27x_RTD_R21-11_6.0.0_D2506_SafetyPackage.zip" - contains FMEA reports and Safety Manual.
- "SW32K3_S32M27x_RTD_R21-11_6.0.0_D2506_QualityPackage.zip"
- Various other files: GettingStarted.htm start page and associated images, the license.txt EULA file and the Uninstall.exe utility for removing the RTD installation.

1.2 Installation Design Studio

1.2.1 Bundled in S32 Design Studio

S32 RTD is delivered bundled in the S32 Design Studio. In this case, it's already configured and ready to use. New S32DS project wizard and New S32DS project from Example can be used to create S32 RTD based projects.

1.2.2 Delivered as an extension for S32 Design Studio

S32 RTD is delivered as an Update Site for S32 Design Studio "*S32 Design Studio 3.6.1*". In this case, it must be installed by opening Help -> S32 Design Studio Extensions and Updates -> Add Update Sites and selecting the archive file containing the S32 RTD software and then check the S32 RTD software package to be installed and continue the installation process. After it is installed, New S32DS project wizard and New S32DS project from Example can be used to create S32 RTD based projects.

1.3 Installation EB Tresos

Follow the installer steps. By default the installer will create a link between the installation target directory and a selected EB Tresos installation. If you choose not to create a link, you can later create one manually or you can copy all "<mod>_TS_T40D34M60I0R0" directories and .JAR files to the "<Tresos Install Path>\plugins" directory.

2 Release Specifics

The S32K3_S32M27x Real-Time Drivers Version 6.0.0 is AUTOSAR R21-11 compliant. The AUTOSAR Configuration ARXML specification takes precedence over AUTOSAR SWS PDF Specifications if there are discrepancies.

The S32K3 Real-Time Drivers Version 6.0.0 can be used also in non-AUTOSAR environment, as a collection of peripheral drivers designed to simplify and accelerate application development on NXP microcontrollers.

2.1 Release Details

This is the NXP S32K3_S32M27x Real-Time Drivers Release Version 6.0.0, qualified as RFP release in terms of quality, supporting AUTOSAR R21-11 and non AUTOSAR, with functionalities and tests on S32K358(Rev 1.1), S32K396(cut 1.1), S32K311, S32K342, S32K312, S32K344, S32K388, S32K389 and S32M276 (cut 2.0).

This release contains a deviation from AUTOSAR recommended version check inside source files for more details.

This release has RFP qualification for all drivers.

RFP qualified drivers can be used in production.

This release was tested using:

- Silicon P32K358GHMJBS 1P14E CTAA2336A (Rev1.1).
- Silicon P32K396EHMJBS 1P40E QAA2331A (E5) (cut 1.1).
- Silicon P32K311HVS 0P98C CTZA2242B (E5).
- Silicon P32K344EHVMMS 1P55A CTSB2128B
- Silicon P32K312NHVPBS 0P09C CTZM2132B.
- Silicon P32K342EHVPBE 0P97C CTZM2139A.
- Silicon P32K388HMS 0P39J CTAA2332D (E5).
- Silicon P32K389HHMJGS 0P23N CTAA2506A.
- Silicon P32M276CC MKHS 0P69K 20230904 (E5-B0) (Use for CANTRCV).
- Silicon P32M276LC MKHS 0P69K 20230904 (E5-B0) (Use for LINTRCV).
- Mini Module XS32K3X8CVB-Q289 PCB 53108 RevX3 SCH RevA1.
- Mini Module XS32K396-BGA-DC PCB 54614 RevX1 SCH RevA.
- Mini Module XS32K3X2CVB-Q100 PCB 48306 RevX1 SCH RevA.
- Mini Module XS32K3XXCVB-Q257 PCB 47020 RevA1 SCH RevX2.
- Mini Module XS32K3X2CVB-Q172 PCB 48307 RevX1 SCH RevA.
- Mother Board X-S32K2XX-MB PCB 31431 RevX3 SCH RevB.
- Mother Board X-S32K3XXX-MB PCB 47386 RevA SCH RevA.
- Mother Board X-S32X-MB version A PCB 54935 RevX1 SCH RevA.
- EVB S32K3X4EVB-Q257 47827 PCB RevX1 SCH RevA.
- EVB S32K3X4EVB-T172 PCB 53148 RevX5 SCH RevB.
- EVB S32K312EVB-Q172 PCB 50892 RevA SCH RevB.
- EVB S32K3X8EVB-Q289 PCB 54870 RevX2 SCH RevB2
- EVB S32K388EVB-Q289 PCB 88925 RevX1 SCH RevA
- CVB XS32M2XXCVB-Q064 PCB 53099 RevX1 SCH RevA.
- CVB XS32K388CVB-Q289 PCB RevA SCH RevX3.
- CVB XS32K389CVB-Q437
- EVB S32K358 HyperRAM internal validation board (for Mem_Exfls only).
- HSE frimware release: S32K344: hse_fw_s32k344 0.2.55.0 (RFP).

- HSE frimware release: S32K312: hse_fw_s32k312 0.2.55.0 (RFP).
- HSE frimware release: S32K342: hse_fw_s32k342 0.2.55.0 (RFP).
- HSE frimware release: S32K358: hse_fw_s32k358_0.2.55.0 (RFP).
- HSE frimware release: S32K311: hse_fw_sS2k311_0.2.55.0 (RFP).
- HSE frimware release: S32K396: hsse_fw_s32k396_0.2.50.0 (RFP).
- HSE frimware release: S32M276: hse_fw_s32m276_0.2.55.0 (RFP).
- HSE frimware release: S32K388: hse_fw_s32k388_0.2.49.0 (RFP).
- HSE frimware release: S32K389: hse_fw_s32k389_0.2.70.0 (RFP).
- VDK Simulation Version: S32K388: R5.1.1 (Smoke test for all drivers except AE, Zipwire, CanTrcv, LinTrcv, Dpga, Gdu, Messaging and Mem_eep).

In all source files, Software Version values are checked (major, minor, patch). AUTOSAR release or SWS versions are not checked during preprocessing/template generation.

The correct SWS versions are exported by each module.

The functions contained in the Dem, Det, EcuC, EcuM, Rte, OS and interface plugins are sample stub functions.

These functions should be replaced by the user developed code during integration.

The Resource module is needed to select the MCU derivative.

The derivatives supported can be found in the Resource module definition file, parameter 'ResourceSubderivative'.

The following limitations are present in this release:

Known limitation:

- Due to low SRAM memory space on S32K310, S32K311, S32K312, S32K322, S32K341, S32K342, S32M274 and S32M276 derivatives, users should select FLASH profile to create new project on S32 Design Studio.
- On S32K388, the Mem_ExFls driver with Qspi could not be tested due to hardware limitations and on S32K358 the Hyperflash memory sometimes data read is incorrect.
- Mcl driver has the following limitation when using variants:
  - EB and S32DS HL - Driver logic channels/instances must contain "VS_x" at the end of the name,e.g. DMA_LOGIC_CH_6_VS_0, MOTOR0_LOGIC_INPUT_0_VS_0, LCU_LOGIC_INSTANCE_0_VS_0, MOTOR0_LOGIC_INPUT_0_VS_0
  - S32DS Ip layer - Driver logic channels/instances must contain "SA_" as a prefix, e.g. SA_DMA_LOGIC_CH_1, SA_MOTOR0_LOGIC_INPUT_0.
  Note: This limitation was introduced due to implementation of requirement CPT_RTD_00543 (MR 200).

Known issue with IAR compiler, all RTD drivers:

- Warning regarding stack usage is thrown for reference implementations of core exceptions in startup files when drivers are compiled with IAR. These functions are provided as reference code and can be replace/ modified by the application.
- Usage of IAR compiler option "-enable_stack_usage " will issue warnings regarding uncalled functions (eg : interrupt handlers). This should be disregarded.
- IAR cannot analyze stack usage for function in .s file and the function with indirect call(function pointer).

Known issue with DIAB compiler, all RTD drivers:

- These are the derivatives not supported for Diab: S32K342, S32K341, S32K322, S32K396, S32K311, S32M276, S32K389 and their sub-derivatives (S32K356, S32K394, S32K376, S32K374, S32K366, S32K310, S32M274)

Known issue with GCC compiler, all RTD drivers:

- Warning regarding enum size is thrown by the linker due to usage of "-fno-short-enums" option: "use of enum values across objects may fail". The drivers do not use any library enum types - no functional impact.

Known issue for PE Micro debug plugins in Design Studio:

- Debugging an application in RAM might fail if another application is present in target flash (debug communication lost during startup, MCU boots the application in flash). Workaround proposed: erase flash before loading an application in RAM; this can be done with the following command launched in the PE for example GDB Server console: "pegdbserver_console.exe -device=NXP_S32K3xx_S32K344 -programmingtype=3 -runafterprogramming=0 -interface=USBMULTILINK -startserver -singlesession -quitafterprogramming -flashobjectfile=path_to_a_srec_or_elf_file".

The following limitations are present in this release, beside the ones presented in Drivers Manuals:

- During this SW product development, the achieved code coverage is between 80.18% min and 100% max, as it can be seen in the individual Code Coverage Summary reports. Nevertheless, the whole code went through a diligently inspection-based review.
- Certain components—Adc, Gpt, Port, MemAcc, Pwm, I2C, Mem_ExFls, Mem_InFls, Rm, I2s, Sent, Platform, Spi, Fee,Eth, Zipwire, Uart, Can, Lin, CanTrcv, LinTrcv and Mcu—include functions with a code coverage index below 80%. For detailed metrics, please refer to the LDRA_coverage_summary reports provided for each component and included in the Quality Pack.
- Certain components—Gpt, Sent, Pwm, Mem_ExFls, Mem_InFls, Rm, Mcu, Eth, Zipwire,Can, Lin, LinTrcv and I2s —include a number of functions currently have 0% code coverage. A comprehensive list of these functions is available in the LDRA_coverage_summary reports provided for each component and included in the Quality Pack.

RTD Header Files for main derivatives reference

Table 1. RTD Header Files for main derivatives reference

Derivatives	RTD Header files
S32K344	S32K3 Reference Manual Rev. 3, 10/2021
S32K324	S32K3 Reference Manual Rev. 3, 10/2021
S32K314	S32K3 Reference Manual Rev. 3, 10/2021
S32K312	S32K3 Reference Manual Rev. 4, 04/2022
S32K311	S32K3 Reference Manual Rev. 7, 05/2023
S32K341	S32K3xx Reference Manual Rev.5, 09/2022
S32K342	S32K3xx Reference Manual Rev.5, 09/2022
S32K322	S32K3xx Reference Manual Rev.5, 09/2022
S32K358	S32K3xx Reference Manual Rev. 8_Update, 11/2024
S32K388	S32K3 Reference Manual Rev. 9, 08/2024
S32K389	S32K3xx Reference Manual Rev. 10, 04/2025
S32K39, S32K37, S32K36	S32K39,S32K37 and S32K36 Reference Manual Rev.4, 11/2024
S32M276	S32M27x Reference Manual, Rev.4, 09/2024

Note: The header file of sub-derivatives use header file of main derivatives

2.2 Used Documentation

This release was developed and tested based on the following documents:

Table 2. Reference Manuals

Document Title	Version and Date
S32K3xx Reference Manual	Rev.9, 07/2024
S32K3xx Data Sheet	Rev. 10, 07/2024
S32M27x Reference Manual	Rev.5, 02/2025
S32M2xx Data Sheet	Rev. 8 — 02/2025
S32K39, S32K37 and S32K36 Reference Manual	Rev. 4, 11/2024
S32K39 and S32K37 Data Sheet	Rev.4 — 06/2024

Table 3. Implemented Errata

Document Title	Maskset	Date
S32K358 Mask Set Errata for Mask	1P14E	Rev. 4, 6/2024
S32K311 Mask Set Errata	0P98C	Rev. 11/ January/2024, 1/2024
S32K396 Mask Set Errata for Mask	0P40E	Rev. FEB2024, 2/2024
S32K396 Mask Set Errata for Mask	1P40E	Rev. MAR2024, 3/2024
S32K312 Mask Set Errata for Mask	0P09C	Rev. 14/Dec/2023, 12/2023
S32K342 Mask Set Errata for Mask	0P97C	Rev. 14, 12/2023
S32K344 Mask Set Errata for Mask	0P55A/1P55A	Rev. 12/Dec/2023, 12/2023
S32K388 Mask Set Errata for Mask	0P39J/0P24N	Rev. 1, 7/2024
S32M276 Mask Set Errata for Mask	P98C+P69K	Rev. 1, 8/2024
S32K389 Mask Set Errata for Mask	mask_id	Rev. 1.1 — 18 September 2024

2.3 Supported Derivatives

The software described in this document is intended to be used with the following microcontroller devices from NXP:

- s32k310_hdqfp100
- s32k310_lqfp48
- s32k311_hdqfp100 / MWCT2015S_hdqfp100
- s32k311_lqfp48
- s32k312_hdqfp100 / MWCT2016S_hdqfp100
- s32k312_lqfp100
- s32k312_hdqfp172 / MWCT2016S_hdqfp172
- s32k314_hdqfp172
- s32k314_mapbga257

- s32k322_hdqfp100 / MWCT2D16S_hdqfp100
- s32k322_hdqfp172 / MWCT2D16S_hdqfp172
- s32k324_hdqfp172 / MWCT2D17S_hdqfp172
- s32k324_mapbga257
- s32k341_hdqfp100
- s32k341_hdqfp172
- s32k342_hdqfp100
- s32k342_hdqfp172
- s32k344_hdqfp172
- s32k344_mapbga257
- s32k394_mapbga289
- s32k394_lqfp176
- s32k396_mapbga289
- s32k396_lqfp176
- s32k374_mapbga289
- s32k374_lqfp176
- s32k376_mapbga289
- s32k376_lqfp176
- s32k364_mapbga289
- s32k364_lqfp176
- s32k366_mapbga289
- s32k366_lqfp176
- s32k358_hdqfp172
- s32k358_mapbga289
- s32k356_hdqfp172
- s32k356_mapbga289
- s32k328_hdqfp172
- s32k328_mapbga289
- s32k338_hdqfp172
- s32k338_mapbga289
- s32k348_hdqfp172
- s32k348_mapbga289
- s32m274_lqfp64
- s32m276_lqfp64
- s32k388_mapbga289
- s32k389_mapbga437

The mapping between MWCT2xxxS parts and S32K3XX is showed in the table below:

Table 4. Derivatives mapping

MWCT2xxxS derivative	S32K3 derivative
MWCT2D17S_MQFP172	S32K324_MQFP172
MWCT2D16S_MQFP100	S32K322_MQFP100
MWCT2D16S_MQFP172	S32K322_MQFP172
MWCT2016S_MQFP172	S32K312_MQFP172
MWCT2016S_MQFP100	S32K312_MQFP100
MWCT2015S_MQFP100	S32K311_MQFP100

Note: MWCT part numbers contain NXP confidential IP for Qi Wireless Power and they tested with:

- P32K344EHVMMS 1P55A CTSB2128B (and in S32K324 configuration).
- P32K312NHVPBS 0P09C CTZM2132B.
- P32K311HVS 0P98C CTZA2242B.

2.4 Modules Configuration

2.4.1 EB Tresos

Modules configurations were developed and tested using the Tresos Configuration Tool version "*EB Tresos Studio 29.0.0 b220329-0119*"

Configuration definition files were developed according to AUTOSAR R21-11, AUTOSAR_EcucParamDef.arxml

A folder named "<mod>_TS_TtDdMmIiRr" exists for each delivered module (<mod>). It is called a Tresos plugin for the module. A plugin contains the AUTOSAR module definition file (epd), the Tresos Xpath Data Model module definition file (xdm), the module user and integration manuals, the module configuration generation template source files, and the module driver static source files. Additional necessary Tresos specific tooling files are also included.

Plugin Encoding: <mod>_TS_TtDdMmIiRr

Important change related to the plugin notation:
- "m" = coding major and minor version number, can contain 1 or more digits
- "i" = patch number.
The major version number will be left out, if it is "0", in this case "m" contains 1 digit only, otherwise it contains 2 digits

For this release:

- t=40, CortexM Architecture
- d=34, S32K3XX (derivative)
- m=60, Release major and minor version
- i=0, Release patch version
- r=0, Reserved

2.4.2 S32 Design Studio

Configuration components were developped using "*S32 Design Studio 3.6.1*".

The components are split in three tools inside S32 Design Studio: Pins Tool, Clocks Tool, Peripherals tool which enable the generation of configuration structures to be used by both Autosar and low-level drivers.

2.5 Support and Driver Plugins Delivered

Table 5. Support and Driver Plugins Delivered

Plugin	Low level interface	SW Version	Description
ADC	Bctu_Ip, Adc_Sar_Ip, Sdadc_Ip	sw version 6.0.0	Driver, Analog to Digital Conversion
BASENXP	N/A	sw version 6.0.0	Base Module, General AUTOSAR and Hardware Specific register files
CRC	Crc_Ip	sw version 6.0.0	Driver, Cyclic Redundancy Check
DIO	Siul2_Dio	sw version 6.0.0	Driver, Digital Input Output

Table 5. Support and Driver Plugins Delivered*...continued*

Plugin	Low level interface	SW Version	Description
ETH_43_GMAC	GMAC_ip	sw version 6.0.0	Driver, Ethernet
FEE	N/A	sw version 6.0.0	Driver, Flash EEPROM Emulation
GPT	Emios_Gpt, Pit, Rtc, Stm	sw version 6.0.0	Driver, General Purpose Timer
I2C	FlexIO_I2C, LPI2C	sw version 6.0.0	Driver, Inter-Integrated Circuit
I2S	FlexIO_I2S, Sai_Ip	sw version 6.0.0	Driver, Inter-IC Sound
ICU	Emios_Icu, Cmp, Siul2_Icu, Wkpu	sw version 6.0.0	Driver, Input Capture Unit
LIN_43_LPUART_FLEXIO	FlexIo_Lin, LPUART	sw version 6.0.0	Driver, Local Interconnect Network
MCL	Cache_Ip, Dma_Ip, Lcu_Ip, Trgmux_Ip, Emios_Mcl	sw version 6.0.0	Driver, Microcontroller Library
MCU	Clock_Ip, Power_Ip, Ram_Ip, Siul2_Mcu, Emios_Mcu	sw version 6.0.0	Driver, Microcontroller Unit
OCU	Emios_Ocu	sw version 6.0.0	Driver, Output Control Unit
PLATFORM	startup, IntCtrl_Ip, Intm_Ip, Mpu_M7_Ip, System_Ip	sw version 6.0.0	Driver, Platform
PORT	Siul2_Port, Tspc_Port	sw version 6.0.0	Driver, Port
PWM	Emios_Pwm, FlexIo_Pwm, Etpu_Pwm	sw version 6.0.0	Driver, Pulse Width Modulation
RESOURCE	N/A	sw version 6.0.0	Resource Module, Required by all other modules to select MCU derivative
RM	Axbs_Ip, Xrdc_Ip, Sema42_Ip, Xbic_Ip, Pflash_Ip, Virt_Wrapper_Ip, Dmamux_Ip, Mscm_Ip	sw version 6.0.0	Resource Module, Resource Manager
SENT	FlexIo_Sent	sw version 6.0.0	Driver, Single edge nibble transmission
SPI	SPI FlexIO_Spi, Lpspi, Dspi	sw version 6.0.0	Driver, Serial Peripheral Interface
UART	FlexIo_UART, LPUART	sw version 6.0.0	Driver, UART Driver
ZIPWIRE	N/A	sw version 6.0.0	Driver, Zipwire
AE	Hvm_Ip, Aec_Ip	sw version 6.0.0	Driver, Aplication Extention
WDG	Swt_Ip, AeWdog_Ip	sw version 6.0.0	Driver, Watchdog
MEM_43_INFLS	C40_Ip, Pflash_Ip	sw version 6.0.0	Driver, Mem Internal Flash
MEM_43_EXFLS	Qspi_Ip	sw version 6.0.0	Driver, Mem External Flash

Table 5. Support and Driver Plugins Delivered*...continued*

Plugin	Low level interface	SW Version	Description
MEM_43_EEP	Sd_Emmc_Ip	sw version 6.0.0	Driver, Mem EEPROM
MEMACC		sw version 6.0.0	Driver, MemAcc
MESSAGING	Mu_Ip	sw version 6.0.0	Driver, Messaging
GDU	Gdu_Ip	sw version 6.0.0	Driver, Gate Driver Uinit
LINTRCV_43_AE	N/A	sw version 6.0.0	Driver, Lin Transceiver
CANTRC_43_AE	N/A	sw version 6.0.0	Driver, Can Transceiver
DPGA	Dpga_Ip	sw version 6.0.0	Driver, DPGA Driver
CANIF	N/A	sw version 6.0.0	Support Stub, Controller Area Network Interface
NVM	N/A	sw version 6.0.0	Support stub, NVRAM Manager
DEM	N/A	sw version 6.0.0	Support Stub, Diagnostic Event Manager
DET	N/A	sw version 6.0.0	Support Stub, Development Error Tracer
ECUC	N/A	sw version 6.0.0	Support Stub, ECU Configuration
ECUM	N/A	sw version 6.0.0	Support Stub, ECU State Manager
ETHIF	N/A	sw version 6.0.0	Support Stub, Ethernet Interface
ETHTRCV	N/A	sw version 6.0.0	Support stub, Ethernet Transceiver
ETHSWT	N/A	sw version 6.0.0	Support stub, Ethernet Switch
LINIF	N/A	sw version 6.0.0	Support Stub, Local Interconnect Network Interface
MEMIF	N/A	sw version 6.0.0	Support Stub, Memory Interface
OS	N/A	sw version 6.0.0	Support stub, Operating System
RTE	N/A	sw version 6.0.0	Support Stub, only for Schedule Manager
WDGIF	N/A	sw version 6.0.0	Support Stub, Watchdog Interface
MKA	N/A	sw version 6.0.0	Support Stub, Ethernet Interface

2.6 Module Plugin Folder Structure

Table 6. Module Plugin Folder Structure

Folder or file	Description
<mod>_TS_TtDdMmIiRr\anchors.xml	Tresos Configuration tooling documentation data file
<mod>_TS_TtDdMmIiRr\plugin.xml	Tresos Configuration tooling data file
<mod>_TS_TtDdMmIiRr\ant_generator.xml	Tresos Configuration tooling data file
<mod>_TS_TtDdMmIiRr\autosar\<mod>.epd	Module Parameter Definition in AUTOSAR format
<mod>_TS_TtDdMmIiRr\config\<mod>.xdm	Module Parameter Definition in Tresos XDM format
<mod>_TS_TtDdMmIiRr\config_ext\<mod>PreConfiguration.xdm	Module Parameter Default Configuration in Tresos XDM format[1]

Table 6. Module Plugin Folder Structure*...continued*

Folder or file	Description
<mod>_TS_TtDdMmIiRr\doc\AUTOSAR_RTD_<mod>_IM.pdf	Module Integration Manual
<mod>_TS_TtDdMmIiRr\doc\AUTOSAR_RTD_<mod>_UM.pdf	Module User's Manual
<mod>_TS_TtDdMmIiRr\generate_PB	Post-build source files (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_PB\src	Post-build source file templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_PB\include	Post-build source file header templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_LT	Link-time source files (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_LT\src	Link-time source file templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_LT\include	Link-time source file templates (only if applicable)
<mod>_TS_TtDdMmIiRr\generate_PC\	Pre-compile source files
<mod>_TS_TtDdMmIiRr\generate_PC\src	Pre-compile source files templates
<mod>_TS_TtDdMmIiRr\generate_PC\include	Pre-compile source files templates
<mod>_TS_TtDdMmIiRr\generate_swcd	Module BSWMD file
<mod>_TS_TtDdMmIiRr\include\	Module driver header files
<mod>_TS_TtDdMmIiRr\META-INF	Tresos Configuration tooling data and signature files
<mod>_TS_TtDdMmIiRr\src\	Module driver source files[2]

Notes:

[1] Not available for all plugins.

[2] The Support Stub Resource contains the "resource" folder instead of the "src" folder.

2.7 Compiler Options

This release was developed and tested with:

- NXP GCC 10.2.0 20200723
- Green Hills Multi 7.1.6d / Compiler 2021.1.4
- IAR ANSI C/C++ Compiler v.8.50.10 (safety version)
- Wind River Diab Compiler v7.0.6

2.7.1 DIAB Compiler/Linker/Assembler Options

Table 7. Compiler Options

Option	Description
-tARMCORTEXM7MG:simple	Selects target processor (hardware single-precision, software double-precision floating-point)
-mthumb	Selects generating code that executes in Thumb state
-std=c99	Follows the C99 standard for C
-Oz	Like -O2 with further optimizations to reduce code size
-g	Generates DWARF 4.0 debug information
-fstandalone-debug	Emits full debug info for all types used by the program

Table 7. Compiler Options*...continued*

Option	Description
-Wstrict-prototypes	Warn if a function is declared or defined without specifying the argument types
-Wsign-compare	Produce warnings when comparing signed type with unsigned type
Wdouble-promotion	Give a warning when a value of type float is implicitly promoted to double
-Wunknown-pragmas	Issues a warning for unknown pragmas
-Wundef	Warns if an undefined identifier is evaluated in an #if directive. Such identifiers are replaced with zero
-Wextra	Enables some extra warning flags that are not enabled by '-Wall'
-Wall	Enables all of the most useful warnings (for historical reasons this option does not literally enable all warnings)
-pedantic	Emits a warning whenever the standard specified by the -std option requires a diagnostic
-Werror=implicit-function-declaration	Generates an error whenever a function is used before being declared
-fno-common	Compile common globals like normal definitions
-fno-signed-char	Char is unsigned
-fno-trigraphs	Do not process trigraph sequences
-V	Displays the current version number of the tool suite
-c	Stop after assembly and produce an object file for each source file
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DMPU_ENABLE	Predefine MPU_ENABLE as a macro, with definition 1. Enable MPU default configuration from startup code under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

Table 8. Assembler Options

Option	Description
-mthumb	Selects generating code that executes in Thumb state
-Xpreprocess-assembly	Invokes C preprocessor on assembly files before running the assembler
-Xassembly-listing	Produces an .lst assembly listing file
-c	Stop after assembly and produce an object file for each source file
-tARMCORTEXM7MG:simple	Selects target processor (hardware single-precision, software double-precision floating-point)

Table 9. Linker Options

Option	Description
-e Reset_Handler	Make the symbol Reset_Handler be treated as a root symbol and the start label of the application
linker_script_file.dld	Use linker_script_file.dld as the linker script. This script replaces the default linker script (rather than adding to it)
-m30	m2 + m4 + m8 + m16
-Xstack-usage	Gathers and display stack usage at link time
-Xpreprocess-lecl	Perform pre-processing on linker scripts
-Llibrary_path	Points to the libraries location for ARMV7EMMG to be used for linking
-lc	Links with the standard C library
-lm	Links with the math library
-tARMCORTEXM7MG:simple	Selects target processor (hardware single-precision, software double-precision floating-point)

2.7.2 GCC Compiler/Linker/Assembler Options

Table 10. Compiler Options

Option	Description
-mcpu=cortex-m7	Targeted ARM processor for which GCC should tune the performance of the code
-mthumb	Generates code that executes in Thumb state
-mlittle-endian	Generate code for a processor running in little-endian mode
-mfpu=fpv5-sp-d16	Specifies the floating-point hardware available on the target
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions
-std=c99	Specifies the ISO C99 base standard
-Os	Optimize for size. Enables all -O2 optimizations except those that often increase code size

Table 10. Compiler Options*...continued*

Option	Description
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-Wall	Enables all the warnings about constructions that some users consider questionable, and that are easy to avoid (or modify to prevent the warning), even in conjunction with macros
-Wextra	This enables some extra warning flags that are not enabled by -Wall
-pedantic	Issue all the warnings demanded by strict ISO C. Reject all programs that use forbidden extensions. Follows the version of the ISO C standard specified by the aforementioend -std option.
-Wstrict-prototypes	Warn if a function is declared or defined without specifying the argument types
-Wundef	Warn if an undefined identifier is evaluated in an #if directive. Such identifiers are replaced with zero
-Wunused	Warn whenever a function, variable, label, value, macro is unused
-Werror=implicit-function-declaration	Make the specified warning into an error. This option throws an error when a function is used before being declared
-Wsign-compare	Warn when a comparison between signed and unsigned values could produce an incorrect result when the signed value is converted to unsigned.
-Wdouble-promotion	Give a warning when a value of type float is implicitly promoted to double
-fno-short-enums	Specifies that the size of an enumeration type is at least 32 bits regardless of the size of the enumerator values.
-funsigned-char	Let the type char be unsigned by default, when the declaration does not use either signed or unsigned
-funsigned-bitfields	Let a bit-field be unsigned by default, when the declaration does not use either signed or unsigned
-fomit-frame-pointer	Omit the frame pointer in functions that don’t need one. This avoids the instructions to save, set up and restore the frame pointer; on many targets it also makes an extra register available.
-fno-common	Makes the compiler place uninitialized global variables in the BSS section of the object file. This inhibits the merging of tentative definitions by the linker so you get a multiple-definition error if the same variable is accidentally defined in more than one compilation unit
-fstack-usage	Makes the compiler output stack usage information for the program, on a per-function basis
-fdump-ipa-all	Enables all inter-procedural analysis dumps
-c	Stop after assembly and produce an object file for each source file

Table 10. Compiler Options*...continued*

Option	Description
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DMPU_ENABLE	Predefine MPU_ENABLE as a macro, with definition 1. Enable MPU default configuration from startup code under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.
--sysroot= $ (NEWLIB_DIR)	Specifies the path to the sysroot, for Cortex-M7 it is $ (TOOLCHAIN_DIR)/arm-none-eabi/newlib
-specs=nano.specs	Use Newlib nano specs
-specs=nosys.specs	Do not use printf/scanf

Table 11. Assembler Options

Option	Description
-Xassembler-with-cpp	Specifies the language for the following input files (rather than letting the compiler choose a default based on the file name suffix)
-mcpu=cortex-m7	Targeted ARM processor for which GCC should tune the performance of the code
-mfpu=fpv5-sp-d16	Specifies the floating-point hardware available on the target
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions
-mthumb	Generates code that executes in Thumb state
-c	Stop after assembly and produce an object file for each source file

Table 12. Linker Options

Option	Description
-Wl,-Map,filename	Produces a map filer

Table 12. Linker Options*...continued*

Option	Description
-T linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
--entry=Reset_Handler	Specifies that the program entry point is Reset_Handler
-nostartfiles	Do not use the standard system startup files when linking
-mcpu=cortex-m7	Targeted ARM processor for which GCC should tune the performance of the code
-mthumb	Generates code that executes in Thumb state
-mfpu=fpv5-sp-d16	Specifies the floating-point hardware available on the target
-mfloat-abi=hard	Specifies the floating-point ABI to use. "hard" allows generation of floating-point instructions and uses FPU-specific calling conventions
-mlittle-endian	Generate code for a processor running in little-endian mode
-ggdb3	Produce debugging information for use by GDB using the most expressive format available, including GDB extensions if at all possible. Level 3 includes extra information, such as all the macro definitions present in the program
-lc	Link with the C library
-lm	Link with the Math library
-lgcc	Link with the GCC library
-specs=nano.specs	Use Newlib nano specs
-specs=nosys.specs	Do not use printf/scanf
--sysroot=$ (LIB_DIR)	Specifies the path to the sysroot, for Cortex-M7, it is $ (TOOLCHAIN_DIR)/arm-none-eabi/newlib

2.7.3 GHS Compiler/Linker/Assembler Options

Table 13. Compiler Options

Option	Description
-cpu=cortexm7	Selects target processor: Arm Cortex M7
-thumb	Selects generating code that executes in Thumb state
-fpu=vfpv5_d16	Specifies hardware floating-point using the v5 version of the VFP instruction set, with 16 double-precision floating-point registers
-fsingle	Use hardware single-precision, software double-precision FP instructions
-c99	Specifies the ISO C99 base standard
--ghstd=last	Use the most recent version of Green Hills Standard mode (which enables warnings and errors that enforce a stricter coding standard than regular C and C++)
-Osize	Optimize for size
--gnu_asm	Enables GNU extended asm syntax support
-dual_debug	Generate DWARF 2.0 debug information

Table 13. Compiler Options*...continued*

Option	Description
-G	Generate debug information
-keeptempfiles	Prevents the deletion of temporary files after they are used. If an assembly language file is created by the compiler, this option will place it in the current directory instead of the temporary directory
-Wimplicit-int	Produce warnings if functions are assumed to return int
-Wshadow	Produce warnings if variables are shadowed
-Wtrigraphs	Produce warnings if trigraphs are detected
-Wundef	Produce a warning if undefined identifiers are used in #if preprocessor statements
--unsigned_chars	Let the type char be unsigned, like unsigned char
--unsigned_fields	Bitfelds declared with an integer type are unsigned
--no_commons	Allocates uninitialized global variables to a section and initializes them to zero at program startup
--no_exceptions	Disables C++ support for exception handling
--no_slash_comment	C++ style // comments are not accepted andgenerate errors
--prototype_errors	Controls the treatment of functions referenced or called when no prototype has been provided
--incorrect_pragma_warnings	Controls the treatment of valid #pragma directives that use the wrong syntax
-c	Stop after assembly and produce an object file for each source file
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DMPU_ENABLE	Predefine MPU_ENABLE as a macro, with definition 1. Enable MPU default configuration from startup code under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

Table 14. Assembler Options

Option	Description
-cpu=cortexm7	Selects target processor: Arm Cortex M7
-fpu=vfpv5_d16	Specifies hardware floating-point using the v5 version of the VFP instruction set, with 16 double-precision floating-point registers
-fsingle	Use hardware single-precision, software double-precision FP instructions
-preprocess_assembly_files	Controls whether assembly files with standard extensions such as .s and .asm are preprocessed
-list	Creates a listing by using the name and directory of the object file with the .lst extension
-c	Stop after assembly and produce an object file for each source file

Table 15. Linker Options

Option	Description
-T linker_script_file.ld	Use linker_script_file.ld as the linker script. This script replaces the default linker script (rather than adding to it)
-e Reset_Handler	Make the symbol Reset_Handler be treated as a root symbol and the start label of the application
-map	Produce a map file
-keepmap	Controls the retention of the map file in the event of a link error
-Mn	Generates a listing of symbols sorted alphabetically/ numerically by address
-delete	Instructs the linker to remove functions that are not referenced in the final executable. The linker iterates to find functions that do not have relocations pointing to them and eliminates them
-ignore_debug_references	Ignores relocations from DWARF debug sections when using -delete. DWARF debug information will contain references to deleted functions that may break some third-party debuggers
-Llibrary_path	Points to library_path (the libraries location) for thumb2 to be used for linking
-larch	Link architecture specific library
-lstartup	Link run-time environment startup routines. The source code for themodules in this library is provided in the src/libstartup directory
-lind_sd	Link language-independent library, containing support routines for features such as software floating point, run-time error checking, C99 complex numbers, and some general purpose routines of the ANSI C library

Table 15. Linker Options*...continued*

Option	Description
-v	Prints verbose information about the activities of the linker, including the libraries it searches to resolve undefined symbols
-keep=C40_Ip_AccessCode	Avoid linker remove function C40_Ip_AccessCode from Fls module because it is not referenced explicitly
-nostartfiles	Controls the start files to be linked into the executable

2.7.4 IAR Compiler/Linker/Assembler Options

Table 16. Compiler Options

Option	Description
--cpu=Cortex-M7	Targeted ARM processor for which IAR should tune the performance of the code
--cpu_mode=thumb	Generates code that executes in Thumb state
--endian=little	Generate code for a processor running in little-endian mode
--fpu=FPv5-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant.
-e	Enables all IAR C language extensions
-Ohz	Optimize for size. the compiler will emit AEABI attributes indicating the requested optimization goal. This information can be used by the linker to select smaller or faster variants of DLIB library functions
--debug	Makes the compiler include debugging information in the object modules. Including debug information will make the object files larger
--no_clustering	Disables static clustering optimizations. Static and global variables defined within the same module will not be arranged so that variables that are accessed in the same function are close to each other
--no_mem_idioms	Makes the compiler not optimize certain memory access patterns
--do_explicit_zero_opt_in_named_sections	Disable the exception for variables in user-named sections, and thus treat explicit initializations to zero as zero initializations, not copy initializations
--require_prototypes	Force the compiler to verify that all functions have proper prototypes. Generates an error otherwise
--no_wrap_diagnostics	Does not wrap long lines in diagnostic messages
--diag_suppress=Pa050	Suppresses diagnostic message Pa050
-DIAR	Predefine IAR as a macro, with definition 1
-DUSE_SW_VECTOR_MODE	Predefine USE_SW_VECTOR_MODE as a macro, with definition 1. By default, the drivers are compiled to handle interrupts in Software Vector Mode.

Table 16. Compiler Options*...continued*

Option	Description
-DD_CACHE_ENABLE	Predefine D_CACHE_ENABLE as a macro, with definition 1. Enables data cache initalization in source file system.c under the Platform driver
-DI_CACHE_ENABLE	Predefine I_CACHE_ENABLE as a macro, with definition 1. Enables instruction cache initalization in source file system.c under the Platform driver
-DMPU_ENABLE	Predefine MPU_ENABLE as a macro, with definition 1. Enable MPU default configuration from startup code under the Platform driver
-DENABLE_FPU	Predefine ENABLE_FPU as a macro, with definition 1. Enables FPU initalization in source file system.c under the Platform driver
-DMCAL_ENABLE_USER_MODE_SUPPORT	Predefine MCAL_ENABLE_USER_MODE_SUPPORT as a macro, with definition 1. Allows drivers to be configured in user mode.

Table 17. Assembler Options

Option	Description
--cpu Cortex-M7	Targeted ARM processor for which IAR should generate the instruction set
--fpu VFPv5-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant.
--cpu_mode thumb	Selects the thumb mode for the assembler directive CODE
-g	Disables the automatic search for system include files
-r	Generates debug information

Table 18. Linker Options

Option	Description
--map filename	Produces a map file
--config linkerfile	Use linkerfile as the linker script. This script replaces the default linker script (rather than adding to it)
--cpu=Cortex-M7	Selects the ARM processor variant to link the application for
--fpu=FPv5-SP	Use this option to generate code that performs floating-point operations using a Floating Point Unit (FPU). Single-precision variant.
--entry _start	Treats _start as a root symbol and start label
--enable_stack_usage	Enables stack usage analysis. If a linker map file is produced, a stack usage chapter is included in the map file
--skip_dynamic_initialization	Dynamic initialization (typically initialization of C++ objects with static storage duration) will not be performed automatically during application startup

Table 18. Linker Options*...continued*

Option	Description
--no_wrap_diagnostics	Does not wrap long lines in diagnostic messages

2.8 Examples and Demos

The drivers provide a set of examples. For details, please refer to Examples\...\readme.txt file from each driver folder.

3 Known Issues for S32K3_S32M27x RTD 6.0.0

3.1 Known Issues for 6.0.0

ID	Headline
ARTD-189731	[ADC] ADC_SAR_IP_IS_USED macro not generated correctly in CT
ARTD-189510	[GPT][S32K3XX-M27X] Different code gen between EB and CT for Rtc Ip
ARTD-189500	[GPT][S32K3XX_M27X] Parameter "clkMode" is unused in Gpt_Ipw_SetClockModeInStance function
ARTD-189496	[WDG] Missing support ERR052226 for some derivatives
ARTD-188961	[S32K3xx_S32M27x_6.0.0][WDG] Remove a redundant function generated in the plugin
ARTD-188855	[S32K3XX][Messaging]Fix Warning in Examples
ARTD-188846	[S32K3xx_S32M27x_6.0.0][PORT] Compare generated code between generators
ARTD-188699	[gpt] Issue in the implementation of MR200.
ARTD-188692	[OCU] No errors were detected when using the same EMIOS channel with another module
ARTD-188575	[mem_infls] If ownership has been granted to another domain (e.g., HSE), the Lock API must not be invoked from a different domain.
ARTD-188561	[S32K3xx_S32M27x_6.0.0][GPT]: Fix violations MISRA C-2012 Rule 8.4
ARTD-188544	[MCU] WKPU must be enabled before entering any low power modes
ARTD-186366	[SPI][S32K3 600] Plugins interface issue
ARTD-186252	SpiBaudrateConfig is not detected when "SpiUseBaudrateConfig" is checked for LLD, HLD is fine.
ARTD-186174	[S32K3xx_S32M27x_6.0.0][Port] Can not import CMP1_CMP1_OUT mode from Eb to s32ds
ARTD-186127	[S32K3XX_S32M27X RTM 6.0.0] Failure at building step when using autosar OS
ARTD-186048	[PWM] Issue related to Pwm_EnableFaultNotification function on run time
ARTD-186027	[PWM]: Difference when generate file from EBT and S32CT
ARTD-184166	[MCL] Some statements/branches cannot be reached
ARTD-184082	[adc] [Safety Assessment] The MISRA rule 2.5 needs to be fixed
ARTD-184031	[crc] [Safety Assessment] The MISRA rule 2.5 needs to be fixed
ARTD-183514	[PWM][EMIOS] Pwm_Init generates a spike in the output signal.
ARTD-183441	[MCL] Feature LCU software sync mode does not work correctly
ARTD-183296	[mem_infls] Lock of the sector is not performed if ownership was previously held by another Domain
ARTD-183169	[S32K3xx_S32M27x_6.0.0] [CRC]: Wrong calculation with Crc_CalculateCRC32C

ID	Headline
ARTD-182249	[MCU] Missing SXOSC clock gate in resource file
ARTD-181183	[FLS] Fls Timeout not reported if Flash Array Integrity (UT0_AID) bit is not set after FLASH_USER_TEST_WAIT interval
ARTD-180730	GPT PIT max LDVALn[TSV]
ARTD-180663	[spi] Implement check on partition assigned for correctness or out of bounds accesses
ARTD-180639	[platform] Implement check on partition assigned for correctness or out of bounds accesses
ARTD-180585	[gpt] Implement check on partition assigned for correctness or out of bounds accesses
ARTD-180570	[rm] Implement check on partition assigned for correctness or out of bounds accesses
ARTD-180531	[crc] Implement check on partition assigned for correctness or out of bounds accesses
ARTD-180516	[base] Implement check on partition assigned for correctness or out of bounds accesses
ARTD-180510	[adc] Implement check on partition assigned for correctness or out of bounds accesses
ARTD-176983	S32T(S32K324): No validation from development team with Application Extension due to the Hardware not being available.
ARTD-175409	DIO Component file generation issue
ARTD-174406	[Clock]S32K310 PLL_PHI Clock config
ARTD-169518	[SPI] Cannot config more SpiExternalDevice on S32DS with S32G-RTD 5.0.0
ARTD-167877	S32K312 RTD 4.0.0 use of FLS driver to UTEST write
ARTD-159275	[ALL_GENERAL] Build fail when use trusted call by AUTOSAR OS or ZEPHYR
ARTD-143460	[Mem_INFLS] ADR Register return wrong value when abort a write operation
ARTD-141044	[GPT] Functions in ".h" file but does not include in "ReqExport.txt" file
ARTD-137946	[GPT] [S32K3XX] Fix failed items in code review and design review checklist
ARTD-110833	[FLS] Update driver following Errata ERR051358 for S32K3XX
ARTD-66533	[S32K3xx_S32M27x_6.0.0] GPT: STM timer Call back not triggered if resolution is less than 6 micro sec
ARTD-47333	[SPI][S32K3] Flexio slave CPHA=0 reports Rx overrun error at the last Rx frame when CS is de-asserted
ARTD-127904	[MEM_INFLS] Stuck at load code to ram when enabling loop unrolling option on Diab
ARTD-143126	[S32K3XX_S32M27x_5.0.0][I2S]: Flexio DMA transmits incorrect data when BytesWidth is 8
ARTD-54102	[SPI][S32K][FLEXIO] Master CS is only continuous between datas in channel but not between channels in job
ARTD-142720	[MCU] Wrong implementation of the function Power_Ip_MC_ME_SocStandbyEntry
ARTD-141470	[MCU] Wrong implementation of the sequence of enabling and disabling PLL
ARTD-137968	[MCU] Optimize the function Clock_Ip_EnableCmuFcFceRefCntLfrefHfref
ARTD-143904	[MCU] Wrong implementations of QSPI_MEM_CLK conditions on the interface
ARTD-144078	[S32M27x] Application boot not implemented with S32M27x
ARTD-142971	[MCU] Mcu component show wrong value for external clock S32K388
ARTD-143213	[MCU][S32K3-S32M27x] wrong implement clock source CGM_MUX11 in interface
ARTD-142935	[MCU] Remove functions that cannot be called in S32K3XX_S32M27x_5.0.0

ID	Headline
ARTD-126874	[Mem_ExFls] "Return value" field in ReqExport for Mem_Suspend and Mem_Resume is not correct - follow up
ARTD-124738	[FLS] Macro C40 FLS_MAX_VIRTUAL_SECTOR is incorrect
ARTD-141875	[OCU] Fix the findings after code/design review against checklist
ARTD-61591	[MEM_EXFLS] Bulk data read is not stable on K358, on HyperFlash board
ARTD-98052	[GPT] Fix the findings after code/design review against checklist
ARTD-99143	[PWM] Solve findings from design and code review against checklist
ARTD-98127	[Ocu] Fix code and design review findings
ARTD-75827	[Mcu] The S32K3X4EVB-T172 EVB enters in a sequential reset state
ARTD-101235	[MCU][S32K3-S32M27x] wrong list clock
ARTD-100060	[FEE] Implementation of Fee_JobEndNotification is not correct
ARTD-99266	[MemAcc] Interface of MemAcc_RequestLock is inconsistent between ReqImport.txt and MemAcc.h files (Follow-up)
ARTD-46975	[S32K3XX] [FLS] Bulk data read is not stable on K358, on HyperFlash board
ARTD-7913	[MCU] Fix VSMD errors related to XPath expression for MIN attributes - resource file not found
ARTD-188575	[mem_infls] If ownership has been granted to another domain (e.g., HSE), the Lock API must not be invoked from a different domain.
ARTD-183296	[mem_infls] Lock of the sector is not performed
ARTD-190452	[Mem_InFls] Update description for Mem_43_INFLS_IPW_Cancel
ARTD-190510	[Mem_InFls] Remove redundant definition C40_IP_MAIN_INTERFACE_ENABLED

4 Changes List for S32K3_S32M27x RTD 6.0.0

4.1 Change List for 6.0.0

ID	Subtype	Headline and Description
ARTD-25673	Bug	[SPI] DMA TCD is not reset when Spi_Cancel called in Slave mode Detailed description (how to reproduce it): Spi_Cancel is called to cancel transfer of SPI in Slave mode in the fault case but DMA is not reset. At next transfer, TCD of TX/RX channel will not updated and the last TCD configuration will be used leading to incorrectly behavior of transfer. Preconditions: Spi_Cancel API is called in Slave mode Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Receive data of next Slave channel is incorrect Expected behavior: Work fine Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update Spi_Cancel function to reset the value of some variables which is using to identify some TCD parameters of next channel is needed to update or not. State->IsPreTxBufferNull = FALSE; State->IsPreRxBufferNull = FALSE; State->PreTxMajorLoopCount = 0u; State->PreRxMajorLoopCount = 0u;

ID	Subtype	Headline and Description
		!screenshot-1.png|thumbnail!
ARTD-37721	Bug	[S32ZE 090] [RM] Exclusive Area usage is redundant in XBIC Detailed description (how to reproduce it): Some Exclusive Area are used inappropriately with atomic writing And it can cause a fail at runtime with XBIC Ip (after Rm_XbicErrorInjection(), a fail can be occured when call SchM_Exit_Rm_RM_EXCLUSIVE_AREA_03) Need to review again all Exclusive Area in driver Preconditions: Enable XBIC IP and use Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Run fail (a error raise for XBIC before transaction) Expected behavior: Error raise for XBIC after transaction Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-75883	Bug	[S32K1_M24X RTM 2.0.0] MemAcc: MemAcc_Erase return not ok when start erase address correct but not align with sector size of current subaddressarea Detailed description (how to reproduce it): MemAcc: MemAcc_Erase return not ok when start erase address correct but not align with sector size of current subaddressarea Preconditions: adressarea contains multiple HW type Test Case ID (internal TC that caught the defect) optional: Memacc_TS_020 Observed behavior: MemAcc return E_NOT_OK Expected behavior: MemAcc return E_OK Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-96452	Bug	[platform] Remove adhoc CCOPT values and use generated values based on resource Detailed description (how to reproduce it): Remove custom CCOPT and use generated values based on resource used see [PR comment|https://bitbucket.sw.nxp.com/projects/ARTD/repos/platform/pull-requests/751/overview?commentId=2165839] Remove the mentions from UM/IM as well Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Custom CCOPT are requested to be used by customer to build the code for a specific NPI these values should be generated based on configuration and not forced in CCOPT in makefiles Expected behavior: Use generated values Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-98607	Bug	[MCU][S32K3-S32M27x] Fix finding review checklist Detailed description (how to reproduce it): There are findings after perform review checklist in ticket ARTD-89404. Check the report in crucible ARTD-89404 and fix all the findings. Preconditions: N/A

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Violations in review checklist Expected behavior: All the violations are fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-101677	Bug	[S32K3xx_S32M27x_4.0.0] S32CT: Un-available SWT1 gate still exist on interface Detailed description (how to reproduce it): On S32K348, unavailable SWT1 gate still exists on the interface Preconditions: S32K348, S32CT Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Unavailable SWT1 gate still exists on the interface Expected behavior: Unavailable SWT1 gate does not exist on the interface Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-102661	Bug	[Uart] Uart header file shall follows the naming convention as CDD_Uart.h Detailed description (how to reproduce it): For below CDD modules, include files are not prefixed with CDD in *Uart* plugin, CDD_Uart.h i added with below macro inclusion #ifndef UART_H #define UART_H instead, should have been as #ifndef CDD_UART_H #define CDD_UART_H Preconditions: #ifndef CDD_UART_H #define CDD_UART_H Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: as Detailed description Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Preconditions
ARTD-107524	Bug	[SPI] In RTD_SPI_UM.pdf file, guideline DMA Mux configuration is incorrect Detailed description (how to reproduce it): !image-2024-01-05-15-52-36-720.png! Following the UM file, DMA MUX Source was configured at the Mcl module instead of RM module as actually. Preconditions: Guideline for DMA MUX configuration must be noted correct in UM file Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: as Detailed description

ID	Subtype	Headline and Description
		Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-109944	Bug	[Mem_43_INFLS]: C40 flash return PEP error if no synchronization with sbaf is implemented Detailed description (how to reproduce it): Customers meet issue while using C40 drivers. They are using C40 driver (Mem_43_INFLS) and place all the driver codes into RAM, with debugger, full speed run, no issue observed. However, without debugger > reset the board/power down cycle the board > then attach debugger. Found that the program runs into error with flash PEP error. We re-appeared the issue with a basic example code (Please refer to the attached example project). In this example project, "access code" to RAM enabled. According to the test result, it seems the blocks 1 and 2 don't have problem, but the blocks 0 and 3 have problem. If we erase any sector of the block 1 & 2 first, then all the blocks can work normally, but if we erase any sector of the block 0 or 3, it will report PEP error at the beginning (first sector you try to erase). Preconditions: 1. Erase any sector which belongs to block 0 or 3. 2. Power down cycle the board/ reset the board, then free run without debugger. 3. Attach to system, check the result/status. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Returned PEP error Expected behavior: Running without any error with/without debugger Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-111402	Bug	[MCU] Update PLL clock ranges according with RM Detailed description (how to reproduce it): Some of the clocks (for S32K39 si S32K37) cannot be configured in ranges mentioned in RM !image-2024-02-09-16-11-16-451.png! !image-2024-02-09-16-11-27-526.png! !image-2024-02-09-16-11-41-462.png! !image-2024-02-09-16-11-56-036.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Cannot configure the upper limit of some clocks as mentioned in the RM Expected behavior: Clocks can be configured as stated in RM Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update clocks ranges as pe latest RM.
ARTD-111785	Bug	[PWM][PWM_ETPU] The duty value returned after calling the Etpu_Pwm_Ip_GetDuty function is incorrect Detailed description (how to reproduce it): First, I call the Etpu_Pwm_Ip_Init function with duty = 4000U and Period = 8000U.

ID	Subtype	Headline and Description
		Next, I call the Etpu_Pwm_Ip_UpdateDuty function with {*}duty = 983U{*}. The value written into the Etpu_Ip_WriteU24Param function is {*}239 (but the actual value is 239.99){*}. !image-2024-02-16-14-45-13-958.png|width=561,height=103! Finally, I call the Etpu_Pwm_Ip_GetDuty function, the u24ActiveTime value taken from the Etpu_Ip_ReadU24Param function is {*}rounded to 239{*}. This leads to an error in the return value of the Etpu_Pwm_Ip_UpdateDuty function (978U compared to 983U). !image-2024-02-16-14-48-47-355.png|width=577,height=122! Preconditions: Period: 8000U DutyCycle: 983U Test Case ID (internal TC that caught the defect) optional: Ip_Etpu_TS_002 (Ip_Etpu_TC_FCT_0024) Observed behavior: The duty value after calling the Etpu_Pwm_Ip_GetDuty function (978U) is different from the expected value (983U) Expected behavior: The duty value after calling the Etpu_Pwm_Ip_GetDuty function is the same as the expected value Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-112288	Bug	[ADC] Bctu setting the last conversion of the list Detailed description (how to reproduce it): Customer Nexteer reported issue with using Adc_CtuSetList() [SW32K3_RTD_R21-11_3.0.0_P07_D2306] to change BCTU list during the runtime. Adc_CtuSetList() is calling Bctu_Ip_ConfigChanList responsible for update of the list. Update is executed in 2 steps. 1) loop calling of Bctu_SetConvListElemWithTag to update list element. 2) calling Bctu_SetConvListLastElement to set the last element of the list. there is a short moment between step 1 and step 2 when last element of the list is not set (bit LAST_y or LAST_y_plus_1 in LISTCHR). if this item is being executed in this moment, conversions get outside of the list space and malfunction occurs. For more details contact: John Floros [john.floros@nxp.com|mailto:john.floros@nxp.com] Tomas Fedor [tomas.fedor@nxp.com|mailto:tomas.fedor@nxp.com] Expected behavior: No space for mall function in Adc_CtuSetList() and Bctu_Ip_ConfigChanList during the runtime call. Proposed solution optional: Instead of the 2 step approach, all bits in LISTCHR register should be set within one write._
ARTD-112669	Bug	[ALL_GENERAL] modules.h file <module> always STD_OFF Detailed description (how to reproduce it): GPT module is enabled in EB tresos configuration tool(ver 29.0), but macro USE_GPT_MODULE in module.h file is always STD_OFF.* !image-2024-02-23-17-48-13-906.png! The issues is happen in another modules, like SPI, DIO, PORT.* !image-2024-02-23-18-02-33-413.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The defined macros for the modules are consistently set to STD_OFF. Expected behavior: The module's define macro is set to STD_ON during usage. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-114088	Bug	[PWM][PWM_ETPU] Generate spike pulse with Etpu_Pwm

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): I am configuring channels as shown : !image-2024-03-06-14-41-42-170.png|width=621,height=99! Issue 1:* After calling Pwm_Init() still generate spike pulse The spike occurs after stepping through pEtpu_Ip_Regs->CHAN[pPwmInstance->u8Channel].HSRR.B.HSR = ETPU_PWM_IP_HSR_INIT* in function Etpu_Pwm_Ip.c. Sharp pulse occurs when set polarity =LOW , Duty =100% (eTPUA_CH_0) !image-2024-03-06-15-07-45-513.png|width=553,height=74! !image-2024-03-06-15-09-23-910.png|width=550,height=142! Issue 2 : Calling the Pwm_SetDutyCycle/ Pwm_SetPeriodAndDuty function after the Pwm_SetOutputToIdle function is called will cause a spike pulse to appear. First, I call {*}Pwm_Init(){*}. then I call the Pwm_SetDutyCycle/ Pwm_SetPeriodAndDuty function with Duty =100% and call the Pwm_SetOutputToIdle function. Next, I call the Pwm_SetDutyCycle/ Pwm_SetPeriodAndDuty function again with Duty = 100%. After stepping through the {*}Etpu_Pwm_Ip_Start{*}() function in the Pwm_SetDutyCycle function, a spike pulse will appear. !image-2024-03-06-21-19-20-145.png|width=607,height=220! !image-2024-03-06-21-19-33-949.png|width=617,height=182! Preconditions: Setup Channel PWM_ETPU Issue 1: POLARITY = PWM_LOW DutyCyle* = 100% Issue 2: All case Polarity and Duty in file config Pwm.xdm Test Case ID (internal TC that caught the defect) optional: Pwm_TS_106 {_}CFGSETS=11{_}{_}{{_}}tresos\{_} Observed behavior: Spike pulse occur when call Pwm_Init function Expected behavior: No occurs pulse occurs Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ARTD-114185	Bug	[PWM] [ETPU] New_configuration generated by ECPD not map with Original_configuration
		
		Detailed description (how to reproduce it)
		
		Create Pwm_Etpu project on S32DS
		Add Etpu_Pwm, Etpu_Ip, ... component
		Generate ECVD, ECPD and mex file
		Run test suite with setup to check ecpd
		Check report and compare New_configuration vs Original_configuration
		How to generate ecpd file :
		After layout to {*}S32DS{*}, You need to go to the codegenerator.js file
		!image-2024-03-07-17-41-30-862.png|width=470,height=213!
		You need to change this code information
		if (scriptApi.getUtils().getHeadlessState()) {
		if (CGFilter.exportEcpd) {
		var configComponentList = profile.getMcuInfo().getAvailableComponents().getConfigComps().toArray();
		var mcuPackageName = profile.getMcuInfo().getPackage().toLowerCase();
		for each (var configComponent in configComponentList) {
		if (CGFilter.exportComponent(configComponent.getId())) {
		if (configComponent.isOptionSet("ecucDefinitionCollection")) {
		scriptApi.logInfo("[codeGenerator] Generating ECPD for " configComponent.getId());
		scriptEcpd.generateEcpdFile(configComponent, configComponent.getId() "_" mcuPackageName);
		}
		}
		}
		}
		}
		edited into
		var configComponentList = profile.getMcuInfo().getAvailableComponents().getConfigComps().toArray();
		var mcuPackageName = profile.getMcuInfo().getPackage().toLowerCase();
		for each (var configComponent in configComponentList) {
		if (CGFilter.exportComponent(configComponent.getId())) {
		if (configComponent.isOptionSet("ecucDefinitionCollection") && (configComponent.getId() === "Etpu_Pwm")) {
		scriptApi.logInfo("[codeGenerator] Generating ECPD for " configComponent.getId());
		scriptEcpd.generateEcpdFile(configComponent, configComponent.getId() "_" mcuPackageName);
		}
		}
		}
		After editing is complete, restart the project on s32ds so that the ecpd file appears

ID	Subtype	Headline and Description
		Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Ip_Etpu_TS_ECPD_001 Observed behavior: The number of files in the New_configuration and Original_configuration folders is different !image-2024-03-07-01-20-36-807.png|width=678,height=245! In Etpu_Pwm_s32k396289bga.ecpd file , there is no "Channel Base Address" node !image-2024-03-07-17-36-09-509.png|width=668,height=291! Expected behavior: All generated code have to mapping Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-124368	New Feature	[eth] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-133773	New Feature	[CAN] Add support for TX Low\High Msg Buff First NewWorkDescription: The new S32N79 (Luxor) for FLEXCAN add support in hardware for new feature as which message buffer first. Lowest-number message buffer first If CTRL1[LBUF] is 1, the first (lowest number) active transmission message buffer found is the arbitration winner. MCR[LPRIOEN] has no effect when CTRL1[LBUF] is 1. Highest-priority message buffer first If CTRL1[LBUF] is 0, the arbitration process searches for the active transmission message buffer with the highest priority. The frame of this message buffer has a higher probability of winning the arbitration on the CAN bus when multiple external nodes compete for the bus simultaneously. The sequence of bits considered for this arbitration is called the arbitration value of the message buffer. The transmission message buffer with the lowest arbitration value among all transmission message buffers has the highest priority. If two or more message buffers have equivalent arbitration values, the message buffer with the lowest number is the arbitration winner. The composition of the arbitration value depends on MCR[LPRIOEN]. High Attention to the Arbitration Process in order to don't create priority inversion. Requirement source: Update only if added a new field in configurator for HLD. (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-134904	Bug	[MCU]no/wrong Limit check for ODIV2 clock in MCU Clock/PLL Tresos Config Detailed description (how to reproduce it): [Very important check needed in Tresos config otherwise risk of field issues! ODIV2 max limit frequency not sufficiently clear documented in RM. A max limit check also missing in Tresos Config. Customer was using this config and went into series, error occured much later during production due to much too high bus frequency–> field return was needed . To avoid such cases please implement limit check for ODIV2 clock Clock config A was used with wrong settings like shown in picture in red. Based on our specification below and confirmation from design max. speed at ODIV2 clock is 480MHz like shown in the green setup (even if not mentioned in the RM : "Table 144. System clock frequency limitations).As shown in the WRONG Tresos config below (version 29.0) it can be seen gthat this wrong configuration is possible without and error in Tresos. Limit check to be implemented in Tresos to check if ODIV2 output is >480MHz in that configuratino and as well different ODIV2 clock checks for other configurations.

ID	Subtype	Headline and Description
		!image-2024-07-04-13-11-32-486.png! Spec: !image-2024-07-04-13-43-18-856.png|width=832,height=171! Spec also states that divider rations in Clock option table has to be followed, design confirmed that this is the max. speed. !image-2024-07-04-13-45-24-427.png|width=672,height=95! demonstration with Tresos 29 that wrong ODIV2 clock possible to be configured: !image-2024-07-04-13-47-37-873.png|width=715,height=847!] Preconditions: [ODIV2 clock >480MHz] Test Case ID (internal TC that caught the defect) optional: [not applicable] Observed behavior: [no limit check] Expected behavior: [configuration not allowed if ODIV2 output frequency >480MHz for this config and other ODIV2 limit checks for other configs] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [see expected behavior]
ARTD-137064	Bug	[pwm] eTPU example Etpu_Pwm_Ip_Example_S32K396 issue based on [SW32K3_RTD_R21-11_4.0.0_P14] Detailed description (how to reproduce it): [Run the Etpu_Pwm_Ip_Example_S32K396 on S32DS IDE[SW32K3_RTD_R21-11_4.0.0_P14][S32K3_ETPU_SW_4.7_1.0.0], the project cannot be build after generating the code in the config tool. found that not all the required source/headers are brought into the project by the configuration tool. !image-2024-07-11-11-47-11-337.png! Whether this version cannot support the eTPU PWM example based on S32DS config tool? and there are only eTPU_PWM module, not the eTPU module. !image-2024-07-11-11-50-38-632.png!] Preconditions: [import Etpu_Pwm_Ip_Example_S32K396 example project] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [cannot build the project] Expected behavior: [build project successfully] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [none]
ARTD-137835	Bug	[MCU] Wrong implementation of Clock_Ip_DisableCmuFcFceRefCntLfrefHfref Detailed description (how to reproduce it): There is a note in RM as below !image-2024-07-16-11-17-34-608.png! The driver is implementing as below !image-2024-07-16-11-18-39-219.png! If TimeoutOccured = True, it means SR[RS] = 0 but the driver still allows disabling the frequency check Preconditions:

ID	Subtype	Headline and Description
		N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Wrong implementation of Clock_Ip_DisableCmuFcFceRefCntLfrefHfref Expected behavior: Correct implementation of Clock_Ip_DisableCmuFcFceRefCntLfrefHfref Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-140877	Bug	[MCU] Wrong pll range for S32K3XX Detailed description (how to reproduce it): In description of node PLL_PHI1_Frequency, it has valid range for S32K3XX is 120-320Mhz. But user can configure 64Mhz !image-2024-07-22-14-51-17-225.png|width=472,height=298! !image-2024-07-22-14-51-44-464.png|width=580,height=181! Preconditions: EBT Test Case ID (internal TC that caught the defect) optional: MCU_TS_059 Observed behavior: Description of node and range of node is not match Expected behavior: Correct range of node to 120-320 as RM: S32K3xx_RM_Rev9_DraftA.pdf Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-141828	Bug	[MCU] WKPU must be enabled before entering any low power modes Detailed description (how to reproduce it): On S32K396 Step 1: Call a run mode or SOC_PREPARE_STANDBY disabling WKPU Step 2: Call STANDBY_MODE The status is as the below !image-2024-07-29-09-39-59-091.png! While there is a note in the driver !image-2024-07-29-09-40-49-775.png! => Add enabling WKPU in the func Power_Ip_PMC_PrepareLowPowerEntry Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing implementation of enabling WKPU before entering any low power modes Expected behavior: WKPU must be enabled before entering any low power modes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-141909	Bug	[MEMACC][S32N 1.0.0] Memory section for _SEC_VAR_INIT_UNSPECIFIED is missing from MemAcc_Bswmd.arxml Detailed description (how to reproduce it): in the file ..\MemAcc_TS_T31D62M10I0R0\generate_PB\src\MemAcc_PBcfg.c

ID	Subtype	Headline and Description
		below mention section is define, [!IF "node:value(AutosarExt/MemAccMultiCoreType3Support)='true'"!][!// [!VAR "MemAccSection" = "'_SEC_VAR_SHARED_INIT_UNSPECIFIED_NO_CACHEABLE'"!][!// [!ELSE!][!// [!VAR "MemAccSection" = "'_SEC_VAR_INIT_UNSPECIFIED'"!][!// [!ENDIF!][!// Observed behavior: Memory Section for "_SEC_VAR_INIT_UNSPECIFIED" is missing from MemAcc_Bswmd.arxml. Expected behavior: Memory Section for "_SEC_VAR_INIT_UNSPECIFIED" should be present in MemAcc_Bswmd.arxml. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update MemAcc_Bswmd.arxml to contain memory Section for "_SEC_VAR_INIT_UNSPECIFIED.
ARTD-142122	Bug	[sent] Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid. In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached. Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. Otherwise, we can use this command to enable case sensitive for all created subfolders and no need to renew them: "(Get-ChildItem foldername Recurse Directory).Fullname ForEach-Object {fsutil file setCaseSensitiveInfo "$_" enable}" # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-142255	Bug	[MCU] Wrong implementation of the function Power_Ip_PMC_EnableLastMile Detailed description (how to reproduce it): The function Power_Ip_PMC_EnableLastMile has a comment If external BJT is using on the PCB board ... !image-2024-07-30-16-51-54-394.png! => if ((boolean)TRUE != BJTused) is wrong. It should be if ((boolean)TRUE == BJTused) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Wrong implementation of the function Power_Ip_PMC_EnableLastMile Expected behavior: Correct implementation of the function Power_Ip_PMC_EnableLastMile

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-142242	New Feature	[S32K3XX][IMPLEMENTATION] Add support in Ethernet driver for GMAC features (Flexible PPS, EEE). Description: Pulse Per Second Feature were implemented on SAF85-SAF86-S32R41. Currently the implementation was updated on HLD and IPL. It should be implemented also on IPW for S32K3 which has the same GMAC IP and support also Pulse Per Second Feature The dev tests should be created as well for S32K3
ARTD-142417	Bug	[MCU] Wrong implementation of the function Power_Ip_PMC_DisableLastMile Detailed description (how to reproduce it): There is a sequence in RM like the below !image-2024-07-31-14-16-36-013.png! It does not care the status of PMC.CONFIG and if using BJT or not (only not applicable for S32K3x8, S32K312, S32K311 and S32K310). However the driver is implementing like the below if (0U != (IP_PMC->CONFIG & PMC_CONFIG_LMBCTLEN_MASK)) only means if LMBCTLEN is enabled or not. The driver should only care if having LMBCTLEN, it will simultaneously write 0 to both PMC.CONFIG[LMEN] and PMC.CONFIG[LMBCTLEN] !image-2024-07-31-14-21-00-530.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Wrong implementation of the function Power_Ip_PMC_DisableLastMile Expected behavior: Correct implementation of the function Power_Ip_PMC_DisableLastMile Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-142487	Bug	[MCU] Clock reference display wrong clock name Detailed description (how to reproduce it): Issue in S32K358: Step 1: Add Clock_Ip_ReferencePoint in s32ct, add all clock name which supported. Issue : Clock_Ip_ReferencePoint display EMAC_CLK_RX, EMAC_CLK_TX, EMAC_CLK_TS but them not be define. The correct name is GMAC_CLK_RX, GMAC_CLK_TX, GMAC_CLK_TS Preconditions: s32ct, s32k358 Test Case ID (internal TC that caught the defect) optional: Ip_Clock_TC_FCT_0021 Observed behavior: GMAC_CLK_RX, GMAC_CLK_TX, GMAC_CLK_TS has wrong name in Clock_Ip_ReferencePoint Expected behavior: GMAC_CLK_RX, GMAC_CLK_TX, GMAC_CLK_TS be display in Clock_Ip_ReferencePoint Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-142732	Bug	[MCU][S32K3x4]Investigate the erata ERR050583 Detailed description (how to reproduce it): S32K3x4 0P55A_1P55A Errata Rev12_Dec_2023.pdf have the erata "ERR050583: MC_CGM: Functional reset during Clock dividers update can result in a Power on Reset sequence" need to investigate and implement if need Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: in S32K3x4 0P55A_1P55A Errata Rev12_Dec_2023.pdf have erata maybe impact to Mcu driver need to be investigate

ID	Subtype	Headline and Description
		Expected behavior: investigate new erata and implement Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-142927	Bug	[ADC] DSPSS gain and offset parameter has wrong range value Detailed description (how to reproduce it): DSPSS gain and offset parameter has wrong range value. The current version of the drivers has the limits for the gain and offset parameter set to: Gain: 0-65535 Offset: 0-4294967295 !image-2024-08-05-16-33-02-906.png|width=844,height=86! The actual range should be following: Gain: 32768 to 32767 Offset: 214748368 to 2147483647 !image-2024-08-05-16-33-25-774.png|width=763,height=169! Also same situation on S32DS. Preconditions: Driver tag: ADC_630 Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011_cfg10 Observed behavior: Have warning in report Expected behavior: Correct range of parameters Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-143301	Bug	[MCU] Wrong implementation of the function Ram_Ip_GetRamState Detailed description (how to reproduce it): Sequence of the function is as the below Check if clock status for STCU2 is enabled. If not, enable it The issue here is that if STCU2 is enabled failed => Timeout occured => the code below enabling STCU2 clock should not be implemented => Add if(!TimeoutOccured) => continue implementing !image-2024-08-07-14-51-18-693.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Wrong implementation of the function Ram_Ip_GetRamState Expected behavior: Correct implementation of the function Ram_Ip_GetRamState Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-143342	Bug	[PORT][Multicore parallel] Port_Ipw_SetGpioDirChangeability does not work properly when running on 2 cores at the same time Detailed description (how to reproduce it): Configure two pins on the same port (pin0 and pin1) pin0 runs on core 0 pin1 runs on core 1 call Port_SetPinMode(pin0 ,PORT_GPIO_MODE); Port_SetPinMode(pin1 ,PORT_GPIO_MODE);

ID	Subtype	Headline and Description
		E.g: pin0 mscr52, pin1 mscr54 on S32K388 Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Port_TS_200 Observed behavior: !image-2024-08-07-16-49-29-480.png! test passed on iar, ghs, diab compiler but failed on gcc compiler the value of Port_lpw_au16GPIODirChangeability is incorrect when running on 2 cores at the same time Each element of the above array represents 1 port, each bit of that element corresponds to 1 pin. When running this function at the same time on 2 cores: If the two pins are on two different ports, the driver will modify different elements of the Port_lpw_au16GPIODirChangeability array => no conflicts will occur If the two pins are in the same ports, the driver will modify the same element of the Port_lpw_au16GPIODirChangeability array => the value may be overwritten => failed the test Expected behavior: Port_lpw_SetGpioDirChangeability works correctly when running on 2 cores at the same time Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-143385	Bug	[pwm] Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid. In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached. Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. Otherwise, we can use this command to enable case sensitive for all created subfolders and no need to renew them: "(Get-ChildItem foldername Recurse Directory).Fullname ForEach-Object {fsutil file setCaseSensitiveInfo "$_" enable}" # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-143750	Bug	[ETH] Compare code gen between EB and CT Detailed description (how to reproduce it): Compare code gen between EB and CT. See photos to see the difference !image-2024-08-09-16-51-23-857.png! !image-2024-08-09-16-51-46-802.png!

ID	Subtype	Headline and Description
		!image-2024-08-09-17-01-26-414.png! Preconditions: Compare generated code beetwen EB and CT on K388 Test Case ID (internal TC that caught the defect) optional: Eth_TS_203 Eth_TS_204 Eth_TS_003 Observed behavior: Different between EB and CT generated filed for K388 Expected behavior: No different Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-143777	Bug	[ADC] Generation of some defines in precompile files is based on variant-aware nodes Detailed description (how to reproduce it): Need to check all defines which generated in precompile files but value obtained from variant-aware nodes (E.g: CTU_IP_FIFO_DMA_RAW_EN or AdcGroup_0_AdcChannel_1 symbolic names) Preconditions: Using test with VARIANT_NO > 1 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: the CTU_IP_FIFO_DMA_RAW_EN might be = OFF for all variants (if last variant in EB or first variant in CT = false) Expected behavior: defines which generated in precompile file shouldn't obtain value from variant-aware node Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-143857	Bug	[MCU] Unperfect implementation of LVSC register configuration Detailed description (how to reproduce it): PMC for K388 and K389 Power_Ip_PMC_PowerInit and Power_Ip_PMC_VoltageErrorIsr configures the LVSC register, it clears the reserved bitfields. The default values of the reserved bitfields in LVSC register are undefined reset values by default and should remain as they are. !image-2024-08-12-11-32-00-168.png!!image-2024-08-12-11-32-27-085.png!!image-2024-08-12-11-32-55-022.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Unperfect implementation of LVSC register configuration Expected behavior: Correct the implementation of LVSC register configuration Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Implement read-modify-write register
ARTD-144240	Bug	[I2S]: EBT/DS Comparison: Separate Rx/Tx enabling and Separate Rx/Tx Callbacks not available in EBT Detailed description (how to reproduce it): Mismatch between ebt and ds code generation for flexio when RX is disable. In EBT code generation, rx's pin alway plus 1, rx data line is enable or disable though. But in DS code generation, rx's pin is plus 1 when rx data line is enable and rx's pin is 0 when rx data line is disable. Preconditions: RX is disable i2s over Flexio Test Case ID (internal TC that caught the defect) optional: COT_004_cfg2

ID	Subtype	Headline and Description
		Observed behavior: Mismatch between ebt and ds code generation for flexio when RX is disable !screenshot-1.png|thumbnail! Expected behavior: Code gen is the same between EBT and DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-144263	Bug	[PORT]GPI pins need to disable the options dedicated for output mode Detailed description (how to reproduce it): For S32G2 and AS32G3, there are certain number of pins which can only work in input mode, namely GPI pins. For example, the PA_10 (MSCR10, GPI[10]) in SIUL2_0, PJ_02 (MSCR146, GPI[146]) in SIUL2_1. Please refer to the attached S32G2_IOMUX.xlsx in S32G2 RM and S32G3_IOMUX.xlsx in S32GG3 RM respectively for more details. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The dedicated attributes of GPIO pin output mode, i.e. PortPin Ode, PortPin Drection, PortPin Output Slew Rate are configurable for GPI pins. Expected behavior: The dedicated attributes of GPIO pin output mode should not be configurable for GPI pins. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Disable the configuration items of the dedicated attributes of GPIO pin output mode when GPI pin is being configured.
ARTD-145593	Bug	[memacc] Locking mechanism needs rework part 2 - Follow up Detailed description (how to reproduce it): The locking mechanism needs rework part 2 to address the comments in the pull request: [Pull Request #301: [ARTD-112686] Rework the locking mechanism NXP Bitbucket|https://bitbucket.sw.nxp.com/projects/ARTD/repos/memacc/pull-requests/301/overview] Merge all updated parts into the develop branch. Preconditions: Refer to the ticket: ARTD-112686 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Operations from other address areas are possible during the lock. Expected behavior: HW device should not accept any jobs until unlock (ASR req) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-145689	Bug	[MemAcc]: Job with higher priority executed after lower priority job in state retry Detailed description (how to reproduce it): job with lower priority in state retry call job with higher priority call main func Preconditions: job with lower priority in state retry Test Case ID (internal TC that caught the defect) optional: MemAcc_TC_334 Observed behavior: job with higher priority executed after lower priority job Expected behavior: job with lower priority executed after higher priority job Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-145817	Bug	[MEMACC] Memory section for _SEC_VAR_INIT_UNSPECIFIED is missing from MemAcc_Bswmd.arxml - Follow up Detailed description (how to reproduce it): In the file ..\MemAcc_TS_T31D62M10I0R0\generate_PB\src\MemAcc_PBcfg.c below mention section is define, [!IF "node:value(AutosarExt/MemAccMulticoreType3Support)='true'"!][!// [!VAR "MemAccSection" = "'_SEC_VAR_SHARED_INIT_UNSPECIFIED_NO_CACHEABLE'"!][!// [!ELSE!][!// [!VAR "MemAccSection" = "'_SEC_VAR_INIT_UNSPECIFIED'"!][!// [!ENDIF!][!// Consider merging all changes from this pull request into the develop branch: [Pull Request #300: [ARTD-141909] Memory section for SEC_VAR_INIT_UNSPECIFIED is missing from MemAcc_Bswmd.arxml NXP Bitbucket|https://bitbucket.sw.nxp.com/projects/ARTD/repos/memacc/pull-requests/300/overview] Observed behavior: Memory Section for "_SEC_VAR_INIT_UNSPECIFIED" is missing from MemAcc_Bswmd.arxml. Expected behavior: Memory Section for "_SEC_VAR_INIT_UNSPECIFIED" should be present in MemAcc_Bswmd.arxml. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update MemAcc_Bswmd.arxml to contain memory Section for "_SEC_VAR_INIT_UNSPECIFIED.
ARTD-146330	Bug	makefile MACRO DMULTIPLE_CORE should be defined in the ASOPT instead of CCOPT makefile MACRO DMULTIPLE_CORE should be defined in the ASOPT instead of CCOPT,otherwise the MACRO is not effective in the startup_cm7.s file. Addtionally, if ggdb3 can be added, then when we debug the elf in the S32DS, the source .s file can be referred. without ggdb3 added, we can only see the assembly code when debugging an elf file. !image-2024-09-04-16-23-25-530.png|thumbnail! !image-2024-09-04-16-25-28-220.png|thumbnail! !image-2024-09-04-16-29-58-977.png|thumbnail! !image-2024-09-04-16-34-02-690.png|thumbnail!
ARTD-146887	Bug	[SAI] SAI receiver loses data when switching buffers. Detailed description (how to reproduce it): When the SAI IP driver fills the data buffer, it stops the reception and only then calls the user callback. Also, if the user calls Sai_Ip_Receive in the callback, the function starts by resetting the Rx FIFO and the internal receiver logic. As a result, at least one frame will be lost. Customer usecase: IPV layer SAI0 with 4 lines with DMA 10MHz Preconditions: SAI receiver continuously receives data. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: At least one frame is lost when changing the Rx buffer. Expected behavior: Data should be received without errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: I think the best solution would be to add two new functions which the user can call from the callback to replace the Rx / Tx buffers. The driver would call the callback first, and only stop transmission/reception if the user did not provide a new buffer. These new functions should not reset the FIFO and be as fast as possible, which will also help improve performance, because currently the driver can't keep up with the data in interrupt mode for a bit clock of 10 MHz. For reference I attach the changes I did locally to fix the data loss issue. I included the original file for comparison.
ARTD-147678	Bug	[ARTD][GMAC] Can not transmit preemptable frame Detailed description (how to reproduce it): When enable frame preemption on S32K396, the frame can transmit, but in the receive side there are nothing. Preconditions:

ID	Subtype	Headline and Description
		Enable internal loopback mode. Enable frame preemption. !image-2024-09-18-10-39-53-431.png! !image-2024-09-18-10-40-13-996.png! Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Run test on loopback mode, transmit only 1 preemptable frame. Didn't get preemptable frame on the receive side. !image-2024-09-18-10-46-09-499.png! Expected behavior: Can transmit and receive both express and preemptable frames. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A.
ARTD-148314	Bug	[MCU]Lacks PRAMC2 support Detailed description (how to reproduce it): In driver code, Lacks PRAMC2 support !image-2024-09-24-10-39-01-768.png! In RM have mentioned !image-2024-09-24-10-39-50-263.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Lacks PRAMC2 support Expected behavior: PRAMC2 is supported by driver Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-149170	Bug	[SAF8X R41 3.0.0] [MemAcc] Error when importing the ECPD file on EB Tresos _*Detailed description (how to reproduce it): An error message appears when importing the ECPD file, see the image bellow: !image-2024-10-01-10-25-05-770.png! Preconditions: MemAccMulticoreType1Support = FALSE Using the .ECPD file instead of .XDM file Test Case ID (internal TC that caught the defect) optional: MemAcc_TS_COT_006 Observed behavior: Appear an error message and can't generate the code Expected behavior: Generated the code without any issue Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-149535	Bug	[PORT] Compilation failed when selecting IGF and TSPC on multivariant configuration Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Create 3 loadable variant configurations on configurator (EBT or S32CT) as below (for more detail: please check the attachment files): VS0: the node IGF_FGEN: enable VS1: the node IGF_FGEN: disable VS2: the node IGF_FGEN: disable Generate the code with above configurations Compile the code Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There's an error presented at the files Port_VS_0_PBcfg.c, Port_VS_1_PBcfg.c and Port_VS_2_PBcfg.c because the global variables aIgf_InitConfigArr_VS_0, aIgf_InitConfigArr_VS_1 and aIgf_InitConfigArr_VS_0 have not declared yet Expected behavior: Please update the generated code for IGF_NUM_OF_CHANNELS_CONFIG and IGF_PORT_CONFIG_PB/ IGF_PORT_CONFIG_[!"text:toupper(.)"!]_PB in the file Igf_Port_Ip_Cfg.h when IGF is enabled on each variant configuration are not the same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-149656	Bug	[spi] Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid. In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached. Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. Otherwise, we can use this command to enable case sensitive for all created subfolders and no need to renew them: "(Get-ChildItem foldername Recurse Directory).Fullname ForEach-Object {fsutil file setCaseSensitiveInfo "$_" enable}" # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-150835	New Feature	[GMAC][IMPLEMENTATION] [Eth, RTD] S/G support for NETC, GMAC, transparent to AUTOSAR API CR description:_* GM team has asked for an extension of the AUTOSAR buffer model for the Eth interface to improve the memory usage under Eth traffic of mixed size with a bias toward small frames. The typical AUTOSAR approach to Eth frame buffering is to allocate buffers large enough for the MAX Eth frame size. However, if the large frames are uncommon this leads to a low usage of the reserved memory.

ID	Subtype	Headline and Description
		The ask is to support buffers smaller than the frame size, implicitly supporting scatter/gather in the Eth drivers, while maintaining compatibility with the AUTOSAR APIs. The technical proposal is to: decouple the max frame size from the buffer size, allocate small buffers (GM is planning to do 128B buffers), on Tx: introduce logic in the driver to reserve multiple consecutive buffers for frames larger than size of one buffer. The driver returns a single pointer on buffer request but internally tracks multiple buffers allocated for this Tx. descriptor > buffer association is fixed, in case of frames using multiple buffers Tx is done using multiple descriptors. to address the wrap-around case at the end of the ring, we should allocate additional buffering at the end, allowing a large frame to fit in the last (extended) buffer in the ring. Tx clean-up should also account for S/G and ensure that all buffers of a frame have been transmitted. on Rx: enable S/G in HW. frames in the first part of the ring will be contiguous, driver will have to track multiple Rx buffers / descriptors but present a single pointer to the upper layers. frames at the end of the ring may be fragmented, split between buffers and the end and at the beginning of the ring. These must be linearized by the driver could be copied to a single separate large buffer, or preferably linearized in place using additional space at either the beginning or the end of the ring. GM is planning to allocate up to 16KB of memory for a BD ring. Buffer size is expected to be 128B. Max frame size should be assumed <= 1536 (128*12). Tx extra buffering at the end of the ring should be 1408B (1536-128). An equivalent buffer should also be allocated at beginning (or end) of Rx ring for linearization. This is required for both S32N5 / ENETC and S32K3 / GMAC. Reason for this change: improve mem usage for Eth I/O with traffic of mixed size, with a bias toward small frames. Benefit: reduce memory waste for applications that send/receive mostly small Eth frames plus occasional large frames. Onetime CR/Strategic CR: strategic Use-case: Eth I/O with traffic of mixed size, with a bias toward small frames. HW documentation reference (as applies): ENETC BG HW/Application Engineer contact (as applies): [text placeholder]_ Note: relevant documents to be attached to the ticket.
ARTD-151004	Bug	[ETH][GMAC] S32K328 does not support same features as S32K358 Detailed description (how to reproduce it): S32K328 mentions that RGMII is not supported while it should be since is the same as S32K358, also when adding FreeRTOS, there is no definition for S32K328, so it does not compile. Fix for the S32K328 should be added, or supporting the same features as S32K358 with the appropriate linker file. There is no difference in the peripheral support in the S32K328 against the S32K358 !image-2024-10-10-18-02-22-749.png|thumbnail! !image-2024-10-10-18-03-04-628.png|thumbnail!
ARTD-151027	Bug	[ADC] Adc_GetStreamLastPointer using wrong GroupIndex with ReOrder feature Detailed description (how to reproduce it): Wrong the address of Pointer to result buffer pointer for case config: AdcEnableGroupStreamingResultReorder = true. GroupIndex = 1 (other than 0). Channel count groupIndex 1 other channel count groupIndex 0. AdcEnableSetChannel = false.

ID	Subtype	Headline and Description
		In group config AdcStreamResultGroup = true. In test case call Adc_GetStreamLastPointer() function. Preconditions: Configuration as described above. Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0116 (Adc_TS_025) Observed behavior: Incorrect the address of Pointer to result buffer pointer when use Adc_GetStreamLastPointer() Expected behavior: Correct the address of Pointer to result buffer pointer when use Adc_GetStreamLastPointer() for this case. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-151692	Bug	[pwm] Etpu resources in PWM plugin are incorrect/obsolete The eTPU resources in PWM plugin are incorrect/obsolete. This issue is related to eTPU relevant variants eTPU relevant variants/phantoms [Pwm_s32k396_mapbga289.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k396_mapbga289.txt] [Pwm_s32k396_lqfp176.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k396_lqfp176.txt] [Pwm_s32k394_mapbga289.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k394_mapbga289.txt] [Pwm_s32k394_lqfp176.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k394_lqfp176.txt] [Pwm_s32k366_mapbga289.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k366_mapbga289.txt] [Pwm_s32k366_lqfp176.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k366_lqfp176.txt] [Pwm_s32k364_mapbga289.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k364_mapbga289.txt] [Pwm_s32k364_lqfp176.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/browse/specific/S32K3XX/resource/Pwm_s32k364_lqfp176.txt] The value of _Pwm.EtpuChanBaseAddressStart is obsolete, it should be 0x406884C0 (valid for S32K3_ETPU_SW_4.7_1.0.1_HF01) The actual value can be found in Etpu_CDD resource: [Etpu_s32k396_mapbga289.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/etpu/browse/specific/S32K3XX/resource/Etpu_s32k396_mapbga289.txt] (_Etpu.ChanBaseAddressStart_) The S32K36X phantoms contain 16 channels instead of 32 The value Pwm.EtpuChannels should be changed from 32 to 16 The value Pwm.EtpuChannel.List should be reduced (Engine_A/B_Channel_0 Engine_A/B_Channel_15) For other variants without eTPU HW, all .List values should be empty (not sure if empty list is correct here) Whenever the Pwm.EtpuChanBaseAddressStart is updated in resources, it affects the Etpu PWM channels configuration CPBA values must be recalculated within existing .xdm files for developer tests and example code: Pwm/PwmEtpu/PwmEtpuChannels/Channel Base Address !image-2024-10-17-11-20-39-039.png|width=447,height=193! Additionally, there would be great to setup the communication channel with eTPU team for passing information when eTPU changes will require modification of resources typically EtpuChanBaseAddressStart is often changed when new eTPU FW is integrated into Etpu_CDD.
ARTD-152303	Bug	[LIN] Lin_LinTrcv_FrameTransfer_S32M276 example does not respect the configured baudrate for the Lin channel Detailed description (how to reproduce it): 1) Open the Lin_LinTrcv_FrameTransfer_S32M276 and run it on board 2) Check the baudrate of the Lin signal on the bus Preconditions: RTD version: SW32K3_S32M27x_RTD_R21-11_5.0.0 Observed behavior: The configured baudrate for the Lin channel is 9600: !image-2024-10-21-15-55-38-601.png! By using a Peak PLIN device with the auto-detect baudrate functionality, I noticed that the actual baudrate of the signal was doubled (19200). !image-2024-10-21-15-59-30-613.png! This behaviour was reproduced for other configured baudrates, each time the detected baudrate was doubled. Expected behavior:

ID	Subtype	Headline and Description
		The detected baudrate should have been 9600, same as the one configured. Proposed solution optional: This issue seems to be resolved by changing the clock reference of the Lin channel from AIPS_SLOW_CLK to AIPS_PLAT_CLK. !image-2024-10-21-16-06-16-290.png!
ARTD-152633	Bug	The K3 GMAC_TS_CLOCK of Mcu clock configuration is always 0 in EB tresos Detailed description (how to reproduce it): [Open the GMAC_TS_CLOCK configure page in EB 29.0 of Mcu module clocking configuration, will find its always 0.Which affects the Eth GMAC Timestamping capturing: !image-2024-10-24-11-17-42-518.png! !image-2024-10-24-11-14-54-975.png!! image-2024-10-24-11-17-59-391.png!] Preconditions: [Using EB tresos tool to configure it. There is no problem when using S32DS .mex tool.] Test Case ID (internal TC that caught the defect) optional: [SFDC:#00660303] Observed behavior: [GMAC_TS_CLOCK always 0 whatever reference clocking is.] Expected behavior: [It changes to the right value accordingly.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-152778	Bug	[S32K3XX][LPSPI] PCS continuous mode is not working for halfduplex receive mode Detailed description (how to reproduce it): Set Lpspi_Ip mode to 4 wire half duplex mode and enable "Keep CS asserted". This does not have any effect. A workaround has been implemented to set the CONTC bit on every transfer except for the first one. !image-2024-10-25-10-09-54-230.png! Preconditions: Set Lpspi_Ip mode to 4 wire half duplex mode and enable "Keep CS asserted" Test Case ID (internal TC that caught the defect) optional: Observed behavior: Keep CS asserted does not have any effect. Expected behavior: Continuous mode should be available for Lpspi 4 wire half duplex mode. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-153524	Bug	CAN Enhanced FIFO lost frame workaround. Hi RTD team, Recently we found a CAN hardware bug and it is confirmed by CAN IP design team. The description of this bug shows below: FlexCAN Rx enhanced FIFO dropped frame silently when there is a writing to C&S code of some specific TxMBs in a very short time window. This hardware bug appears differently depend on timestamp feature. With Timestamp enabled, we see this problem if TX request is generated around EOF 6th bit. With Timestamp disabled, we see this problem if TX request is generated around IFS 1st bit. And most important thing is this hardware bug happened in some specific TxMBs. If we use below TxMBs, this bug will always happen in previous mentioned time window (tested in {*}S32K312{*}): MBDSR*|*CAN TX frame Payload length*|*MAXMB+1 (Total MBs)*|*Failing MBs 0|8 bytes|64|0,2,10,12,20,22,30,32,40,50,60 1|16 bytes|42|0,2,10,12,20,22,30,32,40 2|32 bytes|24|0,2,10,12,20,22 3|64 bytes|14|0,2,10,12 This hardware bug happened not only in all K3 series, but also in S32Z, S32N, S32R, etc.

ID	Subtype	Headline and Description
		We get the workaround from the design team is that if we do not use the erroneous MBs, this issue will not happen. So, for the workaround provided by design team. Could we modify driver code or change AutoSAR & non-AutoSAR configuration MBs to avoid using the erroneous MBs? For the detail of this hardware bug and reproduce project, pls find the attached PPT. And pls feel free to discuss with me how to implement this workaround.
ARTD-153946	Bug	[S32K3XX] Undefined reference __CORE3_VTOR while building K344 examples While building a set of examples for K344, the error "undefined reference to CORE3_VTOR" is encountered: see build_error_print_screen This is applicable for all compilers Observed behavior: build error when building K344 examples for crypto driver Expected behavior: Build passed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add highlighted line from attached print screen linker_flash_s32k344_printscreen,
ARTD-154141	Bug	[SPI][S32K3]: Test build fails when enabling DmaContMemTransfer with Post-Build and Multipartition configurations Detailed description (how to reproduce it): There is an error at build step when configuring Post-build and Multipartition with DmaContMemTransfer in testing. !image-2024-11-06-10-33-54-280.png! !image-2024-11-06-10-34-41-025.png! !image-2024-11-06-10-35-55-266.png! Generated files: !image-2024-11-06-10-38-06-167.png! !image-2024-11-06-10-39-53-029.png! !image-2024-11-06-10-40-12-358.png! Report failed: !image-2024-11-06-10-42-37-342.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Spi_TC_COT_0001 Observed behavior: Test build fails when enabling DmaContMemTransfer with Post-build and Multipartition configurations Expected behavior: Test must be passed when DmaContMemTransfer enabled with Post-build and Multipartition configurations. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-154308	Bug	[RTD_TRAIN_PILOT][LIN] Different number arguments of Flexio_Lin_Ip_IrqHandler function at source and header Detailed description (how to reproduce it): [By tag LIN_144, missing argument uint8 HwInstance at header file Flexio_Lin_Ip.c: !image-2024-11-07-14-41-19-288.png! Flexio_Lin_Ip_Irq.h: !image-2024-11-07-14-41-37-984.png! Beside that, different type of variable {*}Base{*}[] ({*}FLEXIO_Type }}) when assign to Flexio_Lin_Ip_apxBases (const FLEXIO_Type) !image-2024-11-07-15-10-56-451.png!

ID	Subtype	Headline and Description
		] Preconditions: [Use FlexIO] Test Case ID (internal TC that caught the defect) optional: [Lin_TS_100] Observed behavior: [Build fail due to incompatible function !image-2024-11-07-14-44-47-186.png!] Expected behavior: [N/A] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Update argument at header file: void Flexio_Lin_Ip_IrqHandler(uint8 ShifterIndex, uint8 ShifterMaskFlag, uint8 ShifterErrorMaskFlag); > void Flexio_Lin_Ip_IrqHandler({*}uint8 HwInstance{*}, uint16 ShifterIndex, uint16 ShifterMaskFlag, uint16 ShifterErrorMaskFlag)]
ARTD-154435	Bug	Function Adc_Sar_Ip_SetUserGainAndOffset has wrong guard Detailed description (how to reproduce it): The function Adc_Sar_Ip_SetUserGainAndOffset has a wrong guard in Adc_Sar_Ip.h/c Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compilation error if ADC_CALIBRATION is ON and ADC_SAR_IP_USER_OFFSET_GAIN_REG_AVAILABLE is OFF This is caused because the callee of Adc_Sar_Ip_SetUserGainAndOffset is under ADC_CALIBRATION guard. Expected behavior: No compilation error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: the #if ADC_SAR_IP_USER_OFFSET_GAIN_REG_AVAILABLE used in Adc_Sar_Ip.h/.c should be replaced with ADC_CALIBRATION or with an logical OR with the actual ADC_SAR_IP_USER_OFFSET_GAIN_REG_AVAILABLE.
ARTD-154948	Bug	[Mem_ExFls] Bswmd file should not have MemMainFunctionPeriod configurable Detailed description (how to reproduce it): Mem_43_EXFLS_TimingEvent_MainFunction field in the Bswmd is not generated correctly. Preconditions: Customer wants to use the Bswmd for MainFunction scheduling. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Issue with the bswmds Expected behavior: No issue Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Investigate and update the Bswmd to use "<PERIOD>0</PERIOD>" for the Mem_43_EXFLS_TimingEvent_MainFunction Investigate if the names of the fields are corect
ARTD-158242	Bug	[PORT] Wrong memory section put for Port_aUnusedPads array Detailed description (how to reproduce it): Wrong memory section is put for Port_aUnusedPads. Now is PORT_START_SEC_CONFIG_DATA_16 but it should be PORT_START_SEC_CONFIG_DATA_UNSPECIFIED Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA

ID	Subtype	Headline and Description
		Observed behavior: Wrong memory section is put for Port_aUnusedPads Expected behavior: Correct memory section is put for Port_aUnusedPads Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Correct the driver with the section memory

ARTD-158249	Bug	[S32K3XX][LPSPI] Half duplex receive over DMA not working
		
		Detailed description (how to reproduce it):
		Configure SPI for halfduplex mode, 8 bit data width, 4 wire mode (transfer 4 bits). Activate DMA and use Lpspi_Ip_AsyncTransmitHalfDuplex in receive mode. The first transfer works, but then the DMA configuration gets overwritten in Lpspi_Ip_TxDmaConfig and transfers stop working.
		
		Observed behavior:
		
		The problem is in the driver flow in Lpspi_Ip.c:
		
		Line 1222: if ((LPSPI_IP_HALF_DUPLEX_RECEIVE == State->ExternalDevice->DeviceParams->TransferType) && (FALSE == State->IsPreChanneHalfDuplexIRxMode))
		
		After the first halfduplex transfer, this condition is not met and the else branch overwrites the DMA configuration.
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		if (LPSPI_IP_HALF_DUPLEX_RECEIVE == State->ExternalDevice->DeviceParams->TransferType)
		{
		if(FALSE == State->IsPreChanneHalfDuplexIRxMode)
		{

ARTD-158660	New Feature	[PORT][DIO] Add constraint when adding both Port and Siul2_Port component in S32DS
		
		NewWorkDescription:
		Starting from the inquiry here: https://jira.sw.nxp.com/browse/ARTD-142138 there was a compile error when using both Port and Siul2_Port component but the error was not clear.
		
		We can improve this to have a better message in configuration saying what exactly the user needs to do.
		
		Requirement source:
		FAE on behalf of customer request
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		
		Proposed solution optional:
		In Port_Cfg.h or any generated files in S32DS:
		
		for each (var componentInstanceConfig in ComponentConfigurationsList)
		{
		if (componentInstanceConfig.getComponent().getId() == "Siul2_Port")
		{
		scriptApi.logError("Please remove either Port or Siul2_Port component ")
		}
		}

ARTD-159970	Bug	[I2c] Missing support ERR052121 for S32K311 S32M276 S32K389 S32K388 Detailed description (how to reproduce it): In the new errata file on S32K3XX release, I2c driver have some derivatives does not support ERR052121 S32K311_0P98C: ERR052121 Not support S32M276_P98C+P69K: ERR052121 Not support S32K389_<mask_id>: ERR052121 Driver does not support S32K389 derivatives => Not support S32K388_0P39J/0P24N: ERR052121 Not support Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In the new errata file on S32K3XX release, I2c driver have some derivatives does not support ERR052121{*}{*} _**_ Expected behavior: Support errata for all off the derivatives Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: N/A
ARTD-159985	Bug	[Mem_ExFls][S32K3XX] Wrongly handled memory mapping-Static variables in function scope Detailed description (how to reproduce it): [Update 14Nov2024: to item 2). See attached all Port Config Files The values IDM_HW_VARIANT_LOW or IDM_HW_VARIANT_HIGH refer to different packages of the K3 SOC (sub-derivatives). High variant uses the derivative s32k322_hdqfp172 Mid and Low variants use the derivative s32k322_hdqfp100 Update 8Nov2024: to item 4) subitem 3). customer confirms raised the point is not valid > Swt_Ip_apCallbackPtr is properly wrapped with WDG_START/STOP_SEC_VAR_CLEARED_UNSPECIFIED. to item 4): Variable: Emios_Ip_paxBase is used in both: Emois_Mcl_Ip.c and Emois_Mcl_Ip_Irq.c in ..eclipse\plugins\Mcl_TS_T40D34M20I0R0\src. Apparently the following extern declaration: !image-2024-11-08-18-48-46-553.png! Should be wrapped with the same allocation keywords as in case of the definition: !image-2024-11-08-18-49-05-108.png! So MCL_START/STOP_SEC_VAR_INIT_UNSPECIFIED_NO_CACHEABLE. Wrongly handled memory mapping 1) Static variables in function scope Overall Sw requirement of the customer: !image-2024-09-03-07-59-57-045.png! RTD use cases as such encountered: Static variables in function in MCAL Gpt driver source code Gpt_GetTimeElapsed::returnHwChannelInfo Gpt_StopTimer::returnHwChannelInfo Static variables in function in MCAL Mcu driver source code Clock_Ip_SetCmuFcFceRefCntLfrefHfref::Hash Clock_Ip_CgmXPcfsSdurDivcDiveDivs::Hash Clock_Ip_CallEmptyCallbacks::FunctionWasCalled Clock_Ip_ClockInitializeObjects::Clock_Ip_bObjectsAreInitialized Power_Ip_MC_RGM_ResetDuringStandby::StandbyResetStatus Crypto: Crypto_Hse_PushJobsFromQueuesToHse::u32ObjectCounter 2) Variables that are not wrapped with allocation keywords RTD use cases as such encountered: Port: gu8_port_NumberOfConfiguredPins in Port_Cfg.c 3) Variables not properly wrapped with allocation keywords RTD use cases as such encountered: # GPT_START_SEC_CONFIG_DATA_UNSPECIFIED wraps variable and not a const in generated GPT file: Gpt_Ipw_PBcfg.c # Wkpu_Ip_NMIConfig_PB (Icu) is wrapped by CONST allocation keyword: !image-2024-09-03-08-06-10-544.png! 4)* *Mixing variables of different init characteristics under same keyword The problem is that CLEARED init policy is used for DATA that is zero initialized explicitly in code and at the same the same init policy is used for DATA that is not initialized explicitly in code and so producing a linker error that C-objects of different init characteristics are part of the same data block: !image-2024-09-03-08-07-12-657.png! There is another similar case: PORT_START_SEC_VAR_CLEARED_UNSPECIFIED_NO_CACHEABLE Variable Swt_Ip_apCallbackPtr shall be wrapped by NOINIT allocation keyword: !image-2024-09-03-08-07-47-396.png! variable Emios_Ip_paxBase shall be wrapped by NOINIT allocation keyword 5) Mixing allocation keywords for the same variable

ID	Subtype	Headline and Description
		Slightly different allocation keywords are used for same variables.: Wdg_au32InstanceCoreUsed wrapped by WDG_START_SEC_CONFIG_DATA_32 in .h files and by WDG_START_SEC_CONFIG_DATA_UNSPECIFIED in .c files Wdg_au16CfgInitialTimeout and other variables wrapped by WDG_START_SEC_CONFIG_DATA_16 in .h files and by WDG_START_SEC_CONFIG_DATA_UNSPECIFIED in .c files] Preconditions: [NTR] Test Case ID (internal TC that caught the defect) optional: [NTR] Observed behavior: [see above] Expected behavior: [1) static variables must be moved to file static scope 2) /3/ variables to be properly wrapped with allocation keywords 4) do not mix variables of different init characteristics under same keyword 5) Do not mix allocation keywords for the same variable Question: Is that fixed in RTD version 4.0 P24 which is planned for Series production?] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [see above]
ARTD-160201	Bug	[MCU] FXOSC bypass bit(FXOSC_CTL[OSC_BYP]) will not be generated appropriately Description: SWS reported that FXOSC Bypass configuration in McuFXOSC will not be applied to generated source code. As you can see in the figure below, even when FXOSC Bypass's checkbox is cleared, XOSC bypass option in Clock_I_PBcfg.c will be 0. #if CLOCK_XOSCS_NO > 0U { FXOSC_CLK, / Clock name associated to xosc / 40000000U, / External oscillator frequency. / 1U, / Enable xosc. / 157U, / Startup stabilization time. / 0U, / XOSC bypass option / This value is always 0 0U, / Comparator enable / 12U, / Crystal overdrive protection / }, Proposal solution: Update the code(By*P*ass to By*p*ass) of in the file Clock_Ip_RegOperations.m from: [!MACRO "GetXoscBypass","Name"![!// [!NOCODE!] [!VAR "capitalName" = "text:replace($Name,substring($Name,2),text:tolower(substring($Name,2)))"!] [!VAR "bypassPath" = "concat('Mcu',$Name,'/Mcu',$capitalName,'ByPass')"!] to: [!MACRO "GetXoscBypass","Name"![!// [!NOCODE!] [!VAR "capitalName" = "text:replace($Name,substring($Name,2),text:tolower(substring($Name,2)))"!] [!VAR "bypassPath" = "concat('Mcu',$Name,'/Mcu',$capitalName,'Bypass')"!]
ARTD-160673	Bug	[BASE] Syntax error in modules.h Detailed description (how to reproduce it): When Base module is generated it reports errors because of the implementation from modules.h file. !image-2024-12-11-09-46-28-790.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A

ID	Subtype	Headline and Description
		Observed behavior: Base module does not generate Expected behavior: Base module generates with success Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-160676	New Feature	[CRC][CRC32C]Update resource files to remaining platforms for support CRC32C polynomial NewWorkDescription: Update resource files to remaining platforms for support CRC32C polynomial with software mode, table mode, hardware mode (hardware mode only support on some platforms) Requirement source: RM for checking hardware mode support (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Adding/Updating these resources: Crc.Hardware.PolygExt.IsAvailable Crc.Hardware.Support32CastagnoliCalculation Crc.Hardware.Support64HardwareCalculation Crc.AutosarType.List Crc.NonAutosar.Crc32CMode.List Crc.Protocols.AllTypes.List Crc.Protocols.OnlyHardwareExtSupport.List
ARTD-161099	Bug	[ETH] All the timeouts used in code should be configurable Detailed description (how to reproduce it): For some specific boards, the hardcoded timeouts used in code as IPW_TIMEOUT_1MS_U32 should be configurable by user, as their board or setup might be different than the one used by NXP internal. Preconditions: Some of the existing timeouts are fixed. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: For some specific setups, there can be an issue having timeouts fixed. Expected behavior: Let the user the possibility to configure all the timeouts. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Let the user the possibility to configure all the timeouts.
ARTD-161473	Bug	[ADC] Compiler Directives #define 's are generating in single line in EB Tresos 29.7 NewWorkDescription: This issue only applicable on EB Tresos {color}*{color:#ff0000}29.7{color}*{color:#ff0000} (I know that curenlty we test on EB Tresos 29.0.0 so it is not an issue at this time) . Reported by Elektrobit The compiler directives #defines in generated files are coming in single line instead of next lines eg in ADC module (other modules as I2S, DPGA have the same issue), as shown below the macro ADC_SAR_IP_SELFTEST_ENABLED generated in same line continuously after ADC_SAR_IP_WDG_ENABLED: EB Input: This is basically the expected behavior: if AUTOSPACING is enabled and a command is at the end of a line (here, the IF/ELSE/ENDIF), the line-break gets removed. This did not change, but now this also works for included and macro files (which is probably the case here?). You can either add a [!CR!] the end of the line or add an empty line File: Adc_Sar_Ip_CfgDefines.h #define ADC_SAR_IP_ECH_ENABLED (STD_OFF) #define ADC_SAR_IP_JECH_ENABLED (STD_OFF) #define ADC_SAR_IP_EOCTU_ENABLED (STD_OFF) #define ADC_SAR_IP_EOC_ENABLED (STD_OFF) #define ADC_SAR_IP_WDG_ENABLED(STD_OFF)#define ADC_SAR_IP_SELFTEST_ENABLED(STD_OFF)#define ADC_SAR_IP_DEV_ERROR_DETECT(STD_OFF)#define ADC_SAR_IP_TIMEOUT_TYPE (OSIF_COUNTER_DUMMY) #define ADC_SAR_IP_TIMEOUT_VAL (3000UL)

ID	Subtype	Headline and Description
		Please consider this ticket in the future if we test on EB Tresos 29.7 Requirement source: N/A Proposed solution optional: In MCAL plugin., The files which are responsible for this macro generation (eg, I2s_RegOperations.m) need to updated as per shown below Current implementation : #define ADC_SAR_IP_DEV_ERROR_DETECT [!IF "AutosarExt/AdcSarIpDevErrorDetect"!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!] Proposed Update : #define ADC_SAR_IP_DEV_ERROR_DETECT ([!IF "AutosarExt/AdcSarIpDevErrorDetect"!]STD_ON[!ELSE!]STD_OFF[!ENDIF!])
ARTD-161649	Bug	Issue in Trgmux_Ip.c with User Mode Execution Detailed description (how to reproduce it): In the *TrigMux* source file, {{{}Trgmux_Ip.c{}}}, the customer encountered an issue that arises when enabling User Mode Execution. !image-2024-12-17-10-16-15-096.png! !image-2024-12-17-10-43-57-409.png! !image-2024-12-17-10-46-19-493.png! Preconditions: No issue Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: as Detailed description Expected behavior: No issue Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: !image-2024-12-17-10-55-45-196.png!
ARTD-162507	Bug	[ADC] Generation error when adding ADC component to S32CT project Detailed description (how to reproduce it): add adc in S32CT and generate code !image-2024-12-19-10-42-46-857.png! Preconditions: Add module adc in S32CT Test Case ID (internal TC that caught the defect) optional: All test S32CT Observed behavior: Test S32CT generate error Expected behavior: Test S32CT generate, build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-162650	Bug	[GDU][S32K1-S32M24x] CDD_Gdu_PBcfg.h has config struct macro when using PreCompile mode Detailed description (how to reproduce it): When configure GDU with PreCompile mode and number of variants less or equal to 1, there is a macro defined as GDU Ip config struct in CDD_Gdu_PBcfg.h file. !image-2024-12-20-10-33-20-356.png! The CDD_Gdu_PBcfg.h file shall be empty in this case. References: [AMNG-6443] [ALL_GENERAL] Missing extern definitions of config structures NXP JIRA

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: Gdu_TS_005 Expected behavior: The CDD_Gdu_PBcfg.h file shall be empty when VariantPreCompile configuration variant and variant no <=1 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-162671	Bug	[MCU] Wrong function definition convention Detailed description (how to reproduce it): CCOV tool cannot parse functions having wrong convention { need to be on a new line wrong convention !image-2024-12-20-14-14-29-625.png! correct convention !image-2024-12-20-14-14-42-176.png! It causes that a significant number of functions is reported as being not covered by test cases (CE_zero_percent) List of functions which have incorrect convention is listed in CE_zero_percent sheet in RTD_MCU_CodeCoverage_Summary (2).xlsx Pls check all functions in the driver and correct them Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Wrong function definition convention Expected behavior: Correct function definition convention Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-162747	Bug	[Mem_InFls][S32K3XX] Wrongly handled memory mapping-Static variables in function scope Detailed description (how to reproduce it): [Update 14Nov2024: to item 2). See attached all Port Config Files The values IDM_HW_VARIANT_LOW or IDM_HW_VARIANT_HIGH refer to different packages of the K3 SOC (sub-derivatives). High variant uses the derivative s32k322_hdqfp172 Mid and Low variants use the derivative s32k322_hdqfp100 Update 8Nov2024: to item 4) subitem 3). customer confirms raised the point is not valid > Swt_Ip_apCallbackPtr is properly wrapped with WDG_START/STOP_SEC_VAR_CLEARED_UNSPECIFIED. to item 4): Variable: Emios_Ip_paxBase is used in both: Emois_Mcl_Ip.c and Emois_Mcl_Ip_Irq.c in ..eclipse\plugins\Mcl_TS_T40D34M20I0R0\src. Apparently the following extern declaration: !image-2024-11-08-18-48-46-553.png! Should be wrapped with the same allocation keywords as in case of the definition: !image-2024-11-08-18-49-05-108.png! So MCL_START/STOP_SEC_VAR_INIT_UNSPECIFIED_NO_CACHEABLE. Wrongly handled memory mapping

ID	Subtype	Headline and Description
		1) Static variables in function scope Overall Sw requirement of the customer: !image-2024-09-03-07-59-57-045.png! RTD use cases as such encountered: Static variables in function in MCAL Gpt driver source code Gpt_GetTimeElapsed::returnHwChannelInfo Gpt_StopTimer::returnHwChannelInfo Static variables in function in MCAL Mcu driver source code Clock_Ip_SetCmuFcFceRefCntLfrefHfref::Hash Clock_Ip_CgmXPcfsSdurDivcDiveDivs::Hash Clock_Ip_CallEmptyCallbacks::FunctionWasCalled Clock_Ip_ClockInitializeObjects::Clock_Ip_bObjectsAreInitialized Power_Ip_MC_RGM_ResetDuringStandby::StandbyResetStatus Crypto: Crypto_Hse_PushJobsFromQueuesToHse::u32ObjectCounter 2) Variables that are not wrapped with allocation keywords RTD use cases as such encountered: Port: gu8_port_NumberOfConfiguredPins in Port_Cfg.c 3) Variables not properly wrapped with allocation keywords RTD use cases as such encountered: # GPT_START_SEC_CONFIG_DATA_UNSPECIFIED wraps variable and not a const in generated GPT file: Gpt_lpw_PBcfg.c # Wkpu_Ip_NMIConfig_PB (Icu) is wrapped by CONST allocation keyword: !image-2024-09-03-08-06-10-544.png! 4)* *Mixing variables of different init characteristics under same keyword The problem is that CLEARED init policy is used for DATA that is zero initialized explicitly in code and at the same the same init policy is used for DATA that is not initialized explicitly in code and so producing a linker error that C-objects of different init characteristics are part of the same data block: !image-2024-09-03-08-07-12-657.png! There is another similar case: PORT_START_SEC_VAR_CLEARED_UNSPECIFIED_NO_CACHEABLE Variable Swt_Ip_apCallbackPtr shall be wrapped by NOINIT allocation keyword: !image-2024-09-03-08-07-47-396.png! variable Emios_Ip_paxBase shall be wrapped by NOINIT allocation keyword 5) Mixing allocation keywords for the same variable Slightly different allocation keywords are used for same variables.: Wdg_au32InstanceCoreUsed wrapped by WDG_START_SEC_CONFIG_DATA_32 in .h files and by WDG_START_SEC_CONFIG_DATA_UNSPECIFIED in .c files Wdg_au16CfgInitialTimeout and other variables wrapped by WDG_START_SEC_CONFIG_DATA_16 in .h files and by WDG_START_SEC_CONFIG_DATA_UNSPECIFIED in .c files] Preconditions: [NTR] Test Case ID (internal TC that caught the defect) optional: [NTR] Observed behavior: [see above] Expected behavior: [1) static variables must be moved to file static scope 2) /3/ variables to be properly wrapped with allocation keywords 4) do not mix variables of different init characteristics under same keyword 5) Do not mix allocation keywords for the same variable Question: Is that fixed in RTD version 4.0 P24 which is planned for Series production?] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [see above]
ARTD-163105	Bug	[PORT] Resource for NotAvailableMscrs pins are missing some pins Detailed description (how to reproduce it): For example: resource file: Port_s32k342_hdqfp100.txt, the Port.Siul2Instance0NotAvailableMscrs is missing pin 39 and 121.

ID	Subtype	Headline and Description
		The formula for them is: Port.Siul2Instance0NotImplementedMscrs : pins that doesn't exist in CR column Port.Siul2Instance0NotAvailableMscrs : = Port.Siul2Instance0NotImplementedMscrs pins that doesn't exist in resource-column Preconditions: NA Test Case ID (internal TC that caught the defect) optional: any Observed behavior: not yet defined Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Review & Update resources
ARTD-163176	Bug	[MCU] Correct ORIGIN information for ECUC node in xdm and template Detailed description (how to reproduce it): Some ECUC node need has ORIGIN as AUTOSAR_ECUC, but it is M4_XDM_AR_MODULE_ORIGIN for some platforms. Example for K1: !image-2024-12-24-18-24-21-447.png|width=535,height=245! Please recheck all platforms for xdm and template file for all ECUC node Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Manually review Observed behavior: ORIGIN information is not correct Expected behavior: ORIGIN information is correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-163512	Bug	[MCU][Doc]: Wrong contents in the RTD_MCU_UM.pdf Detailed description (how to reproduce it): wrong contents in the RTD_MCU_UM.pdf version 5.0.0: !image-2025-01-02-10-04-45-512.png|width=516,height=145! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-163565	Bug	[UART] Incorrect description in FMEA file Detailed description (how to reproduce it): Uart_Deinit function has no return type following the requirement CDD_UART_00007 but in FMEA file No 3.1 line 21 and No 3.4 line 29 , Uart_Deinit function still require a return E_NOT_OK in case timeout error occured. !image-2025-01-02-15-08-02-814.png! !image-2025-01-02-15-08-54-484.png! Preconditions:

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: Uart_TC_WBT_0009 Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-163678	Bug	[Platform]S32K3xx-M27x] Wrong information in comment part of MPU configuration Detailed description (how to reproduce it): !_thumb_1595833.png|thumbnail! start/end addresses of cacheable mpu region do not map to current mpu configuration in Platform module. It should be updated to start address of int_sram region with cacheable_ram_size Preconditions: use package of [BLN_RTD_4.7_S32K3XX_S32M27x_4.0.0_P25|https://jira.sw.nxp.com/issues/?jql=project%3D%22ARTD%22%20AND%20%22Reported+Version%22%3D%22BLN_RTD_4.7_S32K3XX_S32M27x_4.0.0_P25%22%20ORDER%20BY%20priority%20ASC] Test Case ID (internal TC that caught the defect) optional: Static Review Observed behavior: wrong information of MPU configuration for cacheable mpu region Expected behavior: cacheable mpu region of comment part should map to current mpu configuration Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update comment part to correct current mpu region
ARTD-163854	Bug	[Pwm][Flexio][S32K3] Function used to validate parameter passed in Pwm_EnableNotification not correct Detailed description (how to reproduce it): Currently, Pwm driver has a condition in function Pwm_Ipw_ValidateNotification as bellow used to validate the type of edge notification passed in function Pwm_EnableNotification for Flexio Ipv: !image-2025-01-06-23-52-25-477.png|width=789,height=365! With this implementation, users can't use a type of edge notification if its corresponding option in node Flag Event response is configured on EBT > This doesn't make sense. For example: If FLEXIO_PWM_IP_IRQ_ON_RISING_EDGE is configured for node {*}Flag Event response{*}, then user can't use the type of rising edge notification by calling Pwm_EnableNotification: !image-2025-01-06-15-36-11-346.png|width=541,height=247! Preconditions: Configure FLEXIO_PWM_IP_IRQ_ON_RISING_EDGE for node Flag Event response Pass PWM_RISING_EDGE into function Pwm_EnableNotification PwmDevErrorDetect is checked Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: An Det error is raised, which prevents user from using the rising edge notification via Pwm_EnableNotification if FLEXIO_PWM_IP_IRQ_ON_RISING_EDGE configured for node Flag Event response Expected behavior: There is no Det error raised when using the rising edge notification via Pwm_EnableNotification if FLEXIO_PWM_IP_IRQ_ON_RISING_EDGE configured for node Flag Event response. (also for the falling edge, both edges) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-163908	Bug	[Port] Some APIs need to be check DET before access data Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		In function Port_lpw_SetPinDirection, has access pUsedPadConfig array use PinIndex before checking out-of-range. It can be happened when user pass value out-of-range, caused crash when run !image-2025-01-07-15-02-37-162.png|width=914,height=466! Preconditions: PVT_PORT_S32J100_0.4.1_CD_001 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Access out-of-range array Expected behavior: Should be check range before access data element Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-163943	Bug	[S32K1_M24X 3.0.0] [OCU] Difference when generate file from EBT and S32CT Detailed description (how to reproduce it): When generate test , there are some differences between eb tresos and s32ct. Details in the attached file: Preconditions: Generate on EBT tresos and S32CT and compare generated files Test Case ID (internal TC that caught the defect) optional: Ocu_TS_100, OCU_TS_007 Observed behavior: When generate test, there are some differences between eb tresos and s32ct Expected behavior: When generate test, both eb tresos and s32ct are the same Note:* in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-164127	New Feature	[SPI] Documentation for maximum baudrate not correct -> update limit in code Detailed description (how to reproduce it): S32k31x limits were not described correctly in Reference manual See ticket TKT0666905 in dpdm The S32k31x can reach 10Mbps on LPSPI1-5 but with SCK 33/66 duty cycle. Preconditions: [~nxf49103] before you start on this, check with [~nxf93027] if we received confirmation for removing the limit Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-164169	Bug	[Mem_43_INFLS]: Wrong block number for UTEST areas Detailed description (how to reproduce it): Wrong block number for UTEST areas. UTEST belongs to block0, same with the code flash. the wrong block number will cause the access code(AC) works abnormal. When we try to operate the UTEST area, even we enable the AC feature, in current implementation, we treat it as different block, then we will not copy the code to RAM, so it will trigger the RWW issue. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A

ID	Subtype	Headline and Description
		Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-164397	Bug	[OCU][S32K1_M24X 3.0.0] Duplicate macro define name between 2 modules Ocu and Qdec module Detailed description (how to reproduce it): When I configure Ocu and Qdec in 1 configuration, when building test, I get this error !image-2025-01-13-17-13-20-952.png! I check and see that we duplicate macro define name between 2 modules Ocu and Qdec. Please help me check !image-2025-01-13-17-13-41-376.png! !image-2025-01-13-17-15-56-327.png! !image-2025-01-13-17-17-02-853.png! Preconditions: configure Ocu and Qdec in 1 configuration Test Case ID (internal TC that caught the defect) optional: Ocu_TS_001 Observed behavior: Duplicate macro define name between 2 modules Ocu and Qdec module Expected behavior: Macro define name between 2 modules Ocu and Qdec are different Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-164609	Bug	[ETH]: Failed to generate file "Gmac_Ip_VS_0_PBcfg.c" Detailed description (how to reproduce it): Failed to generate file "Gmac_Ip_VS_0_PBcfg.c" !image-2025-01-15-09-17-57-353.png|thumbnail! Preconditions: Use attach file for more details Test Case ID (internal TC that caught the defect) optional: ETH_TS_ECPD (test_eth) Observed behavior: Failed to generate file "Gmac_Ip_VS_0_PBcfg.c" Expected behavior: no more errors code gen Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-164764	New Feature	[IMPLEMENTATION] Messaging: provide way to not initialize all MUs and add APIs to be able to initialize MUs separately CR description:_* At startup, not all MUs need to be initialized (depending on the power domain) At runitme, MUs can be re(initialized) independently Reason for this change: Clean initialization and reinitialization of specific MUs, not all. Benefit: Robust SW. Unblocks features related to Cohort re-start.

ID	Subtype	Headline and Description
		Onetime CR/Strategic CR: [text placeholder]_ Use-case: [text placeholder] HW documentation reference (as applies): [text placeholder]_ HW/Application Engineer contact (as applies): [text placeholder]_ Note: relevant documents to be attached to the ticket.
ARTD-164829	Bug	[GDU][S32K1_M24X 3.0.0] Issue about ISR function of GDU Detailed description (how to reproduce it): # According to requirement {*}CPR_RTD_00011.gdu{*}: ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. In case driver has not init yet and there is a spurious interrupt, the ISR function below would not clear flags. ! image-2025-01-16-15-04-43-071.png! # GDU peripheral has several interrupt types (1 for high voltage detect and 6 for desaturation) (The INTEN register use for enabling GDU interrupt) !image-2025-01-16-15-14-16-348.png! GDU driver only uses one callback function to handle all interrupts which are not the same and ISR function handles all interrupts at once when there is an occurred interrupt. It leads to interrupt may not be treated the right way. Test Case ID (internal TC that caught the defect) optional: Gdu_TS_008 Expected behavior: # ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. # ISR shall define specific callback functions for each interrupt and handle them one by one. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: You can refer other module to implement ISR function # To satisfy requirement CPR_RTD_00011.gdu [^Pit_Ip_ProcessCommonInterrupt.txt][^Pit_Ip_ProcessCommonInterrupt.txt] # To handle each interrupt one by one [^OCU_ISR.txt]
ARTD-164870	New Feature	[IMPLEMENTATION] [TSN S32K396] Add 802.1Qbu support into RTD GMAC driver What is the problem/necessity of the task: TSN stack is using RTD drivers GMAC driver; Support for 802.1Qbv, 802.11Qbu is required scope similar to S32ZE; The target Due date assumes the feature is available sooner to be tested in engineering builds, the feature shall be available in RTD S32K396 5.0.0 RTM scheduled for Auf/24; If this release with this feature is not delivered TSN stack release will defeature support only 802.1Qbv; What do we need to do to solve the issue: Please provide us NXP RTD driver release: Example RTD application as a part of the package (example working, incl. startup, linker scripts available) with focus on Ethernet communication. Please provide RC at least three weeks before the release date to allow testing before the release. Please provide both Tresos and S32DS (CT) packages. How we can test this: NXP RTD drivers Ethernet communication API's will be tested. QoS/TSN features will be tested. Are the requirements affected: Yes. currently RTD supports only 802.1Qbv, Qbu is needed
ARTD-164948	Bug	[Dio] Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid. In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached.

ID	Subtype	Headline and Description
		Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. Otherwise, we can use this command to enable case sensitive for all created subfolders and no need to renew them: "(Get-ChildItem foldername Recurse Directory).Fullname ForEach-Object {fsutil file setCaseSensitiveInfo "$_" enable}" # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-165306	Bug	[SPI] In SpiDmaContMemory feature, a fullduplex transfer after a transmit halfduplex transfer, the received data in rx buffer of fullduplex transfer will be wrong. Detailed description (how to reproduce it): In SpiDmaContMemory feature, if there is a fullduplex transfer after a transmit halfduplex transfer, the received data in rx buffer of fullduplex transfer will be wrong. Preconditions: Use DmaContMem feature Test Case ID (internal TC that caught the defect) optional: Spi_TC_FCT_1231 Observed behavior: In SpiDmaContMemory feature, if there is a fullduplex transfer after a transmit halfduplex transfer, the received data in rx buffer of fullduplex transfer will be wrong. Expected behavior: All transfers work correctly Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-165399	Bug	[FEE R21.11] EB,DS will report an error when the node does not exist Detailed description (how to reproduce it): EB,DS will report an error when the " FeeBufferAlignmentValue" node does not exist or may not be referenced Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: FEE_TC_001 Observed behavior: EB,DS does not report an error when the " FeeBufferAlignmentValue" node does not exist or may not be referenced Expected behavior: EB,DS will report an error when the " FeeBufferAlignmentValue" node does not exist or may not be referencedEB, DS will report an error when the " FeeBufferAlignmentValue" node does not exist or may not be referenced Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-165906	Bug	[Sent][S32K3XX] The Flexio_Sent_Ip_IrqHandler does not exist on plugins

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): the Flexio_Sent_Ip_IrqHandler does not exist on plugins. So, it makes fail at build !image-2025-01-21-14-55-51-613.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Sent_TS_010 Observed behavior: Failed at build Expected behavior: Build success Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ARTD-166157	Bug	[CAN] MainFunction_Read Buffer Allocation issue
		
		Detailed description (how to reproduce it):
		The customer use Driver in Polling mode with an Os that allocate the Stack dinamically and have a 5 Ms Task where he calls the Can_43_FLEXCAN_MainFunction_Read which > Can_43_FLEXCAN_Ipw_MainFunction_Read which allocates a buffer and pass the to the > FlexCAN_Ip_Receive and set the MB Status in RX if the receive will not happen at second call will call again this sequence but the message buffer could be alocated to other address and the FlexCAN_Ip_Receive will return status busy but will not set new address of the message buffer and keeps the older value from previous call.
		
		Preconditions:
		This describe the extracted flow of the sequences :
		Can_43_FLEXCAN_MainFunction_Read ( );
		{
		Can_43_FLEXCAN_Ipw_MainFunction_Read ( );
		{
		Flexcan_Ip_MsgBuffType ReceivedDataBuffer;
		//-> This changes every time we call the function,
		// because of the OS, the stack is dynamically allocated
		
		FlexCAN_Ip_Receive (ReceivedDataBuffer);
		{
		FlexCAN_StartRxMessageBufferData (ReceivedDataBuffer);
		{
		if (state->mbs[mb_idx].state != FLEXCAN_MB_IDLE)
		{
		result = FLEXCAN_STATUS_BUSY;
		// If I don't receive, I will keep entering here
		// The ReceivedDataBuffer may change its location every time we call the function
		}
		else
		{
		//We will enter here only if state == IDLE
		state->mbs[mb_idx].state = FLEXCAN_MB_RX_BUSY; // In the 1st call
		state->mbs[mb_idx].pMBmessage = ReceivedDataBuffer;
		}
		}
		}
		Test Case ID (internal TC that caught the defect) optional:
		N?A
		
		Observed behavior:
		This is happening in the OS context where the Tasks can have different allocation on the stack, bettwen multiple calls.
		
		Expected behavior:
		Correct behavior to allocate each time call the correct buffer address.
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		[....]

ARTD-166406	New Feature	[Resource][GENERAL] Higher granularity for ARM Core Architecture selection CR description: SAF SW product is dependent on RTD drivers, among others also on Resource configuration Tresos plugin, where we reuse generated output from configurable options: ResourceSubderivative ARM_CoreArchitecture For SAF code it is needed to raise granularity of the ARM_CoreArchitecture item, ideally on the architecture version level. At the moment RTD Resource module provides granularity on the Architecture Profile level e.g.: ARM_M_ARCH ARM_R_ARCH ARM_A64_ARCH

ID	Subtype	Headline and Description
		SAF needs to differentiate also on ARM Architecture version level e.g.: ARMV8_AARCH64 ARMV8_AARCH32 ARMV8_RARCH ARMV8_MARCH ARMV7_MARCH ARMV6_MARCH Reason for this change: SAF has specific code depending on the particular ARM architecture e.g. ARMv6-M, ARMv7-M, ARMv8-M,... ARMv8-AARCH64, ARMv8-RARCH... Benefit: SAF doesn't need to implement workarounds to achieve this granularity on its own. Maybe other products or customer application can benefit for the same reason as well. For the platforms where there is e.g. M7 core and M33 core (or M0 core) we can differentiate between them. Onetime CR/Strategic CR: Strategic CR to be implemented for all Platforms. Use-case: From SAF sCheck code e.g.: #if ((SAFETY_BASE_ARMV8_AARCH32 == SAFETY_BASE_PLATFORM_ARM) (SAFETY_BASE_ARMV8_AARCH64 == SAFETY_BASE_PLATFORM_ARM)) #include "sCheck_Lib_ARMv8A.h" #endif HW documentation reference (as applies): [Arm CPU Architecture Arm®|https://www.arm.com/architecture/cpu] HW/Application Engineer contact (as applies): Reporter Note: relevant documents to be attached to the ticket.
ARTD-166493	Bug	[DPGA] Compiler Directives #define 's are generating in single line in EB Tresos 29.7 NewWorkDescription: This issue only applicable on EB Tresos {color}*{color:#ff0000}29.7{color}*{color:#ff0000} (I know that curenlty we test on EB Tresos 29.0.0 so it is not an issue at this time) . Reported by Elektrobit The compiler directives #defines in generated files are coming in single line instead of next lines eg in ADC module (other modules as I2S, DPGA have the same issue), as shown below the macro ADC_SAR_IP_SELFTEST_ENABLED generated in same line continuously after ADC_SAR_IP_WDG_ENABLED: EB Input: This is basically the expected behavior: if AUTOSPACING is enabled and a command is at the end of a line (here, the IF/ELSE/ENDIF), the line-break gets removed. This did not change, but now this also works for included and macro files (which is probably the case here?). You can either add a [!CR!] the end of the line or add an empty line File: Adc_Sar_Ip_CfgDefines.h #define ADC_SAR_IP_ECH_ENABLED (STD_OFF) #define ADC_SAR_IP_JECH_ENABLED (STD_OFF) #define ADC_SAR_IP_EOCTU_ENABLED (STD_OFF) #define ADC_SAR_IP_EOC_ENABLED (STD_OFF) #define ADC_SAR_IP_WDG_ENABLED(STD_OFF)#define ADC_SAR_IP_SELFTEST_ENABLED(STD_OFF)#define ADC_SAR_IP_DEV_ERROR_DETECT(STD_OFF)#define ADC_SAR_IP_TIMEOUT_TYPE (OSIF_COUNTER_DUMMY) #define ADC_SAR_IP_TIMEOUT_VAL (3000UL) Please consider this ticket in the future if we test on EB Tresos 29.7 Requirement source: N/A Proposed solution optional: In MCAL plugin., The files which are responsible for this macro generation (eg, I2s_RegOperations.m) need to updated as per shown below Current implementation : #define ADC_SAR_IP_DEV_ERROR_DETECT [!IF "AutosarExt/AdcSarIpDevErrorDetect"!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!] Proposed Update : #define ADC_SAR_IP_DEV_ERROR_DETECT ([!IF "AutosarExt/AdcSarIpDevErrorDetect"!]STD_ON[!ELSE!]STD_OFF[!ENDIF!])

ID	Subtype	Headline and Description
ARTD-166496	Bug	[I2S] Compiler Directives #define 's are generating in single line in EB Tresos 29.7 NewWorkDescription: This issue only applicable on EB Tresos {color}*{color:#ff0000}29.7{color}*{color:#ff0000} (I know that curenlty we test on EB Tresos 29.0.0 so it is not an issue at this time) . Reported by Elektrobit The compiler directives #defines in generated files are coming in single line instead of next lines eg in ADC module (other modules as I2S, DPGA have the same issue), as shown below the macro ADC_SAR_IP_SELFTEST_ENABLED generated in same line continuously after ADC_SAR_IP_WDG_ENABLED: EB Input: This is basically the expected behavior: if AUTOSPACING is enabled and a command is at the end of a line (here, the IF/ELSE/ENDIF), the line-break gets removed. This did not change, but now this also works for included and macro files (which is probably the case here?). You can either add a [!CR!] the end of the line or add an empty line File: Adc_Sar_Ip_CfgDefines.h #define ADC_SAR_IP_ECH_ENABLED (STD_OFF) #define ADC_SAR_IP_JECH_ENABLED (STD_OFF) #define ADC_SAR_IP_EOCTU_ENABLED (STD_OFF) #define ADC_SAR_IP_EOC_ENABLED (STD_OFF) #define ADC_SAR_IP_WDG_ENABLED(STD_OFF)#define ADC_SAR_IP_SELFTEST_ENABLED(STD_OFF)#define ADC_SAR_IP_DEV_ERROR_DETECT(STD_OFF)#define ADC_SAR_IP_TIMEOUT_TYPE (OSIF_COUNTER_DUMMY) #define ADC_SAR_IP_TIMEOUT_VAL (3000UL) Please consider this ticket in the future if we test on EB Tresos 29.7 Requirement source: N/A Proposed solution optional: In MCAL plugin., The files which are responsible for this macro generation (eg, I2s_RegOperations.m) need to updated as per shown below Current implementation : #define ADC_SAR_IP_DEV_ERROR_DETECT [!IF "AutosarExt/AdcSarIpDevErrorDetect"!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!] Proposed Update : #define ADC_SAR_IP_DEV_ERROR_DETECT ([!IF "AutosarExt/AdcSarIpDevErrorDetect"!]STD_ON[!ELSE!]STD_OFF[!ENDIF!])
ARTD-166614	New Feature	[UART] Address CPR_RTD_00543 (MR200) - Implementation NewWorkDescription: The driver shall prevent configuration of the same hardware instance between HL configuration and standalone IP configuration. Requirement source: CPR_RTD_00543 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-167021	Bug	[ICU]Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid. In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached. Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. Otherwise, we can use this command to enable case sensitive for all created subfolders and no need to renew them: "(Get-ChildItem foldername Recurse Directory).Fullname ForEach-Object {fsutil file setCaseSensitiveInfo "$_" enable}" # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-167860	Bug	[FEE]: Fee_Cancel works abnormal Detailed description (how to reproduce it): The Fee_Cancel API works abnormal. When we try to cancel an on going job, like Write. The Fee_Cancel function will cause error, We will never trigger a new write job anymore, according to debugging. the pointer maintenance is wrong. For example, when the first write job executed and the header info had written, but the data didn't start yet, then we cancel the job at this time, the pointer add 8 byte. but when a new write job request, it will write from the same address, but this address had been written some previous data, then it cause error. Another thing, the Fee_GetStatus, Fee_GetJobResult will return wrong status after call the Fee_Cancel. both these two variables was changed in Fee_Cancel function. but in fact, it didn't canceled really. You can take a reference from the attached test project. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Error Expected behavior: See above Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-168046	Bug	[RM] Inconsistency between EB and DS config in tab Xrdc Domain Assignment Detailed description (how to reproduce it): In the Domain Peripheral and Memory Assignment tab. If the configured list is empty, it will generate the error on EB, but there is no error on DS. !image-2025-02-13-13-20-48-522.png! Preconditions: Enable Xrdc IP Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Inconsistency about error log between EB and DS Expected behavior: It should be identic Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check and update the validation on DS for XRDC
ARTD-168635	Bug	[RM]DMAMUX chapter is missing in user manual Detailed description (how to reproduce it): DMAMUX chapter is missing in user manual !image-2025-02-17-16-10-41-491.png|thumbnail! Preconditions:

ID	Subtype	Headline and Description
		Open UM of S32K3 500 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: DMAMUX chapter is missing in user manual Expected behavior: DMAMUX chapter present Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-168826	Bug	[PLATFORM] Missing prototype declaration of Mpu_M7_Ip_GetErrorDetails_Privileged in MPU_M7 IP when compiling IAR Safety version Detailed description (how to reproduce it): IAR 8.50.10 Safety version compiler required prototype declaration for all invoked functions. MPU_M7 IP source code missed the prototype declaration of Mpu_M7_Ip_GetErrorDetails_Privileged Prototype: boolean Mpu_M7_Ip_GetErrorDetails_Privileged(Mpu_M7_Ip_ErrorDetailsType pErrorDetails); Preconditions: IAR 8.50.10 Safety version compiler, MPU_M7 is enabled in configuration tool Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: build failed Expected behavior: build passed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add prototype into source file MPU_M7_Ip.c boolean Mpu_M7_Ip_GetErrorDetails_Privileged(Mpu_M7_Ip_ErrorDetailsType pErrorDetails);
ARTD-168937	Bug	[Spi] ecvd missing some node relative of SpiBaudrateConfig Detailed description (how to reproduce it): ecvd file missing some nodes as below picture: !image-2024-10-17-15-50-16-227.png|thumbnail! !image-2024-10-17-15-58-27-020.png|thumbnail! Preconditions: use SpiBaudrateConfig Test Case ID (internal TC that caught the defect) optional: Ip_Spi_TS_E01 Spi_TS_Cot_002 Observed behavior: ecvd file missing some node Expected behavior: ecvd file not missing any node Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-169345	Bug	[ADC][Train] Code that cannot be used is present in plugin Detailed description (how to reproduce it): Build adc plugin on platforms which have limited functionality, and code not applicable to that platform will still be present inside plugin. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Code not applicable to specific platform still present in plugin Expected behavior:

ID	Subtype	Headline and Description
		Code not applicable to one platform should not be generated in plugin. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-169515	Bug	[icu] fix fail in step generation and build for RTD_TRAIN Detailed description (how to reproduce it): Resource module needs to be updated to have the K389 resource created for an urgent package to be delivered on K3, this will affect the drivers that did not get the chance to add a resource for K389. A new Resource tag with this change will be applied in trains, if the resource is missing from a driver, as a temporary solution, a dummy K389 resource can be added. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: dev test Icu_TS_014 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add resource for S32K389
ARTD-169518	Bug	[SPI] Cannot config more SpiExternalDevice on S32DS with S32G-RTD 5.0.0 Detailed description (how to reproduce it) : Cannot add more SpiExternalDevice !image-2025-02-24-16-27-53-883.png! !image-2025-02-24-16-24-45-143.png! !image-2025-02-24-16-25-11-584.png! Preconditions: n/a Test Case ID (internal TC that caught the defect) optional: n/a Observed behavior: n/a Expected behavior: n/a Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: n/a
ARTD-169697	Bug	[MemAcc] Error in compiling when MemAccJobEndNotificationName is not configured. Detailed description (how to reproduce it): When I do not configure notification when a job finish, I still can generate successfully but got error in compiling !image-2025-02-25-13-09-30-557.png! !image-2025-02-25-13-10-00-890.png! !image-2025-02-25-13-10-35-822.png! Preconditions: Do not configure MemAccJobEndNotificationName Test Case ID (internal TC that caught the defect) optional: N/A

ID	Subtype	Headline and Description
		Observed behavior: Build errror Expected behavior: build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-169857	New Feature	[adc] Add s32k389_mapbga437 Resource for driver The resource module needs to be updated to have the K389 resource created for an urgent package to be delivered on K3, as all drivers need to add a resource for K389. Eg: Mcl S32K389 resource: [Mcl_s32k389_mapbga437.txt|https://bitbucket.sw.nxp.com/projects/ARTD/repos/mcl/browse/specific/S32K3XX/resource/Mcl_s32k389_mapbga437.txt] A new Resource tag was already applied on Trains, if the resource is missing from a driver, as a temporary solution, a dummy K389 resource can be added.
ARTD-172268	Bug	[LPI2C] Unable to set Clock Hold in slave mode. Detailed description (how to reproduce it): It is not possible to configure Clock Hold (SCFGR2[CLKHOLD]) for slave mode in the LPI2C driver. In imperfect hw setups it is possible to have unequal impedances on the SCL and SDA lines, causing SCL signal to rise faster than SDA. If SCL rising edge immediately follows an SDA rising edge, this could cause a change in the actual order of the edges, and the apparition of an unintended STOP event on the line. Clock Hold feature is meant to fix this case, by increasing the time between SCL rising edge and SDA rising edge. Usually SDA line is changed soon after the SCL falling edge, so long before the next SDA rising edge. But there is an exception, after the address byte, if there was clock stretching while LPI2C waits for data from the application. When the data is provided, if the first bit is "1", LPI2C will set SDA high, and immediately stop the clock stretching, causing SCL to go high. This is when the issue above occurs. I could eliminate the issue setting SCFGR2[CLKHOLD] to a non-zero value, but I had to edit the driver, as this setting is not available. Preconditions: Imperfect hw setup, clock stretching while waiting for data from application, data starting in "1" bit. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: With no clock hold, sometimes communication fails due to false STOP detected on the line. Expected behavior: clock hold != 0 is needed to prevent this issue. Proposed solution optional: Allow clock hold and data valid configuration in slave mode.
ARTD-172394	Bug	[MCU]: Possible wrong operation for LVSC register Detailed description (how to reproduce it): In the Power_Ip_PMC_VoltageErrorIsr function, the operation for the LVSC register, it seems we want to clear the flag, and current implementation is write 0. but according to the RM, we should to write 1 to clear the flag, please double check the design purpose with the RM. !image-2025-03-03-16-37-52-469.png! !image-2025-03-03-16-36-07-621.png! Preconditions: ALWAYS Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: I guess the purpose should be achieved like this: IP_PMC->LVSC &= (uint32)(~PMC_LVSC_UV_IRQ_FLAGS_MASK32);

ID	Subtype	Headline and Description
		IP_PMC->LVSC |= (uint32)(PMC_LVSC_UV_IRQ_FLAGS_MASK32);
ARTD-172427	Bug	[GMAC] Verify that the MUX used to select the clk_rx_i, clk_tx_i are set for all the derivatives Detailed description (how to reproduce it): !image-2025-03-03-14-11-42-017.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Bits from DCMRWF3 are not written by anyone. Expected behavior: Bits from DCMRWF3 to be written by Ethernet diver Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-172560	Bug	[Mem_INFLS] Build fail C40_IP tests Detailed description (how to reproduce it): identifier "IP_PFLASH_TYPE_COMMON" is undefined identifier "ElapsedTicks" is undefined identifier "CurrentTicks" is undefined identifier "TimeoutTicks" is undefined Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_0001 Observed behavior: !image-2025-03-04-11-26-37-692.png! Expected behavior: Build tests pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-173086	Bug	[MemAcc] Exclusive Areas are missing for guarding global variables in MainFunction Detailed description (how to reproduce it): External Assumption analysis was not done correctly and some EA are missing. Please refer to this guideline: https://confluence.sw.nxp.com/display/AUTORD/Exclusive+Area+Guideline All functions can be considered as needing to be protected with EA's except Init and Deinit Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Analysis was wrongly done, some Exclusive Areas are missing. Expected behavior: No issues Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add missing Exclusive Areas.
ARTD-173248	Bug	[S32K1-S32M27x][MemAcc] Update code fix HIS_CALL, HIS_LEVEL Detailed description (how to reproduce it): HIS_LEVEL, HIS_CALL violations need to fixed Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A

ID	Subtype	Headline and Description
		Observed behavior: there are some HIS_CALL, HIS_LEVEL have not fix Expected behavior: They need to fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update driver code
ARTD-173448	New Feature	[ICU] Address CPR_RTD_00543 (MR200) - Implementation NewWorkDescription: Context: Clarify MR200 / CPR_RTD_00543 to either be included for the next K1 release or permanently excluded. Decided to : 1. keep the requirement excluded for k1 3.0.0 as it was on previouse release 2. clone the ticket for all drivers in RTD +*with scope of addressing the implementation*+ on any next release (any NPI) and not keeping on excluded requirements Action needed on driver level: Update Variant attribure* for the internal requirement CPR_RTD_00543 to be consistent with generic {*}Verify if implementation exist{*}s or need an implementation ticket in ARTD to adress it. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-173481	New Feature	[PWM][S32K3XX-S32M27X] Implement CPR_RTD_00543 (MR200) NewWorkDescription: Context: Clarify MR200 / CPR_RTD_00543 to either be included for the next K1 release or permanently excluded. Decided to : 1. keep the requirement excluded for k1 3.0.0 as it was on previouse release 2. clone the ticket for all drivers in RTD +*with scope of addressing the implementation*+ on any next release (any NPI) and not keeping on excluded requirements Action needed on driver level: Update Variant attribure* for the internal requirement CPR_RTD_00543 to be consistent with generic {*}Verify if implementation exist{*}s or need an implementation ticket in ARTD to address it. Requirement source: CPR_RTD_00543 Proposed solution optional: NA
ARTD-173606	New Feature	[base] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173612	New Feature	[crc] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173615	New Feature	[port] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources

ID	Subtype	Headline and Description
		Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png| width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173618	New Feature	[eth] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources and s32k389_mapbga437 resource Add S32K312 100LQFP support Add support S32K389 Proposed Solution: For S32K312: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png| width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted For S32K389: According to Change request:ARTD-117240, Add following resource to support S32K389: s32k389_mapbga437
ARTD-173627	New Feature	[i2c] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png| width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173630	New Feature	[i2s] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png| width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173642	New Feature	[mcl] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png| width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173657	New Feature	[pwm] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources and s32k389_mapbga437 resource Add S32K312 100LQFP support Add support S32K389

ID	Subtype	Headline and Description
		Proposed Solution: For S32K312: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted For S32K389: According to Change request:ARTD-117240, Add following resource to support S32K389: s32k389_mapbga437
ARTD-173663	New Feature	[sent] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173666	New Feature	[spi] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173669	New Feature	[uart] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources and s32k389_mapbga437 resource Add S32K312 100LQFP support Add support S32K389 Proposed Solution: For S32K312: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted For S32K389: According to Change request:ARTD-117240, Add following resource to support S32K389: s32k389_mapbga437
ARTD-173672	New Feature	[wdg] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution:

ID	Subtype	Headline and Description
		Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173687	New Feature	[mem_inflls] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173690	New Feature	[mem_exflls] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173696	New Feature	[mem_eep] [IMPLEMENTATION] [K312] Add S32k312_lqfp100 resources Add S32K312 100LQFP support Proposed Solution: Assumption:+ lqfp100 package is 100% same pinout and muxing as hdqfp100, !image-2024-09-25-08-53-20-147.png|width=588,height=44! duplicate and rename resource file "_s32k312_hdqfp100" to "_s32k312_lqfp100" for all drivers and perform a check for compile only tests. duplicate S32DS data based on former hdqfp input, 35 drivers will be impacted
ARTD-173932	New Feature	[Mem_Eep][uSDHC] Improve driver code: Do not run eMMC command in case of SD card configuration only NewWorkDescription: Currently, Sd_Emmc_Ip_Init() will try to init with eMMC card first (send CMD01 SD_EMMC_IP_COMMAND_MMC_SEND_OPERATION_CONDITION), if there is no response, the driver will try to init with SD card later (send CMD08 SD_EMMC_IP_COMMAND_SEND_INTERFACE_CONDITION). This is not necessary to run eMMC command while configured to run SD card only. Also, it will solve the issue when running VDK. The VDK encountered an error when running eMMC command in case of SD card configuration only. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:
ARTD-173948	Bug	[ETH] requirement define not mapping with IP supported Detailed description (how to reproduce it): Define type for IP GMAC wrong as below: !image-2025-03-14-16-21-12-915.png! !image-2025-03-14-16-35-07-208.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Define STATUS_ENET_RX_QUEUE_EMPTY should be changed to GMAC in requirement

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-174054	Bug	[CAN_43_FLEXCAN]: Validation of destination node of CAN_43_FlexCAN incompatible with customer tooling There is an issue with validation of the destination node of Can_43_FLEXCAN. Customer tooling does not fulfill this string (screenshot attached) because their configuration might start with "their own package name" instead of Can_43_FLEXCAN. !image-2025-03-17-13-22-05-220.png|width=650,height=147! While it is understood that it is used to validate whether the referenced node is in the same package module with current node or not, but it seems to be incompatible if some customer has to use the CAN driver in combination without the CAN stack.
ARTD-174081	Bug	[S32K3xx_S32M27x_6.0.0][CRC]: Fail at generating plugin of CRC Detailed description (how to reproduce it): When I generate plugin of Crc at local, there're some error with XDM file. Detail in image below !image-2025-03-17-16-21-12-030.png! !image-2025-03-17-16-21-28-907.png! Observed behavior: Failed at generating plugin Expected behavior: Dev update new xdm file to fix error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-174571	New Feature	[LPI2C] Unable to set DBGEN in Master Enable NewWorkDescription: We need to use the LPI2C Master with the debugger connected, thus, the DBGEN bit from MCR has to be set. Requirement source: Proposed solution optional: In LPI2C_Set_MasterEnable() function from Lpi2c_Ip_HwAccess.h, RegValue = LPI2C_MCR_DBGEN_MASK.
ARTD-175875	Bug	[ADC] S32K36X resource not match between EB tresos and RM Detailed description (how to reproduce it): [Two customer Lincontrol-K366-BGA, 四川道恒底盘-K364-BGA Both the customer issues are that the resources not matching between EB Tresos and the s32k396 RM, detailed info is shown below. The customer has an urgent issue with SW debugging. 1, Emios In RM Channel 0~7 are not available in K36X, but in EB Tresos, 16~23 not available !image-2025-03-24-13-24-11-874.png! but in the RTD EB config tool, the channel 0-15 are available. !image-2025-03-24-13-24-51-863.png! 2, SAR ADC In RM SAR-ADC 0~2 not available but in EB Tresos SAR-ADC 4~6 not available !image-2025-03-24-13-27-31-093.png! In the RTD, ADC0-3 are available. !image-2025-03-24-13-27-50-934.png!] Preconditions: [check above] Test Case ID (internal TC that caught the defect) optional: [check above]

ID	Subtype	Headline and Description
		Observed behavior: [check above] Expected behavior: [check above] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-175909	Bug	[ICU] S32K36X resource not match between EB tresos and RM Detailed description (how to reproduce it): [Two customer Lincontrol-K366-BGA, 四川道恒底盘-K364-BGA Both the customer issues are that the resources not matching between EB Tresos and the s32k396 RM, detailed info is shown below. The customer has an urgent issue with SW debugging. 1, Emios In RM Channel 0~7 are not available in K36X, but in EB Tresos, 16~23 not available !image-2025-03-24-13-24-11-874.png! but in the RTD EB config tool, the channel 0-15 are available. !image-2025-03-24-13-24-51-863.png! 2, SAR ADC In RM SAR-ADC 0~2 not available but in EB Tresos SAR-ADC 4~6 not available !image-2025-03-24-13-27-31-093.png! In the RTD, ADC0-3 are available. !image-2025-03-24-13-27-50-934.png!] Preconditions: [check above] Test Case ID (internal TC that caught the defect) optional: [check above] Observed behavior: [check above] Expected behavior: [check above] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-176064	Bug	[WDG] Status variable Wdt_Ip_abStatus is not set after invoking Wdg_ChannelInit() with OFF_MODE Detailed description (how to reproduce it): Init Wdg with OFF_MODE Change mode to SLOW_MODE Waiting to Wdg timeout and check Wdg callback function Preconditions: Test Case ID (internal TC that caught the defect) optional: Wdg_TC_FCT_0305 Wdg_TC_FCT_0307 Observed behavior: Invoke Wdg_ChannelInit() > Wdg_InitialHardware(), in Wdg_InitialHardware() because of default mode is OFF_MODE > Invoke Wdg_Ipw_SetMode() !image-2025-03-25-14-02-51-842.png|thumbnail! Wdg_Ipw_SetMode() does not set Wdt_Ip_abStatus to TRUE (only Wdg_Ipw_Init() can do this), so other function will determine WDG is UnInit status. like Wdt_Ip_IrqHandler() function, will not implement callback function !image-2025-03-25-14-07-30-039.png|thumbnail! Expected behavior: Wdg_ChannelInit() with OFF_MODE can set Wdt_Ip_abStatus to true

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-176396	Bug	[CAN] FlexCan_Ip_Wrapper.h contains specific code for specific OSes Detailed description (how to reproduce it): FlexCan_Ip_Wrapper.h file contains specific code for a specific OS which violates the general requirement which states that drivers must be OS agnostic. !image-2025-03-26-09-56-16-961.png! Preconditions: none Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Os specific code in driver implementation Expected behavior: No Os specific code in driver implementation Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove the specific code for a specific OS. Check this solution to be used ARTD-165968
ARTD-176736	Bug	[GPT] Undefined Gpt_Channel_EnableChainMode and Gpt_Channel_DisableChainMode functions Detailed description (how to reproduce it): undefined Gpt_Channel_EnableChainMode and Gpt_Channel_DisableChainMode functions: !image-2025-03-28-14-13-00-747.png! M4_SRC_USER_PARAM_0 is not generated: !image-2025-03-28-14-14-18-098.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Gpt_TS_002 Observed behavior: Build fail with undefined functions Expected behavior: Build success with Gpt_Channel_EnableChainMode and Gpt_Channel_DisableChainMode functions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update to generate M4_SRC_USER_PARAM_0 for platform that support chain mode
ARTD-177241	Bug	[ADC]Warning: AdcGroupHwTriggerSource cannot be empty Detailed description (how to reproduce it): When the user selects "Adc Group Trigger Source" as "ADC_TRIGG_SRC_SW", the following warning appears when "Adc Group Hardware Trigger Source" is empty. !image-2025-04-02-09-33-27-347.png! This warning caused an error on the Vector Davinci tool when the customer imported the configuration file (.arxml) into this tool. Preconditions: No warnings Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: as Detailed description Expected behavior: No warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-177632	Bug	Lpuart_Uart_Ip_SetBaudRate bug

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): [If MaxOsr >= 5U, the driver stores incorrect CalculatedBaud] Preconditions: [-] Test Case ID (internal TC that caught the defect) optional: [696822] Observed behavior: [CaculatedBaud is from the last iteration] Expected behavior: [CalculatedBaud is the best fit] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [!image-2025-04-07-10-09-31-722.png|thumbnail!]
ARTD-177658	Bug	[PWM][S32K3XX] Notification fault is not disabled after calling Pwm_Init() Detailed description (how to reproduce it): According to Requirement SWS_PWM_00052, Pwm_Init will disable all notifications. !image_1.png|width=695,height=589! However, In the Pwm_Init function, we are setting fault interrupt using FlexPwm_Ip_SetFltInterruptHw function. > That is incorrect with req SWS_PWM_00052. !image_2.png|width=800,height=554! If in the Pwm_Init function disable all notifications, then need to create a function to be able to Enable/Disable notifications during runtime In release K1, created PWM_EnableFaultnotification and PWM_DisableFaultnotification to solve the problem [https://bitbucket.sw.nxp.com/projects/ARTD/repos/pwm/commits/be0ae5e06f5aaed5713eba414ab6d47d7311d3e0#generic%2Fsrc%2FPwm.c] Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A {_}*Observed behavior:*{_}{*}{{*}} Notification fault is not disabled after calling Pwm_Init() function Expected behavior: Pwm_Init function will disable all notifications Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-177708	Bug	[S32K3xx_S32M27x_6.0.0][MEM_INFLS]: C40_Ip_MainInterfaceSectorErase cannot return C40_IP_STATUS_ERROR_INPUT_PARAM Detailed description (how to reproduce it): C40_Ip_MainInterfaceSectorErase function cannot return C40_IP_STATUS_ERROR_INPUT_PARAM with invalid parameter. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_0005 Observed behavior: C40_Ip_MainInterfaceSectorErase function return C40_IP_STATUS_ERROR not C40_IP_STATUS_ERROR_INPUT_PARAM: Expected behavior: C40_Ip_MainInterfaceSectorErase function return C40_IP_STATUS_ERROR_INPUT_PARAM Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-177820	Bug	[mem_infls] SectorStep is wrong calculated, leading to wrong sector lock register being checked Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		All APIs are impacted. SectorStep}} variable is not correct calculated Preconditions: sector is locked Test Case ID (internal TC that caught the defect) optional: 001 Observed behavior: wrong sector is unlocked Expected behavior: correct sector to be unlocked Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-177877	Bug	[MEMACC] Analyze adding MEMACC_EXCLUSIVE_AREA_04 in MemAcc_MainFunction MemAcc need to add and analyze the MEMACC_EXCLUSIVE_AREA_04 in driver
ARTD-177909	New Feature	[Port] Provide Design Studio support for S32K389 derivative NewWorkDescription: For S32K3 6.0.0 RTM release, S32K389 Design Studio support is needed. Tresos support for S32K389 was already added together with previous release S32K3 6.0.0 CD01. An engineering build drop will be done on 15 April, with focus on S32K389 Tresos Design Studio support.
ARTD-177912	New Feature	[Dio] Provide Design Studio support for S32K389 derivative NewWorkDescription: For S32K3 6.0.0 RTM release, S32K389 Design Studio support is needed. Tresos support for S32K389 was already added together with previous release S32K3 6.0.0 CD01. An engineering build drop will be done on 15 April, with focus on S32K389 Tresos Design Studio support.
ARTD-178097	Bug	[Mcu]: Change default config of two nodes Detailed description (how to reproduce it): Optimize this option by change to uncheck related to ARTD-145116 !image-2025-04-10-11-09-02-114.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Default is disabled (check) Expected behavior: Default is enabled (uncheck) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-178170	Bug	[S32K3xx_S32M27x_6.0.0][MEM_INFLS]: C40_Ip_EccDataErrorSuppression function is not working Detailed description (how to reproduce it): Cannot set DERR_SUP bits on PFCR4 register lead to test ecc is error. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_0012 Observed behavior: !image-2025-04-10-11-23-17-302.png! Expected behavior: C40_Ip_EccDataErrorSuppression is working. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-177987	New Feature	[crc] CR implementation: Revision History for UM and IM

ID	Subtype	Headline and Description
		NewWorkDescription: The chapter Revision History in RTD now always remains v1.0 across releases, does not detail the change history, only release name. !image-2025-02-05-17-49-55-576.png|width=592,height=185! There was a request from Functional Safety Manager for it to have unique identification of version for a document, change history briefly explaining changes between versions. Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Step ||Instruction 1.1 Ensure the tag of rtd_docgen before using is: BLN_RTD_DOCGEN_01.00.03* (or newer tag). 1.2 For build_env: please ensure the correct tag of rtd_docgen is in the release manifest. please add the file "{*}revhistory.dox{*}" from the attachment of this ticket to the folder with following path and start adding your context: "..\dev\test\test\specific\<platform>\doc\dox\common\sub_revision_history" decide the "build_env_revision_extra_x.y" id to extend the table for specific release with general info. This info will be printed in all driver manuals. decide the "driver_revision_extra_x.y" id to extend the table for specific release with info from drivers. Inform this id to everyone for each releases. 1.3 For drivers: please add the file "{*}driver_revhistory.dox{*}" from the attachment of this ticket to the folders with following paths: "..\dev\drivers\AutoSAR\<module>\specific\<platform>\doc\dox\um\sub_revision_history" "..\dev\drivers\AutoSAR\<module>\specific\<platform>\doc\dox\im\sub_revision_history" start adding your context inside the id for the release (ask G10 or check the file revhistory.dox* from build_env) Note See the attachment "{*}examples{*}" for an example of how the .dox files will be in the releases. See the attachment "{*}output_expectation{*}" for an example of how the pdf files will be in the releases. See chapter 5 for more information: [link|https://bitbucket.sw.nxp.com/projects/AMPAT/repos/rtd_docgen/commits/512fa07ea4e3148f718ef669ab337953e9a5ff24#docs%2FUserManualDocumentation.pdf] Now, we concentrate on the context/changes for drivers. How can you remember all the necessary changes from the previous release to the current release and put them in driver_revhistory.dox file? Choose {+}one of the following{+}: Use .exe file Step ||Instruction 2.1 Repo sync or clone these tools and put them together in same folder: define_revision_history: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2] 2.2 Open command line in "define_revision_history" folder, enter the command: {code:java} define_revision_history.exe stn define_revision_history product_name RTD platform_name S32R module_name dio pre_path_file E:\UM_IM\RTD_DIO_UM_RTM_2.0.0.pdf cur_path_file E:\UM_IM\RTD_DIO_UM_RTM_3.0.0.pdf o output_folder Where: product_name: RTD platform_name: {_}<take folder specific name from driver's repo>{_}. E.g: S32R pre_path_file: _<path to file1> cur_path_file :_ _<path to file2> 2.3 Check output excel file for the diff (E.g: ..\define_revision_history\output_folder) and start writing your changes in driver_revhistory.dox file. 2.4 Re-generate the manuals and check the chapter Revision History. Ensure the format of the table still follows as the attachment "{*}output_expectation{*}" Note See the readme here for further ways to run the define_revision_history script: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse/docs?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2] Alternative: Use python. Step ||Instruction 2.1 Repo sync or clone these tools and put them together in same folder: define_revision_history: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2] Autotools Framework: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/auto_tool_fw] Common libs: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/common_libs/browse] 2.2 Install python 3.9.13: [https://www.python.org/downloads/release/python-3913/] ({_}A later version of Python can be used, but it was not verified and might have issues{_}) 2.3 Add this python to Path variable. 2.4 Open cmd and run: python m pip install pdfplumber python m pip install Pillow 2.5 Open command line in "auto_tool_fw" folder, enter the command:{code:java} python autotools.py stn define_revision_history product_name RTD platform_name S32R module_name dio pre_path_file E:\UM_IM\RTD_DIO_UM_RTM_2.0.0.pdf cur_path_file E:\UM_IM\RTD_DIO_UM_RTM_3.0.0.pdf o output_folder Where: product_name: RTD platform_name: {_}<take folder specific name from driver's repo>{_}. E.g: S32R pre_path_file: <path to file1> cur_path_file : <path to file2> 2.6 Check output excel file for the diff (E.g: ..\define_revision_history\output_folder) and start writing your changes in driver_revhistory.dox file. 2.7 Re-generate the manuals and check the chapter Revision History. Ensure the format of the table still follows as the attachment "{*}output_expectation{*}"

ID	Subtype	Headline and Description
		Note See the readme here for further ways to run the define_revision_history script: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse/docs?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2]
ARTD-178001	New Feature	[uart] CR implementation: Revision History for UM and IM NewWorkDescription: The chapter Revision History in RTD now always remains v1.0 across releases, does not detail the change history, only release name. !image-2025-02-05-17-49-55-576.png|width=592,height=185! There was a request from Functional Safety Manager for it to have unique identification of version for a document, change history briefly explaining changes between versions. Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Step ||Instruction 1.1 Ensure the tag of rtd_docgen before using is: BLN_RTD_DOCGEN_01.00.03* (or newer tag). 1.2 For build_env: please ensure the correct tag of rtd_docgen is in the release manifest. please add the file "{*}revhistory.dox{*}" from the attachment of this ticket to the folder with following path and start adding your context: "..\dev\test\test\specific\<platform>\doc\dox\common\sub_revision_history" decide the "build_env_revision_extra_x.y" id to extend the table for specific release with general info. This info will be printed in all driver manuals. decide the "driver_revision_extra_x.y" id to extend the table for specific release with info from drivers. Inform this id to everyone for each releases. 1.3 For drivers: please add the file "{*}driver_revhistory.dox{*}" from the attachment of this ticket to the folders with following paths: "..\dev\drivers\AutoSAR\<module>\specific\<platform>\doc\dox\um\sub_revision_history" "..\dev\drivers\AutoSAR\<module>\specific\<platform>\doc\dox\im\sub_revision_history" start adding your context inside the id for the release (ask G10 or check the file revhistory.dox* from build_env) Note See the attachment "{*}examples{*}" for an example of how the .dox files will be in the releases. See the attachment "{*}output_expectation{*}" for an example of how the pdf files will be in the releases. See chapter 5 for more information: [link|https://bitbucket.sw.nxp.com/projects/AMPAT/repos/rtd_docgen/commits/512fa07ea4e3148f718ef669ab337953e9a5ff24#docs%2FUserManualDocumentation.pdf] Now, we concentrate on the context/changes for drivers. How can you remember all the necessary changes from the previous release to the current release and put them in driver_revhistory.dox file? Choose {+}one of the following{+}: Use .exe file Step ||Instruction 2.1 Repo sync or clone these tools and put them together in same folder: define_revision_history: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2] 2.2 Open command line in "define_revision_history" folder, enter the command: {code:java} define_revision_history.exe stn define_revision_history product_name RTD platform_name S32R module_name dio pre_path_file E:\UM_IM\RTD_DIO_UM_RTM_2.0.0.pdf cur_path_file E:\UM_IM\RTD_DIO_UM_RTM_3.0.0.pdf o output_folder Where: product_name: RTD platform_name: {_}<take folder specific name from driver's repo>{_}. E.g: S32R pre_path_file: _<path to file1> cur_path_file :_ _<path to file2> 2.3 Check output excel file for the diff (E.g: ..\define_revision_history\output_folder) and start writing your changes in driver_revhistory.dox file. 2.4 Re-generate the manuals and check the chapter Revision History. Ensure the format of the table still follows as the attachment "{*}output_expectation{*}" Note See the readme here for further ways to run the define_revision_history script: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse/docs?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2] Alternative: Use python. Step ||Instruction 2.1 Repo sync or clone these tools and put them together in same folder: define_revision_history: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2] Autotools Framework: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/auto_tool_fw] Common libs: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/common_libs/browse] 2.2 Install python 3.9.13: [https://www.python.org/downloads/release/python-3913/] ({_}A later version of Python can be used, but it was not verified and might have issues{_}) 2.3 Add this python to Path variable. 2.4 Open cmd and run: python m pip install pdfplumber python m pip install Pillow 2.5 Open command line in "auto_tool_fw" folder, enter the command:{code:java} python autotools.py stn define_revision_history product_name RTD platform_name S32R module_name dio pre_path_file E:\UM_IM\RTD_DIO_UM_RTM_2.0.0.pdf cur_path_file E:\UM_IM\RTD_DIO_UM_RTM_3.0.0.pdf o output_folder Where: product_name: RTD platform_name: {_}<take folder specific name from driver's repo>{_}. E.g: S32R pre_path_file: <path to file1> cur_path_file : <path to file2>

ID	Subtype	Headline and Description
		2.6 Check output excel file for the diff (E.g: ..\define_revision_history\output_folder) and start writing your changes in driver_revhistory.dox file. 2.7 Re-generate the manuals and check the chapter Revision History. Ensure the format of the table still follows as the attachment "{*}output_expectation{*}" Note See the readme here for further ways to run the define_revision_history script: [link|https://bitbucket.sw.nxp.com/projects/APNGTOOL/repos/define_revision_history/browse/docs?at=refs%2Ftags%2FPVT_DEFINE_REVISION_HISTORY_01.00.01_V2]
ARTD-179249	Bug	Compiler Options on GHS Compiler for Realtime Cores Detailed description (how to reproduce it): GHS Compiler seems to have a differentiation between the C99 (strict) and c99 (not stric, meaning extensions of c99 are permitted). This situation does NOT apply to DIAB or GCC. The RTD team has the following Guideline mentioning "ISO/IEC 9899:1999 standard and shall compile without warning", however the is no distinction / specification of the terminology "STRICT" being requested. There is a slight chance that "C99" capital letter as the standard and "C99" compiler option (strict) have been wrongly associated in the context of GHS as this is the only compiler that makes the distinction as such. # DIAB and GCC both make use of the "-std=c99" or "-std=c89" or "std=ansi" in the case of strict. # the use of "-pedantic" or "-pedantic-errors" will treat the warnings as errors thus satisfying the second part of the rule " compile without warning" but does not influence the "Strict" part, meaning distinguishing between the C99 ISO Standard and the extensions that it comes with. # Making use of "Strict" = C99 but without extensions means the extensions have to be eliminated in the DIAB and GCC, which is NOT possible, unless the compiler option is actually set to C89 or C90 instead. In conclusion, based on the following information and investigation i believe that the Compiler Option for GHS is not set correctly and needs to be changed. References and information: GHS Compiler Manual DIAB Compiler Manual GCC Compiler Manual IAR Compiler Manual Tasking Compiler manual Standards and definitions of standards: [https://gcc.gnu.org/c99status.html] [https://www.gnu.org/software/gnu-c-manual/gnu-c-manual.html] [https://gcc.gnu.org/onlinedocs/gcc-3.2/gcc/C-Dialect-Options.html] [https://en.wikipedia.org/wiki/C99] !image-2025-04-10-12-23-53-901.png|width=451,height=420! Preconditions: Build Test Case ID (internal TC that caught the defect) optional: To be confirmed Observed behavior: Due to inconsistency of Compiler options and the differences between different compilers, they are NOT currently aligned. Expected behavior: Build should run with ISO C99 as "c99 " for GHS. ISO C 99 is followed with no warnings and errors but there is no reference of "Strict". Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the RTD Compiler options accordingly to use c99 instead of C99.
ARTD-179716	New Feature	[Port][S32K3] NotUsedPortPin: Consider new mode option to don't touch all of non-configured signals NewWorkDescription: If a pin wasn't configure in PortContainer, it will be set by Port_Init with the configuration in NotUsedPortPin. Right now, NotUsedPortPin has 2 mode options: GPIO and ALT0. Please consider a use-case that user won't touch to this pin, leave this pin with default configuration at Power-Of-Reset Requirement source: None (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: None
ARTD-179722	Bug	[port][S32K3] Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid. In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached.

ID	Subtype	Headline and Description
		Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. Otherwise, we can use this command to enable case sensitive for all created subfolders and no need to renew them: "(Get-ChildItem foldername Recurse Directory).Fullname ForEach-Object {fsutil file setCaseSensitiveInfo "$_" enable}" # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-179725	Bug	[gpt][S32K3] Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid. In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached. Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. Otherwise, we can use this command to enable case sensitive for all created subfolders and no need to renew them: "(Get-ChildItem foldername Recurse Directory).Fullname ForEach-Object {fsutil file setCaseSensitiveInfo "$_" enable}" # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-180020	New Feature	[I2C] Address CPR_RTD_00543 (MR200) for requirements and implementation Context: Clarify MR200 / CPR_RTD_00543 to either be included for the next K1 release or permanently excluded.

ID	Subtype	Headline and Description
		Decided to : 1. keep the requirement excluded for k1 3.0.0 as it was on previouse release 2. clone the ticket for all drivers in RTD with scope of addressing the implementation on any next release (any NPI) and not keeping on excluded requirements Action needed on driver level: Update Variant attribure for the internal requirement CPR_RTD_00543 to be consistent with generic {*}Verify if implementation exist{*}s or need an implementation ticket in ARTD to adress it. If is needed please create artd ticket and inform group owner.
ARTD-180023	New Feature	S32K3: Add automatic migration of Pin config to Port HLD NewWorkDescription: Users create the pinmux allocation for their board using the Pin config tool in S32DS. However, the work done in Pin config tool cannot be easily exported to an Autosar environment, as Port HLD pin list needs to be filled manually. This becomes hardwork for 200 pins, and for sure could be automated by S32CT, as all the needed info exists in the Pin config tool. Requirement source: Customer request. (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-180027	New Feature	S32K3 High Current in Sleep mode customer failures caused by the default RTD port driver for non used pins. Detailed description (how to reproduce it): When the device is commanded to go into sleep mode, the current consumption is not within the limits when the default port driver configuration for non used pins is used, the challenge is that not every device will show this behavior even with the input buffers enabled. This makes hard for NXP customers to identify the problem before releasing their product. Preconditions: Customer using the default RTD port driver configuration for non used pins. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: High Current consumption Expected behavior: Current consumption within the characterized limits. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change the default port configuration for non used pins from "Input" to "Disabled" to be in alignment with NXP hardware design guidelines for non used pins.
ARTD-180063	Bug	[ADC] Remove the code not applicable for S32K3XX platform Detailed description (how to reproduce it): Now in LDRA summary report, there are many functions have code exposure equal 0%. After review. I saw those functions are not supported on S32K3XX platform but still be present inside the plugin Detail functions: (red line) !image-2025-04-16-09-08-17-729.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Functions not supported on the platform but still exist in the plugin. Expected behavior: No function has CE = 0% in the LDRA report Proposed solution optional: N/A
ARTD-180072	Bug	[S32K3_S32M27x 6.0.0][CRC]: Fix finding on review checklists Detailed description (how to reproduce it): Design and coding violate the convention. Detailed finding are list on this ticket: ARTD-132116 Preconditions: S32K3_S32M27x 6.0.0

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Have violations. Expected behavior: Have no violation. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-180096	New Feature	[MCL] Update driver code to support CPR_RTD_00543 (MR200) for S32K3 platform NewWorkDescription: Update driver code to support CPR_RTD_00543 (MR200) for S32K3 platform. Proposed solution optional: Flow step by step according to section 14. Fulfilling MR 200 in document [NXP_RTD_AUTOSAR_S32CT_V2.pptx|https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDIRvDlnrzP1m0TZ9elQ?e=ZW2eJw] to implement for CT generation code.
ARTD-180143	Bug	[ICU]Missing WKPU_CH_35 channel for S32K396 derivative Detailed description (how to reproduce it): In the file S32K39_and_S32K37_IOMUX.xlsx, there is a WKPU[35] pin that can be used as an input pin and this channel can be used for S32K396_289bga !image-2025-04-16-11-00-47-862.png! !image-2025-04-16-10-55-47-983.png! Preconditions: review file S32K39_and_S32K37_IOMUX.xlsx Test Case ID (internal TC that caught the defect) optional: review file S32K39_and_S32K37_IOMUX.xlsx Observed behavior: Missing WKPU_CH_35 channel for S32K396_289bga Expected behavior: add WKPU_CH_35 channel for S32K396_289bga Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add WKPU_CH_35 channel to file CORTEXM_S32K3XX_s32k396_mapbga289.properties
ARTD-180160	New Feature	[SPI] Implement CPR_RTD_00543 (MR200) for Spi NewWorkDescription: Implement CPR_RTD_00543 (MR200) for Spi. Requirement source: CPR_RTD_00543 (MR200) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-180222	New Feature	[CanTrcv] Introduce ASR R23-11 Description:_* Analyse, Implement and test Autosar R23-11 for RTD driver. {_}*Consider the following steps*{_}: Review the needed changes for driver based on : [2024.03.29 ASR R21-11 vs ASR R23-11|https://nxp1.sharepoint.com/:f:/r/sites/Zebra/Shared%20Documents/Requirements/2024.03.29%20-%20ASR%20R21-11%20vs%20ASR%20R23-11?csf=1&web=1&e=hlNN14], analyse for all NPIs affected Create linked tickets for spliting and isolating the activities for driver Check driver dev test/example into Tresos 30.0.0 and verify import/export of epc/epd into and from S32DS 3.6 Implement support for R23-11 while maintaining the possibility of delivering the R21-11 driver (proposals: use #ifdef in code, use different files for generic to separate version support, but keep in mind that LKOB shall be generated consistenly for the generic code and maintainance effort shall be minimized as much as possible) Create linked ticket in AAI for ELM requirements review after initial import in component (the import will be done by ReqManagers and will be signaled via email)

ID	Subtype	Headline and Description
		References: Standard documents : [AutosarR23-11|https://nxp1.sharepoint.com/:f:/s/Zebra/Es-F1VPsDOpGhUItnPxgrnEB1MEuybLYg0ZxMsLw2hfT1g?e=WvpBt2] Overview of the changes: [AUTOSAR_CP_TR_ReleaseOverview|https://nxp1.sharepoint.com/:b:/s/Zebra/EWVln3nMqVZFjRbcQOoqkbYBelhV8kq5Siw5jw0Yod2XRg?e=PfOoRY] Technical recommendations: [AUTOSAR support for SW products.pptx|https://nxp1.sharepoint.com/:p:/s/APPlatformArchitectureGroup/EenK9FOp6HBBvHWNfgI5z4YB8ZWAtLTGVSLQbkM9IJqkkg?e=NvMZO9]
ARTD-180679	New Feature	[S32K3xx_S32M27x_6.0.0][MEM_EXFLS]: Review and update driver according to Traceability reports NewWorkDescription: The traceability isn't 100%, there are requirements are not covered. !https://bitbucket.sw.nxp.com/rest/api/1.0/projects/ARTD/repos/mem_exfls/attachments/118265|width=845,height=407! Requirement source: ASR SWS, ELM7 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update driver code and design to cover requirements
ARTD-180540	Bug	[dio] Implement check on partition assigned for correctness or out of bounds accesses Detailed description (how to reproduce it): It was noticed that some drivers do not implement all the checks needed for partition id information in multicore context. Some are missing the check on the correctness partition callee some are not testing for out of bounds accesses in configuration arrays. Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are cases not covered that may results in null pointer accesses or wrong accesses. Expected behavior: Cover all corner cases. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) {*}Proposed solution{*}: 1. All drivers must check if the calee ECUC partition ID is assigned to the used configuration resource/channel/instance of the driver. Example: {*}Cover NULL_PTR partition access{*}: DriverEcucPartitionRef uses the partition number 2, but the driver receives the ID for partition 4. DET MSN_E_PARAM_CONFIG error should be raised 2. All drivers must check if the calee ECUC partition ID is not higher than the maximum number of ECUC partitions stored in configuration. Example: {*}Cover out of range partition ID access{*}: ECUC declares N partitions, driver receives partition number N+1. DET MSN_E_PARAM_CONFIG error should be raised. ======= 3. Base driver must replace the macro for getting UserID with an inline function which checks if the ApplicationID received from OS is not out of bounds. (No action necessary for other drivers) 4. Base driver must replace the call to GetApplicationID with GetCurrentApplicationID. (No action necessary for other drivers)
ARTD-180543	Bug	[dpga] Implement check on partition assigned for correctness or out of bounds accesses Detailed description (how to reproduce it): It was noticed that some drivers do not implement all the checks needed for partition id information in multicore context. Some are missing the check on the correctness partition callee some are not testing for out of bounds accesses in configuration arrays. Preconditions: None

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are cases not covered that may results in null pointer accesses or wrong accesses. Expected behavior: Cover all corner cases. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) {*}Proposed solution{*}: 1. All drivers must check if the calee ECUC partition ID is assigned to the used configuration resource/channel/instance of the driver. Example: {*}Cover NULL_PTR partition access{*}: DriverEcucPartitionRef uses the partition number 2, but the driver receives the ID for partition 4. DET MSN_E_PARAM_CONFIG error should be raised 2. All drivers must check if the calee ECUC partition ID is not higher than the maximum number of ECUC partitions stored in configuration. Example: {*}Cover out of range partition ID access{*}: ECUC declares N partitions, driver receives partition number N+1. DET MSN_E_PARAM_CONFIG error should be raised. ======= 3. Base driver must replace the macro for getting UserID with an inline function which checks if the ApplicationID received from OS is not out of bounds. (No action necessary for other drivers) 4. Base driver must replace the call to GetApplicationID with GetCurrentApplicationID. (No action necessary for other drivers)
ARTD-180549	Bug	[eth] Implement check on partition assigned for correctness or out of bounds accesses Detailed description (how to reproduce it): It was noticed that some drivers do not implement all the checks needed for partition id information in multicore context. Some are missing the check on the correctness partition callee some are not testing for out of bounds accesses in configuration arrays. Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are cases not covered that may results in null pointer accesses or wrong accesses. Expected behavior: Cover all corner cases. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) {*}Proposed solution{*}: 1. All drivers must check if the calee ECUC partition ID is assigned to the used configuration resource/channel/instance of the driver. Example: {*}Cover NULL_PTR partition access{*}: DriverEcucPartitionRef uses the partition number 2, but the driver receives the ID for partition 4. DET MSN_E_PARAM_CONFIG error should be raised 2. All drivers must check if the calee ECUC partition ID is not higher than the maximum number of ECUC partitions stored in configuration. Example: {*}Cover out of range partition ID access{*}: ECUC declares N partitions, driver receives partition number N+1. DET MSN_E_PARAM_CONFIG error should be raised. ======= 3. Base driver must replace the macro for getting UserID with an inline function which checks if the ApplicationID received from OS is not out of bounds. (No action necessary for other drivers) 4. Base driver must replace the call to GetApplicationID with GetCurrentApplicationID.

ID	Subtype	Headline and Description
		(No action necessary for other drivers)
ARTD-180603	Bug	[LinTrcv] Implement check on partition assigned for correctness or out of bounds accesses Detailed description (how to reproduce it): It was noticed that some drivers do not implement all the checks needed for partition id information in multicore context. Some are missing the check on the correctness partition callee some are not testing for out of bounds accesses in configuration arrays. Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are cases not covered that may results in null pointer accesses or wrong accesses. Expected behavior: Cover all corner cases. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) {*}Proposed solution{*}: 1. All drivers must check if the calee ECUC partition ID is assigned to the used configuration resource/channel/instance of the driver. Example: {*}Cover NULL_PTR partition access{*}: DriverEcucPartitionRef uses the partition number 2, but the driver receives the ID for partition 4. DET MSN_E_PARAM_CONFIG error should be raised 2. All drivers must check if the calee ECUC partition ID is not higher than the maximum number of ECUC partitions stored in configuration. Example: {*}Cover out of range partition ID access{*}: ECUC declares N partitions, driver receives partition number N+1. DET MSN_E_PARAM_CONFIG error should be raised. ======= 3. Base driver must replace the macro for getting UserID with an inline function which checks if the ApplicationID received from OS is not out of bounds. (No action necessary for other drivers) 4. Base driver must replace the call to GetApplicationID with GetCurrentApplicationID. (No action necessary for other drivers)
ARTD-180624	Bug	[messaging] Implement check on partition assigned for correctness or out of bounds accesses Detailed description (how to reproduce it): It was noticed that some drivers do not implement all the checks needed for partition id information in multicore context. Some are missing the check on the correctness partition callee some are not testing for out of bounds accesses in configuration arrays. Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are cases not covered that may results in null pointer accesses or wrong accesses. Expected behavior: Cover all corner cases. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) {*}Proposed solution{*}: 1. All drivers must check if the calee ECUC partition ID is assigned to the used configuration resource/channel/instance of the driver. Example: {*}Cover NULL_PTR partition access{*}: DriverEcucPartitionRef uses the partition number 2, but the driver receives the ID for partition 4. DET MSN_E_PARAM_CONFIG error should be raised

ID	Subtype	Headline and Description
		2. All drivers must check if the calee ECUC partition ID is not higher than the maximum number of ECUC partitions stored in configuration. Example: {*}Cover out of range partition ID access{*}: ECUC declares N partitions, driver receives partition number N+1. DET MSN_E_PARAM_CONFIG error should be raised. ======= 3. Base driver must replace the macro for getting UserID with an inline function which checks if the ApplicationID received from OS is not out of bounds. (No action necessary for other drivers) 4. Base driver must replace the call to GetApplicationID with GetCurrentApplicationID. (No action necessary for other drivers)
ARTD-180642	Bug	[port] [S32K3XX] Implement check on partition assigned for correctness or out of bounds accesses Detailed description (how to reproduce it): It was noticed that some drivers do not implement all the checks needed for partition id information in multicore context. Some are missing the check on the correctness partition callee some are not testing for out of bounds accesses in configuration arrays. Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are cases not covered that may results in null pointer accesses or wrong accesses. Expected behavior: Cover all corner cases. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) {*}Proposed solution{*}: 1. All drivers must check if the calee ECUC partition ID is assigned to the used configuration resource/channel/instance of the driver. Example: {*}Cover NULL_PTR partition access{*}: DriverEcucPartitionRef uses the partition number 2, but the driver receives the ID for partition 4. DET MSN_E_PARAM_CONFIG error should be raised 2. All drivers must check if the calee ECUC partition ID is not higher than the maximum number of ECUC partitions stored in configuration. Example: {*}Cover out of range partition ID access{*}: ECUC declares N partitions, driver receives partition number N+1. DET MSN_E_PARAM_CONFIG error should be raised. ======= 3. Base driver must replace the macro for getting UserID with an inline function which checks if the ApplicationID received from OS is not out of bounds. (No action necessary for other drivers) 4. Base driver must replace the call to GetApplicationID with GetCurrentApplicationID. (No action necessary for other drivers)
ARTD-180666	Bug	[uart] Implement check on partition assigned for correctness or out of bounds accesses Detailed description (how to reproduce it): It was noticed that some drivers do not implement all the checks needed for partition id information in multicore context. Some are missing the check on the correctness partition callee some are not testing for out of bounds accesses in configuration arrays. Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are cases not covered that may results in null pointer accesses or wrong accesses. Expected behavior:

ID	Subtype	Headline and Description
		Cover all corner cases. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) {*}Proposed solution{*}: 1. All drivers must check if the calee ECUC partition ID is assigned to the used configuration resource/channel/instance of the driver. Example: {*}Cover NULL_PTR partition access{*}: DriverEcucPartitionRef uses the partition number 2, but the driver receives the ID for partition 4. DET MSN_E_PARAM_CONFIG error should be raised 2. All drivers must check if the calee ECUC partition ID is not higher than the maximum number of ECUC partitions stored in configuration. Example: {*}Cover out of range partition ID access{*}: ECUC declares N partitions, driver receives partition number N+1. DET MSN_E_PARAM_CONFIG error should be raised. ======= 3. Base driver must replace the macro for getting UserID with an inline function which checks if the ApplicationID received from OS is not out of bounds. (No action necessary for other drivers) 4. Base driver must replace the call to GetApplicationID with GetCurrentApplicationID. (No action necessary for other drivers)
ARTD-180724	New Feature	[IMPLEMENTATION] Use eTPU TCR clock in calculation of PWM period for eTPU hardware channels CR description:_* This CR is based on the dependency ticket ARTD-162694. The calculation of PWM period in the PWM plugin for eTPU hardware channels should be updated to correctly calculate the period in ticks from period entered in seconds. Currently, if the Period in Ticks option is not enabled (1 see the picture) and thus the Default Period (2) is entered in seconds, the actual period in ticks is calculated using the MCU clock reference (3). !pwm_1.png! However, the correct ticks value should be calculated using eTPU counter frequency, obtained from the Etpu plugin. This frequency depends on eTPU clock source and prescaler selection, and also on the Etpu Channel ID (whether it is on Engine A or B) and on Etpu Channel Time Base selection in Etpu Hardware Channel definition (see picture below): !pwm2.png! The algorithm for obtaining correct clock frequency is as follows: IF Etpu Channel ID contains Engine A IF Etpu Channel Time Base == ETPU_PWM_TIME_BASE_TCR1 Use Engine A TCR1 Clock Frequency (from Etpu/EtpuEngineASettings/EngineATimeBase1/EngATcr1ClockValue node) ELSE Use Engine A TCR2 Clock Frequency (from Etpu/EtpuEngineASettings/EngineATimeBase2/EngATcr2ClockValue node) ELSE The same IF-ELSE for Etpu Channel Time Base but using Engine B TCR1/2 clock values. The picture shows Engine A TCR1 Clock Frequency configuration in Etpu plugin. !etpu_tcr1.png! The calculation should be updated in ip\IPV_Etpu\generate\ETB\Etpu_Pwm_Ip_RegOperations.m file. For reference, please see the MotorControl code in: ip\IP_Etpu\generate\EBT\Etpu_As_Ip_RegOperations.m The Etpu clock for Engine A or B based on the Etpu channel is obtained as follows: !etpu_code_tcr.png! If possible, the MCU clock reference in PWM channel should be disabled to indicate to the user that this value is not used in case of Etpu hardware channel.

ID	Subtype	Headline and Description
		This task applies both to EB Tresos and DS32 Config Tool. Requirement for the Etpu plugin parameters that should be used in the PWM plugin: [https://elm.nxp.com/rm/resources/TX_i0QaYOkmEe-qaNWesERhZw?oslc_config.context=https%3A%2F%2Felm.nxp.com%2Frm%2Fcm%2Fstream%2F_vUxd0P4vEe2ulZM7bgVqfQ] Related task in MotorControl plugin: [https://jira.sw.nxp.com/browse/ETPUSW-1419] MotorControl repository: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/motor_control/browse] Reason for this change: The period in ticks should be calculated correctly. Benefit: The Pwm channels that use eTPU hardware will operate with correct period as defined in the configuration. Onetime CR/Strategic CR: [text placeholder]_ Use-case: [text placeholder] HW documentation reference (as applies): [text placeholder]_ HW/Application Engineer contact (as applies): [text placeholder]_ Note: relevant documents to be attached to the ticket.
ARTD-180798	New Feature	[IMPLEMENTATION] [S32K3] RTD IP Level CAN-FD RAM Partition Sizing CR description:_* Customer is Ford is requesting: The three RAM partitions for CAN-FD should be able to have different Payload Sizes. In AUTOSAR context: !image-2024-06-21-09-07-00-295.png|thumbnail! In generated file: !image-2024-06-21-09-07-56-956.png|thumbnail! In non-AUTOSAR: !image-2024-06-21-08-30-26-331.png|thumbnail! In generated file: !image-2024-06-21-08-31-42-024.png|thumbnail! So, the customer want to request this feature for non ASR (IP layer) also. This if for all derivatives of S32K3XX. Reason for this change: Can change number of MB depends on payload size can be configured for each MB. Benefit: It makes sense to update the RTD as more customers move away from Autosar. Enable customer usecases Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): NA

ID	Subtype	Headline and Description
		HW/Application Engineer contact (as applies): Scott Obrien [scott.obrien@nxp.com] Note: relevant documents to be attached to the ticket.
ARTD-180815	Bug	[ADC] Fix failed run on manifest for TRAIN Detailed description (how to reproduce it): Using probe to run ADC_TS_000 causes error that stuck in Sys_Init (SVChandler API) Test Case ID (internal TC that caught the defect) optional: ADC_TS_000 of SAF86 !image-2025-04-18-09-46-02-034.png!!image-2025-04-18-09-46-16-843.png!
ARTD-180896	Bug	[PWM] Trust function is not needed for FlexPwm Detailed description (how to reproduce it) Because FlexPwm does not have a protect register. So the driver will not support IPV_Pwm_Ip_TrustedFunctions.h !image-2025-04-21-14-04-54-198.png|width=903,height=108! However{*}, FlexPwm_Ip_ClrUserAccessAllowed{*} and FlexPwm_Ip_SetUserAccessAllowed are using in FlexPwm_Ip.c !image-2025-04-18-10-21-16-546.png|width=736,height=255! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: TC_002 Observed behavior: FlexPwm_Ip_ClrUserAccessAllowed and FlexPwm_Ip_SetUserAccessAllowed are using in FlexPwm_Ip.c Expected behavior: Remove function FlexPwm_Ip_ClrUserAccessAllowed and ** *FlexPwm_Ip_SetUserAccessAllowed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-180915	New Feature	[IMPLEMENTATION][S32K3] CLONE - FlexCAN driver needs support "MIXED" Can ID Message Type CR description:*_ This request comes from customer LGE. They encountered scenarios where they needed to use "MIXED" MB type when using FlexCAN, but FlexCAN's driver currently cannot distinguish between "Extended" and "Mixed" MB types for receiving way. !image-2024-04-03-10-00-50-748.png|width=562,height=71! There are burst RX CAN frames coming from vehicle diagnostic device for ECU reprogramming. S32G2 FlexCAN receives the burst RX CAN frames. S32G2 routes CAN frames to destination ECU. So FIFO method is necessary to avoid can frame drop. Legacy FIFO or Enhanced FIFO is applied. There are various destination devices with standard-id and extended-id. FlexCAN FIFO feature can recevie only one can id type. Both Standard-id filter and extended-id should be supported at the same time. Standard-id filter and extended-id filter should be configured separately in the filter table as the below picture. Standard-id and extended-id should be received to FIFO at the same time. !image-2024-04-04-10-05-16-260.png|width=614,height=281! Reason for this change: [text placeholder]_ — Benefit: [text placeholder]_ Onetime CR/Strategic CR: [text placeholder]_ Use-case: [text placeholder]

ID	Subtype	Headline and Description
		HW documentation reference (as applies): [text placeholder]_ HW/Application Engineer contact (as applies): [text placeholder]_ Note: relevant documents to be attached to the ticket.
ARTD-180925	Bug	[ETH] Exclude trusted function out of platform that not has register to protect Detailed description (how to reproduce it): S32K3XX don't have register to protect. So, we don't need trusted function: !image-2025-04-18-13-59-57-303.png! Some function have CE = 0%. please check and hidden these function if not support for S32K3XX. Please check detail in file CodeCoverage_Sumary.xlsx !image-2025-04-18-14-12-12-064.png! Please check other platform. Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Remove these function out of this platform and CE not equal 0 when run CCOV. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-180941	Bug	[S32K3xx_S32M27x_6.0.0][WDG] Swt_Ip_Unlock() caused Hard Fault when unlock operation is unsuccessful Detailed description (how to reproduce it): Set SLB in CR of SWT before initializing SWT Invoke Swt_Ip_Init() > Swt_Ip_Unlock() in Swt_Ip_Unlock, comment second unlock command to make unlock fail condition Preconditions: Test Case ID (internal TC that caught the defect) optional: Ip_Swt_TS_010 Observed behavior: Swt_Ip_Unlock() caused Hard Fault after re-locking SWT when unlock operation is unsuccessful, as following figure: !image-2025-04-18-16-32-28-062.png|thumbnail! Expected behavior: Swt_Ip_Unlock() does not cause Hard Fault when unlock operation is unsuccessful Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-180945	Bug	[ICU]Functions Cmp_Ip_EnableInterrupt and Cmp_Ip_DisableInterrupt do not enable and disable RRF_IE bit when used Detailed description (how to reproduce it): when using the Cmp_Ip_EnableInterrupt and Cmp_Ip_DisableInterrupt functions to enable and disable the RRF_IE bit (Round-Robin Flag Interrupt Enable) bit, but these 2 functions are not doing this: !image-2025-04-18-17-03-03-951.png! !image-2025-04-18-17-03-27-434.png! Preconditions: Use LCMP channels in Trigger mode common issue that occurs in all derivatives Test Case ID (internal TC that caught the defect) optional: Ip_Cmp_TC_FCT_4005(Ip_Cmp_TS_194)

ID	Subtype	Headline and Description
		Icu_TC_FCT_3105(Icu_TS_116) Observed behavior: Functions Cmp_Ip_EnableInterrupt and Cmp_Ip_DisableInterrupt do not enable and disable RRF_IE bit when used Expected behavior: The Cmp_Ip_EnableInterrupt and Cmp_Ip_DisableInterrupt functions need to enable and disable the RRF_IE bit when used. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to enable and disable RRF_IE bit in trigger mode when using 2 functions Cmp_Ip_EnableInterrupt and Cmp_Ip_DisableInterrupt
ARTD-180952	Bug	[S32K3xx_S32M27x_6.0.0][PLATFORM]: S32K389 Error on linker flash of IAR Detailed description (how to reproduce it): Error on Linker Flash of IAR already defined: symbol int_flash_fls_rsv_start !image-2025-04-21-08-19-38-087.png! Preconditions: S32K389, linker Flash of IAR Test Case ID (internal TC that caught the defect) optional: Platform_TS_COT_LK_flash Observed behavior: already defined: symbol int_flash_fls_rsv_start Expected behavior: Build pass with linker IAR Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Redefine int_flash_fls_rsv_region
ARTD-181004	Bug	[S32K3xx_S32M27x_6.0.0][MESSAGING]: Remove redundant mailboxes on S32K389 Detailed description (how to reproduce it): Tag: PVT_MESSAGING_IPCF_FSS_RTD_INTEGRATION_02 According to S32K3xx Reference Manual, Rev. 9, 07/2024, currently supports 4 mailboxes for each transmit and receive channel of MUA and MUB !image-2025-04-21-11-05-26-725.png! S32K389 MessagingMuTransmittingChannel: currently allowing 7 mailboxes to be selected !image-2025-04-21-10-59-02-142.png! Preconditions: redundant mailbox configuration Test Case ID (internal TC that caught the defect) optional: Messaging_Mu_TS_001 Observed behavior: hardfault when configuring mailboxes not support Expected behavior: cannot config out range Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: clear all mailboxs not
ARTD-181177	Bug	[S32K3xx_S32M27x_6.0.0][MEM_INFLS]: ECC error test cause hardfault with user mode configuration Detailed description (how to reproduce it): Hardfault when call C40_Ip_GetPflashDataErrorSuppressionStatus with user mode configuration Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_0012

ID	Subtype	Headline and Description
		Observed behavior: N/A Expected behavior: Call function by OsIf_Trusted_Call Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-181247	Bug	[MEM_EEP] [S32K3XX] Compiler Warning on S32K3XX Detailed description (how to reproduce it): Detail on exel file Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Mem_TC_FCT_0004 Observed behavior: Compile warning in plugin Expected behavior: No compile warning in plugin Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-181250	Bug	[GPT][S32K3] DataAbort_Handler when call Gpt_Init function Detailed description (how to reproduce it): Driver jump to DataAbort_Handler() after call Gpt_ValidateParamPtrInit() in Gpt_Init() function: at line 877: in case of configuration with Precompile, configPtr = NULL so then driver try to call configPtr->u32PartitionId which is incorrect !image-2025-04-22-15-58-16-748.png! Preconditions: Call Gpt_Init() function with NULL_PTR and GPT_MULTIPARTITION_ENABLED == STD_ON Test Case ID (internal TC that caught the defect) optional: Gpt_TS_002_cfg3 Observed behavior: Drive jump to DataAbort_Handler() Expected behavior: Call Gpt_Init() fucntion success Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-181392	Bug	[S32K3_600] [CRC] Wrong implementation of req SWS_Crc_00072 Detailed description (how to reproduce it): In API function of CRC library, we shouldn't use BSW module as Det(description in SWS_Crc_00072 req) !image-2025-04-23-14-18-26-548.png! !image-2025-05-07-11-08-12-287.png! !image-2025-05-07-11-08-48-373.png! !image-2025-05-07-11-09-15-740.png! !image-2025-05-07-11-09-50-463.png! Observed behavior: Wrong implementation Expected behavior: Dev update driver code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-181408	Bug	[WDG] endif positioned wrongly Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		[in Wdg_EnvCfg.h there is an issue with the position of #endif , which can be fixed as shown on the right side. !image-2025-04-15-16-15-44-973.png!] Preconditions: [none] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [build error] Expected behavior: [no \\\{*}build error\\\{*}] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [see in picture]
ARTD-181417	Bug	[MCL] Trusted functions in the MCL plugin have not been included in the trusted header file Detailed description (how to reproduce it): Trusted functions below in the MCL plugin have not been included in the trusted header file*_ Mcl_Dma_SetUserAccessAllowed hwAcc_ArmCoreRx_DataCacheClean hwAcc_ArmCoreRx_DataCacheCleanByAddr hwAcc_ArmCoreRx_DataCacheDisable hwAcc_ArmCoreRx_DataCacheEnable hwAcc_ArmCoreRx_DataCacheInvalidate hwAcc_ArmCoreRx_DataCacheInvalidateByAddr hwAcc_ArmCoreRx_InstructionCacheClean hwAcc_ArmCoreRx_InstructionCacheCleanByAddr hwAcc_ArmCoreRx_InstructionCacheDisable hwAcc_ArmCoreRx_InstructionCacheEnable hwAcc_ArmCoreRx_InstructionCacheInvalidate hwAcc_ArmCoreRx_InstructionCacheInvalidateByAddr Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: TC_002 in int module Observed behavior: Some Trusted functions in the MCL plugin have not been included in the trusted header file Expected behavior: Add them in the trusted header file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-181411	Bug	[S32K3xx_S32M27x_6.0.0][ICU]: Incorrect resource for some derivertive with IpV WKPU Detailed description (how to reproduce it): Some resource file for derivertive K3 need update: Derivertive have one core but in resource have two core for Icu.IcuConfigSet.IcuChannel.IcuHwChannel.IcuWkpuCoresSupport: S32K312, S32K341, S32K342, S32K314, S32K344 Derivertive have tow core but in resource have three core for Icu.IcuConfigSet.IcuChannel.IcuHwChannel.IcuWkpuCoresSupport: S32K324 !image-2025-04-23-15-40-56-511.png! !image-2025-04-24-09-33-28-629.png! Some channel WKPU not support but still have in resource some derivertive: S32K311: WKPU[30], WKPU[34] > WKPU[63] S32K312, S32K341, S32K342, S32K322: WKPU[35], WKPU[60], WKPU[61], WKPU[62], WKPU[63] S32K344, S32K324, S32K314, S32K358, S32K348, S32K338, S32K328, S32K388: WKPU[60], WKPU[61], WKPU[62], WKPU[63] !image-2025-04-23-16-05-06-312.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: Update corect resource

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update resource folow RM and IO MUX file
ARTD-181447	Bug	[S32K3][MEM_EXFLS] Missing trusted function in header file Detailed description (how to reproduce it): Qspi_Ip_SetAhbSeqWriteId_Privileged function is missing in Qspi_Ip_TrustedFunctions.h !image-2025-04-23-18-49-08-172.png! Preconditions: user mode enabled Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_COT_014 Observed behavior: as description Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: refer to ARTD-16450
ARTD-181497	Bug	[ETH] Maintain CPR_RTD_00543/MR200 implementation Detailed description (how to reproduce it): CPR_RTD_00543 needed to be checked and maintained. for example on K3XX(just a quick finding, not all), when both HLD and IP components added, EthEnableCacheManagement is not enabled in HLD but enabled in IP, GMAC_HAS_CACHE_MANAGEMENT should be STD_ON, but STD_OFF !image-2025-04-24-10-59-43-684.png|thumbnail! Preconditions: add both HLD and IP components into same project Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: build failed/code gen unexpected Expected behavior: build passed/code gen as expected Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: check and maintain CPR_RTD_00543/MR200
ARTD-181603	Bug	[BASE] Different between Tresos and S32DS generator on compare_code_gen Detailed description (how to reproduce it): Some different between code generated by EB_tresos and S32DS as below: !image-2025-04-24-16-54-40-068.png! !image-2025-04-24-16-54-24-628.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Base_TS_001 Observed behavior: Expected behavior: No different appear Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-181628	Bug	[S32K3xx_S32M27x_6.0.0][MESSAGING]: Build fail due to too many initializer values Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Build fail GHS due to too many initializer values Preconditions: Messaging_Ipw_CfgType struct has one variable !image-2025-04-24-23-58-12-362.png! But code generate has two variable !image-2025-04-25-00-01-29-634.png! Test Case ID (internal TC that caught the defect) optional: Messaging_TS_001 Observed behavior: build fail ghs !image-2025-04-25-00-02-29-025.png! Expected behavior: build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [..]
ARTD-181643	Bug	S32K3: PORT_CODE_SIZE_OPTIMIZATION generate STD_ON even for derivatives not K310, K311, K312 Detailed description (how to reproduce it): #define PORT_CODE_SIZE_OPTIMIZATION (STD_ON) when: 1. Change resource to S32K312 2. Enable Code Size Optimization 3. Change resource to S32K314 4. Generate code Preconditions: PORT_422 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: #define PORT_CODE_SIZE_OPTIMIZATION (STD_ON) Expected behavior: #define PORT_CODE_SIZE_OPTIMIZATION (STD_OFF) for S32K314 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-181656	Bug	[PWM][ETPU] Fix run-time error caused by constant identifier in init and config structures Detailed description (how to reproduce it): Create, build and run code with Etpu_Pwm. Preconditions: Build option: Debug_Flash Test Case ID (internal TC that caught the defect) optional: Observed behavior: After initialization of Etpu_Pwm, CPU goes to HardFault caused by writing data to structure marked as const. Expected behavior: Code will generate PWM by using Etpu. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Remove const identifier in Etpu_Pwm_Ip_Instance and Etpu_Pwm_Ip_Config structures in configurations for EBT and UCT. !image-2025-04-25-09-26-07-335.png! !image-2025-04-25-09-26-50-199.png!
ARTD-181785	Bug	[S32K3xx_S32M27x_6.0.0][ICU]: User mode not support for IpVaults Emios, Cmp and Wkpu so node use mode should be dissable in S32DS interface

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): User mode not support for Ivp Emios, Cmp and Wkpu so node use mode should be dissable in S32DS interface:{*}{*} !image-2025-04-26-13-58-53-607.png! !image-2025-04-26-13-57-56-424.png! !image-2025-04-26-13-59-16-890.png! !image-2025-04-26-13-59-41-790.png! Preconditions: S32DS Test Case ID (internal TC that caught the defect) optional: Icu_TS_035 Observed behavior: N/A Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-181812	Bug	S32K3_M27x 6.0.0] [[AE] There are slight errors in File Version Check Detailed description (how to reproduce it): in CDD_Ae_Ipw_Cfg.h, the error message of File Version Check shoube be #error "CDD_Ae_Ipw_Cfg.h and CDD_Ae_Cfg.h have different vendor ids" !image-2025-04-26-15-31-35-568.png! The same in CDD_Ae_Ipw_VS_0_PBcfg.c !image-2025-04-26-15-34-13-261.png! Preconditions: n/a Test Case ID (internal TC that caught the defect) optional: Ae_TS_001 Observed behavior: Compare_code_gen test failed Expected behavior: Compare_code_gen test passed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-181815	Bug	[MEM_EEP] [S32K3XX] Redundant DET line in driver Detailed description (how to reproduce it): !image-2025-04-26-15-42-26-599.png|width=543,height=245! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Mem_TC_FCT_0005 Observed behavior: Redundancy det error in driver, Line 963 in file Mem_43_EEP.c Expected behavior: Driver does not have line 963 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Clear line 963
ARTD-181824	Bug	[S32K3XX_S32M27x_6.0.0][MEM_EXFLS] Hardfault occurs on iar compiler Detailed description (how to reproduce it): hard fault occurred on tests compiled by iar compiler !image-2025-04-26-16-04-06-774.png!

ID	Subtype	Headline and Description
		Preconditions: compiled by iar AHB region (start from 0x68000000) is configured as cacheable Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_101 Observed behavior: as description Expected behavior: no hardfault Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: After configuring the AHB region as a non-cacheable region, as specified in the S32G Reference Manual, no hardfault occur !image-2025-04-26-16-14-04-469.png! Please investigate this and ask the RM team if there is a missing note about this limitation in the S32K3 RM Solution: Add barrier to sync instruction and data when enable AHB read Add note to config AHB cache when initialize driver in UM
ARTD-181929	Bug	[ETH] implement CPR_RTD_00011.eth for GMAC_CommonIRQHandler Detailed description (how to reproduce it): need to check if driver initialized before access Gmac_apxState !image-2025-04-28-09-31-19-707.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Gmac_apxState is not checked before access it Expected behavior: Gmac_apxState is checked, if NULL_PTR then clear IFLAG and exit from ISR Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-181954	New Feature	[Mem_InFls] [S32K3_S32M27x_6.0.0] Update the driver following the new update of header files for S32K3XX_S32M27x. NewWorkDescription: The header file have the new update in the ticket ARTD-181521 So Mem_InFls driver need to following update due to have new header for S32K36.h The resource file of derivatives (S32K364, S32K366) need to following update. Requirement source: Follow the change in the ticket ARTD-181521 Proposed solution optional: In 4 file resource below: 1. Mem_InFls_s32k364_lqfp176.txt 2. Mem_InFls_s32k364_mapbga289.txt 3. Mem_InFls_s32k366_lqfp176.txt 4. Mem_InFls_s32k366_mapbga289.txt should be change Mem.InFls.Header : S32K39 > S32K36
ARTD-181924	New Feature	[MESSAGING] Combined usage of HL and IPL interfaces on S32CT NewWorkDescription: It shall be allowed, in a non-Autosar context, to combine usage of both a high level interface and a low level interface, even mapping on same peripheral, but different instances. This extends to both interfaces' source code and configuration support.

ID	Subtype	Headline and Description
		Presentation (Section 13. "Fulfilling MR-200") [https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=kfY9TG] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update configuration and source code follow Section 13. "Fulfilling MR-200"
ARTD-182175	Bug	[ETH] Failure at build when using autosar OS Detailed description (how to reproduce it): Driver build fail when using autosar os with trusted function !image-2025-04-28-16-21-08-546.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Int_TC_COT_001.c Observed behavior: Some include file have to workaround follow this file: !image-2025-04-28-16-22-23-388.png! Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-182259	Bug	[Sent] Build fail DMA Test Detailed description (how to reproduce it): Due to the MCL code update to support MR200, the naming of DMA channels has changed. However, in the Sent driver, we obtain the channel name using the Logic Channel Name, causing DMA tests to fail during the build. https://teams.microsoft.com/l/message/19:3d87b50dc4124e8e9f59f3293c2c179b@thread.tacv2/1745807420678?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1745485407409&teamName=Zebra&channelName=00.%20S32K3XX_S32M27x_6.0.0&createdTime=1745807420678 !screenshot-1.png|thumbnail! Preconditions: Use DMA mode Test Case ID (internal TC that caught the defect) optional: Ip_Sent_Flexio_TS_016 Ip_Sent_Flexio_TS_017 Ip_Sent_Flexio_TS_020 Sent_TS_017 Sent_TS_019 Sent_TS_021 Sent_TS_022 Observed behavior: build fail !image-2025-04-29-10-24-08-313.png|thumbnail! !image-2025-04-29-10-25-01-562.png|thumbnail! Expected behavior: build success Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-182262	Bug	[GPT][S32K3XX-M27X] Gpt multipartition not support for K389 Detailed description (how to reproduce it): Now Gpt multipartition not support for new derivative S32K389 !image-2025-04-29-10-24-04-436.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Gpt_TS_300

ID	Subtype	Headline and Description
		Observed behavior: Not support multi partion for K389 Expected behavior: Add support multi partition for K389 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-182270	Bug	[ICU] Remove some eMios channel in S32K36 derivatives Detailed description (how to reproduce it): eMIOS channels 0-7 are not available in S32K36x, so need to remove in resource file. K39X support 2 CMP instance, but have 3 option in HwInterrupt Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: remove eMIOS channels 0-7 in resource file for S32K36 derivative
ARTD-182342	Bug	[Base]: Update EA for Software Semaphores Detailed description (how to reproduce it): As described in the attached picture, the Exclusive Instructions that are used on some S32K3 derivatives for semaphore functionality do not work as expected. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: None Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Guard software semaphore implementation with LDREX and STRX with Exclusive Instructions that disable interrupts.
ARTD-182345	Bug	[RTE]: Add exclusive area for Base Detailed description (how to reproduce it): Add 2 exclusive area for software sema4 in Base Preconditions: NA Test Case ID (internal TC that caught the defect) optional: None Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-182351	Bug	[ICU][SIUL2_ICU] Driver not raise error when sellect channel not config hwinterrupt Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		When config SIUL2 in S32K396, hwchannel 3 is used, however channel 4 is not registered in hw interrupt > Driver not raiise error !image-2025-04-29-16-36-23-622.png! !image-2025-04-29-16-36-39-268.png! Test Case ID (internal TC that caught the defect) optional: Ip_Siul2_TS_COT_EQ_001 Expected behavior: Driver raise error when using hw channel without registered in hw interrupt Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-182374	New Feature	S32K3 High Current in Sleep mode customer failures caused by the default RTD port driver for non used pins - Update Manuals NewWorkDescription: [Update manuals related to [ARTD-180027] S32K3 High Current in Sleep mode customer failures caused by the default RTD port driver for non used pins. NXP JIRA] Requirement source: [None] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [Update manuals related to [ARTD-180027] S32K3 High Current in Sleep mode customer failures caused by the default RTD port driver for non used pins. NXP JIRA]
ARTD-182512	Bug	[mem_infls] [S32K3_S32M27x_6.0.0] Mem.InFls.Region2.Addr is not exist for S32K394, S32K374, S32K364 Detailed description (how to reproduce it): The XPath-expression "ecu:get('Mem.InFls.Region2.Addr')" caused an error: (35010) The requested ECU resource property "Mem.InFls.Region2.Addr" does not exist Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_InFls_TC_FCT_0001 Observed behavior: !image-2025-05-05-11-04-40-874.png! Expected behavior: Undfine C40_IP_REGION_2_ADDR/C40_IP_REGION_3_ADDR for S32K394, S32K374, S32K364 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-182558	Bug	[mem_infls] [S32K3_S32M27x_6.0.0] identifier "C40_Ip_VirtualSectorsType" is undefined Detailed description (how to reproduce it): When creating new test suite to cover requirement CPR_RTD_00679 to verify trusted API function in the driver with autosar OS Tester need to include below files in..\dev\test\test_int\specific\S32K3XX\include\Trusted_Include\Os_TrustedFunctions.h see ticket [ARTD-180703|https://jira.sw.nxp.com/browse/ARTD-180703] for more details C40_Ip_Types.h C40_Ip_Cfg.h Generate, build the test and the issue is identifier "C40_Ip_VirtualSectorsType" is undefined and mismatch version among header files !buildfail2.png|thumbnail! !build_fail.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: test case Mem_InFls_TC_COT_0012 of test suite Mem_InFls_TS_COT_012 Observed behavior: This issue (mismatch version among header files make the tydef C40_Ip_VirtualSectorsType is not regconized I try to workaround by remove 2 header files: !workaround.png|thumbnail! but issue still remain because line 120 and line 110 below were using function included in these 2 header files: !workaround2.png|thumbnail! Expected behavior: build successfully Proposed solution optional: I recommend:

ID	Subtype	Headline and Description
		add typedef uint32 C40_Ip_VirtualSectorsType; in C40_Ip_Types.h and remove typedef uint32 C40_Ip_VirtualSectorsType; in C40_Ip_Cfg.h to avoid fail when build test !solution.png|thumbnail!
ARTD-182747	Bug	[PWM] Build fail because Base update header file for S32K36X Detailed description (how to reproduce it): Test build failed because Base module updated header file for S32K36x (before S32K36x using header file of S32K39). !image-2025-05-06-09-54-38-987.png|width=796,height=512! !image-2025-05-06-09-55-00-894.png|width=571,height=307! Due to PR : [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/pull-requests/2404/overview] Driver Base update header file for K36X Preconditions: Run test with K36X Test Case ID (internal TC that caught the defect) optional: Pwm_TS_COT_001 Observed behavior Test build fail Expected behavior: Update include file for S32K36X using header file that defined for S32K36x Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-182806	Bug	[S32K3xx_S32M27x_6.0.0][MemAcc] Job end notification function which is not called after MemAcc cancel job completion Detailed description (how to reproduce it): Perform Fee_Write > Fee_Mainfunction > Fee_Cancel > MemAcc_Mainfunction > Fee Write After doing MemAcc_Mainfunction after Fee_Cancel, Fee_eJobResult still is MEMIF_JOB_PENDING. So can't call new job. !image-2025-05-06-10-13-00-882.png|width=842,height=371! !image-2025-05-06-10-11-57-438.png|width=836,height=309! Preconditions: Test Case ID (internal TC that caught the defect) optional: Fee_TC_402 Observed behavior: Fee Job end notification function which is not called after MemAcc cancel job completion Expected behavior: Fee Job end notification function which is called after MemAcc cancel job completion Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update driver code, MemAcc_JobEndNotify will be called after MemAcc cancel job completion
ARTD-182817	Bug	[Mem_InFls] Bswmd file should not have MemMainFunctionPeriod configurable Detailed description (how to reproduce it): Mem_43_EXFLS_TimingEvent_MainFunction field in the Bswmd is not generated correctly. Preconditions: Customer wants to use the Bswmd for MainFunction scheduling. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Issue with the bswmds Expected behavior: No issue Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Investigate and update the Bswmd to use "<PERIOD>0</PERIOD>" for the Mem_43_EXFLS_TimingEvent_MainFunction Investigate if the names of the fields are corect
ARTD-182820	Bug	[Mem_Eep] Bswmd file should not have MemMainFunctionPeriod configurable

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Mem_43_EXFLS_TimingEvent_MainFunction field in the Bswmd is not generated correctly. Preconditions: Customer wants to use the Bswmd for MainFunction scheduling. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Issue with the bswmds Expected behavior: No issue Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Investigate and update the Bswmd to use "<PERIOD>0</PERIOD>" for the Mem_43_EXFLS_TimingEvent_MainFunction Investigate if the names of the fields are corect
ARTD-182845	Bug	[GDU] Gdu_Init function have issue related DET error Detailed description (how to reproduce it): Gdu_Init function have issue related DET error Case 1: with GDU_PRECOMPILE_SUPPORT = ON When parameter Configuration <> NULL, driver not raise error Case 2: with GDU_PRECOMPILE_SUPPORT = OFF When parameter Configuration = NULL, driver raise error GDU_DET_ERROR_PARAMETER But follow requirement CPR_RTD_00563.gdu driver should raise error GDU_E_INIT_FAILED Test Case ID (internal TC that caught the defect) optional: Gdu_TC_0000.c Expected behavior: Gdu_Init function will raise error follow requirement CPR_RTD_00563.gdu Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-182888	New Feature	[base] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182891	New Feature	[can] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source:

ID	Subtype	Headline and Description
		According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182894	New Feature	[crc] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182897	New Feature	[dio] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182915	New Feature	[icu] [RTD]Adding K356 (6MB phantom of K358) support

ID	Subtype	Headline and Description
		Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182924	New Feature	[mcl] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182930	New Feature	[ocu] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*}

ID	Subtype	Headline and Description
		s32k356_{*}mapbga289{*}
ARTD-182933	New Feature	[platform] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182936	New Feature	[port] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182939	New Feature	[pwm] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}:

ID	Subtype	Headline and Description
		Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182942	New Feature	[rm] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182969	New Feature	[mem_infls] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182972	New Feature	[mem_exfls] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part.

ID	Subtype	Headline and Description
		No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182978	New Feature	[mem_eep] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-182990	New Feature	[build_env] [RTD]Adding K356 (6MB phantom of K358) support Description: Adding K356 ((6MB phantom of K358) support Requirement source: According to Change Request: [https://jira.sw.nxp.com/browse/AUTOSW-2300] Add S32K356 (6MB phantom of K358). {*}Note{*}: Assuming* the only change in the hardware is the memory size and no other parts are affected (clocks, pins, etc.) Assuming* no additional functional testing is required, since the hardware is identical (except for memory size) with the other derivative, from a testing point of view, only the multi-config tests that verifies the possibility of correctly configuring a project with the new part needs to be updated to include also this part. No examples are planned for this derivative and the effort doesn't include any kind of release activities, since it assumes it is included in an already planned release {*}Proposed solution{*}: Each driver makes a copy of the resource file of a similar derivative and only updates properties which are memory size relevant and update the resource file naming accordingly to the new K356 phantom: s32k356_{*}hdqfp172{*} s32k356_{*}mapbga289{*}
ARTD-183047	Bug	[ETH][S32K3XX]: Cannot get path for node EthFramePreemptionRxResidueQueue with IP layer Detailed description (how to reproduce it): 1. Cannot get path for node EthFramePreemptionRxResidueQueue with IP layer. This node in HLD layer can get the path. !image-2025-05-07-07-57-45-029.png|thumbnail! And The value of EthPtpTimeCounterMaxAdjustPercentage is out of sync between EB and CT. !screenshot-1.png|thumbnail! !screenshot-2.png|thumbnail! 2. The min value of EthPtpTimeCounterMaxAdjustPercentage is different beetwen EB and CT template

ID	Subtype	Headline and Description
		!image-2025-05-12-15-43-38-009.png! !image-2025-05-12-15-43-58-385.png! Preconditions: EthEnableFramePreemption is true Test Case ID (internal TC that caught the defect) optional: IP_GMAC_TS_ECVD_001 Observed behavior: Cannot get path for node EthFramePreemptionRxResidueQueue with IP layer. This node in HLD layer can get the path. Expected behavior: Can get path for node EthFramePreemptionRxResidueQueue with IP layer. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-183077	Bug	[S32K3xx_S32M27x_6.0.0][MEM_EXFLS]: Generate code with wrong include file on Qspi_Ip_Features.h Detailed description (how to reproduce it): When generate code for K36X derivative the file Qspi_Ip_Features.h include S32K9.h instead of S32K6.h !image-2025-05-07-11-51-53-603.png! Preconditions: Generate code for K36X Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Driver builds failed. !image-2025-05-07-11-52-51-654.png! Expected behavior: Driver buildable. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-183172	Bug	[S32K3xx_S32M27x_6.0.0][SPI]: An error has occurred on S32CT after deleting FLEXIO_SPI in SpiPhyUnit Detailed description (how to reproduce it): After deleting "FLEXIO_SPI" in SpiPhyUnit node, it causes an error that cannot continue configure Spi on S32CT. !image-2025-05-07-16-40-45-971.png! !image-2025-05-07-16-40-58-585.png! !image-2025-05-07-16-41-12-176.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Spi_TC_COT_0001 (Spi_TS_Cot_002) Observed behavior: Can not configure Spi on S32CT after deleting Expected behavior: All tests must be Spi configured on S32CT. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-183175	Bug	[S32K3XX]MCU: Update Ram section for K36x Detailed description (how to reproduce it): in S32K39_S32K37_and_S32K36_RM_Rev4.pdf S32K36x dóe not support section CM7_1 ITCM,DTCM,...detail in the S32K39x_memorymap !S32K39x_memorymap.png|thumbnail! need to update on resource and description on EBT !resource S32K36x.png|thumbnail! Preconditions: PVT_MCU_S32N_1.8.0_CD03_003 Test Case ID (internal TC that caught the defect) optional: NA

ID	Subtype	Headline and Description
		Observed behavior: ram section for K36x is not correct with Rm Expected behavior: ram section for K36x is correct with Rm Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-183245	Bug	[MEM_EEP] [S32K3XX] Some generated code is not present on S32DS Detailed description (how to reproduce it): Lack of code generation in S32DS !image-2025-05-08-10-08-08-945.png|width=546,height=308! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Mem_TC_FCT_0002 Mem_TC_FCT_0010 Observed behavior: Lack of code when generate code with config os_custom and os_system in S32DS Expected behavior: Not lack of code when generate code with config os_custom and os_system in S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ARTD-183265	Bug	[S32K3xx_S32M27x_6.0.0][CRC] Implement requirement CPR_RTD_00420.crc for some non_autosar APIs
		
		Detailed description (how to reproduce it):
		Missing implementation requirement CPR_RTD_00420.crc for some non_autosar APIs !image-2025-05-08-11-59-18-837.png|width=473,height=73!
		
		Preconditions:
		[SW Auto RTD R2x-11|https://elm.nxp.com/rm/web#]
		void Crc_SetChannelConfig(const uint32 Channel, const Crc_ChannelConfigType pxChannelConfig);
		uint64 Crc_SetChannelCalculate(const uint32 Channel, const uint8 pCrcData, const uint32 CrcLength, const uint64 CrcStartValue, const boolean IsFirstCall);
		uint64 Crc_GetChannelResult(const uint32 Channel);
		
		Test Case ID (internal TC that caught the defect) optional:
		NA
		
		Observed behavior:
		Missing implementation
		
		Expected behavior:
		implemented missing part
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		check upon each API call if the requested resource is configured to be available on the current partition, and in case of error will return CRC_E_PARAM_CONFIG

ARTD-183352	Bug	[I2S] Generate fail when using separate Tx/Rx without utilizing Rx/Tx DMA channels Detailed description (how to reproduce it): Generate fail when using separate Tx/Rx without enable Rx/Tx DMA channels. Issue 1: When using only TX and DMA mode without enable FlexioI2sDmaRxChannel node. When using only RX and DMA mode without enable FlexioI2sDmaTxChannel node. Issue 2: EBT can generate separate Tx/Rx configurations without enabling Rx/Tx DMA channels, and it does so without any error or warning logs Preconditions: Using I2s over Flexio Using only Tx/RX and Disable Rx/Tx Channel

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: I2s_TS_204 I2s_TS_205 I2s_TS_206 I2s_TS_207 Observed behavior: using only TX and DMA mode without enable FlexioI2sDmaRxChannel node. !image-2025-05-08-16-56-52-394.png! using only RX and DMA mode without enable FlexioI2sDmaTxChannel node. !image-2025-05-08-16-54-52-778.png! Expected behavior: Issue 1: Test can build successfully Issue 2: I think we have to add an error log or warning log Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-183593	Bug	[UART] The section of memory where the state stucture of Flexio is stored can be empty Detailed description (how to reproduce it): [Update 14Nov2024: to item 2). See attached all Port Config Files The values IDM_HW_VARIANT_LOW or IDM_HW_VARIANT_HIGH refer to different packages of the K3 SOC (sub-derivatives). High variant uses the derivative s32k322_hdqfp172 Mid and Low variants use the derivative s32k322_hdqfp100 Update 8Nov2024: to item 4) subitem 3). customer confirms raised the point is not valid > Swt_Ip_apCallbackPtr is properly wrapped with WDG_START/STOP_SEC_VAR_CLEARED_UNSPECIFIED. to item 4): Variable: Emios_Ip_paxBase is used in both: Emois_Mcl_Ip.c and Emois_Mcl_Ip_Irq.c in ..eclipse\plugins \Mcl_TS_T40D34M20I0R0\src. Apparently the following extern declaration: !image-2024-11-08-18-48-46-553.png! Should be wrapped with the same allocation keywords as in case of the definition: !image-2024-11-08-18-49-05-108.png! So MCL_START/STOP_SEC_VAR_INIT_UNSPECIFIED_NO_CACHEABLE. Wrongly handled memory mapping 1) Static variables in function scope Overall Sw requirement of the customer: !image-2024-09-03-07-59-57-045.png! RTD use cases as such encountered: Static variables in function in MCAL Gpt driver source code Gpt_GetTimeElapsed::returnHwChannelInfo Gpt_StopTimer::returnHwChannelInfo Static variables in function in MCAL Mcu driver source code Clock_Ip_SetCmuFcFceRefCntLfrefHfref::Hash Clock_Ip_CgmXPcfsSdurDivcDiveDivs::Hash Clock_Ip_CallEmptyCallbacks::FunctionWasCalled Clock_Ip_ClockInitializeObjects::Clock_Ip_bObjectsAreInitialized Power_Ip_MC_RGM_ResetDuringStandby::StandbyResetStatus Crypto: Crypto_Hse_PushJobsFromQueuesToHse::u32ObjectCounter 2) Variables that are not wrapped with allocation keywords

ID	Subtype	Headline and Description
		RTD use cases as such encountered: Port: gu8_port_NumberOfConfiguredPins in Port_Cfg.c 3) Variables not properly wrapped with allocation keywords RTD use cases as such encountered: # GPT_START_SEC_CONFIG_DATA_UNSPECIFIED wraps variable and not a const in generated GPT file: Gpt_lpw_PBcfg.c # Wkpu_lp_NMIConfig_PB (Icu) is wrapped by CONST allocation keyword: !image-2024-09-03-08-06-10-544.png! 4)* *Mixing variables of different init characteristics under same keyword The problem is that CLEARED init policy is used for DATA that is zero initialized explicitly in code and at the same the same init policy is used for DATA that is not initialized explicitly in code and so producing a linker error that C-objects of different init characteristics are part of the same data block: !image-2024-09-03-08-07-12-657.png! There is another similar case: PORT_START_SEC_VAR_CLEARED_UNSPECIFIED_NO_CACHEABLE Variable Swt_lp_apCallbackPtr shall be wrapped by NOINIT allocation keyword: !image-2024-09-03-08-07-47-396.png! variable Emios_lp_paxBase shall be wrapped by NOINIT allocation keyword 5) Mixing allocation keywords for the same variable Slightly different allocation keywords are used for same variables.: Wdg_au32InstanceCoreUsed wrapped by WDG_START_SEC_CONFIG_DATA_32 in .h files and by WDG_START_SEC_CONFIG_DATA_UNSPECIFIED in .c files Wdg_au16CfgInitialTimeout and other variables wrapped by WDG_START_SEC_CONFIG_DATA_16 in .h files and by WDG_START_SEC_CONFIG_DATA_UNSPECIFIED in .c files] Preconditions: [NTR] Test Case ID (internal TC that caught the defect) optional: [NTR] Observed behavior: [see above] Expected behavior: [1) static variables must be moved to file static scope 2) /3/ variables to be properly wrapped with allocation keywords 4) do not mix variables of different init characteristics under same keyword 5) Do not mix allocation keywords for the same variable Question: Is that fixed in RTD version 4.0 P24 which is planned for Series production?] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [see above]
ARTD-183630	Bug	[S32K3xx_S32M27x_6.0.0][PORT] Build fail on ghs, iar compiler Detailed description (how to reproduce it): Use port and no configuration for input glitch filter (S32K396) Build test on iar, ghs compiler Preconditions: no configuration for input glitch filter* Test Case ID (internal TC that caught the defect) optional: Port_TS_006 Observed behavior: build fail on ghs, iar compiler. !image-2025-05-12-09-44-27-719.png! Expected behavior: no error when building test Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-183624	Bug	[S32K3xx_S32M27x_6.0.0][MEM_INFLS]: Update C40_Ip_Instance for global C40_IP function Detailed description (how to reproduce it): C40_Ip_pFlashBaseAddress[C40_Ip_Instance] in some global C40_Ip functions is not update Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_1001 Observed behavior: Example: C40_Ip_ArrayIntegrityCheck, C40_Ip_CheckUserTestStatus, ... Expected behavior: Update like this: !image-2025-05-12-09-15-57-293.png! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-183696	Bug	[S32K3XX][Sema42] Sema4 may work incorrectly in case multi-core multi-elf Sema4 may work incorrectly in case multi-core multi-elf because sema4 is using logical channels, and the variable Rm_Ipw_pSema42LogicChannelConfig that stores the hw mapping information may be not accessed from all cores. !image-2025-05-12-13-53-42-063.png!
ARTD-183710	Bug	[mem_infls]C40_IP_USER_TEST_WAIT macro need to be generated by EB,CT Detailed description (how to reproduce it): C40_IP_USER_TEST_WAIT macro need to be generated by EB,CT, currently it set as Defaut in driver Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Fee_TC_001 Observed behavior: C40_IP_USER_TEST_WAIT was set defaut in driver Expected behavior: C40_IP_USER_TEST_WAIT macro need to be generated by EB,CT tool Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-183725	Bug	[mem_infls] [S32K3_S32M27x_6.0.0] PFLASH0_PFCR4_DERR_SUP_MASK undeclared for S32M27x Detailed description (how to reproduce it): When creating new test suite to cover requirement CPR_RTD_00679 to verify trusted API function in the driver with autosar OS Tester need to include below files in..\dev\test\test_int\specific\S32K3XX\include\Trusted_Include\Os_TrustedFunctions.h see ticket [ARTD-180703|https://jira.sw.nxp.com/browse/ARTD-180703] for more details C40_Ip_Types.h C40_Ip_Cfg.h Generate, build the test and the issue error: 'PFLASH_PFCR4_DERR_SUP_MASK' undeclared (first use in this function); !undeclare macro.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: test case Mem_InFls_TC_COT_0012 of test suite Mem_InFls_TS_COT_012 Observed behavior: Currently, in RM for M276 doesn't have DERR_SUP register like K3 and build step is failed !RMM276.png|thumbnail! !RMK3.png|thumbnail! Expected behavior: Build succesfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-183955	Bug	[Sent] Driver make error when config another module use FLEXIO hw Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Sent driver updated for MR-200 prevent configuration of the same hardware instance between HL configuration and standalone IP configuration. But now it makes error when add configuration for another module that use FLEXIO hw too(spi, uart,..) !image-2025-05-13-14-10-12-396.png|thumbnail! example config Int_TS_003 1.mex see attach file Preconditions: Add configuration for module use FLEXIO hw sent, spi or uart at the same time Test Case ID (internal TC that caught the defect) optional: Int_TS_301 Observed behavior: Generate error Expected behavior: No error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-184014	Bug	[GPT][MemMap]: Some variables' definition conflict with the section attribute in memmap Detailed description (how to reproduce it): Some variables' definition conflict with the section attribute in memmap. For example,: In the Gpt module. The variable: {*}Stm_Ip_u32TargetValue{*}{*}[]/{*}{*}Stm_Ip_u32NextTargetValue[]{*} which with a default initial value when definition. but it was located in the .mcal_bss_no_cacheable section. This will case compiling error （test with IAR） or unexpected binary file content. !image-2025-05-13-16-16-40-679.png|width=1051,height=284! Preconditions: Always Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiling error or unexpected contents in binary file. Expected behavior: Source code should be following the coding rule more strictly. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Had a code review carefully for all the module code by each module owner.
ARTD-184025	Bug	[mcu] [Safety Assessment] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Following the RTD MISRA deviation for MISRA Rule 2.5, justification by a comment is allowed only in the following case: If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a source file*{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Misra report Observed behavior: NA Expected behavior: MISRA rule 2.5 either correctly comment or to be fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-184109	Bug	[i2s] [Safety Assessment] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Following the RTD MISRA deviation for MISRA Rule 2.5, justification by a comment is allowed only in the following case:

ID	Subtype	Headline and Description
		If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a source file*{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Misra report Observed behavior: NA Expected behavior: MISRA rule 2.5 either correctly comment or to be fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-184112	Bug	[sent] [Safety Assessment] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Following the RTD MISRA deviation for MISRA Rule 2.5, justification by a comment is allowed only in the following case: If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a source file*{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Misra report Observed behavior: NA Expected behavior: MISRA rule 2.5 either correctly comment or to be fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-184203	Bug	[wdg] [Safety Assessment][S32K3][SAF85xx] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Following the RTD MISRA deviation for MISRA Rule 2.5, justification by a comment is allowed only in the following case: If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a source file*{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Misra report Observed behavior: NA Expected behavior: MISRA rule 2.5 either correctly comment or to be fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-184302	Bug	[Gmac]wrong calculation for PPSWidth field on the PPS feature Detailed description (how to reproduce it): wrong calculation for PPSWidth field on the PPS feature:

ID	Subtype	Headline and Description
		EthCtrlPulsePerSecondDutyCycle is config to 10% on EB but when running it is showing 20% so it different between config and report !image-2025-05-14-17-31-48-699.png! => Root cause: wrong calculation for PPSWidth field in the Gmac.ip.c file_ !image-2025-05-14-17-35-16-481.png|width=843,height=318!{*}{*} Test Case ID (internal TC that caught the defect) optional: Eth_TS_008 Observed behavior: wrong calculation for PPSWidth field Expected behavior: correct calculation for PPSWidth field Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Example: !image-2025-05-14-17-37-43-373.png|width=514,height=230! !image-2025-05-14-17-40-25-135.png|width=465,height=176!
ARTD-184481	Bug	[UART]: The generated code is different between EB and CT Detailed description (how to reproduce it): enable Rx DMA channel for MSC instance on S32K396, without enable Tx DMA channel Preconditions: driver tag: PVT_UART_S32K3XX_S32M27X_RTM_6.0.0_V08 test tag: PVT_TEST_UART_S32K3XX_M27X_600_030 Test Case ID (internal TC that caught the defect) optional: Uart_TS_0018 Observed behavior: gen pass trên EB but gen fail on CT EB: !image-2025-05-15-11-06-12-557.png|width=963,height=152! CT: !image-2025-05-15-11-06-06-418.png! Expected behavior: gen pass on both EB and CT Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-184514	Bug	[adc] [Safety Assessment] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Following the RTD MISRA deviation for MISRA Rule 2.5, justification by a comment is allowed only in the following case: If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a source file*{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Misra report Observed behavior: NA Expected behavior: MISRA rule 2.5 either correctly comment or to be fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-184546	Bug	[PWM][ETPU][S32K3XX-M27X-600] Initialization sequence of Etpu_Pwm incorrect

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): An issue reported by Etpu team regarding to the initialization sequence of Etpu_Pwm: !image-2025-05-15-17-16-58-152.png|width=568,height=213! It is currently incorrect, the eTPU channel cannot be enabled (set a non-zero priority) before it is fully initialized. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Initialization sequence not correct. Expected behavior: Initialization sequence is correct. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-185813	Bug	[S32K3xx_S32M27x_6.0.0][MEM_EXFLS]: Differences between code generated by eb and ct Detailed description (how to reproduce it): there are some differences between code generated by tresos and s32ds as below !image-2025-05-19-08-34-27-200.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_000 Observed behavior: as description Expected behavior: no differences between 2 configurators Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-185836	Bug	[S32K3xx_S32M27x][MEM_INFLS]: Calculate wrong value for LockDomainIDValue Detailed description (how to reproduce it): calculate wrong value for LockDomainIDValue in C40_Ip_CheckLockDomainID_CheckRegister function cause hardfault when read LockDomainIDValue Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_0001 in Ip_C40_TS_001 Observed behavior: !image-2025-05-19-10-29-06-747.png! Expected behavior: update algorithm Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-185880	Bug	[[S32K3xx_S32M27x_6.0.0][MEM_EXFLS]: Add S32K388 derivative into example list Detailed description (how to reproduce it): S32K388 example is not available into example list Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: S32K388 example is not available into example list Expected behavior:

ID	Subtype	Headline and Description
		S32K388 example is available into example list Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add S32K388 derivative in example list
ARTD-186124	Bug	Copyright deviations need to be updated Detailed description (how to reproduce it): Few of the existing RTD Source Files having copyright text which is not in line with the actual convention. Which leads the copyright violations which needs to be fixed. The detailed file list is available in the attached document. Preconditions: Copyright Issues in RTD Files needs to be corrected. Test Case ID (internal TC that caught the defect) optional: Local Copyright Script Run (Example: Precommit Builds) Observed behavior: Copyright Violations. Expected behavior: No Copyright Violations Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-186620	Bug	[OCU]: Unused macros causing misra violations Detailed description (how to reproduce it): We found some wrongly commented misra 2.5 rule. They are actually not used in the driver code. Here are the following misra violations 16267931|MISRA C-2012 Rule 2.5|1164|Advisory|Low| Quality|Macro "EMIOS_OCU_IP_HWACCESS_MODULE_ID" is defined but never used.|/AU-RTDCIOC304-7/sources/cf52b14924/output/eclipse/plugins/Ocu_TS_T40D34M60I0R0/include/Emios_Ocu_Ip_HwAccess.h 10942666|MISRA C-2012 Rule 2.5|1164|Advisory|Low| Quality|Macro "OCU_USER_MODE_SOFT_LOCKING" is defined but never used.|/AU-RTDCIOC304-7/sources/cf52b14924/output/eclipse/plugins/Ocu_TS_T40D34M60I0R0/include/Ocu_EnvCfg.h 11464669|MISRA C-2012 Rule 2.5|1164|Advisory|Low| Quality|Macro "OCU_EMIOS_ODIS_MASK" is defined but never used.|/AU-RTDCIOC304-7/sources/cf52b14924/output/eclipse/plugins/Ocu_TS_T40D34M60I0R0/include/Emios_Ocu_Ip_Types.h 10942511|MISRA C-2012 Rule 2.5|1164|Advisory|Low| Quality|Macro "EMIOS_FREEZE_ENABLE" is defined but never used.|/AU-RTDCIOC304-7/sources/cf52b14924/output/eclipse/plugins/Ocu_TS_T40D34M60I0R0/include/Emios_Ocu_Ip_Types.h Preconditions: Misra check to be ran Test Case ID (internal TC that caught the defect) optional: Ocu_TS_001 Observed behavior: Wrongly commented misra violations Expected behavior: No misra violations caused by unused lines of code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-186689	Bug	[Dio][S32K3] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Misra report contains commented Rule 2.5 for unused define inside source file. 31925477|MISRA C-2012 Rule 2.5|1164|Advisory|Low| Quality|Macro "SIUL2_DIO_IP_NUM_OF_PIN_PORT_U16" is defined but never used.|/AU-RTDCID242-17/sources/cf52b14924/output/eclipse/plugins/Dio_TS_T40D34M60I0R0/src/Siul2_Dio_Ip.c|111|Intentional|Dismissed|The macro can be used in the application, but it is not used in the current test. SnapshotId:|204588 If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a {color:#de350b}source file{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions:

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-186695	Bug	[Port][S32K3] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Misra report contains commented Rule 2.5 for unused define inside source file. 1164|Advisory|Low| Quality|Macro "SIUL2_NUM_OF_PIN_PORT" is defined but never used.|/AU-RTDCIPO322-44/sources/cf52b14924/output/eclipse/plugins/Port_TS_T40D34M60I0R0/src/Siul2_Port_Ip.c|122|Intentional|Dismissed|The macro can be used in the application, but it is not used in the current test. SnapshotId:|204776 If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a {color:#de350b}source file{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-186837	Bug	[MCU][S32K3] - dereferencing NULL_PTR value within Clock_Ip_apxCmu structure Detailed description (how to reproduce it): Anytime when Clock_Ip_CMU_ClockFailInt) is called. Preconditions: CMU support enabled in the configuration Test Case ID (internal TC that caught the defect) optional: Observed behavior: When MPU is set to catch reads from a NULL_PTR, BusFault is triggered. Expected behavior: Don't read from NULL_PTR address. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add check for NULL_PTR before reading from Clock_Ip_apxCmu e.g. !image-2025-05-22-16-33-21-601.png!
ARTD-187027	Bug	[GPT][S32K3-M27X][S32DS] Generate fail when enable multi partition on S32DS Detailed description (how to reproduce it): Generate fail on S32DS with error: !image-2025-05-23-15-15-54-179.png! Preconditions: Enable multi partition for Gpt Test Case ID (internal TC that caught the defect) optional: Gpt_TS_001_cfg3 (with VV_COMPARE_CODE_GEN=ON and MultiPartition=ON) Observed behavior: gen fail Expected behavior: gen success without error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-187967	Bug	[ETH] : Example have generate failure Detailed description (how to reproduce it): gen fail on s32ds !image-2025-05-26-10-23-19-902.png|width=1819,height=973! !image-2025-05-26-10-23-59-235.png|width=1557,height=741! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Example have generate fails Expected behavior: generate pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-188019	Bug	[S32K3XX_S32M27X 6.0.0] BASE: Missing SFACR register in S32K358_QuadSPI header files Detailed description (how to reproduce it): According to S32K3xx_RM_Rev9.pdf, S32K358 have SFACR register but there is no information of that register in S32K358_QuadSPI header file. !image-2025-05-26-14-24-30-864.png|width=515,height=427! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_COT_003 Observed behavior: build failed Expected behavior: build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-188048	Bug	[S32DS] Build fail core M7_1_0/M7_2_0 build with RAM/FLASH : when creating new project for S32K322, S32K324, S32K338, S32K358 and S32K388 derivatives Detailed description (how to reproduce it): Step1: In S32DS choose File > New > S32DS Application project Step2: Fulfil project name and Choose Family from the *Test Data* column-> Next Step3: Select the required toolchain plugin from the toolchain tab x number of tools chains Step4: Type a project name(e.g NewProject). Step5: Select SDK version from *Test Data* column Step6: Select only core from *Test Data* column Step7: Click Finish Step8: Build project (Debug_RAM/Flash) Step9: Click on Update code Step10: Build project (Debug_RAM/Flash) Step11: Debug project, the program jumps to "main" function Preconditions: NA Test Case ID (internal TC that caught the defect) optional: INTEGRATION_TC_018 Observed behavior: Build fail core M7_1_0/M7_2_0 build with RAM/FLASH when creating new project for S32K322, S32K324, S32K328, S32K338, S32K358 and S32K388 derivatives on IAR/GHS/DIAB compiler With debug RAM : #include "Siul2_Port_Ip_Cfg.h" "C:\Users\nhungtt5\workspaceS32DS.3.6.1_S32K3\S32K388\S32K388_M7_1_0\RTD \include\Siul2_Port_Ip.h",46 Fatal error[Pe1696]: cannot open source file "Siul2_Port_Ip_Cfg.h" searched: "C:\Users \nhungtt5\workspaceS32DS.3.6.1_S32K3\S32K388\S32K388_M7_1_0\RTD\include\"

ID	Subtype	Headline and Description
		With debug Flash : !image-2025-05-26-19-21-17-555.png|width=951,height=144! Build fail core M7 build with RAM when creating new project for S32M274, S32M276 on GHS compiler !image-2025-05-26-19-27-55-638.png|width=921,height=165! Expected behavior: All projects generate and build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-188059	Bug	[UART]: Code generate is incorrect when config MSC channel for S32K396 on S32DS Detailed description (how to reproduce it): config MSC channel on S32DS: Preconditions: test tag: PVT_TEST_UART_S32K3XX_M27X_600_058 dev tag: PVT_UART_S32K3XX_S32M27X_RTM_6.0.0_Q03 !image-2025-05-26-16-37-10-512.png|width=651,height=295! Test Case ID (internal TC that caught the defect) optional: UART_TS_0018 Observed behavior: code generate is incorrect: !image-2025-05-26-16-39-48-540.png|width=1168,height=387! Expected behavior: code generate is correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-188071	Bug	[Rm] Missing SAF required dependency Detailed description (how to reproduce it): Compiling RTD 6.0.0 in K3 Platform Bundle led to following error: !image-2025-05-26-13-26-03-287.png|width=930,height=414! Ticket was created to SAF team, their analysis showed that RTD removed a macro that SAF was relying on see comments in [https://jira.sw.nxp.com/browse/ARTD-187835] Decision was to create this ticket for RTD to fix the missing macro Preconditions: Install RTD Test Case ID (internal TC that caught the defect) optional: Bundle_TC_001 Observed behavior: Errors at compile time Expected behavior: No errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-188365	Bug	[mem_infls] Indexing in PFCBLKa_LOCKMASTER_SSb is wrong Detailed description (how to reproduce it): Function C40_lp_GetLockDomainIDValue is impacted Preconditions: Test Case ID (internal TC that caught the defect) optional: 001

ID	Subtype	Headline and Description
		Observed behavior: hardfault observed on S32K324 Expected behavior: No hardfault. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-189161	Bug	[S32K3] All modules using EMIOS generates wrong configuration file Detailed description (how to reproduce it): Using RTD from the location [https://nl-nxrm.sw.nxp.com/#browse/browse:AMP_ProductEngineering:auto_tools_products%2FRTD%2FS32K3XX%2F4_7%2FBUILD_ENG%2FRTM_6_0_0%2F20250528-1802%2FSW32K3_S32M27x_RTD_R21-11_6.0.0_D250528_DesignStudio_updatesite.zip] The pwm module generates wrong configuration file when Ocu module is configured !image-2025-06-02-09-15-53-978.png! Check attached S32DS pproject Preconditions: Configure PWM and Ocu to use EMIOS periferal. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Failing to compile PWM configuration file. Expected behavior: Compile is succesfful Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: fix it and test with other modules(PWM, Icu, OCU, GPT) that use the same peripheral.
ARTD-191048	Bug	[adc] [Safety Assessment] The MISRA rule 2.5 needs to be fixed Detailed description (how to reproduce it): Following the RTD MISRA deviation for MISRA Rule 2.5, justification by a comment is allowed only in the following case: If the macro is located in an IP header file and is used on the application side, the rule violation can be justified with a comment. Otherwise, the macro should be removed. If the violation occurs in a source file*{color}, the issue must be resolved by either removing the redundant macro or moving it to a header file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Misra report Observed behavior: NA Expected behavior: MISRA rule 2.5 either correctly comment or to be fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: TBD
ARTD-173715	Bug	S32K3 RTD 5.0.0 integration with GM HSE FW clock patch. Hello team, There was an issue on ETAS side when using the RTD 5.0.0 with the GM HSE FW where during the initialization there will be no communication with the Shared Ram Interface. Apparently the issue got fixed by a specific patch and ETAS is requesting to see this fixed in the RTD if using only FIRC it will be working but changing to a configuration that uses the PLL is triggering issues, the mentioned fixed is the following: Tried Config0 (low performance) using only FIRC --> It works Tried Config1 (low performance) using only FIRC and (PLL Disabled) and (disable MCU control for all MUXs except MUX0) --> It works Tried Config2 (High performance) using PLL and (disable MCU control for all MUXs except MUX0) --> It doesn't work Apply Patch to static MCAL in Clock_Ip_Data.c by apply the below change:

ID	Subtype	Headline and Description
		The result of this patch that all Configurations are working fine. // #if defined(CLOCK_IP_CGM_X_DE_DIV_STAT_WITHOUT_PHASE_WAIT_FOR_HSE_CORE) // /* HSE_CLK clock / {CLOCK_IP_CGM_0_INSTANCE, CLOCK_IP_DIV_TRIGGER_CMU_HSE, CLOCK_IP_HSE_EXTENSION, 0U, CLOCK_IP_SEL_0_INDEX, CLOCK_IP_DIV_3_INDEX, 0U, 0U, CLOCK_IP_CMU_5_INSTANCE}, / HSE_CLK clock */ // #else /* HSE_CLK clock / {CLOCK_IP_CGM_0_INSTANCE, CLOCK_IP_DIV_TRIGGER_CMU, CLOCK_IP_HSE_EXTENSION, 0U, CLOCK_IP_SEL_0_INDEX, CLOCK_IP_DIV_3_INDEX, 0U, 0U, CLOCK_IP_CMU_5_INSTANCE}, / HSE_CLK clock */ //#endif Best Regards, Jesus Cinco

4.2 Change List for 5.0.0

ID	Subtype	Headline and Description
ARTD-15573	New Feature	[ADC] Hw triggering using BCTU should avoid redefinition of configuration parameters At this moment Adc tresos configuration interface contains two place holders for configuring the HW triggers: Adc/AdcConfigSet/AdcHwTrigger (used only for AUTOSAR HW Trigger mode) and Adc/AdcConfigSet/BctuHwUnit/BctuInternalTrigger (_used for CTU mode). For BCTU mode: BctuTriggerSource contains the same information as given by AdcHwTrigger container. Having the same information twice should be avoided since may be misleading and may create confusion. Optimal solution would be to change the BctuTriggerSource_ from enum to reference type and reference inside it Adc/AdcConfigSet/AdcHwTrigger_, this way the parameter is not deleted (avoiding epc issues) and the already defined AdcHwTrigger may be put to use. Another issue is caused by BctuInternalTrigger_/_BctuDataDestination parameter which has different naming format for the FIFO label (*BCTU_FIFOx*) than the FIFO index (*FIFO{color:#ff0000}_{color}x*) defined in Adc/AdcConfigSet/BctuHwUnit/BctuResultFifo. Since processing strings during code generation may be error prone, (especially since enum labels might be changed in the future) so the good solution would be to provide a reference type paramenter to the dc/AdcConfigSet/BctuHwUnit/BctuResultFifo if BctuDataDestination BCTU_FIFO*x and Adc.xdm should validate that the correct reference is used. Note. Is important to know that in AUTOSAR, Higher level components generally relay on configuration to get the information from lower level component. Use of references to channels, groups or other type of such container is always preferred to hard-coding since it allows reconfiguration to be done much more easier. In our case for any application which may use the BCTU configuration, the input will always be Adc/AdcConfigSet/BctuHwUnit/BctuInternalTrigger configuration which connects ADC channels to FIFO and provides a single entry point which can be referenced as container by the configuration of the application. However, is not practical for any application to use another referenced (i.e. to the FIFO configuration) since this information is/should be already provided by BctuInternalTrigger,
ARTD-23249	New Feature	[I2S] Update Flexio I2S IP SendDataBlocking functions to support only polling Cleanup/update Flexio I2S IP SendDataBlocking functions to support only polling according to decision from this thread [Razvan-Nicolae Tilimpea: Topic closed.Zebra Final decision : Sync > flag pollin… |https://teams.microsoft.com/l/message/19:ffb5bcb3ccf94d4cb64209a2b0fe242f@thread.tacv2/1588575882139?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1588064430502&teamName=Zebra&channelName=Group%200&createdTime=1588575882139] posted in Zebra / Group 0 at Monday, May 4, 2020 10:04:42 AM Please update accordingly also UM, requirements, UML, etc. if needed Can refer to implementation from UART/I2C as reference Pros and cons about decision can be found unfortunately only on this initial thread in Romanian, but decision still stands: [Razvan-Nicolae Tilimpea: Sync-MCAL VS Blocking-SDK |https://teams.microsoft.com/l/message/19:ffb5bcb3ccf94d4cb64209a2b0fe242f@thread.tacv2/1588064430502?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1588064430502&teamName=Zebra&channelName=Group%200&createdTime=1588064430502] posted in Zebra / Group 0 at Tuesday, April 28, 2020 12:00:30 PM
ARTD-29346	Bug	[Mcu] Validation error due to missing PreConfiguredConfiguration Detailed description (how to reproduce it): There is reported the following error while running the bswmd file validations in third party Autosar configuration tool: Constr_4045-In a BswImplementation <BswImplementation_0> the reference PreConfiguredConfigurations containing EcucModuleConfigurationValues <>, the reference implementConfigVariant is empty or NULL.[Infos]

ID	Subtype	Headline and Description
		<BswImplementation_0> : </Mcu_TS_T40D34M20I0R0/Implementations/BswImplementation_0>,<> : </TS_T40D34M20I0R0/McuPreConfiguration>,ERROR,S32K344_Integration_example,paramdef/bswmd_static/Mcu_Bswmd_original.arxml The error is reported because there is the following reference to preconfigured configuration: <PRECONFIGURED-CONFIGURATION-REF DEST="ECUC-MODULE-CONFIGURATION-VALUES">/TS_T40D34M20I0R0/McuPreConfiguration</PRECONFIGURED-CONFIGURATION-REF> But there is no preconfigured configuration available in Autosar format (only in Tresos proprietary format in Mcu_TS_T40D34M20I0R0\config_ext\McuPreConfiguration.xdm). Preconditions: Using third party configuration editor (not Tresos). Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Error reported during validation of bswmd file Expected behavior: No error reported during validation of bswmd file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the preconfigured configuration in Autosar format. For now we have resolved the issue by deleting the reference from Mcu bswmd file, i.e. removing this line from Mcu_Bswmd.arxml file: <PRECONFIGURED-CONFIGURATION-REF DEST="ECUC-MODULE-CONFIGURATION-VALUES">/TS_T40D34M20I0R0/McuPreConfiguration</PRECONFIGURED-CONFIGURATION-REF> So it looks as follows: !mcu_preconfigured_config_reference.png!
ARTD-58468	Bug	[ADC] The macro ADC_IPW_SDADC_IS_USED is not variant aware Detailed description (how to reproduce it): The macro *ADC_IPW_SDADC_IS_USED* is currently not variant aware, it will be over-written by the last variant when generating the project. Preconditions: Using test with VARIANT_NO > 1 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The ADC_IPW_SDADC_IS_USED* might be = OFF for all variants (if last variant in EB or first variant in CT = false) Expected behavior: The macro ADC_IPW_SDADC_IS_USED should have value STD_ON whenever SDADC hardware is used in the project Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-63527	Bug	[MemAcc] MemAcc_JobRetrying return not correct value when blankcheck operation determined a mismatch Detailed description (how to reproduce it): [SAF85_S32R41 1.0.0][MemAcc] MemAcc_JobRetrying return not correct value when the blankcheck operation determined a mismatch !image-2023-04-19-06-28-45-505.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: JobResult return MEMACC_MEM_FAILED Expected behavior: JobResult return MEMACC_MEM_INCONSISTENT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-75130	Bug	Incomplete Paths in "Debug RAM" configuration Detailed description (how to reproduce it): When I create a project using the RTDs for the S32K311 and I compile "Debug RAM" there are erros. These errors are not present if I compile "Debug FLASH".

ID	Subtype	Headline and Description
		Preconditions: Create a project in S32DS for the device S32K311 Test Case ID (internal TC that caught the defect) optional: Observed behavior: If I use "Debug RAM", there are a lot of erros Expected behavior: No errros Note:*_ Proposed solution optional: Complete the paths for "Debug_RAM" (See the attached pictures)
ARTD-81094	Bug	[MCU]: The Ram section can't support init the TCM area which the address start with 0 Detailed description (how to reproduce it): The Ram section can't support initial the TCM area which the address start with 0. !image-2023-08-03-17-04-49-815.png! Preconditions: The RAM address is start with 0. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Report error Expected behavior: Works well Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-81655	Bug	[I2s]FXIO I2S force to enable both Tx&Rx even when only Tx used Detailed description (how to reproduce it): [After adding an FlexIO I2S component in .mex file, trying to enable only Tx or Rx] Preconditions: [Configured FXIO_mcl for I2S pin.] Test Case ID (internal TC that caught the defect) optional: [N/A] Observed behavior: [Found configure error reported by .mex tool. Besides, if both Tx&Rx enabled, the callback function will be invoked by Rx even we only use Tx sendData but not invoke Rx receive API.] Expected behavior: [The FXIO I2S Tx / Rx can be independently enabled and use, the callback function will not be invoked twice if we didn't initiate both Tx&Rx process.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-85979	New Feature	Linker file doesn't support custom memory sections Linker file coming from RTD release does not support custom memory sections for NXP SW products. Workaround: Defined fixed paths and create a new linker file in Platform Bundle → did not use the linker file coming from platform. Folder structure: !https://confluence.sw.nxp.com/download/attachments/283895473/image-2023-7-18_8-28-5.png?version=1&modificationDate=1689658086056&api=v2|width=474,height=211! Sections added for NXP RTOS, IPCF, SCST, SAF. NXP RTOS Sections: ostext

ID	Subtype	Headline and Description
		acmcu_code_rom acmem_43_infls_code_rom osrodata osbss ossbss IPCF Sections: osstack OS_MAIN_STACK_MIN and OS_MAIN_STACK_MAX SCST Sections: m7_scst_rom_data m7_scst_test_shell_data m7_scst_test_shell_code m7_scst_test_code m7_scst_test_code m7_scst_test_branch_code0 m7_scst_test_branch_code1 m7_scst_ram_data m7_scst_ram_data_target0 m7_scst_ram_data_target1 m7_scst_ram_test_code m7_scst_vector_table SAF Sections: s32_saf_text s32_saf_const s32_saf_const_flash_0 s32_saf_const_flash_1 s32_saf_const_flash_2 s32_saf_const_flash_3 s32_saf_const_flash_4 s32_saf_const_flash_5 ramcode_no_cacheable s32_saf_data s32_saf_data_exec_8k_0 s32_saf_data_exec_8k_1 s32_saf_bss s32_saf_bss_persist_reset s32_saf_bss_full_access s32_saf_bss_sram_0 s32_saf_bss_sram_1 s32_saf_bss_sram_2 s32_saf_bss_sram_3 s32_saf_bss_no_cacheable s32_saf_shared_no_cacheable s32_saf_scheck_requests_no_cacheable s32_saf_scheck_faults_no_cacheable s32_saf_bss_tcm_0 s32_saf_bss_tcm_1 s32_saf_const_cfg
ARTD-83911	Bug	[MCU] Power_Ip, Power_Ip_ResetType The comments of Power_Ip_ResetType enum are incorrect !image-2023-08-23-15-41-38-652.png|thumbnail!
ARTD-85015	New Feature	Confusing SIUL2 instance for input pins Detailed description (how to reproduce it): [For the input pins, SIUL2 instance configuration seems incorrect and confusing for users. E.g. PAD_005 can be configured as CAN_0_RX in SIUL2_3 instance as per IOMUX. And its IMCR is indeed in SIUL2_3. !image-2023-09-05-16-58-38-204.png|width=537,height=134! But users have to select SIUL2_0 to select CAN_HUB_CAN_0_RX_IN otherwise there is no such pin mode. !image-2023-09-05-16-59-44-539.png|width=360,height=250! There may be RTD configuration logic behind this but it's confusing for users. Can you please correct the logic or add notes?] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		[N/A] Observed behavior: [No pin mode selection in the correct SIUL2 instance for input signals] Expected behavior: [Have pin mode selection in the correct SIUL2 instance for input signals] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [correct the logic or add notes]
ARTD-85526	Bug	[Pins tool] Check all the bitfields in MSCRs again, show as N/A for unavailable cases for S32K3, S32XX, S32K1XX Detailed description (how to reproduce it): [Pins tool] Check all the bitfields in MSCRs again, show as N/A for unavailable cases HLD: for these bit-fields, disable/readonly/inactive the corresponding nodes in HLD (EB+CT) Pins from PBY_00 in SIUL2_AE on S32E cannot enable APC in pins tool (n/a for now) Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Show as N/A for unavailable bitfields for each pin. Expected behavior: Check all the bitfields in MSCRs again, show as N/A for unavailable cases Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Pins from PBY_00 in SIUL2_AE on S32E cannot enable APC in pins tool (n/a for now) > The conclusion is to remove Analog Pad Control column from UI of Pins tool and generate .analogPadControl = PORT_ANALOG_PAD_CONTROL_ENABLED whenever ADC mode was chosen
ARTD-85812	Bug	[S32ZE 1.0.0][sent] Fix code review rule 45 from checklist To-Do: Starting from code review checklist, fix rule 45 !image-2023-09-12-14-33-45-909.png! Checklist with findings can be found in [Pull Request #194: [ARTD-80297] Initial commit with intermediate status of the review checklist NXP Bitbucket|https://bitbucket.sw.nxp.com/projects/ARTD/repos/sent/pull-requests/194/diff#specific/S32ZSE/doc/reports/Review_Checklist/RTD_SENT_Checklist_for_Code_Review_Intermediate.xls] Guideline: [RTD Coding Guideline|https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20Coding%20Guideline.docx] [RTD UML Design Guideline.pptx|https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20UML%20Design%20Guideline.pptx]
ARTD-90948	New Feature	[fls] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf , replace mqfp with hdqfp CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 And replace all occurences of mqfp with hdqfp* *(mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641)* Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies):

ID	Subtype	Headline and Description
		S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90950	New Feature	[eep] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf , replace mqfp with hdqfp CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 And replace all occurences of mqfp with hdqfp* *(mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641)* Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-91212	New Feature	[ADC] Support for thread order of DSPSS Clock threshold mode NewWorkDescription: Add configuration of thread order that should be used with clock threshold mode. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) N/A Proposed solution optional: N/A
ARTD-92750	Bug	[I2C] Analyzing and Re-structure the inclusion between layers according to Autosar Standard Detailed description (how to reproduce it): In current implementation in i2c driver, IPW.c file is calling CDD.h file to get some typedef struct on Types.h file. This doesn't follow to inclusion of RTD project. !MicrosoftTeams-image (1).png|thumbnail!. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: IPW layer include CDD layer Expected behavior: Should be CDD include IPW include IPV

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Analyze and re-struct all layers in repo
ARTD-93670	Bug	[MCU] Remove functions that cannot be called in S32K3XX Detailed description (how to reproduce it): In order to decrease the CE index to 0, below functions need to be removed because they can not be called in S32ZSE Power_Ip_RDC_SetUserAccessAllowed Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Above functions cannot be called Expected behavior: Remove such functions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-95686	Bug	[MCU] Coding convention violations Detailed description (how to reproduce it): 4 red marked lines are using tab characters instead of 4 space characters !image-2023-10-11-10-39-32-814.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: 4 red marked lines are using tab characters instead of 4 space characters Expected behavior: Correct 4 red marked lines Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-95698	Bug	[MCU] Missing function prototypes Detailed description (how to reproduce it): List of Missing function prototypes 1. Clock_Ip_PllPowerClockIp !image-2023-10-11-11-11-47-470.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing function prototypes Expected behavior: Add function prototypes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-112685	Bug	[memacc] The driver should not be hardware-dependent Detailed description (how to reproduce it): # The driver should not be hardware-dependent. It is the job of the Mem drivers to abstract the hardware details. Currently the MemAcc configuration contains the device name, which is taken from resources: !image-2024-05-23-11-25-46-655.png!

ID	Subtype	Headline and Description
		# Device name is imported from the Mem driver and used to ensure that two jobs for the same device are not done in parallel. But this is a non-standard configuration item, so it should not be imported, because the MemAcc should work with any Mem implementation. Instead, the Mem driver instance should be used. One Mem driver instance corresponds to a device and can only perform one job at a time. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: MemAcc configuration contains device name (e.g. XSPI) Expected behavior: The driver should not be hardware-dependent Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: the Mem driver instance should be used
ARTD-112683	Bug	[memacc] Fail status for pending job Detailed description (how to reproduce it): There is an inconsistency of the job status and job result (MemAcc_GetJobStatus, MemAcc_GetJobResult) when a Mem job fails and is retried. The result is updated in the Job info structure and from now on MemAcc_GetJobResult will return MEMACC_MEM_FAILED, even though MemAcc_GetJobStatus still returns MEMACC_JOB_PENDING. This can be confusing for the application, and not quite in line with the standard: Note: If a MemAcc job is still pending, the API returns the result of the last MemAcc job. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: MemAcc_GetJobResult will return MEMACC_MEM_FAILED, even though MemAcc_GetJobStatus still returns MEMACC_JOB_PENDING Expected behavior: MemAcc_GetJobResult should updated status only when job is complete Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-97444	Bug	[MCU] Missing restraints on the interface for system clock freq Detailed description (how to reproduce it): S32K34x has LMAUTOEN which mention that !image-2023-10-23-09-38-06-357.png! However, the CT and EB interface only raise 1 warning like below !image-2023-10-23-09-41-37-762.png! !image-2023-10-23-09-42-41-781.png! => Errors must be raised following RM's mention for each time LMEN=0 and SYS clock is not FIRC or higher Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing restraints on the interface for system clock freq Expected behavior: Add restraints on the interface for system clock freq Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97516	Bug	[MCU] Correct clock source for LPUART Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Clock source for LPUART in Clocks tool interface and Clock_Ip_Frequency.c is not correct. See sheet "Snapshot" in report in Crucible for more detail. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: LPUART clock source is incorrect Expected behavior: LPUART clock sources are correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97521	Bug	[MCU] SXOSC some bit fields are not supported Detailed description (how to reproduce it): SXOSC has some bit fields: ALC_D, CUR_PRG_SF, CUR_PRG_COMP and GM_SEL that are not implemented (driver and configuration) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Some SXOSC bits aren't supported Expected behavior: The SXOSC bits are supported Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97527	Bug	[MCU] CM7_0_TCM_CLKEN and CM7_1_TCM_CLKEN are no longer exist Detailed description (how to reproduce it): [MCU] CM7_0_TCM_CLKEN and CM7_TCM_CLKEN are no longer exist in RM but still available in driver and configurator Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: CM7_0_TCM and CM7_1_TCM are still available in some derivative's gate list Expected behavior: Those gate are removed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97539	Bug	[MCU] Some clock muxs for S32K388 are implemented incorrect Detailed description (how to reproduce it): Some clock muxs of S32K388 are not implemented correctly follow RM. See report in Crucible, sheet "K3xx(except K344 and subders)" index 9 and 11 for more detail. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Some clock muxs are not implemented correctly follow RM Expected behavior: Clock muxs are implemented follow RM

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97557	Bug	[MCU] Clock system diagram is not mapping to the driver Detailed description (how to reproduce it): S32K396 Mux 3 and mux 4 are using AIPS_SLOW_CLK on the diagram instead of AIPS_PLAT_CLK as the interface ! image-2023-10-23-16-52-21-498.png! Interface !image-2023-10-23-16-54-18-141.png! S32K358 Mux 7 is using GMAC_MII_RGMII_RX_CLK and GMAC_MII_RMII_RGMII_TX_CLK as sources but the interface lacks GMAC_MII_RMII_RGMII_TX_CLK Diagram: !image-2023-10-23-17-01-31-976.png! Interface: !image-2023-10-23-17-09-03-145.png! S32K388 Mux3 and mux4 on the interface have CORE_CLK as their sources which are not present on the diagram !image-2023-10-23-17-15-30-093.png! !image-2023-10-23-17-17-15-976.png! Mux 6 has the wrong names of GMAC0_MII {*}RGMII{*}{_}RX_CLK and GMAC0_MII_RMII{_}{*}RGMII{*}_TX_CLK on the interface (GMAC0_MII_RMII_TX_CLK and GMAC0_MII_RX_CLK => Wrong) !image-2023-10-23-17-37-32-968.png! Mux7 is using redundant sources PLL_PHI0_CLK and PLLAUX_PHI0_CLK and uses the wrong name of GMAC0_MII_RMII_{*}RGMII{*}_TX_CLK on the interface (GMAC0_MII_RMII_TX_CLK =>wrong) compared to the diagram !image-2023-10-23-17-47-48-605.png! !image-2023-10-23-17-49-57-408.png! Mux 8 is using redundant sources PLL_PHI0_CLK and uses the wrong name of GMAC0_MII_RMII_{*}RGMII{*}_TX_CLK on the interface (GMAC0_MII_RMII_TX_CLK =>wrong) compared to the diagram !image-2023-10-23-17-52-02-243.png! !image-2023-10-23-17-53-00-051.png! Mux 9 is using redundant sources PLL_PHI0_CLK and uses the wrong name of GMAC0_MII {*}RGMII{*}RX_CLK, _ _GMAC0_MII_RMII{*}RGMII{*}_TX_CLK, GMAC1_MII {*}RGMII{*}RX_CLK,_ _ GMAC1_MII_RMII{*}RGMII{*}_TX_CLK on the interface (GMAC0_MII_RMII_TX_CLK and GMAC0_MII_RX_CLK, GMAC1_RMII_EXT_CLK, GMAC1_MII_RX_CLK => Wrong) !image-2023-10-23-17-58-45-677.png! !image-2023-10-23-17-59-08-261.png! Mux11 is using redundant source PLL_PHI0_CLK !image-2023-10-23-18-01-20-126.png! !image-2023-10-23-18-02-22-280.png! Mux15 is using redundant sources (PLL_PHI0_CLK and PLLAUX_PHI0_CLK) and the wrong name of GMAC1_MII_RMII{*}RGMII{*}_TX_CLK !image-2023-10-23-18-04-49-070.png! !image-2023-10-23-18-05-29-744.png! Mux16 is using redundant source (PLL_PHI0_CLK) and the wrong name of GMAC1_MII_RMII{*}RGMII{*}_TX_CLK !image-2023-10-23-18-06-40-315.png! !image-2023-10-23-18-06-56-013.png! K358

ID	Subtype	Headline and Description
		EMAC needs to be changed to GMAC !image-2023-11-06-10-20-24-621.png! !image-2023-11-06-10-20-52-089.png! !image-2023-11-06-10-21-16-209.png! !image-2023-11-06-10-26-03-780.png! !image-2023-11-06-10-26-56-033.png! !image-2023-11-06-10-27-13-367.png! !image-2023-11-06-10-27-40-888.png! !image-2023-11-06-10-29-42-354.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Clock system diagram is not mapping to the driver Expected behavior: Correct the driver Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97549	Bug	[MCU] Some bits in DCM_GPR:DCMRWF2 aren't supported Detailed description (how to reproduce it): PGOOD_POLARITY is mentioned in chapter "41.8 PMIC Handshake with MCU (applicable for S32K3x8)" as a bit will impact to handshake feature. Bit "PLL1 LOL Reset Enable" relates to Lost of lock reset feature. Need to be supported. Those bits need to be supported. !screenshot-1.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Those bits are not supported Expected behavior: Those bits are supported Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97560	Bug	[MCU] FXOSC Differential mode is not available anymore but exist in configurator Detailed description (how to reproduce it): FXOSC Differential mode is not available anymore but exist in configurator: description field of some nodes. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Differential mode is not available anymore but exist in configurator Expected behavior: Differential mode is removed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97588	Bug	[MCU] Configurable SIRC Trimming node though considered reserved

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): SIRC Trimming can be configured on the interface though it is considered reserved following RM's mentions !image-2023-10-24-08-37-39-461.png! !image-2023-10-24-08-38-06-715.png! !image-2023-10-24-08-38-20-013.png! This mistake is causing build failures on K311 !image-2023-10-24-08-39-21-434.png! because DCM_GPR_DCMRWF2_FIRC_TRIM_BYP_STDBY_EXT_MASK is removed from the header files !image-2023-10-24-08-41-25-258.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: SIRC Trimming can be configured on the interface though it is considered reserved following RM's mentions Expected behavior: Remove SIRC Trimming nodes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98104	Bug	[MCU] Inconsistent levels of alarms between CT and EB Detailed description (how to reproduce it): On EB, this below case is considered as an error !image-2023-10-27-14-04-44-130.png! but it is a warning for CT !image-2023-10-27-14-06-50-654.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Inconsistent levels of alarms between CT and EB Expected behavior: Update both interfaces consistently Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98194	Bug	[MCU] Redundant lines of code Detailed description (how to reproduce it): Below lines of code underlined in red can be removed as they are redundant due to below reason VoltageDetectFlags of such cases have only 1 flag therefore after VoltageDetectStatus = (VoltageDetectStatus >> 16U); EventReport = (VoltageDetectStatus & VoltageDetectFlags); EventReport = 0 or EventReport = VoltageDetectFlags !image-2023-10-30-09-56-31-137.png! !image-2023-10-30-09-59-32-933.png! !image-2023-10-30-10-01-07-666.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Redundant lines of code

ID	Subtype	Headline and Description
		Expected behavior: Remove such lines of code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98258	Bug	[MCU] Wrong system clock frequency limitations on the interface Detailed description (how to reproduce it): 1. M276 ({*}AIPS_PLAT_CLK{*}, *AIPS_SLOW_CLK range is not corrected follow RM mention in {*}EB and CT tool{*}) AIPS_PLAT_CLK can be configured 80MHz* but the maximum frequency is mentioned in RM 60MHz !image-2023-10-30-14-44-36-040.png|width=762,height=421! AIPS_SLOW_CLK can be configured 40MHz but the maximum frequency is mentioned in RM {*}30MHz{*}{*}{*} !image-2023-10-31-09-12-41-563.png|width=813,height=293! !image-2023-10-30-14-48-23-823.png! {*}+2. K312 and K311 ({*}{*}AIPS_PLAT_CLK{*}{*},{*} *AIPS_SLOW_CLK range is not corrected follow RM mention in {*}EB and CT tool{*}{*}){*} AIPS_PLAT_CLK can be configured 80MHz but the maximum frequency is mentioned in RM 60MHz AIPS_SLOW_CLK can be configured 40MHz but the maximum frequency is mentioned in RM 30MHz !image-2023-10-30-14-59-55-148.png|width=886,height=475! !image-2023-10-30-15-00-35-353.png|width=732,height=490! 3. K388 QSPI_MEM_CLK range is not corrected (EB tool). RM mention is 160 MHz !image-2023-11-02-15-09-22-364.png|width=889,height=270! RM mention: !image-2023-11-02-15-10-50-493.png|width=752,height=565! 4. S32K358 DCM_CLK can be configured 60 MHz (EB and CT tools) but the maximum frequency is mentioned in RM 48 MHz !image-2023-11-02-15-13-37-044.png|width=735,height=297! !image-2023-11-02-15-13-46-159.png|width=642,height=116! RM mention:* {*}!image-2023-11-02-15-14-44-873.png!{*}{*}{*} Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Wrong system clock frequency limitations on the interface Expected behavior: Correct system clock frequency limitations on the interface Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98343	Bug	[MCU] Wrong descriptions Detailed description (how to reproduce it): 1. McuAlternateResetIsrUsed !image-2023-10-31-10-57-20-596.png|width=817,height=238! need to change to POWER_IP_RESET_ALTERNATE_ISR_USED !image-2023-10-31-10-58-38-332.png|width=815,height=89! 2. FLEXCAN_CLK should be more detailed OnlyFLEXCAN[3]_PE_CLKis available on theS32K322, S32K341,and S32K342 FLEXCAN[3:7]_PE_CLK on K358, K388

ID	Subtype	Headline and Description
		!image-2023-10-31-11-03-52-794.png! !image-2023-10-31-11-05-00-658.png! !image-2023-10-31-11-08-06-057.png! 3. GMAC RX CLK Need to add GMAC_CLK_RX: S32K358 Mux 8 and mux9 should be also updated !image-2023-10-31-11-23-23-913.png! !image-2023-10-31-11-25-41-737.png! !image-2023-10-31-11-26-03-680.png! Wrong errors: Clock User Mode Support needs to be changed to Get Clock Frequency !image-2023-11-09-08-39-00-978.png! 4. Wrong description for pll node: !image-2024-07-22-13-49-41-902.png! !image-2024-07-22-13-50-18-869.png! !image-2024-07-22-13-50-48-152.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Wrong descriptions Expected behavior: Correct descriptions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98714	Bug	[PWM] Different between code driver and requirement export Detailed description (how to reproduce it): [Requirement export has not been updated about some type of argument, function and miss some new function (or maybe change name function a lot). Tester had stand at test tag: PVT_TEST_PWM_S32K3XX_M27X_400_140* and dev tag: PWM_125 Please open attachment .xlsx to detail] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [N/A] Observed behavior: [Checking code driver and requirement export] Expected behavior: [No different between prototype in both code driver and requirement export] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Update at requirement export]
ARTD-98777	Bug	[Ocu] Get wrong channel when calling Ocu_StartChannel Detailed description (how to reproduce it): When configuring the Ocuchannelid not in ascending order but instead in a random arrangement, the desired channel is called incorrectly when calling the Ocu_StartChannel function. See details in attached image: !image-2023-11-02-13-26-43-321.png|width=939,height=190! Example: I am starting Ocu_StartChannel(0) then OcuChannelid=0 it will call OcuHWSpecificSettings_6(EMIOS_2_CH_16). ! image-2023-11-02-14-25-53-789.png|width=881,height=362! When debug sees Ocu_StartChannel(0) then OcuChannelid=0 it is calling OcuHWSpecificSettings_0(EMIOS_0_CH_4). ! image-2023-11-02-14-28-27-231.png|width=875,height=402!

ID	Subtype	Headline and Description
		It is getting the wrong array value Ocu_Ipw_IpChCfgPB_VS_0[OCU_CONF_CHANNELS_PB] in file Ocu_Ipw_VS_0_PBcfg.c ! image-2023-11-02-14-42-24-100.png|width=874,height=806! This problem occurs similarly to S32CT Configuration in attached file. Preconditions: Run on EBT and S32CT Test Case ID (internal TC that caught the defect) optional: Ocu_TS_104 Observed behavior: Called wrong channel Expected behavior: Call the correct channel Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98793	Bug	[S32K3XX_4.0.0] SENT: Update Generate Code Template to generate SENT_CONFIG_EXT only in PB mode Collection of all configuration structures declarations currently generate all both Precompile and PostBuild Mode. #define SENT_CONFIG_EXT Update generate code template. It only generated in PostBuild Mode. !image-2023-09-19-17-56-30-474.png!
ARTD-99062	Bug	[MCL] The code generated between EB and CT tools is different Detailed description (how to reproduce it): The code generated between EB and CT tools is different. Please see the attached file below for more details. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mcl_TS_COT_006 Observed behavior: The code generated between EB and CT tools is different. Expected behavior: The code generated between EB and CT tools is same. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-99176	Bug	[MCU] Redundant options of Spread Selection node Detailed description (how to reproduce it): On K311 Spread Selection has 2 options !image-2023-11-06-11-41-44-355.png! but RM mentions !image-2023-11-06-11-44-43-336.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Redundant options of Spread Selection node Expected behavior: Correct Spread Selection node Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-99276	Bug	[MCU] SMPSCONFIG can not be configured Detailed description (how to reproduce it): On S32DS interface, SMPSCONFIG can not be configured for K358 and K396 !image-2023-11-07-10-31-06-247.png! !image-2023-11-07-10-31-49-191.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: SMPSCONFIG can not be configured Expected behavior: SMPSCONFIG can be configured Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-99519	Bug	[MCU]Optimize the definition of the reset reason to avoid mistake from users. Detailed description (how to reproduce it): The definition of the reset reason is different for different APIs. # For the API: Mcu_GetResetReason. The low-level return the below enum value which the DES located in the lower bits. ! image-2023-11-08-09-56-03-919.png! 2.For the API: Mcu_GetResetRawValue. The low-level return another MACRO list which the FES located in the lower bits. !image-2023-11-08-09-57-21-434.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not yet synchronized definitions between the two APIs Expected behavior: Synchronized definitions between the two APIs Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-99776	Bug	[S32K3 4.0.0][Mem_ExFls] Wrong inclusion of MemAcc_GeneralTypes.h In memory drivers the file MemAcc_GeneralTypes.h is included for E_MEM_SERVICE_NOT_AVAIL but as per AUTOSAR R21-11, MCAL should not include MemAcc_GeneralTypes.h, the define of macro should come from Std_Types.h
ARTD-100022	New Feature	[Icu] Add Filter Clock Select for IcuEmiosDigitalFilter. NewWorkDescription: The eMIOS filter support two clocks in FCK bit: 0b Prescaled clock 1b eMIOS module clock !image-2023-11-13-10-24-08-282.png! But the configuration in EB/CT doesn't support clock selection: !image-2023-11-13-10-27-34-248.png! Please help add this feature because the default clock source possibly does not meet the customer's current filtering needs. Community post [How to Choose the Clock for IcuEmiosDigitalFilter NXP Community|https://community.nxp.com/t5/S32K3-Internal-Community/How-to-Choose-the-Clock-for-IcuEmiosDigitalFilter/td-p/1753366] Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-100186	Bug	[AE][S32M27x] Fix finding review checklist Detailed description (how to reproduce it): There are findings after perform review checklist in ticket ARTD-89426. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Violations in review checklist Expected behavior: All the violations are fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100174	Bug	[S32K3xx_S32M27x_4.0.0] CRC: Function in ReqExport.txt doesn't match with function in driver code Detailed description (how to reproduce it): [When I compare functions in ReqExport.txt and functions in driver code, I saw some differents. Details in attach file] Preconditions: [N/A] Observed behavior: [N/A] Expected behavior: [They are matched 100%] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-100203	Bug	[MEM_INFLS]: Conflict check before write/erase Detailed description (how to reproduce it): In current implementation, we didn't considering the conflict access with HSE FW, its better to check the status by GPR register which indicate whether HSE FW are using flash before write/erase. Preconditions: HSE FW are using flash Test Case ID (internal TC that caught the defect) optional: None Observed behavior: fls driver may return error Expected behavior: Before write/erase, check the GPR register status. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Use software semaphore to make a arbitration mechanism
ARTD-100602	Bug	[S32K3xx_S32M27x_4.0.0] MCU: Mcu_GetClockFrequency for QSPI_SFCK_CLK in S32K388 return wrong value Detailed description (how to reproduce it): Mcu_GetClockFrequency for QSPI_SFCK_CLK in S32K388 return wrong value !image-2023-11-15-21-37-45-765.png!!image-2023-11-15-21-37-57-078.png! Preconditions: S32K388 Test Case ID (internal TC that caught the defect) optional: Mcu_TC_K3_1001 Observed behavior: return wrong value Expected behavior: return expected value Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: [....]
ARTD-100848	New Feature	[ZIPWIRE] Implement Errata ERR051988 using the define from Base NewWorkDescription: Due to the time constraints of the CF milestone the Errata was implemented without the specific tag in Base(Soc_Ips.h) Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Implement the errata from ARTD-99359 using the define added in ARTD-100564.
ARTD-100876	Bug	[MCU] Reset after configuring CMU_FC_6 on K388 Detailed description (how to reproduce it): RM mentions that CMU_FC_6's source is FIRC_CLK !image-2023-11-17-17-38-27-765.png! However, Reset happens if driver implements as RM's mentions (FIRC_CLK is the source of CMU_FC_6) !image-2023-11-17-17-40-12-739.png! I tried to use FXOSC as the source of CMU_FC_6 => no issue !image-2023-11-17-17-41-55-717.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Reset event after configuring CMU_FC_6 on K388 Expected behavior: No reset event happens Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-101261	Bug	[MCU][S32K3-S32M27x] wrong divider mask and divider register Detailed description (how to reproduce it): in register description,the cgm0mux11dc0[DIV] of K311, K312, K342, K344 have 4 bit divider in but in register on S32DS and header file have 3 bit divider !image-2023-11-20-19-09-37-043.png|thumbnail! !image-2023-11-20-19-10-46-241.png|thumbnail! ! image-2023-11-20-19-11-53-542.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: have 3 bit divider value in register and header Expected behavior: have 4 bit divider value in register and header Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-101322	Bug	[PWM][S32DS] Cannot generate channel when config channel Id equal total number channel Detailed description (how to reproduce it): [Change channel ID from equal Channel index (value of current Channel ID is 2) to total number (3 channel). In this configuration, we have 3 channel pwm is PwmChannel_0, PwmChannel_1 and PwmChannel_2. After generate with changed Channel Id of PwmChannel_2 configuration, Pwm_VS_0_PBcfg.c loose the changed channel. The attachment 7z file contain code generate and configuration before and after change only one node Channel ID of PwmChannel_2.] Preconditions: [Change value of Channel ID of any channel to total number channel will not raise any error.] Test Case ID (internal TC that caught the defect) optional: [Pwm_TS_100_FlexIo] Observed behavior: [Change channel ID from 2 to 3 but s32ds did not raise any error

ID	Subtype	Headline and Description
		!image-2023-11-21-14-35-11-821.png! Code generation with this changed configuration missed PwmChannel_2 !image-2023-11-21-14-37-04-902.png!] Expected behavior: [Change value of channel ID equal or exceed number of total channel is not valid] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Channel ID must mapping with channel index]
ARTD-101457	Bug	[ADC] DSPSS is not working in clock threshold mode Detailed description (how to reproduce it): DSPSS is not working on clock threshold mode with multiple threads running in parallel Preconditions: ADC driver tag: ADC_517 Test Case ID (internal TC that caught the defect) optional: Adc_TS_DSPSS_001 cfg clock_threshold Observed behavior: Because of the workaround reset routine when start a new conversion: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/adc/pull-requests/1259/diff#ip/IP_SDADC/src/Sdadc_Ip.c?t=872] It impacts other running threads Expected behavior: DSPSS work with clock threshold mode. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-101475	Bug	[Mem_INFLS]: The performance for read is too slow. Detailed description (how to reproduce it): The performance of the read operation is too bad. According to my test, it needs 321 times of the mainfunction call for 160 Bytes of data. Its unreasonable. !image-2023-11-21-17-48-12-909.png! !image-2023-11-21-17-48-24-592.png! !image-2023-11-21-17-48-32-359.png! !image-2023-11-21-17-48-40-135.png! !image-2023-11-21-17-48-51-634.png! Preconditions: Burst mode disabled Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Cost too much time Expected behavior: improve the performance Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-101563	Bug	[AE] Fix warnings in VSMD report. Detailed description (how to reproduce it): Have some warnings in VSMD report. !image-2023-11-22-14-02-13-021.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A

ID	Subtype	Headline and Description
		Observed behavior: Warnings in VSMD report Expected behavior: No warnings in VSMD report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-101659	Bug	[PORT] [S32K3XX_S32M27X] Error with the default configuration on pin tool S32CT Detailed description (how to reproduce it): Get error with the default configuration when configure route all pins on pin tool {*}Issue 1{*}: Safe mode control (SMC) is not disabled when configure input mode PTA4 PTA10 ({*}all derivatives{*}) !image-2023-11-23-14-34-46-185.png! {*}Issue 2{*}: OBE field appears error when configure mode adc0_s13 (input) on pin PTF6 only package LQFP176 !image-2023-11-23-14-16-55-236.png! Issue 3: OBE and DSE fields appear error when configure input mode on pin PTE12 only package LQFP176 !image-2023-11-23-14-22-50-845.png! Preconditions: Configure on pin tool S32CT Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Get error with the default configuration on pin tool Expected behavior: No error appears on pin tool. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-101662	Bug	[S32K3XX][Rm] Incorrect the MRC minimum size Detailed description (how to reproduce it): Lack the modulo 32 byte invalidation for start address and check minimum size for a region Preconditions: Enable XRDC and add config for memory region Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Cannot configure Expected behavior: Can configure Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the config template
ARTD-101685	Bug	[S32K3xx_S32M27x_4.0.0] [Mem_Eep] Build fail when enable multicore type 3 Detailed description (how to reproduce it): Error when build multicore type 3 test Preconditions: multicore type 3 enable Test Case ID (internal TC that caught the defect) optional: Observed behavior: error when build multicore type 3 with mem_eep Expected behavior: Build and run multicore type 3 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add missing variable field in the structure type.

ID	Subtype	Headline and Description
ARTD-101723	Bug	[ETH][GMAC] Clock signals for GMAC on S32K388 are not configurable because of lacking of information in Reference Manual Detailed description (how to reproduce it): The GMAC clock signals clk_rmii_i, clk_tx_i and clk_rx_i on S32K388 cannot be configured due to unclear information about the DCMGPR registers as described in S32K3XX Reference Manual Rev. 8, Draft B, 9/2023 !image-2023-11-23-17-37-56-938.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The GMAC clock on the S32K388 cannot be configured Expected behavior: The GMAC clock on the S32K388 can be configured Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-101717	Bug	[S32K3xx_S32M27x_4.0.0] I2S: Examples failed - 358 and k388 Detailed description (how to reproduce it): EB and DS Example on S32K344 is failing on P32K344EHVMMS 0P55A, P32K344EHVPBS 1P55A, on S32K396 (P32K396EHMJBS OP40E), DS example is failing Preconditions: example test on EBT and DS Test Case ID (internal TC that caught the defect) optional: I send new update for example EBT: I2s_Flexio_Flexio_example_S32K358 => Passed I2s_Flexio_Flexio_example_S32K388 => FAIL (receive buffer is 0) I2s_Flexio_Sai_example_S32K344 => fail on Q257 (receive buffer is 0) and Q172: checking match receive buffer and send data is fail I2s_Sai_Flexio_example_S32K358 => passed I2s_Sai_Sai_example_S32K388 => FAIL (receive buffer is 0) I2s_Flexio_example_S32K396 => Passed DS I2s_Example_Flexio_Master_Tx_Flexio_Slave_Rx_S32K396 => FAIL (receive buffer is 0) I2s_IP_Example_Flexio_Master_Tx_Flexio_Slave_Rx_S32K396 => passed I2s_Example_Flexio_Master_Tx_Sai_Slave_Rx_S32K344 => passed I2s_IP_Example_Flexio_Master_Tx_Sai_Slave_Rx_S32K344 => fail on Q257 (receive buffer is 0) and Q172: checking match receive buffer and send data is fail I2s_Example_Flexio2Flexio_S32K388 => stuck running (stuck at Port Init) I2s_Example_Sai2Sai_S32K388 => stuck running (stuck at Port Init) I2s_IP_Example_Sai2Sai_S32K388 => stuck running I2s_IP_Example_Flexio2Flexio_S32K388 => FAIL (receive buffer is 0) I2s_Sai_Flexio_example_S32K358 => FAIL (receive buffer is 0) I2s_IP_Sai_Flexio_example_S32K358 => stuck at Get status Observed behavior: example is fail, https://nxp1.sharepoint.com/:x:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B7D79D20A-C605-4A29-979C-AA2C7ED2EE59%7D&file=RTD_EXAMPLE_TestReport.xlsx&nav=MTVfezAwMDAwMDAwLTAwMDEtMDAwMC0wMjAwLTAwMDAwMDAwMDAwMH0&MAGLEV.p2p_ns.rwc&action=default&mobileredirect=true Expected behavior: example is pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Investigate failing test cases, these are passing on the older version of chips.
ARTD-101805	Bug	[S32K3XX] [BASE]: Missing DLLCRA bitfield of S32K344_QUADSPI.h Detailed description (how to reproduce it): _**_ The header files of S32K344_QUADSPI.h is missing some defines for MASK, SHIFT, WIDTH for QuadSPI_DLLCRA_DLLEN. Currently, this defines is not impact to K344 because Quadspi is using system clocks (80mhz in sys_init) which is unnecessary to enableDLL. However, if user want to run QSPI on S32K33 with higher clock config (for example 120mhz), it is required to have those defines to enableDLL {*}{*}{_}*!image-2023-11-24-15-10-34-355.png|width=587,height=388!*{_} Going deeper into the RM of S32K3xxRM_rev8_DraftB, I see that there are many more missing defines of some bits in some registers, so I will also list them here to check: DLLCRA_DLLEN MCR_ISD2FA DLLCRA_DLLEN DLLCRA_SLAVE_AUTO_UPDT DLLCRA_DLL_REFCNTR

ID	Subtype	Headline and Description
		DLLCRA_DLLRES FLSHCR_TDH Preconditions: Review the RM and header file. Test Case ID (internal TC that caught the defect) optional: No Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-101855	Bug	[MCU] PMC_AE_MONITOR[LVDCF] flag is not cleared by Mcu driver after AE reset As stated by RM, PMC_AE_MONITOR[LVDCF] is always set after AE reset !image-2023-11-24-17-51-48-768.png! Mcu doesn't clear flags anymore but In order to work properly, CanPHY IP expects the flag must be cleared. other than that. the flags should be cleared/handled after reset in order to not loss event after that. !image-2023-11-24-17-54-59-912.png! please help to investigate it in Mcu driver if it should clear the flags or not, now when using CanTrcv driver, we must clear the flag manually in our tests.
ARTD-101890	Bug	[WDGIF] "Unsatisfied components dependencies..." error displays when adding "wdg" driver Detailed description (how to reproduce it): 1. Create NPW for S32K322/S32K374/S32K376/S32K394 to enable RTD 2. Open S32CT Tools > Peripherals Tool 3. Click on the "SDK Management" tool 4. Select "wdg" driver Observed behavior: There is an error displayed "Unsatisfied components dependencies...": !image-2023-11-26-22-09-40-660.png|thumbnail! Expected behavior: No error displays
ARTD-102167	Bug	[crc] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-102182	Bug	[dio] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-102221	Bug	[i2s] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none

ID	Subtype	Headline and Description
		Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-102242	Bug	[memacc] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-102275	Bug	[port] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not.

ID	Subtype	Headline and Description
		Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-102296	Bug	[sent] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.

ID	Subtype	Headline and Description
ARTD-102466	New Feature	Exclusive Area implementation for OUDIS register in function Emios_Mcl_Ip_ComparatorTransferDisable NewWorkDescription: Adding Exclusive Area implementation for register OUDIS in function Emios_Mcl_Ip_ComparatorTransferDisable Compare with function Emios_Pwm_Ip_ComparatorTransferDisable in PWM module, the function Emios_Mcl_Ip_ComparatorTransferDisable located in PWM_Exclusive_Area_30 !image-2023-11-30-13-25-08-827.png! Not have this implementation in Mcl_Emios_SetCounterBusPeriod !image-2023-11-30-13-25-46-318.png! Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Adding Exclusive Area implementation for register OUDIS same with other modules.
ARTD-102484	Bug	[Mem_InFls] Generated files got missing names when nodename too long Detailed description (how to reproduce it): Put name of MemInstance longer (such as MemInstance_Local_Config_Bank_A) !image-2023-11-30-14-58-44-463.png! Generate project and check Mem_43_INFLS_Cfg.c file Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Mem_43_INFLS_MemInstances definition has wrong SectorBatch's name: Mem_43_INFLS_MemInstance_Local_Config_Bank_A_SectorB cause errors !image-2023-11-30-15-00-57-087.png! Expected behavior: Correct name as Mem_43_INFLS_MemInstance_Local_Config_Bank_A_SectorBatch, Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-102599	Bug	[PWM] Emios_PWM error for setting up deadtime in example Detailed description (how to reproduce it): Select example Emios_Pwm_Ip_Example_S32K344, Config Emios_PWM channel mode as OPWMCB Config Deadtime differ than 0 Config PWM Emios channel equal to MCL Master bus Prescaler Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generation error occurs: Information: [Generation error][ERR050575] The channel EMIOS_0_CH_4 configured in OPWMCB mode with lead or trail dead time insertion features enabled must have channel prescaler equal to the timebase channel prescaler configured in MCB mode in MCL. !image-2023-12-01-17-46-29-440.png! Expected behavior: No error when channel prescaler equal to the timebase channel prescaler configured in MCB mode in MCL Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-102603	Bug	[Mem_Eep] Missing condition in Mem_Eep.xdm: "MemMaxReadBlockSize" and "MemMaxWriteBlockSize" must be 512byte aligned Detailed description (how to reproduce it): Missing condition in Mem_Eep.xdm: "max read" and "max write" must be 512byte aligned "MemMaxReadBlockSize" and "MemMaxWriteBlockSize" are the maximum number of bytes to read/write/erase in one cycle of the Mainfunction. Currently, Mem_Eep driver only support read/write/erase with blocks (multiple of 512). So "MemMaxReadBlockSize" and "MemMaxWriteBlockSize" must be 512byte aligned. !image-2023-12-03-10-21-06-545.png! Preconditions:

ID	Subtype	Headline and Description
		NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing condition in Mem_Eep.xdm: "max read" and "max write" must be 512byte aligned Expected behavior: In Mem_Eep.xdm: "max read" and "max write" must be 512byte aligned Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add condition in Mem_Eep.xdm and .component
ARTD-104259	Bug	[MemAcc]: Fee swap error when the read & write burst size configured to 128. Detailed description (how to reproduce it): Swap error when the read & write burst size configured to 128. when decrease the burst read size to 1, and the burst write size to 8, it works normally. The issue come from MemAcc, when Fee request a length =128, and the requested area is on 2 sub address area (see the picture for easier to understand). MemAcc should split 2 request for each SubAddress area (Mem Instance). But currently, MemAcc only request the first subaddress with length =128. > The mem driver will not accept the job because the length is over the size of the mem instance > job fail. Please refer to the attached project which based on the default example. [^Fee_Example_S32K344.7z] Preconditions: read & write burst size configured to 128 and trigger swap. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: FEE return error, can't swap as expected. Expected behavior: None Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update code to split request for 2 SubAddress when the length is bigger than remaining length of the first SubAddress
ARTD-104315	Bug	[adc] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change

ID	Subtype	Headline and Description
		node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-104707	Bug	[Mem_InFls] Perform exclusive area analysis Detailed description (how to reproduce it): Missing reentrancy safeguards for C40_Ip_pFlashBaseAddress in C40_Ip_InvalidPrefetchBuff*_ function. This can cause unexpected behavior during concurrent calls. To ensure that all critical sections are guarded, exclusive area analysis should be done. Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Do exclusive area analysis.
ARTD-104795	New Feature	[build_env] Need to use the common Reference List in UM and IM instead for all drivers [ARTD] Need to use the common Reference List in UM and IM instead for all drivers Currently I analyzed and observed that the Reference List in UM and IM are not consistent and sometimes there are errors not up to date and in sync with the Internal SOW document. It seems to me that the UM/IM Reference List are generated for each driver based on information of each driver, but not taken from some common information of the release. For the test documentations, the document reference list are taken from build environment that is common for all drivers. I suggest to use the same approach for the Reference List of UM/IM. Please see more details in the Attached Excel file. This is the list of items checked https://nxp1.sharepoint.com/:x:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B09D2643E-CBEE-4169-BF51-780E32363E85%7D&file=Tool_Support_Automate_RRR.xlsx&action=default&mobileredirect=true The reason: Since the information in Reference List is not taken from the common source, so there are issues for some modules that the Reference is not correct. This take time (effort) of QA team. Analysis: This need to be discussed and reviewed by the Technical Leads of RTD in G0
ARTD-104981	Bug	[Spi][S32K3]When HREQSupport is false, SpiHostRequest value is still used !image-2023-12-12-09-28-51-346.png! !image-2023-12-12-09-28-59-577.png! Proposed solution: add a check for spiReqSupport
ARTD-105008	New Feature	[SPI][SLAVE MODE] Could SPI driver update TX/RX buffer address directly when a transfer has completed? Similar with UART driver. NewWorkDescription: [Customer used RTD IPL driver and the SPI worked in slave mode with DMA. Customer feedback the large time cost between 2 SPI transfer. They call Lpspi_Ip_AsyncTransmit() in callback to start next transfer. They only want to update the TX/RX buffer address but the IPL Transmit_ api will re-configure the whole module, it costs time. The IPL API Lpspi_Ip_AsyncTransmit()_ cost much time. In UART driver, we could call SetTxBuffer() in callback {_}CompleteSendUsingDma{_}() to update the tx buffer and start the next transfer directly. It saves time. It seems that there isn`t any similar API to implement this feature in SPI driver. The TxDmaContinueTransfer()_ in SPI driver couldn`t update the buffer. Update/Clarification: Performance improvement requested between two transfers: 2us (the shorter the better) Update: Customer uses only IP Layer Update: Customer needs to change the Tx Buffer address between two transfers. Address of Rx buffer is already fixed in place before we start the transfer. Customers uses the DMA. Update: Customer uses only slave mode in this use case. Update: Customer SPI use case: Continuous CS, 8B per frame, Datawidth=8bit]

ID	Subtype	Headline and Description
		Requirement source: [Customer wish a SPI api which is similar with SetTxBuffer()_ in UART to only update buffer address when a transmission is completed instead of calling Transmit api. Or optimize Lpspi_Ip_AsyncTransmit() execution efficiency.]
ARTD-105081	Bug	[ADC] Incorrect maximum constraint of BctuNewDataDMAEnableMask on S32DS Detailed description (how to reproduce it): On S32DS, node "BctuNewDataDMAEnableMask" only allows the maximum value of 7. !image-2023-12-13-15-06-23-480.png! But on S32K396, the BCTU_1 can support up to 4 ADC instances which requires the mask value is 0b1111 (15d) Preconditions: Using BCTU on S32K396 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: See description Expected behavior: Can configure any of 4 ADC hardware instances Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Correct the "max_expr" attribute of node "BctuNewDataDMAEnableMask" Refer to the correct constraint in node "BctuAdcTargetMask"
ARTD-105092	Bug	[ADC] Generated defines for BCTU IP instances used are always 0 Detailed description (how to reproduce it): Defines for BCTU IP instances used are always 0 !image-2023-12-13-15-14-36-741.png! Preconditions: Using 2 BCTU instances on S32K396 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: See description Expected behavior: Macro defines fot BCTU instances used must be match with the configurator Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update code generation for S32DS: !image-2023-12-13-15-16-49-412.png!
ARTD-105117	Bug	[S32K3] [RTD] Problems while updating RTD from 3.0.0 to 4.0.0 Detailed description (how to reproduce it): The 4.0.0 conflict with 3.0.0. The 3.0.0 SDK package selection disappeared after installing 4.0.0. Which means that once user installed 4.0.0, the old projects of 3.0.0 cannot be open with 3.0.0 RTD anymore. This is not conducive to users' management of old projects, and it's a common requirement for SW upgradation. (The 1.0.0, 2.0.x don't conflict with 4.0.0.) !image-2023-12-13-15-26-56-756.png|thumbnail! Besides, although the 3.0.0 SDK package disappeared, we still can find the 3.0.0 in Installation Details. That didn't make sense. Upgrading 3.0.0 to 4.0.0 has problems. When we open the old 3.0.0 project after installing 4.0.0, it reported error of SDK settings. !image-2023-12-13-16-22-06-982.png|thumbnail! !image-2023-12-13-16-22-17-040.png|thumbnail! It seems that we can attach the 4.0.0 to project to upgrade the SDK, like following:

ID	Subtype	Headline and Description
		!image-2023-12-13-16-24-03-541.png|thumbnail! !image-2023-12-13-16-24-10-685.png|thumbnail! !image-2023-12-13-16-24-45-413.png|thumbnail! But the function is not perfect enough. There still are a lot of modification should be made by user after upgradation because the compilation settings and Driver configuration are not 100% inherited. !image-2023-12-13-17-17-04-241.png|thumbnail! !image-2023-12-13-16-33-32-838.png|thumbnail! !image-2023-12-13-16-26-46-318.png|thumbnail! There still was error with SDK settings even though after attaching new SDK: !image-2023-12-13-17-24-13-220.png|thumbnail! And partial files weren't upgraded successfully after attaching new SDK: !image-2023-12-13-17-26-49-320.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-105229	Bug	[S32K3] Wrong SW Version in startup.c of 4.0.0 Detailed description (how to reproduce it): The startup.c file has wrong SW Version: !image-2023-12-14-11-00-45-888.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-105430	Bug	[MCL]: Invalidate cache line works abnormal in some case Detailed description (how to reproduce it): The logic in "hwAcc_ArmCoreMx_DataCacheInvalidateByAddr" function have some problem. Suppose the below situation: if addr % CACHE_LINE != 0 && (addr length) % CACHE_LINE <= (addr % CACHE_LINE) then we will miss invalidating the last line. Then it will cause many upper layer issues. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: None Expected behavior: None

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-105454	Bug	[Spi][ASR 4.7][ASR 4.4] Meaning of parameter Length in Spi_SetupEB() Detailed description (how to reproduce it): In our implementation, Function Spi_SetupEB() has parameter Length looks like mean that the number of byte of SrcDataBuffer and DestDataBuffer. However, our customer said that it should be the number of element that defined under Framesize (SpiDataWidth) as per Autosar Spec: !image-2023-12-15-19-26-02-545.png! For example: Config Channel's SpiDataWitdh = 16bit Spi_DataBufferType TxChBuf[2] = \{0xaa,0xbb}; Spi_DataBufferType RxChBuf[2]; Spi_SetupEB(Channel, TxChBuf, RxChBuf, 1} {color}>* {color:#172b4d}In their opinion, the Length in this case should be 1 (means 16bits as per SpiDataWidth).* But in our current implementation, this value in this case must be 2*{color}Seems that the Autosar spec is not clear in this case, so it make some confusions for us. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The customer needs to set the length in bytes for the SPI transfer in {*}SPI_SetupEB{*}() function. Parameter SpiEbMaxLength is also affected Expected behavior: The customer needs to set the length in data elements as per SPI 00180 requirement for the SPI transfer in SPI_SetupEB() function SWS_Spi_00180 SWS_Spi_00376 Also check following document for clarifications within autosar forum on this topic: [^AUTOSAR+JIRA +2023-12-20T10_06_30+0100.doc]_ Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Treat the Length parameter as number of data elements which can be in uint8, uint16 and uint32 as defined by {*}SpiDataWidth{*}. For SpiDataWidth uint 16 the length must be multiplied by 2 For SpiDataWidth uint32 the length must be multiplied by 4 So the same IP functions can be used.
ARTD-105463	Bug	[Rm] Missing Xrdc_0_USDHC PDAC in Tresos configuration Detailed description (how to reproduce it): When configuring S32K358 Rm module in EB Tresos, in XRDC Peripheral Config is not possible to configure USDHC (PDAC slot number 313) which is documented in memmap of S32K3XXRM Reference Manual Rev. 8 DraftB, 09/2023. !image-2023-12-15-15-11-55-743.png! Preconditions: Configure XRDCPeripheralSlot {*}Xrdc_0_USDHC{*}. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Error appear when configure {*}Xrdc_0_USDHC{*}. Expected behavior: Possibility to configure {*}Xrdc_0_USDHC{*}. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: To update missing entries in Rm resource files for derivatives S32K328, 338, 348, 358
ARTD-105805	Bug	[S32K3][ICU] ICU timestamp notification is different from its function description.

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): According to the description of ICU timestamp notification in ICU UM, the user notification shall be called if the number of requested timestamps (Notification interval > 0) are acquired. !image-2023-12-19-11-14-17-818.png! But this notification was called every time if timestamp came, no matter what the setting of NotifyInterval was. It was called every time in below position. !image-2023-12-19-11-18-05-610.png! !image-2023-12-19-11-23-49-614.png! And more unreasonable, user notification function will be invoked twice if the number of requested timestamps was met. !image-2023-12-19-11-23-15-553.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-105913	New Feature	[ICU] Change SAIC(0x2) to SAIC(0x42) to capture input signal level. NewWorkDescription: As described in AAI-2092, the 31st bit of A register can be used to indicate rising and falling edge in SAIC sub-mode: !image-2023-12-20-11-10-33-283.png! !image-2023-12-20-11-39-48-530.png! Not only the API to be improved, but also we strongly suggest changing the SAIC(0x2) to SAIC(0x42). One use case is that timestamps with signal level indicators can used for very high frequency and high precision signal measurement. Here is a demo to show the use case of it: [^Icu_Pwm_Demo_Rtd200_Q172.zip] (modified the RTD code) Because of the execution time of ICU ISR, the Signal Measurement mode cannot deal with neither very high frequency, nor very short pulse. And some customers compliant it several times. It's a real requirement from marketing, but also a feature of eMIOS. Requirement source: RM (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: See description.
ARTD-106093	New Feature	[MCU] Check that reserved bitfields from register are not cleared/ are not overwritten. NewWorkDescription: Check that reserved bitfields from register are not cleared/ are not overwritten. Example in Clock_Ip_SetPlldigRdivMfiMfnSdmenSsscgbypSpreadctlStepnoStepsize() in Mcu_TS_T40D11M40I0R0\src\Clock_Ip_Pll.c Issue: It clears the reserved bitfields along with setting the bitfields RDIV and MFI*. According to FMEA, registers should be written with "read-modify-write". Requirement source: Safety requirement, do not overwrite reserved bitfields from registers. Proposed solution optional: [....]
ARTD-106295	Bug	RTD for S32M2XX (AE10 Driver) Issue 1: RTD Driver shall fix bug related to Frame Counter Fault processing SPI comm has GHS in which Frame Counter occupies bits from 14:8, which gives it range 0 127. Variable u32FrameCounter is never checked and never limited to max value of 127. On AE side, if counter goes above, it starts from 0 again, this needs to be implemented on RTD side

ID	Subtype	Headline and Description
		Issue 2: This is for S32M27X platform, NMI flag is never cleared in WKPU (it should be done by RTD side) Issue 3: This is for S32M27X platform, NMI can be only edge sensitive. This causes problem as, we only read fault status once. In case another fault happens during handling of initial fault, this new fault is not handled. There has to be logic done at the end of fault processing, to read back Fault/Event status and if anything is pending to call again AEC_IRQEventFaultHandler(); Issue 4: Current implementation uses Lpspi_Ip_Cancel function in MNI. This fixes problems with SPI, but creates new one. Previous interrupted communication is not aware of this problem, and LPSPI timeout occurs. But due to this, interrupt for handling of AE faults is postponed for this timeout interval (default is 50ms). Please fix it, so if Lpspi_Ip_Cancel is called, ongoing comm is notified and doesnt get stuck in that timeout loop. Issue 5: Reading of Faults and Events when injected through IRQ_SET register is not working properly. Faults/Event is recognized, but GHS is checked only for Event, and if not event is pending, fault is not handled. (function AEC_IRQEventFaultHandler)
ARTD-106808	Bug	[GMAC] Failed to run internal loopback on GMAC1 Detailed description (how to reproduce it): Create S32DS from example => Gmac_Ip_InternalLoopback_S32K388 And then update the code The application is OK with GMAC0. But when change GMAC0 to GMAC1 !image-2023-12-26-10-26-54-772.png! Keep other configs as GMAC0. And then press update code. And update the main.c (pls see the attached file). The process can not pass_ _Gmac_Ip_GetTransmitStatus. / Wait for the frame to be transmitted / do { Status = Gmac_Ip_GetTransmitStatus(INST_GMAC_0, 0U, &TxBuffer, &TxInfo); } while (Status == GMAC_STATUS_BUSY); Expected behavior: The program can send and receive the frame. And then run loopback on PHY.
ARTD-106823	Bug	[SAF8X R41 2.0.0] MemAcc: Can't generate when enable multicore type 1 Detailed description (how to reproduce it): Generate fail when enable multicore type 1 Preconditions: enable multicore type 1 Test Case ID (internal TC that caught the defect) optional: MemAcc_TS_090 Observed behavior: !image-2023-12-26-14-29-58-876.png|thumbnail! [...] Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-106969	Bug	[Det] Det error get overwritten Detailed description (how to reproduce it) Det_ErrorId[DET_NO_ECU_CORES] may get overwritten by multiple error report. Preconditions Inject error by call Fee_Read with wrong parameter(BlockNumber, BlockOffset,...). Test Case ID (internal TC that caught the defect) optional: Fee_TC_FCT_1004 Observed behavior: Det_ErrorId[DET_NO_ECU_CORES] may get overwritten by multiple error report and return only last error Expected behavior Det_TestLastReportError return the injected error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: Add support for internal ram log for det module. Structure of ram log should fulfill requirement of fan-out mechanism. (static linked list should be prefered) Det_LastReportError and other function for det_stub which mainly use for testing should be keep the same functionalities
ARTD-107202	Bug	[OS]: redefine ResumeAllInterrupts/SuspendAllInterrupts Detailed description (how to reproduce it): ResumeAllInterrupts & SuspendAllInterrupts already defined in OsIf_Internal.h. Redefined in Os.h. Even though the OS is a stub module, but it's better to fixed it. With GCC, it only report warning, but with GHS, it will report error directly. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: None Expected behavior: None Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-107325	Bug	[ETH] Wrong range in MainFunction loop Detailed description (how to reproduce it): The range of the loop that goes through all controllers in the MainFunction is wrong Preconditions: More than 1 controller is configured, and there are different numbers of controllers configured in different variants Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The loop may loop through unconfigured controllers Expected behavior: The loop should only go through configured controllers Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change upper limit of the loop in MainFunction to use the number of configured controllers for that specific configuration !image-2024-01-03-09-35-59-902.png!
ARTD-107489	Bug	[S32K3_S32M27x 4.0.0 P11] Eep: Missing K328, K338, K348 derivatives in file sdk_manifest_eep.xml and do not using common header file S32K358_USDHC.h for K3X8 Detailed description (how to reproduce it): Missing K328, K338, K348 derivatives in file sdk_manifest_eep.xml. Do not using common header file S32K358_USDHC.h for K3X8 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Eep_TC_COT_0001 Observed behavior: NA Expected behavior: Add K328, K338, K348 derivatives in file sdk_manifest_eep.xml. using common header file S32K358_USDHC.h for K3X8 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add K328, K338, K348 derivatives in file sdk_manifest_eep.xml.

ID	Subtype	Headline and Description
		using common header file S32K358_USDHC.h for K3X8
ARTD-107595	Bug	[ADC] DSPSS output threshold parameter has wrong lower limit value DSPSS output threshold parameter has wrong lower limit value. The current version of the drivers has the limits for the OutputThreshold parameter set to: Min:2 down-sampling factor Max: ≤ half of output buffer size The actual limits should be following: Min: 2 Max: ≤ half of output buffer size The current limit does not prevent the CFSDADC FW from correct functionality. But it does decrease the flexibility of processed data transfer from the CFSDADC FW to the host application memory.
ARTD-107788	Bug	[crc] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107809	Bug	[dio] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated.

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107833	Bug	[i2s] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107842	Bug	[mcl] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from:

ID	Subtype	Headline and Description
		# When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=484,height=405! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107857	Bug	[port] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107866	Bug	[sent] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references

ID	Subtype	Headline and Description
		Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107875	Bug	[spi] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif

ID	Subtype	Headline and Description
ARTD-107878	Bug	[uart] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107896	Bug	[ae] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4:

ID	Subtype	Headline and Description
		ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107899	Bug	[CanTrcv] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107902	Bug	[dpga] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11:

ID	Subtype	Headline and Description
		ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-107923	Bug	[LinTrcv] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-108781	Bug	[pwm][S32K3XX] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated.

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-109044	Bug	[S32K3] Support K3 derivatives has 4 bit MSCR[SSS] Detailed description (how to reproduce it): In Port_lpw.c using this macro SIUL2_MSCR_SSS_U32 with define 3 bit mask: #define SIUL2_MSCR_SSS_U32 ((uint32)0x00000007U) But it should be 4bit mask in S32K396: !image-2024-01-17-14-34-09-589.png|width=477,height=135! Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: S32K396 has MSCR[SSS] 4bit Expected behavior: Support MSCR[SSS] both for S32K396 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-109108	Bug	[LIN]: Lin driver not enable overrun interrupt in LPUART instance Detailed description (how to reproduce it): Lin driver doesn't enable overrun interrupt (CTRL[ORIE]) in LPUART instances Preconditions: Lin driver doesn't report overrun error, some bits misbehave when an overrun error occurs Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Lin driver not enable overrun interrupt (CTRL[ORIE]) in LPUART instances Expected behavior: Enable overrunt interrupt in LPUART instances Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-109118	Bug	[platform] Remove adhoc CCOPT values and use generated values based on resource Detailed description (how to reproduce it): Remove custom CCOPT and use generated values based on resource used see [PR comment|https://bitbucket.sw.nxp.com/projects/ARTD/repos/platform/pull-requests/751/overview?commentId=2165839] Remove the mentions from UM/IM as well Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior:

ID	Subtype	Headline and Description
		Custom CCOPT are requested to be used by customer to build the code for a specific NPI these values should be generated based on configuration and not forced in CCOPT in makefiles Expected behavior: Use generated values Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-109666	New Feature	[SPI][DSPI IP][Implementation] CONT_SCKE, FAST PCS Task for activating and testing continuous SCK, bit CONT_SCKE should be set. Output: Measurements before and after of throughput with logical analyzer/oscilloscope Estimation of changes to have this feature in SW design update code update dev testing documentation update traceability
ARTD-109740	Bug	[Mem_43_INFLS]: The flash driver unlocks the wrong register for the special area Detailed description (how to reproduce it): When unlock the last sector of the block 3, the flash low level driver will set the wrong register bit. In theory, the last sector of the block 3, it should clear the MSB in register PFCBLK_SPELOCK[3], but in current implementation, it will clear the PFCBLKU_SPELOCK[4]. After analysis, it seems caused by the inappropriate max sector number. the sector number equal 527, but the max virtual sector also defined as 527, then it will execute the wrong branch in the low level driver. !image-2024-01-23-14-47-12-350.png! !image-2024-01-23-14-47-17-173.png! !image-2024-01-23-14-47-25-783.png! Preconditions: Erase/Write the last sector of block 3 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: clear the wrong register bit Expected behavior: clear the corresponding bit according to the address Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: chech the max virtal number
ARTD-110125	New Feature	[MCU] Support new bit field CTRL[ALC_D] for FXOSC NewWorkDescription: Custoemr request Support new bit field CTRL[ALC_D] for FXOSC in MCU module. Requirement source: [ASR SWS] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-110362	New Feature	S32K3 Synchronizing flash read/write access between HSE and application Core NewWorkDescription: Customer Joynext use S32K358 to develop Commod project for VW. This project is based on NXP RTD and HSE FW. Due to recent ECC issue in HSE, this maybe caused by S32K3 Synchronizing flash read/write access between HSE and application Core. We suggest custoemr need to follow 14.6.5 Synchronizing flash read/write access between HSE and application core chapter in RM758222-HSE-B Firmware Reference Manual V2.2.pdf. But from customer's opinion, They think this synchronization should be deal with in related RTD drivers. In fact, this is some reasonable from customer view due to HSE and RTD are both provided from NXP. Would you please help check whether can integrate this Synchronizing flash read/write access between HSE and application core feature into RTD driver?

ID	Subtype	Headline and Description
		thanks best wishes Mike Cao Requirement source: ASR SWS (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
ARTD-110490	Bug	[ETH][GMAC] Compare the difference in gen code between EB and CT Driver tag: PVT_ETH_STRX_RTM_200_024 Test tag: PVT_TEST_ETH_ARTD_SAF_200_QP_V06 TS ID: Eth_TS_042, Eth_TS_204, Eth_TS_004 (Run with *VV_COMPARE_CODE_GEN=ON) Update code to fix the difference in gen code between eb and ct. !image-2024-01-29-15-34-40-319.png! !image-2024-01-29-15-34-58-767.png! !image-2024-01-29-15-35-34-118.png!!image-2024-01-29-15-35-13-658.png! !image-2024-01-29-15-35-56-005.png! !image-2024-01-29-15-36-13-711.png!!image-2024-01-29-15-36-24-637.png!!image-2024-01-29-15-35-25-040.png!
ARTD-110516	Bug	[BASE] OsIf_GetElapsed() Function error when run with the SysTick interrupts of FreeRtos Detailed description (how to reproduce it): OsIf_GetElapsed() function when running with FreeRtos. xPortStartScheduler() of FreeRtos will allway initialize SysTick() with freertos's own interrupt. !image-2024-01-29-15-51-25-885.png! !image-2024-01-29-15-51-39-316.png! !image-2024-01-29-15-52-56-809.png! !image-2024-01-29-15-53-12-184.png! !image-2024-01-29-15-53-19-010.png! Osif functions of base driver RTD consider SysTick to run continuously from the max value 0xFFFFFFFF > 0 before reloading and not use interrupt TICKINT=0. When OsIf runs with FreeRtos, when init it will not re-init the sys_tick, but will still follow the FreeRtos configuration and use interrupt TICKINT=1. If I change value Register 0xE000E010 follow base driver RTD it run successful. If still keep follow the FreeRtos configuration it run fail. Preconditions: s32ds 3.5.8 S32K3XX_RTD_4_7_RTM_4_0_0_DS_updatesite_D231127.zip Test Case ID (internal TC that caught the defect) optional: Base_TC_FCT_1002.c Platform_Base_Bundle_TC_OsIfGetElapsed.c Observed behavior: Failed to run OsIf_GetElapsed() function with Freertos. Expected behavior: Base driver should support run with Freertos when use interrupt systick TICKINT=1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: OsIf_Timer_System_Internal_Systick.c !image-2024-02-22-09-47-31-288.png! !image-2024-02-22-09-48-10-760.png!

ID	Subtype	Headline and Description
ARTD-110590	Bug	[MCU]The 3 rd. core can not boot by the Mcal Driver on S32K338 Detailed description (how to reproduce it): [This issue is detected on S32K338, when user integrated the RTD driver. The CM_7_0 boot through IVT 'boot header', and I use the MCU function 'Power_Ip_MC_ME_ConfigureCore' to boot the CM_7_1/CM_7_2. The CM_7_2 can not boot normally. After debugging the code, I found that the RTE error "POWER_IP_REPORT_TIMEOUT_ERROR" was triggered when the CM_7_2 was enabled through PRTN0_CORE4_PCONF[CCE] as following picture. !image-2024-01-30-14-21-42-139.png|width=1071,height=494! After the valid KEY combinations are written onto the CTL_KEY register, until timer expired the status of PRTN0_CORE4_STAT[CCS] was always that the clock is inactive as following picture. !image-2024-01-30-14-24-00-158.png|width=1010,height=469!] Preconditions: [# A 3-core software project with Mcal Driver base on RTD 3.0.0 P07 for S32K338 # Hardware Board: S32K3X8EVB-Q289] Test Case ID (internal TC that caught the defect) optional: [None] Observed behavior: [The CM_7_2 can not boot normally] Expected behavior: [The CM_7_2 can boot successfully.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [According to testing results, I found that a timeout period need to be inserted when the clock status of CM_7_1 is active as blew picture. !image-2024-04-29-15-35-13-377.png! This is just a workaround. The root cause need to be explained from RTD SW team.]
ARTD-110635	New Feature	[IMPLEMENTATION] [ADC] Add async mode support for Adc_Calibrate Context: The Adc_Calibrate() API will take 10.5ms per ADC instance, and 21ms for two ADC instances, which will add 21ms to the bootup time. Customers want to reduce bootup {*}time{*}. They tried to configure the NRSMPL bit of the SMR register, but we can't guarantee the accuracy of this way, because we have checked with the HW team, and we don't have some test data under this configuration. Idea: From the code of {_}Adc_Sar_Ip_DoCalibration(){_}, the while() loop that polls the CALBISTREG takes about 10ms per instance to wait for the calibration to complete. Customer wants to add async mode support. Asynchronous support means moving this polling loop to another API, then customer code can call the "another API" after 10ms to check if ADC calibration is complete. Avoid the M7 core being busy waiting for this 10ms to reduce the bootup time. Question: Customer wants to know whether API Adc_Calibrate() supports asynchronous mode, will it be feasible?
ARTD-110643	Bug	[I2s]Polling transfer type not working on Flexio Detailed description (how to reproduce it): I2S Flexio2Flexio communication with polling Preconditions: Flexio master send data to flexio sllave

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: TS0102 Observed behavior: DevAssert on channel validation Expected behavior: No DevAssert Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Replace (uint8)Master->FlexioCommon.ResourceIndex/2U with [(uint8)Master->FlexioCommon.ResourceCount/2U
ARTD-111286	Bug	S32K3 RTD FLASH Driver generates a fault when used with the HSE Detailed description (how to reproduce it): If a service is called when the HSE is doing Flash operations it will block the access to the application cores to that specific block of Flash and trying to operate over that Flash block will result on getting a Fault on the accessing application core. If a writing FLASH operation is done over the indicated flash block that is being modified/used by the HSE the result ends up in a Fault generated on the environment. It is required to poll for the HSE GPR (0x4039C028) for the corresponding bits indicating that the application core can or can't access specific Flash Blocks. !image-2024-02-07-11-52-29-553.png|width=400,height=438! Preconditions: Request an HSE service that operates over Flash such as Key Provisioning. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The application core goes into Fault error when trying to do a memory writing after calling an HSE Service. Expected behavior: The application core should wait until the corresponding flags are cleared and proceed with the desired operation. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Include a verification over the HSE GPR to verify that the desired operation is possible to be done without any restriction or possible fault to happen.
ARTD-111329	Bug	[icu] Wkpu_Ip_GetInputState seems incorrectly implemented Hello, The function Wkpu_Ip_GetInputState (Wkpu_Ip.c) seems to be incorrectly implemented. In the image attached, according to the variable name, it seems that it was supposed to read the register IRER in line 837, but it is reading the WRER instead. Then the read WRER value is compared against 0x0u which doesn't seem to make sense. !https://community.nxp.com/t5/image/serverpage/image-id/261947i87D1F707374E11D3/image-size/medium?v=v2&px=400! Shouldn't the correct implementation at line 837 be: u32regWkpuIRER = base->IRER & channelMask; ? With the current implementation the wakeups are not correctly reported by the function. The if condition in line838 {color}{color:#000000}is expecting the WRER to be 0, but a configured wakeup will have a 1 in the corresponding bit position instead. Info regarding the RTD version (for S32K324): Project : RTD AUTOSAR 4.7 Platform : CORTEXM Peripheral : Emios Siul2 Wkpu LpCmp Dependencies : none Autosar Version : 4.7.0 Autosar Revision : ASR_REL_4_7_REV_0000

ID	Subtype	Headline and Description
		Autosar Conf.Variant : SW Version : 3.0.0 Build Version : S32K3_RTD_3_0_0_P07_D2306_ASR_REL_4_7_REV_0000_20230629
ARTD-111453	Bug	[Base] Incorrect SuspendInterrupts abstraction over FreeRTOS Detailed description (how to reproduce it): Create a S32DS project that also integrates FreeRTOS. Add a periodic interrupt in the GPT. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Upon suspending all interrupts within a GPT ISR, with OsIf_SuspendAllInterrupts, from OsIf_Internal.h, when using FreeRTOS, will call taskEXIT_CRITICAL(), which will result in an assertion failure, since the function is not meant to be called from an ISR context. Expected behavior: Successfully suspend interrupts Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The OsIf should rather call taskEXIT_CRITICAL_FROM_ISR(), when in an interrupt context Some more information from FreeRTOS forum: https://forums.freertos.org/t/why-vportentercritical-is-not-safe-called-from-an-interrupt-context/12912/4
ARTD-111511	Bug	[UM][IM] Correct input.json file for each specific platform. Detailed description (how to reproduce it): input.json is wrongly completed only for S32R !screenshot-1.png! Preconditions: Generation of manuals. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: See detailed description. Expected behavior: Generate correct manuals. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Correct input.json with the name of each corresponding platform name.
ARTD-111578	Bug	[Spi][S32K3XX_S32M27X] Fix differences between code generated by EB and DS Detailed description (how to reproduce it): There are differences between code generated by EB and DS. For K396: 1> Reference links for all test reports on AF: [http://iridum.ea.freescale.net/1/project/ar_go_compare_code_gen_spi_ci/details] [http://iridum.ea.freescale.net/1/project/ar_go_compare_code_gen_1_spi_ci/details|http://iridum.ea.freescale.net/1/project/ar_go_compare_code_gen_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://iridum.ea.freescale.net/1/project/fileexplorer/ZTpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] 2> Ref links for detailed excel report:_ _(points to the "[ar_go_compare_code_gen_spi_ci]/ {_} [ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "{_}{_}build{_}{_}" folder){_} [http://iridum.ea.freescale.net/1/project/fileexplorer/ZTpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] For K344: 1> Reference links for all test reports on AF:

ID	Subtype	Headline and Description
		[http://flores.ea.freescale.net/1/project/ar_go_compare_code_gen_spi_ci/details] [http://flores.ea.freescale.net/1/project/ar_go_compare_code_gen_1_spi_ci/details|http://flores.ea.freescale.net/1/project/ar_go_compare_code_gen_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://flores.ea.freescale.net/1/project/fileexplorer/ZTpcbG9jYWxfMDBcb3V0cHV0XHByb2plY3Rz] 2> Ref links for detailed excel report: (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "build" folder){_} [http://flores.ea.freescale.net/1/project/fileexplorer/ZTpcbG9jYWxfMDBcb3V0cHV0XHByb2plY3Rz] For K342: 1> Reference links for all test reports on AF: [http://laptev.ea.freescale.net/1/project/ar_go_compare_code_gen_spi_ci/details] [http://laptev.ea.freescale.net/1/project/ar_go_compare_code_gen_1_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://laptev.ea.freescale.net/1/project/fileexplorer/ZTpcbG9jYWxfMDBcb3V0cHV0XHByb2plY3Rz] 2> Ref links for detailed excel report:_ _(points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "build" folder){_} [http://laptev.ea.freescale.net/1/project/fileexplorer/ZTpcbG9jYWxfMDBcb3V0cHV0XHByb2plY3Rz] For K358: 1> Reference links for all test reports on AF: [http://zcz01-3157.ea.freescale.net/0/project/ar_go_compare_code_gen_spi_ci/details] [http://zcz01-3157.ea.freescale.net/0/project/ar_go_compare_code_gen_1_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://zcz01-3157.ea.freescale.net/0/project/fileexplorer/ZTpcbG9jYWxfMDBcb3V0cHV0XHByb2plY3Rz] 2> Ref links for detailed excel report: (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "build" folder){_} [http://zcz01-3157.ea.freescale.net/0/project/fileexplorer/ZTpcbG9jYWxfMDBcb3V0cHV0XHByb2plY3Rz] For M276: 1> Reference links for all test reports on AF: [http://zcz01-3163.ea.freescale.net/0/project/ar_go_compare_code_gen_spi_ci/details] [http://zcz01-3163.ea.freescale.net/0/project/ar_go_compare_code_gen_1_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://zcz01-3163.ea.freescale.net/0/project/fileexplorer/ZDpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] 2> Ref links for detailed excel report: (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "build" folder){_} [http://zcz01-3163.ea.freescale.net/0/project/fileexplorer/ZDpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] For K311: 1> Reference links for all test reports on AF: [http://zcz01-3159.ea.freescale.net/0/project/ar_go_compare_code_gen_spi_ci/details] [http://zcz01-3159.ea.freescale.net/0/project/ar_go_compare_code_gen_1_spi_ci/details|http://zcz01-3159.ea.freescale.net/0/project/ar_go_compare_code_gen_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://zcz01-3159.ea.freescale.net/0/project/fileexplorer/RTpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz|http://laptev.ea.freescale.net/1/project/fileexplorer/ZTpcbG9jYWxfMDBcb3V0cHV0XHByb2plY3RzXGFyX2dvX2NvbXBhcmVfY29kZV9nZW5fc3BpX2NpXHRhcmdldA==]

ID	Subtype	Headline and Description
		2> Ref links for detailed excel report:_ _(points to the "[ar_go_compare_code_gen_spi_ci]/ {_} [ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "build" folder){_} [http://zcz01-3159.ea.freescale.net/0/project/fileexplorer/RTpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] For K388: 1> Reference links for all test reports on AF: [http://10.171.89.149/0/project/ar_go_compare_code_gen_spi_ci/details] [http://10.171.89.149/0/project/ar_go_compare_code_gen_1_spi_ci/details|http://10.171.89.149/0/project/ ar_go_compare_code_gen_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://10.171.89.149/0/project/fileexplorer/ZDpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] 2> Ref links for detailed excel report:_ _(points to the "[ar_go_compare_code_gen_spi_ci]/ {_} [ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "build" folder){_} [http://10.171.89.149/0/project/fileexplorer/ZDpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] For K312: 1> Reference links for all test reports on AF: [http://celtic.ea.freescale.net/2/project/ar_go_compare_code_gen_spi_ci/details] [http://celtic.ea.freescale.net/2/project/ar_go_compare_code_gen_1_spi_ci/details|http://celtic.ea.freescale.net/2/project/ ar_go_compare_code_gen_spi_ci/details] or (points to the "[ar_go_compare_code_gen_spi_ci]/ {_}[ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "test-results" folder){_} [http://celtic.ea.freescale.net/2/project/fileexplorer/ZTpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] 2> Ref links for detailed excel report:_ _(points to the "[ar_go_compare_code_gen_spi_ci]/ {_} [ar_go_compare_code_gen_1_spi_ci]"{_}{_}-> "target" > "build" folder){_} [http://celtic.ea.freescale.net/2/project/fileexplorer/ZTpcbG9jYWxfMDFcb3V0cHV0XHByb2plY3Rz] Reference steps: (eg: [Spi_TS_001_cfgPB_CORE0 for K396|http://zcz01-3158.ea.freescale.net/0/project/fileexplorer/ RDpcbG9jYWxfMDBcb3V0cHV0XGFydGlmYWN0c1xhcl9nb19jb21wYXJlX2NvZGVfZ2VuX3NwaV9jaVwyMDI0MDcxODExMTIxOTIzOTAwMFx0YXJnZ 1. Points to the debug* folder: !image-2024-07-19-10-00-49-872.png! 2. For total excel report: points to the compare_include* and *compare_src* folders !image-2024-07-19-10-02-23-702.png! 3. For detailed excel reports: points to the compare_log* * *folder > include* folder and *src* folder !image-2024-07-19-10-03-26-939.png! !image-2024-07-19-10-04-27-962.png! The files do not match as shown below: !image-2024-07-19-10-06-41-487.png! !image-2024-07-19-10-13-19-361.png! !image-2024-07-19-10-15-26-862.png! !image-2024-07-19-10-17-24-137.png! !image-2024-07-19-10-20-46-088.png! !image-2024-07-19-10-26-24-459.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: All tests in class [ar_go_compare_code_gen_spi_ci] with derivative: S32K396 Spi_TS_003 Spi_TS_006 Spi_TS_007 Spi_TS_008 Spi_TS_101 Spi_TS_102

ID	Subtype	Headline and Description
		Spi_TS_103 Spi_TS_1031 Spi_TS_104 Spi_TS_105 Spi_TS_106 Spi_TS_107 Spi_TS_113 Spi_TS_115 Spi_TS_120 Spi_TS_121 Spi_TS_122 Spi_TS_124 Spi_TS_301 Spi_TS_302 Spi_TS_303 Spi_TS_M03 Spi_TS_M08 Spi_TS_Cot_001 Spi_TS_Feature_Compile Spi_TS_D01 Spi_TS_109 Spi_TS_MUL_106 Observed behavior: The report failed. Expected behavior: There is no more difference between code generated by EB and DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-111537	Bug	[S32K3-S32M27x][pwm] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/ OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png! Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-112171	Bug	[BASE][S32K3] PUSHR register of S32K39_DSPI should be split into TX FIFO and CMD FIFO according to Reference manual description

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): PUSHR(32bit) register of S32K39_DSPI should be split into TX FIFO(16bit) and CMD FIFO(16bit) according to Reference manual description. Additionally, same IP type on S32ZE also split PUSHR register Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: PUSHR register was not spitted to FIFO.TX and FIFO.CMD Expected behavior: PUSHR register is spitted to FIFO.TX and FIFO.CMD Note:* in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-112248	Bug	[Mcl] No_init variable was put in the VAR_INIT region Detailed description (how to reproduce it): Mcl_au8EmiosLogicToHwInstance[eMIOS_INSTANCE_COUNT] and Mcl_au8FlexioLogicToHwInstance[FLEXIO_INSTANCE_COUNT] are no_init variable but they are put in the VAR_INIT region MCL_START_SEC_VAR_INIT_UNSPECIFIED_NO_CACHEABLE. They should be put in No_init region MCL_START_SEC_VAR_CLEARED_UNSPECIFIED_NO_CACHEABLE !image-2024-02-20-10-46-09-793.png! Preconditions: No_init variable was put in the VAR_INIT region MCL_START_SEC_VAR_INIT_UNSPECIFIED_NO_CACHEABLE. Observed behavior: Variables are in the Incorrect region. Expected behavior: Variables are in the correct region. Follow Coding_NXPDrivers_CompilerAbstraction_MemMap: [https://nxp1.sharepoint.com/:p:/s/Zebra/ETwcdn9fq2lPlKiRHHfyz2IBQ65w7dVyMNpIIFilWboF7A?e=JpRwPbBasic] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Put them in No_init region MCL_START_SEC_VAR_CLEARED_UNSPECIFIED_NO_CACHEABLE
ARTD-112280	Bug	[Startup] The -O3 optimization level causes the MCU to enter in a HardFault at startup I'm using S32DS 3.5 with the SW32K3_S32M27x_RTD_R21-11_4.0.0_D2311_DS_updatesite for S32K3. I built the Dio_example_S32K344(set on FLASH) from your examples library with the O3 optimization level for the compiler: !image-2024-02-20-10-31-16-633.png|width=534,height=317! The application is successfully downloaded onto the target MCU but it enters in a HardFault state in the init_data_bss() function from startup.c file when data is copied from ROM to RAM: !image-2024-02-20-10-37-47-403.png|width=577,height=313!
ARTD-112327	Bug	[PWM][PWM_ETPU] The expected duty value does not match the actual duty value for IPL. Detailed description (how to reproduce it): The expected duty value does not match the actual duty value. I am configuring Etpu_Pwm for the IP layer with Period = 8000U and Duty = 4000U (expect duty=50%). However, after call Etpu_Pwm_Ip_Init function, The measured duty value is only about 12%. !image-2024-02-21-13-46-18-816.png! !image-2024-02-21-10-33-26-504.png|width=436,height=311! I am seeing, in Etpu_Pwm_Ip (on s32ds) , duty has a {*}unit of ticks{*}. !image-2024-02-21-10-40-21-169.png!

ID	Subtype	Headline and Description
		But in the Etpu_Pwm_Ip_Init function, the duty value is processed into calculation !image-2024-02-21-10-46-05-255.png|width=539,height=69! This is only true for HLD tests because the duty value on the HLD layer is configured in percentages (not ticks) (range of duty: 0x0 0x8000; 0x0 :0%, 0x8000 : 100%). If duty has a {*}unit of ticks{*}, I think the duty value written to the Etpu_Ip_WriteU24Param function is the value that can be configured directly (pPwmConfig->u16DutyCycle) without any calculation. Preconditions: Config Etpu_Pwm for IpL Call Ip layer functions that update the duty value Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The expected duty value does not match the actual duty value. Expected behavior: The expected duty value = the actual duty value. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: I have 2 suggestions : # If you leave the duty unit as ticks, the duty value written to the function Etpu_Ip_WriteU24Param must be the value configured directly (on s32ds) (pPwmConfig->u16DutyCycle) without any calculation # If you leave duty as a percentage (range of duty: 0x0 0x8000; 0x0 :0%, 0x8000 : 100%), you need to correct some information to avoid errors on s32ds. !image-2024-02-21-12-26-51-052.png|width=495,height=83!!image-2024-02-21-13-13-48-893.png|width=431,height=117!
ARTD-112353	Bug	[Mem_ExFls][Fls] Update Qspi_Ip_DLLGetSlaveLockStatusA function to correctly return E_OK in case the lock register is not implemented Detailed description (how to reproduce it): Some bits/ registers do not exist in header file as RM: DLLSR for S32K322 target and others File check: \plugins\BaseNXP_TS_T40D34M30I0R0\header\S32K322_QUADSPI.h Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There's no definition of DLLSR register While using S32K322, calling the Qspi_Ip_ControllerInit() function results in an infinite loop. Because the function Qspi_Ip_DLLGetSlaveLockStatusA() or Qspi_Ip_DLLGetLockStatusA() returns “FALSE” forever. Due to missing QuadSPI_DLLSR_SLVA_LOCK_MASK and QuadSPI_DLLSR_DLLA_LOCK_MASK inside S32K322_QUADSPI.h in the folder “\software\PlatformSDK_S32K3\RTD\BaseNXP_TS_T40D34M30I0R0\header\header”, the 2 functions above return FALSE. !https://nxp.file.force.com/servlet/servlet.FileDownload?file=00P2p00004iNohOEAS! Expected behavior: DLLSR definitions existed in S32K322 and other targets Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update <Target>_QUADSPI.h
ARTD-112378	Bug	[MCL] Wrong comment for MISRA 14.4 and 8.6 Detailed description (how to reproduce it): The MISRA violation is wrongly commented !https://jira.sw.nxp.com/secure/temporaryattachment/81839934ff560b8c3f94dafceb9f820d599e6640/temp14433001801685912085_image-2024-02-21-14-24-14-290.png! !https://jira.sw.nxp.com/secure/temporaryattachment/81839934ff560b8c3f94dafceb9f820d599e6640/temp3459599817815330297_image-2024-02-21-14-24-34-555.png! Preconditions: Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Fix MISRA violation
ARTD-112386	Bug	[WDG][MemMap]: Some variables' definition conflict with the section attribute in memmap Detailed description (how to reproduce it): Some variables' definition conflict with the section attribute in memmap. For example,: In the Wdg module. The variable: Wdg_aePreviousMode[] which with a default initial value when definition. but it was located in the .mcal_bss section. This will case compiling error or unexpected binary file content. !image-2024-02-22-09-56-49-054.png! In the Gpt module. The variable: Gpt_Ipw_HwInstanceConfig_PB[] which is a normal variable, but it was located to .mcal_const_cfg section, which means it shouldn't be changed. Variable: Gpt_Ipw_ChannelConfig_PB and Fee_JobScheduleLookupTable also have the similar issue. !image-2024-02-22-09-57-07-701.png! Preconditions: Always Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiling error or unexpected contents in binary file. Expected behavior: Source code should be following the coding rule more strictly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Had a code review carefully for all the module code by each module owner.
ARTD-112522	Bug	[lin] [S32K3_S32M27x] Problem configuring the Lin Frame Timeout Detailed description (how to reproduce it): The response timeout value is wrong, no need to divide by 10 !image-2024-02-22-17-57-08-317.png! Preconditions: The response timeout value is wrong, no need to divide by 10 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The expression to calculate response time contain "{*}div 10{*}" Expected behavior: The expression to calculate response time shouldn't contain "{*}div 10{*}" Note:* in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-112639	Bug	[RM]Rename Pflash MasterProtectionConfig to avoid misra warning in single config Detailed description (how to reproduce it): Misra deviation 5.8 reported for Pflash_MasterProtectionConfig !image-2024-02-23-09-19-16-506.png! Preconditions: Check misra report from previous releases Test Case ID (internal TC that caught the defect) optional: MISRA report Observed behavior: Justification is not correct since for multiple configuration, there is no misra warning.

ID	Subtype	Headline and Description
		!image-2024-02-23-09-49-55-302.png! For single configuration MISRA warning is accurate due to array and member name having same naming !image-2024-02-23-09-18-34-398.png! Expected behavior: Array name should be different from member name in single config Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Rename array to not have conflict
ARTD-112689	Bug	[MCU] Why FlexIO on S32K3XX is driven by AIPS_PLAT_CLK Detailed description (how to reproduce it): Please check if it is a bug in S32K3 Clock tool: FLEXIO0_CLK is driven by AIPS_PLAT_CLK, while it should be CORE_CLK as RM It leads to wrong calculation in FlexIO_I2c IPV when calculating baudrate Version check: RTD S32K3 4.0.0 RM: S32K3XXRM_Rev_5 Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-112700	Bug	[RTE] Compiler warnings Detailed description (how to reproduce it): Compile the RTD with ghs, gcc, diab Preconditions: RTD installed Test Case ID (internal TC that caught the defect) optional: Bundle_TC_001 Observed behavior: Warnings raised at compile time: !image-2024-02-23-16-05-22-700.png! !image-2024-02-23-16-05-53-989.png! !image-2024-02-23-16-06-20-648.png! Expected behavior: No warnings reported Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-112712	Bug	[RTE] Compiler warnings - diab only Detailed description (how to reproduce it): Compile the RTD with DIAB Preconditions: RTD installed

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: Bundle_TC_001 Observed behavior: Warnings raised at compile time see attachement Expected behavior: No warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-112948	Bug	[RTE] Diab Compiler warnings Detailed description (how to reproduce it): Compile the RTD with DIAB Preconditions: RTD installed Test Case ID (internal TC that caught the defect) optional: Bundle_TC_001 Observed behavior: Warnings raised at compile time: !image-2024-02-26-15-32-45-355.png! Expected behavior: No warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-112956	Bug	[SENT]Add Flexio Note in User Manual for debug mode Detailed description (how to reproduce it): Complaint from customer that K388 Sent example does not receive frames correctly about 60% of the time. (See ARTD-105970) Preconditions: Adding breakpoints in the code, breaks the synchronization between Flexio timer and signal. Also Flexio does not stop during debug mode. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Using breakpoints, the Sent driver will interpret the break in the flow as errors. Expected behavior: Add limitation in user manual mentioning that breakpoints will induce calibration/nibble/crc errors and are expected since Flexio timers do not stop during debug. Correct way to debug is to watch in realtime the Error array. Also:_* Add limitation related to first Calibration error reported at startup and reason for it. Proposed solution optional: Update UM with limitation.
ARTD-112976	Bug	[OCOTP][S32K3XX] Fix finding from Safety Assessment for UML design Detailed description (how to reproduce it): There is comment from Safety Assessment for UML design as below: "All HLD APIs and Mem OTP APIs are not depicted. Model functions which are complex say > 5 complexity., else abstract the functionality in the caller flowchart." Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing information as SA's comment in UML design Expected behavior: Add information to UML design as SA's comment

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-113363	Bug	[DPGA] Fix Warning in traceability matrix caused by fix safety Assessment Detailed description (how to reproduce it): warning in the traceability matrix !image-2024-02-28-14-21-08-883.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: warning in the traceability matrix Expected behavior: No warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-113366	Bug	[SPI] SpiCsSelection disabled leads to PCS0 being used as fixed value Detailed description (how to reproduce it): SpiCsSelection needs to be enabled to switch Peripheral chip select. If it is not enabled, PCS0 will be used as fix value For Slave devices this can be confusing as no warning is issued. Preconditions: SpiCsSelection disabled SPICsIdentifier is not PCS0 !image-2024-02-28-09-42-09-853.png! Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: CS is generated with PCS0 value Expected behavior: CS shall be generated with value chosen by user OR Issue warning that SpiCsSelection needs to be enabled Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A Also, GPIO is used, see if CsIdentifier can be greyed out !image-2024-03-01-13-36-48-049.png!
ARTD-113481	Bug	[Platform]The DTCM and ITCM section defined in the Linker file is not correct for S32K338 Detailed description (how to reproduce it): [The DTCM and ITCM sections defined in the Linker File(linker_flash_c0_s32k388.ld and linker_flash_c1_s32k388.ld) are incorrect according to the DTCM and ITCM size in S32K338 memory area. The size of ITCM0 shall be 32KB according to the S32K3xx Reference Manual. !image-2024-02-29-17-00-22-135.png|width=484,height=162! But in "linker_flash_c0_s32k388.ld" file the size of the ITCM section is defined as 64KB. !image-2024-02-29-17-16-16-967.png|width=519,height=390! The size of DTCM0 shall be 64KB according to the S32K3xx Reference Manual. !image-2024-02-29-17-18-07-930.png|width=514,height=128!

ID	Subtype	Headline and Description
		But in "linker_flash_c0_s32k388.ld" file the size of the DTCM section is defined as 128KB. !image-2024-02-29-17-22-35-893.png|width=481,height=358! If the user uses this file, the area in which ITCM/DTCM is initialized will exceed the corresponding range, it will cause an error to be triggered and ITCM/DTCM initialization to fail. For Core1, the same problem also exists in the "linker_flash_c0_s32k388.ld" file.] Preconditions: [None] Test Case ID (internal TC that caught the defect) optional: [None] Observed behavior: [The ITCM/DTCM initialization is failed.] Expected behavior: [The ITCM/DTCM initialization is successfully.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Linker file for Core_0 !image-2024-02-29-17-27-52-690.png|width=522,height=402! Linker file for Core_1 !image-2024-02-29-17-29-37-818.png|width=524,height=410!]
ARTD-113486	Bug	[WDG][S32K3XX] Fix finding from Safety Assessment for UML design Detailed description (how to reproduce it): There is comment from Safety Assessment for UML design as below: "All IRQ handlers per IP (FlexIo, Lpuart etc) like Lpuart_Lin_Ip_IRQHandler is not depicted to handle spurious logic, break detection, wakeup and frame handling" Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing information as SA's comment in UML design Expected behavior: Add information to UML design as SA's comment Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-114173	Bug	[SPI]Fix Misra findings Rule 8.4 on IP Driver code level Detailed description (how to reproduce it): MISRA justifications not used according to agreed deviation on k3 (mainly) and on others platforms. !image-2024-03-06-16-21-34-609.png! Preconditions: Runtime configuration is applicable for post build file where the MISRA deviation can be justified. For other cases they shall be justified. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: MISRA deviation for rule 8.4 applied where should be fixed Expected behavior: MISRA deviations fixed for rule 8.4 in IP files Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: [....]
ARTD-114634	Bug	[ICU] Differences between the EBT and S32CT for the IcuHwInterruptConfigList configuration I am using S32DS 3.5 with SW32K3_S32M27x_RTD_R21-11_4.0.0_D2311 and EB tresos 29.0. I encounter the following issue when trying to configure the IcuHwInterruptConfigList within the ICU component. S32CT configuration: IcueMios: IcueMios_0_Channel_3 IcuChannels: IcuChannel_1 IcuChannelRef: /Icu/Icu/IcuConfigSet/IcueMios_0/IcueMios_0_Channel_3 IcuHwInterruptConfigList: EMIOS_0_CH_3 It is mandatory to enable within the IcuHwInterruptConfigList the eMIOS instance of the already configured ICU channel, otherwise the following warning will be displayed. !image-2024-03-11-15-30-11-099.png|width=507,height=33! !image-2024-03-11-15-29-22-224.png|width=390,height=153! This change will modify the Emios_Icu_Ip_PBcfg.h by updating the interrupt used. !image-2024-03-11-15-36-33-712.png|width=530,height=208! EB tresos configuration: IcueMios: IcueMios_0_Channel_3 IcuChannels: IcuChannel_1 IcuChannelRef: /Icu/Icu/IcuConfigSet/IcueMios_0/IcueMios_0_Channel_3 IcuHwInterruptConfigList: EMIOS_0_CH_3 !image-2024-03-11-15-56-55-903.png|width=597,height=28! The IcuHwInterruptConfigList instances will not modify the Emios_Icu_Ip_PBcfg.h file as well as in the S32CT case and will not affect the interrupt used. The interrupt, alongside the Emios_Icu_Ip_PBcfg.h is modified directly at ICU channel configuration, as shown below. !image-2024-03-11-15-43-06-417.png|width=477,height=211! I was wondering about the use of this IcuHwInterruptConfigList in EB tresos due to as far as I can understand, it has no effect on enabling the interrupt.
ARTD-114652	Bug	[PWM][ETPU] Import test from EB to CT failed Detailed description (how to reproduce it): When I import the test from EB to CT, I see that the ChannelBaseAddress value isn't updated !image-2024-03-11-22-52-07-546.png|width=374,height=231! How to import test from EB to CT : when generating test on EB, it will appear an epc file Then, you go into S32DS, click import and select import ECU !image-2024-03-11-22-58-26-730.png|width=175,height=243!!image-2024-03-11-22-58-59-551.png|width=259,height=185! Select merge and select browse is the path to the epc file !image-2024-03-11-23-00-33-459.png|width=455,height=142! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Import test from eb to ct fail Expected behavior: Import test success Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-114671	Bug	[I2C][FlexIO] FlexIO I2C DMA optimized Mode conflicts with Polling mode Detailed description (how to reproduce it): When a FlexIO I2C channel configuration was enabled with DMA optimized mode, a timeout error occurs in synchronous transmission I2c_SyncTransmit(). The reason is that the wrong Timer status is read in Flexio_I2c_Ip_MasterCheckStatus(). The correct one should look like this (local modified): !image-2024-03-12-10-24-37-247.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: See description
ARTD-114680	Bug	[I2C][FlexIO] Why does FlexIO I2C DMA optimized Mode use Polling method when Size <= 2? In Flexio_I2c_Ip_MasterStartDmaTransfer(), the driver uses Polling mode in case of Size <=2. Why is it implemented by this way? !image-2024-03-12-10-34-07-504.png! There is an issue as described in ARTD-114671. Therefore, customer encountered problem when they used FlexIO I2C to transmit 1/2 bytes data with DMA optimized mode. DMA optimized mode has much stronger reliability than Polling method. Using Polling method in DMA optimized mode was very confused for customer. Polling method has risk that it would be interrupted by ISR. DMA should be used for any number of bytes, including Size <= 2. Another solution is adding OsIf_SuspendAllInterrupts() and OsIf_ResumeAllInterrupts() before and after Polling in case of Size <=2, so that it could not be interrupted.
ARTD-114772	Bug	[Mem_InFls] Mem_JobResultType deviates from AUTOSAR Detailed description (how to reproduce it): the Mem-drivers of the mentioned MCAL. Mem_JobResultType is deviates from AUTOSAR. According to SWS_Mem_10019, there should be e.g. : MEM_43_EXFLS_INCONSISTENT MEM_43_EXFLS_ECC_UNCORRECTED MEM_43_EXFLS_ECC_CORRECTED. But it is defined in the MCAL: MEM_43_EXFLS*_JOB*_INCONSISTENT MEM_43_EXFLS*_JOB*_ECC_UNCORRECTED MEM_43_EXFLS*_JOB*_ECC_CORRECTED. Same is valid for INFLS and EEP Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: the Mem-drivers of the mentioned MCAL. Mem_JobResultType is deviates from AUTOSAR Expected behavior: the Mem-drivers of the mentioned MCAL. Mem_JobResultType follows from AUTOSAR Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-114882	New Feature	[Mem_InFls] S32K3 Flash C40 Driver Add New Feature For Utest Mode In the S32K3 RTD C40_Ip driver, there is API "C40_Ip_ArrayIntegrityCheck" for flash array integrity check and also API for flash margin read. But there are also other test modes such as ECC check, EDC check, Address check, which are important for customer. Is it possible to add such features into C40_Ip driver?

ID	Subtype	Headline and Description
ARTD-115126	Bug	[PWM][PWM_ETPU] Missing ExclusiveArea in function Etpu_Pwm_Ip_UpdateInterruptMode() Detailed description (how to reproduce it): Insert Exclusive Area region into Etpu_Pwm_Ip_UpdateInterruptMode() function due to RMW operation on registers CR and CISR_A/B by calling sub-functions Etpu_Ip_ClearChannelInterruptFlag(), Etpu_Ip_EnableInterrupt() and Etpu_Ip_DisableInterrupt() from Etpu. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Observed behavior:*_ Expected behavior:*_ Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional
ARTD-116430	Bug	[boot_header]: The boot header is wrong for S32K3XX Detailed description (how to reproduce it): The boot header is wrong for S32K358, S32K388, etc. There are only three cores' entry and the XRDC configuration still there, but as we know, xrdc is only used in very old sbaf FW. !image-2024-03-20-17-59-25-681.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: None Observed behavior: System startup failed Expected behavior: adapt a correct boot header for each chip. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-116433	Bug	[SENT]Issue related to Flexio SENT driver with DMA on S32K3 in SPC mode Detailed description (how to reproduce it): The customer can't receive data from sent sensor with Flexio SENT driver and DMA on S32K3. They updated the functions as below to accommodate the SPC pulse. Findings in the SENT driver Flexio_Sent_Ip.c Flexio_Sent_Ip_Ch0Callback(); This is the Callback function when there is a successful DMA transfer This function calls Flexio_Sent_Ip_DmaHandler(x,y); {*}{color:#FF0000}Update 1{color}{*}: in the function Flexio_Sent_Ip_DmaHandler(), the highlighted numbers were originally 3 and 4 in the driver. To accommodate the SPC pulse, incremented these by 1. From what it was observed and understood, the DMA buffer memory was not accommodating the SPC pulse for which a DMA transfer was made and not accounted for. !image-2024-03-20-16-54-56-640.png! {*}{color:#FF0000}Update 2{color}{*}: DMA Initialisation in Flexio Sent {*}Flexio_Sent_Ip_InitDma{*}{*}({*}{*}uint8{*} Instance, uint8 ResourceConfig, const Flexio_Sent_Ip_StateType Receiver); TCD initialization parameter values – highlighted here. Originally 3, now 4 to accommodate SPC pulse. It looks like these parameters need to be updated when we have SPC pulse consideration. !image-2024-03-20-16-57-25-141.png! I attached the SPC SENT pulse and the configuration file of them. Preconditions: as Detailed description Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: SENT SPC has not worked with DMA.

ID	Subtype	Headline and Description
		Expected behavior: SENT SPC driver with DMA should work OK. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Detailed description
ARTD-116694	Bug	[MCU] Driver is not implementing SWS_Mcu_00133 completely Detailed description (how to reproduce it): If McuDevErrorDetect is disabled and Mcu_GetResetReason is called before Mcu_Init Mcu_GetResetReason will not equal MCU_RESET_UNDEFINED !image-2024-03-21-17-52-17-995.png! It does not obey SWS_Mcu_00133 !image-2024-03-21-17-53-25-590.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mcu_TC_FCT_0089 Observed behavior: Driver is not implementing SWS_Mcu_00133 completely Expected behavior: Implement SWS_Mcu_00133 completely and all other requirements related to UNDEFINED results Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Move line #if (MCU_VALIDATE_GLOBAL_CALL == STD_ON) from Mcu_GetResetReason into Mcu_HLDChecksEntry and Mcu_HLDChecksExit !image-2024-03-21-18-03-59-155.png! !image-2024-03-21-18-04-12-829.png!
ARTD-117866	New Feature	[RM] Add option for global RM Init function or separate per each IP at HLD level Original request: Can we consider splitting the RM module to implement different modules separately ? At present, the RM module includes many peripherals, such as XRDC, SEMA42, XBIC, DMA MUX, MSCM, etc. At present, we have encountered some problems when integrating functional safety software, as XRDC is not configured in the boot header yet and it often needs to be initialized earlier. But other modules such as XBIC may need to be initialized later. However, currently these modules are placed within the same RM module, making it difficult to achieve the above requirement by calling the RM-Init function: initializing different modules at different stages. NewWorkDescription: In order to allow for greater flexibility and to cover use case when integrator needs to have a customer order of init, an option in configuration must allow a global init or an init per IP level. Requirement source: FAE, CPRT (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create node "Global RM driver Init" with default value True to allow for same functionality in future releases When option is disabled, in CDD_Rm the init functions must be per IP: RM_XRDC_Init(), RM_SEMA4_Init(), RM_DMAMUX_Init() etc. For similar use case, see Fss_Rem_Pm_IrmInit and Fss_Rem_Pm_InitEscm in [Source of CDD_Fss_Rem_Pm.c fss_rem_pm NXP Bitbucket|https://bitbucket.sw.nxp.com/projects/ARTD/repos/fss_rem_pm/browse/generic/src/CDD_Fss_Rem_Pm.c]
ARTD-117881	Bug	[AE]Rename Base to BaseNXP in EBT and OsIf to BaseNXP in S32CT Detailed description (how to reproduce it): Base module changed from Base to BaseNXP it should be updated on both EB and CT. !image-2024-03-26-14-19-29-096.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: Change Base to BaseNXP

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-117973	Bug	Mem_43_INFLS_IPW_CheckLoadAc - JobBlockSector is wrong Detailed description (how to reproduce it): Fls driver copies the Ac code to SRAM in case it uses the same block as the targeted area to erase. It seem that for the last sector, the calculation will provide the next block as location, which will lead to no copy to SRAM, and sometimes lead to RWW Hardfault. Preconditions: Use last sector of a blcok Test Case ID (internal TC that caught the defect) optional: . Observed behavior: !image-2024-03-26-13-58-17-181.png! Expected behavior: Last sector job should copy the Ac code to RAM. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Don;t increment the JobAddrStart
ARTD-119801	Bug	[pwm] Fix Misra findings Rule 8.4 on IP Driver code level Detailed description (how to reproduce it): MISRA justifications not used according to agreed deviation on k3 (mainly) and on others platforms. Preconditions: Runtime configuration is applicable for post build file where the MISRA deviation can be justified. For other cases they shall be justified. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: MISRA deviation for rule 8.4 applied where should be fixed Expected behavior: MISRA deviations fixed for rule 8.4 in IP files Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-120448	Bug	[SPI] SpiBaudrate limit not correct for S32K388 Detailed description (how to reproduce it): LPSPI2 and LPSPI5 Spibaudrate is limited to 10MHz in configurator, while it should be 20MHz Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Error when setting 20MHz Expected behavior: 20MHz should work, maybe with some warning related to the right pins. There should be a warning but not an error, in my opinion. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-123170	Bug	[BUILD_ENV][BASE] Copyright need to be updated Detailed description (how to reproduce it): There are many warnings on bamboo due to copyright: [bamboo3.sw.nxp.com/download/AU-RTDCIB-BLDCIPLG/build_logs/AU-RTDCIB-BLDCIPLG-42.log|https://bamboo3.sw.nxp.com/download/AU-RTDCIB-BLDCIPLG/build_logs/AU-RTDCIB-BLDCIPLG-42.log] [ERROR] !!!COPYRIGHT Malformed !!! build 03-Apr-2024 17:33:02 [INFO] !image-2024-04-03-22-19-12-203.png|width=662,height=113!

ID	Subtype	Headline and Description
		!image-2024-04-03-22-20-09-472.png|width=659,height=83! Consider fixing on develop branch for all platforms both build env and base Boards Affected has been updated.{color}{*}{*} {_}*Preconditions:*{_}{*}{{*}} Test Case ID (internal TC that caught the defect) optional: {_}*Observed behavior:*{_}{*}{{*}} Expected behavior Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In build env/config_tpb.mak: COPYRIGHTED_TO="NXP Semiconductors" should be changed to COPYRIGHTED_TO="NXP" In base: Add copyright to header file, check TPB for xml Run locally the copyrighter tool for plugins directory base and another driver (platform, gpt) to detect if some files were missed. Disregard example folder(s).
ARTD-123302	Bug	[UART] Header file CDD_Uart.h should have #ifndef CDD_UART_H Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Header file CDD_Uart.h has wrong #ifndef UART_H Expected behavior: The macro should be #ifndef CDD_UART_H Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The macro should be #ifndef CDD_UART_H
ARTD-123437	Bug	[Mem_InFls] Update Service ID value [hex]. Detailed description (how to reproduce it): Update Service ID. Bellow is example from the Mem_InFls driver. !image-2024-03-26-08-45-18-122.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-123544	New Feature	[I2C] Add support CPR_RTD_01131.i2c requirement NewWorkDescription: CPR_RTD_01131.i2c: The driver shall document how many FlexIO hardware resources(e.g. timers, shifters) are used per configured instance. Note: This information shall be documented in the driver User Manual. Requirement source:

ID	Subtype	Headline and Description
		CPR_RTD_01131.i2c (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A
ARTD-140458	Bug	Previous IVT configuration still present on new projects Detailed description (how to reproduce it): Whenever you create a new project to use with the RTD, the startup_cm7.s file that configures the IVT still has the previous structure of the IVT where the XRDC configuration is being considered even when that is not mentioned anymore on the new sBAF. This needs to be updated to match the new IVT Fields. There is also a mention in the HSE Reference Manual indicating that the reserved values on the IVT must be filled with 0XFF and instead they are being filled with 0x00. Preconditions: It appears to be present in all of the current RTD releases (BLN_RTD_4.7_S32K3XX_S32M27x_4.0.0_P08) It always happens whenever you select to use the RTD. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong IVT fields are being filled out/defined in the code structure. Expected behavior: The IVT needs to match the new documentation to fulfill the expected structure of the new sBAF. Proposed solution optional: Verify the new HSE FW Reference Manual for the current IVT structure and fix it according to the documentation.
ARTD-123766	Bug	[LIN] Incorrect copyright Detailed description (how to reproduce it): Wrong copyright !image-2024-04-09-15-52-46-479.png! Preconditions: Build plugin on bamboo Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong copyright Expected behavior: Update copyright Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-123793	Bug	[ETH][GMAC] Casting to Gmac_Ip_PayloadType may lead to undefined values Detailed description (how to reproduce it): Casting the payload type to Gmac_Ip_PayloadType may lead to undefined values as the value casted is on 3 bits and Gmac_Ip_PayloadType only defines 4 possible values Preconditions: Gmac_Ip_ReadFrame is called using a valid info pointer and the payload type value does not fit in the values defined by Gmac_Ip_PayloadType Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The cast to the enumeration type will fail See also the MISRA 10.5 reported and incorrectly commented Expected behavior: All possible values shall be casted Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Either define all the possible values for Gmac_Ip_PayloadType or use a different mask
ARTD-124084	Bug	[I2S] Flexio DMA I2s can't trigger next transfer using callback function. Detailed description (how to reproduce it): The Flexio want to trigger next transmission using callback function. But after the end of the first transmission, we can receive anything

ID	Subtype	Headline and Description
		Preconditions: Using Flexio DMA Using callback function Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Flexio I2s can't trigger next transfer using callback function. Expected behavior: Flexio I2s trigger next transfer using callback function and transfer exatly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-124324	New Feature	[CanTrcv] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124347	New Feature	[crypto_ace_ng] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124359	New Feature	[dio] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124362	New Feature	[dpga] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration.

ID	Subtype	Headline and Description
		# Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124398	New Feature	[i2s] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124407	New Feature	[LinTrcv] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124425	New Feature	[mem_ifls] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124458	New Feature	[port] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124485	New Feature	[spi] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69]

ID	Subtype	Headline and Description
		Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-124882	New Feature	[PORT] Missing implement requirement SWS_Port_00043, SWS_Port_00055, SWS_Port_00082 NewWorkDescription: Validation change from review to test case. To check and ensure the implementation for these requirements: SWS_Port_00043 : The function Port_Init shall avoid glitches and spikes on the affected port pins. Hint: make sure the OBE/IBE as the last steps. SWS_Port_00055 : The function Port_Init shall set the port pin output latch to a default level (defined during configuration) before setting the port pin direction to output. SWS_Port_00082 : The PORT Driver module shall not provide the facility to configure pin level inversion. The default value shall be set (i.e. not inverted) Requirement source: SWS_Port_00082, SWS_Port_00055, SWS_Port_00043 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:
ARTD-125328	Bug	[Clock]: the clock configuration tree has a wrong limitation range for some items Detailed description (how to reproduce it): The clock configuration tree has a wrong limitation range for some items: PLLAUX_PHI1. According to the RM, if we configure the clock following Option A+, the PLLAUX_PHI1 for S32K358 should be 25MHz, but in S32CT, it limited to the range from 48MHz to 320MHz. !image-2024-04-19-18-27-02-950.png|thumbnail! !image-2024-04-19-18-27-24-415.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Report error Expected behavior: correct it Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-125538	Bug	[MCL] The EB Tresos Tool generates includes in MCL for disabled components and causes the build to fail I'm using the SW32K3_S32M27x_RTD_R21-11_4.0.0 RTD version. When you uncheck the Enable or Generate checkboxes in EB Tresos for components like UART, LIN, I2C etc., you get the following error: !image-2024-04-19-15-55-47-699.png! In the Flexio_Mcl_Ip_Cfg_Defines.h generated file by the configuration project, in the folder generate/include, the “{_}Flexio_UART_Ip_CfgDefines.h{_}” header is present, although it should not be. In the following screenshot, there is a comparison between the files Flexio_Mcl_Ip_Cfg_Defines.h from both configuration projects, EB Tresos, respectively S32 Configuration Tools: !image-2024-04-19-15-55-54-912.png|width=1007,height=351! In S32 Configuration Tools case, when the UART component is disabled, the “{_}Flexio_UART_Ip_CfgDefines.h”{_} header is not included in the Flexio_Mcl_Ip_Cfg_Defines.h file. In this case, the build of the project is successful.
ARTD-125838	Bug	[S32NZ5X 1.0.0] Fee: FEE_CLUSTER_OVERHEAD macro generated by EB and S32DS mismatch Detailed description (how to reproduce it): # Turn FeeSubAddressAreaRetirement on # Generate code with EBtresos # Take the EPC output files as input for S32DS # Generate code with S32DS # Compare the two generated code Preconditions: FeeSubAddressAreaRetirement turned on. Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Fee_TC_FCT_0705 Observed behavior: The macro on the left was generated by EBtresos, the other by S32DS !image-2024-04-23-14-14-03-870.png|width=982,height=13! Expected behavior: The macros generated by EBtresos and S32DS must have the same value with the same input config files. For example: In the case above, 112 is the correct value. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-125950	Bug	[XRDC]: The parameters defined by the function are different from those declared externally Detailed description (how to reproduce it): The parameters defined by the function: Xrdc_Ip_SetProcessID_Privileged are different from those declared externally. !image-2024-04-24-10-00-08-249.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Obvious conflict error. Expected behavior: Fix Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-134112	Bug	[S32K3xx][Peripherals] Error occurs after using feature "Reset to Processor Defaults" Precondition*: RTD data: S32K3_S32M27x Real-Time Drivers AUTOSAR R21-11 Version 4.0.0 Patch 14 Detailed description (how to reproduce it): 1. Create S32K3xx processor 2. Open Peripherals tool 3. Peripherals > Reset to Processor Defaults > Recommended default state > Reset 4. Check Problems view Observed behavior: 4. Error occurs (See attachments) Expected behavior: 4. No error, No warning. Note*: This issue occurs with all supported environment (Windows, Linux, Mac)
ARTD-126336	Bug	[FEE]: Some variables' definition conflict with the section attribute in memmap Detailed description (how to reproduce it): Some variables' definition conflict with the section attribute in memmap. For example,: In the Wdg module. The variable: Wdg_aePreviousMode[] which with a default initial value when definition. but it was located in the .mcal_bss section. This will case compiling error or unexpected binary file content. !image-2024-02-22-09-56-49-054.png! In the Gpt module. The variable: Gpt_Ipw_HwInstanceConfig_PB[] which is a normal variable, but it was located to .mcal_const_cfg section, which means it shouldn't be changed. Variable: Gpt_Ipw_ChannelConfig_PB and Fee_JobScheduleLookupTable also have the similar issue. !image-2024-02-22-09-57-07-701.png! Preconditions: Always Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiling error or unexpected contents in binary file. Expected behavior: Source code should be following the coding rule more strictly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Had a code review carefully for all the module code by each module owner.

ID	Subtype	Headline and Description
ARTD-126358	Bug	A bug of system tick calculation if the OS is enabled Detailed description (how to reproduce it): Background: Due to Jira ticket ARTD-61688, the maximum value in the OsIf_Timer_System_Internal_GetElapsed() function has been changed from S32_SysTick->RVR to SYSTICK_MAX. It's totally fine if you use OsIfBaremetalType. However, if the customer add the operating system, this change is a bug because SYSTICK_MAX will not be equal to S32_SysTick->RVR. OsIf_Timer_System_Internal_Init() in RTD will not be called(pls check Figure 1), and the value in S32_SysTick->RVR will not be initialized to 0xFFFFFFu, which is equal to SYSTICK_MAX. The maximum value is not a real value as expected. So the value of dif will be affected when using system tick (pls check Figure 2). !image-2024-04-28-10-14-22-947.png|width=571,height=501! !image-2024-04-28-10-19-49-256.png|width=376,height=242! Preconditions: OS is enabled Observed behavior: The calculated dif is greater than the real dif Expected behavior: The maximum value is the actual value from S32_SysTick->RVR instead of SYSTICK_MAX Proposed solution optional: !image-2024-04-30-15-29-12-230.png|width=658,height=256!
ARTD-126556	Bug	[S32NZ5X 1.0.0] Fee: Functional operations failed when enable SubAddressArea Retirement Detailed description (how to reproduce it): # Fee Virtual Page Size is set to 32(maybe other numbers will do as well). # Write page size in Mem_43_Exfls is set equal to Fee Virtual Page Size(32). # Enable SubAddressArea Retirement. Preconditions: As mentioned above. Test Case ID (internal TC that caught the defect) optional: Fee_TC_FCT_0705.c Observed behavior: Fee_eJobResult = MEMIF_JOB_FAILED whenever performs Fee_Init, Fee_Write,... Expected behavior: Fee_eJobResult = MEMIF_JOB_OK; Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Hint: FEE_CLUSTER_OVERHEAD should be calculated so that it is divisible by Write page size or Fee Virtual Page Size
ARTD-127586	Bug	[FEE] EB tool does not give error mesage when config block with size is too large Detailed description (how to reproduce it): EB tool does not give error mesage when config block with size is too large ex: cluster size: 4096 byte block size : 4000 byte => EB must give error message to user Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: EB tool does not give error mesage when config block with size is too large Expected behavior: EB tool will give error mesage to user when config block with size is too large Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-127680	Bug	[MemAcc] Investigate issue on CT config when selecting to use Read Burst Detailed description (how to reproduce it): Issue appears when generating MemAcc_PBcfg.c when MemAccUseReadBurst. The exact error is in the "MemAcc generation error" attachment Preconditions:

ID	Subtype	Headline and Description
		MemAccUseReadBurst is checked in the CT config Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Generation error, see attached picture Expected behavior: No issues Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Investigate and see if this issue can be reproduced.
ARTD-127792	Bug	[S32N5 1.0.0] MEM_EXFLS: Compare generated code between EB and DS is not same when inport EB to DS Detailed description (how to reproduce it): MEM_EXFLS: Compare generated code between EB and DS is not same when inport EB to DS. Detail see the picture below. !image-2024-05-16-17-01-58-316.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compare generated code between EB and DS is not same when inport EB to DS. Expected behavior: Compare generated code between EB and DS is same when inport EB to DS. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-127916	Bug	[BLN_RTD_4.7_S32K3XX_S32M27x_4.0.0]Program arm-none-eabi not found in Path and invalid project path when import Examples Detailed description (how to reproduce it): 1. Import any S32M276 RTD Examples, ex: Ae_Handler_Faults_Example_DS_001_S32M276 CanTrcv_Example_S32M276 Dpga_example_S32M276 .... 2. Observe Problems tab 3. Right-click to project > C / C Build > Settings > Cross Settings > Observe Path Preconditions: ONLY Install RTD of S32M27x DO NOT install RTD of S32K3xx Test Case ID (internal TC that caught the defect) optional: TL30-16461: TL30_00380_01510 Observed behavior: 2. Errors: {color}Program "arm-none-eabi-..." not found in PATH Warnings: Invalid project path 3. Path is $\{S32DS_{color:#ff0000}*K3*{color}_ARM32_GNU_10_2_TOOLCHAIN_DIR} Expected behavior: 2. No errors, warnings 3. It should be $\{S32DS_{color:#ff0000}*M2*{color}_ARM32_GNU_10_2_TOOLCHAIN_DIR} path
ARTD-127925	Bug	[FEE-ASRr21.11] fix violations for Cert-c report Detailed description (how to reproduce it): fix violations for Cert-c report as in excel file Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A

ID	Subtype	Headline and Description
		Observed behavior: violations for Cert-c report as in excel file Expected behavior: no violations for Cert-c report as in excel file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-128104	New Feature	[Mem_43_EXFLS] Compile error on K311 Detailed description (how to reproduce it): Due to Qspi_Ip_Features.h (Mem_43_EXFLS_TS_T40D34M40I0R0\generate_PC\include\Qspi_Ip_Features.h) /*========== INCLUDE FILES 1) system and project includes 2) needed interfaces from external units 3) internal and external interfaces from this unit ==========*/ [!INDENT "0"![!// [!IF "ecu:has('Mem.ExFls.External.Qspi.Header')"![!// #include "[!"ecu:get('Mem.ExFls.External.Qspi.Header')"!]" [!ENDIF!][!// since the feature is not being supported . As per CORTEXM_S32K3XX_s32k311_mqfp100.properties 'Mem.ExFls.External.Qspi.Header' is empty Because of this in file Qspi_Ip_Features.h it is not including anything as shown below : /*========== INCLUDE FILES 1) system and project includes 2) needed interfaces from external units 3) internal and external interfaces from this unit ==========*/ #include "" Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compile error Expected behavior: Compile success Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-128316	Bug	[ZIPWIRE] The hwAccZipwireLfast_ConfigureSIUL function should be removed in drive for S32K396 Detailed description (how to reproduce it): hwAccZipwireLfast_ConfigureSIUL can use both master and slave role(currently the drive only allow use on master role), roles that the user will freely decide so hwAccZipwireLfast_ConfigureSIUL functions will develop by user or tester not the drive. !image-2024-05-22-11-55-24-166.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: All case Observed behavior: As Detailed description Expected behavior: The hwAccZipwireLfast_ConfigureSIUL function should be removed in drive for S32K396 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The hwAccZipwireLfast_ConfigureSIUL function should be removed in drive for S32K396
ARTD-128564	New Feature	[IMPLEMENTATION] [S32K3x8] Configuration property to control PGOOD_POLARITY bit in MCU driver(SetMode func) Please analyze adding support for the PGOOD_POLARITY bit (from DCMRWF2 reg) control through a configuration property in the MCU driver. Based on this value's property the MCU driver may set this bit when a transition to STOP mode is requested (SetMode function).

ID	Subtype	Headline and Description
		This property may be also set in the same way PMIC_PGOOD_HNDSHK_BYP (bypass handshake) is configured (in Mcu_Init). These two properties are tightly coupled.
ARTD-129192	Bug	The contents of modules.h files generated by S32DS and EB are inconsistent Detailed description (how to reproduce it): Customers found that when they used the same configuration to generate files for Dio_Example_S32G399A_M7 in RTD 4.0.2 P08, the content in modules.h generated using EB and using S32DS was inconsistent. The details are shown in the figure below. !image-2024-05-28-15-07-08-740.png|width=563,height=151! Preconditions: Import Dio_Example_S32G399A_M7 into EB and S32DS Test Case ID (internal TC that caught the defect) optional: Observed behavior: USE_DIO_MODULE value is different in EB and S32DS Expected behavior: USE_DIO_MODULE value is the same in EB and S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-129204	Bug	S32K3 UART IDLE callback not implemented Please fix by adding below code. !image-2024-05-28-16-03-29-208.png|thumbnail!
ARTD-129198	Bug	[FEE-ASRr21.11] fix violations for CWE, Misra report Detailed description (how to reproduce it): fix violations for CWE, MISRA report as in excel file Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: violations for Misra, CWE report as in excel file Expected behavior: no violations for Misra, CWE report as in excel file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update code to fix Cert-C violation
ARTD-129297	Bug	[Port] Fix SA Finding: Using invalid direction to set pin direction Detailed description (how to reproduce it): No measure are applied to check invalid parameter "direction" for function Port_SetPinDirection Preconditions: Call Port_SetPinDirection with invalid value (valid value is PORT_PIN_IN = 0, PORT_PIN_OUT = 1, PORT_PIN_INOUT = 2, PORT_PIN_HIGH_Z = 3) Test Case ID (internal TC that caught the defect) optional: None Observed behavior: If the invalid direction passed to Port_SetPinDirection, this function will set the direction as PORT_PIN_HIGH_Z. This is unwanted behavior Expected behavior: If development error detection is enabled, DET must have raise when passed invalid parameter. For example: PORT_E_PARAM_INVALID_DIRECTION reported when calling Port_SetPinDirection(0, PORT_PIN_OUT); Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check the validation of parameter "direction". If invalid, the function must skipped and return without any action
ARTD-130062	New Feature	[S32K3XX_S32M27x_5.0.0] Driver activities for GPT

ID	Subtype	Headline and Description
		Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B7B6532C2-E191-4857-905B-7FB5DBF18A33%7D&file=SW32K3_S32M27x%20RTD%20ASR%20R21-11%204.0.1%20SOW.docx&action=default&mobileredirect=true]
ARTD-130144	New Feature	[S32K3XX_S32M27x_5.0.0] Driver activities for ICU Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B7B6532C2-E191-4857-905B-7FB5DBF18A33%7D&file=SW32K3_S32M27x%20RTD%20ASR%20R21-11%204.0.1%20SOW.docx&action=default&mobileredirect=true]
ARTD-130226	New Feature	[S32K3XX_S32M27x_5.0.0] Driver activities for OCU Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B7B6532C2-E191-4857-905B-7FB5DBF18A33%7D&file=SW32K3_S32M27x%20RTD%20ASR%20R21-11%204.0.1%20SOW.docx&action=default&mobileredirect=true]
ARTD-130267	New Feature	[S32K3XX_S32M27x_5.0.0] Driver activities for PWM Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B7B6532C2-E191-4857-905B-7FB5DBF18A33%7D&file=SW32K3_S32M27x%20RTD%20ASR%20R21-11%204.0.1%20SOW.docx&action=default&mobileredirect=true]
ARTD-131347	Bug	[S32K3XX_S32M27X][Port] S32DS Pins tool generate code incorrectly when add PowerAndGround pins Detailed description (how to reproduce it): 1. Create project in S32DS In Pins tool: 2. Add 1 PowerAndGround pins first 3. Add 1 other peripheral pin (e.g GPIO pin) 4. Generate code !image-2023-11-27-14-59-14-258.png! Step 2 and step 3 MUST follow above order Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Code generate for GPIO pin is incorrect, it becomes NOT AVAILABLE almost attribute: !image-2023-11-27-14-57-47-970.png! Expected behavior: PowerAndGround is routed as default, so it should not be added or affect to other pins if user add it into Pins list Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-131784	New Feature	[wdg] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-131789	Bug	[wdg] Validation of partition reference should be OS version independent Detailed description (how to reproduce it): Some RTD drivers (Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes) have the following check when [drv]MulticoreEnabled = 'true': <a:tst expr="count(text:grep(node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef, .)) = 0" true="The ECUC partition must be defined in OS."/> RTD shall not validate references against a certain OS version. There can be any OS version, either in a Tresos compatible plugin format or not. Creating a dependency to a certain version will cause the following validation error: !https://jira.sw.nxp.com/secure/attachment/1295507/image-2023-11-27-16-04-31-321.png!

ID	Subtype	Headline and Description
		Preconditions: [drv]MulticoreEnabled is set to 'true' and a correct configuration of the partition is done in OS. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: The following drivers Adc, Crc, Dio, Icu, Platform, Port, Pwm, Serdes show validation error is Tresos even when a correct reference to a partition is configured. Expected behavior: No error should be caused if different OSes are used. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Option 1) Change node:refs('ASPathDataOfSchema:/TS_T40D11M40I2R0/Os')/OsApplication/*/OsAppEcucPartitionRef To something like: as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef as found in CAN. Option 2) Alternatively this check can be removed altogether since drivers should not be aware of Os partition configuration. The reason is simple: partition configuration is part of high level components like: EcuM, BSWM and RTE, all above driver level.
ARTD-131854	Bug	[ARTD][GMAC] Gmac_Ip_TxTimeAwareShaperData->GateControlList is NULL after initialization Detailed description (how to reproduce it): On function Gmac_Ip_TxTimeAwareShaperInit, the Gmac_Ip_TxTimeAwareShaperData structure is initialized. The problem is that Gmac_Ip_TxTimeAwareShaperData->GateControlList remains NULL and later in code, it writes something to the 0x0 address (picture attached). This can be fixed by adding the following line, before the for loop (picture attached): Gmac_Ip_TxTimeAwareShaperData[Instance].GateControlList = Config->Gmac_pCtrlTxTimeAwareShaper->GateControlList;* Expected behavior: Gmac_Ip_TxTimeAwareShaperData->GateControlList should point to the correct address from the configuration. Proposed solution optional: Proposal solution inside the Description section.

ARTD-131859	Bug	[ARTD][GMAC] Wrong TimeoutOccured condition inside Gmac_Ip_EnableTimeGateScheduling function
		
		Detailed description (how to reproduce it):
		Inside Gmac_Ip_EnableTimeGateScheduling function, there is a wrong timeout condition (picture attached). This is causing the function to return GMAC_STATUS_ERROR when TimeoutOccurred=False. This is making the Eth_43_GMAC_StartTas to fail.
		
		Possible fix:
		
		if ((TimeoutOccurred ...) \{GMAC_STATUS_ERROR} instead of
		
		if ((!TimeoutOccurred ...) \{GMAC_STATUS_ERROR}
		
		Proposed solution optional:
		See the Detailed description section.

ARTD-131933	New Feature	[IMPLEMENTATION] Comet - Windriver Diab issues with v7.0.4 and update to newer version v.7.0.6 Description:_* Update diab version to 7.0.6 as requested in SOW in section "S32K3_S32M27x 5.0.0 release scope" Verify that nightly build uses and Base test is running with new compiler.

ID	Subtype	Headline and Description
ARTD-131949	New Feature	[gpt] [S32K3_S32M27x 5.0.0] Review the changes for new Reference Manual and Data Sheet new versions NewWorkDescription: Review the changes of Reference manual and Data sheet new version for S32K3_S32M27x 5.0.0 release Requirement source: New RM and DS documents: Reference Manual |S32K3xx Reference Manual, Rev.9, Draft A, 05/2024 || [S32K3xx_RM_Rev9_DraftA.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K3xx/RM/S32K3xx_RM_Rev9_DraftA.pdf?csf=1&web=1&e=A4teVY] S32K39 and S32K37 Reference Manual, Rev. 3, 03/2024 || [S32K39RM_and_S32K37RM_Rev3 1.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K396/RM/S32K39RM_and_S32K37RM_Rev3%201.pdf?csf=1&web=1&e=iPwW98] S32M27x Reference Manual, Rev.3 RC, 04/2024|| [S32M27x_RM_Rev3_RC.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32M27x/RM/S32M27x_RM_Rev3_RC.pdf?csf=1&web=1&e=3IYyb9] Datasheet |S32K39 and S32K37 Data Sheet, Rev.3 — 03/2024 || [S32K39_and_S32K37_DS_Rev.3.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K396/DS/S32K39_and_S32K37_DS_Rev.3.pdf?csf=1&web=1&e=blqIWL] S32K3xx Data Sheet, Rev. 10, Draft A, 03/2024 || [S32K3xx_DS_Rev10_DraftA.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K3xx/DS/S32K3xx_DS_Rev10_DraftA.pdf?csf=1&web=1&e=Q2NJLS] S32M2xx Data Sheet, Rev. 3 RC2 — 10/2023 || [S32M2xx_DS_Rev3_RC2.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32M27x/DS/S32M2xx_DS_Rev3_RC2.pdf?csf=1&web=1&e=RC1odZ] Proposed solution optional: Notes: If a software change needs to be implemented, a new ticket (Bug or New Feature) is raised. The new ticket should be linked to this ticket This ticket shall be closed with resolution "Fixed No Action Taken" after completing the review and raising the necessary implementation tickets, if applicable.
ARTD-131971	New Feature	[rm] [S32K3_S32M27x 5.0.0] Review the changes for new Reference Manual and Data Sheet new versions NewWorkDescription: Review the changes of Reference manual and Data sheet new version for S32K3_S32M27x 5.0.0 release Requirement source: New RM and DS documents: Reference Manual |S32K3xx Reference Manual, Rev.9, Draft A, 05/2024 || [S32K3xx_RM_Rev9_DraftA.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K3xx/RM/S32K3xx_RM_Rev9_DraftA.pdf?csf=1&web=1&e=A4teVY] S32K39 and S32K37 Reference Manual, Rev. 3, 03/2024 || [S32K39RM_and_S32K37RM_Rev3 1.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K396/RM/S32K39RM_and_S32K37RM_Rev3%201.pdf?csf=1&web=1&e=iPwW98] S32M27x Reference Manual, Rev.3 RC, 04/2024|| [S32M27x_RM_Rev3_RC.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32M27x/RM/S32M27x_RM_Rev3_RC.pdf?csf=1&web=1&e=3IYyb9] Datasheet |S32K39 and S32K37 Data Sheet, Rev.3 — 03/2024 || [S32K39_and_S32K37_DS_Rev.3.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K396/DS/S32K39_and_S32K37_DS_Rev.3.pdf?csf=1&web=1&e=blqIWL] S32K3xx Data Sheet, Rev. 10, Draft A, 03/2024 || [S32K3xx_DS_Rev10_DraftA.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K3xx/DS/S32K3xx_DS_Rev10_DraftA.pdf?csf=1&web=1&e=Q2NJLS] S32M2xx Data Sheet, Rev. 3 RC2 — 10/2023 || [S32M2xx_DS_Rev3_RC2.pdf|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32M27x/DS/S32M2xx_DS_Rev3_RC2.pdf?csf=1&web=1&e=RC1odZ] Proposed solution optional: Notes: If a software change needs to be implemented, a new ticket (Bug or New Feature) is raised. The new ticket should be linked to this ticket This ticket shall be closed with resolution "Fixed No Action Taken" after completing the review and raising the necessary implementation tickets, if applicable.
ARTD-132005	New Feature	[adc] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176

ID	Subtype	Headline and Description
		{*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132008	New Feature	[base] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132011	New Feature	[can] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132014	New Feature	[crc] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132017	New Feature	[dio] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132023	New Feature	[fee] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396

ID	Subtype	Headline and Description
		Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132026	New Feature	[gpt] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132029	New Feature	[i2c] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132032	New Feature	[i2s] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132035	New Feature	[icu] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176

ID	Subtype	Headline and Description
		s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132038	New Feature	[lin] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132041	New Feature	[mcl] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132044	New Feature	[mcu] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132047	New Feature	[ocu] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132050	New Feature	[platform] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms

ID	Subtype	Headline and Description
		NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132053	New Feature	[port] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132056	New Feature	[pwm] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132059	New Feature	[rm] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132062	New Feature	[sent] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396:

ID	Subtype	Headline and Description
		s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132065	New Feature	[spi] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132068	New Feature	[uart] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132071	New Feature	[wdg] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132077	New Feature	[ae] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket

ID	Subtype	Headline and Description
ARTD-132086	New Feature	[mem_infls] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132089	New Feature	[mem_exfls] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132095	New Feature	[mem_eep] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132098	New Feature	[gdu] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132104	New Feature	[otp] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR)

ID	Subtype	Headline and Description
		Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132107	New Feature	[resource] [S32K3_S32M27x 5.0.0]_Add support S32K364 and S32K366 Phantoms NewWorkDescription: Add support S32K364 and S32K366 phantom of S32K396 Requirement source: According to Change Request: AAI-2144 Add S32K364 and S32K366 Phantoms (more details please refer this CR) Proposed solution optional: Add following resources to support those phantoms of S32K396: s32k364_mapbga289, s32k364_lqfp176 s32k366_mapbga289, s32k366_lqfp176 {*}Note{*}: S32K364 and S32K366 are cut down versions of S32K396. If the features present are unclear, please reach out for clarification. HW/APP engineer contact point can be found in AAI-2144 ticket
ARTD-132389	New Feature	[WDG] Improve to use IP_SWT_BASE_PTRS array in Swt_Ip.c to avoid branching when have new platform NewWorkDescription: Now in Swt_ip.c we are using the define SWT_IP_DISCOUNTINUOUS_INSTANCE_IDS to detect if the instances are discontinuous !image-2023-12-14-16-44-40-725.png! But incase we have new platform also have the instances are discontinuous the solution above may not work (example saf86 have two instance : swt0 and swt3) so this solution will not work for saf86 so we need to create a new define into Swt_Ip_Cfg_Defines.h to define the base address array. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-132628	Bug	[ETH] S32K388 GMAC1 xMII mode and RGMII Tx loopback not correctly initialized Detailed description (how to reproduce it): Eth_43_GMAC_Ipw_SelectPhyInterface() incorrectly configures S32K388 GMAC1 xMII mode and RGMII TX clock loopback. Moreover, it rewrites xMII configuration of GMAC0. Preconditions: Multiple Ethernet controllers configured on S32K388. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: GMAC1 xMII mode is incorrectly written into DCMRWF1[MAC_CONF_SEL]. GMAC1 RGMII TX clock loopback is is incorrectly enabled by setting DCMRWF1[MAC_TX_RMII_CLK_LPBCK_EN]. Expected behavior: GMAC1 xMII mode is written into DCMRWF4[MAC2_CONF_SEL]. GMAC1 RGMII TX clock loopback is enabled by setting DCMRWF2[MAC2_LOOBPACK_CLK_SEL] and DCMRWF2[MAC2_TX_RMII_CLK_LPBCK_EN]. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: As per expected behavior section.
ARTD-132710	Bug	[Base] Wrong inclusion of MemAcc_GeneralTypes.h In memory drivers the file MemAcc_GeneralTypes.h is included for E_MEM_SERVICE_NOT_AVAIL but as per AUTOSAR R21-11, MCAL should not include MemAcc_GeneralTypes.h, the define of macro should come from Std_Types.h
ARTD-132721	Bug	[S32K3 4.0.0][Mem_InFls] Wrong inclusion of MemAcc_GeneralTypes.h In memory drivers the file MemAcc_GeneralTypes.h is included for E_MEM_SERVICE_NOT_AVAIL but as per AUTOSAR R21-11, MCAL should not include MemAcc_GeneralTypes.h, the define of macro should come from Std_Types.h
ARTD-132727	Bug	[S32K3 4.0.0][Mem_Eep] Wrong inclusion of MemAcc_GeneralTypes.h

ID	Subtype	Headline and Description
		In memory drivers the file MemAcc_GeneralTypes.h is included for E_MEM_SERVICE_NOT_AVAIL but as per AUTOSAR R21-11, MCAL should not include MemAcc_GeneralTypes.h, the define of macro should come from Std_Types.h
ARTD-132738	Bug	S32K3 shareable SRAM will not be ECC initialized correctly. Hi RTD team, We found that in the linker_flash_c0_s32k3xx.ld in Platform module, the shareable SRAM area will not be initialized in startup as the linker define the INT_SRAM_END = ORIGIN(ram_end_c0), which will be the input of SRAM loop in startup_cm7.s. Here is the example on S32K322: The variable is defined in linker_flash_c0_s32k322.ld: !image-2024-06-11-17-56-44-449.png! !image-2024-06-11-17-57-05-243.png! The sram loop in startup code will not cover this area: !image-2024-06-11-17-58-41-023.png! This will lead to hard fault every time when application trying to write the shareable area as it is not initialized. !image-2024-06-11-17-56-02-172.png! Could you please fix this in the next version or if you could have some advice on this?
ARTD-132867	New Feature	[platform] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of Oslf_GetCoreID to OslfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-132918	New Feature	[Base] Hardcode ksdk value for S32DS P-SDK NewWorkDescription: Hardcode ksdk version value inside sdk_manifest_base.xml for all available platforms. In order to support backward compatibility with other software products, ksdk version needs to be hardcoded. Other products use this to identify the RTD P-SDK and to extend it with their own drivers/components. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Use the confluence page to find the ksdk version value for the platform. https://confluence.sw.nxp.com/display/AUTORD/Platform+SDK+information+for+RTD+releases
ARTD-133086	New Feature	[Port] Update the error description for funtional group name Detailed description (how to reproduce it): The current error log is causing confusion for users: " Naming of the Functional Group in the Pins Tool should be: PortContainerName_PeripheralFunctionalGroupName. E.g: PortContainer_0_BOARD_InitPeripherals, with PortContainer_0 is the name of the PortContainer 0, BOARD_InitPeripherals is the name of the Peripheral Functional Group " Preconditions: Pins Tools functional group name != Port_Container_Name Port_Variant_Name

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: None Observed behavior: {noformat} description="Naming of the Functional Group in the Pins Tool should be: PortContainerName_PeripheralFunctionalGroupName. E.g: PortContainer_0_BOARD_InitPeripherals, with PortContainer_0 is the name of the PortContainer 0, BOARD_InitPeripherals is the name of the Peripheral Functional Group" {noformat} Expected behavior: make the error log easier to read and understand Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional !chrome-extension://bpggmmljdiliancllaapiggllnkbjocb/logo/48.png!
ARTD-133132	New Feature	[adc] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-133203	Bug	[LIN]Lin Response Timeout Possible Issue Detailed description (how to reproduce it): !image-2024-06-17-14-13-29-985.png! !image-2024-06-17-14-07-11-847.png! !image-2024-06-17-14-07-32-650.png! Preconditions: In the Lpuart_Lin_Ip_PBcfg.c file, the correct fomula should be: [!VAR "LinResponseTimeoutValue" = "ceiling(8*(LinResponseTimeout div 10) 1000000 (1 div $Baudrate))"!] Or the better solution can be: [!VAR "LinResponseTimeoutValue" = "ceiling(10*(LinResponseTimeout div 10) 1000000 (1 div $Baudrate))"!] Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: as Detailed description Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Preconditions
ARTD-133306	New Feature	Support DMA error notification for S32DS NewWorkDescription: Support DMA error feature for S32DS Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-133539	Bug	Flexio UART Baudrate wrong calculation The flexio UART baudrate calculation is wrong. need to change manually. 80000000(flexio clk)/16/119407 != 20 !image-2024-06-19-15-19-09-865.png|thumbnail!
ARTD-133576	New Feature	[SPI][DSPI IP][Implementation] CONT_SCKE Task for activating and testing continuous SCK, bit CONT_SCKE should be set.

ID	Subtype	Headline and Description
		Output: Measurements before and after of throughput with logical analyzer/oscilloscope Estimation of changes to have this feature in SW design update => 1h code update => configuration (2h) aligned with existed code (1h) dev testing => 2h documentation update =>1h (guideline and driver limitation) traceability => 2h
ARTD-133632	New Feature	[I2C] ERR052121: LPI2C: NACK Detect Flag can be set when IGNACK=1 NewWorkDescription: ERR052121: LPI2C: NACK Detect Flag can be set when IGNACK=1 Description The NACK detect flag (MSR[NDF]) can be set even when the Controller Configuration 1 (MCFGR1[IGNACK]=0b1). The LPI2C will not automatically generate a STOP or repeated START if the NACK detect flag (MSR[NDF]=0b1) and the ignore NACK are set (MCFGR1[IGNACK]=0b1). Thus, the transfer will continue as if the (MSR[NDF]) had not been set. The LPI2C will continue to block a new START condition if (MSR[NDF]=0b1). Workaround When (MCFGR1[IGNACK]=0b1), the (MSR[NDF]) must be cleared by software, writing (MSR[NDF]=0b1) to allow new I2C transfers to start. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A
ARTD-133731	Bug	[S32ZSE 2.0.0] MemAcc: multicore type 1 run with data fauld when config with one Mem driver and one channel sema4 Detailed description (how to reproduce it): multicore type 1 detect a data fauld whenrun through the function MemAcc_Init Preconditions: Multicore type 1 Use one Mem IP driver Use one channel sema4 Test Case ID (internal TC that caught the defect) optional: MemAcc_TS_090 Observed behavior: Expected behavior: No error when run multicore Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-133850	New Feature	[ADC] Update SdAdc IPL component NewWorkDescription: update AutosarExt tab, change component from tab view to table view Requirement source: N/A Proposed solution optional: change to look like SarAdc
ARTD-133873	Bug	[MemAcc] Inconsistency between gen tools: EB and S32CT Detailed description (how to reproduce it): some minor differences in generated codes (attached in the ticket) between EB and S32ct: !image-2024-06-23-09-50-29-888.png|thumbnail! Preconditions: Derivative: S32ZSE Multicore Type 1: Enable Multicore Type 3: Enable

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: MemAcc_TS_110 Observed behavior: Expected behavior: Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-133913	Bug	[S32K3] Some S32K3 SIUL2 header files MSCR[SSS] should be 4-bit Detailed description (how to reproduce it): The S32K3xx_RM_Rev9_DraftA.pdf follow SOW S32K3_M27 5.0.0 has MSCR[SSS] is 4bit: !image-2024-06-24-11-24-19-492.png|width=499,height=133! !image-2024-06-24-11-24-58-163.png|width=554,height=176! But the header file of S32K312, 42-41-22, 44-24-14 still 3-bit SSS: !image-2024-06-24-11-27-28-697.png|width=666,height=236! Preconditions: BASE_544 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Some S32K3 header file is 3-bit SSS Expected behavior: Follow S32K3 500 RTM, MSCR[SSS] should be 4-bit Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-134037	Bug	The condition of HW channel in configuration of LIN and UART driver is incorrect Detailed description (how to reproduce it): Case 1: When config channel LPUART_MSC for UART and LIN driver, no error is occurred Case 2: When config channel LPUART_1 for UART driver and LPUART_IP_11 for LIN driver, the error is occurred All of those cases are incorrect. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The error is triggered incorrectly when config HW channel Expected behavior: The error is triggered correctly when config HW channel Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the condition in the configuration code
ARTD-134040	Bug	[DPGA] Build fail due to enable the copyright check Detailed description (how to reproduce it): Build fail when enable the copyright check [https://bamboo3.sw.nxp.com/browse/AU-RTDCICDD-BLDCIPLG-1/log] Preconditions: enable the copyright checking Test Case ID (internal TC that caught the defect) optional: NA

ID	Subtype	Headline and Description
		Observed behavior: Build fail and could not push tag to manifest: !image-2024-04-12-14-41-19-841.png! !image-2024-04-12-14-41-27-406.png! Expected behavior: Build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update copyright for all files
ARTD-134062	Bug	[I2C] Investigate unsafe memory access in Lpi2c Slave DMA mode Issues from Solutions team regarding DMA transfer are described below. More details will be added after investigation Slave DMA reaches the end of the Rx buffer but master didn't finished yet Tx addresses are not well updated and random data are sent Potentially unsafe memory access during DMA transfer. Case 1 (DMA writes outside the Rx buffer if the master sends transfer size larger than Rx buffer): txBuffer[16U] and rxBufferSlave[8U] Lpi2c is configured as a slave using DMA Master writes 16 bytes to the slave, but slave prepares a buffer of 8 bytes. The first 8 bytes received are put in the rxBufferSlave but the remaining 8 are written outside the buffer, in continuation !image-2024-06-27-17-05-46-516.png! Case 2 (DMA reads from different location outside the buffer, with an offset of 0x08): Master requests a transfer of 16 bytes, but the slave prepares a txBuffer2 of 8 bytes First 8 bytes are sent correctly by the Slave, but the next 8 bytes are sent from a different location (i.e. address of last byte sent 0x08) !image-2024-06-27-17-13-09-133.png!
ARTD-134147	Bug	The condition of HW channel in configuration of LIN and UART driver is incorrect Detailed description (how to reproduce it): The condition of HW channel in configuration of LIN and UART driver is incorrect. The HW channel of LIN will report error when same HW channel in UART, but it don't Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The error is triggered incorrectly when config HW channel Expected behavior: The error is triggered correctly when config HW channel Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the condition in the configuration code
ARTD-134194	Bug	[SENT]Apply guideline rules 28, 31, 32, 38, 41, 42, 45 Apply following rules on source code: 28 tab indented 4 spaces 31 lines shall have unix ending format 32 paires of matching braces 38 unary operators shall stick to variable or expression 41 paranthesis shall stick to expression 42 case labels shall be indented on leve from switch 45 function parameters shall be aligned on the same column Guideline: [RTD Coding Guideline|https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20Coding%20Guideline.docx] [RTD UML Design Guideline.pptx|https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20UML%20Design%20Guideline.pptx]
ARTD-134229	Bug	MCU: Type of function "Clock_Ip_GetClockFrequency" not follow Requirement Detailed description (how to reproduce it): According to ReqExport then type of function "{*}Clock_Ip_GetClockFrequency{*}" must be "{*}uint64{*}" but in driver code it is "{*}uint32{*}" !image-2024-06-17-22-42-16-308.png! !image-2024-06-17-22-41-48-814.png!

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update type of function Clock_Ip_GetClockFrequency follow ReqExport
ARTD-134467	Bug	[GPT][MemMap]: Some variables' definition conflict with the section attribute in memmap Detailed description (how to reproduce it): Some variables' definition conflict with the section attribute in memmap. For example,: In the Wdg module. The variable: Wdg_aePreviousMode[] which with a default initial value when definition. but it was located in the .mcal_bss section. This will case compiling error or unexpected binary file content. !image-2024-02-22-09-56-49-054.png! In the Gpt module. The variable: Gpt_Ipw_HwInstanceConfig_PB[] which is a normal variable, but it was located to .mcal_const_cfg section, which means it shouldn't be changed. Variable: Gpt_Ipw_ChannelConfig_PB and Fee_JobScheduleLookupTable also have the similar issue. !image-2024-02-22-09-57-07-701.png! Preconditions: Always Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiling error or unexpected contents in binary file. Expected behavior: Source code should be following the coding rule more strictly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Had a code review carefully for all the module code by each module owner.
ARTD-134638	New Feature	[BASE] Update new header files of S32K3XX according to new RM. NewWorkDescription: Header files of S32K3XX need to be updated according to new RM. Refer the following table mentioned in SOW. !image-2024-07-09-12-06-20-566.png! Requirement source: S32K39 and S32K37 Reference Manual, Rev. 3, 03/202 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update header files
ARTD-134745	New Feature	[S32K3XX][Mem_InFls] Add software semaphores for K3 derivatives without the SEMA4 IP NewWorkDescription: There is no way to sync between the HSE core and application core on S32K3XX platforms that don't have hardware semaphores (see attached picture) Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add Software semaphores support Investigate how these SW semaphores can be assigned in Ram to be also visible for both Fls and Crypto driver
ARTD-134748	New Feature	[S32K3XX][Base] Add software semaphores for K3 derivatives without the SEMA4 IP NewWorkDescription: There is no way to sync between the HSE core and application core on S32K3XX platforms that don't have hardware semaphores (see attached picture) Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: add Multicore support on K310/K311/K312 derivatives that don't have Sema4 support (from resource files) add Software semaphores support on the previously mentioned derivatives. investigate how these SW semaphores can be assigned in Ram to be also visible for the HSE Core.
ARTD-134756	Bug	[i2c] Using the sint8 data type for variables 'I2c_as8ChannelHardwareMap' and 'I2c_as8PartitionHardwareMap' would violate the CertC standard Detailed description (how to reproduce it): Value of array I2c_as8ChannelHardwareMap[Channel] will be used to get element of I2c_aeChannelStatus array. So. it cannot be a negative number

ID	Subtype	Headline and Description
		Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ARTD-134765	Bug	I2C driver needs added protection against potential race conditions
		
		Detailed description (how to reproduce it):
		
		There is the following code in the Lpi2c_Ip_MasterSendDataBlocking:
		
		if(Master->I2cIdle)
		{
		Master->BufferSize = TxSize;
		Master->DataBuffer = TxBuff;
		Master->Direction = LPI2C_IP_SEND;
		Master->SendStop = SendStop;
		Master->I2cIdle = FALSE;
		Master->Status = LPI2C_IP_BUSY_STATUS;
		
		Means, first there is a check if the bus is idle and then it is set to busy. It is possible that a task executes the if clause, but doesn't reach the bus busy setting, yet, because it does get interrupted by another task. That other task could also issue an i2c transfer, happily seeing that the bus is still idle.
		A "test-and-set" mechanisms needs to be implemented to protection against race-conditions, i.e. adding task suspend/resume for atomically checking and setting Master->I2cidle.
		
		Preconditions:
		NA
		
		Test Case ID (internal TC that caught the defect) optional:
		NA
		
		Observed behavior:
		See description
		
		Expected behavior:
		Race conditions should not occur
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		[....]

ARTD-134768	Bug	[I2C] Can not use Lpi2c instace macro when use Lpi2c2 for first channel Detailed description (how to reproduce it): Create a S32DS project and add Lpi2c_Ip component Add Lpi2c2 for first channel Generate code Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_Lpi2c_TS_200 Observed behavior: LPI2C_CHANNEL_0 defined is 2 Expected behavior: With Lpi2c Ip module we have only 2 instances, so if use Lpi2c1 generated code should be generate to 0 and Lpi2c2 is 1 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-134776	Bug	[wdg] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253!

ID	Subtype	Headline and Description
		In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-134782	Bug	[I2C] EB tresos not raise an error when baudrate out of range operation mode Detailed description (how to reproduce it): Add I2c component into EB tresos Chose Standard operating mode Config values to change the baudrate higher than 400kps Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The warning does not appear if the baud rate value does not match the mode And I see that when use Flexio_I2c, some error raise from Lpi2c while we not use Expected behavior: Need condition with specific operating mode Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Refer S32DS
ARTD-134785	New Feature	[I2C] Create an additional I2c.Lpi2c.OffsetValue element in the resource file NewWorkDescription: Update new I2c.Lpi2c.OffsetValue element in the resource file. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A
ARTD-134792	Bug	[I2C] High speed support Target only Detailed description (how to reproduce it): Create a EBtresos/S32DS and add CDD_I2c component Config Lpi2c channel with master mode

ID	Subtype	Headline and Description
		Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: I2c_TS_COT_EQ01 Observed behavior: In Reference Manual, Lpi2c support high speed mode for Target only. But we have high speed config field in Lpi2c_Master section Expected behavior: High speed config field should be remove in Lpi2c_Master section if not supported Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-134806	Bug	S32K388 startup_cm7.s does not support CM7_3 Hi RTD team, The startup code startup_cm7.s in S32K388 platform module does not support boot the CM7_3. The CM7_3 enable bit and start address are not included in the IVT structure. !image-2024-07-03-17-47-59-848.png! Could you please help to fix this in the next RTD version?
ARTD-134841	New Feature	[ADC] Support DMA error notification NewWorkDescription: Currently, DMA error notification has not been supported Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support DMA error notification for ADC
ARTD-136494	New Feature	[IMPLEMENTATION] BCTU DMA configuration CR description: There is not possible to used own address for the destination of the DMA which move the data from the BCTU FIFO triggered by the watermark level. Reason for this change: This change is necessary for using the BCTU together with the eTPU because we need move the measured data into concrete memory. Also when i will need to place the result into the core TCM or specific area i need to configure there the destination address. Benefit: Safe moving the data between automatic generated output buffer and proper address where the data needs to be stored. Use-case: Motor Control HW documentation reference (as applies): Tested on the S32K39 EVB. HW/Application Engineer contact (as applies): Tomas Kulig Note: relevant documents to be attached to the ticket.
ARTD-136661	New Feature	[icu] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of Oslf_GetCoreID to OslfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_}

ID	Subtype	Headline and Description
		reference implementation(s) : ARTD-97002
ARTD-136689	New Feature	[WDGIF] Generate a new macro to represent all instances used NewWorkDescription: When we develop a new platform that has more WDG instances in the past, the Wdgif needs to be updated as the condition bellow : !image-2022-12-23-13-33-39-040.png|width=892,height=191! To avoid wasting effort on this, the code generation can generate a new macro to represent all instances which are being used. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Generate a new macro if there is at least one WDG instance is being used: *{color:#00875a}USE_WDG_INSTANCE_ANY Use this new macro instead of repeating each macro for each instance
ARTD-136750	New Feature	[S32K3XX_S32M27x_5.0.0][MEMACC] Generate UML for the S32K3XX platform from the Generic design folder by using the EAExporter tool. NewWorkDescription: Generate UML for the S32K3XX platform from the Generic design folder by using the EAExporter tool. Requirement source: \dev\drivers\AutoSAR\memacc\generic\doc\design\RTD_MEMACC_SDD.EAP Proposed solution optional: Using the EAExporter tool to generate UML for the S32K3XX platform.
ARTD-136804	Bug	EB example project verify error based [SW32K3_S32M27x_RTD_R21-11_4.0.0_P19] Detailed description (how to reproduce it): [when import example SW32K3_S32M27x_RTD_R21-11_4.0.0_P19\eclipse\plugins\Dio_TS_T40D34M40I0R0\examples\EBT \S32K396\Dio_Example_S32K396\TresosProject, and click verify project, there some error appear in the error log, detailed info can be found in the blew picture. !image-2024-07-09-14-38-38-398.png!] Preconditions: [Import example project SW32K3_S32M27x_RTD_R21-11_4.0.0_P19\eclipse\plugins\Dio_TS_T40D34M40I0R0\examples\EBT \S32K396\Dio_Example_S32K396\TresosProject] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [some error appear when verify the EB example project] Expected behavior: [pass example verification] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [none]
ARTD-136869	Bug	Frame Counter Bug RTD Driver shall fix bug related to Frame Counter Fault processing SPI comm has GHS in which Frame Counter occupies bits from 14:8, which gives it range 0 127. Variable u32FrameCounter is never checked and never limited to max value of 127. On AE side, if counter goes above, it starts from 0 again, this needs to be implemented on RTD side
ARTD-136872	Bug	NMI flag not cleared in WKPU for S32M27X NMI flag is never cleared in WKPU (it should be done by RTD side)
ARTD-136875	Bug	Check Fault/Event for S32M27X at the end of fault processing This is for S32M27X platform, NMI can be only edge sensitive. This causes problem as, we only read fault status once. In case another fault happens during handling of initial fault, this new fault is not handled. There has to be logic done at the end of fault processing, to read back Fault/Event status and if anything is pending to call again AEC_IRQEventFaultHandler();
ARTD-136878	Bug	LPSPI timeout fix Current implementation uses Lpspi_Ip_Cancel function in MNI. This fixes problems with SPI, but creates new one. Previous interrupted communication is not aware of this problem, and LPSPI timeout occurs. But due to this, interrupt for handling of AE faults is postponed for this timeout interval (default is 50ms). Please fix it, so if Lpspi_Ip_Cancel is called, ongoing comm is notified and doesnt get stuck in that timeout loop.

ID	Subtype	Headline and Description
ARTD-136882	Bug	Injection of fault not working correctly Reading of Faults and Events when injected through IRQ_SET register is not working properly. Faults/Event is recognized, but GHS is checked only for Event, and if not event is pending, fault is not handled. (function AEC_IRQEventFaultHandler)
ARTD-136898	Bug	[icu] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT # !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins # !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-136906	Bug	[MCL] Build fail on S32K3XX with compiler IAR Detailed description (how to reproduce it): build tests that use the mcl module with IAR Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Uart_TS_4001 Observed behavior: Build fail !image-2024-07-10-09-54-57-003.png|width=543,height=177! Expected behavior: Build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-136931	New Feature	[GDU] Implement CPR_RTD_01182.gdu NewWorkDescription: Implement CPR_RTD_01182.gdu

ID	Subtype	Headline and Description
		Requirement source: CPR_RTD_01182.gdu:Pending interrupt flags shall be cleared before enabling interrupts. Rationale: If the interrupt flag was set by a spurious event enabling the interrupt will cause an unwanted interrupt event. Proposed solution optional: [....]
ARTD-136954	New Feature	[pwm] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of Oslf_GetCoreID to OslfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-136967	Bug	[PWM][FLEXIO/EMIOS] Pwm_Init generates a spike in the output signal. Detailed description (how to reproduce it): When i config channel tests in VS_0 as a picture bellow ({*}Idle state is HIGH{*}) !image-2024-07-10-16-29-32-010.png! In VS_1 . I config channel tests in VS_0 as a picture bellow ({*}Duty = 0%, polarity is LOW{*}) !image-2024-07-10-16-38-12-835.png! After calling Pwm_Init, there is a spike in the output signal. !image-2024-07-10-16-45-35-980.png! Please re-check this function !image-2024-07-10-16-48-51-812.png! In the same issue, when i config for Emios Channel !image-2024-07-12-10-09-00-552.png! Preconditions: Config more than 1 VS . In VS0 used Idle state is HIGH* and in VS_1 configured so that the signal is HIGH Test Case ID (internal TC that caught the defect) optional: Pwm_TS_106 configuration 6 Observed behavior: Pwm_Init generates a spike in the output signal. Expected behavior: Pwm_Init does not generate a spike on output signal. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-137000	New Feature	[IMPLEMENTATION] [ADC] Integrate latest 1.0.1 RTM CFSDADC FW into RTD Description:* CR description:_* Coolflux released a new 1.0.1 RTM release of their FW that supports the S32K36X derivatives. Benefit for this change:_* Adds DSPSS support to K36X derivatives. Use-case:_* Motor control. Technical recommendations:_* [to be filled in by assigned SW Architect]_ Planning recommendations:_* [to be filled in by assigned SW Program Manager]_

ID	Subtype	Headline and Description
ARTD-137127	New Feature	[MCU] Support FIRC_DIV_SEL for K396 NewWorkDescription: Support FIRC_DIV_SEL for K396 Requirement source: S32K396RM Rev. 3, 03/2024 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A
ARTD-137280	Bug	[Mem_InFLS] Caculate CRC incorrect when enable utest mode Detailed description (how to reproduce it): Mem_43_INFLS_pConfigPtr->u16ConfigCrc != Mem_43_INFLS_CalcCfgCRC() Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_InFls_TC_FCT_0019 Observed behavior: !image-2024-07-02-17-47-41-667.png!!image-2024-07-02-17-48-33-041.png! Expected behavior: Caculate CRC correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-137307	Bug	[Mem_Infls] Async mode is not completely asynchronous Detailed description (how to reproduce it): Currently, write/erase is not completely asynchronous. on each mainfunction call, the job is complete done on hardware. > it is not Async actually. The driver should be return immediate after set job on hardware. And will check the status on the next mainfunction call. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The driver set job on hardware and waits status on the mainfunction Expected behavior: The driver set job on hardware and return immediately, and check status on the next main function. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: implement the async mode correctly
ARTD-137398	Bug	[S32K3XX_S32M27x_5.0.0] PLATFORM: Compare generated code between generators NewWorkDescription: Report all test in the attachment RTD_PLATFORM_CompareCodeGenMergeReport.xlsx{*}{*} IntCtrl_Ip_CfgDefines.h !image-2024-07-15-09-52-38-195.png|width=1310,height=126! Details infor for file c type and h type !image-2024-07-15-09-51-26-865.png|width=1309,height=563! List file .h are different IntCtrl_Ip_CfgDefines.h List file .c are different Platform_Ipw_Cfg.c Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Codes gen in EB are the same in CT

ID	Subtype	Headline and Description
ARTD-137412	Bug	[Mem_ExFls] Driver accepts a job with Length of 0xFFFFFFFF Detailed description (how to reproduce it): if we call Mem_43_EXFLS_Write(0U, 2U, TxData, 0xFFFFFFFFU); mean while start sector address is 2, sector size is 0x1000, the driver accepts that job it is not logical Preconditions: length passed to write function is 0xFFFFFFFFU Test Case ID (internal TC that caught the defect) optional: Mem_TC_API_0000 Observed behavior: N/A Expected behavior: The driver must not accept jobs like that Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-137418	Bug	[Mem_Infls] The container "MemInstance" and node "MemInstanceId" need to improve to follow requirement [ECUC_Mem_00003] + [ECUC_Mem_00007] Detailed description (how to reproduce it): The current value of the node "MemInstanceId" in the configuration interface does not make sense, Following the requirement "ECUC_Mem_00007", it should be "ID of the related memory driver instance". So "MemInstance" will be one container for each Mem driver instance. for example: The S32K3XX platform has only 1 memory driver instance QSPI_0, so the container "MemInstance" will be one container only for one Mem driver instance (QSPI_0). The value of the node "MemInstanceId" should be 0x0U. The S32ZE platform has 2 memory driver instances QSPI_0 and QSPI_1, so the container "MemInstance" will be 2 containers maximum for 2 Mem driver instances (QSPI_0 QSPI_1). The node "MemInstanceId" value should be 0x0U and 0x01 in order. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The current node is no reference to the mem driver instance: !image-2024-07-12-22-13-49-860.png! Expected behavior: "MemInstance" will be one container for each Mem driver instance. The node "MemInstanceId" value should be "ID of the related memory driver instance". Requirement source: [ECUC_Mem_00003] [ECUC_Mem_00007] Proposed solution optional: N/A
ARTD-137421	Bug	[ICU] Build fail when IcuWakeupFunctionalityApi = ON and IcuReportWakeupSource = OFF Detailed description (how to reproduce it): Build fail when IcuWakeupFunctionalityApi = ON and IcuReportWakeupSource = OFF both are RTD notes Preconditions: when IcuWakeupFunctionalityApi = ON and IcuReportWakeupSource = OFF Test Case ID (internal TC that caught the defect) optional: Icu_TS_COT_900 Observed behaviour: N/a Expected behaviour: N/a Note: in the “Expected behaviour” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:N/a
ARTD-137724	Bug	[ICU] Incorrect version checking and duplicate include Detailed description (how to reproduce it): 1 Not include Std_Types.h in Ftm_Icu_Ip_Types.h file but driver still checking version of this file !image-2023-11-30-16-48-09-948.png|thumbnail! Solution: Remove checking Std_Types.h version in Ftm_Icu_Ip_Types.h file

ID	Subtype	Headline and Description
		2 Dulicate incldue " Wkpu_lp_Types.h" in Wkpu_lp.h file. because Wkpu_lp_Types.h already incldued in Wkpu_lp_Cfg.h !image-2023-11-30-16-48-20-626.png|thumbnail! !image-2023-11-30-16-48-31-322.png|thumbnail! !image-2023-11-30-16-48-50-598.png|thumbnail! Solution: Remove #include "Wkpu_lp_Types.h" in Wkpu_lp.h file Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-137872	New Feature	[can] [IMPLEMENTATION] R21-11 Multicore Concept changes - multipartition vs multicore CR description: Add support for multi-partition support according to [AUTOSAR_EXP_BSWDistributionGuide.pdf R21-11|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Standards/AutosarR21-11/BSWGeneral/AUTOSAR_EXP_BSWDistributionGuide.pdf?csf=1&web=1&e=OrlE69] Implementation requested on driver : # Drivers must have the configuration structures implemented based on the number of partitions and not the number of cores. # Drivers must replace the existing call of OsIf_GetCoreID to OsIfGetUserID. # Drivers must have in the configuration structures the referenced Ecuc Partition. # Drivers must replace existing core_id check to partition_id check. # Example(s) must be updated and this shall be seen as an input for future definition on Platform Base Bundle configuration. # Single core constraints which don't allow enabling the multicore (multipartition) on one core must be removed from driver. # Update label and description of "{_}Multicore Support Enable"{_} node to "{_}MultiPartition Support Enable"{_} reference implementation(s) : ARTD-97002
ARTD-137897	New Feature	[ADC] Implement requirement CPR_RTD_01182.adc for SDADC and DSPSS NewWorkDescription: Pending interrupt flags shall be cleared before enabling interrupts. SDADC : Sdadc_Ip_EnableInterruptEvents DSPSS : DSPSS_InterruptEnable Requirement source: CPR_RTD_01182.adc (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A
ARTD-137936	Bug	[Base][K3 5.0.0] Fix the latest revision of header files for S32K388 Crypto ACE Detailed description (how to reproduce it): There are multiple changes between the rev. 1.2, 2023-04-05 and rev. 1.3, 2023-09-12 of header files for AES_ACCEL, ACE, FEED and RESULT DMA. The latest revision adds changes incompatible with the Crypto Ace driver and can't be compiled and used. Preconditions: Switch to BaseNXP tag PVT_BASE_S32K3XX_4.0.0_P12_002 and attempt a Crypto Ace ng build on S32K388. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The driver isn't able to build correctly and even if the code was changed to use the header files, it would still not work due to hardware implementation vs header file access. Expected behavior: The Crypto Ace driver builds correctly using the latest revision of header files. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Make a comparison between the PVT_BASE_S32K3XX_4.0.0_P12_002 and PVT_BASE_S32K3XX_S32M27X_4.0.0_P04_001 and fix the differences.
ARTD-137950	Bug	[Mem_Eep] The container "MemInstance" and node "MemInstanceId" need to improve to follow requirement [ECUC_Mem_00003] + [ECUC_Mem_00007]

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): The current value of the node "MemInstanceId" in the configuration interface does not make sense, Following the requirement "ECUC_Mem_00007", it should be "ID of the related memory driver instance". So "MemInstance" will be one container for each Mem driver instance. for example: The S32K3XX platform has only 1 memory driver instance QSPI_0, so the container "MemInstance" will be one container only for one Mem driver instance (QSPI_0). The value of the node "MemInstanceId" should be 0x0U. The S32ZE platform has 2 memory driver instances QSPI_0 and QSPI_1, so the container "MemInstance" will be 2 containers maximum for 2 Mem driver instances (QSPI_0 QSPI_1). The node "MemInstanceId" value should be 0x0U and 0x01 in order. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The current node is no reference to the mem driver instance: !image-2024-07-12-22-13-49-860.png! Expected behavior: "MemInstance" will be one container for each Mem driver instance. The node "MemInstanceId" value should be "ID of the related memory driver instance". Requirement source: [ECUC_Mem_00003] [ECUC_Mem_00007] Proposed solution optional: N/A
ARTD-137980	New Feature	[S32K3xx][MEM_INFLS] Implement support for HW backed ongoing NVM job cancellation {*}Description{*}: <Below template to be filled-out, bold sections are mandatory.> CR description:_* R21-11 mem drivers layers (either MEM_ACC or MEM IP drivers) to be modified to allow an upper NVM request to cancel the ongoing job by leveraging the C40 IP HW support. Benefit for this change:_* Fulfill customer expectations, fully enable our devices HW support, differentiate from the competition. Use-case:_* One obvious use-case is being able to stop an ongoing lengthy NVM write job and store critical diagnostics data in case of a imminent ECU shutdown or brownout reset. Technical recommendations:_* While not strictly specified by ASR R21-11, NXP should add this functionality as it leverages on our device capabilities and fulfills customer request. Planning recommendations:_* [to be filled in by assigned SW Program Manager]_
ARTD-138335	Bug	[S32K3_M27X 5.0.0][Port]: Compare generated code between generators Detailed description (how to reproduce it): The generated files between EBT and S32CT are not the same when importing epc file For more details, open the attached file: *{color:#de350b}build.zip EB code gen path:*_ (.c, .h, .xdm) build\$(TEST_NAME)\generate(include/src) CT code gen path:* (.c, .h, .mex) build\$(TEST_NAME)\generate\s32ct_project\generate_s32ct\generate(include/src) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Port_TS_001 Port_TS_COT_001 cfg20 Port_TS_006

ID	Subtype	Headline and Description
		Observed behavior: Port_TS_001 igf_port_ip_cfg.h !image-2024-07-17-17-59-18-287.png|width=1043,height=61! tspc_port_ip_cfg.h !image-2024-07-17-17-59-34-730.png|width=1116,height=296! Port_TS_COT_001 cfg20 igf_port_ip_cfg.h !image-2024-07-17-18-02-13-142.png|width=1206,height=100! igf_port_ip_vs_0_pbcfg.h !image-2024-07-17-18-02-53-570.png|width=1024,height=52! Igf_Port_Ip_VS_0_PBcfg.c !image-2024-07-17-18-03-10-858.png|width=1175,height=89! Port_TS_006 Siul2_Port_Ip_Cfg.h !image-2024-07-17-18-03-55-610.png|width=937,height=57! Siul2_Port_Ip_PBcfg.c !image-2024-07-17-18-04-42-543.png|width=959,height=475! Expected behavior: The code generated between EB and CT is the same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-138869	Bug	[PLATFORM][S32K3XX_S32M27x_5.0.0] Enable Core3 occur hardfault with K396 Detailed description (how to reproduce it): Enable Core3 occurr hardfault on K396 because K396 don't have core 3 in RM, it only have 3 core (0,1,2) Preconditions: run test multicore Test Case ID (internal TC that caught the defect) optional: Platform_TS_MUL_001 Platform_TS_MUL_002 Observed behavior: hardfault at line EnableCore3 in startup_cm7.s Expected behavior: Not enable core 3 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update startup code, change condition to #if (CM7_3_ENABLE == 1) !image-2024-07-18-11-02-53-631.png|width=580,height=163!
ARTD-140360	Bug	[S32K3/M2] FCCU ITCM and DTCM faults set during startup code Detailed description (how to reproduce it):

ID	Subtype	Headline and Description

		During startup code execution the FCCU status flag CM7_0_ITCM_ECC_ERR is set (due to ARM core speculative memory access before TCM memory is initialized).
		
		Preconditions:
		N/A
		
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		
		Observed behavior:
		FCCU status flag CM7_0_ITCM_ECC_ERR is set during startup code execution.
		
		Expected behavior:
		FCCU status flag CM7_0_ITCM_ECC_ERR not set during startup code execution.
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		Move the ITCM and DTCM initialization in the beginning of the startup code (i.e. to be done as soon as possible after reset to prevent ARM core speculative access). See attachment code how to it was fixed with customer.
		And use the MOV and MOVT instructions instead of LDR.
		
		Example code:
		
		/ Workaround Enabling ITCM and disabling RETEN ITCM Init to avoid ECC faults /
		NOP
		MOV r1,#0xEF90
		MOVT r1,#0xE000
		LDR r0, [r1]
		bic r0, r0, #0x4
		orr r0, r0, #0x1
		str r0, [r1]
		
		ITCM_Init:
		/ Initialize ITCM ECC /
		ldr r0, =__ITCM_INIT
		cmp r0, 0
		/ Skip if TCM_INIT is not set /
		beq ITCM_LOOP_END
		
		ldr r2, =__INT_ITCM_START
		ldr r3, =__INT_ITCM_END
		
		cmp r2, r3
		bge ITCM_LOOP_END
		
		movs r0, 0
		movs r1, 0
		ITCM_LOOP:
		strd r0, r1, [r2], #8
		cmp r2, r3
		blt ITCM_LOOP
		ITCM_LOOP_END:
		
		/ Enabling DTCM and disabling RETEN /
		NOP
		MOV r1,#0xEF94
		MOVT r1,#0xE000
		LDR r0, [r1]
		bic r0, r0, #0x4
		orr r0, r0, #0x1
		str r0, [r1]
		
		DTCM_Init:
		/ Initialize DTCM ECC /
		ldr r0, =__DTCM_INIT
		cmp r0, 0
		/ Skip if DTCM_INIT is not set /
		beq DTCM_LOOP_END
		
		ldr r2, =__INT_DTCM_START
		ldr r3, =__INT_DTCM_END
		
		cmp r2, r3
		bge DTCM_LOOP_END
		
		movs r0, 0
		movs r1, 0
		DTCM_LOOP:
		strd r0, r1, [r2], #8
		cmp r2, r3
		blt DTCM_LOOP
		DTCM_LOOP_END:

ARTD-140356	Bug	[S32K3xx_S32M27x_5.0.0] Error when generating code for S32K364, S32K366

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Create new project for S32K364, S32K366 add port component some pins Generate code !image-2024-07-18-15-17-02-522.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Port_TS_COT_013 Observed behavior: Error when generating code on EB: !image-2024-07-18-15-15-29-650.png! !image-2024-07-18-15-16-34-980.png! on CT: crash when opening peripheral: !image-2024-07-18-15-23-24-813.png! Expected behavior: No error when generating code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-140443	Bug	[PWM] Error related to set period on FlexPwm_Ip Detailed description (how to reproduce it) Issue 1: Duty, Deadtime, Phase shift can be configured to be larger than {*}period{*}. Due to period, Duty, Deadtime, Phase shift will following ticks so that is not true !image-2024-07-19-09-06-16-744.png! !image-2024-07-19-09-08-25-489.png! Issue 2: The configuration values of period and duty are different The configuration values of period is in the range 0 65535 The configuration values of duty is in the range 0 65534. So if i config period is 65535 ticks, i cann't use 100% duty cycle !image-2024-07-19-09-16-20-361.png! !image-2024-07-19-09-16-35-937.png! Preconditions: Using FlexPwm_Ip Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Issue 1: Duty, Deadtime, Phase shift can be configured to be larger than period Issue 2: The configuration values of period and duty are different Expected behavior: Issue 1 : Rasing error when Duty, Deadtime, Phase shift can be configured to be larger than period Issue 2: The configuration values of period and duty are the same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-140479	Bug	[gpt] Driver makefile needs to be updated with the correct version of AUTOSAR SWS specification Detailed description (how to reproduce it): !image-2023-12-29-14-56-48-393.png|width=645,height=253! In <driver>.mak file, the information of AUTOSAR module SWS specification version are incorrect. E.g.: some drivers contains 4.3 references Preconditions: NA

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Wrong information from: # When importing project to EBT !image-2023-12-29-14-59-58-330.png|width=470,height=393! # plugin.xml from plugins !image-2023-12-29-15-01-33-443.png|width=310,height=306! Expected behavior: The information needs to be updated. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the information from <driver>.mak based on the supported version of ASR for drivers that are delivering ASR R2x-11: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_7_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 7 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif only for drivers that are delivering ASR 4.4: ifeq ($(AR_RELEASE_REVISION),ASR_REL_4_4_REV_0000) SWS_SPEC_VERSION_MAJOR = 4 SWS_SPEC_VERSION_MINOR = 4 SWS_SPEC_VERSION_PATCH = 0 SWS_SPEC_VERSION_SUFFIX = Rev_0000 endif
ARTD-140486	Bug	[gpt] Incorrect section memory for the variables Detailed description (how to reproduce it): As in [Driver]_Memmap.h, section memory xx_START_SEC_CONFIG_DATA_xx refers to the .mcal_const_cfg section, which is for constant value. However, in Gpt driver some variables are defined as a variable which is not a const type. for example in Gpt_Ipw_PBcfg.c #define GPT_START_SEC_CONFIG_DATA_UNSPECIFIED #include "Gpt_MemMap.h" Gpt_Ipw_HwInstanceConfigType Gpt_Ipw_HwInstanceConfig_PB_VS_0_P_EcucPartition_0[5U]= {... } Gpt_Ipw_HwChannelConfigType Gpt_Ipw_ChannelConfig_PB_VS_0_P_EcucPartition_0[8U]= {... } #define GPT_STOP_SEC_CONFIG_DATA_UNSPECIFIED #include "Gpt_MemMap.h" Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Correct section memory Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to add const for the variable for data configuration in generation file
ARTD-140492	Bug	[ICU]Some SIUL2_IP_PDAC addresses are not being defined correctly when VIRTWRAPPER_SUPPORT is enabled Detailed description (how to reproduce it): When using the VirtWrapper support support feature, the SIUL2_IP_PDA address is incorrectly generated !image-2024-07-19-10-54-21-814.png|thumbnail! , causing the siul2 register address to be written to the wrong address.

ID	Subtype	Headline and Description
		Preconditions: SIUL2_ICU_IP_VIRTWRAPPER_SUPPORT ==STD_ON Test Case ID (internal TC that caught the defect) optional: Icu_TC_FCT_0201(Icu_TS_100) Observed behavior: Some SIUL2_IP_PDAC addresses are not being defined correctly when VIRTWRAPPER_SUPPORT is enabled Expected behavior: SIUL2_IP_PDAC addresses are generated correctly when VIRTWRAPPER_SUPPORT is enabled Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In the file Siul2_Icu_Ip_Defines.h, you need to define the correct addresses: #define SIUL2_IP_PDAC0_BASE (0x40290000U) #define SIUL2_IP_PDAC0 ((SIUL2_Type)SIUL2_IP_PDAC0_BASE) #define SIUL2_IP_PDAC1_BASE (0x40298000U) #define SIUL2_IP_PDAC1 ((SIUL2_Type)SIUL2_IP_PDAC1_BASE) #define SIUL2_IP_PDAC2_BASE (0x402A0000U) #define SIUL2_IP_PDAC2 ((SIUL2_Type)SIUL2_IP_PDAC2_BASE) #define SIUL2_IP_PDAC3_BASE (0x402A8000U) #define SIUL2_IP_PDAC3 ((SIUL2_Type)SIUL2_IP_PDAC3_BASE) #define SIUL2_IP_PDAC4_BASE (0x402F4000U) #define SIUL2_IP_PDAC4 ((SIUL2_Type)SIUL2_IP_PDAC4_BASE) #define SIUL2_IP_PDAC5_BASE (0x40348000U) #define SIUL2_IP_PDAC5 ((SIUL2_Type)SIUL2_IP_PDAC5_BASE)
ARTD-140779	Bug	[LINTRCV] difference between driver files that generated by S32CT and EB tresos Detailed description (how to reproduce it):*_ the difference between driver file that generated by S32CT and EB tresos as below: !image-2024-07-21-23-18-49-426.png!!image-2024-07-21-23-18-25-766.png! !image-2024-07-21-23-19-54-747.png! !image-2024-07-21-23-21-54-250.png! Driver should be limited channel ID and should have error when config 2 or more channel that using same Hardware channel as below: TS: LinTrcv_TS_COT_001 !image-2024-07-23-14-02-04-080.png! !image-2024-07-23-14-02-11-246.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: LinTrcv_TS_COT_001, LinTrcv_TS_M01,LinTrcv_TS_001,LinTrcv_TS_013,LinTrcv_TS_014,LinTrcv_TS_017,LinTrcv_TS_004,LinTrcv_TS_003,LinTrcv_TS_D01 Observed behavior: Expected behavior: No difference raised Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: No difference raised
ARTD-140789	Bug	[S32K3 M27X 5.0.0] Dio: Compare generated code between generators Detailed description (how to reproduce it): # The generated files between EBT and S32CT are not the same when importing epc file. It doesn't cause compilation error but report from compare tool is failed. The inconsistency is mentioned as attached images. Error detected at: Driver tag: DIO_193 Test tag: PVT_TEST_DIO_S32K3XX_M27X_500_V17 Derivative: S32K396 List files compare: Dio_Cfg.h, Siul2_Dio_Ip_Cfg.h, Dio_Cfg.c => The difference in comments and defined values leads to the tool catching different errors Example: 2. In file: dio_cfg.c !image-2024-07-26-14-39-17-378.png|width=1049,height=244! For details see file: Compare_Report.zip

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: Test suite: Dio_TS_010, Dio_TS_011, Dio_TS_COT_002, Dio_TS_003, Dio_TS_005, Dio_TS_701, Dio_TS_200, Dio_TS_201, Dio_TS_202, Dio_TS_203, Dio_TS_020, Dio_TS_013, Dio_TS_COT_060 Observed behavior: Compare generated code between different generators Expected behavior: Compare generated code between similar generators Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-140821	Bug	[S32K3XX][Mem_Infls] The LoadAc operation still occurs when JobBlockSector =C40_IP_BLOCK_INVALID, BlockAc = C40_IP_BLOCK_INVALID Detailed description (how to reproduce it): The LoadAc operation still occurs when JobBlockSector =C40_IP_BLOCK_INVALID, BlockAc = C40_IP_BLOCK_INVALID in IPW_CheckLoadAc function Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The LoadAc operation still occurs when JobBlockSector =C40_IP_BLOCK_INVALID, BlockAc = C40_IP_BLOCK_INVALID in IPW_CheckLoadAc function Expected behavior: The LoadAc operation does not doccur when JobBlockSector =C40_IP_BLOCK_INVALID, BlockAc = C40_IP_BLOCK_INVALID in IPW_CheckLoadAc function Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-140826	Bug	[S32K3XX][Mem_Infls] The driver does not return ERROR immediately when the Erase/Write job is not approved in IP layer Detailed description (how to reproduce it): The LoadAc operation still occurs when JobBlockSector =C40_IP_BLOCK_INVALID, BlockAc = C40_IP_BLOCK_INVALID in IPW_CheckLoadAc function Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The LoadAc operation still occurs when JobBlockSector =C40_IP_BLOCK_INVALID, BlockAc = C40_IP_BLOCK_INVALID in IPW_CheckLoadAc function Expected behavior: The LoadAc operation does not doccur when JobBlockSector =C40_IP_BLOCK_INVALID, BlockAc = C40_IP_BLOCK_INVALID in IPW_CheckLoadAc function Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-140839	Bug	[S32K3XX][Mem_Infls] Erase opration will be missing sector when user config sectorbust > sector size Detailed description (how to reproduce it): Erase opration will be missing sector when user config sectorbust > sector size Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Erase opration will be missing sector when user config sectorbust > sector size Expected behavior: Erase operation will erase all

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-140866	Bug	[ZIPWIRE] Driver missing implement CPR_RTD_00011.zipwire Detailed description (how to reproduce it): Issue happen in S32ZSE and S32K396 According the requirement CPR_RTD_00011.zipwire: ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. But driver not checking driver initialized or not (picture 1). ISR handler just only check interrupt flag and interrupt enable bit. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Zipwire_TC_FCT_0015 Observed behavior: Driver missing to implement CPR_RTD_00011.zipwire Expected behavior: ISR handler still do Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add code to check driver initialized or not first then checking flag if driver initialized
ARTD-140925	Bug	[S32K3XX_S32M27x_5.0.0][UART]: Difference between EB and CT gen code Detailed description (how to reproduce it): When running compare code gen tests suite, there are some difference about code gen between CT and EB (file log on Attachment) Preconditions: Running compare code gen test Test Case ID (internal TC that caught the defect) optional: Uart_TS_0001 Observed behavior: Difference code gen between CT and EB Expected behavior: The code gen between CT and EB need to be the same Proposed solution optional: N/A
ARTD-140928	Bug	[Fee][MemMap]: Some variables' definition conflict with the section attribute in memmap Detailed description (how to reproduce it): Some variables' definition conflict with the section attribute in memmap. For example,: In the Wdg module. The variable: Wdg_aePreviousMode[] which with a default initial value when definition. but it was located in the .mcal_bss section. This will case compiling error or unexpected binary file content. !image-2024-02-22-09-56-49-054.png! In the Gpt module. The variable: Gpt_lpw_HwInstanceConfig_PB[] which is a normal variable, but it was located to .mcal_const_cfg section, which means it shouldn't be changed. Variable: Gpt_lpw_ChannelConfig_PB and Fee_JobScheduleLookupTable also have the similar issue. !image-2024-02-22-09-57-07-701.png! Preconditions: Always Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiling error or unexpected contents in binary file. Expected behavior: Source code should be following the coding rule more strictly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Had a code review carefully for all the module code by each module owner.
ARTD-140955	Bug	[DIO][S32K3XX_M27X 5.0.0] Configuration error on S32DS of S32K396 Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		When configuring channel groups on S32DS, unavailable pins can still be configured and will not be reported as an error when configured as on Tresos. EX: config channel group for Port_0 Configuration on EB: {*}!image-2024-07-22-17-38-36-007.png!{*}{*} Configuration on S32DS:{*} !image-2024-07-22-17-38-56-945.png! {_}*Preconditions:*{_}{*}{*} Dio: DIO_193}} Test_Dio: PVT_TEST_DIO_S32K3XX_M27X_500_V18}} Derivative: S32K396 Test Case ID (internal TC that caught the defect) optional: Dio_TS_ECPD_001 Observed behavior: Channel group can configure not available pins Expected behavior: Channel group cannot configure unavailable pins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-141179	Bug	[S32K3XX 5.0.0] Mem_ExFls: Generate fails on DS Detailed description (how to reproduce it): Cannot generate ipw config files on DS !image-2024-07-23-13-31-03-349.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_001 (VV_COMPARE_CODE_GEN=ON) Observed behavior: as description Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-141184	Bug	[S32K3XX 5.0.0] Mem_ExFls: Generate fails when ecpd mode enabled Detailed description (how to reproduce it): Cannot generate config files !image-2024-07-23-13-37-32-280.png! Preconditions: modify codegenerator.js to generate ecpd file Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_COT_013 Observed behavior: as description Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-141214	Bug	[PWM] Difference EB and CT Detailed description (how to reproduce it): In file Pwm_VS_0_PBcfg.c !image-2024-07-23-14-14-39-110.png|width=539,height=280! In file Pwm_Ipw_Cfg.h !image-2024-07-23-14-16-28-756.png|width=535,height=187!

ID	Subtype	Headline and Description
		!image-2024-07-23-14-16-57-610.png|width=543,height=148! Please help me check in attach .zip file Preconditions: Compare code gen between EB and CT Test Case ID (internal TC that caught the defect) optional: Pwm_TS_001 CFG_SETS=1_tresos Observed behavior: Difference between EB and CT Expected behavior: Compare code gen pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-141329	Bug	[PWM][EMIOS] Registers A and B not cleared after calling Pwm_DeInit function Detailed description (how to reproduce it): After calling Pwm_DeInit function, A and B registers are not cleared. These registers are only cleared in IP layer Non_Asr. Preconditions: Call Pwm_DeInit function with an eMios channel. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Registers A and B are not cleared after calling Pwm_DeInit function. Expected behavior: Registers A and B are cleared after calling Pwm_DeInit function. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-141385	Bug	[SPI][S32K3] Implement DSPI errata ERR051648 for S32K39_37 Detailed description (how to reproduce it): Implement 2 new DSPI erratas for S32K39_37: ERR051648 SPI In Continuous Selection Format observed tASC timing differs from the expected one. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Implement 2 new DSPI erratas for S32K39_37. Expected behavior: Implement 2 new DSPI erratas for S32K39_37. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: ERR051648 SPI In Continuous Selection Format observed tASC timing differs from the expected one => integrate the implementation from SPI_IP to DSPI_IP ERR051701 SPI De-asserting of CONT bit in the Continuous Selection Format is not mandatory for the last frame => ignore due to not affect to spi hardware
ARTD-141390	Bug	[Pwm] Cannot generate ECPD file Detailed description (how to reproduce it): Cannot generate ECPD file when max_id value and max_expr are getFeature(`FEATURE_PWM_TIMERNUMERICALPRECISION`) !image-2024-07-24-17-31-21-807.png|width=538,height=339! Preconditions: Gen test ecpd

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: Pwm_TS_ECPD_001 for all derivatives Observed behavior: Cannot gen ecpd file Expected behavior: Gen ecpd file success Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Replace the max value is "16777214.0" !image-2024-07-24-17-33-08-319.png|width=951,height=199!
ARTD-141511	Bug	[S32K3xx_S32M27x_5.0.0][S32K396][s32ct-HLD] build fails with ghs compiler Detailed description (how to reproduce it): Build test with ghs compiler Preconditions: GENERATOR = s32ct Test Case ID (internal TC that caught the defect) optional: Port_TS_004 Port_TS_005 Observed behavior: http://panama.ea.freescale.net/1/project/ar_int_for_ct_port_ghs/20240725023824639000/details build error: !image-2024-07-25-14-11-22-091.png|width=990,height=238! Expected behavior: build successfully Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-141598	Bug	[S32K3XX_M27X 5.0.0] [DIO] Channel group configuration error on S32DS Detailed description (how to reproduce it): When configuring channel groups on EB. Channel group only pins with read/write functionality can be configured. EX: config chanle group Pins 0,1 (only read) of Port 0 on S32K396 !image-2024-07-26-09-09-40-171.png! These 2 pins are readable but not configurable. !image-2024-07-26-09-51-52-204.png! Preconditions: Dio: DIO_198 DIO_ITG: PVT_TEST_DIO_S32K3XX_M27X_500_V24 Derivative: All Test Case ID (internal TC that caught the defect) optional: Dio_TS_003 Observed behavior: Channel group only pins with read/write functionality can be configured. Expected behavior: Channel group can only be read or can only be written can still be configured Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional
ARTD-141647	Bug	[Mem_INFLS] Fixing Compiler Warning Detailed description (how to reproduce it): fix compiler warning Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_InFls_TC_FCT_0001 Observed behavior:

ID	Subtype	Headline and Description
		[^RTD_MEM_Compiler_Warnings (6) 1.xlsx] Expected behavior: Build succed without compiler warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-141857	Bug	[LIN_LPUART]The Lin baudrate divisor was generated that didn't same each other on S32DS and EB Tresos Detailed description (how to reproduce it): S32K344, LPUART_IP_0, AIPS_PLAT_CLK = 80MHZ Baudrate divisor value in EB tresos is different to Design studio. Lpuart_Lin_Ip_VS_0_PBcfg.c [EB tresos] !https://community.nxp.com/t5/image/serverpage/image-id/290219i9914993FD4558004/image-size/medium?v=v2&px=400! [Design studio] !https://community.nxp.com/t5/image/serverpage/image-id/290223iCE0F7DB1234B4F79/image-size/medium?v=v2&px=400! The divisor is 0x103 in EB, but it is 0x104 in DS, when baudrate is set to 19200 bps, Why the divisor is different? The divisor seems to be generated by combination generate_PB/Lin_BaudRate_Comp.m and src/Lpuart_Lin_Ip_PBcfg.c So when I tried to change Lin_BaudRate_Comp.m like below in EB to adjust the divisor, but I met verify error. [!VAR "BaudrateConf_Value" = "($ClockFrequencyFromMcu div ($LinBaudrate 16)) 1"!] > [!VAR "BaudrateConf_Value" = "($ClockFrequencyFromMcu div ($LinBaudrate 16)) "!] Customer wants to set 0x104 in EB, because it is more accurater. But there is no way to change the divisor. Preconditions: On EB Tresos, with baudrate = 19200, the baudrate divisor should be generated as 0x104 in stead of 0x103 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: as Detailed description Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-141870	Bug	[Platform] Update symbol Mem_43_INFLS_ACEraseRomStart/Mem_43_INFLS_ACWriteRomStart in linker flash IAR Detailed description (how to reproduce it): Mem_INFLS Driver has feature Load code to ram to handling case Read while Write. Function C40_Ip_AccessCode will be loaded to ram when this case happened. Address of C40_Ip_AccessCode is Mem_43_INFLS_ACEraseRomStart/ Mem_43_INFLS_ACWriteRomStart (need same block with code building on FLASH). But in IAR toolchain, Address of C40_Ip_AccessCode is different block with code building so C40_Ip_AccessCode is not load to ram. Lead to cannot handling case Read while Write. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_InFls_TC_FCT_0004 Observed behavior: !image-2024-07-29-13-46-22-426.png!!image-2024-07-29-13-46-35-093.png! Expected behavior: Mem_43_INFLS_ACEraseRomStart/Mem_43_INFLS_ACWriteRomStart in int_pflash_start Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-142062	Bug	[wdg] Generated headers cannot be built in case sensitive file systems Detailed description (how to reproduce it): Create S32DS Project from Example, configure the project with any valid configuration and generate the code. When building the project there will be errors since the path is invalid.

ID	Subtype	Headline and Description
		In conclusion, the case sensitive issues are found in RTD drivers. See the slide attached. Preconditions: The host file system being used to build the sources is case-sensitive. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When you build the project there will be errors since the path is invalid. Expected behavior: Generated sources can be build in case-sensitive systems. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Assume always that sources are building in a case-sensitive file system, therefore use the filename path in the C preprocessor includes directives with the same case as the actual filename path. Steps: # Create new folder "C:\NXPCaseSensitive" (or use the existing ones) now we call it as "working folder". # Run the below command on Windows PowerShell opened in administrator mode:"{*}Enable-WindowsOptionalFeature Online FeatureName Microsoft-Windows-Subsystem-Linux{*}". It takes few seconds and will prompt you to restart your computer. # After restarting, open the command prompt in administrator mode and run: "{*}fsutil.exe file SetCaseSensitiveInfo <YourDestinationFolder> enable{*}" where <YourDestinationFolder> is the folder to enable the case sensitive. # Install S32DS and RTD test environment into the above working folders (from step 1). # Ensure all subfolders inside working folder (from step 1) are renew (re-created, re-layout, re-generated,...) after step 3. # Smoke check by building a development test/examples. Hint: # To check the status of case sensitive for the folder: "fsutil.exe file {*}query{*}CaseSensitiveInfo <YourDestinationFolder>". # To disable the case sensitive: "fsutil.exe file {*}Set{*}CaseSensitiveInfo <YourDestinationFolder> {*}disable{*}". # We can enable the case sensitive only the folders that contain the information released to the customers: "../output/eclipse/plugins" folder and "../PlatformSDK_<NPI>" folders
ARTD-142162	Bug	[Spi] DSPI IP does not support 64-bit frames Detailed description (how to reproduce it): Setup frame size is 64 bits by call function Dspi_Ip_UpdateFrameSize. Then transfer 40 bytes expect will transfer 5 frame size 64 bit. But driver transfer 5 frame size 32 bit. Preconditions: frame size 64 bits Test Case ID (internal TC that caught the defect) optional: Ip_Dspi_TC_FCT_1101 Observed behavior: transfer 5 frame size 32 bit. Expected behavior: transfer 5 frame size 64 bit Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-142172	Bug	[S32K3xx_S32M27x_5.0.0] Inconsistent between EB and CT when configuring pin as analog mode Detailed description (how to reproduce it): 1. Create new project on EB, CT 2. add pin and config pin as analog mode 3 Enable PortPinPue, PortPinPus, PortPinDse, PortPinPke, PortPinIfe, PortPinSlewRate E.g MSCR 32 mode ADC4_ADC4_S10_IN S32K396 !image-2024-07-30-11-37-21-663.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Port_TS_004 Observed behavior: on EB: PUE, PUS, DSE, PKE, IFE, SRE bit: Disable on CT: PUE, PUS, DSE, PKE, IFE, SRE bit: Enable !image-2024-07-30-11-30-42-347.png!

ID	Subtype	Headline and Description
		Expected behavior: The code generated on EB and CT is consistent. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-142229	Bug	[S32K3XX_S32M27x_5.0.0][DIO]: The number of available pins differs between EB and S32DS on some sub derivaties Detailed description (how to reproduce it): on some sub-derivaties the number of pins available on the S32DS is different from the number of pins available on the EB. EX: on sub-derivative s32k394_lqfp176 The number of pins available in the resource and on EB is 191 !image-2024-07-30-15-39-43-609.png! The number of pins available on S32DS !image-2024-07-30-15-41-17-188.png|width=561,height=305! The number of partitions on the channel is more than the number of available pins !image-2024-07-30-16-04-40-360.png! Preconditions: Sub-Derivatives: s32k394_lqfp176, s32k358_hdqfp172, s32k396_lqfp176 Dio: PVT_DIO_S32K3XX_S32M27X_RTM_5.0.0_006 Test_Dio: PVT_TEST_DIO_S32K3XX_M27X_500_V28 Test Case ID (internal TC that caught the defect) optional: compare_code_gen: Dio_TS_COT_002 Observed behavior: The number of available pins on S32DS is incorrect. Expected behavior: The number of pins available on the S32DS is correct as in the resource Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-142246	Bug	[S32K3XX_S32M27x_5.0.0][MEMACC]: MemAcc allows two cores to request mems jobs at the same time Detailed description (how to reproduce it): MemAcc allows two cores to request mems jobs at the same time Preconditions: Multicore type 3 Test Case ID (internal TC that caught the defect) optional: MemAcc_TS_100 Observed behavior: MemAcc only allows one core to request mems job at a time Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-142262	Bug	[Mem_INFLS] Update Mem_43_INFLS_Suspend/Mem_43_INFLS_Resume function to improve CCOV Detailed description (how to reproduce it): Mem_43_INFLS_Suspend/Mem_43_INFLS_Resume functions have redundant code. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_InFls_TC_FCT_0012 Observed behavior: Code in (MEM_43_INFLS_SUSPEND_RESUME_SUPPORT == STD_ON) !image-2024-07-30-17-20-18-959.png! Expected behavior: Std_ReturnType RetVal = E_MEM_SERVICE_NOT_AVAIL; return RetVal;

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-142335	Bug	[S32K3XX_S32M27x_5.0.0] Issue test fail run DMA2 with enable cache Detailed description (how to reproduce it): Fix issue for cache enable. I read data from fuction : "Mem_43_EEP_Ipw_CompareReadBuffer" storage at : u8ReadBuffer = (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, I see 16 bytes data at the end of buffer equal 0. But I disable cache in Systerm Control Register. Data buffer read is oki /*Enable Cache*/ !image-2024-07-31-09-31-19-417.png! /*Disable cache*/ !image-2024-07-31-09-34-28-734.png! Preconditions: Test Suite enable cache had failed. Test Case ID (internal TC that caught the defect) optional: Mem_Eep_TS_001 (Cfg_Set: CFG_SETS=5_tresos, 8_tresos, 11_tresos) Observed behavior: Test fail read Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-142431	Bug	[S32K3XX_S32M27x_5.0.0][SPI]: Can not update the parameters in SpiBaudrateConfig on EB with VariantPostBuild Detailed description (how to reproduce it): Users can not update these nodes with VariantPostBuild. !image-2024-07-31-17-57-18-355.png! !image-2024-07-31-15-32-11-325.png! Code generated: !image-2024-07-31-17-04-29-373.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Spi_TC_FCT_1001 Observed behavior: Can not update the parametes in SpiBaudrateConfig on EB with VariantPostBuild. Expected behavior: The parameters in SpiBaudrateConfig must be update correctly on EB with VariantPostBuild. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-142454	Bug	Mem_ExFls - compile errors when user mode enabled Detailed description (how to reproduce it): Dependencies: Steps to reproduce: # Configure Mem_ExFls with user mode enabled # Configure Os to support calling trusted function # Integrate trusted function calls following section 5.8 User mode support in IM document > warning in compiling as QSPI_IP_ENABLE_USER_MODE_SUPPORT not defined

ID	Subtype	Headline and Description
		Preconditions: n/a Test Case ID (internal TC that caught the defect) optional: Bundle_TS_UserMode Observed behavior: cannot compile the driver with user mode enabled Expected behavior: can compile without errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: n/a
ARTD-142537	Bug	[MEM_INFLS] Generation error in MEM_43_INFLS module if using MEMACC not provided by NXP Detailed description (how to reproduce it): When user add MemAcc config which is not provided by NXP, into Mem_Infls project, they cannot generate code and face below error: !Error.png! MemAccMulticoreType3Support parameter is not present in User MemAcc. In NXP MemAcc this parameter is present under AutosarExt(under non AUTOSAR parameter) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Cannot generate code in EB Tresos Expected behavior: User can use their MemAcc, as long as it comply Autosar spec Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to check if the node path exists before get value of MemAccMulticoreType3Support
ARTD-142540	Bug	[MEM_EXFLS] Generation error in MEM_43_INFLS module if using MEMACC not provided by NXP Detailed description (how to reproduce it): When user add MemAcc config which is not provided by NXP, into Mem_Exfls project, they cannot generate code and face below error: MemAccMulticoreType3Support parameter is not present in User MemAcc. In NXP MemAcc this parameter is present under AutosarExt(under non AUTOSAR parameter) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Cannot generate code in EB Tresos Expected behavior: User can use their MemAcc, as long as it comply Autosar spec Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to check if the node path exists before get value of MemAccMulticoreType3Support
ARTD-142547	Bug	[MEM_EEP]Cloned: Generation error in MEM_43_INFLS module if using MEMACC not provided by NXP Detailed description (how to reproduce it): When user add MemAcc config which is not provided by NXP, into Mem_Infls project, they cannot generate code and face below error: !Error.png! MemAccMulticoreType3Support parameter is not present in User MemAcc. In NXP MemAcc this parameter is present under AutosarExt(under non AUTOSAR parameter) Preconditions: N/A

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Cannot generate code in EB Tresos Expected behavior: User can use their MemAcc, as long as it comply Autosar spec Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to check if the node path exists before get value of MemAccMulticoreType3Support
ARTD-142674	Bug	[S32K3XX_S32M27x_5.0.0][MCL]: Missing requirement CPR_RTD_01182.mcl for Lcu module Detailed description (how to reproduce it): [Pending interrupt flags shall be cleared before enabling interrupts. Rationale: If the interrupt flag was set by a spurious event enabling the interrupt will cause an unwanted interrupt event. ID: 267 Req ID: CPR_RTD_01182.mcl] Preconditions: [] Test Case ID (internal TC that caught the defect) optional: [Mcl_TS_024] Observed behavior: [requirement hasn't covered yet] Expected behavior: [requirement covered by test code] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: []
ARTD-142699	Bug	[S32K3XX_S32M27x_5.0.0][PORT]: Incorrect MUX signal select for some mode cause build fail on S32K388 Detailed description (how to reproduce it): Example for Mode GMAC1_GMAC1_RGMII_TXCTL_OUT (MSCR 107), in S32CT is generating with {*}mux = PORT_MUX_AS_GPIO{*}, it have to PORT_MUX_ALT8 like Pintools. !image-2024-08-02-12-33-23-613.png|width=883,height=427! !image-2024-08-02-12-34-16-108.png|width=950,height=471! Preconditions: PVT_PORT_S32K3XX_S32M27X_RTM_5.0.0_011 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The Mux of Alt mode have to correctly
ARTD-142856	Bug	[S32K3XX] [DIO] Wrong information remark in FMEA Detailed description (how to reproduce it): In FMEA report, wrong chapters are referred in 6.1 Safety paths are affected in FMEA. !image-2024-08-05-11-16-58-427.png|width=801,height=267! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A

ID	Subtype	Headline and Description
		Observed behavior: N/A Expected behavior: Update FMEA report. Correct information. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-142896	Bug	[S32K3XX_S32M27x_5.0.0] Mising VendorApiInfix in ECVD file Detailed description (how to reproduce it): Checking the ECVD file on the S32DS config and the ECVD file when importing EPC from EB to S32DS Preconditions: DIO: PVT_DIO_S32K3XX_S32M27X_RTM_5.0.0_010 PORT: PVT_PORT_S32K3XX_S32M27X_RTM_5.0.0_011 DIO_ITG: PVT_TEST_DIO_S32K3XX_M27X_500_V34 PORT_ITG: PVT_TEST_PORT_S32K3XX_M27X_500_V30 Test Case ID (internal TC that caught the defect) optional: Dio: Dio_TS_ECPD_001 Observed behavior: Issue 1: Dio component Mising VendorApiInfix in ECVD file !image-2024-08-05-15-01-04-360.png! Issue 2: Port component SYNC_SIZE and SYNC_VALUE options appear together in VendorApiInfix (Port.component) !image-2024-08-05-14-44-37-988.png! Expected behavior: full VendorApiInfix information in ECVD file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-143175	Bug	[S32K3XX_S32M27x_5.0.0][DIO][PORT]: Incorrect jump information in board of example test Detailed description (how to reproduce it): Perform example test. Check readme (EB), description (S32DS) file and check information on boards. Preconditions: DIO: PVT_DIO_S32K3XX_S32M27X_RTM_5.0.0_010 PORT: PVT_PORT_S32K3XX_S32M27X_RTM_5.0.0_011 Test Case ID (internal TC that caught the defect) optional: EX: Dio: Dio_Example_S32K358 Port: Port_Example_S32K358 Observed behavior: 1. derivative S32K358 JTAG Cortex Debug on board is J365 20-pin but the information in the readme file is J205 20-pin and j281 and j617 are also not on the board of derivative S32K358. in readme and description file !image-2024-08-06-15-15-15-550.png! 2. derivative S32K388 J71.2 is not on board !image-2024-08-06-15-48-07-901.png|width=618,height=175! Expected behavior: correct jump information Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional
ARTD-143178	New Feature	[S32K3XX_S32M27x_5.0.0][MCU]: Remove "inlude "Mcal.h"" in "Clock_Ip_Type.h" NewWorkDescription: Remove "{*}inlude "Mcal.h"{*}" in "{*}Clock_Ip_Type.h{*}" to check Trusted function from testing side

ID	Subtype	Headline and Description
		Remove "{*}uint32{*}" in OsIf_Trusted_Call_Return((uint32)Power_Ip_MC_RGM_GetResetReason) to fix build fail when use OsIfAutosarOsType
ARTD-143186	Bug	[S32K3XX_S32M27x_5.0.0][MEMACC]: The initial value for the variable containing the sema4 chanel was not initialized successfully. Detailed description (how to reproduce it): The initial value for the variable containing the sema4 chanel was not initialized successfully. Preconditions: compile: iar test type: multicore type 1 Test Case ID (internal TC that caught the defect) optional: MemAcc_TS_090 MemAcc_TS_110 Observed behavior: Memacc_u8Sema4Gate is located in the bss region. All initial values are 0. !image-2024-08-06-17-23-03-745.png|thumbnail! Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-143423	Bug	[MemAcc] Fix violations with Plugin Check Detailed description (how to reproduce it): There are duplicate UUID tags in xdm file: !image-2024-08-08-08-36-12-361.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Fixed all violations Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change UUID
ARTD-143629	Bug	[S32K3XX_S32M27x_5.0.0][PORT]: Fix the MISRA C-2012 Rule 8.5 : Symbol "Siul2_Port_Ip_SetUserAccessAllowed" is declared more than once. Detailed description (how to reproduce it): Symbol "Siul2_Port_Ip_SetUserAccessAllowed" is declared more than once. !image-2024-08-09-10-33-57-062.png|width=904,height=391! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Fix the Misra violation Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-143861	Bug	[Mem_INFLS] C40_Ip_EccLogicCheck canot return C40_IP_STATUS_ECC_CORRECTED Detailed description (how to reproduce it): C40_Ip_EccLogicCheck cannot return C40_IP_STATUS_ECC_CORRECTED on S32K388, toolchain Diab Preconditions:

ID	Subtype	Headline and Description
		N/A Test Case ID (internal TC that caught the defect) optional: Mem_InFls_TC_FCT_0028 Observed behavior: N/A Expected behavior: Update MCAL_DATA_SYNC_BARRIER; MCAL_INSTRUCTION_SYNC_BARRIER before read in C40_Ip_EccLogicCheck. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-145518	Bug	Unnessessary Casting whan calling Power_Ip_MC_RGM_GetResetReason with UserMode support enabled Detailed description (how to reproduce it): [following issue when enabling User Mode Support for Mcu driver: After we have enabled User Mode Support by the relevant configuration option, the following line in file: Power_Ip.c became effective: ResetReason = (Power_Ip_ResetType)OsIf_Trusted_Call_Return((uint32)Power_Ip_MC_RGM_GetResetReason); — Which expands to: ResetReason = (Power_Ip_ResetType)Call_(uint32)Power_Ip_MC_RGM_GetResetReason_TRUSTED(); Which is giving the following errors and warning at compilation: ResetReason = (Power_Ip_ResetType)Call_Power_Ip_MC_RGM_GetResetReason();_ "C:\Brose\laraarc\EE\Workspaces\Brose_shm_08\SW_bmw_shm_08_scu\E_nxp_s32k3_mcal\eclipse\plugins\Mcu_TS_T40D34M20I0R0\src\Power_Ip.c",556 Warning[Pe1665]: concatenation with "(" in macro "OsIf_Trusted_Call_Return" does not create a valid token — ResetReason = (Power_Ip_ResetType)Call_Power_Ip_MC_RGM_GetResetReason();_ "C:\Brose\laraarc\EE\Workspaces\Brose_shm_08\SW_bmw_shm_08_scu\E_nxp_s32k3_mcal\eclipse\plugins\Mcu_TS_T40D34M20I0R0\src\Power_Ip.c",556 Error[Pe254]: type name is not allowed — ResetReason = (Power_Ip_ResetType)Call_Power_Ip_MC_RGM_GetResetReason();_ "C:\Brose\laraarc\EE\Workspaces\Brose_shm_08\SW_bmw_shm_08_scu\E_nxp_s32k3_mcal\eclipse\plugins\Mcu_TS_T40D34M20I0R0\src\Power_Ip.c",556 Error[Pe065]: expected a ";" — It seems the problem is the seems to be unnecessary casting: ResetReason = (Power_Ip_ResetType)OsIf_Trusted_Call_Return({*}(uint32){*}Power_Ip_MC_RGM_GetResetReason); — When the casting is removed the errors does not pop up at compilation anymore. This is blocker for our customer's urgent Functional Safety delivery]

ID	Subtype	Headline and Description
		Preconditions: [user mode support enabled] Test Case ID (internal TC that caught the defect) optional: [-] Observed behavior: [compilation error/warning] Expected behavior: [no compilation error/warning] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [remove casting]
ARTD-145634	Bug	[AE] [S32K3_M27x 5.0.0]: Frame counter issues Detailed description (how to reproduce it): Issue 1: if a fault occurs, the Framecount in GHS will be reset but with the current implementation, the variable Aec_Ip_u32FrameCounter is not reset. Frame Count Error will be raised and the program will jump to Frame Count callback (if enabled) in every SPI read or write. In my point of view, this is not an expected behavior or we shall provide an option on configuration interface (EB/CT) for users to decide to reset Aec_Ip_u32FrameCounter or not Issue 2: After a Frame Count Fault is raised and handled, Aec_Ip_u32FrameCounter and Frame Count in GHS should be the same (The same as clearing the interrupt flag). If not, the program will jump to callback in every SPI read/write and the next fault can not be handled. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: [Ae_TC_FCT_0501|https://bitbucket.sw.nxp.com/projects/ARTD/repos/test_ae/browse/generic/src/Ae_TC_FCT_0501.c] Observed behavior: Aec_Ip_u32FrameCounter is not reset after faults occur Expected behavior: Aec_Ip_u32FrameCounter is reset after faults occur Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-146200	New Feature	[Mem_ExFls][S32K3 5.0.0] Add support for HyperRAM NewWorkDescription: Add support for HyperRAM memory on S32K3XX. Add Example for HyperRam Update UM/IM for HyperRam support Requirement source: CPRD: New requirement should be added. (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support for HyperRAM at Init time so that the customers can access it via the AHB bus. Test it on S27KL0642 memory on the customer custom board.
ARTD-146586	New Feature	[IMPLEMENTATION] S32K3: Async vs Sync Mode on Spi Driver The S32K3 SPI driver that we provide is supposed to be Level 2 AUTOSAR compliant !MicrosoftTeams-image.png|width=532,height=141! Level 2 means that the controller can handle both asynchronous and synchronous transmissions. However, this is partially true with our S32K3 SPI driver, as we can handle asynchronous and synchronous transmissions as long as we set two different SPI channels. Don't be confused with the mechanism. One thing is the mode (asynchronous or synchronization) and another thing is the mechanism (polling or interrupt). The problem is with the mode, not in the mechanism. In summary, SPI driver can handle 3 modes: Sync Mode Async Mode Interrupt Async Mode Polling However, with the current driver implementation: If SPI0 is configured in Sync Mode... we cannot use the AsyncTransmit() function If SPI0 is configured in Async Mode... we can do both interrupt and polling in runtime. But we cannot use SyncTransmit() function

ID	Subtype	Headline and Description
		The reason why... is because of the SpiPhyUnitSync parameter in Tresos/ConfigTools. When the user calls the function Spi_AsyncTransmit() or Spi_SyncTransmit().... there is a check in the functions to see if the channel is configured as Sync or Async. This is preventing the customer for using Async and Sync calls on the same SPI channel !image.png|width=538,height=197! The request/update is to remove the SpiPhyUnitSync parameter as this is obsolete since Autosar 4.3 !image (1).png|width=479,height=341!
ARTD-146767	Bug	[mcl] Removed definitions to be manually added fpr successful build Detailed description (how to reproduce it): [rated as high prio due to upcoming SW freeze at customer. While updating the MCAL from RTD 2.0.0 to RTD 4.0.0 P24 Brose has faced some issues during compilation and, they had to patch the generated code for the successful build. Issue # 1 Mcl Build Error: Error[Pe020]: identifier "Emios_Mcl_Ip_0_MasterBusConfig" is undefined Following definitions were removed from Emios_Mcl_Ip_PBcfg.h and I had to add them manually in the file. / Emios channel configuration / extern const Emios_Ip_MasterBusConfigType Emios_Mcl_Ip_0_MasterBusConfig[1U]; / Emios channel configuration / extern const Emios_Ip_MasterBusConfigType Emios_Mcl_Ip_1_MasterBusConfig[1U]; I suspect it is because of the new change in the generator of Emios_Mcl_Ip_PBcfg.h. In my opinion, the reference to the EmiosMclMasterBus shall be “MclConfig/EmiosCommon/{*}/EmiosMclMasterBus/{*}”. This could be the reason why the MasterBus configs are not generated. Previously this condition did not exist. !image-2024-09-06-21-15-55-673.png! Preconditions: [no] Test Case ID (internal TC that caught the defect) optional: [no] Observed behavior: [see above] Expected behavior: [no compilation error due to missing definitions] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-147259	Bug	[S32K3] OsIf Systick with FreeRTOS compile error Detailed description (how to reproduce it): Compiling error in the OsIf_Timer_System_Internal_Systick.c with FreeRTOS. !image-2024-09-12-11-10-44-274.png! Preconditions: Configure Base to work with FreeRTOS: !image-2024-09-12-11-13-17-830.png! Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Compile failed Expected behavior: Compile passed. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: Change in Oslf_Timer_System_Internal_Systick..h file : #include "FreeRTOSConfig.h" with #include "FreeRTOS.h"

4.3 Change List for 4.0.0.P14

ID	Subtype	Headline and Description
ARTD-105646	Bug	[PWM][PWM_ETPU] function "Eptu_Pwm_Ip_IrqHandler" has no prototype when build on IAR compiler Detailed description (how to reproduce it): function "Eptu_Pwm_Ip_IrqHandler" has no prototype when build on IAR compiler !image-2023-12-18-16-05-30-354.png|width=689,height=45! Preconditions: Build on IAR compiler Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: build fail test with IAR compiler Expected behavior: Add "Eptu_Pwm_Ip_IrqHandler" function prototype => build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-114127	Bug	[PWM][PWM_ETPU] Missing resources on other derivative S32K396_289 Pins Detailed description (how to reproduce it): I am configuring test build only with derivative {*}s32k396_lqfp176{*}. When I generate a test with the derivative s32k396_lqfp176, the error shown below appears: !image-2024-03-06-19-37-54-365.png|width=533,height=178! These resources are only available for derivative s32k396_mapbga289 but are not available for other derivatives. Please add more resources for other derivatives (at least add derivative {*}s32k396_lqfp176{*}) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Pwm_TS_COT_002 Observed behavior: Gen build fail with other derivative s32k396_mapbga289 Expected behavior: Gen Build Pass with other derivative {*}s32k396_mapbga289{*}{*}{*} Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional
ARTD-114272	Bug	[PWM] Tresos generation errors Detailed description (how to reproduce it): Generate tresos configuration for RTD Preconditions: Derivative is set to K396 Test Case ID (internal TC that caught the defect) optional: Bundle_TC_001 Observed behavior: PWM code generation fails: !image-2024-03-07-11-21-45-281.png! Expected behavior: No errors

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-114360	Bug	[PWM][ETPU] Output signal fails when set Period is greater than 16 bits and Duty is 100% Detailed description (how to reproduce it): Period is set in the range (0 16777214) (24bit) When t set period = 16777214 , and expect DutyCycle = 100% Then the Duty value stored in the array aEtpu_Pwm_Ip_DutyCycle is 16777214 (24bit) !image-2024-03-08-14-03-21-095.png|width=730,height=57! However, the array's data type is uint16 !image-2024-03-08-14-05-07-984.png|width=458,height=54! This causes the duty value stored in the array to overflow when the period value is greater than 16 bits Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The duty value written to the array overflows when the period value is greater than 16 bits Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change the data type of aEtpu_Pwm_Ip_DutyCycle array from uint16 > uint32 or uint64 !image-2024-03-08-14-14-58-388.png|width=466,height=49! !image-2024-03-08-14-17-43-973.png!
ARTD-114595	Bug	[ETPU] Build fails on 2 compilers ghs and iar Detailed description (how to reproduce it): Build fail occurs with tests using interrupts (iar , ghs complilers) !image-2024-03-11-17-05-14-725.png|width=517,height=201! This error is because the ISR() macro has not been defined You can include Osif_Internal.h or Osif.h to define the ISR macro Preconditions: Test using interrupt on CT Build on iar and ghs compilers Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Build fail on 2 compilers IAR and GHS Expected behavior: Build Pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Include Osif_Internal.h or Osif.h to define the ISR macro
ARTD-115962	Bug	[pwm] Errors of missing Etpu resources when generate example of PWM Detailed description (how to reproduce it): generate example K344/K358/K388 Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Errors of missing resources of eTPU Expected behavior: No errors when generate examples for K344/K358/K388

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-115533	Bug	[PWM][ETPU] Resource for driver is unavailable Detailed description (how to reproduce it): Customer input on community : I have an issue with latest MCAL versions SW32K3_S32M27x_RTD_4.4_4.0.0_P11/ SW32K3_S32M27x_RTD_R21-11_4.0.0_P12. I try to generate Pwm, but fail with the error message: Parsing file "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY58455\external\ThirdParty\Mcal_S32k\Supply\tresos\plugins \Pwm_TS_T40D34M40I0R0/generate_PB/Etpu_Pwm_Ip_RegOperations.m (signed)", line "133" The XPath-expression "ecu:get('Etpu.SDMAddressStart')" caused an error: (35010) The requested ECU resource property "Etpu.SDMAddressStart" does not exist Preconditions: Use PWM driver in configuration Test Case ID (internal TC that caught the defect) - optional: NA Observed behavior: Issue on generation - resource not available Expected behavior: Generation complete Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution - optional: NA

4.4 Change List for 4.0.0 P12

ID	Subtype	Headline and Description
ARTD-29004	New Feature	[SPI] Support DSPI IP on S32K396 NewWorkDescription: Support DSPI IP on S32K396 Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support DSPI IP on S32K396
ARTD-111090	Bug	[CRYPTO_NG] Can't generate Crypto_43_HSE_Cfg.c from EPD project Detailed description (how to reproduce it): Tag Crypto Sec: PVT_CRYPTO_SEC_NG_SAF85_SAF86_S32R41_V009 Can't generate Crypto_43_HSE_Cfg.c from EPD project: In test case Crypto_TS_E01, we need to generate all Cfg.h files and Cfg.c files separately from XDM project and EPD project using 1 Crypto_43_HSE config and compare them together to make sure they are the same. With this bug, we can't generate Crypto_43_HSE_Cfg.c. Test Case ID (internal TC that caught the defect) optional: Crypto_TS_E01 Observed behavior:*_ !image-2024-02-01-15-04-46-463.png! Expected behavior:*_ All Cfg.h files and Cfg.c files from XDM project and EPD project should be generated successfully and those from XDM project should be the same with those from EPD project. Note:* in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-111629	New Feature	[PWM] Add necessary files for eTPU integration on patch release line NewWorkDescription: In order to have eTPU integrated over RTD patch release, the RTE and Base have to offer support for the eTPU required files, as below: The list of eTPU related changes in RTD drivers which needs to be part release:

ID	Subtype	Headline and Description
		1. [base|https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/browse] MotorControl_MemMap.h, Etpu_MemMap.h and RdcChecker_MemMap.h files as seen on: [base/browse/generic/include|https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/browse/generic/include] Added files shall be incorporated into [base/specific/S32K3XX/Base.mak|https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/browse/specific/S32K3XX/Base.mak] 2. [rte|https://bitbucket.sw.nxp.com/projects/ARTD/repos/rte/browse] SchM_Etpu.h, SchM_Motor_control.h, SchM_Rdc_checker.h as seen on [rte/generic/include|https://bitbucket.sw.nxp.com/projects/ARTD/repos/rte/browse/generic/include] SchM_Etpu.c, SchM_Motor_control.c, SchM_Rdc_checker.c as seen on [rte/generic/src|https://bitbucket.sw.nxp.com/projects/ARTD/repos/rte/browse/generic/src] Added files shall be incorporated into [rte/specific/S32K3XX/Rte.mak|https://bitbucket.sw.nxp.com/projects/ARTD/repos/rte/browse/specific/S32K3XX/Rte.mak] Please note all these changes are already done on develop, but have to be integrated in release branch that will be released in BLN_RTD_4.7_S32K3XX_S32M27x_4.0.0_P12 Requirement source: Dependency (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-112171	Bug	[BASE][S32K3] PUSHR register of S32K39_DSPI should be split into TX FIFO and CMD FIFO according to Reference manual description Detailed description (how to reproduce it): PUSHR(32bit) register of S32K39_DSPI should be split into TX FIFO(16bit) and CMD FIFO(16bit) according to Reference manual description. Additionally, same IP type on S32ZE also split PUSHR register Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: PUSHR register was not spitted to FIFO.TX and FIFO.CMD Expected behavior: PUSHR register is spitted to FIFO.TX and FIFO.CMD Note:* in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-111054	Bug	[Spi] Driver can be buildable when SpiDMAFastTransfer is not enable but the SpiMaxFastTransfer have the value. Detailed description (how to reproduce it): Driver should be buildable when SpiDMAFastTransfer is not enable but the SpiMaxFastTransfer have the value. Preconditions: NA Test Case ID (internal TC that caught the defect) - optional: NA Observed behavior: Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution - optional: NA
ARTD-105357	Bug	[memacc] Remove Duplicated MemSectorBatch check NewWorkDescription: Memacc config forbids 2 sub-areas to use the same sector batch, issuing this error: "Duplicated MemSectorBatch between sub address areas" I think this should be removed, it should be allowed to refer the same sector batch twice, for example if an application wants to use sectors 1, 2, 10, 11 of the same sector batch. Then it will need two sub-areas, 2 sectors each, pointing to the same batch but different sector offset Requirement source:

ID	Subtype	Headline and Description
		Proposed solution - optional:
ARTD-114023	Bug	[CRYPTO_NG] Update FMEA for Crypto_ProcessJob Detailed description (how to reproduce it): Update FMEA section 1 with the case of Crypto_ProcessJob() mentioned by safety assessor. Preconditions: NA Test Case ID (internal TC that caught the defect) - optional: NA Observed behavior: NA Expected behavior: The case should be detailed in FMEA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution - optional: Additional Information test that covers the topic CRYPTO_TC_FCT_0047 test specification (see chapter 4.48.2) RTD_CRYPTO_TS 1.pdf https://bitbucket.sw.nxp.com/projects/ARTD/repos/test_crypto_ng/browse/generic/src/Crypto_TC_FCT_0047.c

4.5 Change List for 4.0.0

ID	Subtype	Headline and Description
ARTD-6356	Bug	[mcu] Cannot enable CMU_FC_5 interrupts Cannot enable CMU_FC_5 interrupts. I am using the second configuration, enabled CMU_FC_5 FHH and FLL asynchronous interrupts. But register was not updated !image-2021-01-15-14-40-01-089.png|width=885,height=483!
ARTD-9657	New Feature	[BUILD_ENV] Create a .dox page for all IMs to clarify the OsIf timeout approach NewWorkDescription: Clarify for the users the OS initialization issue (sys timers not available before OS is initialized) and their options. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create a .dox page to clarify the OsIf timeout approach and modify the ToC in rtd_docgen so that it will be automatically included by all IMs.
ARTD-14171	New Feature	[CRYPTO]AES XTS Support NewWorkDescription: Implement AES XTS encryption and decryption for S32G2 because HSE Firmware supports the cipher via {{HSE_SRV_ID_XTS_AES_CIPHER}} service and hseXtsAesCipherSrv_t }}structure. The Autosar 4.4.0 maps as follows the AES XTS service: !image-2021-07-19-17-31-39-964.png! Requirement source: Autosar 4.4.0 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-14689	New Feature	[CRC][Optimize] Remove runtime configuration for the channels NewWorkDescription: The CRC driver needs optimizations for bit reversal and table/software calculation. Proposed solution optional: 3. Remove runtime configuration for the channels, channel configuration shall be static. (maybe maintain runtime configuration only for Logic Channels configured in hardware mode.)
ARTD-17521	New Feature	[ICU][S32K3XX] Improve ICU CCOV index for S32K3XX NewWorkDescription: Improve code coverage GPT for S32K3XX 4.4 RTM 2.0.0 for comment 3:

ID	Subtype	Headline and Description
		(3) Technically feasible: This statement/branch has not been reached, and test improvement is needed Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-19536	Bug	[S32XX][PORT] Port driver have to add some Det_reportError function following requirement Detailed description (how to reproduce it): If Det is enabled, some function shall report specify error and return without any other action. Detail: CPR_RTD_00423.port: The function Port_ResetPinMode shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00426.port*: The function Port_SetAsUnusedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00428.port*: The function Port_SetAsUsedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. SWS_Port_00223: The function Port_SetPinMode shall reportPORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Port driver should add some Det_reportError function with specify error following the requirement in Detailed Description.
ARTD-23856	New Feature	[PORT] Add several key functions for 1st phase evaluation of K3 SW Touch Sense Solution NewWorkDescription: The Software for Self-Capacitance Touch Sense Solution shall be ported on S32K3 RTD and evaluated (just like it was done with Motor Control). Before creating any specific drivers, I want to evaluate the performance of current RTD low level drivers when running the Touch Sense self-capacitance app. To be able to do that, I would need the RTD team to add several functions into specific drivers (adc, siul and tspc). Requirement source: GPIS Solution Team Proposed solution optional: Please see attached ppt with required functions to be added.
ARTD-25304	New Feature	[CRYPTO] Add support for HashEdDSA(ED25519ph) NewWorkDescription: Add support in the existing signature generation and verification code for HashEdDSA(ED25519ph). The HSE firmware supports this service via bHashEddsa parameter: !image-2022-03-23-15-42-11-081.png! Autosar specification does not support this service so an extension to the Crypto_AlgorithmFamilyType must be made by adding a new define like CRYPTO_ALGOFAM_ED25519PF. !image-2022-03-23-15-44-25-331.png! In the internal function Crypto_Hse_FillSignRequestDescriptor() the HSE descriptor must be filled in accord with the primitive configured in the job: !image-2022-03-23-15-39-59-535.png! Requirement source: Customer (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:

ID	Subtype	Headline and Description
		Update the configuration with a new Crypto_AlgorithmFamilyType that represent the service and the code in order to fill the descriptor accordingly.
ARTD-25932	New Feature	[BASE][S32DS] Remove the reference clock from BaseNXP in IPL to Mcu/EcuC in HLD Detailed description (how to reproduce it): S32DS: Get rid of the reference clock from BaseNXP in IPL to Mcu/EcuC in HLD. !image-2022-04-15-16-45-54-723.png! {_}*Preconditions:*{_}{*}{*} Test Case ID (internal TC that caught the defect) optional: Observed behavior: The component from IPL depends on the other in HLD Expected behavior: The component from IPL can work independently, without any reference from HLD.{*}{*} Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-26343	New Feature	[SPI] Could SPI driver update TX/RX buffer address directly when a transfer has completed? Similar with UART driver. NewWorkDescription: [Customer used RTD IPL driver and the SPI worked in slave mode with DMA. Customer feedback the large time cost between 2 SPI transfer. They call Lpspi_Ip_AsyncTransmit() in callback to start next transfer. They only want to update the TX/RX buffer address but the IPL Transmit_ api will re-configure the whole module, it costs time. The IPL API Lpspi_Ip_AsyncTransmit()_ cost much time. In UART driver, we could call SetTxBuffer() in callback {_}CompleteSendUsingDma{_}() to update the tx buffer and start the next transfer directly. It saves time. It seems that there isn`t any similar API to implement this feature in SPI driver. The TxDmaContinueTransfer()_ in SPI driver couldn`t update the buffer. Update/Clarification: Performance improvement requested between two transfers: 2us (the shorter the better) Update: Customer uses only IP Layer Update: Customer needs to change the Tx Buffer address between two transfers. Address of Rx buffer is already fixed in place before we start the transfer. Customers uses the DMA. Update: Customer uses only slave mode in this use case. Update: Customer SPI use case: Continuous CS, 8B per frame, Datawidth=8bit] Requirement source: [Customer wish a SPI api which is similar with SetTxBuffer()_ in UART to only update buffer address when a transmission is completed instead of calling Transmit api. Or optimize Lpspi_Ip_AsyncTransmit() execution efficiency.]
ARTD-26361	New Feature	[icu] Emios ICU overflow notification There is a request from EINFOCHIPS to support overflow detection is other ICU modes such as Edge Detect. The RTD description says: !image-2022-05-09-13-27-26-453.png|thumbnail! But as the attached test project shows, we can have MCB BUS A overflow interrupt even with the Edge detect mode. Can it be added? Also, why the description says this? !image-2022-05-09-13-29-28-208.png|thumbnail! While we can have real-time overflow notification the HW allows that, and it works in my test project.
ARTD-26639	Bug	[Mcu] [S32DS] Name of McuModeSettingConf is generated as hardcode Detailed description (how to reproduce it): If user renamed of Functional groups in ClockTool (equivalent with node Name of McuModeSettingConf), it will not generated as expectation. !image-2022-05-20-16-56-43-735.png! This name will be used as parameter of Mcu_InitClock Api. Currently, driver is generating the hard code as below (in Mcu_Cfg.h) !image-2022-05-20-16-59-34-235.png! Preconditions: Renamed McuClockSettingConfig and try to use that name in Mcu_InitClock

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Driver is hardcoding the name of McuClockSettingConfig Expected behavior: Should use name of node instead hardcoding Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-28058	Bug	[MCU]: The last mile regulator auto turn over enable bit will be cleared in default Detailed description (how to reproduce it): The last mile regulator auto turn over enable bit will be cleared in default, it is caused by the following two items: !image-2022-06-23-17-10-11-226.png! !image-2022-06-23-17-10-19-474.png! If customer didn't care this two items and keep it in default status, the code will clear the PMC CONFIG register, at such case, it have risk to damage the MCU. because commonly use's project work on PLL which with high speed. by the way, another suggestion is that we'd better check the runtime clock and the LMEN bit status. detail information, please refer to the RM. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: MCU HW have the risk to damage Expected behavior: None Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-29209	Bug	[DIO] Investigate the violations from CWEReport Detailed description (how to reproduce it): There are 2 violations were found in the RTD_DIO_CWEReport. Please come to see the attachment for more details Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There are 2 violations were found in the RTD_DIO_CWEReport. Please come to see the attachment for more details Expected behavior: All the violations need to be fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-35215	New Feature	[UART] - Support custom baudrate values NewWorkDescription: In configurator, create a new configuration where user can choose values of the OSR, DIV in order to set the desired baudrate value. The configuration must show the calculated value, and must throw errors in case of an wrong setting. Requirement source: Customer Request Proposed solution optional:

ID	Subtype	Headline and Description
ARTD-35228	New Feature	[ADC] Multicore support for BCTUs Detailed description (how to reproduce it): BCTU doesn't support multicore at the moment Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-38119	Bug	[GMAC][SAF85xx] Fatal Bus Error detected when receiving Eth frame at high throughput Detailed description (how to reproduce it): Ensure RFE firmware available since RFE_PLL needed then load and run provided elf file for cortex-A53. On Ubuntu machine: Open serial terminal to communicate with the board, for eg: python m serial.tools.miniterm raw <USB port> 115200 These message should display (type Enter if not): !image-2022-09-10-22-09-28-232.png|width=543,height=58! Then, type zperf udp download and Enter: !image-2022-09-10-22-10-35-289.png|width=396,height=189! Open another terminal on the machine and type: iperf c 192.0.2.3 u l 1470 b 200M Wait until this message is appeared: !image-2022-09-10-22-40-58-663.png|width=687,height=186! Checking DMA_CH0_Status register: !image-2022-09-10-22-14-13-830.png|width=638,height=137! Preconditions: Board X-STRX-DIGSKT-V1: Ensure PHY AR8033 is connected Ensure UART can be used to communicate with other devices (for e.g over microUSB port on board). Ubuntu machine: There is at least one unused ethernet port on Ubuntu machine which can be used to connect to the board. Download and install iperf 2.0.5. Download/install a software (for e.g [pyserial|https://pypi.org/project/pyserial/]) for UART communication between board and the machine Connect the ethernet port with RJ45 port on the board. - Connect microUSB port on the board to USB port on the machine Test Case ID (internal TC that caught the defect) optional: Observed behavior: When receiving throughput big enough (for eg. 200 Mbps), a fatal bus error occurs on receive path. Source code under rx callback, basically just read a eth frame, provide the new buffer for GMAC driver and move frame to higher layer on network stack: !image-2022-09-10-22-18-11-885.png|width=493,height=287!

ID	Subtype	Headline and Description
		Expected behavior: The error is not happen and the throughput can be measured, for eg with 100Mbps ({*}iperf c 192.0.2.3 u l 1470 b 100M{*}): !image-2022-09-10-22-42-15-619.png|width=607,height=167! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-38632	Bug	[Dio] S32DS doesn't raise an error when naming two Channel Group Identification that are similar. Detailed description (how to reproduce it): at port 0: !screenshot-1.png|thumbnail! at port 1: !screenshot-2.png|thumbnail! Dio Channel Group Indentification are similar names. But S32DS doesn't raise an error. Preconditions: Make a new S32Z project, add Dio, and configure as described above. Test Case ID (internal TC that caught the defect) optional: Dio_TC_COT_201 Observed behavior: Like above Expected behavior:*. An error must be raised Proposed solution optional:
ARTD-40110	New Feature	HSE Authenticated Key Import configuration of Crypto driver The "Authenticated Key Import" configuration for the EB tresos is not friendly for use. The use case is key updating. In current implementation, the user needs to set the "Key Container Address" and the "Authentication Tag" in the EB tresos, It implies that: the user needs to allocate some memory at the Key Container Address, and need to construct a proper key container at the address. This is not very friendly to use. And the format of key container is not described in the UM. the auth tag of the container cannot be updated in runtime. For key updating, the user must know the value of the (opt. encrypted) new key at first. This is not reasonable for key updating at runtime. Not sure if the current implementation can be improved? the requirement: keys should be able to be updated in runtime
ARTD-40374	Bug	[MCL] Update generated Dma Ip Multicore configuration structure Detailed description (how to reproduce it): The generated structure that contains the Dma Ip Multicore configuration is partially initialized (menmber pMultiCoreDmaChannelConfig of the structure). !image-2022-09-28-14-56-32-963.png! There's also a MISRA warning: !image-2022-09-28-14-57-59-727.png! Preconditions: Enable multicore Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The array pMultiCoreDmaChannelConfig which is menmber of the structure Dma_Ip_MultiCoreConfigType Dma_Ip_MultiCoreConfig_VS_0 is partially initialized, depending on how many DMA logic channels are configured. Expected behavior: All array/structure members shall be intitialized. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Solution one: Keep current implementation but also initialize with zero the remaining members of the structure (the Dma logic channels that were not configured).

ID	Subtype	Headline and Description
		Solution two: Update the Dma_Ip_MultiCoreConfigType type : !image-2022-09-28-15-05-39-369.png! instead of const uint8 pMultiCoreDmaChannelConfig[DMA_IP_NOF_HWV3_CH]; a pointer shall be defined and the pMultiCoreDmaChannelConfig array shall be generated with the size of the DMA logic channels configured. At the initialization stage the Dma_Ip_MultiCoreConfigType structure for the second member will receive the address of the generated array.
ARTD-40410	Bug	[S32DS] Debug failed with NPW S32K396 attached RTD + IAR Toolchain RTD build: *The engineering drop build D2209 for RTD S32K396 CD02 with the updated core name: [https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? id=%2Fsites%2FZebra%2FShared%20Documents%2F00%2E%20DeliverableCenter %2FS32K3%2F3%2E0%2E0%20CD02%20%28S32K396%20CD02%29%2Fredrop%20S32DS %2FSW32K396%5FRTD%5F4%2E4%5F3%2E0%2E0%5FCD02%5FD2209%5Fupdatesite %2Ezip&parent=%2Fsites%2FZebra%2FShared%20Documents%2F00%2E%20DeliverableCenter %2FS32K3%2F3%2E0%2E0%20CD02%20%28S32K396%20CD02%29%2Fredrop%20S32DS] Test case 1: Detailed description (how to reproduce it): # Create a single K396 project to enable RTD with the IAR toolchain 8.50.10 # Select project > Open S32CT > change some config of Pin, Clock, Peripheral # Update code # Build the project with build config "{*}Debug_RAM{*}" # Debug project Observed behavior: 4. There is a warning displayed (see detailed on attached image) 5. The PC does not jump to main, stops at 0x0 Expected behavior: 4,5: Build and debug successfully without any errors, or warnings. Note: Build the project with build config "Debug" still have a warning but Debug with debug config "Debug" is successful and stops at main.c Test case 2: Detailed description (how to reproduce it): # Create project multicore K396 with enabling SDK S32CT with IAR toolchain 8.50.10 # Select boot core project > Open S32CT > change some config of Pin, Clock, Peripheral, DCD, IVT # Update code # Do step2-4 with all slave core project # Build the project with build config "{*}Debug_RAM{*}" # Debug project multicore Observed behavior: 5. There is a warning displayed (see detailed on attached image) 6. The PC does not jump to main, stops at "{*}HardFault_Handler()"{*} Expected behavior: 5,6: Build and debug successfully without any errors, or warnings. Note: Debug with Debug config "Debug" is failed.
ARTD-45025	New Feature	[LINTRCV] Implement wakeup functionality as per Autosar R21-11 NewWorkDescription: There are 3 Wakeup methods described in AUTOSAR_SWS_ECUStateManager. The sequence diagrams must be analyzed and have a conclusion on how to implement on the LinTrcv driver. Analyze also the impact on other modules. If any implementation is required, create tickets. Create dev test and test functionality. Revise the LinTrcv_SetWakeupMode which does not implement SWS_LinTrcv_00135 SWS_LinTrcv_00136 Requirement source: ASR SWS Proposed solution optional: [SWS_LinTrcv_00135] ⌈Enabled: If the function LinTrcv_SetWakeupMode is called with TrcvWakeupMode == LINTRCV_WUMODE_ENABLE and if the LinTrcv module has a stored wakeup event pending for the addressed bus, the LinTrcv module shall execute the notification within the API call or immediately after (depending on the implementation).⌋() [SWS_LinTrcv_00136] ⌈Disabled: If the function LinTrcv_SetWakeupMode is called with TrcvWakeupMode == LINTRCV_WUMODE_DISABLE, then the notifications for wakeup events are disabled on the addressed network. It is required by

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		the transceiver device and the underlying communication driver to detect the wakeup events and store it internally in order to raise the event when the wakeup notification is enabled again.]() [SWS_LinTrcv_00137] [Clear: If the function LinTrcv_SetWakeupMode is called with TrcvWakeupMode == LINTRCV_WUMODE_CLEAR, then a stored wakeup event is cleared on the addressed network
ARTD-45018	New Feature	[SPI] For baudrate and delay time calculation, add a node to switch between the current automation mode and a new manual mode NewWorkDescription: For Spi baudrate and delay time calculation, add a node to switch between the current automation mode and a new manual mode. Automation mode: inputs are desired baudrate and delay times; outputs are register generated values as PRESCALE, SCKDIV, SCKPCS, PCSSCK, DBT. SCK baud rate = (fP/PBR) x [(1+DBR)/BR] currently calculated with smallest error compared to requested input. Manual mode: inputs are register values as PRESCALE, SCKDIV, SCKPCS, PCSSCK, DBT; outputs are the calculated baudrate and delay times for the inputs. Show automatic calculation for SCK baud rate = (fP/PBR) x [(1+DBR)/BR] in the user interfaces as the customer understands the output of the configuration Explain in User manual the switch between Automation mode and Manual mode for SCK calculation Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A
ARTD-45149	New Feature	[CRYPTO_NG] Encrypted and authenticated asymmetric and symmetric key export NewWorkDescription: The Autosar specification does not support natively encrypted and/or authenticated key export thus the Crypto driver has to define several extensions to allow the upper layers to extract keys in an encrypted and/or authenticated format that will be accepted by the HSE firmware key export restrictions. Requirement source: HSE (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-45755	New Feature	[PORT] Recommended configuration can not be integrated by EB automatically Detailed description (how to reproduce it): Elektrobit is reporting an issue when integrating the Port Recommended configuration. Current PortRecConfiguration_JtagPins.xdm for S32K3 2.0.0 is: <d:lst type="TOP-LEVEL-PACKAGES"> <d:ctr name="Port" type="AR-PACKAGE"> <d:lst type="ELEMENTS"> <d:chc name="Port" type="AR-ELEMENT" value="MODULE-CONFIGURATION"> <d:ctr type="MODULE-CONFIGURATION"> <a:a name="DEF" value="ASPath:/TS_T40D34M20I0R0/Port"/> <d:var name="IMPLEMENTATION_CONFIG_VARIANT" type="ENUMERATION" value="VariantPostBuild"> <a:a name="IMPORTER_INFO" value="@DEF"/> </d:var> The fix would be: <d:lst type="TOP-LEVEL-PACKAGES"> <d:ctr name="TS_T40D34M20I0R0" type="AR-PACKAGE"> <d:lst type="ELEMENTS"> <d:chc name="PortRecConfigurationStandard" type="AR-ELEMENT" value="MODULE-CONFIGURATION"> <d:ctr type="MODULE-CONFIGURATION"> <a:a name="DEF" value="ASPath:/TS_T40D34M20I0R0/Port"/> <d:var name="IMPLEMENTATION_CONFIG_VARIANT" type="ENUMERATION" value="VariantPostBuild"> <a:a name="IMPORTER_INFO" value="@DEF"/> </d:var> Preconditions: This issue was reported for S32K3 2.0.0 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Port can not be fully integrated by EB. Expected behavior: Port should be fully integrated by EB. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Verify and apply EB suggested changed.

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ARTD-46078	Bug	[ETH][S32K3] Create a MACRO in base for errata ERR050705 Create a Macro: ERR_IPV_GMAC_E050705 in module base at file include/{*}Soc_Ips.h{*} for errata ERR050705 !!! IMPORTANT NOTE !!! This bug was not implemeted in this release BLN_RTD_4.7_S32K3XX_S32M27x_3.0.0. As a workaround, for the customers that are impacted by this bug a compiler flag should be added at the compile time: gcc {_}DERR_IPV_GMAC_E050705{_}={_}STD_ON{_} [options] [source files] [-o output file]
ARTD-46992	Bug	[Uart] Uart header file shall follows the naming convention as CDD_Uart.h Detailed description (how to reproduce it): For CDD drivers, the naming convention should be: CDD_[Module].h, according to the following spec: !image-2022-12-12-13-33-25-264.png|width=752,height=356! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The header file in Uart is Uart.h, which doesn't follow AUTOSAR spec. Expected behavior: The header file in Uart should be CDD_Uart.h Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CE's comment: All CDD modules follow the naming convention, except uart. We should have an unique naming convention.
ARTD-47508	New Feature	[IMPLEMENTATION] [ETH] Implement/review Qbv support CR description: Formalize requirements for qbv support in the Ethernet driver. The support shall mean having the Time Aware Shaper parameters configurable and runtime functionality to start and stop the Scheduler. Reason for this change: TSN interest of customers Benefit: Exposing a hardware feature that is useful for customers Onetime CR/Strategic CR: Onetime CR Use-case: Using 802.1qbv (TAS) in customer applications HW documentation reference (as applies): N/A HW/Application Engineer contact (as applies): N/A Note: relevant documents to be attached to the ticket.
ARTD-47712	New Feature	[CRYPTO] HSE IP multicore information in IM NewWorkDescription: Add HSE IP multicore information in the multicore chapter of the IM driver manual. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-48251	New Feature	[ADC] Documenting code for SDADC and DSPSS functions, data types following doxygen format NewWorkDescription: All functions, structs, enums and defines (of SDADC and DSPSS) should be well documented using proper doxygen tags in order to appear correctly in the UM. Improve node configuration description from chapter "{*}2 List of configurable parameters{*}" in "{*}CFSDADC_FW_User Manual.pdf{*}"

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		Requirement source: N/A Proposed solution optional: Guideline: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=127258744]
ARTD-52623	Bug	[CAN] Wrong idHit value Detailed description (how to reproduce it): idHit is stored only for the last instance of FlexCan configured. Preconditions: Multiple instances are configured Test Case ID (internal TC that caught the defect) optional: N.A Observed behavior: The correct value is returned only for the last instance configured. Expected behavior: To work for all the instances Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: See attached diff
ARTD-52741	Bug	[ADC] Compiler error due to missing prototype of Adc_Ipw_Adc0DmaTransferCompleteNotification when using BCTU control mode Detailed description (how to reproduce it): Customer is using complex ADC use case with DMA (BCTU control mode) in which they configure their own notification function at the end of ADC DMA transfer (plus their own customized DMA channel setup). They do not configure Adc_Ipw_Adc0DmaTransferCompleteNotification in MCL but instead their own notification function. With this configuration there is reported the following compiler error: "C:\nxp\SW32K3_RTD_4.4_2.0.0\eclipse\plugins\Adc_TS_T40D34M20I0R0\src\Adc_Ipw_Irq.c",1872 Error[Pa045]: function "Adc_Ipw_Adc0DmaTransferCompleteNotification ".mcal_text"" has no prototype Preconditions: Using compiler option –require_prototypes Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiler error Expected behavior: No compiler error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the missing Adc_Ipw_Adc0DmaTransferCompleteNotification function prototype
ARTD-53030	New Feature	[CAN] Implement support for RAM ECC operation on S32K3 platform NewWorkDescription: At the present version of RTD, FlexCAN_Init will call FlexCAN_DisableMemErrorDetection to disable ECC. We don't have APIs for operating FlexCAN ECC that can be directly called by the user. Requirement source: Proposed solution optional: There can be any APIs in the future that support ECC operations such as error injection, reporting, etc.
ARTD-53051	Bug	[SPI][S32K3] Inconsistent SCK in continuous transfer Detailed description (how to reproduce it): When SpiExternalDevice is configured with SpiDataShiftEdge = TRAILING, SpiShiftClockIdleLevel = LOW (CPOL = CPHA = 0), and SpiExternalDevice/SpiCsContinuous = TRUE, generated SCK low level duration may be incorrect between subsequent series of SCK pulses, defined by SpiChannel/SpiDataWidth. See attachment (SpiBaudRate = 1.0E-7, SpiChannel/SpiDataWidth = 8, LPSPI2 input clock 40MHz, SCK yellow, SOUT purple, CS green).

ID	Subtype	Headline and Description
		This can be worked-around by configuring SpiExternalDevice/SpiTimeCs2Cs with desired SCK low level duration, but ideally, it should be handled automatically by the driver code. As stated in SpiTimeCs2Cs description, this parameter shouldn't affect continuous transfers anyway. Preconditions: SpiExternalDevice/SpiBaudRate configured with resulting LPSPI_CCR1[SCKSET] > 0. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Incorrect SCK low pulse (inter-frame delay) in continuous transfer, Expected behavior: SCK low pulse duration consistent in continuous transfer. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: LPSPI_CCR1[SCKSCK] should be set equal to LPSPI_CCR1[SCKSET].
ARTD-54761	New Feature	[WDG] Update documentation with note about fix for Multiple instances of Wdg cannot generate in parallel NewWorkDescription: An issue will be occurred with multiple Wdg instances generation in parallel. The reason for this issue is, only a single plugin folder for Wdg is used to supports multiple instances, and the folders like "generate", "generate_PC", "generate_PB", "generate_swcd" are common. They are all accessed from plugin xml for each instance from the TemplateBasedCodeGenerator. We should warn users about Multiple instances of Wdg cannot generate in parallel. Requirement source: Customer Request Proposed solution optional: # Add the following setting in TemplateBasedCodeGenerator of WDG instances: !image-2022-12-01-18-51-26-654.png! 2. Add a note in UM/IM about this limitation.
ARTD-54963	New Feature	[ADC] Support transferring the processed data of DSPSS by using DMA in optimized mode NewWorkDescription: Add DMA support for SDADC standalone and with DSPSS integration ({*}Part 3{*}) Add DMA support to transfer data from DMA read buffer in XMEM of DSPSS to user's buffer (DSPSS enabled*{color}) in OptimizedDma mode Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) N/A Proposed solution optional: N/A
ARTD-55195	Bug	EMAC Rx Hang under high loading Detailed description (how to reproduce it): [run customer's project (No OS, no stack (bare-metal ICMP)), use tcpreplay to cyclic ping it with high frequency (60K), continue about decades minutes.] Preconditions: [S32K3x4 Q257 EVB TJA1101 daughter board, S32DS 3.4.3 S32K3 RTD RTM 2.0.1 LLD] Test Case ID (internal TC that caught the defect) optional: [SFDC case #00515886] Observed behavior: [Rx frame length = 0 will be printed in uart, and no ICMP response from K3] Expected behavior: [no rx length error happen, or there is dedicated API for clear this error / resume the Rx process] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [It may related with another SFDC case #00495248, which reported by the same customer which has been closed with a workaround provided by customer.]
ARTD-55421	Bug	[adc] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261!

ID	Subtype	Headline and Description
		In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55435	Bug	[crypto] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55443	Bug	[dpga] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55521	Bug	[zipwire] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-56166	Bug	[ZIPWIRE] Initialize Slave failure in HIGH_SPEED_MODE Detailed description (how to reproduce it): Config master and slave in high speed mode, synctimeout is not equal 0 Debug pararell master and slave into Zipwire_MasterHighSpeedInit and Zipwire_SlaveHighSpeedInit Master had ran into step 14 15 and 16(in RM), ICLC 0x2 had been sent (picture 3) Slave had received ICLC 0x2 and hw auto turn on RIISR[ICPONF] (picture 1) and it is in step 9. but Zipwire_WaitPllOnCommand function check Iclc ping fame request . (picture 1). This action will raise timeout error due to there is no Iclc ping fame request. Preconditions: high speed mode Test Case ID (internal TC that caught the defect) optional: Zipwire_TC_FCT_0022 Observed behavior: Zipwire_Init failure for slave in high speed mode Expected behavior: No timeout error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: May be Zipwire_WaitPllOnCommand() should check RIISR[ICPONF] instead of hwAccZipwireLfast_IclcPingFrameRequestReceivedFlag()
ARTD-56629	New Feature	[ADC] Support limitcheck for SDADC units NewWorkDescription: Support limitcheck feature for SDADC units Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) N/A Proposed solution optional: N/A
ARTD-56794	New Feature	[ADC] Handle DSPSS errors events NewWorkDescription: Handle DSPSS errors events: buffer underrun, address mismatch, DMA mismatch/transfer error,...

ID	Subtype	Headline and Description
		Also investigate the case when the result is invalid in function Adc_Ipw_EndSoftwareConvSdAdc to take appropriate actions Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) N/A Proposed solution optional: N/A
ARTD-56950	New Feature	[S32K3 3.0.0]MemAcc: implement MemAccBufferAlignmentValue feature NewWorkDescription: implement MemAccBufferAlignmentValue feature req: ECUC_MemAcc_00025 Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-58474	New Feature	[Crypto] Add support for TCM operations NewWorkDescription: Add resource information related to TCM support for all supported platforms. Requirement source: Customer request. Proposed solution optional: Update resource files with following entries: # Crypto.TcmSupport : Support for TCM (only for Cortex M7 cores) # Crypto.ItcmAddrStart : ITCM Start Address # Crypto.ItcmAddrEnd : ITCM End Address # Crypto.ItcmAddrOffset.List : List of address offsets for ITCM Backdoor depending on core # Crypto.DtcmAddrStart : DTCM Start Address # Crypto.DtcmAddrEnd : DTCM End Address # Crypto.DtcmAddrOffset.List : List of address offsets for DTCM Backdoor depending on core
ARTD-58492	New Feature	[ADC] Update text description for SDADC resolutions NewWorkDescription: SDADC only supports 15-bit resolution, the 16th is only the signed bit to specify the result is positive or negative. We should update the text description for this node in the configurator to avoid confusion that SDADC can support 16-bit resolution. Requirement source: N/A Proposed solution optional: N/A
ARTD-58499	New Feature	[ADC] Support for DSPSS Clock threshold mode NewWorkDescription: Support for DSPSS Clock threshold mode, current implementation only supports Sample threshold mode. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) N/A Proposed solution optional: N/A
ARTD-58502	New Feature	[ADC] Add support to use threads calibration set feature of DSPSS NewWorkDescription: Add support to use {*}DSPSS_ThreadsCalibrationSet{*}. Currently, this function is not used by ADC driver. This function can be called during runtime to change the calibration settings. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) N/A Proposed solution optional: N/A
ARTD-58511	New Feature	[ADC] Support to use DSPSS OptimizationLevel configuration NewWorkDescription:

ID	Subtype	Headline and Description
		Make OptimizationLevel configurable, currently its value is fixed with DSPSS_CFSDADC_OPTIMIZATION_NONE Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) N/A Proposed solution optional: N/A
ARTD-58867	Bug	[Base]SW32ZE_RTD_R21-11_0.9.0_P01: Issues with VERSION INFORMATION in BASE Detailed description (how to reproduce it): According to AUTOSAR_SWS_BSWGeneral.pdf, the version information is defined like <MIP>_VENDOR_ID (see attached Published_Information.png) with MIP being <Ma>[_<vi>_<ai>] (see MIP_Define.png). The problem is that the Module abbreviation "Platform" is reserved for Platform Types (see Module_List.png). The defines like PLATFORM_VENDOR_ID PLATFORM_AR_RELEASE_MAJOR_VERSION are reserved for the PlatformTypes.h file (generate file). But in the MCAL, the CDD Platform uses these macros to define its version information. This can lead to redefinitions. !image-2022-12-09-14-42-03-929.png! !image-2022-12-09-14-46-12-880.png! !image-2022-12-09-14-46-45-077.png! Preconditions: #define PLATFORM_VENDOR_ID 43 #define PLATFORM_AR_RELEASE_MAJOR_VERSION 4 #define PLATFORM_AR_RELEASE_MINOR_VERSION 7 #define PLATFORM_AR_RELEASE_REVISION_VERSION 0 #define PLATFORM_SW_MAJOR_VERSION 0 #define PLATFORM_SW_MINOR_VERSION 9 #define PLATFORM_SW_PATCH_VERSION 0 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: #define PLATFORM_TYPES_VENDOR_ID 43 #define PLATFORM_TYPES_AR_RELEASE_MAJOR_VERSION 4 #define PLATFORM_TYPES_AR_RELEASE_MINOR_VERSION 7 #define PLATFORM_TYPES_AR_RELEASE_REVISION_VERSION 0 #define PLATFORM_TYPES_SW_MAJOR_VERSION 0 #define PLATFORM_TYPES_SW_MINOR_VERSION 9 #define PLATFORM_TYPES_SW_PATCH_VERSION 0 Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Preconditions
ARTD-59354	Bug	[LINTRCV] Cannot generate an *.ecpd file when creating a test ecvd Detailed description (how to reproduce it): .ecpd file not generated !image-2023-03-07-09-17-25-159.png|thumbnail! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: !image-2023-03-07-09-16-49-204.png|thumbnail!
ARTD-59451	Bug	[ZIPWIRE] Blocking function return BUSY due to transfer is not done Detailed description (how to reproduce it): Step 1: Confgigurable ZipwireTimeoutDuration = 1 Step 2 Debug this line in program zipwire_status = Zipwire_ReadBlocking(0, 0, &TestDescriptor_read[0], 10); EU_ASSERT(zipwire_status == ZIPWIRE_IP_STATUS_SUCCESS);

ID	Subtype	Headline and Description
		zipwire_status = Zipwire_GetChannelStatus(ZIPWIRE_LOGIC_INSTANCE_0, 0); EU_ASSERT(zipwire_status == ZIPWIRE_IP_STATUS_SUCCESS); Issue: Zipwire_ReadBlocking return busy due to read transfer is not done. Zipwire_Ip_LaunchRWCommand set channel busy in the fist read, IRQ functiob will set channel not busy if remaining = 0.But Zipwire_ReadBlocking return this channel (busy) state right after Zipwire_Ip_LaunchRWCommand return cuccess. No time for read IRQ excute. The issue is the same for all blocking function. Maybe sequence checking timeout of blocking function is wrong. Blocking function should return success after transfer done or timeout error after transfer not done intime. Please check agian them: Zipwire_Ip_WriteBlocking, Zipwire_Ip_ReadBlocking, Zipwire_Ip_WriteDmaBlocking, Zipwire_Ip_StreamWrite, Zipwire_Ip_RequestId, Zipwire_Ip_Trigger. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Zipwire_TC_FCT_0009 Zipwire_TC_FCT_0010 Observed behavior: Zipwire_ReadBlocking return but channel still busy. Zipwire_ReadBlocking can not return ZIPWIRE_IP_STATUS_TIMEOUT due to wrong checking timeout sequence. Expected behavior: Blocking function should return success after transfer done or timeout error after transfer not done intime. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Please try to change 3 to 2
ARTD-78873	New Feature	[IMPLEMENTATION] [SENT][K3xx] Add SPC support in FlexIO SENT driver CR description: SPC (Short PWM Code) is a very common feature in sensors with SENT interface, which will make the unidirectional SENT communication to bidirectional. FlexIO SENT can support SPC functionality (see attachment AN). Recently we received a very crucial requirement for the SPC support in SENT, with a considerable business. This would be the key to make success in ESP application for K3. It requires SPC as soon as possible, best in RTD next release. Reason for this change: If there is no SPC function for SENT, customer may not choose S32K3 to develop ESP. Below is some already known business requiring SENT (with SPC): BeiJing Autonics Technology: ESP GM, S32K388 SENT, dropped FuDi Tech: ESP HanDing: ESP, 4 SENT channel nexteer: ESP, 6 SENT channel Benefit: This would be the key to make success in ESP application for K3, gaining business. Onetime CR/Strategic CR: S32K3 platform Use-case: ESP (Electronic Stability Program) HW documentation reference (as applies): Please see attached AN for more info. !image-2023-02-03-17-59-22-244.png! HW/Application Engineer contact (as applies): [~nxf65050] Note: relevant documents to be attached to the ticket.
ARTD-59883	Bug	[mem_infls] Update driver following Errata ERR051127 for S32K3XX NewWorkDescription: Implement fix for ERR051127 "PFLASH: Flash read during array integrity may return incorrect read data Link: S32K3x4: Mask Set Errata for Mask 0P55A/1P55A, Rev. 14/Oct/2022, https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FErrata%2FS32K3x4%200P55A%5F1P55A%20Errata%20Rev14%5FOct

ID	Subtype	Headline and Description
		%5F2021%2Epdf&viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FErrata Requirement source: NA Proposed solution optional: update code follows workaround of Errata. If cannot implement, Errata information will update in UM/IM
ARTD-60141	Bug	[MCU] Low power modes of S32Kxx cannot operate as expected Detailed description (how to reproduce it): On S32K3xx, If chips is set in low power modes, it cannot be woken up Preconditions: Set low power modes Test Case ID (internal TC that caught the defect) optional: Mcu_TS_012, Mcu_TS_011 Observed behavior: Chips cannot be woken up from lowpower modes Expected behavior: Chips can be woken up from lowpower modes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-60374	Bug	[Port] No error when enable invert control in input mode Detailed description (how to reproduce it): Create new project (S32K396) add port_pin, Mscr = 32 enable Invert control !image-2023-03-16-16-41-08-422.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When mode and direction are input: ADC mode => no error other input mode => generate error !image-2023-03-16-16-45-32-986.png! !image-2023-03-16-16-45-47-123.png! Expected behavior: Error when enable invert with Input mode Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-60407	New Feature	[Port] Remove I3C Driver from RTD release Description: Need to remove I3C driver from release , IP shall not be used. {noformat} Errata: ERR051298: I3C: The I3C feature may not work reliably Description: The I3C module may not be 100% reliable to fulfill the protocol. This feature is not recommended for use. Workaround: There is no workaround for this. {noformat} Check Port driver and manuals if we have references to I3C ip and remove them.
ARTD-60442	Bug	[MCU] Range of SWG_CLK is different between EB and CT Detailed description (how to reproduce it): Issue 1 in S32K396: SWG_CLK had maximum frequency is 20mhz (picture1)

ID	Subtype	Headline and Description
		But user possible to configurable this to out of 20mhz (picture2) The same issue for Cgm0Mux15 LFAST_REF_CLK The same issue for Cgm0Mux10 picture 3 and 4: EB check max of QuadSPI_SFCK is 120mhz but the value in picture 1 is for QSPI_2XSFIF Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Frequency can be configurable higer than maximum Expected behavior: No error about frequency range Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-60460	Bug	[OCU] Fix VSMD rule TpsEcuc_08033 violation, for OcuHWSpecificSettingsRef parameter Detailed description (how to reproduce it): Generate the VSMD report and check the rule violation "TpsEcuc_08033", inside the report. !image-2023-03-17-08-48-36-413.png! Preconditions: Build OCU plugins Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: TpsEcuc_08033 rule violation. Expected behavior: No violation related to TpsEcuc_08033 rule. Proposed solution optional: NA
ARTD-60618	Bug	[S32M27x][Pins tool] Missing TSPC, ADC Interleave configuration Detailed description (how to reproduce it): # Missing resource csv file for ADC Interleave (EBT, HLD, Pins tool) in S32M27x # Missing configuration in Pins tool for S32M27x !image-2023-03-20-10-57-10-258.png|width=1278,height=234! Preconditions: PORT_228 PVT_BASE_S32K3XX_RTM_3.0.0_022 Test Case ID (internal TC that caught the defect) optional: None Observed behavior: # Missing TSPC configuration for S32M27x # Missing resource csv file for ADC Interleave Expected behavior: 1. User can configure TSPC for S32M27x (m276, m274) 2. Generate code for ADC Interleave when user configure corresponding ADC channel. 2. Generate with correct tpsc value and adc interleave channel 3. Build done Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Becareful with these registers !image-2023-03-20-15-23-22-472.png!
ARTD-60920	Bug	[Mcu] SXOSC is not available in 100 pin and 48 pin packages Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		SXOSC is not available in 100 pin and 48 pin packages but SXOSC is still supported on S32K312/S32K322/S32K341/S32K342 100 pin !image-2023-03-22-11-25-23-845.png|thumbnail! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: SXOSC is still supported on S32K312/S32K322/S32K341/S32K342 100 pin Expected behavior: remove SXOSC on S32K312/S32K322/S32K341/S32K342 100 pin resource file and configurations Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: remove SXOSC on S32K312/S32K322/S32K341/S32K342 100 pin resource file and configurations
ARTD-61009	Bug	[MCL] Fix INTEGER_OVERFLOW violation in CWE report Detailed description (how to reproduce it): There is a INTEGER_OVERFLOW violation in Mcl_Dma_SetUserAccessAllowed function. Need to analyze and fix in the next release. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: There is no violation in CWE report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-61100	Bug	[Crypto] Remove the HSE interface file from the Crypto driver plugin Detailed description (how to reproduce it): NewWorkDescription: Remove the HSE interface file from the Crypto driver plugin For both examples cases (SBT and DS) the path to the location of HSE interface must be provided on compile time. Storage of file should not be in RTD plugin to not including files from other products deliverables. Preconditions: example usage Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The HSE interface is provided in the DS example of crypto driver. Expected behavior: Path for the HSE interface should be provided through include path on compile time. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: see above
ARTD-61124	Bug	[Integration][PORT] Pins tool: Incorrect build version Detailed description (how to reproduce it): "Build version" in project header files are incorrect on M274, K396, K394, K358, K348, K344, K342, K341, K338, K328, K324, K322, K314, K312, K311, K310 after CT-building Preconditions: Step1 Using S32K3XX_RTD_4_7_RTM_3_0_0_DS_updatesite_2303_signed Step2 Create a new project on S32DS Step3 Update code Step4 Check include files

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: "Build version" in project header files are incorrect on M274, K396, K394, K358, K348, K344, K342, K341, K338, K328, K324, K322, K314, K312, K311, K310 after CT-building Expected behavior: "Build version" in project header files are correct on M274, K396, K394, K358, K348, K344, K342, K341, K338, K328, K324, K322, K314, K312, K311, K310 after CT-building Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-61153	Bug	[Platform] Wrong I-Cache initialization timing Detailed description (how to reproduce it): The following code of init I-Cache is not correct: C:\NXP\SW32_RTD_4.4_4.0.0\eclipse\plugins\Platform_TS_T40D11M40I0R0\startup\src\system.c #ifdef I_CACHE_ENABLE /*init Code caches*/ S32_SCB->ICIALLU = 0UL; / invalidate I-Cache / S32_SCB->CCR = (uint32)SCB_CCR_IC_Msk; / enable I-Cache / MCAL_DATA_SYNC_BARRIER(); MCAL_INSTRUCTION_SYNC_BARRIER(); #endif /*I_CACHE_ENABLE*/ Please add DSB and ISB after invalidating I-Cache. Or it will cause NCF2, CM7_0 I-Cache ECC error. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Cause NCF2, CM7_0 I-Cache ECC error. Expected behavior: No any error in NCF fault in FCCU. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Please add DSB and ISB after invalidating I-Cache.
ARTD-61176	Bug	[DPGA] Fix all warnings when run Traceability Matrix reports Detailed description (how to reproduce it): There are some warnings in Traceability matrix report (check attachment) which need to be addressed. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: There are no warnings in traceability matrix report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-61230	Bug	[Mem_Eep] Build fail when disable BlankcheckAPIs node on EB Detailed description (how to reproduce it): Build fail when disable BlankcheckAPIs node on EB !image-2023-03-27-11-10-51-829.png|width=690,height=407! !image-2023-03-27-11-12-05-891.png! # When disable BlankcheckApis, the function Mem_43_Eep_ProcessBlankCheckJob have prototype but not definition. # Change config param Mem_43_EepBankCheckApi to Mem_43_EepBlankCheckApi # Check for other defines also. Preconditions:

ID	Subtype	Headline and Description
		Enable BlankCheckAPIs Test Case ID (internal TC that caught the defect) optional: Mem_TC_COT_001 Observed behavior: Build fail Expected behavior: Build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-61326	Bug	[Zipwire] Fix MISRA violations Detailed description (how to reproduce it): There are many MISRA Violations. Preconditions: Code Test Case ID (internal TC that caught the defect) optional: Code Observed behavior: There are many MISRA Violations. Expected behavior: Fix or comment the MISRA Violations. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix or comment the MISRA Violations.
ARTD-61329	Bug	[Zipwire] Fix VSMD Errors Detailed description (how to reproduce it): There are VSMD Errors present Preconditions: Configuration Test Case ID (internal TC that caught the defect) optional: Configuration Observed behavior: There are VSMD Errors present Expected behavior: Fix VSMD Errors present Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix VSMD Errors present
ARTD-61607	Bug	[GDU] Fix VSMD warnings Detailed description (how to reproduce it): There are warnings in the VSMD report. There are errors for the other k3 derivatives. Preconditions: none Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: No warnings, no errors. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: Add check the module is available on a derivative or not. Update UUID for some nodes on xdm.
ARTD-61804	Bug	GMAC Rx buffer is leaked when receiving frame errors Detailed description (how to reproduce it): if ETH_RX_IRQ_ENABLED is STD_OFF, delay calling Eth_Receive() will cause RX FIFO overflow, then RDES3.OV is set, the error frame will be ignored and corresponding buffer is leaked. shown as following code snippet. !image-2023-04-03-15-13-19-647.png! Preconditions: // Test Case ID (internal TC that caught the defect) optional: // Observed behavior: buffer is leaked and eventually RX stops working Expected behavior: No buffer leak Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Recycle buffers in case of error frames
ARTD-61822	Bug	GMAC RX BD issue when receiving timetamp Detailed description (how to reproduce it): Enable EthGlobalTimeSupport for GMAC. !image-2023-04-03-15-32-06-051.png! No boundary judgment when reading timestamp from Context Descriptor: !image-2023-04-03-15-42-06-327.png! And RDES3.LD needs to be checked for a valid timestamp as the description for RDES0.TSA ! image-2023-04-03-15-44-20-672.png! Preconditions: // Test Case ID (internal TC that caught the defect) optional: // Observed behavior: RX stops working because of BD execption Expected behavior: RX works normal when EthGlobalTimeSupport is enabled Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: //
ARTD-62231	New Feature	[LINTRCV] Analyze the implementing with LinTrcv_GetBusWuReason function NewWorkDescription: There are multiple requirements which describe the implementing with LinTrcv_GetBusWuReason function. Analyze them and have a final solution how to support this function. Requirement source: ASR SWS (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: This ticket was implemented in ARTD-45025. Step to implementing: For M24x and M27x only support two reasons of wake up: Type||Meaning LINTRCV_WU_INTERNALLY The transceiver has detected, that the network has been woken up by the ECU via a request to NORMAL mode.

ID	Subtype	Headline and Description
		LINTRCV_WU_BY_BUS The transceiver has detected, that the network has caused the wake up of the ECU. Call AeLinPhy_LinTrcv_Ip_CheckWakeupFlag function to verify wakeup flag is set or not , if set, set status to LINTRCV_WU_BY_BUS. If no, call AeLinPhy_LinTrcv_Ip_GetMode function to get current mode is NORMAL mode or not, if yes, set status to LINTRCV_WU_INTERNALLY. otherwise , Lintrcv can't detect any reason, set status to LINTRCV_WU_NOT_SUPPORTED. And if driver can't get communication to the transceiver => LINTRCV_WU_ERROR will be return

ARTD-62435	Bug	Missing memory barrier for GMAC driver
		
		Detailed description (how to reproduce it):
		GMAC's RX probability stops working during stress test. After investigation, it was found that certain places were missing WMB, For example below code snippet;
		
		void Gmac_Ip_ProvideRxBuff(uint8 Instance,
		uint8 Ring,
		const Gmac_Ip_BufferType Buff)
		{
		Gmac_Ip_ChannelType Base;
		Gmac_Ip_BufferDescriptorType Bd;
		Gmac_Ip_BufferDescriptorType CtxtBd;
		Gmac_Ip_BufferDescriptorType ListBd;
		uint32 TailPtr; GMAC_DEV_ASSERT(Instance < FEATURE_GMAC_NUM_INSTANCES);
		GMAC_DEV_ASSERT(Gmac_apxState[Instance] != NULL_PTR);
		GMAC_DEV_ASSERT(Ring < Gmac_apxState[Instance]->RxRingCount);
		GMAC_DEV_ASSERT(Buff != NULL_PTR); Base = Gmac_apxChBases[Instance][Ring]; Bd = Gmac_apxState[Instance]->RxAllocDesc[Ring];
		ListBd = (Gmac_Ip_BufferDescriptorType)Base->DMA_RXDESC_LIST_ADDRESS;
		TailPtr = Base->DMA_RXDESC_TAIL_POINTER; GMAC_DEV_ASSERT((Bd->Des3 & GMAC_RDES3_OWN_MASK) == 0U);
		if ((Bd->Des1 & GMAC_RDES1_TSA_MASK) != 0U)
		{
		CtxtBd = ((uint32)&Bd[1U] >= (uint32)&ListBd[Base->DMA_RXDESC_RING_LENGTH 1UL])? ListBd : &Bd[1U]; if (Gmac_Ip_RestoreRxCtxtDescr(CtxtBd) == TRUE)
		{
		Gmac_apxState[Instance]->RxAllocDesc[Ring] = CtxtBd;
		}
		} Bd->Des0 = (uint32)Buff->Data;
		Bd->Des1 = 0U;
		Bd->Des2 = 0U;
		Bd->Info0 = (uint32)Buff->Data;
		Bd->Info1 &= GMAC_INFO1_CONSUMED_MASK;
		Bd->Des3 = GMAC_RDES3_OWN_MASK GMAC_RDES3_INTE_MASK GMAC_RDES3_BUF1V_MASK;
		Gmac_apxState[Instance]->RxAllocDesc[Ring]++;
		if ((uint32)Gmac_apxState[Instance]->RxAllocDesc[Ring] >= (uint32)&ListBd[Base->DMA_RXDESC_RING_LENGTH 1UL])
		{
		Gmac_apxState[Instance]->RxAllocDesc[Ring] = ListBd;
		} Base->DMA_RXDESC_TAIL_POINTER = TailPtr;
		}
		
		Write memory barrier is needed before writing Bd->Des3 and also before writing Base->DMA_RXDESC_TAIL_POINTER
		
		Preconditions:
		//
		
		Test Case ID (internal TC that caught the defect) optional:
		//
		
		Observed behavior:
		GMAC Rx stopped, DMA_CH0_Status is 0x002015c5. Following bits are set:
		1'b1: Error during data transfer by Rx DMA
		
		Expected behavior:
		All works well
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:

ARTD-62453	Bug	[I2S] Channel 1 DMA configure wrongly in DS Detailed description (how to reproduce it): Issue 1: When DMA enable with MUX line, 2 channel DMA have to configure. But channel 1 didn't get value from configuration correctly. Issue 2: Functional Group get name to put the file name wrongly with uppercase added in generated file. For example:

ID	Subtype	Headline and Description
		Functional Group: BOARD_InitPeripherals Generated file: Sai_Ip_BOARD_InitPeripherals_PBcfg.h File included in another file: Sai_Ip_BOARD_INITPERIPHERALS_PBcfg.h. Please check this for all generated files. Preconditions: DMA enable Mux LINE used. Test Case ID (internal TC that caught the defect) optional: I2s_TS_120 I2s_TC_FCT_2200, I2s_TC_FCT_1201, I2s_TC_FCT_1200 Observed behavior: Issue 1: Channel 1 is 0 if channel 2 is disabled. Issue 2: File included in another file is different name with generated file. Expected behavior: Issue 1: Channel 1 get value from configuration correctly. Issue 2: File included in another file is have similar name with generated file. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Issue 1: aDmaChannel get value for channel 1 from channel 2. See image. Issue 2: Remove .toUpperCase() from variantName for #include "file<variantName>".
ARTD-62550	Bug	[Spi] Fail generating code with DMA fast transfer on DS Detailed description (how to reproduce it): Fail generating code with DMA fast transfer on DS DS Tool do not raise errors when configuring wrong with require 2, 3 for Spi/SpiDriver/SpiSequence/SpiEnableDmaFastTransfer node: "When this parameter is enabled, this Sequence will be transferred using DMA ScatterGather and CPU used only for processing end of Sequence. SpiAutosarExt/SpiEnableDmaFastTransferSupport must be checked to support this feature. Note: This feature requires: 1. All parameters in External Device linked to each Job in this Sequence must be the same except SpiCsIdentifier, SpiCsContinous. 2. The parameters SpiDataWidth and SpiTransferStart in Channel assigned to each Job in this Sequence must be the same. 3. In each Channel, the number of data buffers is NOT higher than 32767 if SpiDataWidth < 9. So, SpiIbNBuffers and SpiEbMaxLength must be assigned to suitable values. 4. Only Master mode is supported." Preconditions: Creating DS project with DMA fast transfer Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Log : [DATA] Error resolving: ((system::getParent($this, 2).getSetting(`SpiEnableDmaFastTransfer`).getValue() == false) (system::deref($this).getSetting(`SpiChannelList`).map((x > system::deref(x.getSetting(`SpiChannelAssignment`))))).filter((x > (x.getSetting(`SpiDataWidth`).getValue() > 9))) (((x.getSetting(`SpiEbMaxLength`).getValue() < 32767) && (x.getSetting(`SpiChannelType`).getValue() == `EB`)) ((x.getSetting(`SpiIbNBuffers`).getValue() < 32767) && (x.getSetting(`SpiChannelType`).getValue() == `IB`))))), Cannot convert value ([Setting: [Type: struct, Id: Spi.SpiDriver.SpiChannel.7], Setting: [Type: struct, Id: Spi.SpiDriver.SpiChannel.12]]) with type: OBJECT to boolean. Expected behavior: Generating successfully project DMA Fast Transfer Project Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-62544	Bug	[ICU]Errors in epd files Detailed description (how to reproduce it): s32m276/S32k11 [Error] Default value of parameter 'Icu/IcuConfigSet/IcuLpCmp/IcuCmpInstanceNumber' is out of range. [Icu_TS_T40D34M30I0R0-autosar-Icu_s32k311_mqfp100.epd, Icu_s32k311_lqfp48.epd, Icu_s32m276_lqfp64.epd] Preconditions: Don't happen those above issues. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: as Detailed description Expected behavior: as Preconditions

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-62547	Bug	[ocu] Errors in epd files Detailed description (how to reproduce it): [Error] According to AUTOSAR standard parameter definition 'Ocu/OcuConfigSet/OcuChannel/OcuHWSpecificSettingsRef' should be ECUC-REFERENCE-DEF. [Ocu_TS_T40D34M30I0R0-autosar-Ocu_s32k388_mapbga289.epd] [Error] DestinationRef of AUTOSAR reference 'Ocu/OcuConfigSet/OcuChannel/OcuHWSpecificSettingsRef' should be '/AUTOSAR/EcucDefs/Ocu/OcuConfigSet/OcuHWSpecificSettings'. [Ocu_TS_T40D34M30I0R0-autosar-Ocu_s32k388_mapbga289.epd] [Error] DestinationRef '/TS_T40D34M30I0R0/Ocu/OcuConfigSet/OcuHWSpecificSettings' of reference 'Ocu/OcuConfigSet/OcuChannel/OcuHWSpecificSettingsRef' should start with '/AUTOSAR/EcucDefs/' (as target is standard AUTOSAR Container). [Ocu_TS_T40D34M30I0R0-autosar-Ocu_s32k388_mapbga289.epd] Preconditions: Don't happen those above issues. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: as Detailed description Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-62946	Bug	[ADC] Incorrect information in UM Detailed description (how to reproduce it): In ADC UM, the following note: 4.188 Parameter AdcUseHardwareNormalGroups This parameter defines if Hardware Normal Groups are used in any Hardware Unit, any variant. It needs to be enabled if Hardware Normal Groups are needed. If Hardware Normal Groups are not needed, this parameter should be disabled for code optimizations. Normal Hardware conversions are not supported on this platform. seems to be not correct. Normal hardware conversion is still supported in K3, and in fact it was working when customers enable it. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Incorrect information of Adc normal hardware conversion in UM Expected behavior: Correct information Adc normal hardware conversion in UM Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-62636	Bug	[CRYPTO] CT Crypto_Cfg.c generation issue leads to build error Reproduce steps: 1. Generate TS_001 2. Open S32DS and create a new project 3. Add Crypto to the project 4. Import the epc from the generated EBT project 5. Generate and build the S32DC project Result: The build fail !image-2023-04-06-15-55-18-841.png|thumbnail! Expected result: The build pass Propose solution: Remove the "," at line 1176 !image-2023-04-06-15-56-12-330.png|thumbnail! As at line 1283: !image-2023-04-06-15-57-29-123.png|thumbnail!

ID	Subtype	Headline and Description
ARTD-62962	Bug	[ETH] - Function which sets the RX external data buffers address in descriptor before starting the communication should not check any flag Detailed description (how to reproduce it): Gmac_Ip_SetRxExternalBuffer must not check any flag related to timestamp (TSA). Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: This function must only set the data buffers to the current bd in the parameter queue. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove the TSA bitfield in DES3 check.
ARTD-63510	Bug	[S32K3][Port][ECPD] The "Pin tool functional group" doesn't work properly when using at least 2 container Detailed description (how to reproduce it): Step 1: Create new project on DS Step2: Add Port component, configure with 2 container (PortContainer_0, PortContainer_1) and one "Pin tool functional Group" !image-2023-04-18-09-40-10-833.png|width=499,height=374! !image-2023-04-18-09-40-33-743.png|width=512,height=351! !image-2023-04-18-09-40-50-950.png|width=522,height=330! Step3: Generate ECVD file Step4: Import ECVD file to EB, generate EPC file Step5: Import EPC file to S32DS (as new one) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Port_TS_COT_019 Observed behavior: in the PortContainer_1, "Pin tool functional group" doesn't work properly, it selected PortContainer_0_BOARD_InitPeripherals instead of PortContainer_1_BOARD_InitPeripherals !image-2023-04-18-09-49-39-362.png|width=486,height=346! !image-2023-04-18-09-49-53-955.png|width=494,height=342! !image-2023-04-18-09-50-30-882.png|width=495,height=315! !image-2023-04-18-09-50-54-755.png|width=512,height=312! Expected behavior: "Pin tool functional group" in all containers works properly Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-63642	Bug	[MCU][K3XX] MC_CGM_MUX8 and MUX9 output frequency limited to 50 MHz in Tresos Detailed description (how to reproduce it): MC_CGM_MUX8 and MUX9 maximum output frequency is limited to 50 MHz. This doesn't allow configuration of: Required 250MHz GMAX Tx clock for 1Gbit/s RGMII operation (see attached PDF for GMAC clocking consider phy_intf_sel[0] = DCM_GPR_DCMRWF1[EMAC_CONF_SEL] = 1) Higher frequency EMAC/GMAC timestamp clock Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior:

ID	Subtype	Headline and Description
		Mcu/McuModuleConfiguration/McuClockSettingConfig/McuCgm0SettingConfig/McuCgm0ClockMux8/ McuClockMux8Divider0_Frequency and Mcu/McuModuleConfiguration/McuClockSettingConfig/McuCgm0SettingConfig/ McuCgm0ClockMux9/McuClockMux9Divider0_Frequency cannot be configured above 50 MHz. Expected behavior: Mcu/McuModuleConfiguration/McuClockSettingConfig/McuCgm0SettingConfig/McuCgm0ClockMux8/ McuClockMux8Divider0_Frequency configurable to 250 MHz. Mcu/McuModuleConfiguration/McuClockSettingConfig/ McuCgm0SettingConfig/McuCgm0ClockMux9/McuClockMux9Divider0_Frequency configurable above 50 MHz. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update Mcu.xdm according to provided information.
ARTD-64547	Bug	[ETH][K3XX] MC_CGM_MUX_8 not driving assigned RGMII Tx clock output pin Detailed description (how to reproduce it): In RGMII mode, GMAC Tx clock is internally generated and provided by MC_CGM_MUX_8 output. To drive the assigned RGMII Tx clock output pin by MC_CGM_MUX_8 output signal, DCM_GPR_DCMRWF1[31] has to be set to 1. This is not handled by Eth driver. See attached PDF for details (please note that DCM_GPR_DCMRWF1[31] is not shown there, but is required to enable pad Tx loopback confirmed by design team). Preconditions: GMAC configured in RGMII mode and MC_CGM_MUX_8 output clock is enabled. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Assigned RGMII Tx clock pin is not driven by MC_CGM_MUX_8 output Expected behavior: Assigned RGMII Tx clock pin is driven by MC_CGM_MUX_8 output Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Modify Eth_43_GMAC_Ipw_SelectPhyInterface() to set DCM_GPR_DCMRWF1[31] = 1 if RGMII mode is selected.
ARTD-65828	Bug	[ADC] 2 DMA request in parallel from both ADC and CTU when starting a CTU control mode conversion after a SW one-shot single access mode group finishes Detailed description (how to reproduce it): Starting sw one-shot single access mode group (ch1, ch5), DMA transfer (DMA ch0). In ADC ISR, ERQ of DMA transfer is re-enabled (calling Adc_StopGroupConversion() will raise det error so cannot used in this case). After sw group finishes, start a CTU control mode conversion with ch1 and ch5 in cmd list (ch5 is last channel), DMA enabled for control mode (DMA ch5). At this point, there are 2 DMA requests from both CTU FIFO threshold and from ADC (because ADC ch5 has completed by cmd list from CTU). !image-2022-07-18-21-36-17-992.png|thumbnail! Preconditions: Describe in description Test Case ID (internal TC that caught the defect) optional: Adc_example_SAF8544 Observed behavior: 2 concurrent ADC and CT DMA requests to 2 separate DMA channels Expected behavior: Only one DMA request from CTU FIFO threshold Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-65905	Bug	[LPUART/DMA] Potential misconfiguration because of shared DMAMUX slot for LPUART Detailed description (how to reproduce it): [Some of the DMAMUX slots are shared. !https://community.nxp.com/t5/image/serverpage/image-id/219791i848E41852B22B070/image-dimensions/714x68?v=v2! Then the DMA request from UART0 will also be routed to DMA channel which has been mapped to UART8. If the user call API to start a transfer through UART0, the DMA channel for UART8 will also be triggered. So there will be a DMA_SBE error in DMA channel for UART8 because the user don`t configure UART8 and its channel. UART1/9 UART2/10 and so on also has this issue. The S32DS RTD configuration tool does not show any error/warning when one DMAMUX source (for example DMA_IP_REQ_MUX0_LPUART0_LPUART8_TX) is selected for two DMA channels.

ID	Subtype	Headline and Description
		!https://community.nxp.com/t5/image/serverpage/image-id/219795i2F52E929AB7DA20D/image-dimensions/692x218?v=v2! Could there be a warning/error for avoiding some potential misconfiguration?] Observed behavior: [DMA_SBE error] Expected behavior: [Add some warning or error for this usage.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ARTD-65961	Bug	Wrong 'PoolSize' limitations imposed by the GMAC RTD driver on S32R41
		
		Detailed description (how to reproduce it):
		If we enable 'GMAC_DEV_ERROR_DETECT' when configuring ETH RTD driver, the software will validate the configurations, in the generated file 'Gmac_Ip.c' > 'Gmac_Ip_Init()', we can see the following code snippets.
		
		#if (GMAC_DEV_ERROR_DETECT == STD_ON)
		PoolSize = 0U;
		
		for (i = 0U; i < Config->Gmac_pCtrlConfig->RxRingCount; i)
		{
		GMAC_DEV_ASSERT(Config->Gmac_paCtrlRxRingConfig[i].RingDesc != NULL_PTR);
		GMAC_DEV_ASSERT(Config->Gmac_paCtrlRxRingConfig[i].RingSize > 1U);
		GMAC_DEV_ASSERT(GMAC_BUFFDESCR_IS_ALIGNED(Config->Gmac_paCtrlRxRingConfig[i].RingDesc));
		GMAC_DEV_ASSERT((Config->Gmac_paCtrlRxRingConfig[i].Buffer == NULL_PTR) GMAC_BUFF_IS_ALIGNED(Config->Gmac_paCtrlRxRingConfig[i].Buffer));
		GMAC_DEV_ASSERT(GMAC_BUFFLEN_IS_ALIGNED(Config->Gmac_paCtrlRxRingConfig[i].BufferLen));
		GMAC_DEV_ASSERT(GMAC_RXRINGLEN_IS_BLOCK_ALIGNED((uint32)Config->Gmac_paCtrlRxRingConfig[i].RingSize Config->Gmac_paCtrlRxRingConfig[i].BufferLen));
		
		PoolSize = ((uint32)Config->Gmac_paCtrlRxRingConfig[i].RingSize Config->Gmac_paCtrlRxRingConfig[i].BufferLen);
		}
		
		GMAC_DEV_ASSERT(PoolSize <= FEATURE_GMAC_MTL_RX_POOL_SIZE);
		
		__
		PoolSize = 0U;
		
		for (i = 0U; i < Config->Gmac_pCtrlConfig->TxRingCount; i)
		{
		GMAC_DEV_ASSERT(Config->Gmac_paCtrlTxRingConfig[i].RingDesc != NULL_PTR);
		GMAC_DEV_ASSERT(Config->Gmac_paCtrlTxRingConfig[i].RingSize > 1U);
		GMAC_DEV_ASSERT(GMAC_BUFFDESCR_IS_ALIGNED(Config->Gmac_paCtrlTxRingConfig[i].RingDesc));
		GMAC_DEV_ASSERT((Config->Gmac_paCtrlTxRingConfig[i].Buffer == NULL_PTR) GMAC_BUFF_IS_ALIGNED(Config->Gmac_paCtrlTxRingConfig[i].Buffer));
		GMAC_DEV_ASSERT(GMAC_BUFFLEN_IS_ALIGNED(Config->Gmac_paCtrlTxRingConfig[i].BufferLen));
		GMAC_DEV_ASSERT(GMAC_TXRINGLEN_IS_BLOCK_ALIGNED((uint32)Config->Gmac_paCtrlTxRingConfig[i].RingSize Config->Gmac_paCtrlTxRingConfig[i].BufferLen));
		
		PoolSize = ((uint32)Config->Gmac_paCtrlTxRingConfig[i].RingSize Config->Gmac_paCtrlTxRingConfig[i].BufferLen);
		}
		
		GMAC_DEV_ASSERT(PoolSize <= FEATURE_GMAC_MTL_TX_POOL_SIZE);
		#endif
		
		the assertion " GMAC_DEV_ASSERT(PoolSize <= FEATURE_GMAC_MTL_RX_POOL_SIZE)" will fail if 'PoolSize' is larger than 'FEATURE_GMAC_MTL_RX_POOL_SIZE' which is a constant 8192 on S32R41. This limitation makes no sense, the 'FEATURE_GMAC_MTL_RX_POOL_SIZE' stands for the FIFO buffer length in the MTL receiving module, while the 'PoolSize' means the receiving circular buffer length in the SRAM, it is supposed that users can set 'PoolSize' to an arbitrary value according to their needs.
		
		I have tried to disable 'GMAC_DEV_ERROR_DETECT' and config 'PoolSize' to a larger value, the ethernet module worked well and showed better performance (less package loss)
		
		Preconditions:
		[none]
		
		Test Case ID (internal TC that caught the defect) optional:
		[none]
		
		Observed behavior:
		[see above]
		
		Expected behavior:

ID	Subtype	Headline and Description
		[see above] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-66176	Bug	[ADC] Driver cannot deinit BCTU IP in case BCTU configured as trigger mode Detailed description (how to reproduce it): In Adc_Ipw_Init function !image-2023-04-26-10-07-25-893.png! In Adc_Ipw_DeInit function !image-2023-04-26-10-08-24-619.png! Preconditions: ADC_IPW_CTU_TRIGGER_MODE_SUPPORTED == STD_ON ADC_HW_TRIGGER_API == STD_ON ADC_IPW_CTU_AVAILABLE == STD_ON ADC_ENABLE_CTU_CONTROL_MODE_API == STD_OFF Test Case ID (internal TC that caught the defect) optional: Adc_TS_007, Adc_TS_013, Adc_TS_045 Observed behavior: See the description Expected behavior: Deinit BCTU_IP successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-66265	Bug	[ETH] Schema file is not using VendorApiInfix In Eth_43_GMAC.xdm default value for VendorApiInfix is empty, also this parameter is configured as OPTIONAL true : <a:da name="DEFAULT" value=""/> <a:a name="OPTIONAL" value="true" Since Eth driver is using VendorApiInfix the lines should be replaced with : <a:da name="DEFAULT" value="GMAC"/>
ARTD-66268	Bug	[LIN] Schema file is not using VendorApiInfix In Lin_43_LPUART_FLEXIO.xdm for VendorApiInfix the OPTIONAL tag is added: <a:a name="OPTIONAL" value="true"/> Since the Lin driver implementation is based on VendorApiInfix this should be mandatory and the OPTIONAL flag should be removed.
ARTD-66323	New Feature	[SPI] Spi_MainFunction_Handling available only for SpiLevelDelivered 1 and 2 In Spi_Bswmd.arxml Spi_MainFunction_Handling is available all the time. According with Autosar requirements this API should be available only for SpiLevelDelivered 1 and 2. For this Spi_Bswmd.arxml should be update to check if SpiLevelDelivered > 0 e.g.: [!VAR "Spi_MainFunction_Handling_Enable"="num:i(node:value(SpiGeneral/SpiLevelDelivered)) > 0 "!][!// ..... [!IF "$Spi_MainFunction_Handling_Enable = 'true'"!] <BSW-MODULE-ENTRY-REF-CONDITIONAL> <BSW-MODULE-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Spi/BswModuleEntrys/Spi_MainFunction_Handling</BSW-MODULE-ENTRY-REF> </BSW-MODULE-ENTRY-REF-CONDITIONAL> [!ENDIF!] Attached there is a unpdated version of the Bswmd which works.
ARTD-66345	Bug	[PORT]UM file has a note need to detail explanation Detailed description (how to reproduce it): In the RTD port driver user manual, for the Parameter PortPinModeChangeable, the document says :_"{color:#FF0000}The function for changing the pin modes is not supported by the safety implementation{color}"

ID	Subtype	Headline and Description
		What does it means exactly? The RTD S32K1 driver should add a detailed explanation for this situation. If don't have a situation occurs as the highlighted content, this content should be removed from UM file. Preconditions: Add detailed explanation Test Case ID (internal TC that caught the defect) optional: None Observed behavior: as Detailed description Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Preconditions
ARTD-66560	Bug	[Port] Wrong configuration file generated Detailed description (how to reproduce it): Adding pins configuration in PinsTool does not automatically add pin configuration in Port HLD driver > this behavior leads to need of manual configuring a new pin in Port HLD and due to fact that this one is not automatically copying the values from pins tool if user does mistakenly configure the values the generated file is wrong Preconditions: add new pin in PinsTool Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: wrong configuration file generated no error or warning hard to check the values in both sides of PinsTool and Port HLD !image-2023-04-28-13-30-51-233.png! !image-2023-04-28-13-31-47-001.png|width=730,height=403! !image-2023-04-28-13-33-00-434.png! Expected behavior: easiness off configuration no error on generated file Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-66938	New Feature	[os] Update copyright template NewWorkDescription: Replace : “(c) Copyright \{year range} NXP Semiconductors All Rights Reserved.” with : Copyright \{year range} NXP !screenshot-2.png! to !screenshot-3.png! Requirement source: as described in “Updating Copyright Years” topic on this guide [https://confluence.sw.nxp.com/display/OSS/File+Headers+-+Copyright+and+License+Information]). (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: as above
ARTD-66959	New Feature	[rte] Update copyright template NewWorkDescription: Replace : “(c) Copyright \{year range} NXP Semiconductors

ID	Subtype	Headline and Description
		All Rights Reserved." with : Copyright \{year range} NXP !screenshot-2.png! to !screenshot-3.png! Requirement source: as described in "Updating Copyright Years" topic on this guide [https://confluence.sw.nxp.com/display/OSS/File+Headers+-+Copyright+and+License+Information]). (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: as above
ARTD-67132	New Feature	[ICU] Improvement to select WKPU channel option NewWorkDescription: For example Target S32K396: To have wakeup on PTD29 which corresponds to WKPU[{*}52{*}] ,under icu configuration we need to configure "IcuWkpuCHannel-->Wkpu Channel" value to \{*}56{*}, ({*}52 offset of 4 internal sources){*} Although natural tendency here is to set 52. No where the documentation suggests the expected channel value is excluding or inclusive of the offset of 4 internal wakeup sources. Requirement source: N/A Proposed solution optional: More convenient and less error prone would be a drop down list of wkpu channel values to select from. Like "WKPU[52]" or "RTI wakeup" etc (instead of only WKPU channel 56)
ARTD-67195	New Feature	[MCU] Check that reserved bitfields from register are not cleared/ are not overwritten. NewWorkDescription: Check that reserved bitfields from register are not cleared/ are not overwritten. Example in Clock_Ip_SetPlldigRdivMfiMfnSdmenSsscgbypSpreadctlStepnoStepsize() in Mcu_TS_T40D11M40I0R0\src \Clock_Ip_Pll.c Issue: It clears the reserved bitfields along with setting the bitfields RDIV and MFI*. According to FMEA, registers should be written with "read-modify-write". Requirement source: Safety requirement, do not overwrite reserved bitfields from registers. Proposed solution optional: [....]
ARTD-67398	New Feature	[IMPLEMENTATION] [S32K3x8] Configuration property to control PMIC_PGOOD_HNDSHK_BYP bit in MCU driver(SetMode func) NewWorkDescription: Add support to configure PMIC_PGOOD_HNDSHK_BYP bit in the MCU configuration. The bit shall be written once at init time, there is no use-case to change it during runtime. Support shall be added to all configurators, on both ASR and non-ASR layers. !image-2023-10-19-10-39-16-841.png! !image-2023-10-19-10-42-21-665.png! !image-2023-10-19-10-43-07-930.png! Requirement source: S32K3xx Reference Manual, Rev.8, Draft B, 9/2023 Proposed Solution:
ARTD-67496	New Feature	[pwm][S32K396] RTD driver enable Pwm_MaskOutputs Api Detailed description (how to reproduce it): The PWM module in RTD driver has a 'Pwm_MaskOutputs' interface, but needs to enable the macro 'PWM_ENABLE_MASKING_OPERATIONS' in configuration tool(EB tresos 29.0). However, it can't be found in EB, and it can't be enabled. We can also see that it called function 'Pwm_Ipw_MaskOutputs' within function'Pwm_MaskOutputs'. But the function 'Pwm_Ipw_MaskOutputs' can't be found in RTD driver. !image-2023-05-08-16-03-31-049.png! !image-2023-05-08-16-04-17-710.png! !image-2023-05-08-16-05-25-035.png! Preconditions: RTD version: SW32K3_RTD_4.4_R21-11_3.0.0_P01_HF01 Configuration tool: EB tresos 29.0.0

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: None Observed behavior: The macro 'PWM_ENABLE_MASKING_OPERATIONS' can't be enabled. And could not find the Ipw layer implementation of the 'Pwm_MaskOutputs' function. Expected behavior: The macro 'PWM_ENABLE_MASKING_OPERATIONS' can be enabled in configuration tool and we can mask pwm submodule output by call function 'Pwm_MaskOutputs'. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-67571	Bug	[CRYPTO] SecondaryInputLength param of MacVerify jobs is measured in bytes when redirection is enabled for SECONDARY_INPUT Detailed description (how to reproduce it): Enable redirection of secondary input and request Crypto driver to process a CMAC, HMAC, GMAC or SIPHASH verify operation Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When redirection is enabled for the secondary input, the Crypto driver code assumes incorrectly that for CMAC, GMAC, HMAC and SIPHASH Verify operations the secondaryInputLength is measured in bits Expected behavior: When redirection is enabled for the secondary input, the Crypto driver code should assume that for CMAC, GMAC, HMAC and SIPHASH Verify operations the secondaryInputLength is measured in bytes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Please find attached 2 source files (before and after) that propose the updates needed in Crypto_Hse.c file of crypto_ng repo. These updates should be tailored over the code of crypto and crypto_ace drivers.
ARTD-70332	Bug	[GPT] The function Pit_Ip_GetLifetimeTimer is not a thread-safe function. Detailed description (how to reproduce it): The function Pit_Ip_GetLifetimeTimer is not a thread-safe function. So, we need an exclusive area for this function. If an interruption occurs after reading the LTMR64H register and before reading the LTMR64L then the after exit interrupt then valueL will not be correct as expected. Test method: Step 1: Insert a code line to trigger an interrupt after reading LTMR64H and before reading LTMR64L. Step 2: In the interrupt function: use a global variable to read the LTMR64L register before performing delay. We should test with delay = 1/2 overflow time of LTMR64L. Step 3: After exiting from the interrupt and completing reading valueL, compare valueL with the global variable above. Preconditions: The additional exclusive area for Pit_Ip_GetLifetimeTimer function. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: as Detailed description Expected behavior: as Preconditions Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: as Preconditions
ARTD-70709	Bug	[ADC] Compile error when enabling Adc Tempsense Api in multi Variant Detailed description (how to reproduce it): If post build is used and more than one post build selectable variant is generated, then get a linker error. In each generated PB variant file the variable AdcVoltageRefs is generated with same name. The variable is used by eclipse\plugins\Adc_TS_T40D34M20I0R0\src\Adc_Sar_Ip.c for the temperature sensor. Preconditions:

ID	Subtype	Headline and Description
		enabling Adc Tempsense Api in multi Variant Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: linker error Expected behavior: no linker error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-70719	Bug	[SPI]Spi_MainFunction_Handling() handled the SPI instances what was configured as synchronous mode Detailed description (how to reproduce it): [There are 2 SPI HW are configured working in synchronous and asynchronous polling modes respectively. Assign 2 SPI HW to 2 Task, synchronous transfer Task1 has lower priority than asynchronous polling transfer Task2. When the Task1 call Spi_SyncTransmit() and polling for push data to FIFO, then the scheduler switches Task1 to high priority Task2. Asynchronous polling transfer Task2 call Spi_MainFunction_Handling() and this function will handle all SPI HW as long as it is in BUSY state even if this SPI HW is working in sync mode (based on configure SpiPhyUnitSync). Return to Task1 but the Lpspi_lp_StateStructureType state has been changed in Spi_MainFunction_Handling() and the synchronous transmission will fail.] Preconditions: [1 SPI HW working in asynchronous polling mode. 1 SPI HW working in synchronous mode. Task scheduler existing.] Observed behavior: [Spi_MainFunction_Handling() handle the SPI HW configured as asynchronous. This is not correct according the SWS_Spi_00361.] Expected behavior: [Add some detection codes to check Spi_apxSpiConfigPtr[SpiCoreID]->HWUnitConfig[HWUnit].PhyUnitConfig->IsSync. The SPI HW which the IsSync field is true should be ignored in Spi_MainFunction_Handling().] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Add some detection codes in Spi_MainFunction_Handling().]

ARTD-70900	Bug	[ETH][GMAC] Gmac_lp_SendFrame: Inappropriate order of writing buffer descriptor
		
		Detailed description (how to reproduce it):
		
		In function Gmac_lp_SendFrame()
		
		{
		Gmac_lp_ChannelType Base;
		Gmac_lp_BufferDescriptorType Bd;
		Gmac_lp_BufferDescriptorType ListBd;
		Gmac_lp_StatusType Status = GMAC_STATUS_SUCCESS; GMAC_DEV_ASSERT(Instance < FEATURE_GMAC_NUM_INSTANCES);
		GMAC_DEV_ASSERT(Gmac_apxState[Instance] != NULL_PTR);
		GMAC_DEV_ASSERT(Ring < Gmac_apxState[Instance]->TxRingCount);
		GMAC_DEV_ASSERT(Buff != NULL_PTR); Base = Gmac_apxChBases[Instance][Ring]; Bd = (Gmac_lp_BufferDescriptorType)Base->DMA_TXDESC_TAIL_POINTER;
		ListBd = (Gmac_lp_BufferDescriptorType)Base->DMA_TXDESC_LIST_ADDRESS; if ((uint32)Bd >= (uint32)&ListBd[Base->DMA_TXDESC_RING_LENGTH 1UL])
		{
		Bd = ListBd;
		} if ((Bd->Des3 & GMAC_TDES3_OWN_MASK) != 0U)
		{
		Status = GMAC_STATUS_TX_QUEUE_FULL;
		}
		else
		{
		Bd->Des0 = (uint32)Buff->Data;

ID	Subtype	Headline and Description

		Bd->Des2 = (uint32)Buff->Length GMAC_TDES2_IOC_MASK GMAC_TDES2_TTSE_MASK;
		Bd->Info0 = (uint32)Buff->Data;
		Bd->Des3 = GMAC_TDES3_FD_MASK GMAC_TDES3_LD_MASK
		(uint32)Buff->Length GMAC_TDES3_OWN_MASK; if (Options != NULL_PTR)
		{
		if (Options->NoInt)
		{
		Bd->Des2 &= GMAC_TDES2_IOC_MASK;
		}
		Bd->Des3 = GMAC_TDES3_CPC(Options->CrcPadIns)
		GMAC_TDES3_CIC(Options->ChecksumIns);
		} Bd++;
		
		/ Issued DMB Before /
		MCAL_DATA_SYNC_BARRIER(); Base->DMA_TXDESC_TAIL_POINTER = (uint32)Bd;
		} return Status;
		}
		
		Above code, the place marked in red programs GMAC_TDES3_OWN_MASK to Des3, For Tx DMA it means that the current BD is already available, but after that the program may update Des2 and Des3 again. This is not a correct programming sequence. GMAC_TDES3_OWN_MASK{color}* {color:#172b4d}should be written at last step in sequence of writing BD.
		
		Preconditions:
		the argument Options* is valid
		
		Test Case ID (internal TC that caught the defect) optional:
		//
		
		Observed behavior:
		//
		
		Expected behavior:
		//
		
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		
		Proposed solution optional:
		//

ARTD-70980	Bug	[MEM_INFLS] PFLASH: Read-While-Write to the same block may return incorrect read data NewWorkDescription: PFLASH: Read-While-Write to the same block may return incorrect read data Requirement source: [Zebra S32K3x4 0P55A_1P55A Errata Rev14_Oct_2021.pdf All Documents (sharepoint.com)|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FErrata%2FS32K3x4%200P55A%5F1P55A%20Errata%20Rev14%5FOct%5F2021%2Epdf&viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FErrata] : ERR051061 Proposed solution optional: There are 2 workaround options: 1) The software can read the Read-While-Write Event Error bit in the Module Configuration Status register (MCRS[RWE]) after system bus reads to make sure there’s no error. In case of error, discard system read data and perform reads again. 2) Avoid Read-While-Write to the same block at the first place. The software shall use synchronization when sharing flash block by multiple masters similar to sharing other hardware resources.
ARTD-71320	New Feature	[MCU] Flash wait states should be in sync with data sheet NewWorkDescription: Flash wait states should be in sync with data sheet Requirement source: Proposed solution optional:

ARTD-71695	Bug	[MEM_EXFLS][QSPI] Add support to escape from being stuck in BUSY state
		
		The customer's code will be stuck in the BUSY state after several read/write operations, until timeout, and loopback again and then still BUSY and timeout.
		do
		{
		/ Add Fault Injection point for FR_ILLINE flag /
		MCAL_FAULT_INJECTION_POINT(FLS_FIP_FR_ERROR_ABORTSUSPEND);
		
		status = Qspi_Ip_ControllerGetStatus(controllerInstance);
		Fls_Qspi_u32ElapsedTicks = OsIf_GetElapsed(&Fls_Qspi_u32CurrentTicks, (OsIf_CounterType)QSPI_IP_TIMEOUT_TYPE);
		if ((STATUS_QSPI_IP_BUSY == status) && (Fls_Qspi_u32ElapsedTicks >= Fls_Qspi_u32TimeoutTicks))
		{
		(void) Det_ReportRuntimeError((uint16)FLS_MODULE_ID, FLS_INSTANCE_ID, FLS_MAINFUNCTION_ID, FLS_E_TIMEOUT);

ID	Subtype	Headline and Description

		status = STATUS_QSPI_IP_TIMEOUT;
		}
		}
		while (STATUS_QSPI_IP_BUSY == status);
		
		Customer's general boot flow:
		1. BootROM(QSPI AHB): using QSPI reconfig parameter 133MHz DDR mode
		2. bootloader(QSPI AHB)-> reuse BootROM settings
		3. M7 AutoSRA(QSPI AHB)-> will call Fls_Init function, after do some write and read, using AHB read via DMA to load uboot code
		4. U-boot
		
		Questions:
		1. The API to reset QSPI after the timeout invoked by monitoring the 'BUSY'. Now, we're trying with Fls_IPW_InitControllers.
		Please see the attached mail to get the detailed modification. This seems can fix their currently BUSY issue. Is it reasonable ?
		
		2. If the AHB reading is invoked during the Fls operation, is it possible to get the QSPI stuck at 'BUSY' state ?
		3. The API to provide the status of flash/qspi which could tell that the AHB reading by the other software module is safe. Currently, below APIs are being used.
		/ Start DMA transfer /
		if(1==Fls_GetStatus() && (2==Fls_GetJob()))
		{
		/*AHB read code*/
		}
		4. The recommended setting of the timeout to monitor the 'BUSY'.
		Please see the attached mail to get the details. Do we have some suggestions about those timeout values?

ARTD-71744	Bug	[k3] Ocotp no error for unsupported derivative Detailed description (how to reproduce it): Install the release, create a new project, add Ocotp, set the resources s32k358_mapbga289, generate code for the current project. Preconditions: EBT 29.2.0 SW32K3_RTD4.4_R21-11_3.0.0_D2303.exe Test Case ID (internal TC that caught the defect) optional: Observed behavior: Failed to run generator for Ocotp: !image-2023-05-30-14-46-23-405.png! Expected behavior: Should receive an warning message which tells us that for S32K derivative, Ocotp is unsupported. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-71948	New Feature	[CRYPTO_NG] Add support for HashEdDSA(ED25519ph) NewWorkDescription: Add support in the existing signature generation and verification code for HashEdDSA(ED25519ph). The HSE firmware supports this service via bHashEddsa parameter: !image-2022-03-23-15-42-11-081.png! Autosar specification does not support this service so an extension to the Crypto_AlgorithmFamilyType must be made by adding a new define like CRYPTO_ALGOFAM_ED25519PF. !image-2022-03-23-15-44-25-331.png! In the internal function Crypto_Hse_FillSignRequestDescriptor() the HSE descriptor must be filled in accord with the primitive configured in the job: !image-2022-03-23-15-39-59-535.png! Requirement source: Customer

ID	Subtype	Headline and Description
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update the configuration with a new Crypto_AlgorithmFamilyType that represent the service and the code in order to fill the descriptor accordingly.
ARTD-72070	Bug	[ADC] Function 'Adc_EnableHardwareTrigger' exception when enabled 'ADC_IPW_SDADC_IS_USED' and 'SDADC_IP_DSPSS_ENABLED' Detailed description (how to reproduce it): We need call function 'Adc_EnableHardwareTrigger' to enable IP SARADC. At the same time, SDADC also need to be used in our project. Before macro 'ADC_IPW_SDADC_IS_USED' and 'SDADC_IP_DSPSS_ENABLED' enable, SARADC initialization work normally. But SARADC initialization exception (hard fault), which is caused by array access out of bounds. In function 'Adc_Ipw_SetupTcdSingleAdcChannel' and 'Adc_Ipw_SetupTcdLastSourceAddressOffset', they call function 'DSPSS_ThreadGetOutputBufferLength', it maybe the root cause of hard fault. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: hard fault. !image-2023-06-01-10-25-32-760.png! Expected behavior: SARADC initialization work normally. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-72195	Bug	[S32K3XX][MEM_EEP] Driver does not support Burst feature Detailed description (how to reproduce it): Driver does not support Burst feature on mem_eep Preconditions: Enable burst setting Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-72283	Bug	[ADC] DSPSS APIs not convenient for split usage Detailed description (how to reproduce it): The APIs of DSPSS do not support the configuration for threads in different cores. All threads must be configured together, which does not satisfy customers' requirements for two motor control applications. They hope to configure the ADC and DSPSS thread for different motors on different cores and the configuration can be controlled independently. The APIs, for now, can only configure the parameters at one core. For example, function 'DSPSS_RetCode_t DSPSS_Start(void)'. Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [.] Observed behavior: [n/a] Expected behavior: [n/a] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-72327	Bug	[pwm] checks for Core reference even though Multicore feature is not enabled Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		In the file {*}Pwm_PBcfg.c{*}, even though the parameter PwmMulticoreEnabled is set to FALSE, it will still try to loop over OsApplication for OsApplicationCoreRef. This check should be performed only if PwmMulticoreEnabled is enabled. Pwm_PBcfg.c: [!LOOP "as:modconf('Os')[1]/OsApplication/*"!] [!SELECT "node:ref(./OsApplicationCoreRef/*[1])"!] [!IF "$numPartition < node:value(./EcucCoreId)"!] [!VAR "numPartition" = "node:value(./EcucCoreId)"!] [!ENDIF!] [!ENDSELECT!] [!ENDLOOP!] Preconditions: Multicore feature is not enabled Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: checks for Core reference even though Multicore feature is not enabled Expected behavior: don't check for Core reference if Multicore feature is not enabled Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: When checking how OsApplicationCoreRef is checked in other Drivers, we see that it is checked for e.g. only when ChannelEcucPartitionRef is configured, e.g. from DIO: [!LOOP "DioChannelEcucPartitionRef/*"!][!// [!VAR "DioCrtPart" = "node:value(.)"!][!// [!LOOP "as:modconf('Os')[1]/OsApplication/*"!][!// [!IF "$DioCrtPart = node:value(./OsAppEcucPartitionRef/*[1])"!][!// [!SELECT "node:ref(./OsApplicationCoreRef/*[1])"!][!// [!VAR "GetThePartitionNumber"="node:value(./EcucCoreId)"!][!// [!VAR "PartitionChannelValue"="bit:or($PartitionChannelValue,(bit:shl(1,$GetThePartitionNumber)))"!][!// [!ENDSELECT!][!// [!ENDIF!][!// [!ENDLOOP!][!// [!ENDLOOP!][!//
ARTD-72501	Bug	[ADC] Problem with ProfileReport of Adc_Calibrate function Detailed description (how to reproduce it): ProfileReport for Adc_Calibrate at version SW32K3_RTD_4.4_2.0.0 was wrong. It reported about 1.527us for the execution time. While it is measured about 1100us in realtime Open Adc_Example and connect a pin port to Logic analyze to measure the time of Adc_Calibrate: set pin to High when Adc_Calibrate and set to Low after finish. !image-2023-06-07-10-10-01-598.png! The time noticed on Logic Analyze 1100us Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The time noticed on Logic Analyze 1100us. While ProfileReport only 1.5us Expected behavior: ProfileReport should equivalent with actual timing for this function Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-72584	Bug	[PWM-FLEXIO][S32DS] Build failed: Inconsistent between file name and include file Detailed description (how to reproduce it): {*}Step 1{*}: Create a new project {*}Step 2{*}: Add Mcl, Mcu, Pwm {*}Step 3{*}: Configure PWM over flexio {*}Step 4{*}: Update code {*}Step 5{*}: Build

ID	Subtype	Headline and Description
		{*}Note{*}: I already checked on both the latest tags of S32K3-S32M27x RTD ASR 4.7 v3.0.0 release and the Update site. I got the same result. I attached the s32ds project in the attached file (zip). You can import and reproduce this issue. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Build fail: workspaceS32DS.3.5.1/pwm_issue1_M7_0_0/generate/include/Flexio_Pwm_Ip_Cfg.h:54:10: fatal error: Flexio_Pwm_Ip_BOARD_InitPeripherals_PBcfg.h: No such file or directory Expected behavior: Build successfully without errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-72603	Bug	[PWM-FLEXIO][S32DS] Build failed once ComponentGenerationMethod is FunctionalGroups Detailed description (how to reproduce it): {*}Step 1{*}: Create a new project {*}Step 2{*}: Add Mcl, Mcu, Pwm {*}Step 3{*}: Configure PWM over flexio {*}Step 5{*}: Go to Global Setting, change ComponentGenerationMethod to FunctionalGroups {*}Step 5{*}: Update code {*}Step 6{*}: Build {*}Note{*}: I already checked on both the latest tags of S32K3-S32M27x RTD ASR 4.7 v3.0.0 release and the Update site. I got the same result. I attached the s32ds project in the attached file (zip). You can import and reproduce this issue. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Build fail: generate/src/Pwm_BOARD_InitPeripherals_PBcfg.c:162:34: error: 'FLEXIO_PWM_IP_BOARD_INITPERIPHERALS_I0_CH0_CFG' undeclared here (not in a function); did you mean 'FLEXIO_PWM_IP_BOARD_InitPeripherals_I0_CH0_CFG'? 162 (Pwm_IpwInstanceType)FLEXIO_PWM_IP_BOARD_INITPERIPHERALS_I0_CH0_CFG, FLEXIO_PWM_IP_BOARD_InitPeripherals_I0_CH0_CFG make: [generate/src/subdir.mk:86: generate/src/Pwm_BOARD_InitPeripherals_PBcfg.o] Error 1 make: Waiting for unfinished jobs.... Expected behavior: Build successfully without errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number, etc.) Proposed solution optional: [....]
ARTD-72698	Bug	[BASE] StandardType are missing suffix U in definition Detailed description (how to reproduce it) There are many macro define in StandardTypes.h are missing U as suffix for definition. Where it actually need to define as unsigned int according to Autosar Spec !image.png|width=464,height=223! eg: brief Logical state active. implements SymbolDefinitions_enum*/#define STD_ACTIVE 0x01 / brief Logical state idle. implements SymbolDefinitions_enum*/#define STD_IDLE 0x00 / brief ON State. implements SymbolDefinitions_enum*/#define STD_ON 0x01

ID	Subtype	Headline and Description
		/ brief OFF state. implements SymbolDefinitions_enum*/#define STD_OFF 0x00 / brief Return code for failure/error. implements SymbolDefinitions_enum*/ #define E_NOT_OK 0x01 Preconditions: Using Base module Test Case ID (internal TC that caught the defect) optional: NONE Observed behavior: Miss match in type Expected behavior: No miss match in type Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Define as Autosar Specification
ARTD-73018	Bug	[ADC] Not return Det error ADC_E_UNINIT when call function before Adc_Init function Detailed description (how to reproduce it): some function called Adc_ValidateCtuControlModeApi before Adc_Init function but return report error ADC_E_UNINIT In code shall return ADC_E_CONTROL_MODE_DISABLED with req Adc_Init() was not called before this function CTU Control Mode is disabled (shall report ADC_E_CONTROL_MODE_DISABLED) !image-2023-06-02-14-28-56-846.png! Preconditions: ADC_ENABLE_CTU_CONTROL_MODE_API = STD_ON Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0702 Adc_TS_012 Observed behavior: not return ADC_E_UNINIT when call some function before Adc_Init function Expected behavior: return ADC_E_UNINIT when call some function before Adc_Init function Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-73320	New Feature	[IMPLEMENTATION] [ETH] Analyze the possibility of adding multi buffer support for TX and RX CR description: The customer needs a way to create a lot "small" buffers where large frames take up multiple slots. Therefore, assume they can configure the driver for 125 buffers of 64-bytes. If they transmit a 100 byte message, it will take up to 2 buffer slots. If they transmit a 512-byte message, it will take up to 4 buffer slots, etc. This gives them a deeper buffer queue when most of my traffic is "smaller" frames but still flexible enough for the occasional large frame. And this is similar for the reception side. If their max frame size is 1500 (because they have 1 or 2 frames of that size), their FIFO buffer will only be 15 deep. So let's say 90% of their traffic is <=256 bytes, this means most of their buffer has been wasted just to cover a couple of large slow frames. Ideally they would like to implement this feature with the built in buffers so they do not have to give up RAM for these buffers. As reference, there is a similar feature from the MPC5777C. Reason for this change: Comet request Benefit: Providing flexibility needed when most traffic is using small frames, so that a bigger number of buffers can be defined, being also able to send/receive bigger frames than the defined size of the frame. Onetime CR/Strategic CR: Strategic CR Use-case: Comet use-case HW documentation reference (as applies): N/A HW/Application Engineer contact (as applies): N/A Note: relevant documents to be attached to the ticket.

ID	Subtype	Headline and Description

ARTD-73728	Bug	RWSC set to reserved value(0) leading to HW fault
		
		In the function Clock_Ip_CodeInRamSetFlashWaitStates() in Clock_Ip_Specific.c , when setting the RWSC, it was written to 0 first which is not necessary. Customer report it will lead to Hard fault in IAR environment. Though it didn't happen in the S32DS, but can you check whether it's better to delete the write 0 code(IP_FLASH->CTL &= FLASH_CTL_RWSC_MASK) ;.
		
		IP_FLASH->CTL &= FLASH_CTL_RWSL_MASK; // this code is not meaningful since RWSL is not clearable by a register write
		IP_FLASH->CTL &= FLASH_CTL_RWSC_MASK; //this code shall be deleted.
		IP_FLASH->CTL = FLASH_CTL_RWSC(RwscSetting); // need to replace "|=" with "="
		
		Please also check whether it's better to use below code which will check RWSL before writing RWSC. This workaround is to reduce the risk of HardFault occurence, but not sure whether it is enough to completely eliminate the HardFault. Would you please come up with any idea how we could completely suppress the instruction prefetch from flash during the CTL[RWSC] register modification? We may also need ISB instruction in addition to DSB instruction.
		
		!image-2023-06-21-11-39-49-065.png|thumbnail!

ARTD-74063	New Feature	[Dpga] implement the feature Functional self-test for the amplifier and the voltage monitoring NewWorkDescription: According S32M24x Reference Manual, Rev. 2 Draft A, 05/2023 implement the feature "Functional self-test for the amplifier and the voltage monitoring" !image-2023-06-23-18-00-50-737.png! Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-74257	Bug	[Rm] Wrong EMAC AHB MDAC generated in Tresos configuration for S32K342 Detailed description (how to reproduce it): When configuring S32K342 in EB Tresos, added master Xrdc_0_EMAC_AHB*, XRDC_MDAC4 is generated instead of XRDC_MDAC5 in Xrdc_Ip_PBcfg.c*. According to Table 67. MDAC configuration, Chapter 19, S32K3xxRM_Rev7*, MDAC4 is not available on K342. Preconditions: Configure XRDC domain in Rm module and add master Xrdc_0_EMAC_AHB*. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Generating XRDC_MDAC4 for master Xrdc_0_EMAC_AHB (XRDC_MDAC5) Expected behavior: Generate XRDC_MDAC5 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix Rm module resources for S32K342 derivative.
ARTD-74547	Bug	[I2C]Multiple definition cause a compilation error Detailed description (how to reproduce it): When I2cErrorCallback was enabled. I2C_MASTER_EVENT_ERROR_FIFO appeared at 2 places: In Lpi2c_Ip_MasterEventType enum in the file Lpi2c_Ip_Callbacks.h Macro generated in the file CDD_I2c_Cfg.h. This caused a compilation error. Preconditions: I2cErrorCallback was enabled Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Has a compilation error. Expected behavior: Has no compilation error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Rename one of them if all of them need to declared and used.
ARTD-74632	Bug	[ADC] Autosar RTD drivers for S32K396 are missing example for SDADC + CoolFlux DSP config Detailed description (how to reproduce it): There is missing example code how to configure SDADC together with CoolFlux DSP in Autosar RTD drivers. Customer is asking for such an example since they are struggling to use RTD drivers to configure SDADC and CoolFlux.

ID	Subtype	Headline and Description
		Also it was requested that single function call would be used to configure the entire SDADC CoolFlux FW so the customer is shielded from the DSPSS configuration and only would see that as SDADC module configuration. Preconditions: there is single function call that configures the SDADC+CoolFlux DSP with input parameter structure that is generated by the config tool. Test Case ID (internal TC that caught the defect) optional: no ID Observed behavior: Multiple function calls are needed to perform to get SDADC and CoolFlux configuration. Plus CoolFlux configuration cannot be done through the config tool, I had to perform this manually. Also the description of the individual function calls in the attached documentation if quite poor. Expected behavior: Proposed solution optional: There is a single function call for entire SDADC CoolFlux DSPSS config with single structure holding the config parameters
ARTD-74755	Bug	[I2C] Missing 'I2c' prefix in Resource files Detailed description (how to reproduce it): Missing 'I2c' prefix for 2 variable in resource file : I2cUnifiedInterrupts:TRUE and I2cMulticoreSupport:TRUE Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing 'I2c' prefix for 2 variable in resource file : I2cUnifiedInterrupts:TRUE and I2cMulticoreSupport:TRUE Expected behavior: All variables in Resource files will be added 'I2c' prefix Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add for I2cUnifiedInterrupts:TRUE and I2cMulticoreSupport:TRUE
ARTD-74847	Bug	[S32M24x] [Gdu] [S32K1_M24x 2.0.0] [S32DS] Gdu build fail in CDD_Gdu_Cfg.h and Gdu_Ip_Cfg.h when User use S32DS Detailed description (how to reproduce it): In CDD_Gdu_Cfg.h, GDU_CFG_VENDOR_ID redefine into GDU_VENDOR_ID_CFG make application build fail In CDD_Gdu_Cfg.h, GDU_IP_NOTIFICATION do not define, it makes the User application build fail when enabling interrupt Preconditions: Gdu has no warning and builds fail in the driver code Test Case ID (internal TC that caught the defect) optional: Gdu_TS_COT_005 use s32ct as generator Observed behavior: GDU_CFG_VENDOR_ID redefine into GDU_VENDOR_ID_CFG make application build fail Expected behavior: Gdu has no warning and builds fail in the driver code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: n/A
ARTD-74968	Bug	[ADC] Missing ADC channels of D2D interface Detailed description (how to reproduce it): bug found in RTD 3.0.0 for s32M27 !image-2023-07-03-09-33-23-711.png! In ADC and BCTU driver there are missing channels used for D2D connection. see S32M27x_RM attachment S32M27x_IOMUX.xls tab D2D Interface. !image-2023-07-03-09-38-03-469.png!

ID	Subtype	Headline and Description
		!image-2023-07-03-09-39-27-285.png! Expected behavior: D2D connection is essential part of the S32M and should be configurable from Config tools as well as from Tresos
ARTD-74975	New Feature	[CRYPTO_NG] Key import update NewWorkDescription: Bring the changes from key import made on crypto repo (ASR 4.4) on ticket ARTD-40110 to crypto_ng. Requirement source: HSE (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Port the implementation from ARTD-40110
ARTD-75008	Bug	[ADC] DSPSS FW Thread failed to re-enable after suspend Detailed description (how to reproduce it): After initializing threads 0 & 1, and also start them. Then suspend thread #0. later re-enable thread #0. Thread 0 seems failed, the DMA trigger from thread 0 cannot be observed anymore. After initialization, using the DSPSS_ThreadEnable() function to start the {*}thread 0 & 1{*}. Then using DSPSS_ThreadSuspend() function to suspend the thread 0. Later, using the DSPSS_ThreadEnable() function to re-enable the thread 0 again. It failed. Preconditions: n/a Test Case ID (internal TC that caught the defect) optional: Observed behavior: Thread 0 failed, no DMA trigger from thread 0 anymore. Expected behavior: Running well with the right DMA trigger signal. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-75102	Bug	[SPI] Error on compilation when using SpiDmaContMemTransferSequenceEnable feature on S32DS Detailed description (how to reproduce it): When enable DMAContMem Feature, but not all sequences use that feature (enable SpiDmaContMemTransferSequenceEnable), it will have error on compilation step. The other cases is good. Preconditions: S32DS configuration Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: error on compilation step Expected behavior: compile successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Spi_PBcfg.c should be modified to check SpiDmaContMemTransferSequenceEnable for NULL_PTR or Spi_DmaConMemTransferTxSeq address
ARTD-75115	Bug	[S32M24x] [Gdu] [S32K1_M24x 2.0.0] Generate false config struct for INTEN field Detailed description (how to reproduce it): When enable low side interrupt node in tresos, the generated config struct won't match the config in EB. Preconditions: GduDesaturationLs0IE, GduDesaturationLs1IE, GduDesaturationLs2IE are enabled. Test Case ID (internal TC that caught the defect) optional: Observed behavior: Generated struct have the wrong values. The struct point to the wrong node and have the wrong mask for INTEN bit field.

ID	Subtype	Headline and Description
		Expected behavior: The INTEN register value should match the configuration in EB. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update source code of the generate config struct part to have it take the value of the correct node and use the correct mask in the struct.
ARTD-75228	Bug	[I2C] I2c Baud Rate node cannot update value immediately on S32DS Detailed description (how to reproduce it): !image-2023-06-23-11-05-02-327.png|thumbnail! On S32DS when we change value of two node I2c Clock High Period and I2c Clock Low Period then value of I2c Baud Rate node doesn't change immediately. It take some time can be changed or cannot change if this current value of node violate the constraint. So it cause the upset for user Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: On S32DS when we change value of two node I2c Clock High Period and I2c Clock Low Period then value of I2c Baud Rate node doesn't change immediately Expected behavior: On S32DS when we change value of two node I2c Clock High Period and I2c Clock Low Period then value of I2c Baud Rate node change immediately Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Current the value of I2c Baud Rate node is being calculated and updated on file Lpi2c_Ip_PBcfg.c, so we can move this calculation into the template file and change the node type as `info`
ARTD-75399	New Feature	[GDU] Add user mode support NewWorkDescription: Add a configuration parameter for user mode support Requirement source: CPR_RTD_00352.gdu Proposed solution optional: [....]
ARTD-75484	Bug	[MemAcc] The start address of subAddressArea does not match with size of sector batch Detailed description (how to reproduce it): when i set a value which does not match with size of sector batch at MemAccLogicalStartAddress node and saw that no any error as show in attched picture . Size of sector batch is 4096 but i set 2048 saw that no any error Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: when i set a value which does not match with size of sector batch at MemAccLogicalStartAddress node and saw that no any error as show in attched pciture Expected behavior: it must have error when user set a value does not match with size of sector batch Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update check validation or automaton set value when user add more subaddressArea
ARTD-75490	New Feature	[wdg] Implement Fault watchdog feature NewWorkDescription: Implement Fault watchdog for observing interrupt responses. Requirement source: S32M27x Reference Manual, Rev. 1, 08/2022, [LINK|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32M27x%2FRM%2FS32M27x%5FRM%5FRev2%5FDraftB%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32M27x%2FRM] Proposed solution optional:

ID	Subtype	Headline and Description
		Add Fault Watchdog to AeWdog Instance, support configuration to enable and initialize timeout duration: development activities: add checkbox: enable fault watchdog => generate a macro in code to guard relative code. add textbox for timeout duration => generate variable and add to config structure => add new code to write this value into register FAULT_WD_CFG (perform when calling Wdg_43_Instance4_Init) testing activities: create new test case with fault event to trigger an interrupt. run test, debug and check result.
ARTD-75894	Bug	[ADC] DSPSS Thread buffers params cannot be configured Detailed description (how to reproduce it): The buffer length in the parameter "ThreadDescriptors" should be changeable. However, there is no api or configuration items for that. The buffer length for input or output might be different from the default params given by the DSPSS FW. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Observed behavior: No way to modify them. Expected behavior: They are available to be modified by users. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-76029	New Feature	[I2C] Add guard LPI2C_IP_COMMON_IRQ_MASTER_AND_SLAVE for function Lpi2c_Ip_ModuleIRQHandler NewWorkDescription: The function Lpi2c_Ip_ModuleIRQHandler is only used if LPI2C_IP_COMMON_IRQ_MASTER_AND_SLAVE is defined. Please investigate and guard all the codes related to this macro to reduce code size Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A
ARTD-76047	Bug	[WDG] Driver does not check lock bit for FAULT WDG Detailed description (how to reproduce it): 1. Driver does not check lock bit for FAULT WDG before write into FAULT WDG configuration !image-2023-07-10-13-35-59-217.png|width=490,height=236! !image-2023-07-10-13-34-19-176.png|width=491,height=339! 2. The unlock sequence need to be correctly, the Private key to be used when writing to LOCK fields !image-2023-07-10-13-44-49-446.png|width=721,height=234! !image-2023-07-10-13-44-00-901.png|width=722,height=112! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Wdg_TS_200 Observed behavior: See the description Expected behavior: See the description Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-76050	Bug	[WDG] AE Wdg can not change mode Detailed description (how to reproduce it): Init AE WDG Change current mode to Fast/Slow/OFF mode AE of S32K1 support re-configuration at run time, but driver does not support change wdg mode.

ID	Subtype	Headline and Description
		Preconditions: Test Case ID (internal TC that caught the defect) optional: Wdg_TC_FCT_0301 Observed behavior: EB configuration does not support mode setting of AE Wdg. !AE_bug.PNG|thumbnail! Expected behavior: EB support mode setting and changing mode Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-77903	Bug	[Gdu] Can't config multi variants with different values in S32DS Detailed description (how to reproduce it): Config multiple variants in S32DS Preconditions: More than 1 variant used Test Case ID (internal TC that caught the defect) optional: Observed behavior: All variants are having the same config values Expected behavior: Each variant can have its own values. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove SYNV_VALUE and update postBuildVariantValue in Gdu.template might fix it.
ARTD-78647	Bug	[I2C] Macros following generate are uncapitalized. Detailed description (how to reproduce it): Because the macros in the generate file are not capitalized, the build process will fail. !image-2023-07-19-10-38-13-616.png! Preconditions: Create test for I2C or use Dev_test TS_I2C_0999. Rename VS_0 to boarrdddd. !image-2023-07-19-10-41-55-949.png! Update again for EcuC !image-2023-07-19-10-43-08-491.png! Re-generate and build. Test Case ID (internal TC that caught the defect) optional: TS_I2C_0999 Observed behavior: The macros in the generate file are not capitalized. Expected behavior: The macros in the generate file are capitalized. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-79139	Bug	[AE] EVENTS_STATUS[FRAMEWIDTH _FL] bit is sometimes set after calling AE_Init() Detailed description (how to reproduce it): After calling AE_Init(), EVENTS_STATUS[FRAMEWIDTH FL] bit is sometimes set (Indicates that the duration of an SPI access was not as expected). This causes the test to be unstable (randomly passed or failed). Then I added a delay before calling Ae_Init() > the test passed. After investigating, I see that the driver code is not implemented to check if AE is booted successfully before accessing to it. The issue I mention above shall come from this. !image-2023-07-21-17-24-19-451.png! Preconditions: EVENTS_ENABLE[FRAMEWIDTH_EN] bit must be set Test Case ID (internal TC that caught the defect) optional: Ae_TS_014 Observed behavior:

ID	Subtype	Headline and Description
		Test randomly failed at Eu_assert() Expected behavior: Test passed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-79773	Bug	[SPI][S32K3XX] Implement workaround for the new ERR051588 NewWorkDescription: Implement workaround for the new ERR051588. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: When clearing the transmit error flag (SR[TEF] = 0b1) following a transmit FIFO underrun, reset the transmit FIFO (CR[RTF] = 0b1) before writing any new data to the transmit FIFO.
ARTD-79894	Bug	[GPT][RTD_RTM_3.0.0] Build fail on the S32DS for S32K328, S32K338, S32K348 Detailed description (how to reproduce it): In sdk_manifest_gpt.xml file, line Rte_Gpt is missing S32K328 S32K338 S32K348 derivatives, leads to fail at building on S32DS Expected behavior: Add S32K328, S32K338, S32K348 line 59 (https://bitbucket.sw.nxp.com/projects/ARTD/repos/gpt/browse/specific/S32K3XX/generate/UCT/sdk_manifest_gpt.xml?at=refs%2Ftags%2FGPT_331)
ARTD-79961	Bug	Power_Ip Power_Ip_MC_RGM_ResetInit() The power_ip driver should always clear the DRET, FRET registers in Power_Ip_MC_RGM_ResetInit() if the escalation is disabled. That means if MC_RGM_FRET_FRET((uint32)0U), MC_RGM_DRET_DRET((uint32)0U) in Power_Ip_MC_RGM_ConfigPB. Currently, DRET is cleared only after POR and FRET is cleared only after a DES reset.
ARTD-80329	Bug	[OCU][S32M27X] Fix VSMD rule TpsEcuc_08033 violation, for OcuHWSpecificSettingsRef parameter Detailed description (how to reproduce it): Generate the VSMD report and check the rule violation "TpsEcuc_08033", inside the report. !image-2023-03-17-08-48-36-413.png! Preconditions: Build OCU plugins Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: TpsEcuc_08033 rule violation. Expected behavior: No violation related to TpsEcuc_08033 rule. Proposed solution optional: NA
ARTD-80489	Bug	[GPT] POSTBUILD option: Lacking include .h files in generated Emios_Gpt_Ip_Cfg.h file Detailed description (how to reproduce it): We’ve created 3 different configuration(B_SAMPLE, B2_SAMPLE, C_SAMPLE) to handle different HWs. By enabling this option in tresos, the generator creates one “PBcfg.h” file for each configuration from each module(see picture 1). !PICTURE_1.png|width=406,height=468! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The thing is that we noticed not all the “cfg.h” files include the 3 “PBcfg.h” files created for each configuration

ID	Subtype	Headline and Description
		Eg the Emios_Icu_Ip_Cfg.h file includes the 3 "PBcfg.h" files(see picture 2) but the Emios_Gpt_Ip_Cfg.h and Rtc_Ip_Cfg.h files not. They just include the latest POSTBUILD configuration created(see picture 3) Is this correct? Shouldn't they have the 3 "PBcfg.h" files(see picture 2) include in it like the Emios_Icu_Ip_Cfg.h file? !PICTURE_2.png|width=446,height=375! !PICTURE_3.png|width=445,height=349! Expected behavior: The included .h files should be the same with Emios_Icu_Ip_Cfg.h Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-80512	Bug	[k3] I2c configuration imported with error from Tresos to Design Studio All the errors have been fixed, the code generated, and build. When the Application was exported from Tresos to Design Studio, in DS we have the error from the image attached. The I2c Baud Rate in Tresos was set to 0 and in DS it have an outrange value. Also if you want set another value/default value it will be overwrite with the same outrange value. please take a look at the following picture, I saw that there is a setValue function called. So doesn't matter what value we set, all the time will have that outrange value. !image-2023-08-01-16-51-05-886.png!
ARTD-81124	Bug	[MCL] Update resource files with additional fields related to cache types available Detailed description (how to reproduce it): During S32N development some restriction were added related to CacheEnable field in Tresos. Because not all cores support L1 caches the CacheEnable field shall be editable only for cores that support L1 cache. For this reason the following fields were added in resource files. " Mcl.Cache.L1RCore:1 Mcl.Cache.L1MCore:0 Mcl.Cache.Lmem:0 " Because the rest of the platforms are missing the above information in resource files the CacheEnable field in Tresos is not editable thus the user is not able to enable Cache support. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CacheEnable field in Tresos is not editable for platforms that support L1 cache. Expected behavior: CacheEnable field shall be editable for cores that support L1 cache and for those that do not support L1Cache the field shall be greydout. Proposed Solution: Changes made in ARTD-79915 shall be reverted and the resource files shall be updated (with the fileds mentioned above) for all platfomrs with L1 cache. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-81841	Bug	[I2C] S32K3 LPI2C slave bus hang issue Detailed description (how to reproduce it): The issue is happend in S32K144, and as the analysis, it can occur in S32K3 also: LPI2C is used as I2C slave device in this project. With low probability, I2C bus will be hung and can't be recover anymore. Please see below picture, SDA and SCK keep as low after the issue. Reset I2C master device can't recover the BUS neither !image-2023-08-09-10-30-43-260.png! In detail, please see the attached file. It included the analysis and proposed solution Preconditions: N/A Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		N/A Observed behavior: Sometimes the Repeated Start Flag and Address Valid Flag both set in 1 IRQ function handler occasionally Expected behavior: If Repeated Start Flag and Address Valid Flag both set in 1 IRQ function handler, the handle for Repeated Start Flag should be handled first. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-82347	Bug	[k3] Mcu configured in DS was imported in Tresos with error Detailed description (how to reproduce it): Install SW32K3_RTD_4.4_R21-11_3.0.0_D2303_DS_updatesite, Configure the Mcu and export it to Tresos. (without errors) Import the Mcu in Tresos and check if it have any error. Preconditions: EB Tresos version 29.2 Design Studion version 3.5 Test Case ID (internal TC that caught the defect) optional: Observed behavior: The Mcu imported in Tresos have an error as you can see in the picture: !https://confluence.sw.nxp.com/download/attachments/283895473/image-2023-7-26_11-44-31.png?version=1&modificationDate=1690361072145&api=v2! Expected behavior: Shouldn't have any error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-82369	New Feature	[SPI] Add supporting Byte Swap configuration NewWorkDescription: Add supporting Byte Swap configuration !image-2023-08-11-16-12-56-569.png|thumbnail! Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-82583	Bug	[Mem_43_INFLS]: Inappropriate check rule for the access code ram addr Detailed description (how to reproduce it): The access code erase/write address is mandatory, this is unreasonable because I have configured the pointer below. From my understanding, just choose between these two places. !image-2023-08-15-11-23-01-143.png|width=495,height=417! Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: None Expected behavior: None Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-82592	Bug	[FEE]: Verify error, but can generate code normally. Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Verify error, but can generate code normally. !image-2023-08-15-12-39-46-568.png! Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: None Expected behavior: None Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-83569	New Feature	[IMPLEMENTATION][ETH][GMAC] Add the buffer index as an output parameter to SendMultiBufferFrame and Eth_SendFrame CR description: The APIs introduced for zero-copy, for sending frames from external buffers don't have the possibility of linking the sent frame with a confirmation from the EthIf. In order to support this, the HLD APIs that are used for sending frames should have an output parameter to give to the application a buffer index to be used for connecting the sent frame with a confirmation response Reason for this change: Improving the integration of zero-copy APIs with the Ethernet stack Benefit: The possibility of linking the sent frame with a TX confirmation Onetime CR/Strategic CR: Strategic CR Use-case: Zero-copy APIs are used HW documentation reference (as applies): N/A HW/Application Engineer contact (as applies): N/A Note: relevant documents to be attached to the ticket.
ARTD-83827	New Feature	[mem_exfls] Update suspend/resume to cover some usercases with 2 external flashs for other platforms NewWorkDescription: Update suspend/resume to cover some usercases with 2 external flashs, when user have 2 external inwhich one of them does not support resume/suspend Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-83876	Bug	HSE_CLK set to 120MHZ leads to S32K312 RESET When creating a new S32DS RTD3.0.0 project for S32K312, the default clock combination is CORE_CLK = 120MHZ; AIPS_SLOW_CLK = 30MZ; HSE_CLK = 120MHZ. The ratio of AIPS_SLOW_CLK to HSE_CLK is 1:4. which does not match the default UTEST setting(HSE_CLK_MODE_AND_GSKT_CTRL). I would suggest to change the HSE_CLK to 60MZ ,which is the same as old RTD version.
ARTD-84029	Bug	[MEM_INFLS]: C40 Array Integrity Check will go into hard fault Detailed description (how to reproduce it): When I try to do C40 Array Integrity Check by call the API: C40_Ip_ArrayIntegrityCheck. System will go into hard fault. After verification, we need to reallocate all the functions used/called in this function to the RAM. Mainly include three functions: C40_Ip_ArrayIntegrityCheck C40_Ip_CheckUserTestStatus DevAssert But they are located in the mcal_text in default, user can't control it. Preconditions:

ID	Subtype	Headline and Description
		specify a ram section to these functions Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Hard fault Expected behavior: work normal Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-84095	New Feature	[CRYPTO_NG] Ordered access rights for Crypto Key Elements SWS_Crypto_00220 NewWorkDescription: New requirements were added for ordered access rights for Crypto Key Elements in Autosar R21-11. One of those requirements is SWS_Crypto_00220. Requirement source: Autosar R21-11 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Analyze the ordered access rights for Crypto Key Elements requirements by checking the file [^Ordered access rights for Crypto Key Elements.xlsx] After understanding the mechanism implement the ticket SWS_Crypto_00220 along with related ECUC_Crypto_00024 and ECUC_Crypto_00027(plus other identified requirements)
ARTD-84880	New Feature	[ADC] - S32K396 RTD ADC driver configurator will contain CFSDADC FW configurable parameters and default NXP use case configuration S32K396 RTD ADC driver configurator will contain CFSDADC FW configurable parameters and default NXP use case configuration. The configurator will contain enumerator, which will allow selection between 1 of three NXP provided use cases. Customer can also select his custom configuration. In case of custom configuration the customer is responsible for the correct and stable FW configuration. The list of configurable parameters and their range is included in the CFSDADC FW user manual. The standard parameters to be configured are highligted in green and the advanced are highligted in yellow. https://bitbucket.sw.nxp.com/projects/CFSDADC_FW/repos/cfsdadc_fw/browse/docs/S32K396/dox/um/CFSDADC_FW_UserManual.pdf The CFSDADC FW team will review and update the document ASAP to contain correct data and range values.
ARTD-85052	Bug	[MCU] Clock Reference Point not updated when the project is exported from Tresos to DS Detailed description (how to reproduce it): We installed the RTD(mentioned in environment section) in Tresos and configured it (no error). Export the app using Im and Exporters Create a new app in Design Studion (install the RTD mentioned in environment section). Import the file in DS (merge to existing) Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: After import all the Wdg modules have the same error : !image-2023-09-05-14-19-15-525.png! Expected behavior: No error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-85222	Bug	[Release]: The compiler parameters in the release note and the IM are not appropriate. Detailed description (how to reproduce it): The compiler parameters in the release note and the IM are not appropriate. In the documents, we didn't add the macro: MPU_ENABLE. If customer configure the parameters following the documents, the software will have problem. suggest add it. In fact, the previous version material have such items. Please verify all the parameter again. Preconditions:

ID	Subtype	Headline and Description
		None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: None Expected behavior: None Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-85381	New Feature	[IMPLEMENTATION] [S32K3xx] CanIf_ControllerBusoff stub implementation is missing from the CanIf stub Integrated SW32K3_RTD_4.4_R21-11_3.0.0_D2303 in Platform Bundle. Following error was detected at linking time: !image-2023-07-19-09-23-02-017.png! As a workaround, CanIf_ControllerBusOff function was added in a test case file. Expectation is that CanIf module should already have this function implemented.
ARTD-85428	Bug	[Mem_ExFls] Jenkins build failure running on Linux OS due to inconsistent casing in the driver Observed Jenkins build failure while using SW32SAF85xx_RTD_R21-11_2.0.0_CD01 with Mem_43_EX_FLS module. The reason is that filenames are case sensitive. (Logs attached file name mem_43_flslog.txt) Environment* *used:* Jenkins node running on Linux OS RTD plugin* *issue:* Module: Mem_43_EX_FLS Source code includes a header file as Mem_43_EXFLS_{*}IPW{*}.h but the file saved in inc folder in lower case as Mem_43_EXFLS_{*}Ipw.h,{*} Source file location c file that is giving call to header file with Upper* *case:* : C:\NXP \SW32SAF85xx_RTD_R21-11_2.0.0_CD01\eclipse\plugins\Mem_43_EXFLS_TS_T40D47M20I0R0\src !image-2023-08-17-11-57-59-998.png! Header file location with lower case header file : C:\NXP\SW32SAF85xx_RTD_R21-11_2.0.0_CD01\eclipse\plugins \Mem_43_EXFLS_TS_T40D47M20I0R0\include !image-2023-08-17-12-04-07-703.png!
ARTD-85967	Bug	[GPT] Incorrect access to Gpt_Ipw_HwChannelConfig if GptChannelId is not configured in order Detailed description (how to reproduce it): Incorrect access to Gpt_Ipw_HwChannelConfig if GptChannelId is not configured in order: !image-2023-09-13-14-18-40-245.png|thumbnail! Preconditions: GptChannelId is not configured in order Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Incorrect access to Gpt_Ipw_HwChannelConfig Expected behavior: Correct access to Gpt_Ipw_HwChannelConfig Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-85996	Bug	[S32K3] Port: Macro "PORT_CONFIG_EXT" generated in Precompile mode Detailed description (how to reproduce it): Create new project (DS and CT) Add port component, add pins, config variant = Precompile Generate and check Port_Cfg.h Preconditions:

ID	Subtype	Headline and Description
		Config variant = Precompile Test Case ID (internal TC that caught the defect) optional: Port_TS_014 Observed behavior: Macro "PORT_CONFIG_EXT" generated in Precompile mode !image-2023-09-13-17-28-33-901.png|width=803,height=800! !image-2023-09-13-17-30-40-623.png! Expected behavior: Macro "PORT_CONFIG_EXT" should not be used in PreCompile mode Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-86086	Bug	[GPT]: The API: Gpt_GetTimeElapsed will get a wrong value for the counting up type timer Detailed description (how to reproduce it): The API: Gpt_GetTimeElapsed will get a wrong value for the counting up type timer. In the low-level code: !image-2023-09-14-18-01-02-631.png|width=861,height=481! !image-2023-09-14-18-02-58-498.png! Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Got a wrong value Expected behavior: Get correct value Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add exclusive project
ARTD-86325	Bug	[gpt] Warnings related to unused function in GPT driver Detailed description (how to reproduce it): Build the RTD without defining RTC_0_CH_0_ISR_USED Preconditions: RTD is compiling Test Case ID (internal TC that caught the defect) optional: Bundle_TC_001 Observed behavior: Following warning is raised at compile time: !image-2023-09-18-16-51-44-332.png! Expected behavior: No warning present Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-86372	Bug	[MCU] remove clock mux12 and mux 17 for S32K3XX Detailed description (how to reproduce it): as new information in Rm S32K3xxRM_Rev8_DraftB, Remove clock mux 12 and mux 17 on S32K388 Remove mux 12 ih S32K358 Preconditions: NA

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: still remaining clock mux 12 and mux 17 in S32K3x8(EB,CT,Driver) Expected behavior: not have clock mux 12 and mux 17 in S32K3x8(EB,CT,Driver) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-86375	Bug	[MCU] rename uSDHC_CLK to USDHC_PER_CLK in S32K358 Detailed description (how to reproduce it): as new information in Rm S32K3xxRM_Rev8_DraftB, name of clock uSDHC_CLK must rename to uSDHC_PER_CLK Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: name of clock mux 13 of S32K358 is uSDHC_CLK Expected behavior: name of clock mux 13 of S32K358 is uSDHC_PER_CLK Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-86381	Bug	[MCU] Remove bypass mode for SXOSC S32K3XX Detailed description (how to reproduce it): as new information in Rm S32K3xxRM_Rev8_DraftB, the bypass mode in SXOSC is remove so Eb,CT need to remove bypass mode in SXOSC clock Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: bypass mode is still remaining in SXOSC clock Expected behavior: bypass mode is removed in SXOSC clock Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-86474	New Feature	[adc] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit:

ID	Subtype	Headline and Description
		Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86477	New Feature	[base] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86480	New Feature	[can] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies):

ID	Subtype	Headline and Description
		n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86486	New Feature	[crypto] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86489	New Feature	[dio] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.

ID	Subtype	Headline and Description
ARTD-86501	New Feature	[i2c] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86504	New Feature	[i2s] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86398	Bug	[S32ZE 1.0.0] CAN: Update Generate Code Template to generate CAN_CONFIG_EXT only in PB mode Detailed description (how to reproduce it): The collection of all configuration structure declarations now generates all of both PC and PB Modes. #define CAN_CONFIG_EXT

ID	Subtype	Headline and Description
		With PC mode it is not created, it is only created in PB Mode. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The macro still be genrated for PreCompile and Link Time Expected behavior: The macro is only generated for Post Build Proposed solution optional: [....]
ARTD-86457	Bug	[S32K3XX_S32M27x][PORT] Missing _IN suffix in ADC Interleave mode Detailed description (how to reproduce it): Can't config ADC interleave mode, it causes this error in build process. !MicrosoftTeams-image (15).png|thumbnail! Preconditions: [Select ADC interleave mode in EB Test Case ID (internal TC that caught the defect) optional: [Port_TS_004] Observed behavior: config ADC interleave mode Expected behavior: Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [add IN in Pin has the ADC interleave mode]
ARTD-86507	New Feature	[icu] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86519	New Feature	[ocu] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP".

ID	Subtype	Headline and Description
		In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86525	New Feature	[port] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86528	New Feature	[pwm] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh

ID	Subtype	Headline and Description
		all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86531	New Feature	[rm] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86534	New Feature	[sent] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit:

ID	Subtype	Headline and Description
		Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86537	New Feature	[spi] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86543	New Feature	[wdg] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a

ID	Subtype	Headline and Description
		HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86546	New Feature	[zipwire] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86555	New Feature	[dpga] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.

ID	Subtype	Headline and Description
ARTD-86564	New Feature	[memacc] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86567	New Feature	[mem_eep] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP". In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86579	New Feature	[resource] [IMPLEMENTATION] Request to rename MaxQFP silicon package to NXP HDQFP CR description: Request to re-name naming of "MaxQFP" silicon package in all NXP deliveries/collateral's/documentation/source code/other occurrences to "NXP HDQFP".

ID	Subtype	Headline and Description
		In case of any constraints due too long naming (2 words/to many letters) exception (e.g. using HDQFP) can be agreed with PL please add proposals in the analysis before PL approval. E.g. in configuration, "mqfp" shall be replaced by "hdqfp" {_}Proposed Solution{_}: replace all occurences of mqfp with hdqfp (mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641) Resource driver needs to replace occurences of mqfp with hdqfp (first update) (4mh) base driver clock and pin tool updates = 24 mh all drivers need to rename the resource files and replace in documentation mqfp with hdqfp (4mh x 25 drivers = 100 mh) all test configurations need to replace everywhere mqfp with hdqfp (8 mh x 25 drivers = 200 mh) extra documentation updates (release notes, etc.) = 16mh Reason for this change: Management request. Benefit: Avoid any legal issues. Onetime CR/Strategic CR: Onetime CR Use-case: n/a HW documentation reference (as applies): n/a HW/Application Engineer contact (as applies): n/a Note: relevant documents to be attached to the ticket.
ARTD-86699	Bug	[MCU]: The description for some configuration item is inappropriate. Detailed description (how to reproduce it): The description for below configuration items is inappropriate. Mcu->McuGeneralConfiguration->Mcu Disable Flash Wait States Config Mcu->McuGeneralConfiguration->Memory Configration Notification Please also remember update the corresponding doc. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Will misguide customers Expected behavior: Update the description Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-89479	Bug	[pwm] FlexPWM function Pwm_SetDutyCycle exception Detailed description (how to reproduce it): We need to call Pwm_SetDutyCycle to update output PWM dutycycle. But in low level function FlexPwm_Ip_LoadValue, it calls function FlexPwm_Ip_SetLoadModeHw that always set each submodule SMn_CTRL.LDMOD. Preconditions: Call function Pwm_SetDutyCycle. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: User can't choose whether submodule need to set SMn_CTRL.LDMOD. Expected behavior: User can choose whether submodule need to set SMn_CTRL.LDMOD. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-89511	Bug	[Mcu] AES_ACCEL clocking issue

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): There is a problem with the generated source code by the MCU driver on the S32K388 derivative that prevents the AES_ACCEL and related peripherals to have enabled clocks. Preconditions: Edit a MCU configuration in EBT. In McuModeSettingConf_0 for ex. locate and enable all clocks in McuPeripheral tab. Clocks of interest are AES_ACCEL, AES_APP0-7, EDMA0-31. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The selected enabled clocks don't get enabled by the MCU driver. Expected behavior: All selected clocks get enabled by the MCU driver. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check the resource file. The MCU.MC_ME.Partition2 may have COFB_2 missing. Check the generated source code (ex. Power_Ip related). It may generate incomplete source code.
ARTD-89522	Bug	[ADC] Incorrect check in ADC_SAR_IP_INST_HAS_CTU_TRIGGER_MODE Detailed description (how to reproduce it): Observed an DET while operating. DET was reported from below point: !screenshot-1.png|thumbnail! Here Driver is checking the 4th Bit: !screenshot-2.png|thumbnail! But as per assignment Driver is assigning only value Bit 0, bit1 and bit2 in the case ADC_INSTANCE_COUNT >=3: !screenshot-3.png|thumbnail! Preconditions: enabling Adc Tempsense Api in multi Variant Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Observed an DET while operating Expected behavior: no DET while operating Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-89568	Bug	[MCU][S32M27x] Functional reset entry timer implementation is missing. Detailed description (how to reproduce it): RM mentions: !image-2023-09-27-11-10-58-972.png|width=680,height=169! Driver code implements: !image-2023-09-27-11-11-30-539.png! The feature is not being implemented on the interface and in the driver code. The feature is important as in some scenario as RM mentions that the functional reset can be escalated to DES reset if timeout occurred => In the case, users don't want DES reset happens as such scenario, Functional reset entry timer must be implemented. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Functional reset entry timer implementation is missing. Expected behavior: Functional reset entry timer implementation is implemented. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-89601	Bug	[MCU][S32K3] The implementation of reading the status of FES register is wrong Detailed description (how to reproduce it): In the function {*}Power_Ip_MC_RGM_GetResetReason{*}, the status of FES register will be ignored if ActiveValue = 0 !image-2023-09-27-14-24-05-770.png! ActiveValue contains the status of DES register !image-2023-09-27-14-25-53-356.png! RM mentions: !image-2023-09-27-14-26-03-793.png! => Therefore if ONLY DES[F_POR] is set{*}, the status of FES register must not be ignored{*} Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The implementation of reading the status of FES register is wrong Expected behavior: The implementation of reading the status of FES register is corrected Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-89606	Bug	[MCU][S32K3] The condition checking before writing to MODE_CONF is missing Detailed description (how to reproduce it): RM mentions: !image-2023-09-27-14-33-24-333.png! Drive code implements: !image-2023-09-27-14-33-32-473.png! It lacks of checking if the values of multiple fields being FUNC_RST and DEST_RST simultaneously equal 1 in the MODE_CONF register Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The condition checking before writing to MODE_CONF is missing Expected behavior: The condition checking before writing to MODE_CONF is supplemented Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-89618	Bug	[MCU] add support PLLDIG.PLLCLKMUX[REFCLKSEL] for S32K3XX Detailed description (how to reproduce it): as new information in Rm S32K3xxRM_Rev8_DraftB, we have PLLDIG.PLLCLKMUX[REFCLKSEL] in the clock diagram but this isn't supported in our driver Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: PLLDIG.PLLCLKMUX[REFCLKSEL] is not available in Mcu driver,ET,CB Expected behavior: PLLDIG.PLLCLKMUX[REFCLKSEL] is available in Mcu driver,ET,CB Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-89624	Bug	[MCU] investigate the new note in new RM related QSPI clock range Detailed description (how to reproduce it): as new information in Rm S32K3xxRM_Rev8_DraftB, have a new note : As MC_CGM_MUX14 have max input frequecny limited to 240 MHz, so while sourcing uSDHC_PER_CLK from PLL_PHI1_CLK, QSPI can run only on 60 Mhz max frequency Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: need to investigate and add constraint if need
ARTD-89853	Bug	[I2C] Missing CDD_I2c_CfgDefines.h file for S32DS Detailed description (how to reproduce it): In previous release, Developer create CDD_I2c_CfgDefines.h file for EBT and miss for S32DS Preconditions: Run project with S32DS Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: EBT with S32DS is inconsistent Expected behavior: EBT with S32DS is consistent Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add CDD_I2c_CfgDefines.h file for S32DS
ARTD-90218	Bug	[MCU] GHS-Build Failure Detailed description (how to reproduce it): GHS-Build Failure !image-2023-10-03-13-52-26-378.png! The struct only has 2 elements but it is generated with 3 elements !image-2023-10-03-13-54-20-123.png! !image-2023-10-03-13-54-29-683.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: GHS-Build Failure Expected behavior: No failure at build phase Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-90222	New Feature	[Implement] - RTD for S32M27x (AE10 Driver) RTD Driver shall implement callbacks for faults from HEALTH STATUS register. g. clock miss, frame counter, wrong answer RTD should re-implement the AE driver to access SPI outside the interrupt and AE read()/write() should be re-entrant. RTD Driver shall use HEALTH STATUS register to distinguish which register (FATLTS/EVENTS) to read to void clearing of error flag triggered by the fault injection.

ID	Subtype	Headline and Description
		RTD driver shall be configurable to skip error flag clearing (to let eMcem driver to handle it if it is present).
ARTD-90553	New Feature	[adc] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90556	New Feature	[base] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.

ID	Subtype	Headline and Description
ARTD-90559	New Feature	[can] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90537	Bug	[PORT] [S32K396] Need to clear bit FGEN before initialize configuration for IGF feature Detailed description (how to reproduce it): bit FGEN is not cleared before configurating for MCR register !image-2023-10-09-18-09-18-674.png! According to RM, need to clear bit FGEN before updating configuration to some bit fields of MCR register. !image-2023-10-04-15-13-13-435.png! Preconditions: Configure IFG feature Test Case ID (internal TC that caught the defect) optional: TS: Port_TS_004 config 2 Observed behavior: bit FGEN is not cleared before configurating IGF feature. Expected behavior: bit FGEN is cleared before configurating IGF feature. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Clear bit FGEN before update config for IGF Register
ARTD-90568	New Feature	[dio] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176

ID	Subtype	Headline and Description
		Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90580	New Feature	[i2c] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90586	New Feature	[icu] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change:

ID	Subtype	Headline and Description
		According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90598	New Feature	[ocu] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90601	New Feature	[platform] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit:

ID	Subtype	Headline and Description
		To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90604	New Feature	[port] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. [06-Oct-2023][Nhat] Check comment: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/port/pull-requests/810/overview?commentId=2145418] The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90622	New Feature	[wdg] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023

ID	Subtype	Headline and Description
		Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90637	New Feature	[mem_eep] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90656	New Feature	[dpga] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit:

ID	Subtype	Headline and Description
		To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90662	New Feature	[ae] [IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90781	Bug	[SW32SAF85xx_RTD_R21-11_2.0.0_CD01_P02][ETH][GMAC] Configuration cannot be generated with UCT due to missing parameters in component Detailed description (how to reproduce it): Build / use of Gmac example application fails. Build / use of Eth example Application fails. Preconditions: SW32SAF85xx_RTD_R21-11_2.0.0_CD01_P02 Package installed Test Case ID (internal TC that caught the defect) optional: Unknown Observed behavior: !image-2023-10-04-17-30-15-768.png! !image-2023-10-04-17-33-25-125.png! Expected behavior: !image-2023-10-04-17-30-55-624.png! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: [..]
ARTD-90787	New Feature	[mem_exfls] Implement ValidateConfigCRC to checks the CRC over configuration NewWorkDescription: Implement ValidateConfigCRC to checks the CRC over configuration Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-90899	New Feature	[ocu] [ITG][IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf , replace mqfp with hdqfp CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 And replace all occurences of mqfp with hdqfp* *(mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641)* Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR: Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90911	New Feature	[spi] [ITG][IMPLEMENTATION] [RTD] Add support S32K376, S32K374, S32K396_176lqpf , replace mqfp with hdqfp CR description: Add support S32K376, S32K374 and S32K396_176lqpf in S32K3_S32M27x 4.0.0 release in Nov 2023. The following resources need to be added: s32k396_lqfp176 s32k394_lqfp176 s32k376_mapbga289 s32k374_mapbga289 s32k376_lqfp176 s32k374_lqfp176 And replace all occurences of mqfp with hdqfp* *(mentioned in Analysis field of CR: https://jira.sw.nxp.com/browse/AAI-1641)* Reason for this change: According to S32K39 and S32K37 Reference Manual, Rev.2, 08/2023 Benefit: To support S32K376, S32K374 Onetime CR/Strategic CR:

ID	Subtype	Headline and Description
		Onetime Use-case: NA HW documentation reference (as applies): S32K39RM_and_S32K37RM_Rev2.pdf([link|https://nxp1.sharepoint.com/teams/25_43/s32k396/Shared%20Documents/Forms/folders.aspx?id=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2%2FS32K39RM_and_S32K37RM_Rev2.pdf&parent=%2Fteams%2F25_43%2Fs32k396%2FShared%20Documents%2FDocumentation%2FRM%2FRM_Rev2]) HW/Application Engineer contact (as applies): NA Note: relevant documents to be attached to the ticket.
ARTD-90976	Bug	[ICU] Error when create or import file .mex in S32CT Detailed description (how to reproduce it): Error when create or import file .mex in S32CT in S32K396, it should be fix in all derivative [CODEGEN] Failed to generate file "Emios_Icu_Ip_Defines.h" Issue: Description: Feature FEATURE_ICU_EMIOS_USEMCLAPI not defined for the Issue: ExpressionContext[child_context = ChildContext[!image-2023-10-05-14-03-16-709.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Icu_TS_010 Observed behavior: Log many error Expected behavior: Not exit error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-90986	Bug	[Base] Update Errata defines for Spi Detailed description (how to reproduce it): Review new Erratas for S32K3XX Spi: K3x4 has 2 erratas ERR050456 ERR_IPV_LPSPIV2_0001 and ERR051588 ERR_IPV_LPSPIV2_0002. Other K3XX derivatives only have 1 errata ERR051588 that will be cover by ERR_IPV_LPSPIV2_0002 implemetation. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update Errata defines for Spi: For K3x4: Define 2 erratas ERR050456 ERR_IPV_LPSPIV2_0001 and ERR051588 ERR_IPV_LPSPIV2_0002. For other K3 derivatives: Remove ERR_IPV_LPSPIV2_0001; define ERR051588 ERR_IPV_LPSPIV2_0002.
ARTD-91065	Bug	[S32K3XX_S32M27x_4.0.0][Mem_Eep] Add device S32k328 S32K338 S32K348 in file sdk_manifest_mem_eep.xml Detailed description (how to reproduce it): Update device S32K338 S32K328 S32K348 in file : sdk_manifest_mem_eep.xml Preconditions: !image-2023-10-05-16-33-32-224.png! Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Observed behavior: Please help me add device S32K328 S32K338 S32K348 Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-91131	Bug	[S32K3xx_S32M27x_4.0.0] [DIO]: Build fail when enable Virtual Wrapper Detailed description (how to reproduce it): 1. When DIO_VIRTWRAPPER_SUPPORT is enabled, some DIO functions will not be available (in file UM of DIO) !image-2023-10-05-17-01-14-613.png|width=604,height=156! Some functions in the IP layer have conditions for VIRT WRAPPER notes, however in the IPW layer these functions are used but do not have conditions for VIRT WRAPPER notes, leading to build faild !image-2023-10-05-17-30-09-968.png|width=986,height=193! 2. Dio_MaskedWritePort not support Virtual Wrapper, need to notify user of configuration error when configuring DioMaskedWritePortApi and DioVirtWrapperSupport simultaneously Preconditions: There must be conditions for these functions when using VIRT WRAPPER Test Case ID (internal TC that caught the defect) optional: Dio_TS_020 Observed behavior: Error: implicit declaration of function Dio_MaskedWritePort not support Virtual Wrapper, need to notify user of configuration error when configuring DioMaskedWritePortApi and DioVirtWrapperSupport simultaneously Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Recheck and update the conditions for the function when using VIRT WRAPPER
ARTD-92322	Bug	[GPT] S32DS issue raised after import configuration from EB tresos Detailed description (how to reproduce it): In S32DS after importing configuration from EB tresos the GPT module has error: Issue: If turn on GptChangeNextTimeoutValueApi! Please enabled isr for use. In EB tresos this error in not present. Preconditions: Create EB tresos project configuration, export using arxml, then import it in the S32DS. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: The S32DS has error after importing EB tresos configuration. Expected behavior: No error in the imported configuration. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-92326	Bug	[MCU] S32DS import from arxml file does not change the settings in Clock Tool Detailed description (how to reproduce it): Export from EB tresos MCU configuration with different default settings in arxml file. Import the configuration in S32DS. Check the values in Clock Tool. Preconditions: none Test Case ID (internal TC that caught the defect) optional: Observed behavior: MCU error in the S32CT:

ID	Subtype	Headline and Description
		This value has been changed in Clock Tool. FXOSC frequency is not enabled in Clock Tool This value has been changed in Clock Tool. Trigger Devider 0 Selection nopt imported in Clock Tool This value has been changed in Clock Tool. CGM0 Clock Mux 1 Devider0 Enable. Expected behavior: No errors after importing the arxml in S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Propagate MCU configuration data to Clock Tool after import.
ARTD-92349	Bug	[GPT][S32DS] Cannot enable GptPredefTimerFunctionalityApi Detailed description (how to reproduce it): Predef timer has not define in "GptChannelConfiguration" so the condition check "GptHwIp" is not correct. GPT_PREDEFTIMER_FUNCTIONALITY_API alway defined is OFF !image-2023-10-06-17-01-18-252.png! Build fail log: !image-2023-10-06-17-09-00-898.png! Preconditions: Configuration using s32ct generator Enable GptPredefTimerFunctionalityApi and do not config STM in "GptChannelConfiguration" [^s32k388_M7_0_0.mex] Test Case ID (internal TC that caught the defect) optional: Gpt_TS_305 Observed behavior: build fail Expected behavior: build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-92352	Bug	[PORT][SS32K3XX] Missing IN OUT suffix in eTPU mode (S32K396), uSHDC mode(S32K358) at pintools, and compilation failed with IGF feature on S32CT Detailed description (how to reproduce it): There are 2 issues with S32K396 on S32CT and 1 issue with S32K358 on S32CT issue 1: missing IN OUT suffix with mode eTPU on pin tool > generate fail S32K396 !image-2023-10-06-17-25-02-325.png! issue 2: Generate inconsistently macro Igf_Port_Ip_VS_0_PB in 2 file Igf_Port_Ip_VS_0_PB.h* and Igf_Port_Ip_VS_0_PBcfg.h > build failed S32K396 !image-2023-10-06-17-27-03-193.png! !image-2023-10-06-17-27-24-268.png! issue 3: missing IN OUT suffix with mode uSHDC on pin tool > generate fail K32K358 !image-2023-10-19-10-49-02-710.png! Preconditions: Config eTPU mode on pintool S32K396 Config uSHDC mode on pintool S32K358 Config IGF mode Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generate failed with eTPU mode Generate failed with uSHDC mode Compilation failed with IGF mode Expected behavior: Generate successfully with eTPU mode Generate successfully with uSHDC mode Compile successfully with IGF mode Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-92361	New Feature	[CRYPTO_NG] Ordered access rights for Crypto Key Elements SWS_Crypto_00222 and SWS_Crypto_00223

ID	Subtype	Headline and Description
		NewWorkDescription: New requirements were added for ordered access rights for Crypto Key Elements in Autosar R21-11. Two of those requirements are SWS_Crypto_00222 and SWS_Crypto_00223 . Requirement source: Autosar R21-11 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-92364	New Feature	[CRYPTO_NG] Ordered access rights for Crypto Key Elements SWS_Crypto_00221 NewWorkDescription: New requirements were added for ordered access rights for Crypto Key Elements in Autosar R21-11. One of those requirements is SWS_Crypto_00221: Jobs shall use the assigned key elements without guarding the key access rights with the following exceptions: If a key element is used for input using the input re-direction, the key element must have access rights CRYPTO_RA_INTERNAL_COPY or lower. If input re-direction is used for CryptoPrimitiveService ENCRYPT/DECRYPT or AEAD_ENCRYPT/AEAD_DECRYPT, the access rights must be set to RA_ENCRYPTED or lower.1) If a key element is used for output re-direction, the key element must have access rights CRYPTO_WA_INTERNAL_COPY or lower. Any key element that is used to generate keys using Key Exchange operation shall have access rights of at least CRYPTO_RA_INTERNAL_COPY or lower. For Key Derivation, the source key shall have access rights of at least CRYPTO_RA_INTERNAL_COPY or lower. The destination key shall have at least the access right of its source key or lower2). Requirement source: Autosar R21-11 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:
ARTD-92372	Bug	[S32K3XX_S32M27x_4.0.0][Mem_Eep] Fix import not match EB tresos with S32CT (S32DS) Detailed description (how to reproduce it): Import not match Tresos with S32DS Preconditions: !image-2023-10-08-16-11-19-438.png! Test Case ID (internal TC that caught the defect) optional: Mem_TC_FCT_0002 Mem_TC_FCT_0010 Observed behavior: In Tresos : mem start address (sector_bach_1) : 4096. Mem Erease Sector Size : random is 2037 byte. > Configure Build gen > report oki But as import S32DS: Mem_address is 4096 is fail > Because node Mem_Erease_sector_size need align with 512. So let be is true: Mem_Erase_Sector_size : 4096 Mem_Address: 4096 Expected behavior Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Suggest: Need add Warning as user config node Mem_Erase_Sector_Size align 512.
ARTD-92740	Bug	[S32K3XX S32M27X 4.0.0] [Mem_InFls]: Build fail with IAR compiler when disable Utest mode api Detailed description (how to reproduce it): Build fail with IAR compiler when disable Utest mode api !screenshot-1.png|thumbnail!

ID	Subtype	Headline and Description
		Preconditions: Utest mode api is disable Test Case ID (internal TC that caught the defect) optional: Observed behavior: build fail with IAR Expected behavior: Build success without error in iar compile Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Must be add #if (STD_ON == C40_IP_UTEST_MODE_API)}} for all API of Utest Mode.
ARTD-92759	Bug	[I2c] Using wrong logical operator in if statement in S32DS code template Detailed description (how to reproduce it): See attachment Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: using wrong & operator in if condition Expected behavior: Shoule be && Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change & to &&
ARTD-93124	Bug	[S32K3XX] [MEM_EXFLS] Read device ID function always returns E_OK Detailed description (how to reproduce it): Mem_43_EXFLS_IPW_DeviceIdMatches always returns E_OK even if the read id is not as expected Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_001 Observed behavior: Init function returns successful Expected behavior: function works properly Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-94231	Bug	Issue with header files when compile project in Linux Detailed description (how to reproduce it): none Preconditions: none Test Case ID (internal TC that caught the defect) optional: none Observed behavior: When compile project in linux, header files mismatching issues are reported /var/jenkins_home/workspace/S_BMS_GEN3_build_patchset_master/src/config/rtd/output/include/Flexio_Uart_Ip_Cfg.h(46) : Fatal Error[Pe1696]: cannot open source file "Flexio_Uart_Ip_S32k3X8EVB_Q289_REVB_PBCfg.h" because the filename of the generate file is : Flexio_Uart_Ip_S32k3X8EVB_Q289_REVB_PBcfg.h Linux case sensitive reported different name of header include files between "...Cfg.h" and "...cfg.h" !image-2023-10-10-11-11-24-388.png|width=703,height=336! Expected behavior: Compile project without errors

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Include correct header files with "...cfg.h" as generated files
ARTD-93677	Bug	[PORT][S32K388] Can not set ONLY_OUTPUT mode by calling Port_SetPinMode function Detailed description (how to reproduce it): Configure one pin which is available ONLY_OUTPUT mode (PTA24 S32K388), at GPIO mode INPUT at first After that, Call Port_SetPinMode* function to switch to *ONLY_OUTPUT mode, can not change to ONLY_OUTPUT mode !image-2023-10-10-10-08-53-247.png! Preconditions: K388 Test Case ID (internal TC that caught the defect) optional: Port_TS_016 Observed behavior: Cannot switch to ONLY_OUTPUT mode by calling Port_setPinMode Expected behavior: Can set ONLY_OUTPUT mode by calling Port_setPinMode Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-94102	Bug	[ICU]Not exits error when tick config other mode in EDGE_COUNT mode Detailed description (how to reproduce it): When choose mode edge counter, tick in other config for other mode but not exits warning or error(just in EB) !image-2023-10-10-11-03-23-632.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Icu_TS_030 Observed behavior: Not have error Log Expected behavior: Have error log when cofig Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-95593	New Feature	[AE] Implement callbacks for faults from GHS register. NewWorkDescription: RTD Driver shall implement callbacks for faults from GHS register. clock miss, frame counter, wrong answer, FSM_status RTD shall implement frame counter checker internally (cannot be done by SAF since we do not handle all SPI transfers RTD shall upon detected GHS Fault call Handlers defined in Tresos (like for regular AE Fault) RTD shall implement new tab in tresos config for GHS faults (only setting needed there is definition for handlers) Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-95602	New Feature	[AE] Implement the AE driver to access SPI outside the interrupt and AE read()/write() should be re-entrant. NewWorkDescription: RTD should re-implement the AE driver to access SPI outside the interrupt and AE read()/write() should be re-entrant. Alternative way would be to process AE fault/event register in low priority interrupt, but for this RTD need to come up with solution for re-entrant function Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-95608	New Feature	[AE] Re-implement the function AEC_IRQEventFaultHandler

ID	Subtype	Headline and Description
		NewWorkDescription: RTD Driver shall use GHS register to distinguish which register (FATLTS/EVENTS) to read to void clearing of error flag triggered by the fault injection. We will double check if we are injecting only faults, if yes, then RTD just need to read {color:#FF0000}fault register first{color} -> (void)Aec_Ip_SpiRead(AEC_FAULT_STATUS_ADDR, AEC_DATAWIDTH_16, &RegStatusFault)* is called before *(void)Aec_Ip_SpiRead(AEC_EVENT_STATUS_ADDR, AEC_DATAWIDTH_16, &RegStatusEventVal) RTD driver should not read the enable bits Read of Fault/Event Status should be done only once, *{color:#FF0000}not within IsrPrio loop!!!! If Prio is same for some event and fault, event is handled first due to faults being at higher index. This needs to be changed, to handle first faults, then events. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-95617	New Feature	[PORT] Add support for multiple configurations in S32CT for S32K3XX_S32M27X and S32K388 new framework and S32K388 ADC Interleave NewWorkDescription: Previously, we limited the number of functional groups (multiple configurations) to 1. Now we want to add support for multiple configurations (in the form of post-build variants and classic functional groups) so that we can also replicate in S32CT the module configurations from EB Tresos in which there are two or more post-build variants. Requirement source: SRS_BSW_00405 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Read the newly introduced section ("13. Multiple Configurations") in the following presentation: [NXP_RTD_AUTOSAR_S32CT_V2|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=r7YbFB] Make sure you have added the SYNC_VALUE and SYNC_SIZE options to each component setting that requires it (as suggested in the presentation, you can use [epdimp2ct|https://nxp1.sharepoint.com/:f:/s/Zebra/EprWIdG7fTNPgdoXtWTgmIsBn1Xo56J_qJQGC37m92ax9A?e=ivi58c] to automate this task as long as you have a matching EPD for your component) Apply the changes shown in the source code references. The main points are: {noformat} [!IF "var:defined('postBuildVariant')"!]{noformat} translates to {noformat} if (useFgInfix()){noformat} The file names and configuration structures should not contain the variant infix when there's no selected post-build variant (actually, most of the changes you'll see in the references are done just to support this use-case) Sanity Check: Check that your driver can be successfully built in all three scenarios: ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO = 0 ## ComponentGenerationMethod = EcucPostBuildVariants and VARIANT_NO > 1 (VARIANT_NO == 1 is the base case from which you started) ## ComponentGenerationMethod = FunctionalGroups (with at least 2 FGs configured in the project) Extensive Testing: By default, EB Tresos cannot generate variant aware EPC files without throwing a null pointer exception. To get around this limitation, the _dreisoft.tresos.autosar2_ plugin must be patched. To do this, download one of the two attached archives, depending on your EBT version, and extract it in <ebt_root_dir>/plugins. # Go to your driver's plugin, open {_}plugin.xml{_}, search for {_}id="EPCGenerator"{_}, and set the value of parameter _"allVariants"_ to {_}"true"{_}. This will enable variant aware EPC file generation for your module. # Create a configuration with at least two post-build variants. The project will need EcuC for post-build variants to be enabled. The configuration should ideally use different values for nodes with postBuildVariantValue=TRUE and different list elements for nodes with postBuildVariantMultiplicity=TRUE. This will ensure that errors in variant handling can be easily caught later on while doing the diffs. # Generate the EPC files by right clicking on your project's configuration and select "Generate Project". If the 1st step has been carried out correctly, there will be a _"PostBuildSelectableVariants.arxml"_ file in _<project_root_dir>/output/output_ and your module's EPC file, lying inside the same directory, will contain lots of _"VARIATION-POINT"_ elements. # Open S32DS and select File > Import > S32 Configuration Tools > Import ECU Configuration. Browse to the location where your EPC files are located within the EBT project and select at least your module's EPC file, EcuC's EPC file and PostBuildSelectableVariants.arxml. Check the _"Import the configuration as a new one"_ radio button and select the processor / package / sdk version accordingly. # Go to the _"Global settings"_ panel and make sure that _ComponentGenerationMethod=EcucPostBuildVariants_ in the System component. # Select _"Update Code"_ to generate your S32DS project files. Perform a comparison/diff of the generated files between S32DS and EBT. *These files should be pretty much identical (sans whitespace or formatting) # Go to the _"Global settings"_ panel again to generate the ECVD files (EcvdGenerationMethod=INDIVIDUAL, browse a location for EcvdOutputPath and click on the _Generate Configuration_ button). Compare/diff your module's EPC file with your module's ECVD file. *These files should be pretty much identical (sans whitespace or formatting)

ID	Subtype	Headline and Description
		# The above steps tested the EBT->S32DS compatibility. To also test the S32DS->EBT compatibility, do the above steps in reverse. That is, start from an S32DS project with post-build variants, generate the ECVD files, import them into EBT, compare again the generated files and the configuration files.
ARTD-95626	Bug	[CRYPTO_NG][S32K3XX_M27X] HseKeyInfoDummy variable in function Crypto_43_HSE_Ipw_CheckKey is stored in wrong memory partition Detailed description (how to reproduce it): Variable HseKeyInfoDummy is lie in int_stack_dtcm area and HSE is unable to process int_stack_dtcm area directly. Hse response to the address parameters are invalid !image-2023-10-10-15-29-53-731.png! Preconditions: tag: CRYPTO_NG_026 Test Case ID (internal TC that caught the defect) optional: Crypto_TC_FCT_0046.c Observed behavior: Derivative: S32K396 load to ram !image-2023-10-10-15-18-26-041.png! !image-2023-10-10-15-20-26-554.png! Expected behavior: HseKeyInfoDummy needs to be stored in the partition which allows HSE to read data from Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-95636	New Feature	[WDG] Rename AeWdog_Ip_Config function to AeWdog_Ip_ConfigWindow Rename the function AeWdog_Ip_Config to AeWdog_Ip_ConfigWindow to be more appropriate
ARTD-95771	Bug	[MCU]: Some MCME register bits are recovered unexpected and don't have configure item for it Detailed description (how to reproduce it): Some MCME register bits are recovered unexpected and don't have configure item for it. For example, the PRTN1_COFB3_CLKEN, now, we can only configure the REQ96 and REQ104, the other bits can't be configured. and the default value for REQ102 is 1 will be recovered to 0. this will cause issue in XRDC. suggest add some configure items for these bits. or don't change the default value. Preconditions: None Test Case ID (internal TC that caught the defect) optional: None Observed behavior: Register bit was recovered to unexpected value Expected behavior: add independent configure item for these bits Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: None
ARTD-95822	Bug	[ADC] Missing ADC channels for S32M27x parts Detailed description: I am using S32DS3.5 with SW32K3_RTD_R21-11_3.0.0_P07_D2306_DS_updatesite. Inside any S32CT or EB Tresos project for S32M27x, in the ADC container at channel configuration, the list of channels that can be selected is smaller than the list present in the reference manual specifications of S32M27x. For instance, the "S" channels from the specifications are S8-23, but inside the project only S14 can be selected for ADC0 instance. !image-2023-10-11-15-24-33-257.png|width=540,height=295! The picture from Design Studio was taken from a S32M276 project.
ARTD-95839	New Feature	[memacc] [IMPLEMENTATION] Multicore Type 1 for MEMACC Driver NewWorkDescription: Implement the multicore "Type 1" for the MEMACC Driver Requirement source:

ID	Subtype	Headline and Description
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Reference the way to implement the multicore "Type 1" on the FLS Driver (AUTOSAR 4.4) Document: NXP_RealTimeDrivers_Multicore.pptx; Autosar Memstack Multicore.pptx
ARTD-95842	New Feature	[memacc] [IMPLEMENTATION] Multicore Type 3 for MEMACC Driver NewWorkDescription: Implement the multicore "Type 3" for the MEMACC Driver Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Reference the way to implement the multicore "Type 3" on the FLS Driver (AUTOSAR 4.4) Document: NXP_RealTimeDrivers_Multicore.pptx; Autosar Memstack Multicore.pptx
ARTD-96046	Bug	[ICU]The value written to the LPCMP_CCR0_LINKEN bit is incorrect Detailed description (how to reproduce it): The LINKEN bit is in the CCR0 register, but in the source code it is mistakenly written to the DCR register so the value will not be written correctly. !image-2023-10-12-10-59-07-182.png|thumbnail! At the same time with the new document RM S32K396RM Rev. 2, 08/2023, the LINKEN bit will be removed, so this bit needs to be removed on s32k396 derivative. Element order in struct Cmp_Ip_TriggerConfigType is incorrect when there are redundant PreSetChannel elements !screenshot-1.png|thumbnail! The value of node IcuTrgInitDelayValue is in the range [0 ,63] because the RR_INITMOD register is 6 bits wide !screenshot-2.png|thumbnail! The value of node IcuCmpFilterSampleCount is in the range [0 ,7] because the RR_INITMOD register is 3 bits wide ! screenshot-3.png|thumbnail! Mode CMP_IP_FUNCTIONALMODE_DISABLED need to write value to CMP_EN equal to 0 In Round-robin trigger mode, IER[CFR_IE] and IER[CFF_IE] bits need to be disable. !screenshot-4.png|thumbnail! Preconditions: uses interface with ipvalt LPCMP Test Case ID (internal TC that caught the defect) optional: Icu_TC_FCT_0233(Icu_TS_118) Observed behavior: The LINKEN bit value is being written incorrectly and this bit needs to be removed on s32k396 derivative The PreSetChannel element is redundant, causing the element order in the Cmp_Ip_TriggerConfigType structure Expected behavior: The LINKEN bit value needs to be written correctly and this bit needs to be removed on s32k396 derivative remove the PreSetChannel element in the Cmp_Ip_TriggerConfigType structure for ipvalt LPCMP Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The LINKEN bit value needs to be written to the CCR0 register and this bit needs to be removed on s32k396 derivative remove the PreSetChannel element in the Cmp_Ip_TriggerConfigType structure for ipvalt LPCMP In the function Cmp_Ip_InitCcr0, remove the statement ccr0 = LPCMP_CCR0_CMP_EN(1u) after writing the registers in the modes and writing LPCMP_CCR0_CMP_EN(0u) in mode CMP_IP_FUNCTIONALMODE_DISABLED in the function Cmp_Ip_EnableInterrupt, in the Round-robin trigger mode you need to disable IER[CFR_IE] and IER[CFF_IE]
ARTD-96129	New Feature	[ICU] Support Virtual Wrapper for S32K3 platform Detailed description (how to reproduce it): Please refer S32K3 RM Rev. 8 DraftB, 09/2023 We found a problem, seems like first analysis for VIRTUAL WRAPPER module is missing part for interrurt on SIUL2 module which currently handle by ICU module. The VIRTUAL_WRAPPER is feature to support SIUL2 register allocation per DomainID (implemented by RM) When enable, VIRT_WRAPPER will change location of base address of SIUL2 registers so ICU need to refer to configuration on RM to select correct base address. You can refer to PORT/DIO to learn how to implement this feature. !image-2023-10-12-16-52-02-918.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior:

ID	Subtype	Headline and Description
		N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: See description for initial information
ARTD-96079	Bug	[ICU]Fix build failed error when using DMA for timestamp mode Detailed description (how to reproduce it): When enabling dma when using the emios_icu iplayer layer, the build error below appears: !image-2023-10-12-16-00-15-484.png|thumbnail! Preconditions: enable dma for ip layer emios_icu Test Case ID (internal TC that caught the defect) optional: Ip_Emios_TC_FCT_3001(Ip_Emios_TS_181) Observed behavior: build failed when dma is enabled Expected behavior: build successfully when dma is enabled Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: replace statement if (IcuChannels.getChildById("IcuChannelRef").getValue().contains("eMiosChannel")) to if (IcuChannels.getChildById("IcuChannelRef").getValue().contains("IcueMios"))
ARTD-96137	Bug	[S32K3xx_S32M27x_4.0.0] DIO: Build fail test CCOV Detailed description (how to reproduce it): Undefine DIO_ENABLE_USER_MODE_SUPPORT in file Siul2_Dio_Ip.c when build test CCOV Preconditions: Derivative S32K396 Test Case ID (internal TC that caught the defect) optional: Dio_TS_101 Observed behavior: Undefine DIO_ENABLE_USER_MODE_SUPPORT in file Siul2_Dio_Ip.c when build test CCOV !image-2023-10-12-17-33-25-643.png|thumbnail! I see it was added in the S32ZSE release. Need remove on PLATFORM S32K3XX https://jira.sw.nxp.com/browse/ARTD-84495 !image-2023-10-12-17-25-31-972.png|thumbnail! Expected behavior: Test CCOV build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-96458	Bug	[ADC] ADC's plugin is generating error for S32K3 M27x platform Detailed description (how to reproduce it): ADC's plugin is generating error !image-2023-10-13-13-38-58-414.png! Preconditions: Driver tag : ADC_477 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: See description above Expected behavior: ADC's plugin generate successful Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-96381	New Feature	[DPGA] Implement S32DS code generate for feature self-test NewWorkDescription: Create code generate for feature self-test in s32DS Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-96695	Bug	[GPT][S32DS] Cannot generate define timeout for Pit_RTI in S32M27X Detailed description (how to reproduce it): In Gpt.component, it lack of "S32M27" (see the picture below) !image-2023-10-13-15-15-12-345.png! This mistake lead to it can't define "PIT_IP_TIMEOUT_COUNTER" and "PIT_IP_TIMEOUT_TYPE" when generate for S32M276(see the picture below) !image-2023-10-13-15-19-13-284.png! Build log (see the picture below): !image-2023-10-13-15-23-06-304.png! Preconditions: Configuration using s32ct generator Configuration use Pit_0 RTI [^M276.mex] Test Case ID (internal TC that caught the defect) optional: Ip_Pit_TS_001 Observed behavior: Build fail Expected behavior: Build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-96741	Bug	[PORT] [S32K3XX_S32M27X] Error with Bswmd validation Detailed description (how to reproduce it): 2 step to validate Bswmd: Compile plugin with option: GENERATE_BSWMD_FILE=ON *Port_Bswmd.arxml is empty !image-2023-10-16-08-29-29-331.png! Bswmd validation: make generate VALIDATE_BSWMD=ON > *errors appear in build log !image-2023-10-16-08-30-28-590.png! Preconditions: Follow 2 steps to validate bswmd Test Case ID (internal TC that caught the defect) optional: Port_TS_BSWMD Observed behavior: Error when validating bswmd, Port_Bswmd.arxml is empty Expected behavior: No error appears. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-96744	Bug	[PORT][S32K3XX_S32M27X] Inconsistently generated file between EBT and S32CT with TSPC feature Detailed description (how to reproduce it): Inconsistently generated file between EBT and S32CT with TSPC feature E.g: when configure PTA17 with mode TSPC support on EBT and S32CT K388 EBT !image-2023-10-16-10-14-45-492.png! S32CT (On pin tool) !image-2023-10-16-10-15-13-240.png!

ID	Subtype	Headline and Description
		Preconditions: Enable TSPC support Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Inconsistently generated file between EBT and S32CT with TSPC feature Expected behavior: Generate files on EBT is consistent with the files on S32CT Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-96750	Bug	[S32K3xx_S32M27x_4.0.0][S32K396] Code generation fails when configuring pin in emios, cmp, hse mode Detailed description (how to reproduce it): Create new project on EB tresos, resource = K396 Add Port module, config 1 pin as emios (cmp, hse) mode and generate code e.g. mscr 50, EMIOS_0_EMIOS_0_CH_15_X_OUT mscr 119, HSE_HSE_TAMPER_LOOP_OUT0_OUT mscr 159, CMP1_CMP1_RRT_OUT ... !image-2023-10-16-10-08-26-323.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: failed to generate file !image-2023-10-16-10-04-15-970.png! Expected behavior: Generate successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-96768	New Feature	[ADC] Added support for new bit field AMSIO[CMPCTRL0] NewWorkDescription: The header file of ADC updated the bit field CMPCTRL0 that belongs to AMSIO register so the Adc driver also updated the functions related to AMSIO register. Requirement source: The header file of Base: [Auto RealTime Drivers / base / 695577cb697 NXP Bitbucket|https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/695577cb69745cb7bc217aace2795f55b38dcb09#specific/S32K3XX/header/S32M27x_ADC.h] and RM.pdf(S32K39RM_and_S32K37RM_Rev2) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update Adc_Sar_EnableHighSpeed function
ARTD-96763	New Feature	[AE]Support a API to change RAW bit. NewWorkDescription: RTD Driver shall implement way how to set RAW bit and not to set it globally in config (add API to change RAW). This prevents us from performing some safety checks. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-96876	New Feature	[mem_exfls] Update general to sync with XSPI from merged branch NewWorkDescription: Update general to sync with XSPI from merged branch ARTD-85708 Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-96870	Bug	[GPT] Not correct header file for K374 and K376 Detailed description (how to reproduce it): Include header file name for K376 and K374 are not correct !image-2023-10-17-13-33-18-459.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Gpt_TS_M03 Observed behavior: build fail Expected behavior: build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Include all IP module should be S32K37_PIT.h
ARTD-96885	Bug	[S32K3XX_S32M27x_4..0.0] Fix gen fail for S32DS because S32K3X8_USDHC.h not found Detailed description (how to reproduce it): /generate/include/Usdhc_Ip_DeviceRegisters.h", line 41: fatal error #2330: STDERR: cannot open source file "S32K338_USDHC.h" STDERR: #include "S32K338_USDHC.h" STDERR: STDERR: Similar with K328 and K348 Preconditions: !image-2023-10-17-14-13-15-093.png! Test Case ID (internal TC that caught the defect) optional: Mem_Eep_TC_COT_0001 Observed behavior: !image-2023-10-17-14-13-31-193.png! Expected behavior: Gen Successfull in S32DS for S32K328 S32K338 S32K348 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-96888	Bug	[S32K3xx_S32M27x_4.0.0] [PORT][Ecpd] Error occurs when configuring the boundary pin Detailed description (how to reproduce it): Step1: Create new project on s32ds, add port component (S32K396 s32k396_mapbga289, S32K388 s32k388_mapbga289) Step2: config port and generate ecpd, ecvd, mex file, .c.h file ({*}original_configuration{*}) Step3: Open port 's plugin, update plugin.xml, link to ecpd file instead of xdm file !image-2023-10-17-11-18-28-113.png|width=958,height=120! Step4: Create new project on EB tresos, import ecvd file and generate epc file Step5: import epc file from EB to S32CT project and generate .c .h file ({*}new_configuration{*}) Step6: Compare original_configuration and new_configuration Preconditions:

ID	Subtype	Headline and Description
		N/A Test Case ID (internal TC that caught the defect) optional: Port_TS_COT_019 Observed behavior: {*}1{*}. An error was generated when configuring the boundary pin (S32K396) !image-2023-10-17-13-36-03-777.png|width=1002,height=470! !image-2023-10-17-13-37-04-289.png|width=1118,height=399! !image-2023-10-17-13-37-36-698.png! {*}2{*}. An error was generated on PTA0 (MODE = {*}FXIO_FXIO_D2_IN{*}) when importing epc from EB to CT (epc file attached below)(S32K396) !image-2023-10-17-14-14-50-585.png! {*}3{*}. EPC file doesn't work on S32DS with S32K388 derivative !image-2023-10-18-10-18-22-695.png! Expected behavior: ecpd works correctly Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-96947	Bug	[S32K3xx_S32M27x_4.0.0] [DIO] Different sort order of Channel ID when importing epc file from EBT into S32DS Detailed description (how to reproduce it): Different sort order of channel ID when importing epc file from EBT into S32DS Preconditions: The order of channel ID arrangement when porting from EB to S32DS must be the same Test Case ID (internal TC that caught the defect) optional Dio_TS_010 Observed behavior: Config EB: !image-2023-10-18-09-51-11-444.png|width=751,height=447! Import to CT The order of channel id is changed leading to run test fail !image-2023-10-18-10-11-18-204.png|width=675,height=382! The difference of the generate file when porting from EB to CT leads to run test fail !image-2023-10-18-09-58-09-457.png|width=822,height=349! Expected behavior Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional
ARTD-96952	Bug	[S32K3xx_S32M27x_4.0.0] DIO: Id node Dio VirtWrapper Support different between EB and S32DS Detailed description (how to reproduce it): ID node Dio VirtWrapper Support different between EB and S32DS EB: <v:var name="*{color:red}DioVirtWrapperSupport{color}*" type="BOOLEAN"> S32DS: <bool id="*{color:red}VirtWrapperSupport{color}*" label="Dio VirtWrapper Support"> Preconditions: All Derivative Test Case ID (internal TC that caught the defect) optional: Dio_TS_020 CFG=3 Observed behavior: ID node Dio VirtWrapper Support different between EB and S32DS Capture 1*: Id node on EB Capture 2*: Id node on S32DS Expected behavior: Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-96937	Bug	[Pwm] Not correct header file for K374 and K376 Detailed description (how to reproduce it): Include header file name for K376 and K374 are not correct. Emios header file: !image-2023-10-18-09-43-09-474.png! Flexio header file: !image-2023-10-18-10-15-15-692.png! FlexPwm has no header file: !image-2023-10-18-10-18-21-836.png! In the header file of Base module S32K37_EMIOS.h is placed. !image-2023-10-18-09-47-14-123.png! Preconditions: Build any test at S32K374 or S32K376 Test Case ID (internal TC that caught the defect) optional: Pwm_TS_COT_001 Observed behavior: Build fail Expected behavior: Build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Rename S32K374_[Module].h to S32K37_[Module].h
ARTD-97014	New Feature	[S32K3xx_S32M27x_4.0.0] PLATFORM: Improve CE index in CCOV report NewWorkDescription: Improve CE_zero_percent Platform_Ipw_InitNonCore function is 0% because MSCM is not support. Please add barrier for this function. !image-2023-10-18-15-16-01-653.png|width=996,height=323! Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: all comments "(3) Technically feasible: This statement/branch has not been reached, and test improvement is needed" need to investigate to add or create some tests to cover more lines of code
ARTD-97033	Bug	[S32K3xx_S32M27x_4.0.0][S32K396][S32CT] build fails when configuring pin in emios, cmp mode Detailed description (how to reproduce it): Create new project on s32ds S32K396 Add port component, config pin as emios (or cmp input) mode update code and build Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: n/a Observed behavior: build fail on s32ds !image-2023-10-18-16-08-51-123.png|width=533,height=312! !image-2023-10-18-16-08-15-736.png|width=945,height=563! !image-2023-10-18-16-11-14-808.png! Expected behavior: build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/a

ID	Subtype	Headline and Description
ARTD-97036	Bug	[ICU]The element order of the array Icu_Ipw_IpChannelConfig_PB_VS_0 is generating is incorrect on S32DS Detailed description (how to reproduce it): When using a configuration that uses the channels on the interface in the same order as the mex file below, the element order of the cu_Ipw_IpChannelConfig_PB_VS_0 array being created is incorrect. marco ICU_GET_PULSE_WIDTH_API always outputs as STD_OFF despite emios channel configuration If channels are configured as NMI only, the ICU_WKPU_MODULE data type is not created !screenshot-1.png|thumbnail! Preconditions: Configure channels on the S32DS interface Test Case ID (internal TC that caught the defect) optional: Icu_TC_WBT_0154,Icu_TC_WBT_0155,Icu_TC_WBT_0156,Icu_TC_WBT_0157,Icu_TC_WBT_0266(Icu_TS_041) Icu_TC_WBT_0402,Icu_TC_WBT_0404,Icu_TC_WBT_0405(Icu_TS_044) Icu_TS_040 Observed behavior: the element order of the cu_Ipw_IpChannelConfig_PB_VS_0 array being created is incorrect. Expected behavior: the element order of the cu_Ipw_IpChannelConfig_PB_VS_0 array being created is incorrectly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change the generated code to produce the correct element order Check Icu_Cfg.h file on S32DS to generate correct ICU_GET_PULSE_WIDTH_API macro need to check the condition for Icu_Ipw_IpConfig_PB_VS_0 to create a containing element ICU_WKPU_MODULE
ARTD-97030	New Feature	[ZIPWIRE] Support LFAST PLL configuration NewWorkDescription: lfast pll will be be clear all bit in PLLCR register after lfast soft reset (pxLfastBase->MCR = DIGRF_TOP_MCR_DRFRST_MASK) in Zipwire_Init. So i think zipwire module should support lfast pll configuration. Mcu module no need to support this pll Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support lfast pll configuration in tresos and s32ct
ARTD-97136	Bug	[GPT] Build code fail on S32DS Detailed description (how to reproduce it): Step 1: Clean generate Wdg_TS_005 with GENERATOR=s32ct Step 2: Build Wdg_TS_005 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Wdg_TC_FCT_0005 Wdg_TC_FCT_0006 Wdg_TC_FCT_1011 Wdg_TC_FCT_1004 Observed behavior: Build code fail on S32DS !image-2023-10-18-17-24-15-079.png|width=1089,height=267! Expected behavior: TS build code successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-97149	Bug	[PWM][FLEXPWM] Some functions are not yet supported for FLEXPWM Detailed description (how to reproduce it): Pwm_SetClockMode function is not yet supported for Flexpwm in HLD !image-2023-10-18-18-00-20-571.png|width=409,height=331! Pwm_SyncUpdate is not supported for FlexPwm :This function is used to upadate duty synchronization for channels in given module, this should be called after Pwm_SetPeriodAndDuty_NoUpdate() or Pwm_SetDutyCycle_NoUpdate() API. However, Flexpwm is not supported. !image-2023-10-18-18-14-00-488.png|width=434,height=268!

ID	Subtype	Headline and Description
		Pwm_GetOutputState {*}{{*}}is not yet supported for FlexPwm{{*}} }}:\{*}When call Pwm_GetOutputState function and and it is processed in the Pwm_Ipw_GetOutputState function, this function is not supported for FlexPwm > State output signal = PWM_LOW > unexpected !image-2023-10-18-18-37-25-825.png|width=415,height=274! !image-2023-11-02-17-09-10-871.png|width=427,height=548! Similar to function Pwm_Ipw_ValidateDeadTime and Pwm_Ipw_ValidateSetPhaseShift, it has not yet been support for FlexPwm. !image-2023-10-18-18-18-01-390.png|width=424,height=185! !image-2023-10-18-18-18-49-501.png|width=423,height=217! Preconditions: Config with FlexPwm Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Some functions are not supported for FlexPwm Expected behavior: Some functions are supported for FlexPwm Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-97166	Bug	Typo in Flexio_Uart_Ip_Cfg.h code generation Detailed description (how to reproduce it): When using UART component in Tresos, Flexio_Uart_Ip_Cfg.h in line 46 generates the following line: #include "Flexio_Uart_Ip_VS_0_PB{*}C{*}fg.h" (uppercase C) This generates compilation error as this file is generated as Flexio_Uart_Ip_VS_0_PB{*}c{*}fg.h (lowecase c). Preconditions: RTD: S32K3_RTD_3_0_0_P10_D2307_ASR_REL_4_7_REV_0000_20230726 Tresos: 29.0,0 Observed behavior: Code generates include incorrectly. Expected behavior: Code generation should change to #include "Flexio_Uart_Ip_VS_0_PB{*}c{*}fg.h Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-97176	Bug	[Gpt] eMIOS counter witdth corresponds to different derivatives Detailed description (how to reproduce it): GptChannelTickValueMax is 65535 (2^16) which is incorrect for eMIOS Gpt channel of derivative S32K39, S32K388 and S32K37. According to reference manual, the eMIOS counter width is 24 bit for derivative S32K39, S32K388 and S32K37. {_}S32K39RM_and_S32K37RM_Rev2{_}{_}!image-2023-10-19-09-55-51-041.png!{_} {_}S32K3xxRM_Rev8_DraftB{_}{_}!image-2023-10-19-09-59-17-393.png!{_} Preconditions: Configure eMIOS Gpt channel for S32K39, S32K388 and S32K37. Observed behavior: EB config: !image-2023-10-19-10-04-07-234.png! CT config: !image-2023-10-19-10-12-48-481.png! Expected behavior GptChannelTickValueMax should be 16,777,216 (2^24) for S32K39, S32K388 and S32K37.
ARTD-97213	Bug	[SPI][S32K3] Fix findings in code review checklist Detailed description (how to reproduce it): Fix findings in code review checklist.

ID	Subtype	Headline and Description
		Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Fix findings in code review checklist. Expected behavior: Fix founding in code review checklist. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix findings in code review checklist.
ARTD-97245	Bug	[S32K3XX] [MEM_EXFLS] Fix gen fail ECPD on DS Detailed description (how to reproduce it): gen fail ECPD on DS !image-2023-10-20-10-21-45-563.png|width=809,height=461! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: function works properly Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97266	New Feature	[GPT] Update SchM_Check_Gpt files in RTE NewWorkDescription: Run the script from rte repo and add the new SchM_Check_Gpt files in rte Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Run the script from rte repo and add the new SchM_Check_Gpt files in rte
ARTD-97433	Bug	[PORT][S32K3XX_S32M27X] Inconsistently generated files between S32CT and EBT when importing EPC file Detailed description (how to reproduce it): Step 1: Create a new project on S32DS for S32K3XX Step 2: Add Port component Step 3: Import epc files from EBT to S32CT. Inconsistently generated files between S32CT and EB when importing EPC file from EBT to S32CT {*}Issue 1: Igf_Port_Ip_Cfg.h ({*}{*}all derivative{*} except S32K396) !image-2023-10-20-17-55-05-191.png|width=1054,height=309! Issue 2: Siul2_Port_Ip_Defines.h (only S32K388) !image-2023-10-27-10-55-25-986.png|width=1071,height=641! Issue 4: modules.h_ _(all derivative epc file as attached) !image-2023-10-20-17-58-14-653.png|width=1130,height=97! Issue 5: 5.1 Missing GPI pin mode when importing EPC to S32CT (all derivative) (E.g: PTA24 PTA25 for S32K388) 5.2 When addding GPI pin: (E.g: PTA15 for S32K396) !image-2023-10-27-14-50-02-315.png|width=983,height=189! {_}*can not config "Initial value" on CT*{_}{*}{{*}}{_}*!image-2023-10-27-14-47-13-666.png|width=928,height=70!*{_} {_}*config and generate successfully on EB*{_}{*}{{*}} !image-2023-10-27-14-48-58-005.png|width=589,height=398!

ID	Subtype	Headline and Description
		Issue 6: Siul2_Port_Ip_VS_0_PBcfg.c (all der) !image-2023-10-20-18-04-36-866.png|width=738,height=337! Issue 7:*_ 7.1: Error when importing epc, direction on EB is "PORT_PIN_HIGH_Z" !image-2023-10-27-14-15-39-936.png! !image-2023-10-27-14-16-04-454.png|width=1008,height=32! 7.2: On ct, "PortPinDirection" is being depended on "PortPinMode" CT: !image-2023-10-27-14-24-30-309.png|width=621,height=381! !image-2023-10-27-14-25-38-930.png|width=623,height=397! EB: !image-2023-10-27-14-27-30-581.png|width=385,height=454! => when configuring {*}PortPinMode = output mode{*}, *PortPinDirection = PORT_PIN_IN on EB => import epc into CT => generated code is inconsistent between eb and ct !image-2023-10-27-14-35-16-190.png|width=906,height=359! {_}Preconditions:{_}{} Compare generated file between S32CT and EBT Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Inconsistently generated files between S32CT and EB Expected behavior: Generated file between S32CT and EB are the same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97468	Bug	[S32K388][I2S] Error "Unsatisfied components dependencies" occurs after adding all components Preconditions: 1. Install S32DS 3.5 base: S32DS.3.5_b220726_win32.x86_64.exe 2. Install Platform 3.5.6: com.nxp.s32ds.update_3.5.6.20230915073815.zip 3. Install S32K3xx dev package: com.nxp.s32ds.s32k3xx.update_3.5.6.20230915093013.zip 4. Install RTD data: S32K3XX_RTD_4_7_CD01_4_0_0_DS_updatesite_2309_signed_2009.zip Test Case: 1. Create project for S32K388 enable RTD 2. Open Peripherals tool 3. Open "Manage SDK Components" 4. Adding all components by clicking on "Select all" Observed behavior: 4. Error: Unsatisfied components dependencies! The following dependencies are missing: [Rte_Adc(ULTILITIES), Rte_I2s(ULTILITIES)] Expected behavior: 4. No error, driver can be added successfully
ARTD-97471	Bug	[S32K3XX][EthIf][EthSwt][EthTrcv]The error message:' 'Unsatisfied components dependencies!' when adding all SDK component from Manage SDK component. Detailed description (how to reproduce it): 1. Create project single core with enable SDK S32CT. 2. Open Peripheral tool. 3. Click 'Manage SDK component' option on toolbar. 4. Verify name of SDK components. 5. Tick all SDK components. Test Case ID (internal TC that caught the defect) optional: TL30_00380_01190 Observed behavior:

ID	Subtype	Headline and Description
		5.* There is error message 'Unsatisfied components dependencies! The following dependencies are missing: [Csm(DRIVER), Crylf(DRIVER), Wdglf(DRIVER)]'. 'OK' button is disable. Expected behavior: 5. SDK components are added and there isn't error 'Unsatisfied components dependencies! The following dependencies are missing: [Csm(DRIVER), Crylf(DRIVER), Wdglf(DRIVER)]'. 'OK' button is enable.
ARTD-97474	Bug	[S32K3XX][GPT] The error message:' 'Unsatisfied components dependencies!' when adding all SDK component from Manage SDK component. Detailed description (how to reproduce it): 1. Create project single core with enable SDK S32CT. 2. Open Peripheral tool. 3. Click 'Manage SDK component' option on toolbar. 4. Verify name of SDK components. 5. Tick all SDK components. Test Case ID (internal TC that caught the defect) optional: TL30_00380_01190 Observed behavior: 5.* There is error message 'Unsatisfied components dependencies! The following dependencies are missing: [Csm(DRIVER), Crylf(DRIVER), Wdglf(DRIVER)]', Rte_Gpt[UTILITIES]. 'OK' button is disable. Expected behavior: 5. SDK components are added and there isn't error 'Unsatisfied components dependencies! The following dependencies are missing: [Csm(DRIVER), Crylf(DRIVER), Wdglf(DRIVER)], Rte_Gpt[UTILITIES]'. 'OK' button is enable.
ARTD-97489	Bug	[MCU]Wait states are incorrect in Clock_Ip_Specific.c Detailed description (how to reproduce it): Flash Wait state value need to get difference value in derivatives of S32K3 as below: In datasheet: refer to the image WaitStateDataSheet and WaitStateData1 In driver: just only one group of Wait state value created to use for all derivatives and it is following the table 29. Refer the image WaitStateInDriver. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Flash Wait State value are same for all derivatives. Expected behavior: Flash Wait State value need to follow Datasheet. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-97505	New Feature	[SPI]Activate host request enable feature NewWorkDescription: Activate HREQ feature to control the start of a SPI bus transfer !image-2023-10-23-10-58-07-418.png! !image-2023-10-23-10-58-56-786.png! Requirement source: CPRT (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: ARTD-84804 [Analysis]SPI/DMA Transfer Based on Periodic External or Internal (Timer) Event part 1 NXP JIRA
ARTD-97533	Bug	[PWM] [EMIOS] The array of channels used according to final variant when configuring multiple variants Detailed description (how to reproduce it): For the test where I configure EMIOS to use the master bus, in the array of channels used, it will include the master bus channel (for example, the image is channel 22. master bus F). !image-2023-10-23-15-25-15-673.png|width=675,height=288! !image-2023-10-23-15-25-58-994.png|width=708,height=287! But if I configure using 3 VS. For VS_0 or VS_1, I use the master bus, but VS_2 (last VS) uses bus_internal, so it is taking the last VS (ie, not including the master config channel for VS_0 or VS_1). !image-2023-10-23-15-27-35-975.png|width=711,height=360!

ID	Subtype	Headline and Description
		!image-2023-10-23-15-27-54-288.png|width=713,height=359! !image-2023-10-23-15-28-08-138.png|width=711,height=336! Preconditions: Config more than 1 VS and VS1 used master bus and VS2 did not use master bus Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: in the array of channels used, it will not include the master bus channel. Expected behavior: in the array of channels used, it will include the master bus channel. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-97564	Bug	[MCU] add support PLLDIG.PLLCLKMUX[REFCLKSEL] forM27x Detailed description (how to reproduce it): we have PLLDIG.PLLCLKMUX[REFCLKSEL] in the clock diagram (M27x) but this isn't supported in our driver Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: PLLDIG.PLLCLKMUX[REFCLKSEL] is not available in Mcu driver,ET,CB Expected behavior: PLLDIG.PLLCLKMUX[REFCLKSEL] is available in Mcu driver,ET,CB Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-97735	New Feature	[memexfls] [IMPLEMENTATION] Update code to support multicore Type 3 for MEMACC Driver NewWorkDescription: Move all global variable to Share no cache region. Add check core ID for each job. Only the core that requests the job can perform the job in the mainfunction Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Reference the way to implement the multicore "Type 3" on the FLS Driver (AUTOSAR 4.4) Document: NXP_RealTimeDrivers_Multicore.pptx; Autosar Memstack Multicore.pptx
ARTD-97775	Bug	[S32K3xx_S32M27x_4.0.0] DIO_PORT: Derivative S32K3XX not support PDACindex VirtWrapper Detailed description (how to reproduce it): In RM S32M276 the PDAC2 address is reserved and not support PDAC2 VirtWrapper but node virtwrapper still selects PDAC2 in EB and S32DS config. In RM S32K358 the PDAC4 address is reserved and not support PDAC4 VirtWrapper but node virtwrapper still selects PDAC4 in EB and S32DS config. In RM S32K342 the PDAC2 address is reserved and not support PDAC2 VirtWrapper but node virtwrapper still selects PDAC2 in EB and S32DS config. Preconditions: S32M276, S32K358 Test Case ID (internal TC that caught the defect) optional: TS_020_cfg1 Observed behavior In file S32M27X_memory_map: PDAC2 address is reserved !image-2023-10-25-11-03-26-715.png|width=817,height=322! Node Dio VirtWrapper Support still selects PDAC2 in EB and S32DS config config EB: !image-2023-10-25-11-05-27-334.png|width=512,height=304! Config S32DS:

ID	Subtype	Headline and Description
		!image-2023-10-25-11-06-08-498.png|width=575,height=260! Expected behavior Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional
ARTD-97810	Bug	[ETH] Schema file is not using VendorApiInfix In Eth_43_GMAC.xdm VendorApiInfix is configured as OPTIONAL true : <a:a name="OPTIONAL" value="true" <a:a name="READONLY" value="false" Since Eth driver is using VendorApiInfix the lines should be replaced with : <a:a name="OPTIONAL" value="false" <a:a name="READONLY" value="true"
ARTD-97803	Bug	[S32K3XX_S32M27x_4..0.0][Mem_Eep] Update clock source USDHC for IP because Mcu change source clock USDHC Detailed description (how to reproduce it): Clock Source Usdhc source info no found because Mcu change name Usdhc_Clk Preconditions: !image-2023-10-25-14-13-54-140.png! Test Case ID (internal TC that caught the defect) optional: Ip_Sd_TC_FCT_0001 Ip_Sd_TC_FCT_0002 Ip_Sd_TC_FCT_0003 Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-97815	Bug	[mcu] Verify that the driver can build using a Variant name containing lowercase characters ! This was marked as fixed in https://jira.sw.nxp.com/browse/ARTD-79006, but is still persisting in S32K3XX 4.0.0 CD01. ! Report from EB regarding* \{*}S32K3XX 4.0.0 CD01{*}{*}:{*} " In file Clock_Ip_PBcfg.h at line 67, The Condition check for Vendor id fails, as "text:toupper($postBuildVariant)" is missing for this condition into the plugin and reports below error #error "Clock_Ip[!IF "var:defined('postBuildVariant')"!]_[!"text:toupper($postBuildVariant)"!][!ENDIF!]_PBcfg.h and Clock_Ip_Types.h have different vendor ids" FYI the Snippet are attached for the above explanation. Note: Similar case is observed in multiple places in the module where "text:toupper($postBuildVariant)" is missing." See attached photos. This issue does not apply to drivers with PreCompile support only, and can be closed in case the driver does not have PostBuild Variant support. Verify that the driver code can successfully build if a variant name containing lower case characters is used. For drivers which support PostBuildVariant, variant names included in defines used for file version checks might be generated in some files as is, using both lower and upper case characters, and in other files they might be changed to all upper case characters; the same applies for file names and file inclusions which might contain variant names. This situation leads to a build error from file version checks as the defines are not the same.

ID	Subtype	Headline and Description
		Code generation should be updated so that all variant name usage in the defines is generated with uppercase characters, and file names to be as-is, in order to avoid any issues for defines which include the variant names. How to test: # Choose a test suite with a PB variant configuration, generate and build the code and make sure everything is ok. # Open EB Tresos: ## On the right hand side, click on the sidebar tab, and then double-click on the "Edit Selectable PostBuildVariants" item. ## In the "Predefined Variants" Tab, add a new variant called "Variant_0", and select its PostBuildSelectableCriterion as 0. (see Picture 1) ## Close the "Edit Selectable PostBuildVariants" tab and save then changes when prompted. ## Open the EcuC module configuration; got to the tab "EcucPostBuildVariantRef", and for the present reference, choose the new variant, "Variant_0". (See Picture 2) ## Go in the "General" tab of EcuC, and in the "EcucPostBuildVariants" container, for "EcucSelectedPostBuildVariantRef" select the new reference to "Variant_0" (See Picture 3) ## Save the project with Ctrl+S, and click on the "Generate Code" button. # Build the project normally using the "p s2" command in ZTH. # If the project builds successfully, then no changes are required in the driver. # If build errors appear. it might be due to incorrect names of files/defines, coming from the variant name. For example, there might be errors coming from the file version checks (See Picture 4). If you look in the code, you will find that the defines or file names are different between two files (See Picture 5). The errors are due to the fact that in some places, the code will generate variant names with upper case, and in other places it will not modify the variant name. Update code generation so that variant names are always UPPER CASE in defines, and as is in file names. For example, if Variant_0 is set, all defines will be {*}<MDL>{*}{*}_AR_RELEASE_MAJOR_VERSION_VARIANT_0_PBCFG{*}, and file names would be {*}<MDL>_Variant_0_PBcfg.h{*}.
ARTD-97832	Bug	[CRYPTO_NG] Crypto_43_HSE_KeyExchangeCalcPubVal does not report CRYPTO_E_SMALL_BUFFER to DET Detailed description (how to reproduce it): Crypto_43_HSE_KeyExchangeCalcPubVal return CRYPTO_43_HSE_RET_SMALL_BUFFER without DET error Preconditions: CryptoDevErrorDetect enable publicValueLengthPtr is small Test Case ID (internal TC that caught the defect) optional: Crypto_TC_FCT_0013 Observed behavior: !image-2023-10-25-16-34-55-286.png! Expected behavior: SWS_Crypto_00195: If a Crypto Driver API is called and any buffer addressed during the operation is too small, then the operation shall not be performed. If development error detection for the Crypto Driver is enabled, then the API function shall report CRYPTO_E_SMALL_BUFFER to the DET, else return E_NOT_OK. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-97829	Bug	[PORT][wizard_data] Missing default pins in Pins tool when creating new project on S32DS Detailed description (how to reproduce it): [PORT][wizard_data] Missing default pins in Pins tool when creating new project on S32DS Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing default pins in Pins tool when creating new project on S32DS Expected behavior: At least 1 pin needs to be added automatically when creating new project on S32DS. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-97835	Bug	[PORT][ResGenFSL] Unnecessary mode generated in mapping files Detailed description (how to reproduce it): Unnecessary mode are generated in mapping files. The ResGenFsl scripts need to be updated to improve this kind of case. Preconditions: NA

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The mapping files were generated with unusual points. Expected behavior: The mapping files should be correctly generated without unusual points. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-97862	Bug	[MEM_INFLS] Bswmd not generated Detailed description (how to reproduce it): Generate the Mem_Infls plugin with the Bswmd.rxml. Observed behavior: Mem_43_INFLS_Bswmd.arxml is generated empty, with only the header file, and errors are reportet by the bswmd tool. Expected behavior: Bswmd file should be generated without any issues. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix Bswmd generation.
ARTD-97867	Bug	[MCU]RamSize in the structure wasn't used as Pointer. In the structure Ram_Ip_RamConfigType, RamSize was declared as a Pointer, but it wasn't used a Pointer. What reason did driver implement this?
ARTD-97980	New Feature	[mem_exfls] Update CT part to sync with XSPI merged branch impact to K3 release NewWorkDescription: Update CT part to sync with XSPI merged branch impact to K3 release ARTD-85708 Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-97986	Bug	[S32K3XX] [MEM_EXFLS] CRC checking failed Detailed description (how to reproduce it): !image-2023-10-26-15-10-12-678.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_001 Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98064	Bug	[ICU][S32DS]Cannot create Icu components on some derivatives Detailed description (how to reproduce it): When configurate in S32DS for S32K374 and S32K376, it lack of configuration components (Icu, Emios_Icu, Wkpu, siul2_icu, Cmp : !image-2023-10-27-09-33-41-406.png|thumbnail! Preconditions: Cannot create Icu components on some derivatives Test Case ID (internal TC that caught the defect) optional: Icu_TC_COT_0239(Icu_TS_COT_001) Observed behavior: Cannot create Icu components on some derivatives Expected behavior: Can create Icu components on some derivatives Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: add some derivatives on file sdk_manifest_icu
ARTD-98067	New Feature	[memInfls] [IMPLEMENTATION] Update code to support multicore Type 3 for MEMACC Driver NewWorkDescription: Move all global variable to Share no cache region. Add check core ID for each job. Only the core that requests the job can perform the job in the mainfunction Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Reference the way to implement the multicore "Type 3" on the FLS Driver (AUTOSAR 4.4) Document: NXP_RealTimeDrivers_Multicore.pptx; Autosar Memstack Multicore.pptx
ARTD-98070	New Feature	[mem_eep] Update code to support multicore Type 3 for MEMACC Driver NewWorkDescription: Move all global variable to Share no cache region. Add check core ID for each job. Only the core that requests the job can perform the job in the mainfunction Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Reference the way to implement the multicore "Type 3" on the FLS Driver (AUTOSAR 4.4) Document: NXP_RealTimeDrivers_Multicore.pptx; Autosar Memstack Multicore.pptx
ARTD-98095	Bug	[S32K3xx_S32M27x_4.0.0] [DIO] Fix compiler warnings Detailed description (how to reproduce it): Compiler warning report have waring on GHS and GCC sheet (attached file below) link station: [http://panama.ea.freescale.net/0/project/custom_compilerwarning/20230816092320688000/details|http://bengal.ea.freescale.net/0/project/custom_compilerwarning/details] Preconditions: tag: DIO_132 Test Case ID (internal TC that caught the defect) optional: Test suite: Dio_TS_020_cfg1_tresos_CORE0 Observed behavior: 207|Dio_lpw_ReverseBits' defined but not used [-Wunused-function]| 207 \ static Dio_PortLevelType Dio_lpw_ReverseBits {_}*Expected behavior:*{_}Compiles without warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-98114	Bug	[ICU] Wrong pin channel Icu LPCMP in S32M276 Detailed description (how to reproduce it): When config Icu LPCMP Negative Input Muxing , just allowed config CMP_IN 0 to 3, but in fact S32M276 have CMP_IN 1, 2, 4, 5. When config CMP_IN 4,5 have error config. !image-2023-10-27-15-08-28-119.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Icu_TS_111 Observed behavior: Generate fail Expected behavior: Test gen pass with config right channe CMP Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-98170	Bug	[S32K3XX_S32M27x_4..0.0][Mem_Eep] Fix compiler Warning for IAR Detailed description (how to reproduce it): Fix compiler warning for IAR Preconditions:

ID	Subtype	Headline and Description
		!image-2023-10-29-11-11-22-061.png! Test Case ID (internal TC that caught the defect) optional: Ip_TC_FCT_001 Ip_TC_FCT_002 ... Observed behavior: Expected behavior: No CWE Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-98222	Bug	[S32K3xx_S32M27x_4.0.0] MEM_EXFLS: Update resources Detailed description (how to reproduce it): Some resources are incorrect, for example: Mem.ExFls.Qspi.Hyperflash.Available: 0, in s32k3x8 derivatives Mem.ExFls.External.Qspi.Header: S32K39_QUADSPI.h, in s32k374, s32k376 Mem.ExFls.External.LUT.Instruction.List need to update Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_COT_003 Observed behavior: generate step failed Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98216	Bug	[Gpt] Missing function in driver Detailed description (how to reproduce it): Function in "ReqExport.txt" file but does not include in "*.h" files of driver code: uint32 Emios_Gpt_Ip_GetCounterValue(uint8 instance, uint8 channel) Functions plugin list: [bengal.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fY2hlY2tpbnRlcmZhY2VcMjAyMzExMTAwNTU4MzUxNjMwMDBcZG93bmxvYWRzXEd http://bengal.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fY2hlY2tpbnRlcmZhY2VcMjAyMzExMTAwNTU4MzUxNjMwMDBcZG93bmxvYaWRzXEd Functions requirement list: [bengal.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fY2hlY2tpbnRlcmZhY2VcMjAyMzExMTAwNTU4MzUxNjMwMDBcZG93bmxvYWRzXEd http://bengal.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fY2hlY2tpbnRlcmZhY2VcMjAyMzExMTAwNTU4MzUxNjMwMDBcZG93bmxvYaWRzXEd Compare result between plugin and requirement: [bengal.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fY2hlY2tpbnRlcmZhY2VcMjAyMzExMTAwNTU4MzUxNjMwMDBcZG93bmxvYWRzXEd http://bengal.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fY2hlY2tpbnRlcmZhY2VcMjAyMzExMTAwNTU4MzUxNjMwMDBcZG93bmxvYaWRzXEd Expected behavior: Driver code have all functions that are listed in requirement. Check tap characters Driver code has tap characters which need to be replaced by spaces. !image-2023-11-06-10-39-16-434.png!

ID	Subtype	Headline and Description
		[oman.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fcGx1Z2luY2hlY2tcMjAyMzExMDMxODU1NDc3OTQwMDBcZG93bmxvYWRzXHJlZ2V4 http://oman.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fcGx1Z2luY2hlY2tcMjAyMzExMDMxODU1NDc3OTQwMDBcZG93bmxvYWRzXHJlZ2V4
ARTD-98352	Bug	[ICU]The difference when generating files between EB and S32DS Detailed description (how to reproduce it): There are some differences between the generated files generated on the EB and S32DS interfaces, this does not affect the driver, but the condition is required to generate the same macro between EB and S32DS Preconditions: Generate on EBT tresos and S32CT and compare generated files Test Case ID (internal TC that caught the defect) optional: Icu_TS_011, Icu_TS_030 Observed behavior: Differences between generated files Expected behavior: Similarity between generated files Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ARTD-98363	New Feature	[WDG] Add validation code for Wdg_Service()
		
		NewWorkDescription:
		Add validations for Wdg_Service() calls, in Wdg_Channel.c. This should satisfy requirements SWS_Wdg_00035, SWS_Wdg_00052.
		
		These should be similar to other Wdg functions.
		
		Requirement source:
		SWS_Wdg_00035: When development error detection is enabled for the Wdg Driver module: the watchdog servicing routine shall check whether the Wdg module's state is WDG_IDLE (meaning the watchdog driver and hardware are initialized and the watchdog is currently not being triggered or switched). If this is not the case, the function shall not trigger the watchdog hardware but raise the development error WDG_E_DRIVER_STATE.
		SWS_Wdg_00052: When development error detection is enabled for the Wdg Driver module: the watchdog servicing routine shall set the Wdg module's state to WDG_BUSY during its execution (indicating, that the module is busy) and shall reset the module's state to WDG_IDLE (indicating, that the module is initialized and not busy) as last operation before it returns.
		
		Proposed solution optional:
		For example, as the verifications in Wdg_SetTriggerCondition in Wdg_Channel.c
		
		#if ((WDG_VALIDATE_GLOBAL_CALL == STD_ON) (WDG_MULTICORE_ENABLED == STD_ON))
		Std_ReturnType Valid = (Std_ReturnType)E_NOT_OK;
		#endif
		
		#if (WDG_MULTICORE_ENABLED == STD_ON)
		volatile uint32 CoreID;
		
		CoreID = (uint32) Wdg_GetCoreID();
		Valid = Wdg_ChannelValidateCoreUsed(CoreID, Instance,WDG_SETTRIGGERCONDITION_ID,WDG_E_PARAM_CONFIG);
		if ((Std_ReturnType)E_OK == Valid)
		{
		#endif
		#if (WDG_VALIDATE_GLOBAL_CALL == STD_ON)
		Valid = Wdg_ChannelValidateTrigerCondition(Instance);
		if ((Std_ReturnType)E_OK == Valid)
		{
		#endif / (WDG_VALIDATE_GLOBAL_CALL == STD_ON /

ARTD-98377	Bug	[PWM]After calling Pwm_DeInit, the signal pin does not return to the idle state Detailed description (how to reproduce it): Configure the polarity and idle state of the channels as shown below and enable PwmEnableMaskOutputs !image-2023-10-31-14-59-17-083.png|width=787,height=263! !image-2023-10-31-15-01-04-128.png! After Init, Using Pwm_MaskOutputs for channel 0 and channel 1, Then calling Pwm_DeInit without calling Pwm_UnMaskOutputs. !image-2023-10-31-15-21-31-390.png|width=677,height=405! Preconditions: Call Pwm_DeInit after calling Pwm_MaskOutputs without calling Pwm_UnMaskOutputs Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: After calling Pwm_DeInit, the signal pin does not return to the idle state

ID	Subtype	Headline and Description
		Expected behavior: After calling Pwm_DeInit, the signal pin will return to the idle state Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98404	New Feature	[ADC] - S32K396 Support limit range for DSPSS parameters in default NXP use case configuration NewWorkDescription: Support limit range for DSPSS configuration parameters Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add limit range for each DSPSS parameter in configurator
ARTD-98432	New Feature	[ADC] Implement API Adc_Sar_Ip_SetUserGainAndOffset NewWorkDescription: Implement Adc_Sar_Ip_SetUserGainAndOffset API for IPL to be used by HLD function Adc_SetUserGainAndOffset. Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [....]
ARTD-98444	New Feature	[S32K3xx_S32M27x_4.0.0] PLATFORM: Fix UUIDs is duplicated NewWorkDescription: Duplicated UUIDs in Platform.xdm and ae.xdm ECUC:bdee5480-3705-4c45-aea3-6775b0d7d806 !image-2023-11-01-09-44-34-343.png! http://oman.ea.freescale.net/0/project/download/ ZDpcbG9jYWxfMDFcb3V0cHV0XGFydGlmYWN0c1xjdXN0b21fcGx1Z2luY2hlY2tcMjAyMzEwMzExNzI3NTU1MjcwMDBcZG93bmxvYWRzXHV1aWRfc Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: UUID must be unique, please change platform UUID to another UUID
ARTD-98456	Bug	[GPT][TRESOS] Some mistakes when using Variant name containing lowercase characters Detailed description (how to reproduce it): Configurate test in EB tresos use variant name containing lowercase characters, it generate something wrong(lack of variant in name). They are updated in ARTD-78973 , however they still not enough. . Some mistakes as below: !image-2023-11-01-10-46-11-132.png! {*}More mistakes are listed in the file.xlsx below{*}. Open and check in it for detail. [^Lower_case_tresos.xlsx] [^Gpt_TS_012_cfgtresos_CORE0.zip] Preconditions: Configurate test in EB tresos use variant name containing lowercase characters. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Lack of some variant name after generation. Expected behavior: Fullfill all variant name after generation. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-98584	Bug	[Mem_Exfls] Duplicated UUIDs tags Detailed description (how to reproduce it): Duplicated UUIDs tags.

ID	Subtype	Headline and Description
		Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2023-11-01-11-28-01-329.png! Expected behavior: Fix duplicate UUID tag Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-98587	Bug	[PWM] Different compared code between EB Tresos and S32CT Detailed description (how to reproduce it): [FlexPwm !image-2023-11-01-11-37-09-333.png! In release K3, there is no user mode for any IP, so in the CT side of driver code, PwmEnableUserModeSupport had been checked by useModePlatformSupport.* Therefore, the define FLEXPWM_IP_ENABLE_USER_MODE_SUPPORT become STD_OFF is corrected, but in the EB side taking only node PwmEnableUserModeSupport So the generated define equal STD_ON is wrong. CT side: !image-2023-11-01-11-42-34-449.png! !image-2023-11-01-11-42-40-588.png! EB side: !image-2023-11-01-11-42-51-628.png! EMIOS !image-2023-11-01-11-43-35-529.png! The different is CT side cannot calculate number of emios channel and wont parse the "0" thing in front of unsigned define {*}U{*}.] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [Pwm_TS_100, Pwm_TS_100_Flexio, Pwm_TS_100_FlexPwm] Observed behavior: [Compare generated EB and CT code] Expected behavior: [No different between EB and CT] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-98593	Bug	[BASE] Gen failed test ECPD on chip K396, K394 Detailed description (how to reproduce it): The error is like the image below when gen test ECPD in der K396, K394 !image-2023-11-01-14-38-01-153.png! Preconditions: gen test ECPD in der K396, K394 Test Case ID (internal TC that caught the defect) optional: Ip_FlexCAN_TS_ECPD_001 Observed behavior: gen failed test Expected behavior:

ID	Subtype	Headline and Description
		gen pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Capitalize the file name like the image below !image-2023-11-01-14-40-47-135.png!
ARTD-98655	Bug	[Port] Including incorrectly header files with derivative S32K376 S32K374 Detailed description (how to reproduce it): Compilation failure on S32K374 S32K376 derivative because of including wrong header file !image-2023-11-01-17-53-00-908.png!!image-2023-11-01-17-53-14-323.png! Preconditions: Compile test on S32K374 S32K376 derivative Test Case ID (internal TC that caught the defect) optional: TS: Port_TS_COT_002 Observed behavior: Compile failed on S32K374 S32K376 derivative Expected behavior: Compile successfully on S32K374 S32K376 derivative Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98686	Bug	[ZIPWIRE] Zipwire_Init failure in HIGH_SPEED_MODE due to slave can not receive ping request after lfast pll enable Detailed description (how to reproduce it): Set master and slave using XOSC/2 = 20mhz Configurable master and slave in HIGH_SEED_MODE, ZipwireLfastFeedbackDivision = 31, ZipwireLfastPllPreDivClk = LFAST_PLL_REF_DIV_2 Issue 1: Zipwire_Init failure in HIGH_SPEED_MODE due to slave can not receive ping request after lfast pll enable due to missing configurable some register (solution update picture 3) Isssue 2: After update isssue 1, pll off slave is enabled too slow, it can not receive ping request from master because clock not stable yet. Master just send ping request one time but it should be update to send ping request many time until receive ping response or timeout. (picture 4) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Zipwire_TC_FCT_0022 Observed behavior: The begin of initialization is alright before enable lfast pll step. Master able to send ping request and slave received it. But after master enable pll and change tx and rx speed and send ping request again, slave can not receive it.(picture 1 and 2) There is not flag in slave's register RIISR[ICPRF]. I still dont know why. All the sequence of initialization are look like in reference manual. Expected behavior: Master and slave Initialize successful Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Issue 1: Picture 3 Issue 2: Picture 4
ARTD-98689	Bug	[mcu] Clock configuration limitation on S32K388 while using EB Tresos Detailed description (how to reproduce it): Customer is trying to do the clock configuration for S32K388 for high performance clock, using EB Tresos, as per the clock configuration table below: !image-2023-11-01-15-59-03-876.png|width=600,height=445! But when customer tries to configure them they are facing limitations with respect to configuring few clocks. The effected clocks are:

ID	Subtype	Headline and Description
		Clock --> Need to configure > Limitation --> Configured > Divider CM7_CORE_CLK > 320 MHz --> 300MHz > 160 MHz --> Divider 7 HSE_CLK > 160MHz > 150 MHz > 64MHz --> Divider 3 AIPS_SLOW_CLK > 40MHz --> 37.5 MHz > 32MHz > Divider 2 AIPS_PLAT_CLK > 80MHz --> 75 MHz > 64MHz > Divider 1 CORE_CLK > 160MHz > 150 MHz --> 106MHz --> Divider 0 The input clock source for Mux 0 is PLL_PH0_CLK. Preconditions: This issue appears using EB Tresos 29.3.0 and RTD SW32K388_RTD_R21-11_4.0.0_CD01_D2309. Observed behavior: EB Tresos shows error messages when trying to configure the previously mentioned clocks, like the following for CM7_CORE_CLK: !image-2023-11-01-16-09-32-317.png|width=305,height=276! Expected behavior: Should be able to configure clocks according to the following table from the Reference Manual: !image-2023-11-01-16-06-36-139.png|width=600,height=445!
ARTD-98692	Bug	[SPI][S32K3] Manual baudrate feature: Update code gen for Lpspi on DS Detailed description (how to reproduce it): S32K3 Update code gen for Lpspi on DS. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-98695	Bug	[icu] Incorrect wakeup configuration Detailed description (how to reproduce it): When IcuWakeupCapability is disabled, IcuWakeup should be removed Preconditions: IcuWakeup should be removed Test Case ID (internal TC that caught the defect) optional: Icu_TS_030 Observed behavior: When import epc into S32DS, code does not generate Issue: When ICU_MODE_WAKEUP measure mode is not selected Wakeup Measurement container must be removed. Expected behavior: Eb configuration ignores this redundant configuration Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98746	Bug	[PWM][FLEXPWM] Cannot enable interrupt for multi channel Detailed description (how to reproduce it): Configure three FlexPwm channels(Channel A, Channel B and Channel X) in the same submodule and select Compare interrupt. Enable PwmNotificationSupported !image-2023-11-02-14-15-33-869.png|width=1046,height=311! !image-2023-11-02-14-15-56-091.png|width=1047,height=343!

ID	Subtype	Headline and Description
		Calling Pwm_EnableNotification for channels .Enable interrupts for channel A(first channel), the value of Compare Interrupt Enables(CMPIE) for channel A is set to 1 . However, after Enable interrupts for channel B(Second channel) ,the value of Compare Interrupt Enables(CMPIE) for channel A is clear . This is wrong. !image-2023-11-02-11-11-47-912.png|width=1071,height=446! When debug, i see that if go through this line code then the value of CMPIE updates, i think this is the problem. !image-2023-11-02-15-22-26-669.png|width=1090,height=489! Preconditions: Enable interrupt at least 2 channels flexpwm simultaneously. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Cannot enable interrupt for multi channel FlexPwm Expected behavior: Can enable interrupt for multi channel FlexPwm Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98762	Bug	[ETH] Fix duplicate UUIDs Detailed description (how to reproduce it): There are some duplicate UUIDs in the xdm file for Eth module on S32K3XX. Please check and fix them. !image-2023-11-02-13-37-18-859.png|thumbnail! Preconditions: Generate plugin and run plugincheck tool Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are some duplicate UUIDs in the xdm file for Eth module on S32K3XX. Expected behavior: No duplicate UUIDs Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-98770	Bug	[S32K3xx_S32M27x_4.0.0] MEM_EXFLS: mismatch in config generate between CT and EB Detailed description (how to reproduce it): !image-2023-11-02-13-55-17-530.png|width=633,height=356! !image-2023-11-02-13-55-38-615.png|width=626,height=352! !image-2023-11-02-13-56-28-549.png|width=628,height=353! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Observed behavior: generate step failed Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-98766	Bug	[Mem_InFls] Cannot run multicore type 3 with two different domain id Detailed description (how to reproduce it): Cannot erase when run multicore type 3 with two different domain id Preconditions: multicore test Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		MemAcc_TS_100 Observed behavior: Cannot erase when run multicore type 3 with two different domain id Expected behavior: Can erase, write when run multicore type 3 with two different domain id Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-98780	Bug	[AE] Fix build fail in CT config Detailed description (how to reproduce it): The raw bit of node AE does not exist so it causes this error. !image-2023-11-02-14-31-28-239.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Build fail on CT Expected behavior: Build pass on CT Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-98831	Bug	[I2S] Build fail when using multicore and disable dev error detect node Detailed description (how to reproduce it): When tester turn off dev error dectect, the driver will build fail. Because u32CoreId is undefined Preconditions: Using multicore and disable dev error detect node Test Case ID (internal TC that caught the defect) optional: I2s_TS_900 Observed behavior: When tester turn off dev error dectect, the driver will build fail. Because u32CoreId is undefined Expected behavior: Driver can use multicore when configuration disable dev error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-98822	Bug	[S32M27x] [Gdu] [S32K3_M27x 4.0.0] Duplicated UUIDs tags Detailed description (how to reproduce it): Duplicated UUIDs tags Preconditions: None Test Case ID (internal TC that caught the defect) optional: Observed behavior: Duplicated UUIDs tags Expected behavior: Non duplicated UUIDs tags Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-98911	Bug	[ETH][S32K3xx] Incorrect computations of timestamping registers Related to ARTD-79904

ID	Subtype	Headline and Description
		Shortly explained: What was wrong: Rounding values resulted in wrong values being stored in registers. Our ptp example was unable to jump and start the fine-tuning due to these approximations. How we fixed it: All constant computations are now done in templates – there are in total three new values computed with maximum possible precision: SSINC register value. SNSINC register value. Multiply ratio for computation of new value for TSAR register. How is our solution better: All three constants were previously handled as non-constant values. Mainly the multiply ratio was previously computed every single time the time correction function was called, resulting in unnecessary computation task. Now this value is being computed just once, in the file generation phase, and then used as a constant. Our solution can handle any frequency-percentage values. The old solution could handle only those that resulted into nice numbers. We used formulas that are using multiplication as much as possible, saving us from several divisions. How we tested it: With 125MHz base clock and 50% (integer result), 25% (periodic result), 20% (integer result), and 10% (float result) percentages being set. Against PTP Grand Master hosted on Linux machine. Please note: We've made changes just to the DS the template since our project doesn't support Tresos yet. Hence, work on Tesos's template is required before merging this patch. Calculations for the init state of registers: float MultiplyRatio = 100.0f / (100.0f – EthPtpTimeCounterMaxAdjustPercentage) = 1.333f float TimeNominalNs= 1000000000 / fTS = 1000000000 / 125000000 = 8.0f uint8 SSINC = (uint8)(TimeNominalNs MultiplyRatio) = 10 = 0xA uint8 SNSINC = (uint8)(((TimeNominalNs MultiplyRatio) – (float)SSINC) 256.0f) = 170 = 0xAA float TimeRequiredINs= (float)SSINC ((float)SNSINC / 256.0) = 10.6640625 float MultiplyRatioCompensation = TimeRequiredINs / TimeNominalNs= 1.3333007813 ADDEND = (uint32)((float)0x100000000LL / MultiplyRatioCompensation) = 32222012096 = 0xC00C00C0 < As you can see it's not approximated 0xC0000000 as before, but it's set more precisely now
ARTD-98920	Bug	[ZIPWIRE] Zipwire read by dma should configurable DataArrayLength > 1 Detailed description (how to reproduce it): In Zipwire read by dma, the fist read request will be trigger by software (picture3). Dma channel (which has responsibility to write into CAR register) will has no job to do due to major loop count = 0 when parameter DataArrayLength = 1 (picture 2). This is a invalid value for BITER bit field in TCD_BITER_ELINKYES register (picture 1). So DataArrayLength should be > 1 in Zipwire read dma transfer. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Zipwire_TC_FCT_0002 Observed behavior: Zipwire read can not operate when DataArrayLength=1 Expected behavior: check DataArrayLength > 1

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-98951	Bug	[AE]Fix limitation when config on both EB and CT Detailed description (how to reproduce it): When config on EB and CT, the error will raised if we don't have ref link in node AePlatformSourceName. !image-2023-11-03-10-13-58-752.png! !image-2023-11-03-10-12-28-162.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The error raised if won't choose source name platform. Expected behavior: No error raised if won't choose source name platform. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-98945	Bug	[S32K3XX][Mem] MemWritePageSize dost not work as in Autosar Spec description Detailed description (how to reproduce it): MemWritePageSize dost not work as in Autosar Spec description => it reduces running performance. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Each write corresponds to this value eg: when user config MemWritePageSize = 8 and want to write 1024 btye => So it takes 1024/8 loops to write all 1024 bytes. Expected behavior: This value is just the smallest unit that the mem can handle Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update again the size of the next chunk of a write job in Mem_Infls_Ipw.c
ARTD-98965	New Feature	[GPT] Update SchM_Check_Gpt files in RTE NewWorkDescription: Run the script from rte repo and add the new SchM_Check_Gpt files in rte Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Run the script from rte repo and add the new SchM_Check_Gpt files in rte
ARTD-98974	Bug	[PORT] Generate failed on S32CT with LQFP176 package and missing enable pin tool with new project Detailed description (how to reproduce it): 2 issues: Generate fail on S32CT with LQFP176 package e.g: S32K376 LQFP176 package !image-2023-11-03-11-17-22-872.png! {_}Pin tool is disabled when creating a new project with S32K374 and S32K376{_}{_}!image-2023-11-03-14-16-57-292.png!{_} Preconditions: Generate with S32CT LQFP176 package. Test Case ID (internal TC that caught the defect) optional: TS: Port_TS_COT_019 Observed behavior:

ID	Subtype	Headline and Description
		Generate failed with LQFP176 package. Pin tool is disabled when creating a new project Expected behavior: Generate successfully with LQFP176 package Pin tool is enabled when creating a new project Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-99025	Bug	[S32K3xx_S32M27x_4.0.0] I2S: Different the syntax name of callback function Detailed description (how to reproduce it): Different the syntax name of callback function between EB and S32DS when using multicore Preconditions: Using multicore to generate file for S32DS and EBT Using FlexIO Test Case ID (internal TC that caught the defect) optional: I2S_TS_900 Observed behavior: !image-2023-11-03-15-21-28-853.png|thumbnail! !image-2023-11-03-15-22-05-854.png|thumbnail! Expected behavior: The same configuration between EB and S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99068	Bug	[ETH][GMAC] Failed to generate file "Gmac_Ip_PBcfg.c". Detailed description (how to reproduce it): Failed to generate file "Gmac_Ip_VS_0_PBcfg.c" when added component ETH_43_GMAC on S32DS. !image-2023-11-03-21-55-17-854.png! Preconditions: Add component Eth_43_GMAC on S32DS Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Failed to generate file "Gmac_Ip_VS_0_PBcfg.c" Expected behavior: No more gen file failed. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-99083	Bug	[S32K3xx_S32M27x_4.0.0] AE: Fail at gen when selecting variant Postbuild Detailed description (how to reproduce it): When selecting variant Postbuild, Tests are failed at gen !image-2023-11-04-17-32-44-840.png! Preconditions: Select variant Postbuild Test Case ID (internal TC that caught the defect) optional: Ae_TC_FCT_0401.c Ae_TC_FCT_0501.c Observed behavior: Failed at gen Expected behavior: no gen errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

ID	Subtype	Headline and Description
ARTD-99086	Bug	[BUILD_ENV][PLATFORM] Ram is not initialized whole for S32K314 S32K324 S32K344 Detailed description (how to reproduce it): Ram is not initialized whole for S32K314 S32K324 S32K344. In RM S32K3xxRM_Rev8_DraftB , these derivative have 160*2 KB. But cmm and linker file only initialize from 0x20400000 to 0x20444000 (mean 272 KB). !image-2023-11-05-18-26-23-899.png|width=943,height=355! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Cmm and linker only define 272 KB ram !image-2023-11-05-18-33-03-557.png|width=700,height=205! !image-2023-11-05-18-35-18-350.png|width=494,height=330! Expected behavior: Initialize 320KB ram for S32K314 S32K324 S32K344 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update size ram in linker files and update Nbytes in cmm to init ram via DMA
ARTD-99156	Bug	[PLATFORM] Missing exclusive area for MPU M7 Detailed description (how to reproduce it): Some registers are Read Modify Write and Write in 3 MPU function as below image. They need to be protected by Exclusive area. !image-2023-11-06-09-48-26-014.png|width=514,height=340! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Didn't have exclusive area for MPU functions Expected behavior: Need to implement exclusive area for 3 above functions. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add exclusive area for 3 MPU functions base on a analysis file is attached
ARTD-99169	Bug	[Pwm] Violate node summary Detailed description (how to reproduce it): In file Pwm.xdm (Ocu_TS_T40D34M40I0R0\config\Pwm.xdm) at line 3204, <a:a name="EDITABLE" value="false"/> *should be name="READONLY" value="true" !image-2023-11-06-10-49-24-101.png! Link station report: [http://bengal.ea.freescale.net/0/project/custom_plugincheck/details] !image-2023-11-06-10-32-37-424.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: No violate node exists. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-99181	Bug	[ADC][S32K3XX] Fix compiler warnings of ADC module Detailed description (how to reproduce it): Fix the compiler warnings of ADC. [^RTD_ADC_Compiler_Warnings.xlsx] Detail see attach file. Preconditions: Driver tag: ADC_491 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: See the description Expected behavior: No warning. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99236	Bug	[S32K3XX_S32M27x_4.0.0][Mem_Eep] Fix import Ecvd Epd fail Detailed description (how to reproduce it): Update Name clock in file Ecvd Epd because node "SdClockReference" change on EB, but not update on DS Note : Import Ecvd Epd fail because: Node "SdClockReference" on xdm EB added "option" but component S32DS not updated. Node "SdClockReference" of component DS has been updated on [ARTD-89498|https://crucible1.sw.nxp.com/action/jira-issue.do?key=ARTD-89498] After update in ARTD-89498, a bug has been found, and fixed in PR in this ticket. Preconditions: Update file epd Test Case ID (internal TC that caught the defect) optional: Mem_Eep_Ecvd_001 Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99282	Bug	[S32K3xx_S32M27x_4.0.0] I2S: Generate missing configuration on S32DS Detailed description (how to reproduce it): When i try to configure multicore on S32DS, i found the configuration is missing Hw configuration array. Because the generate code is checked for partition 0 !image-2023-11-07-10-44-05-790.png|thumbnail! !image-2023-11-07-10-42-29-694.png|thumbnail! !image-2023-11-07-10-44-23-282.png|thumbnail! Preconditions: Using multicore on S32Ds Test Case ID (internal TC that caught the defect) optional: I2S_TS_900 Observed behavior: i found the configuration is missing Hw configuration array. Expected behavior: Generate all Hw configuration array. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-99288	New Feature	[memexfls] [IMPLEMENTATION] Update code to support multicore Type 3 for MEMACC Driver part 2 NewWorkDescription: Move all global variable to Share no cache region only when multicore type3 is enabled. Add check core ID for each job. Only the core that requests the job can perform the job in the mainfunction Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Reference the way to implement the multicore "Type 3" on the FLS Driver (AUTOSAR 4.4) Document: NXP_RealTimeDrivers_Multicore.pptx; Autosar Memstack Multicore.pptx
ARTD-99294	Bug	[Spi][S32K3XX] Spi Compiler warnings Detailed description (how to reproduce it): Compiler warnings on Spi drivers, see in attachment file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: See in attachment file. Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99353	Bug	[dio] Solve code review/ design review findings Detailed description (how to reproduce it): [solve findings for [ARTD-89386] [dio] Perform code review/ design review against checklists NXP JIRA] Preconditions: [None] Test Case ID (internal TC that caught the defect) optional: [None] Observed behavior: [found misalignments of code from guidelines during code review] Expected behavior: [no code findings] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [fix code findings]
ARTD-99356	Bug	[S32K3xx_S32M27x_4.0.0] AE: There are some violations in Plugincheck report Detailed description (how to reproduce it): The violations: <a:a name="EDITABLE" value="false"/> *should be name="READONLY" value="true"*|Ae.xdm:833 <a:a name="EDITABLE" value="false"/> *should be name="READONLY" value="true"*|Ae.xdm:971 Duplicated UUID tags: ECUC:52076fb3-014e-423c-bf0f-11111ec2c8cb|Ae.xdm:773 Ae.xdm:1094 ECUC:ba826417-4632-45aa-a826-557856ffcce2|Ae.xdm:917 Ae.xdm:1077 Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: there are some violations Expected behavior: No violations in Plugincheck report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional:
ARTD-99359	New Feature	[ZIPWIRE] Implement Errata ERR051988 NewWorkDescription: During the LVDS Fast Asynchronous Serial Transmission (LFAST) startup procedure when LVDS Receiver pad (Rx) is enabled and the common voltage is not yet settled on the receiver line the LVDS pad fault status is latched in the Read-Only GPR On Functional Reset 7 register (DCM_GPR.DCMROD7[LVDS_3P3V_RX_FAULT] = 1). This fault cannot be cleared until the common voltage for LVDS pad is settled on the line connected to Rx pad. If the fault is not cleared and the LFAST startup procedure continues without getting the flag cleared the communication between the Master and Slave might not be established correctly at the high speed. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: In this case, the recommended LFAST startup procedure cannot be followed entirely. The Tx pad on the Slave node should be enabled by software before the Rx pad is enabled instead of being enabled from Master using ICLC frame with payload 0x31. Also, make sure LVDS receiver pad fault is cleared after enabling Rx pads on both LFAST Master and Slave node before continuing in the LFAST startup procedure. Do-while loop can be utilized for checking and clearing the fault.
ARTD-99502	New Feature	[memacc]Multicore Type 3 for MEMACC Driver follow-up NewWorkDescription: Implement the multicore "Type 3" for the MEMACC Driver Follow up items: Check if there are any conflict hardware resource. Update dev test will internal flash. Check again memory allocation section for globle varriable. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Reference the way to implement the multicore "Type 3" on the FLS Driver (AUTOSAR 4.4) Document: NXP_RealTimeDrivers_Multicore.pptx; Autosar Memstack Multicore.pptx
ARTD-99565	Bug	[ICU]Fix some warning and error for Example Detailed description (how to reproduce it): Warning when import project example in all example K3XX in S32CT: !image-2023-11-08-11-09-19-898.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: All example S32CT Observed behavior: Warning old version Expected behavior: Not exits warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update file .mex to version update 8
ARTD-99568	Bug	[Mem_InFls] Can not load code to ram on GCC Detailed description (how to reproduce it): Missing include Osif.h in Mem_43_INFLS_IPW.h and wrong section name .acmem_43_infls_code_rom in C40_Ip_Ac.h Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_InFls_TC_FCT_0010 Observed behavior: !image-2023-11-08-11-42-07-440.png! !image-2023-11-08-11-41-57-021.png! Expected behavior: Load to RAM successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		[....]
ARTD-99576	Bug	[ETH][GMAC] Fix compiler warning for ETH module Detailed description (how to reproduce it): Driver code have warning. See attached file for detailed information. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: No compiler warning. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99596	Bug	[AE] Missing a function need to add when transfer SPI. Detailed description (how to reproduce it): Because SPI is updated a function byte swap so it can be affected by the communication process ! image-2023-11-08-15-09-45-839.png! 2.And this node not supported anymore, it need to be removed. !image-2023-11-08-15-38-25-903.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing function update byte swap. Expected behavior: Added a function update byte swap. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-99749	Bug	[S32K3xx_S32M27x_4.0.0] I2S: Divider Value on S32DS is wrong value for IP layer Detailed description (how to reproduce it): The value of divider is wrong after generating on S32DS for IP layer. According the formula to calculate for divider, I have configurated FlexioClock is 80Mhz Baudrate is 50000. The divider should be 255 but the Actual divider is 1 Preconditions: Using IPV Flexio for s32ds Configuring IP layer Master Mode Test Case ID (internal TC that caught the defect) optional: Ip_Flexio_I2s_TS_100 Observed behavior: Divider Value on S32DS is wrong value for Ip layer !image-2023-11-08-16-03-09-887.png|thumbnail! !image-2023-11-08-16-03-31-421.png|thumbnail! !image-2023-11-08-16-03-49-736.png|thumbnail! Expected behavior: Divider Value on S32DS is true when configuring Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99794	Bug	[ETH][GMAC] Unable to configure EthPtpTimeCounterMaxAdjustPercentage node on S32DS Detailed description (how to reproduce it): Unable to configure EthPtpTimeCounterMaxAdjustPercentage node on S32DS and error log: !image-2023-11-09-09-31-05-979.png! Preconditions: Add component Eth_43_GMAC on S32DS

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Unable to configure EthPtpTimeCounterMaxAdjustPercentage node Expected behavior: EthPtpTimeCounterMaxAdjustPercentage node can be configured Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99797	Bug	[PLATFORM] Optimize generation code Detailed description (how to reproduce it): Code generation should NOT use specific derivative macro. Code should be generated depend to derivative is selected from resource. !image-2023-11-09-09-47-46-574.png|width=521,height=520! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: generation code use specific derivative macro. Expected behavior: generation code don't use specific derivative macro, generate code depend to selection derivative Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update generation code to remove redundant code and don't use derivative macro.
ARTD-99819	Bug	[Mem_InFls] RuntimeInfo variable must be separated for each core when using multicore type 1 Detailed description (how to reproduce it): Mem_43_INFLS_eJobRuntimeInfo is pushed in share memory section. It leads to all core access to the same variable. > multicore type 1 works incorectly. Preconditions: Enable multicore type 1 on MemAcc Test Case ID (internal TC that caught the defect) optional: Test multicore of MemAcc Observed behavior: run fail Expected behavior: run pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: global variable only allocated to share memory only when multicore type 3 enable
ARTD-99824	Bug	[PORT] [S32K3XX_S32M27X] Compilation error with lqfp176 package on EBT Detailed description (how to reproduce it): Compilation error with lqfp176 package on EBT S32K374 S32K376 {*}{*}It seems Port_SIUL2_0_aInMuxSettings array is not generated correctlly in Port_Cfg.c file !image-2023-11-09-11-14-01-113.png! It causes compilation error !image-2023-11-09-11-17-48-496.png! Preconditions: Compile with lqfp176 package on EBT S32K374 S32K376 Test Case ID (internal TC that caught the defect) optional: Port_TS_COT_002 Observed behavior: Compilation error with lqfp176 package on EBT S32K374 S32K376 Expected behavior: Compilation success with lqfp176 package on EBT S32K374 S32K376

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-99830	Bug	[ETH][Tresos] Update resource for ETH on S32K338 and S32K348 Detailed description (how to reproduce it): There is an issue in the resource file for Eth on S32K38 and S32K348. It makes the tests failed at generation step with EB Tresos. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Eth_TS_M01 Observed behavior: The test suite failed at generation step with EB Tresos Expected behavior: No error for the test. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-99836	Bug	[WDG] Fast mode and slow mode can be selected without the same clock on DS Detailed description (how to reproduce it): Fast mode and slow mode can be selected without the same clock !image-2023-11-09-14-54-19-738.png|width=777,height=541! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Fast mode and slow mode can be selected without the same clock Expected behavior: Fast mode and slow mode must have the same clock on DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-99845	Bug	[Mem_Eep] RuntimeInfo variable must be separated for each core when using multicore type 1 Detailed description (how to reproduce it): Mem_43_EEP_eJobRuntimeInfo is pushed in share memory section. It leads to all core access to the same variable. > multicore type 1 works incorectly. Preconditions: Enable multicore type 1 on MemAcc Test Case ID (internal TC that caught the defect) optional: Test multicore of MemAcc Observed behavior: run fail Expected behavior: run pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: global variable only allocated to share memory only when multicore type 3 enable
ARTD-99878	Bug	[ICU]Some inconsistencies between the functions in the ReqExport.txt file and the.h files of the driver code Detailed description (how to reproduce it): There are some functions that have differences between the functions in the ReqExport.txt file and the driver code.h file described in the attached file below. void Emios_Icu_Ip_StartTimestamp(uint8 instance, uint8 hwchannel, uint16 bufferPtr, uint16 bufferSize, uint16 notifyInterval) uint16 Emios_Icu_Ip_GetTimeElapsed (uint8 instance, uint8 hwchannel) uint16 Emios_Icu_Ip_GetEdgeNumbers (uint8 instance, uint8 hwchannel) Preconditions: NA Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Some inconsistencies between the functions in the ReqExport.txt file and the.h files of the driver code
ARTD-99894	Bug	[PWM][FlexPWM]Calling Pwm_SetChannelDeadTime function fails with config is mixed Emios and FlexPwm Detailed description (how to reproduce it): When call Pwm_SetChannelDeadTime function with config is mixed Emios and FlexPwm. Then in the Pwm_Ipw_ValidateParamDeadTime function, the macro PWM_EMIOS_USED == STD_ON. That causes the channel configured as FlexPWM to jump into it to handle the Emios_Pwm_Ip_GetPeriod function. !image-2023-11-10-09-00-23-850.png|width=527,height=122! When call Pwm_SetChannelDeadTime function with config is FlexPwm and Deadtime value but the deadtime value is written to the register using Deadtime/2 deadtime value expect = 2000 !image-2023-11-13-11-08-35-904.png! deadtime value is written to the register =1000 !image-2023-11-13-11-04-13-366.png! Preconditions: mixed Emios and FlexPwm. Call Pwm_SetChannelDeadTime function with channel is FlexPwm Test Case ID (internal TC that caught the defect) optional: Pwm_TS_123 Observed behavior: Config is mixed Emios and FlexPwm Call Pwm_SetChannelDeadTime function fails with channel is FlexPwm Expected behavior: Call Pwm_SetChannelDeadTime function fails with channel is FlexPwm not fail Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-99928	Bug	[S32K3xx_S32M27x_4.0.0] LPSPI Errata ERR050456 is not in documentation except for k3x4 Detailed description (how to reproduce it): Create two asynchronous transmits in one SpiPhyUnit on Slave mode. In the first sequence, using Master MAF to create redundant Spi bus transfer to set RDF flag after first sequence ended. In the second sequence, we saw that: RDF can not be cleared right after driver reset Rx FIFO and clear all flags. It may be the errata mentioned in [^S32K3x4 0P55A_1P55A Errata Rev13_Jun_2023.pdf] , but it is not mentioned in other devices 'errata documents in SOW file of S32K3XX_S32M27x_400_RTM release. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Spi_TC_FCT_1026 Spi_TS_105 CFG_SET: LPSPI_CPOL_CPHA_2_64BIT_ERR_E050456_$(GENERATOR) Observed behavior: Before resetting FIFO and clearing flags: !image-2023-11-10-14-11-11-264.png! After resetting and clearing flags: !image-2023-11-10-14-11-43-847.png! Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-99964	Bug	[WDG] Disable WdgClockReferencePoint container from EB and DS interface for AeWdog instance Detailed description (how to reproduce it): The container WdgClockReferencePoint is not used for AeWdog instance. It should be disabled from CT and EB interface Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: WdgClockReferencePoint can be set but it is not used in any code generate file. Expected behavior: WdgClockReferencePoint is disabled Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-100005	Bug	[S32K3XX_S32M27X] PORT: Incorrect "Mscr Pdac Slot" generation when adding Rm module on S32DS Detailed description (how to reproduce it): Generate "Mscr Pdac Slot" incorrect when adding Rm module on S32DS Create project on S32DS Add module Port, Rm and enable Virtual wrapper PORT config MSCR159 RM: config MscrNumber 159 with Mirror = VIRTWRAPPER_PDAC4 When update code: "Mscr Pdac Slot" gen incorrect Preconditions: All Derivative TAG test_port: PVT_TEST_PORT_RTD_K3M27_400_052 Test Case ID (internal TC that caught the defect) optional: Port_TS_009 CFG = 2 Observed behavior: for example: Configuration MSCR159 "Mscr Pdac Slot" gen incorrect.. Config Mirror = VIRTWRAPPER_PDAC4, but gen Mscr Pdac Slot = 0 !image-2023-11-12-21-06-39-135.png|thumbnail! Expected behavior: Generate code match the configuration Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In function GetMscrPDAC(PortPin); !image-2023-11-12-21-27-28-186.png|thumbnail!
ARTD-100011	Bug	[PLATFORM][S32K3xx_S32M27x_4.0.0] CCOV build code error Detailed description (how to reproduce it): Platform_TS_COV_001 fail when build with tag PVT_PLATFORM_S32K3XX_S32M27X_400_031 Error log !image-2023-11-13-08-44-18-637.png|width=725,height=110! Check in code build, it notify error at line 95986 !image-2023-11-13-08-46-29-047.png|width=720,height=140! in file inszt_Platform.c, i check i see that code build was miss a line (in attachment) #if ! defined (S32K39_MC_RGM_H)_* at line 69371 !image-2023-11-13-08-47-52-586.png|width=720,height=144! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Platform_TS_COV_001 Observed behavior: Expected behavior:

ID	Subtype	Headline and Description
		It build have line code #if ! defined (S32K39_MC_RGM_H)* _{_}in line 69371{_} Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add barrier in code gen IntCtrl_Ip_CfgDefines.h !image-2023-11-13-08-51-01-979.png|width=707,height=160!
ARTD-100093	Bug	[S32K3XX_S32M27X] PORT: Incorrect "Imcr Pdac Slot" generation when Enable virtual Wrapper Detailed description (how to reproduce it): Incorrect "Imcr Pdac Slot" in Port_aSIUL2_0_ImcrInitConfig when enable virtual wrapper. Create project Add module Port and enable Virtual Wrapper for example: Configuration MSCR28 !image-2023-11-13-15-41-14-538.png|thumbnail! Preconditions: Derivative S32K358 TAG: PVT_TEST_PORT_RTD_K3M27_400_059 Test Case ID (internal TC that caught the defect) optional: Port_TS_009 CFG = 1 Observed behavior: for example: Configuration MSCR28, IMCR432 with VIRTUAL_WRAPPER_PDAC1, but when generation: Port_aSIUL2_0_ImcrInitConfig_VS_0 gen Incorrect "ImcrPdacSlot" Expected behavior: Generate code match the configuration Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Derivative S32K358 need to update $cINMUX match to $cPdacSlot !image-2023-11-13-15-56-08-782.png|thumbnail!
ARTD-100103	Bug	[S32K3xx_S32M27x_4.0.0] FEE: Compare code gen tresos and s32ct Detailed description (how to reproduce it): Not mactch code gen between eb and ct File: Fee_cfg.h, fee_cfg.c !image-2023-11-13-17-08-25-937.png! Preconditions: !image-2023-11-13-17-09-44-882.png!!image-2023-11-13-17-09-17-215.png! Test Case ID (internal TC that caught the defect) optional: [ar_go_compare_code_gen_fee_ci] Observed behavior: [Test fail] Expected behavior: [Test pass] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100113	Bug	[S32K3xx_S32M27x_4.0.0] AE: there are build errors in CCOV tests Detailed description (how to reproduce it): There are build errors in CCOV tests: ERROR FOUND DURING MACRO EXPANSION WHILE PROCESSING SOURCE LINE 97326 VALUE OF VARIABLE IS NOT DEFINED UNDEFINED VARIABLE IS AEC_IP_NMI_S32M24_INTERRUPT Aec_Ip_Hw_Access_5.cerr Preconditions: CCOV_EN = ON Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Build errors Expected behavior:

ID	Subtype	Headline and Description
		No build errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100180	Bug	[Mem_Eep] Node "u32McuClockInfo" reference clock uSDHC from Mcu on component S32DS incorrectly Detailed description (how to reproduce it): Node "u32McuClockInfo" reference clock uSDHC from Mcu on component S32DS incorrectly. It always refers to the first element of the list McuClockReferencePointFrequency, which may not be uSDHC clock. <info id="u32McuClockInfo" label="Sd Clock Frequency Information" available="true" value="system::getChildrenByASPath(`/AUTOSAR/EcucDefs/Mcu/McuModuleConfiguration/McuClockSettingConfig/McuClockReferencePoint`).get(0).getSetting(`McuClockReferencePointFrequency`).getValue().toInt()"> <description>Sd clock frequency from MCU.</description> </info> Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Node "u32McuClockInfo" reference clock uSDHC from Mcu on component S32DS incorrectly. Expected behavior: Correct node "u32McuClockInfo" reference clock uSDHC from Mcu on component S32DS. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-100156	Bug	[S32K3xx_S32M27x_4.0.0] I2S: Can not edit node for sai_data_line Detailed description (how to reproduce it): When Sai Instance is 0, We can not edit the node for sai data line 1 2 3 !image-2023-11-14-09-21-06-177.png|thumbnail! !image-2023-11-14-09-21-23-776.png|thumbnail! Preconditions: Using EBT SAI Sai instance ID is 0 Test Case ID (internal TC that caught the defect) optional: I2S_TS_130 Observed behavior: When Sai Instance is 0, We can not edit the node for sai data line 1 2 3 Expected behavior: We can edit the node for sai data line 1 2 3 for instance 0 because acording to Reference manual SAI0 suppport 4 channel and SAI1 just support for 1 channel. Please check Reference manual before fixing. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100192	Bug	[S32K3xx_S32M27x_4.0.0] MEMACC: Multicore Type1 unable access Rm_SemaphoreLockGate Detailed description (how to reproduce it): Multicore Type1 unable access function Rm_SemaphoreLockGate(); Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Fee_TS_192 Observed behavior: test fail Expected behavior: test pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: static Std_ReturnType MemAcc_MCoreInitSema4sLock(void);

ID	Subtype	Headline and Description
		!image-2023-11-14-11-06-15-019.png!
ARTD-100206	Bug	[LINTRCV] Wakeup flag should be checked when init driver Detailed description (how to reproduce it): Wakeup flag should be check when init driver to avoid affect from previous test, because AE can receiver wake up event when MCU is power off. So driver of LinTrcv need to check this event raised or not, if it happen, we will call to EcuM function to inform. as mention of req as below: !image-2023-11-14-13-41-38-293.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Wakeup flag will be check Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Wakeup flag will be check
ARTD-100239	Bug	[Mem_InFls] Build fail C40_IP test on IAR Detailed description (how to reproduce it): build C40_Ip test on IAR Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: IP_C40_TC_0001 Observed behavior: !image-2023-11-14-16-20-32-721.png! !image-2023-11-14-16-15-34-392.png! Expected behavior: Build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100242	Bug	[S32K3xx_S32M27x_4.0.0][S32K396][IGF] The generated code is different between EB and CT Detailed description (how to reproduce it): Create new project on EB tresos, generate code import epc from EB to CT, generate code compare generate code EB and CT xdm and epc file attached below Preconditions: n/a Test Case ID (internal TC that caught the defect) optional: Port_TS_004 Observed behavior: the generated code is different between EB and CT !image-2023-11-14-16-32-22-331.png|width=1118,height=233! IGF channel 3: FGEN bit enable on EB and disable on CT (MSCR195) IGF channel 0: can't config on CT (MSCR143) Expected behavior: the generated code is the same between eb and ct, the generated value is correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100263	Bug	[I2C] S32K3 fix EB and DS config after MCU update Detailed description (how to reproduce it): MCU was updated and affects I2c config

ID	Subtype	Headline and Description
		Preconditions: Test Case ID (internal TC that caught the defect) optional: All Observed behavior: Project generate fails Expected behavior: I2c build and devtest pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update I2c config based on new MCU
ARTD-100329	Bug	[S32K3xx_S32M27x_4.0.0] MEM_EXFLS: fix discrepancies in generated config between CT and EB Detailed description (how to reproduce it): there is a discrepancy between EB and CT !image-2023-11-15-10-50-04-594.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_ExFls_TS_COT_001 Observed behavior: test failed Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-100332	Bug	[S32K3xx_S32M27x_4.0.0] [MEMACC] Generate fail in S32ds while disable Multicore type 1 support Detailed description (how to reproduce it): Generate fail in S32ds while disable Multicore type 1 support Preconditions: disable Multicore type 1 support Test Case ID (internal TC that caught the defect) optional: MemAcc for CT testcase Observed behavior: Generate fail Expected behavior: Generate success Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100338	Bug	[S32K3XX_S32M27X] PORT: Incorrect "Imcr Pdac Slot" generation when add RM module Detailed description (how to reproduce it): Incorrect "Imcr Pdac Slot" generation when add RM module Missing support PDAC4, PDAC5 when gen Port_aSIUL2_0_ImcrInitConfig !screenshot-1.png|thumbnail! Preconditions: Derivative S32K396 S32K388 Tag Test_Port: PVT_TEST_PORT_RTD_K3M27_400_068 Test Case ID (internal TC that caught the defect) optional: Port_TS_009 CFG=2 Observed behavior: Expected behavior: Generate code match the configuration

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update template code gen CT: Port_aSIUL2_0_ImcrInitConfig need to update !image-2023-11-15-10-54-52-861.png|thumbnail!
ARTD-100421	Bug	[Mem_InFls] mismatch code gen config Detailed description (how to reproduce it): when disable UTEST MODE in EB tresos config, code generated in S32DS will enable: in file C40_IP_Cfg.h !screenshot-1.png|thumbnail! in file Mem_43_INFLS_CfgDefines.h: !screenshot-2.png|thumbnail! in file Mem_43_INFLS_Cfg.h: !screenshot-3.png|thumbnail! in file Mem_43_INFLS_Cfg.c !screenshot-4.png|thumbnail! when enable UTEST MODE in EB tresos config, code generated in S32DS has some mismatch: in file C40_Ip_Cfg.h: !screenshot-8.png|thumbnail! in file Mem_43_INFLS_Cfg.c: !screenshot-6.png|thumbnail! !screenshot-7.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mem_Infls_TS_008 Mem_Infls_TS_001 Observed behavior: mismatch generated file between EB and CT Expected behavior: Match all generated file between EB and CT Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100424	Bug	[S32K3XX_S32M27x_4.0.0][MemAcc] Fix error when compare ECVD and EPC Detailed description (how to reproduce it): Have some differences when comparing ECVD and EPC. !image-2023-11-15-15-40-58-523.png|width=835,height=374! Preconditions: ECVD and EPC file Test Case ID (internal TC that caught the defect) optional: Memacc_TS_001 Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100545	New Feature	[mem_exfls] Update copyright template NewWorkDescription: Replace : “(c) Copyright \{year range} NXP Semiconductors All Rights Reserved.” with : Copyright \{year range} NXP !screenshot-2.png! to !screenshot-3.png! Requirement source: as described in “Updating Copyright Years” topic on this guide [https://confluence.sw.nxp.com/display/OSS/File+Headers+-+Copyright+and+License+Information]). (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)

ID	Subtype	Headline and Description
		Proposed solution optional: as above
ARTD-100564	New Feature	[BASE] Add define for Zipwire's Errata NewWorkDescription: A define ERR_IPV_ZIPWIRE_E0519988 needs to be defined in Soc_Ips.h file Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add ERR_IPV_ZIPWIRE_E0519988 in Soc_Ips.h file
ARTD-100589	New Feature	[mem_infls] Update copyright template NewWorkDescription: Replace : “(c) Copyright \{year range} NXP Semiconductors All Rights Reserved.” with : Copyright \{year range} NXP !screenshot-2.png! to !screenshot-3.png! Requirement source: as described in “Updating Copyright Years” topic on this guide [https://confluence.sw.nxp.com/display/OSS/File+Headers+-+Copyright+and+License+Information]). (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: as above
ARTD-100594	Bug	[MCU][S32k3XX] build fail in Eb and CT Detailed description (how to reproduce it): build fail when build S32k3x8 !image-2023-11-15-20-26-11-925.png|thumbnail! Preconditions: PVT_MCU_S32K3XX_S32M27X_400_007 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: build fail in Power_Ip_PMC.c when build S32K328 Expected behavior: build pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add macro related PMC_LVSC
ARTD-100598	Bug	Wrong MPU configuration in RTD 3.0.0 P07 S32K314 projects Detailed description (how to reproduce it): [The MPU descriptor for S32K314 PFlash is not configured in system.c When MPU is enabled (default), a fault exception rises] Missing S32K314 macro: !image-2023-11-15-14-34-19-280.png|thumbnail! Preconditions: [Create a new project in S32DS IDE 3.5 with RTD 3.0.0 P07. When the project is run on WH, it should end up in DefaultISR, Hard Fault vector.] Test Case ID (internal TC that caught the defect) optional: [0575123] Observed behavior: [Memory Fault exception due to MPU invalid access] Expected behavior: [MPU descriptor must be configured on the Pflash blocks, provided MPU gets enabled] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Define S32K314 macro
ARTD-100646	Bug	[Mem_Eep] error VSMD

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): error VSMD Rule A207: Default value of parameter 'Mem/SdCfg/u32McuClock' is out of range. !image-2023-11-16-14-34-32-923.png|width=778,height=90! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: error VSMD Expected behavior: fix error VSMD rule A207: Default value of parameter 'Mem/SdCfg/u32McuClock' is out of range. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-100677	Bug	[Mcu] [S32K396] QuadSPI_SFCK/QSPI_2XSFIF descibes in S32CT is not correct Detailed description (how to reproduce it): Configure Clock for S32K396 in S32CT: !image-2023-11-16-16-40-17-509.png! QSPI_2XSFIF_CLK: 12MHz QSPI_SFCK_CLK: 6Mhz Check in Peripherals tool, Mcu module: !image-2023-11-16-16-41-50-801.png! The value showing in McuCgm0ClockMux10 is 6Mhz (QuadSPI_SFCK), but byright it should shows 12Mhz (QSPI_2XSFIF) as describtion as this is S32K396 derivative Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The value showing in McuCgm0ClockMux10 is 6Mhz (QuadSPI_SFCK) Expected behavior: It should shows 12Mhz (QSPI_2XSFIF) as describtion as this is S32K396 derivative Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-100686	Bug	[ADC] Adc_ReadGroup function is working incorrectly on DMA without interrupt mode. Detailed description (how to reproduce it): Setup a conversion with the configuration as bellow: ADC instance0 : Channel 0: Vin = 1V channel 4: Vin = 2V Transfer Type: ADC_DMA Group Without interrupt: TRUE Result buffer is placed in non-cache section After start group conversion, polling the Adc_ReadGroup function until it returns E_OK to get the result data but CH0 output result = CH4 output result = 2V The issue happens with all compilers Preconditions: ADC driver tag: ADC_509 Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0110 Observed behavior: See the description. Expected behavior: Driver works correctly: CH0 output result = 1V and CH4 output result = 2V.

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-100769	Bug	[PORT][S32CT] Generate failed on S32K396 Peripheral ZIPWIRE0 Detailed description (how to reproduce it): Generate fail on S32CT with S32K396 derivative !MicrosoftTeams-image (18).png|thumbnail! !MicrosoftTeams-image (19).png|thumbnail! !MicrosoftTeams-image (20).png|thumbnail! Preconditions: Generate with S32CT S32K396 signal lfast_0_ext_ref, peripheral ZIPWIRE0 Test Case ID (internal TC that caught the defect) optional: TS: Port_TS_COT_019 Observed behavior: Generate fail on S32CT with S32K396 derivative Expected behavior: Generate successfullylon S32CT with S32K396 derivative Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-100797	Bug	[Gpt] Example issue Detailed description (how to reproduce it): DS example: Configurations are created by an older version of tool. Lowercase in package name (for Gpt_Example_S32K396, {_}Rtc_Gpt_Ip_Example_S32K396{_}). Configuration has errors in module: Mcu ({_}Gpt_Example_S32K396,{_} Gpt_Example_S32K344, Gpt_Example_S32K358, {_}Gpt_Example_S32K388{_}) Port EB example (for example K344, K358 and K388): Incorrect information in readme file about pin and board. Run fail because of platform's configuration ({_}Gpt_Example_S32K396{_}) Generate fail ({_}G{_}{_}pt_Example_S32K358).{_} Note: See attached file below for detail information [^testexample.docx] Preconditions: {*}{*}DS example: # Open S32DS. # Importing the S32 Design Studio project # Generating the S32 configuration # Compiling the application # Running the application on the board EB example: # Make sure that all RTD plugins are already installed in the Tresos Studio plugins directory. # Open Tresos Studio. # Import example application project. # Building the example application Expected behavior: Examples run normally without error or warning. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-100816	Bug	[ADC] Cannot reset DSPSS thread's output buffer address when starting new group conversion Detailed description (how to reproduce it): When starting a new Group in the same SDADC unit, the new output data were not written from the start address (which is 0). They were written from the old position of previous Group (see the attachment). Preconditions: NA Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Adc_TS_SDADC with AdcGroup_StreamLinearDmaDspss Observed behavior: See the description. Expected behavior: The output data must be written from the start address of thread output buffer Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-100842	Bug	[ADC] Missing check for wrap event in function DSPSS_CoreBufferRead Detailed description (how to reproduce it): Setup a group conversion with the setting SDADC enable DSPSS feature, Sw triggering, linear streaming buffer, number of sample: 50 DSPSS configuration: !image-2023-11-17-15-40-22-062.png|width=477,height=198! After stream completed, missing data in result buffer: !image-2023-11-17-15-45-18-731.png! Preconditions: ADC driver tag: ADC_513 Test Case ID (internal TC that caught the defect) optional: Adc_TS_DSPSS_001 Observed behavior: Missing data in result buffer Expected behavior: Data recorded fully. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-100873	Bug	[S32K3xx_S32M27x_4.0.0] PORT: Build fail with package hdqfp172 on K348 Detailed description (how to reproduce it): Build fail because PORT_SIUL2_0_INOUT_TABLE_NUM_ENTRIES_U16' undeclared in PortCfg.h file !image-2023-11-17-17-28-49-856.png! Preconditions: K348, package 172 Test Case ID (internal TC that caught the defect) optional: Port_TS_COT_002 Observed behavior: Build fail Expected behavior: Build pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-100916	Bug	[ADC] DSPSS thread cannot enable in hardware trigger mode. Detailed description (how to reproduce it): Convert a conversion with setting: SDADC0 instance and enable DSPSS feature. Trigger source: hardware trigger A continuous conversion, single buffer After the trigger asserted, the DSPSS thread still disable and output buffer equal to 0. Preconditions: ADC driver tag: ADC_514 Test Case ID (internal TC that caught the defect) optional: Adc_TC_DSPSS_0020 Observed behavior: DSPSS thread disable

ID	Subtype	Headline and Description
		Expected behavior: DSPSS thread disable and output buffer as expectation. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-101195	New Feature	[Zipwire] Wrong supported derivatives in UM/IM NewWorkDescription: The Zipwire module is only available on S32K39x and S32K37x derivatives. The remaining ones need to be removed from the "Supported Derivatives" chapter. !image-2023-11-20-10-41-40-813.png|thumbnail! Requirement source: N/A Proposed solution optional: Keep only S32K39x and S32K37x derivatives for zipwire module in the "Supported Derivatives" chapter.
ARTD-101216	Bug	[ADC] DSPSS threads not working because firmware is overwritten by other core Detailed description (how to reproduce it): Setting 2 conversions in multicore Core 0: Use SDADC_0, DSPSS thread 0 Core 2: Use SDADC_1, DSPSS thread 1 When invoke Adc_Init function on core 2, driver loads the FW init PMEM and default configuration into XMEM again making the conversion failed on core 0. Preconditions: ADC driver: ADC_514 Test Case ID (internal TC that caught the defect) optional: Adc_TC_DSPSS_0011 Observed behavior: See the description, test suite failed. Expected behavior: Test suite passed. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-101246	New Feature	[CRYPTO_NG] Remove not supported APIs to improve CE index NewWorkDescription: These functions above are not supported in S32K3XX 4.0.0 platform but still generated in plug-in. It leads to CE index in Code Coverage report is 0%. There is a request not to generate this API to improve CE index in this platform Mu_Ip_Mu2_OredRx_Isr Mu_Ip_Mu2_OredGP_Isr Mu_Ip_Mu3_OredRx_Isr Mu_Ip_Mu3_OredGP_Isr Mu_Ip_Mu4_OredRx_Isr Mu_Ip_Mu4_OredGP_Isr Mu_Ip_Mu5_OredRx_Isr Mu_Ip_Mu5_OredGP_Isr Mu_Ip_Mu6_OredRx_Isr Mu_Ip_Mu6_OredGP_Isr Mu_Ip_Mu7_OredRx_Isr Mu_Ip_Mu7_OredGP_Isr In source file Mu_Ip_Irq.c Requirement source: Follow new approach to improve CE index. Proposed solution optional: NA
ARTD-101658	Bug	[Doc:FEE_UM]: The description of the ECC related will mislead customer In the RTD_FEE_UM.pdf, there is a description of the ECC, it will mislead customer. !image-2023-11-23-15-22-02-382.png! here customer think that he must configure the page size to 32 Bytes. !image-2023-11-23-15-22-39-707.png! But in fact, for S32K3, configure to 8Bytes is OK, and 8Bytes will same many spaces for user, at the same time, It will increase the lifespan of the flash.

ID	Subtype	Headline and Description
ARTD-101957	Bug	[SPI][S32K3xx_S32M27x_4.0.0] The example description is incorrect Detailed description (how to reproduce it): Example desciption is incorrect in test Lpspi_Ip_HalfDuplexTransfer_S32K396 !image-2023-11-27-15-15-20-941.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Example description must to correct. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to update the description.
ARTD-59652	New Feature	[I2S] Merge Slave and Master LLD APIs NewWorkDescription: Develop Slave Flexio I2s Requirement source: FLEXIO_I2S_IP_016_001 FLEXIO_I2S_IP_015_001 FLEXIO_I2S_IP_013_001 FLEXIO_I2S_IP_011_001 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution - optional: NA

4.6 Change List for 3.0.0

ID	Subtype	Headline and Description
ARTD-25946	Bug	[FEE] Warnings of zero-initialized variables with complier IAR Detailed description (how to reproduce it): When building Fee driver with IAR compiler, there are some warnings appear, because of zero-initialized variables still have explicit zero-initializers Root cause: there was an incorrect fixing for{color}{color:#172b4d} compiler warning, it did not follow the rule of zero-initialized variables in "CLEARED" memory sections [https://bitbucket.sw.nxp.com/projects/ARTD/repos/fee/pull-requests/117/diff#generic/src/Fee.c] Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There are compiler warning on IAR Expected behavior: There are no warnings Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove all explicit zero-initializers in the "CLEARED" memory sections. Following the guidline in the ticket: https://jira.sw.nxp.com/browse/ARTD-12239
ARTD-54375	Bug	[FEE] - UM Memory dump example has incorrect information Detailed description (how to reproduce it): In User Manual document, section 3.6.2 Memory Dump Example:

ID	Subtype	Headline and Description
		One group of two clusters is configured: # The first cluster has start address 0x10000. # The second cluster has start address 0x18000. !image-2023-02-03-13-16-09-282.png|width=767,height=295! However, the size of first cluster is 0x10000. It will overlap in the memory of the second clusters. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Start address of 2nd cluster in this example is not correct, will leads to the confusion for customer . It should be change to 0x20000 Expected behavior: Start address of 2nd cluster in this example is not correct, will leads to the confusion for customer . It should be change to 0x20000 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-55453	Bug	[fls] [GENERAL] PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Detailed description (how to reproduce it): In readme.txt file, the following sentence: PLUGINS_DIR The path to the Tresos plugins directory !john_floros_0-1653582301493.png|width=696,height=261! In fact, PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: PLUGINS_DIR points to EB Tresos plugin folder in readme.txt, which is incorrect. Expected behavior: PLUGINS_DIR should point to RTD plugin folder instead of EB Tresos plugin folder in readme.txt. PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLUGINS_DIR should point to RTD plugin folder : PLUGINS_DIR The path to the RTD plugins directory Ex: PLUGINS_DIR = C:/NXP/SW32_RTD/eclipse/plugins
ARTD-55321	Bug	[S32K3XX] [FLS] Qspi_lp_Abort has no prototype Detailed description (how to reproduce it): Qspi_lp_Abort has no prototype, so iar compiler cannot build tests Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Fls_TS_020 Observed behavior: as description Expected behavior: build successfully Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add prototype
ARTD-55731	New Feature	[S32K3 3.0.0] Eep : added feature to enable/disable CRC Configuration Check (req CPR_RTD_00678.eep) NewWorkDescription:

ID	Subtype	Headline and Description
		Eep S32K3 3.0.0 has the new req CPR_RTD_00678.eep uncover. CPR_RTD_00678.eep: An optional, vendor specific parameter shall disable consistency check through CRC of the flash descriptor. Rationale: If the image is already authenticated, the CRC configuration check is not required. Requirement source: CPR_RTD_00678.eep (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Added feature to enable/disable CRC Configuration Check to cover this requirement.
ARTD-59210	Bug	[S32K3XX] [FLS] Update the return value to fix test build and run fail Detailed description (how to reproduce it): wrong the the return value. !image-2023-03-09-09-37-23-076.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Fls_TS_000 Observed behavior: wrong the the return value Expected behavior: test pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-59951	Bug	[S32K3 3.0.0] [EEP] Compiler warning when enable multicore Detailed description (how to reproduce it): When user enable multicore support, compiler report there warning in Rm_Sema42_ChannelType Preconditions: Eep driver have no waring in all configuration case Test Case ID (internal TC that caught the defect) optional: Eep_TS_001 Observed behavior: When user enable multicore support, compiler report there warning in Rm_Sema42_ChannelType Expected behavior: Eep driver have no waring in all configuration case Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: n/A
ARTD-60480	Bug	[S32K3 3.0.0][EEP] Remove redundant codes which support HS200 HS400 in S32K3XX platform Detailed description (how to reproduce it): S32K3XX do not support high speed HS200/HS400 (1v8 mode), this feature has been barrier in driver code to isolate by define and validate in interface. But it will impact to CCOV in test side. Need use M4 to remove redundant codes which support HS200 HS400 in S32K3XX platform Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CCOV in test side is low Expected behavior: CCOV in test side is high Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove redundant codes which support HS200 HS400 in S32K3XX platform

ID	Subtype	Headline and Description
ARTD-25882	Bug	[FLS] Write data error when the data size will go over the sector boundary Detailed description (how to reproduce it): when writing data on a sector in asynchronous mode and if this data length causes spanning, it will causes errors. After code analyze, this is a bug which the low level driver process a wrong sector index when the write data need to cross sectors. And this issue exist in both K1 and K3 RTD. Preconditions: write data in async mode, and the write data size will across the sector edge. Test Case ID (internal TC that caught the defect) optional: None Observed behavior: write data error Expected behavior: Write data normally Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add the index variable when the case happened in the low level driver, can refer to the MCAL code.
ARTD-26477	Bug	[FLS] [QSPI] SEQID is treated as a LUT index Detailed description (how to reproduce it): In the functions mentioned below the lut parameter is actually a sequence ID, and not a LUT index: Qspi_Ip_IpWrite}} Qspi_Ip_IpRead}} Qspi_Ip_IpCommand}} Besides the confusion, the functional defect is that the parameter is checked against the maximum number of LUT registers: DEV_ASSERT_QSPI(lut < QuadSPI_LUT_COUNT);}} Preconditions: none Test Case ID (internal TC that caught the defect) optional: no TC Observed behavior: the check is too permissive Expected behavior: we should differentiate between the id of the sequence and the index of the LUT register Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Besides the functional change proposed below, a better naming of the parameters would be suited: DEV_ASSERT_QSPI(SeqId < QuadSPI_LUT_COUNT / FEATURE_QSPI_LUT_SEQUENCE_SIZE);}}
ARTD-26603	Bug	[Fls][S32ZE_EAR_080] Remove include "Os.h" in Fls.h for avoiding build failed re-declared function Detailed description (how to reproduce it): Since Os.h has been updated as https://bitbucket.sw.nxp.com/projects/ARTD/repos/os/pull-requests/35/diff#generic/include/Os.h: Build failed occure (re-declare ResumeAllInterrupts() and SuspendAllInterrupts()) on GHS if USER_MODE enable . Preconditions: Osif_Internal.h defines the above APIs already Test Case ID (internal TC that caught the defect) optional: All test build on GHS with USER_MODE enable Observed behavior: Build failed on GHS. Expected behavior: Fls.h shall be updated Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-28180	Bug	[FLS][S32K3XX] Issue in data write using C40 flash (lack of end boundary check for input paramerter) Detailed description (how to reproduce it): If FLS address is 8 bytes aligned for ex:(0x500010) and data length is 128 bytes , in that case data is written from 0x500010 to 0x50007F keeping last 16 bytes unchanged. Observed behavior: Only 112 bytes are written from 0x500010 to 0x50007F

ID	Subtype	Headline and Description
		Expected behavior: Data should be written from 0x500010 to 0x50008F i.e 128 bytes Proposed solution optional: [....]
ARTD-47525	New Feature	[FLS] RTD driver memory resource reduction NewWorkDescription: Implement RTD driver memory optimizations. Implementation of Change Request AAI-1345 Compiler used: IAR Requirement source: Customer Request Proposed solution optional: Implement proposals agreed on change request, as per conclusions provided in ppt documents attached to current ticket and AAI-1345. More details available in tickets dedicated for memory optimizations analysis, cloned for each driver from ARTD-43887. Update driver UserManual, UML design and examples accordingly. If new requirements are created, run traceability to ensure the new requirements are covered. Attach to this ticket an xlsx document with memory size before and after optimizations.

4.7 Change List for 2.0.3

ID	Subtype	Headline and Description

4.8 Change List for 2.0.1

ID	Subtype	Headline and Description
ARTD-24427	Bug	[CRYPTO] Error VKMS_ERR_SMALL_BUFFER should be stored on pResult[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Detailed description (how to reproduce it): Error code VKMS_ERR_SMALL_BUFFER is be stored on pResultLength[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] , but it have to stored in pResult[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Preconditions: Call function with length of data is set to 1 Test Case ID (internal TC that caught the defect) optional: Crypto_TC_FCT_VKMS_0003 Observed behavior: Error code VKMS_ERR_SMALL_BUFFER is be stored on pResultLength[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Expected behavior: Error VKMS_ERR_SMALL_BUFFER should be stored on pResult[CRYPTO_CUSTOM_RESP_STATUS_OFFSET_U32] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-26550	Bug	[CRYPTO] Analyze the case to avoid Dir. 4.7 even false positives Detailed description (how to reproduce it): MISRA reports false positive Dir. 4.7, for more details see ARTD-26511 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior:

ID	Subtype	Headline and Description
		There is no Dir. 4.7 reported in the MISRA report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Analyse all the cases of Dir. 4.7 and design a solution(if possible) that does not duplicate the checks.

ARTD-27732	New Feature	[CRYPTO][S32K344][STD] Update the corresponding resource files with HSE_S32K3XX_0.2.1.0_RC1 interface
		
		NewWorkDescription:
		Update resource files:
		# Crypto.HseSptHmac.<HSE FW TYPE> : Support for HMAC_SHA2_(224, 256) as defined in FIPS PUB 198-1 and SP 800-107.
		To =>> # Crypto.HseSptHmac.<HSE FW TYPE> : Support for HMAC_SHA2_(224, 256, 384, 512*) as defined in FIPS PUB 198-1 and SP 800-107.
		Added:
		# Crypto.HseAesBlockModeMask.<HSE FW TYPE> : Support for Cipher modes flags for AES keys.
		# Crypto.HseEccKeyFormat.<HSE FW TYPE> : Support for HSE ECC key format.
		
		Requirement source:
		[...]
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		
		Proposed solution optional:
		[....]

ARTD-27890	Bug	[CRYPTO] Fix Key Generate and Key Derive functions when functionality is disabled from resource Detailed description (how to reproduce it): Run TS 001 when key generation and derivation are disabled from resource Preconditions: GM driver flavour Test Case ID (internal TC that caught the defect) optional: TS 001 Observed behavior: Functions returns E_OK instead of E_NOT_OK Expected behavior: Function returns NOT_SUPPORTED. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: !image-2022-06-17-18-54-14-290.png|thumbnail!
ARTD-28139	New Feature	[CRYPTO][S32K344][STD] Add interface HSE_S32K3XX_0.2.1.0_RC2 NewWorkDescription: Integrate new HSE_S32K3XX_0.2.1.0_RC2 interface. Requirement source: HSE (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create an excel with the comparison of the new interface with old interface Add the new headers in the crypto repo Add the fw image in the crypto repo Update resource files if there is any changes
ARTD-28183	Bug	[CRYPTO] Function Hse_Ip_GeneralPurposeIrqHandler in Hse_Ip does not follow reqs CPR_RTD_00011 and CPR_RTD_00664 Detailed description (how to reproduce it): Function Hse_Ip_GeneralPurposeIrqHandler() tries to process information even when the driver is not initialized. Preconditions: Driver is not initialized Test Case ID (internal TC that caught the defect) optional: FMEA Analysis Observed behavior: Function executes it's body even when driver is not initialized Expected behavior: Function executes it's body when driver is initialized. Please see reqs CPR_RTD_00011 and CPR_RTD_00664 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Execute function's code when driver is intialized.
ARTD-28586	Bug	[CRYPTO] Fix Misra violations for S32K344 201

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): There is one Misra violation in the Crypto driver: 22222925 MISRA C-2012 Rule 8.13 The pointer variable "base" points to a non-constant type but does not modify the object it points to. Consider adding const qualifier to the points-to type. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There is one Misra violation: MISRA C-2012 Rule 8.13. Expected behavior: There is no Misra violation in the Crypto driver Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]

4.9 Change List for 2.0.0

ID	Subtype	Headline and Description
ARTD-6142	New Feature	[PORT] S32K3 ADC channels mux select<*> There are some ADC channels that can be routed to more than one PAD. Such as ADC1_S14, it can be mapped to PTC5 or PTB0. These settings are included in the register DCMRWF4. Is it possible to include this feature in s32ds CT pin config or in PORT module?
ARTD-9555	New Feature	[mcu] Padkeeping auto enabled leading to siul stuck after standby wakeup<*> Pad keeping is enabled by default[0-enable;1-disable]. If user do not set it. After wakeup from standby, without disabling it, the siul module can't be set again. So User need to be notified in S32CT[power module] whether need to enable pad keeping function. Attached is the test code on S32DS3.4+RTD 0.9.0 beta.
ARTD-9729	New Feature	[ICU][CMP] Output Int. Trigger<*> There's no way to select the "INTTRIG_NONE" option in the graphical config. Tool. Therefore, it's not possible to only enable the Round-Robin interrupt.* Which is sometimes required for STANDBY wake-up operation.
ARTD-10734	Bug	[PWM] Redundant parameter configuration on both Higl level and IP level<*> Detailed description (how to reproduce it): Period, (initial) duty cycle, notification and polarity need to be configured in several places while there is a cross check between these parameters, the issue creates a major inconvenience for platform where it is expected to have a large number of PWM channels (like K3). For instance: To set up Period the user must write a value in: Pwm/PwmChanel/PwmPeriodDefault Pwm/PwmEmiosChannel/EmiosChPeriod and when master bus is used: Mcl/EmiosCommon/EmiosMclMasterBus/EmiosMclDefaultPeriod In case of MasterBus configuration this issue become serious since the user configures a period inside the channel but that period value is ignored and the PWM output will be different from the one expected by usr. Preconditions: master bus is configured in MCL and OPWMT mode is selected for PWM channel. Test Case ID (internal TC that caught the defect) optional: none Observed behavior: PWM period is not the one user configured in PWM. Expected behavior: Parameters should be configured only once (see proposed solution) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In most cases the input parameter should be at high level (Pwm channel) definition. There is no need for a period, duty, polarity or notification parameters at IP, in configuration. For eMIOS channels that use Master bus, the period should be written only in MCL and PWM DefaultPeriod parameter should be ReadOnly with its value automatically calculated based on the MCU frequency and the period value from Mcl/EmiosCommon/EmiosMclMasterBus/EmiosMclDefaultPeriod.
ARTD-11235	New Feature	[PWM] Timer drivers should have reference to MCL and MCU common configurations<*

ID	Subtype	Headline and Description
		_*Detailed description (how to reproduce it): When drivers use common resources from other drivers, these resources should be accessed via references to those drivers. For instance in case OCU, PWM and ICU when configured to use eMIOS IP, they might use a common bus configured in MCL. The configuration of each drivers should reference the bus configuration to access certain parameters that may be needed in their internal logic (number of configured counter ticks, dividers etc). Using a reference might also insure that invalid configuration of the bus are not exported to driver. Internal references which are NOT configured by the user SHOULD not be used since they might mask problems. PWM, OCU and GPT drivers should always use references to MCU driver even in cases where AUTOSAR does not require it since a reference to MCU clock will make much easier to determine the frequency of the given channel... For ICU this is not needed since in all cases the result of the ICU measurement is in ticks. Preconditions: [none] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [see description] Expected behavior: [see description] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-12331	New Feature	[BUILD_ENV] Update Ecuc.xdm in project template to match newly added container<*> NewWorkDescription: EcucPduCollection is de-populated after the tresosproject.pl script is run at generation. This causes drivers dependend on that container (i.e Fr) to fail at generation. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add EcucPduCollection in the new template.
ARTD-14050	New Feature	[I3C] Add support for In-band interrupt (IBI)<*> NewWorkDescription: In-band interrupt (IBI) Please refer to initial analysis done in https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Group%204/I3C/I3C_Analysis.xlsx?d=w15656ae7d09a4b49939fa7d8e84207c3&csf=1&web=1&e=RiyG9f Check if requirement available or need any updates Create/update dev test Add section/update UM Update UML if required If examples already available, update examples with any eventual new nodes Requirement source: RM.pdf Proposed solution optional: brief Perform a Slave Request on the I3C bus. details This function is used to request an In-Band Interrupt, Hot-Join, or Master Request IbiData and ExtData parameters are used only ive the Event is an In-Band Interrupt. If the Event is not an In-Band Interrupt, these parameters are ignored in the API's implementation. IbiData and ExtData are ignored if the In-Band Interrupt has no mandatory byte. If the In-Band Interrupt has only one mandatory byte, ExtData is ignored. param[in] Event Type of the event: IBI, HJ, MR param[in] IbiData If IBI, the mandatory byte param[in] ExtData If IBI and more than one madatory byte, pointer to the extra bytes / I3c_Ip_StatusType I3c_SlaveRequestEvent(const I3c_SlaveRequestType Event, const uint8 IbiData, uint8 ExtData);
ARTD-14051	New Feature	[I3C] Add support for Hot-join<*> NewWorkDescription: Hot-join Please refer to initial analysis done in https://nxp1.sharepoint.com/:x:/s/Zebra/EedqZRWa0ElLk5-n2OhCB8MByBV0CEBRFInle2wexrt_0g?e=TP6TXV Check if requirement available or need any updates Create/update dev test Add section/update UM Update UML if required If examples already available, update examples with any eventual new nodes Requirement source: RM.pdf Proposed solution optional: [...]
ARTD-14054	New Feature	[I3C] Add exclusive areas support<*> Implement exclusive areas https://nxp1.sharepoint.com/:p:/s/Zebra/EehFcYqIlpVJkmyNp8pcae4BNyizwm47eVxbN_s7u30Tzg?e=gTPmi7 Analyze and try to move in IPL, to have exclusive areas as small as possible. See details in presentation and recording

ID	Subtype	Headline and Description
		Take into account also BSWMD guideline: https://confluence.sw.nxp.com/display/AUTORD/BSWMD
ARTD-14839	Bug	[RM] Incorrect DERR used for XRDC_1<*> Detailed description (how to reproduce it): In _Xrdc_Ip_GetDomainIDErrorStatus_ function, the Xrdc_DomainErrorWord array, which contains the DERR word index positions, are both used two instance, which is not matched with XRDC_1. Also the loop checks through XRDC_NUMOF_DOMAIN_ERROR_WORD indexes, which is 17, however in XRDC_1 there are only 7 indexes. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In _Xrdc_Ip_GetDomainIDErrorStatus_ function, the _Xrdc_DomainErrorWord array and XRDC_NUMOF_DOMAIN_ERROR_WORD are used for both of these two XRDC instances, which is not correct Expected behavior: Correct values are used for XRDC_1 in _Xrdc_Ip_GetDomainIDErrorStatus_ function Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15328	New Feature	[LIN] Implement CPR_RTD_00543.lin (MR-200)<*> NewWorkDescription: Driver should implement req as below: Req ID||Object Text||Verification Criteria CPR_RTD_00543.lin|The driver shall prevent configuration of the same hardware instance between HL configuration and standalone IP configuration.|Test Case Requirement source: CPR_RTD_00543.lin (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Implement CPR_RTD_00543.lin
ARTD-15535	New Feature	[SPI] Implement new requirement: CPR_RTD_00543.spi<*> NewWorkDescription: Implement new requirements: CPR_RTD_00543.spi and CPR_RTD_00544.spi Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow guiding: https://nxp1.sharepoint.com/:p:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B28A51BA3-C452-40F5-ABB6-A6933671DCD3%7D&file=NXP_RTD_AUTOSAR_S32CT_V2.pptx&action=edit&mobileredirect=true
ARTD-15574	New Feature	[ADC] Parameter for Adc_CtuEnableHwTrigger() should be defined as symbolic values or enums<*> Detailed description (how to reproduce it): In order to enable HW triggering via BCTU mode the user must call Adc_CtuEnableHwTrigger() with the correct trigger source. This trigger source is configurable and enabled in /Adc/AdcConfigSet/BctuHwUnit//BctuInternalTrigger via BctuTriggerSource parameter. However that value is NOT generated anywhere, and the user is unaware what is the correct value for which the Adc_CtuEnableHwTrigger(_Adc_CtuTrigSrcType Trigger_) will work. The documentation does not provide a table o value and Adc_CtuTrigSrcType is defined as integer. Preconditions: BCTU mode configure. Test Case ID (internal TC that caught the defect) optional: note Observed behavior: Function fails at compile time which may happen if the application references the /Adc/AdcConfigSet/BctuHwUnit//BctuInternalTrigger container and expects that a define value is generated in ADC from BctuTriggerSource. Function fails at run time if application does not call Adc_CtuEnableHwTrigger() with the correct index in the list of triggers described in the Reference Manual (chapter 55.1.2) and there is not direct correlation between the table in the RM and the enum used for defining BctuTriggerSource in Adc.xdm. So finding the correct value become a matter of try and error. Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Define Adc_CtuTrigSrcType as enum containing the list of triggers expected by Adc_CtuEnableHwTrigger(). The labels of this enum should be identical with the labels used for BctuTriggerSource.
ARTD-15901	New Feature	[I3C] Implement I3c_SetBaudRate and I3c_GetBaudRate<*> NewWorkDescription: There are some remaining features need to be implemented: / brief Set the baud rate for all subsequent I3C communications. details This function is used to set the baud rate for all subsequent I3C communications. param[in] Instance I3C instance

ID	Subtype	Headline and Description
		param[in] I2cBaud I2c baud param[in] OpenDrainBaud Open Drain baud param[in] PushPullBaud Push pull baud / Std_ReturnType I3c_SetBaudRate(const uint32 Instance, const uint8 I2cBaud, const uint8 OpenDrainBaud, const uint8 PushPullBaud); / brief Get the baud rate of the I3C module. details This function is used to get the baud rate of the I3C module. param[in] Instance I3C instance param[in] I2cBaud I2c baud param[in] OpenDrainBaud Open Drain baud param[in] PushPullBaud Push pull baud / Std_ReturnType I3c_GetBaudRate(const uint32 Instance, uint8 I2cBaud, uint8 OpenDrainBaud, uint8 PushPullBaud); Requirement source: RM (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-16302	Bug	[ADC] AdcPreSamplingOnce has no effect on generated code<*> Detailed description (how to reproduce it): AdcPreSamplingOnce has no effect on codegen of EB/CT UI, should be not editable with default value as "enabled" base on current driver implementation Preconditions: AdcPreSamplingOnce must be fully supported with ON/OFF feature Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: AdcPreSamplingOnce has no effect on generated code. Expected behavior: All nodes should have effect on generated code/be used by the driver. AdcPreSamplingOnce is fully supported Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add support AdcPreSamplingOnce
ARTD-17307	Bug	[S32DS] There are many Semantic errors message raised by S32DS but they are already defined in the project<*> Detailed description (how to reproduce it): There are many Semantic errors message raised by S32DS but they are already defined in the project and the project still build successful. This kind of error will be only appeared in almost of files after open them. They are not raised if the source files are not opened. This problem is appeared on all RTD releases, can check this problem on Examples project. !image-2021-09-27-14-22-49-376.png! Preconditions: The problem can be also reproduced on S32K3: Install the packages: S32 Design Studio 3.4 Service pack 2 with S32K3xx development package build 210923 [LINK|https://nxp1.sharepoint.com/sites/freeshareprivate/S32DSproject/Lists/Builds/DispForm.aspx?ID=1744] RTD S32K3XX RTM100 update side Open example: Can_example_S32K344 Generate code by press "Update code" button on GUI of peripheral tool Build project Open some source files in "RTD" and "board" folders in the project on S32DS GUI Test Case ID (internal TC that caught the defect) optional: Examples project Observed behavior: Semantic errors appears but they are already defined in other files and the project still build successfully Expected behavior: There is no Semantic errors Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17156	New Feature	[SENT] Improve Received Message Diagnostics for sent driver<*> NewWorkDescription: Implements for each channel all receiver diagnostics as specified by the SAE Specifications. 1. Calibration pulse length < 56 clock ticks – 25% or > 56 clock ticks 25%. *2.* *Not the expected number of falling edges between calibration pulses. (Message length is pre-defined by each sensor device). 3. Checksum error. 4. Any nibble data values measured as < 0 or > 15. *5. Successive Calibration Pulses. Sent driver need to improve to implement #2 and #5*.

ID	Subtype	Headline and Description
		Requirement source: SAE Specifications Proposed solution optional: NA
ARTD-17198	Bug	[SPI] SPI_EXCLUSIVE_AREA_02 is missing in bswmd file<*> Detailed description (how to reproduce it): SPI_EXCLUSIVE_AREA_02 is not assigned to any function in bswmd file. This results in compiler error as this exclusive area is not generated by Autosar RTE. Preconditions: Spi driver used with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Exclusive areas 02 is not generated by Autosar RTE Expected behavior: Exclusive areas 02 is generated by Autosar RTE Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the exclusive_areas_to_be_defined_in_bsw_scheduler.dox to map the exclusive areas to a function which is generated into bswmd file.
ARTD-17241	New Feature	[I3C] Input parameter "Instance" should be uint8 ,,"Input parameter ""Instance"" should be uint8 instead of uint32.
ARTD-17268	Bug	[ADC] Unused ADC_MAX_HARDWARE_TRIGGERS define when CTU hardware trigger API is disabled<*> Detailed description (how to reproduce it): ADC_MAX_HARDWARE_TRIGGERS is unused if ADC_ENABLE_CTUTRIG_NONAUTO_API is STD_OFF. Preconditions: EB or CT config with CTU trigger mode disabled. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: ADC_MAX_HARDWARE_TRIGGERS is generated when CTU trigger mode is not enabled. Expected behavior: ADC_MAX_HARDWARE_TRIGGERS should only be generated when CTU trigger mode is enabled. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17358	Bug	[I3C] Arrays are generated from CT even if they contain no elements<*> Detailed description (how to reproduce it): [...] Build plugin and import example in S32DS. Configure IBI Address Registry and Dynamic Address List arrays with no elements and generate. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] !image-2021-09-30-15-25-55-475.png! !image-2021-09-30-15-26-17-595.png! Expected behavior: [...] These arrays should not be generated in PBcfg.c if they contain no elements. In master config structure they should be generated with NULL_PTR, in this case. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17424	Bug	[gpt] Array indices are not correctly generated in DS when multicore support is enabled<*> Detailed description (how to reproduce it): Array index is wrong when the structures are generated per partition, as you can see in attached pictures. !image-2021-10-01-15-17-19-822.png! !image-2021-10-01-15-17-36-860.png! Preconditions: to use Design Studio as config tool to use at least one partition Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: the index is equal with the array size Expected behavior: the index should be the correct one

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: to update the templates to generate the correct index
ARTD-17496	Bug	[ICU] check DMA notification function name 'dmaLogicChannel_InterruptCallback' is wrong<*> Detailed description (how to reproduce it): when configuring more than 1 Mcl DMA channel, if configuring the name of the first channel as 'dmaLogicChannel_Type_1' and the name of the next channel as 'dmaLogicChannel_Type_13' and only one Icu channel configured as a DMA link is used to 'dmaLogicChannel_Type_13'. The node 'dmaLogicChannel_InterruptCallback' in Mcl will be wrong. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17507	Bug	[ADC] Missing exclusive areas in bswmd file<*> Detailed description (how to reproduce it): The folowing excusive areas is not getting generated in rte.c: ADC_EXCLUSIVE_AREA_17 ADC_EXCLUSIVE_AREA_23 ADC_EXCLUSIVE_AREA_24 ADC_EXCLUSIVE_AREA_26 ADC_EXCLUSIVE_AREA_27 ADC_EXCLUSIVE_AREA_39 ADC_EXCLUSIVE_AREA_40 ADC_EXCLUSIVE_AREA_69 ADC_EXCLUSIVE_AREA_70 They are not generated because these exclusive areas are missing or not assigned to a function in bswmd file. Preconditions: Adc driver used with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Exclusive areas not generated by RTE Expected behavior: Exclusive areas are generated by RTE Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add exclusive areas into bswmd file. Internally update the exclusive_areas_to_be_defined_in_bsw_scheduler.dox file to map the exclusive areas to functions and then also add the IP functions into NonASR_ServiceID.xml file.
ARTD-17527	New Feature	[S32K3xx] Only files .c and .h should be showed on Code preview of Peripheral tool<*> Step: 1.Create project S32K3xx attach sdk RTD 1.0.0 with gcc10.2/ghs/iar toolchain 2. Open Peripheral tool, then check Code Preview 3. Add any sdk component then check Code Preview Observed behavior: 2,3: Many files .ecpd (about 70-90 files) are showed Expected behavior: 2,3: Only necessary files .c and .h should be showed
ARTD-17564	Bug	[ADC] Open findings from code review checklist<*> Detailed description (how to reproduce it): Fix remaining findings that were postponed on ARTD-15668. #|Source Code file|Issue |Proposed Correction|Status|Comment 1|All EB and CT generate files using AdcEnableDmaTrasferMode and CtuEnableDmaTrasferMode nodes|Rule 3|AdcEnableDmaTransferMode, CtuEnableDmaTransferMode|Postponed|Postponed due to affect test code 5|All files using source file version information of IPW, some header wrappers in IPL.|Rule 19,25: some defines don't have appropriate prefix equivalent to layer (HLD/IPW/IPL)|Add prefix ADC_IPW, ADC_SAR_IP, BCTU_IP to defines|Postponed|Postponed due to affect test code 6|Adc_Sar_Ip_Types.h|Rule 20,25: RESOLUTION_x of Adc_Sar_Ip_Resolution doesn't have prefix|Add prefix ADC_SAR_IP to defines and update generation code|Postponed|Postponed due to affect test code 7|Adc_Ipw_Types.h|Rule 22: Some typedef missing Ipw prefix|Add prefix Ipw to typedefs|Postponed|Postponed due to affect test code 9|Adc.c, Adc_Ipw.c, Adc_Ip.c, Ctu_Ip.c, Bctu_Ip.c|Rule 28|Correct prefix of global variables|Postponed|Postponed due to affect test code Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA

ID	Subtype	Headline and Description
		Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17575	New Feature	[BUILD_ENV] Update compiler options<*> NewWorkDescription: There are some points conflict and needs to update after review and compare compiler option between SOW with S32DS in the ticket _**_ ARTD-16608 # For GHS: !image-2021-10-06-18-58-23-983.png! Option “-nostartfiles” is an linker option. It also mentioned in GHS document: !image-2021-10-06-18-44-13-702.png! So, this option should be moved from Compiler section to Linker section in excel file [LINK|https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Tools%20(build,%20misra,%20vsmd,%20etc)/Compilers/RTD_Compiler_Options.xlsx?d=wc54fdf4ed62b4036b28bba16838efb73&csf=1&web=1&e=qdKltl] 2. For IAR: !image-2021-10-06-18-57-39-415.png! The define "-DEU_DISABLE_ANSILIB_CALLS" is only used in EUnit.c for testing and not used in our driver code. So it should be removed from our compiler option and move to EUnit. Option “-c” is described in excel file but it is not exist on IAR compiler. So, this option should be removed. !image-2021-10-06-18-56-53-569.png! For more detail please check in email attached. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-17576	Bug	[PWM] Debug and correct nightly build<*> Detailed description (how to reproduce it): Investigate, debug and correct test case that runs nighly on the board. Driver bamboo is failing with inconsistent data on runtime for PWM see log. !image-2021-10-06-15-49-24-543.png|width=843,height=224! [https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?FolderCTID=0x012000D681AD520E486343AF1E2AF7AEE3B740&id=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021%2FreportBLNRTD44S32K3XX10058%5F1776126004%2Ehtml&parent=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Nightly Observed behavior: test case failing on run Expected behavior: test pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17579	Bug	[ICU] Debug and correct nightly build<*> Detailed description (how to reproduce it): Investigate, debug and correct test case that runs nighly on the board. Driver bamboo is failing with test execution fails : see in build [artifact|https://bamboo3.sw.nxp.com/artifact/ARTD-CIICU/BRT/build-46/Dev-Tests-Artifacts/dev_tests_reports/S32K3XX_4.4/gcc] !image-2021-10-06-15-49-24-543.png|width=843,height=224! [https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?FolderCTID=0x012000D681AD520E486343AF1E2AF7AEE3B740&id=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021%2FreportBLNRTD44S32K3XX10058%5F1776126004%2Ehtml&parent=%2Fsites%2FZebra%2FShared%20Documents%2FNightly%2FEmailMessages%5F10%5F2021] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Nightly Observed behavior: test case failing on run Expected behavior: test pass Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17583	New Feature	[RM] XRDC shall allow locking the XRDC registers<*>

ID	Subtype	Headline and Description
		NewWorkDescription: A safety requirement (ARSW-46) requires that XRDC configuration to be lock-able, to prevent other master changing it. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support locking the XRDC configured registers, as a configuration option. Could be done by having some extra masks or in a separate step at the end of init.

ARTD-17736	Bug	[FLS] Qspi_Ip_Read function checks error callout for NULL_PTR instead of ECC callout<*>
		
		Detailed description (how to reproduce it):
		Source code : Qspi_Ip.c
		Function : Qspi_Ip_Read
		There is a process to call eccCheckCallout on line 1168, but line 1166 checks whether errorCheckCallout is NULL_PTR. We believe that it is necessary to check eccCheckCallout.
		/ Call user callout, if available, to check ecc status /
		if ((STATUS_QSPI_IP_SUCCESS == status) && (NULL_PTR != state->configuration->errorCheckCallout))
		{
		status = state->configuration->eccCheckCallout(instance, crtAddress, chunkSize);
		}
		Preconditions:
		N/A
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		errorCheckCallout is checked if it is NULL_PTR
		Expected behavior:
		eccCheckCallout shall be checked if it is NULL_PTR
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Replace the check for NULL_PTR as follows (errorCheckCallout modified to eccCheckCallout):
		/ Call user callout, if available, to check ecc status /
		if ((STATUS_QSPI_IP_SUCCESS == status) && (NULL_PTR != state->configuration->eccCheckCallout))
		{
		status = state->configuration->eccCheckCallout(instance, crtAddress, chunkSize);
		}

ARTD-17766	New Feature	[Wdg] Replace Swt_Ip_FeatureDefine.h with resource symbols and generate in CfgDefines.h<*> NewWorkDescription: [Wdg] Replace Swt_Ip_FeatureDefine.h with resource symbols and generate in CfgDefines.h Requirement source: Internal refactoring Proposed solution optional: [Wdg] Replace Swt_Ip_FeatureDefine.h with resource symbols and generate in CfgDefines.h
ARTD-17794	Bug	[ADC] WDG and EOC might be stuck in Handler with spurious interrupt<*> WDG and EOC function are still available in IPL after disable them from configurator. Only ISR for them are disabled, that can lead to stuck in handler infinite since cannt clear its flag The proposal is to disable all functions related to these feature if disabled on UI and need to handle spurious interrupt for this case
ARTD-17796	Bug	[CRYPTO] Fix compiler warnings reported in S32K3XX 1.0.0 P01 for GM releases<*> Detailed description (how to reproduce it): There are 3 compiler warnings that are listed in the attached Compiler Warnings report. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Crypto_TS_DefineCompile_cfg1_CORE0 Crypto_TS_DefineCompile_cfg2_CORE0 Observed behavior: [...] Expected behavior: No compiler warnings present Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-17800	New Feature	[RM] Improve code for XRDC, common for all platforms ,,"Detailed description (how to reproduce it): Currently, some PID APIs support only 1 instance. But with new platform which may have more than one instance. So those APIs should be update to support. Preconditions: on platform which is support PID feature Test Case ID (internal TC that caught the defect) optional: Dev test 001 Observed behavior: NA

ID	Subtype	Headline and Description
		Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update to support multi instances
ARTD-17802	Bug	[S32K3xx] Board and RTD folder should be excluded after detach SDK<*> Preconditions: Install *S32DS 3.5 B211006* RTD package for S32K3xx: B211007 (S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2110.zip) Test Case: # Create project enable SDK S32CT for any processors (ex: S32K344) # Right-click on project → SDKs → Detach SDK # Check board and RTD folder Observed behavior: RTD and board folder are still *included Expected behavior: RTD and board folder should be excluded Note: This issue is also happened in S32DS 3.4 Update 3 with this RTD package. And It *is not happended in S32DS 3.4 Service pack 2 release _RTD package for S32K3xx: B211007 (*S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2110.zip)
ARTD-17812	Bug	[Adc] MISRA Rule 8.5 Symbol "Adc_Sar_x_Isr" is declared more than once. ,,"Detailed description (how to reproduce it): Symbol ""Adc_Sar_x_Isr"" is declared more than once. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Symbol ""Adc_Sar_x_Isr"" is declared more than once. Expected behavior: Violation is fixed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-17847	Bug	[S32K3] RTD 1.0.0 code generation fails in S32 Design Studio<*> Installed the SW32K3_RTD_4.4_1.0.0_DS_updatesite_D2110.zip inside the S32 Design Studio IDE v3.4 Service Pack 2, following the instructions from the Release Notes (...it must be installed by opening Help > S32 Design Studio Extensions and Updates > Add Update Sites and selecting the archive file containing the S32 RTD software and then check the S32 RTD software package to be installed and continue the installation process.) Imported Uart_Example_S32K344, then pressed the Update Code button the following error is generated (please see attached error.png) Same behavior is reproductible for other examples as well (e.g. Pwm_Example_S32K344)
ARTD-17865	New Feature	[I3c] Integrate DAA in Init function<*> NewWorkDescription: Integrate DAA in Init function Array is already generated by configurator. Need to call API in init with generated array Also add a configurator checkbox & define to allow users to enable/disable this functionality Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-17849	New Feature	[I3c] Validate support for Dynamic Address Assignment<*> NewWorkDescription: Please refer to initial analysis done in [https://nxp1.sharepoint.com/:x:/s/Zebra/EedqZRWa0EILk5-n2OhCB8MByBV0CEBRFInle2wexrt_0g?e=TP6TXV] Check if requirement available or need any updates Create dev test with Dynamic Addressing use 2 boards with I3C Fix findings. Requirement source: RM.pdf Proposed solution optional: [...]
ARTD-17867	New Feature	[I3c] Implement methods to set the slave status activities<*> NewWorkDescription: Implement methods to set the slave activities which are returned by GETSTATUS command. Check if all bitfields should be set by the user. Check if requirement available or need any updates. Requirement source:

ID	Subtype	Headline and Description
		[...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-17898	Bug	[RM] Update the MRC granularity constraints<*> Detailed description (how to reproduce it): The XRDC MRC granularity and alignment restrictions have been increased from 32 bytes to 4KB in newer RM versions. This needs to be updated in the Tresos and CT field checks, to enforce the new values. more details in the attached email thread. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Review the RMs for the Notes mentioning this details, update the CT and EBT schema validations to enforce this new values. [...]
ARTD-17931	Bug	[Wdg] When WdgDevErrorDetect disabled, some generated defines are not used ,,"Detailed description (how to reproduce it): When WdgDevErrorDetect disabled, some generated defines are not used MISRA C-2012 Rule 2.5 1164 Advisory Low Quality Macro ""WDG_TIMEOUT_VALUE_ARRAY"" is defined but never used. /ARTD-CIW55-9/sources/SJA11XX_4.4/output/SJA11XX_SJA1110/wdg/Wdg_TS_Shared_000_cfgPB_CORE0/generate_tresos/include/Wdg_Cfg_Defines.h 228 Intentional Dismissed This violation requires information for indirect service mode MISRA C-2012 Rule 2.5 1164 Advisory Low Quality Macro ""SWT_TIMEOUT_VALUE_ARRAY"" is defined but never used. /ARTD-CIW55-9/sources/SJA11XX_4.4/output/SJA11XX_SJA1110/wdg/Wdg_TS_Shared_000_cfgPB_CORE0/generate_tresos/include/Swt_Ip_Cfg_Defines.h 100 Intentional Dismissed This violation requires information for indirect service mode MISRA C-2012 Rule 2.5 1164 Advisory Low Quality Macro ""WDG_IPW_TIMEOUT_VALUE_ARRAY"" is defined but never used. /ARTD-CIW55-9/sources/SJA11XX_4.4/output/SJA11XX_SJA1110/wdg/Wdg_TS_Shared_000_cfgPB_CORE0/generate_tresos/include/Wdg_Ipw_Cfg_Defines.h Preconditions: Direct service mode disabled Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: See description Expected behavior: Defines are not generated if not used Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Only generate when WdgDevErrorDetect enabled in both S32CT and EBT
ARTD-17933	Bug	[I2c] Cannot migrate EB tresos configuration to CT configuration because note slave address<*> Detailed description (how to reproduce it): [...] I converted example from EB to CT. I import i2c.epc file to CT. Open peripheral tool in S32DS. Have error CDD_i2c component. I saw that the node error belong to Ip layer. It should not add in HLD CDD_i2c component. !image-2021-10-18-16-59-18-790.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] Remove node slave address on CT configuration
ARTD-17951	Bug	[ADC] Unused ISR code when interrupts are disabled in HLD configurator AdcInterrupt tab<*> Detailed description (how to reproduce it): At IPL for all IPs, ISRs are not removed at precompiled, even if interrupts are not being configured. Preconditions: None. Test Case ID (internal TC that caught the defect) optional: [...]

ID	Subtype	Headline and Description
		Observed behavior: ISR code is always compiled. Expected behavior: ISR code not present when corresponding interrupts are not configured. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-17979	Bug	
		[Emios Ip] All emios IP functions have the input parameter not follow the Pascal rule<*>
		
		Detailed description (how to reproduce it):
		[Emios Ip] All Emios IP functions have the input parameter not follow the Pascal rule
		Example:
		void Emios_Mcl_Ip_ComparatorTransferDisable(uint8 instance, uint32 channelMask);
		Emios_Ip_CommonStatusType Emios_Mcl_Ip_Deinit(uint8 instance);
		void Emios_Mcl_Ip_SetReloadInterval(uint8 hwInstance, uint8 hwChannel, uint8 interval);
		Rule 27: Local variables, function parameters and struct members shall use only PascalCase naming, without any special prefix (e.g. Hungarian notation or <Msn>, <Ip> etc.)
		<VarName>
		Example: Channel, State, Index, Config, etc.
		Preconditions:
		NA
		Test Case ID (internal TC that caught the defect) optional:
		NA
		Observed behavior:
		NA
		Expected behavior:
		NA
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		NA

ARTD-17988	New Feature	 [BASE] Use linkerFile tag instead of resourceFile tag in itm file for IAR profile<*> NewWorkDescription: IAR profile setting in itm file should update according to the advice from S32DS team mentioned in the ticket S32DS-24032. For option 'incPaths' tag, 'configId' attribute should be removed. For linker file configuration, linkerFile tag should be used instead of resourceFile tag. So, for Debug_RAM profile, no need to duplicate the options 'incPaths' and 'icfFile'. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-18037	New Feature	 [gpt] Create new APIs for STM and FTM Ips<*> NewWorkDescription: This ticket is cloned because bamboo build is failing for S32XX and S32K3XX platforms because some drivers are not updated for these releases. For this ticket the only thing which is needed is to re-run bamboo plan with these 2 platforms. We received a request for stm and ftm ips from Zephyr team; they need in their application an API which will provide a match with an absolute value as timeout/compare value(refer to the attached picture). Our proposal is to create an API <IpName>_Ip_StartCountingAbsolute(uint8 instance, uint8 channel uint32 timevalue), timevalue_ represents the absolute value of counter register Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]

ARTD-18747	Bug	
		[Wdg] Wdg_ChannelInit fails if SWT is already init out of reset by the IVT config<*>
		
		In S32K3, there is an option to enable the SWT (Watchdog) by the Bootheader, so the watchdog is enable out of reset.
		If this is the case the function Wdg_ChannelInit fails to initialize/configure the SWT long as there is a part of the driver that corroborate if the module is already active or not.
		.....
		if ((Swt_Ip_IsEnable(base)) ((boolean)(Swt_Ip_Unlock(base) == SWT_IP_STATUS_ERROR)))
		{
		ret = SWT_IP_STATUS_ERROR;
		.....
		
		In our Startup code there is a part where the SWT are disabled as there is an Autosar Guideline which mentions:
		/ Autosar Guidance 5 The start-up code shall ensure that the MCU internal watchdog shall not be serviced until the watchdog is initialized from the MCAL watchdog driver. This can be done for example by increasing the watchdog service time. /
		
		But as long as this is no a "MUST", customer mentioned that there is not need to disabled the Watchdog and that the driver should be able to propertly configure the Watchdog even if it is already enable by the bootheader.
		
		They also mentioned that if they try to reconfigure the SWT to extent the period of time to service the watchdog, the init function is still failing.

ID	Subtype	Headline and Description
		So, in conclusion, Wdg_ChannelInit should be able to verify if the SWT is already enabled by the bootheader, and if so, reconfigure it with the application configuration.
ARTD-18759	Bug	[CAN] Timestamp name does not match R41's RM<*> Detailed description (how to reproduce it): Create S32R41 project for CAN testing: Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2021-10-26-15-39-45-435.png! Expected behavior: Timestamp name should be re-checked for PFE !image-2021-10-26-15-39-19-914.png! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-18762	Bug	[Base] Driver and requirement are inconsistent<*> Detailed description (how to reproduce it): There are 3 requirements that are inconsistent between Requirements and Driver code !image-2021-10-26-16-17-07-413.png|thumbnail! Preconditions: Requirement baseline: 26.3 INTREQ_BASE_RTD_4.4_SJA11XX_0.9.0_I03 Base tag: BASE_258 Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: See detail description Expected behavior: The requirement and driver should be consistent Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Create ITWG ticket to update internal requirements
ARTD-18833	New Feature	[BASE] Split ASM_KEYWORD into volatile and non-volatile<*> NewWorkDescription: Split ASM_KEYWORD into volatile and non-volatile in order to avoid compiler warnings related to volatile asm statements used out of functions. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Split ASM_KEYWORD into volatile and non-volatile.
ARTD-18840	New Feature	[adc] [S32 3.0.0] Create driver for S32G3<*> Support derivative S32G3: S32G378A_BGA525 S32G379A_BGA525 S32G398A_BGA525 S32G399A_BGA525 S32G338M_BGA525 S32G339M_BGA525 S32G358A_BGA525 S32G359A_BGA525 With similar support as for S32G2. S32G3 Examples will be developed and tested on EVB Board. For detailed scope of the release see SOW: [S32 RTD for S32 3.0.0 SOW.docx (sharepoint.com)|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BD4BB6374-2FF8-4854-98BF-B8C762052305%7D&file=S32%20RTD%20for%20S32%203.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-18887	New Feature	[platform] [S32K3 2.0.0 CD01] Create driver for S32K342<*> Support derivative S32K342: S32K342_100MQFP S32K342_172MQFP With: Tresos & S32CT support Create Tresos and CT examples for driver and execute examples Run development tests For detailed scope of the release see SOW: [S32K3 RTD ASR 4.4 2.0.0 SOW.docx (sharepoint.com)|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B3C101971-D503-429C-B4CF-779627CDE942%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20SOW.docx&action=default&mobileredirect=true]

ID	Subtype	Headline and Description
ARTD-18894	New Feature	[uart] [S32K3 2.0.0 CD01] Create driver for S32K342<*> Support derivative S32K342: S32K342_100MQFP S32K342_172MQFP With: Tresos & S32CT support Create Tresos and CT examples for driver and execute examples Run development tests For detailed scope of the release see SOW: [S32K3 RTD ASR 4.4 2.0.0 SOW.docx (sharepoint.com)|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7B3C101971-D503-429C-B4CF-779627CDE942%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-18949	Bug	[SPI] Function parameter of Spi_SetupEB was not following the requirement and autosar specs<*> Detailed description (how to reproduce it): The function declaring of Spi_SetupEB was not following the requirement and autosar specs Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Std_ReturnType Spi_SetupEB (Spi_ChannelType Channel, Spi_DataBufferType SrcDataBufferPtr, Spi_DataBufferType DesDataBufferPtr, Spi_NumberOfDataType Length) Expected behavior: Std_ReturnType Spi_SetupEB (Spi_ChannelType Channel, const Spi_DataBufferType SrcDataBufferPtr, Spi_DataBufferType DesDataBufferPtr, Spi_NumberOfDataType Length) Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change Spi_SetupEB to follow requirement and autosar specs
ARTD-18951	New Feature	[ADC] Remove unnecessary checking by FEATURE_ADC_BAD_ACCESS_PROT_CHANNEL<*> For Adc_sar IP driver, FEATURE_ADC_BAD_ACCESS_PROT_CHANNEL is used to not access to unavailable register that can lead to hardfault or unexpected behavior Using this marco requires a lot of checking when accessing many register that takes time and might cause overhead. Proposal to not use it and find the better way to improve driver regarding this Proposal is to improve/remove unnecessary checking by this define
ARTD-18969	Bug	[ARTD][Eth][S32K344] Wrongly truncated buffer on Gmac_Ip_ReadFrame function<*> Detailed description (how to reproduce it): The S32K3 TCPIP stack is ported over Gmac_Ip driver. On Gmac_Ip_ReadFrame function, there is a condition that truncates the receive buffer length: /* *According to requirement CPR_RTD_00284.eth* */ *if (Buff->Length > (uint16)(Bd->Info1 & GMAC_INFO1_LENGTH_MASK)) *{ *Buff->Length = (uint16)(Bd->Info1 & GMAC_INFO1_LENGTH_MASK); *} For some reason, this buffer length is set to 0 when this condition is executed. I assume this happens because Bd->Info1 is already 0 (so it sets the Buff->Length also to 0). (Picture attached) This issue was noticed during TCPIP testing over Gmac_Ip driver. After the board acquired Ipv4 address, we sent pings to it. After several pings, the issue occured. (Picture attached). Notes: If this condition is commented/removed, the TCPIP stack is working well. This condition was not available on RTD S32K3 BETA 0.9.2 Preconditions: S32DS 3.4 with S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2110 installed. S32DS project with Gmac_Ip component configured. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The Gmac_Ip_ReadFrame function sets Rx buffer length to 0 on certain condition is met, making the driver not working correctly anymore. Expected behavior: The buffer length should not be set to 0 in this case. It should be set to its correct value.

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-18975	New Feature	[ETH][GMAC] Improve zero-copy operating mode<*> NewWorkDescription: Improve zero-copy operating mode Requirement source: Internal driver requirements (GMAC_IP_001) (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add compiler-time switches EthCtrlAllocateTxDataBuffers and EthCtrlAllocateRxDataBuffers to avoid extraneous memory consumption when the application provides its own buffers. Add examples of usage in the documentation.
ARTD-18978	Bug	[ADC] BCTU and CTU Ip includes Det.h<*> Detailed description (how to reproduce it): BCTU and CTU Ip includes Det.h in Bctu_Ip_PBcfg.c and Ctu_Ip_PBcfg.c generated from EBT or S32CT Adc_Ipw_Irq.c included Det.h to checking spurious interrupt. But there is no Det need to be reported here because of Rationale: The DEM or DET callback is long in its full implementation, delaying the ISR. Currently, Adc report all DET error at HLD layer Preconditions: N.A. Observed behavior: BCTU and CTU Ip includes Det.h in Bctu_Ip_PBcfg.c and Ctu_Ip_PBcfg.c generated from EBT or S32CT Expected behavior: BCTU and CTU Ip must not have dependency on Det.h Consider remove Det.h also in Adc_Ipw_Irq.c Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N.A.
ARTD-18991	Bug	[CRYPTO] Functions should be return error CRYPTO_E_BUSY when channel busy<*> Detailed description (how to reproduce it): Some function not return error CRYPTO_E_BUSY when channel busy (u8MuChannel = HSE_IP_INVALID_MU_CHANNEL_U8) Preconditions: Call several ProcessJob on async mode to make channel busy Test Case ID (internal TC that caught the defect) optional: Crypto_TC_FCT_0047 Observed behavior: Some function return error E_NOT_OK when channel busy Expected behavior: All function will return error CRYPTO_E_BUSY when channel busy Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-19000	Bug	[Gpt] GPT_CONFIG_VS_0_PB macro is generated when VariantPreCompile is used<*> Detailed description (how to reproduce it): When I run the test with test code covarage, I get a build failed error like the image described below This error is caused by the GPT_CONFIG_VS_0_PB macro that does not contain data in the Gpt_n_PBcfg.h file: #define GPT_CONFIG_VS_0_PB \ Preconditions: Configuration in local file CCOV_ENABLE := ON LDRA_DIR := C:/LDRA_Toolsuite ALLOW_MULTIPLE_INSTANCES:=ON Test Case ID (internal TC that caught the defect) optional: Gpt_TC_FCT_0203(Gpt_TS_C07) Observed behavior: Build failed when running test code coverage Expected behavior: Build is successful when running test code coverage Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: in case of precompile variant this macro shouldn't be generated
ARTD-19050	Bug	[ADC] Disable Aux Trigger from driver and configurator<*> Aux external trigger is not supported on S32G2 and S32R45, S32R41 so it should be disabled from driver and configurator and driver code This is document issue as confirmed by HW team. For more details, refer to attachment
ARTD-19081	Bug	[ETH] The start of index for each fifo read incorrectly<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): follow code driver: !image-2021-11-05-19-22-32-604.png|thumbnail! The start of index of each fifo equal the start of index of previous fifo number of buffers configured for fifo which was calculating. This is incorrectly. It should be he start of index number of buffers configured of previous fifo. Preconditions: Number of fifo > 1 Number of buffers configured in each fifo is different Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The start of fifo's index is incorrectly. Expected behavior: The start of fifo's index need to calculate correctly. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Code should be changed to !image-2021-11-05-19-29-41-691.png|thumbnail!
ARTD-19261	New Feature	[BASE][STUBS][S32CT] Add support for postBuildVariants<*> NewWorkDescription: Add support for postBuildVariants Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update the generic "system" component to provide mechanisms that can enable the creation and usage of postBuildVariants
ARTD-19267	Bug	[LIN] LinNodeType has been generated incorrectly with multi channels setup<*> Detailed description (how to reproduce it): Configuration lin driver with multi channels: Channel 0: Lin node type is Slave. Channel 1: Lin node type is Master. ..... Observed behavior: All LinNodeTypes have been generated to LIN_SLAVE_NODE Expected behavior: LinNodeType of channel 0 is LIN_SLAVE_NODE. LinNodeType of channel 1 is LIN_MASTER_NODE. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-19288	Bug	Flexio Sent lp use float64 variables<*> Detailed description (how to reproduce it): Flexio_Sent_lp.c The function "static Flexio_Sent_lp_StatusType Flexio_Sent_lp_StartTransfer" uses float64 type variable. Line 814 "if(((float64)PulseWidthTick >= SYNC_CAL_TICK_MIN) && ((float64)PulseWidthTick <= SYNC_CAL_TICK_MAX))" Since S32K3 does not support this float type by hardware, it will call div64 library and takes much more execution time. Is it possible to change the float64 to uint32? Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-19312	Bug	[GPT] Do not jump into the Pit_lp_ProcessCommonInterrupt function when using PIT_0_CH_6 channel<*> Detailed description (how to reproduce it): When using interrupt for PIT_0_CH_6 channel, after entering PIT_0_ISR function, we can't jump to Pit_lp_ProcessCommonInterrupt function again because the loop is incorrect. The reason is that the S32R41 platform does not support PIT_RTI Preconditions: Use interrupt of PIT_0_CH_6 channel Test Case ID (internal TC that caught the defect) optional: Gpt_TC_FCT_0007(Gpt_TS_001) Observed behavior: Do not jump into the Pit_lp_ProcessCommonInterrupt function Expected behavior: interrupt works correctly when jumping into Pit_lp_ProcessCommonInterrupt function

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: For S32R41 platform we should change the loop for accuracy
ARTD-19320	Bug	[ETH] Dependency on DEM is still expected when ETH_DEM_EVENT_DETECT = STD_OFF<*> Detailed description (how to reproduce it): Not all inclusions of Dem.h are guarded by macro ETH_DEM_EVENT_DETECT Preconditions: Set EthDisableDemEventDetect = TRUE in configuration Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Build fails if DEM isn't included in the build even though the configuration tells the driver to disable DEM. Expected behavior: Build is passing even if DEM isn't included in the build when configuration tells the driver to disable DEM. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Guard the #include "Dem.h" directives with ETH_DEM_EVENT_DETECT in files Eth.c and Eth_Ipw_Irq.c (their corresponding file version checks)
ARTD-19321	Bug	[S32K3][SENT] A error will be generated when Pause Pulse is enabled.<*> Detailed description (how to reproduce it): In SENT driver, the API Flexio_Sent_Ip_StartTransfer*() is used to measure the PulseWidth of the signal. However, when Pause Pulse is enabled, SUCCESS status will be returned in STATUS_SENT_FAST_SYNC_CALIB phase, not STATUS_SENT_FAST_PAUSE_PULSE phase. Because of that, the Pause Pulse nibble will lead to a error at next STATUS_SENT_FAST_IDLE phase. Customer cannot accept this error. When Pause Pulse is enabled, SUCCESS status should be returned in STATUS_SENT_FAST_PAUSE_PULSE phase. See attached for more information. Preconditions: The Pause Pulse of SENT is enabled Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: When Pause Pulse is enabled, SUCCESS status should be returned in STATUS_SENT_FAST_PAUSE_PULSE phase. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-19326	Bug	[ADC] S32ConfigurationTool: Configuration error when selecting DMA channel for BCTU/CTU FIFO<*> Detailed description (how to reproduce it): [Configuration error when selecting DMA channel for BCTU FIFO, and this problem does not exist in BLN_RTD_4.4_S32K3XX_0.9.0] Preconditions: [Configuration: Tick the "Watermark DMA enable" option, and configure the "Select Dma Channel for Fifo" option] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [Generate error: Value is not available] Expected behavior: [Generate pass] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-19351	Bug	[Adc] S32CT config generate incorrect data of aHwLogicalId<*> Detailed description (how to reproduce it): Code generation for Adc Ipw when configuring only Adc 1 is wrong. Consequently, when using Adc_1, we cannot have result buffer update. Steps: Configure only one Hw unit Adc 1 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Adc_Ipw_PbCfg.c { ADC_IPW_INVALID_LOGICAL_UNIT_ID , ADC_IPW_INVALID_LOGICAL_UNIT_ID , ADC_IPW_INVALID_LOGICAL_UNIT_ID }, / aHwLogicalId / Expected behavior: Adc_Ipw_PbCfg.c { ADC_IPW_INVALID_LOGICAL_UNIT_ID , 1U, ADC_IPW_INVALID_LOGICAL_UNIT_ID }, / aHwLogicalId / Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: [...]
ARTD-19431	New Feature	[RM] XRDC shall allow locking the XRDC registers (implemented on CT)<*> NewWorkDescription: A safety requirement (ARSW-46) requires that XRDC configuration to be lock-able, to prevent other master changing it. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Support locking the XRDC configured registers, as a configuration option. Could be done by having some extra masks or in a separate step at the end of init.
ARTD-19435	Bug	[LIN] Function Lpuart_Lin_lp_AutoBaudCapture can't detect wakeup signal<*> Detailed description (how to reproduce it): After Init driver call function Lpuart_Lin_lp_GoToSleepMode and waiting master node send wakeup signal. But driver can't wakeup when autobaudrate feature enable. Preconditions: In func Lpuart_Lin_lp_AutoBaudCapture, driver only handle case wakeup signal if func Lpuart_Lin_lp_AutoBaudCapture called at least 3 times. But in this case after Init, driver go into SLEEP mode and Lpuart_Lin_lp_AutoBaudCapture never called before. So when received wakeup signal driver only call Lpuart_Lin_lp_AutoBaudCapture 2 time and ignore wakeup signal. !image-2021-11-15-10-59-35-409.png|width=906,height=387! Test Case ID (internal TC that caught the defect) optional: lp_Lpuart_Lin_TC_FCT_0021 Observed behavior: Can't wakeup Expected behavior: Can wakeup Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-19452	Bug	[CRYPTO] HIS_CCM over 20 for two Crypto functions<*> Detailed description (how to reproduce it): Run a bamboo build for S32K3XX 1.0.0 P02 with Coverity enabled, look in Coverity or in the generated HIS report. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Development test case that is run by the bamboo build: Crypto_TS_SharedCfg Observed behavior: Two functions have the CCM above 20: 11250967|HIS_CCM|None|None|Low| Quality|Measured value of CCM metric 21.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|/ARTD-CIC89-2/sources/S32K3XX_4.4/output/eclipse/plugins/Crypto_TS_T40D34M10I0R0/src/Crypto.c|Crypto_KeyElementGet|2808|Intentional|Dismissed|The function will not be split any further in this release to ensure logical consistency. 11485591|HIS_CCM|None|None|Low| Quality|Measured value of CCM metric 21.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|/ARTD-CIC89-2/sources/S32K3XX_4.4/output/eclipse/plugins/Crypto_TS_T40D34M10I0R0/src/Crypto_Hse.c|Crypto_Hse_ExportSymPrivAsymPub|2773|Intentional|Dismissed|The function will not be split any further in this release to ensure logical consistency. Expected behavior: CCM level for all the functions should be below 20. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Rework the functions to have a lower CCM than 20.
ARTD-19455	New Feature	[ICU] fix nightly build for module<*> NewWorkDescription: Nightly build fail because it cannot generate and validate the bswmd file. Fix bug to generate bswmd file. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Check Wkpu_lp_PBcfg.c and remove unneeded code. !image-2021-11-18-10-47-34-262.png|width=820,height=412!
ARTD-19487	Bug	[FLS][S32K3XX] C40 FLS_DATA_BLOCK_END_ADDR<*> FLS_DATA_BLOCK_END_ADDR defined as 0x1003FFFFU (256KB) in C40_lp_CFG.h. However, all the S32K3 parts have 128KB DFlash.
ARTD-19486	New Feature	[BASE][S32CT] Add support to filter generated artifacts and components<*> NewWorkDescription: Add support to filter generated artifacts and components: Invoking the S32DS CLI generator with option "-ExportArgs" will let the user filter the generated artifacts (e.g. "-ExportArgs ecpd" means that only ECPDs will be generated; "-ExportArgs c h" means that only .c and .h files will be generated)

ID	Subtype	Headline and Description
		Invoking the S32DS CLI generator with option "-ExportComponentIds" will let the user filter the generated components (e.g. "-ExportComponentIds Eth_43_GMAC" means that only the generator for Eth_43_GMAC will be invoked) Note: The arguments to both options are case-insensitive (e.g. "eCpD" and "ecpd" are equivalent; "eTh_43_gMac" and "Eth_43_GMAC" are equivalent). The options themselves are optional. If "-ExportArgs" is omitted, no filtering on artifacts is performed. If "-ExportComponentIds" is omitted, no filtering on components is performed. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update System files to support filtering generated artifacts and components.
ARTD-19519	Bug	[S32K3XX][PORT] Pad selection of ADC mux-mode channels does not take effect<*> Detailed description (how to reproduce it): [Pad selection of ADC mux-mode channels does not take effect. For example, no matter in EB or CT configuration interface, when you select PAD46 for ADC0_S9 channel which is driven by PAD1(default) and PAD46, this configuration does not take effect. The reason caused this problem is that the RTD driver won't configure corresponding DCM register bits (DCM.DCMRWF4[2] for ADC0_S9 channel) to select the correct PAD, and this work should be automatically done by the RTD driver instead of manually configuring the register bits by the user.] Preconditions: [Select PAD46 for ADC0_S9 channel which is driven by PAD1(default) and PAD46.] Test Case ID (internal TC that caught the defect) optional: [NA] Observed behavior: [Pad selection of ADC mux-mode channels does not take effect.] Expected behavior: [RTD driver can automatically configure corresponding DCM register bits according to the Pad selection of ADC mux-mode channels.] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [NA]
ARTD-19575	Bug	[PORT] Port driver have to add some Det_reportError function following requirement<*> Detailed description (how to reproduce it): If Det is enabled, some function shall report specify error and return without any other action. Detail: CPR_RTD_00423.port: The function Port_ResetPinMode shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00426.port*: The function Port_SetAsUnusedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00428.port*: The function Port_SetAsUsedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. SWS_Port_00223: The function Port_SetPinMode shall reportPORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Port driver should add some Det_reportError function with specify error following the requirement in Detailed Description.
ARTD-19581	Bug	[SPI][LPSPI] Cannot move received data to Rx buffer if previous channel has RX buffer is NULL in DMA mode<*> Detailed description (how to reproduce it): Cannot move received data to Rx buffer if previous channel has RX buffer is NULL in DMA mode. See attachment email for details. Preconditions: Previous channel using RX buffer is NULL in DMA mode Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Cannot move received data to Rx buffer Expected behavior: Receive data successful Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update driver to update DMA_IP_CH_SET_DESTINATION_SIGNED_OFFSET if previous channel has RX buffer is NULL. Check for TX also in case that previous channel has TX is NULL (transmit default data)
ARTD-19580	Bug	[ICU][S32R41] Don't have Siul2_Icu component in S32DS<*> Detailed description (how to reproduce it): Don't have Siul2_Icu component in S32DS !image-2021-11-18-11-14-07-132.png! Preconditions: N/A

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: lp_Siul2_TS_160 Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-19662	New Feature	[PORT] Allow to configure IMCR with pin as GPIO mode during Port_Init() for S32K3, S32R41, S32ZSE, SJA11XX, SAF85XX ,,"NewWorkDescription: In S32G's BootROM, PF_04 was configured as QSPI_INTA_b, and IMCR[37] was set to 0x2. After that the code jumped to the application where called Port_Init(), with PF_04 was configured as GPIO, and customer expected IMCR[37] would be cleared to 0x0. However, with current implementation of Port driver, Port_Init() doesn't touch IMCR registers with pins configured as GPIO mode. As a result, IMCR[37] was still 0x2, and PF_04 couldn't be used as GPIO mode Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: CE's comment: Since there was a UntouchedIMCR list where user can add pins that they don't want IMCR to be re-configured, my proposal is with the pins configured as GPIO mode in PortContainer, IMCR shall be reset as 0x0. It's better to have an option for user to choose either IMCR would be disabled low or disabled high.
ARTD-19738	Bug	[i2c] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19741	Bug	[lin] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1

ID	Subtype	Headline and Description
		Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19742	Bug	[mcl] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19750	Bug	[pwm] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register

ID	Subtype	Headline and Description
		# Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19756	Bug	[spi] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)

ARTD-19927	Bug	S32K3 SIUL2 ICU code generation issue<*>
		
		Detailed description (how to reproduce it):
		Add an Siul2_Icu component into an S32DS project in the configuration tool and click generate code.
		In the generated file: "Power_Ip_BOARD_InitPeripherals_PBcfg.c"
		const Siul2_Icu_Ip_ChannelConfigType Siul2_Icu_Ip_0_ChannelConfig_PB_BOARD_InitPeripherals[1U] =
		{
		/ brief IcuSiul2Channel_0 /
		{
		/ brief Siul2 HW Module and Channel used by the Icu channel /
		0U,
		/ brief Siul2 Digital Filter enable /
		TRUE,
		/ brief Siul2 Digital Filter value /
		1U,
		/ brief Siul2 request type*/
		SIUL2_ICU_IRQ,
		/ brief Siul2 Edge type*/
		SIUL2_ICU_RISING_EDGE,
		/ brief Callback Pointer /
		NULL_PTR,
		/ brief Notification function /
		&NULL_PTR,
		/ brief Callback Param1*/
		0U
		}
		};
		In this generated structure, the line of "&NULL_PTR" will bring compiling error.
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		[...]
		Expected behavior:
		[...]
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Change the "&NULL_PTR" to be "NULL_PTR"

ARTD-19950	Bug	[adc] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-19991	Bug	[SENT] Sent example should use mcu instead of sys_init and some example descriptions are not correct<*> Detailed description (how to reproduce it): EBT sent example is using sys_init to initial clocking, it should using mcu driver incorrect pin connection for S32K312 and S32K342 example in description Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: EBT sent example is using sys_init to initial clocking incorrect pin connection for S32K312 and S32K342 example in description Expected behavior: Using mcu driver for all example to initial clocking J459 instead of J458 is used to be pin connection Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Using mcu driver for all example to initial clocking J459 instead of J458 is used to be pin connection
ARTD-20018	Bug	[S32K3xx] Version 2.0.0 should be updated to some file .c and .h<*> Step: 1.Create project S32K3xx and attach sdk RTD 2.0.0 2. Open S32CT tool > Update code 3. Open all .c, .h then check Observed behavior: 3. Version 2.0.0 isn't updated to some file as below main.c Siul2_Port_Ip_Cfg.c Siul2_Port_Ip_Cfg.h Expected behavior: 3. Version 2.0.0 is updated
ARTD-20029	Bug	[CAN][HLD-S32CT] This warning 'Issue: CanController_0 should be referred by CanIfCtrlCanCtrlRef' appears even if the controller is referred by CanIf<*> Detailed description (how to reproduce it): Project is created by EBT >import epc files from EBT to S32CT. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Can_TS__CT_115 Observed behavior: !image-2021-11-30-11-48-36-294.png! Expected behavior: No warning appears. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		NA

ARTD-20042	Bug	[S32K3XX] Imprecise bus fault exception in sys_m7_cache_clean() function<*>
		
		Detailed description (how to reproduce it):
		Customer has an issue with system.c from Platform driver on S32K312. The software jumps in an undefined handler (escalated hard fault from bus fault, imprecise) when executing the function sys_m7_cache_clean() at the end of sys_m7_cache_init():
		static void sys_m7_cache_clean(void)
		{
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		S32_SCB->CSSELR = 0U; / select Level 1 data cache /
		ASM_KEYWORD("dsb");
		ccsidr = S32_SCB->CCSIDR;
		sets = (uint32)(CCSIDR_SETS(ccsidr));
		do {
		ways = (uint32)(CCSIDR_WAYS(ccsidr));
		do {
		S32_SCB->DCCISW = (((sets << 5) & (uint32)0x3FE0U)
		((ways << 30) & (uint32)0xC0000000U));
		ASM_KEYWORD("dsb");
		} while (ways != 0U); / within this do while loop imprecise bus fault happens /
		} while(sets != 0U);
		S32_SCB->CSSELR = (uint32)((S32_SCB->CSSELR) 1U);
		S32_SCB->ICIALLU = 0UL;
		ASM_KEYWORD("dsb");
		}
		!image-2021-11-30-12-57-41-450.png!
		!image-2021-11-30-12-57-51-884.png!
		Preconditions:
		N/A
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		Undefined handler (imprecise bus fault) called while executing startup
		Expected behavior:
		No undefined handler (imprecise bus fault) called while executing startup
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Remove the call to sys_m7_cache_clean() from the end of sys_m7_cache_init*() function as follows:
		static void sys_m7_cache_init(void)
		{
		#ifdef D_CACHE_ENABLE
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		/*init Data caches*/
		S32_SCB->CSSELR = 0U; / select Level 1 data cache /
		ASM_KEYWORD("dsb");
		ccsidr = S32_SCB->CCSIDR;
		sets = (uint32)(CCSIDR_SETS(ccsidr));
		do {
		ways = (uint32)(CCSIDR_WAYS(ccsidr));
		do {
		S32_SCB->DCISW = (((sets << SCB_DCISW_SET_Pos) & SCB_DCISW_SET_Msk)
		((ways << SCB_DCISW_WAY_Pos) & SCB_DCISW_WAY_Msk));
		ASM_KEYWORD("dsb");
		} while (ways != 0U);
		} while(sets != 0U);
		ASM_KEYWORD("dsb");
		S32_SCB->CCR = (uint32)SCB_CCR_DC_Msk; / enable D-Cache /
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		#endif
		#ifdef I_CACHE_ENABLE
		/*init Code caches*/
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		S32_SCB->ICIALLU = 0UL; / invalidate I-Cache /
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		S32_SCB->CCR = (uint32)SCB_CCR_IC_Msk; / enable I-Cache /
		ASM_KEYWORD("dsb");
		ASM_KEYWORD("isb");
		#endif
		/*sys_m7_cache_clean();*/ / !!! commented out to solve the issue !!! /
		}
		After commenting out the call of sys_m7_cache_clean() the issue does not happen anymore. Also calling the sys_m7_cache_clean() is very strange as both data and instruction caches are already invalidated and enabled just before that (so there is no need to do it again inside sys_m7_cache_clean()).

ARTD-20043	Bug	[MCL] Compiler error due to missing #ifdef __cplusplus<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		There is generated a compiler error due to missing #ifdef cplusplus } #endif at the end of the following files: Dma_Ip_Cfg_Defines.h Dma_Ip_Cfg_DeviceRegistersV3.h Trgmux_Ip_Cfg_Defines.h Also this code is wrongly placed in Lcu_Ip_DevAssert.h. Preconditions: Using C compiler Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiler error due to missing #ifdef cplusplus Expected behavior: No compiler error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the missing code #ifdef cplusplus } #endif at the end of the following files: Dma_Ip_Cfg_Defines.h Dma_Ip_Cfg_DeviceRegistersV3.h Trgmux_Ip_Cfg_Defines.h Plus also fix the end of Lcu_Ip_DevAssert.h file to be as follows (#ifdef cplusplus moved just before last #endif): #endif / #if (STD_ON == LCU_IP_IS_AVAILABLE) / #ifdef cplusplus } #endif #endif / #ifndef LCU_IP_DEVASSERT_H / Also check all other files whether extern “C” is properly opened and closed.
ARTD-20066	Bug	[ADC] Group sw single continuous without interrupt can not transfer to buffer continuously<*> Detailed description (how to reproduce it): Group sw single continuous without interrupt can not transfer to buffer continuously Preconditions: Group sw single continuous without interrupt DMA transfer Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1408 Adc_TS_013 cfg BetweenDMA Observed behavior: Start group sw single continuous without interrupt Set AN_2 with 5V as out range voltage 0.5 1.5V Read group till E_OK expected time out Set AN_2 with 1V as in range voltage 0.5 1.5V Read group till E_OK expected not time out Real status: buffer is always 0xFFF and not updating Read group till E_OK and timeout occured Expected behavior: Read group till E_OK expected not time out Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-20075	Bug	[RM] XRDC can not rearm PDAC Error Capture register<*> Detailed description (how to reproduce it): Xrdc_Ip_GetDomainIDErrorStatus_Privileged can not rearm PDAC Error Capture register Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Error operate on RECR in DERR_W3_0, DERR_W3_1,DERR_W3_2 Expected behavior: Resets the error capture registers (DERR_W0_d, DERR_W1_d) after rearms instance error capture Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: XRDC_REG_WRITE32(XRDC_DERR_W_ADDR32(u32Instance,XRDC_WORD3,(uint32)u8counter), XRDC_ERROR_RECR_U32); => XRDC_REG_WRITE32(XRDC_DERR_W_ADDR32(u32Instance,XRDC_WORD3,(uint32)(u8counter 16U)), XRDC_ERROR_RECR_U32);
ARTD-20161	Bug	[Clocks Diagram][HSE_CLK]HSE clock need to be limited between 24MHz and 120MHz<*> Detailed description (how to reproduce it): The HSE Firmware is operational when HSE_CLK is between 24MHz and 120MHz, but in the config tools HSE_CLK can be configured to 160Mhz.

ID	Subtype	Headline and Description
		!image-2021-12-03-14-33-14-203.png|width=554,height=217! !image-2021-12-03-14-37-55-331.png! Observed behavior: The observed behavior is currently uncertain, found two cases: 1. The customer project uses config tools and RTD to set HSE_CLK to 160Mhz, causing the program to fail to run, the chip is temporarily secured. 2. The customer configured the HSE clock to 160Mhz through the bare-metal driver written by himself, trig MC_ME "HSE_SWT_RST" flag, even after the configuration is correct, HSE still cannot work， it seems HSE firmware damage. Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check the HSE_CLK after configured
ARTD-20170	New Feature	[RM] Showcase the XRDC and Sema4 locking in examples<*> NewWorkDescription: The XRDC is a complex module and one of the most important ones on the platforms where isolation and virtualization play an important role. Given the difficulty of correctly configuring this module, the XRDC examples (part of RM module) should showcase the XRDC integration with the semaphore module. Requirement source: FAE community, for showcasing a complex topic involved in isolation. Proposed solution optional: Create a new example(preferable) in which you showcase only the XRDC and sema4 integration. lock a region, showcase that you still have read access even without sema4 taken take the sema4, show that you have write now that region the region can be memory (peripheral also if you find any benefit) show that if you do not have the sema4, an error will be reported recover from the error in the same context now force clear the sema4 to highlight this feature also, as it may be needed if the other user is non responsive
ARTD-20214	Bug	[ADC] Build faild when configuring ctu control mode<*> Detailed description (how to reproduce it): Build faild when configuring ctu control mode Preconditions: Configure ctu tab for eq class test AdcEnableCtuControlModeApi is enable Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 46 Observed behavior: Build fail error log: 1. CtuTriggerIndex is 3 but only1 element in CtuHwUnit tab: TARGET:Ctu_Ip_VS_0_PBcfg_c.o STDERR:"e:/S32K1XX/output/S32XX_S32G2XX/adc/Adc_TS_COT_011_cfg46_CORE4/generate_tresos/src/Ctu_Ip_VS_0_PBcfg.c", line 105: error #1981-D: STDERR: empty initializer is non-standard STDERR: }; 2. CtuFifoDmaEn is disable, but CtuDmaFifo0 still in struct Ctu_Ip_FifoConfigType CtuIpResultFifos_VS_0[]: STDERR:"e:/S32K1XX/output/S32XX_S32G2XX/adc/Adc_TS_COT_011_cfg46_CORE4/generate_tresos/src/Ctu_Ip_VS_0_PBcfg.c", line 136: error #20: STDERR: identifier "CtuDmaFifo0" is undefined STDERR: CtuDmaFifo0, / pUserFifoBuffer / STDERR: STDERR: STDERR:"e:/S32K1XX/output/S32XX_S32G2XX/adc/Adc_TS_COT_011_cfg46_CORE4/generate_tresos/src/Ctu_Ip_VS_0_PBcfg.c", line 192: error #28: STDERR: expression must have a constant value STDERR: CtuIpResultFifos_VS_0 / pFifoConfigs / STDERR: Expected behavior: Build done Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-20327	Bug	[CRC] The data in ECVD file different from interface<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: When user add CRC64 custom with polynomial value on S32CT is 0x42F0E1EBA9EA3693, but polynomial value in ECVD file is 0x42F0E1EBA9EA37D8 Expected behavior: Update crc to polynomial value in ECVD file is the same interface Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: N/A
ARTD-20324	Bug	[ADC] Mismatch prototype between driver code and requirements for 3 non-autosar extension APIs<*> Detailed description (how to reproduce it): Mismatch function prototype between driver code and requirements Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Mismatch function prototype between driver code and requirements, see detail in attachment (excel file) Expected behavior: No mismatching Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-20328	Bug	[CAN][S32CT/IPL] Build failed when tranfer type is set to USING DMA but LegacyFIFO is disabled<*> Detailed description (how to reproduce it): Transfer type is set to using_dma but legacy fifo feature is disabled. !image-2021-12-07-19-04-56-139.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Ip_FlexCAN_TS_TRUST_001 Observed behavior: !image-2021-12-07-19-06-47-800.png! Expected behavior: No error at building Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-22018	Bug	[S32K3XX] Implement the WFI errata for CM7 hang<*> Detailed description (how to reproduce it): The CM7 can hang in certain corner-cases upon using WFI instruction (see attached file for more details) Preconditions: see attached file for more details Test Case ID (internal TC that caught the defect) optional: NA {_}*Observed behavior:*{_}unable to wakeup/reattach to M7 core {_}*Expected behavior:*{_}WFI functioning correctly, able to wakeup and re-attach to core anytime there is an interrupt or debug event. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: see attached file for more details implement the proposed workaround in startup file. document this errata in a highly visible place (RTD_S32K3XX_IM and release notes).
ARTD-22027	Bug	[ADC] Incorrect command position in CTU optimization<*> Detailed description (how to reproduce it): When AdcCtuHardwareTriggerOptimization is enabled, the command position in configuration is incorrect in HW groups For example: the Group0 has 3 channel, Group1 has 2 channel, Group0 has 1 channel Then the starting position for G0 pos=0, G1 pos=3, G2 pos=4 But in codegen, the position for G0 pos=0, G1 pos=2, G2 pos=3 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: incorrect CTU/BCTU command position Expected behavior: correct CTU/BCTU command position Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-21725	New Feature	[S32K3 2.0.0] Driver activities for UART<*> Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BD1DC93AE-F154-48B3-8D46-A8F7B0725503%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20SOW.docx&action=default&mobileredirect=true]
ARTD-21882	New Feature	[S32K3 2.0.0] Driver activities for Resource<*>

ID	Subtype	Headline and Description
		Drivers/IPs list in SOW: [see SOW for details|https://nxp1.sharepoint.com/:w:/r/sites/Zebra/_layouts/15/Doc.aspx?sourced oc=%7BD1DC93AE-F154-48B3-8D46-A8F7B0725503%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20S OW.docx&action=default&mobileredirect=true]
ARTD-22269	Bug	[ADC] Remove unused ADC_USER_MODE_REG_PROT_ENABLED and port compiler warning fix<*> Detailed description (how to reproduce it): ADC_USER_MODE_REG_PROT_ENABLED is unused now and need to be removed from codegen Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: ADC_USER_MODE_REG_PROT_ENABLED is unused Expected behavior: not gen ADC_USER_MODE_REG_PROT_ENABLED Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-22288	New Feature	[ETH]Add infix support in the Eth driver<*> NewWorkDescription: Add infix support in the Eth driver Requirement source: Planned activity (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: For having separate and independent namespaces, drivers with the defined multiplicity greater than 1 need to have their name extended with an infix. Steps: Outside of the driver: Add in Base a new MemMap Eth_43_NETC_MemMap.h generated for the new naming Add in Rte new SchM files Schm_Eth_43_NETC,c and Schm_Eth_43_NETC.h generated for the new naming In the driver: Add in the HLD and IPW M4 tags that will be replaced with the infix The files need to be renamed, the types, the functions, etc. Do not rename the types and defines that are specified in Eth_GeneralTypes. Those need to keep their name, as they will be used as defined by all Eth drivers (if more drivers are present in a project) Update the xdm file to change the package name and use the short_name of the driver instead of MODULE_NAME where needed Update the mak file of the driver to rename all files and to propagate the m4_infix_value in all needed files In the tests: Change the xdm configuration for the tests to use the new format Change the mak file of the tests to compile the correct plugin folder Create a wrapper file Eth.h which includes Eth_43_NETC.h and redefines all needed macros, typedefs and functions to point to the newly named entities
ARTD-22309	Bug	[ADC] Adc_Ipw_EndHardwareConv and Adc_Ipw_EndSoftwareConv not used in corner case configuration<*> Detailed description (how to reproduce it): With DMA disabled, SW normal groups with interrupt (no HW normal groups), EOC enabled, Adc Use Hardware Normal Groups disabled: Adc_Ipw_EndHardwareConv not used. Workaround is to enabled AdcUseHardwareNormalGroups, with minor impact on code size. With DMA disabled, HW triggered injected groups (no SW injected groups), EOC enabled, Adc Use Software Injected Group disabled: Adc_Ipw_EndSoftwareConv not used. Workaround is to enable Adc Use Software Injected Group, with minor impact on code size. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Observed behavior: See description Expected behavior: No warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Propose for this release:
ARTD-22352	Bug	S32DS3.4 Pin Tool Configuration for S32K3xx doesn't show 3 external signals per ADC<*> The problem occurs when trying to configure external channels for ADC using a multiplexer. We have 3 output signals per ADC module, in case of ADC0 they are ADC0_MA[0], ADC0_MA[1] and ADC0_MA[2]. The tool however only allows to select mux_output and hence when we attempt to configure the 3 signals, they show an error which tells that there is a conflict. Please see the attached picture.
ARTD-22397	New Feature	[RM] Implement XRDC Gui Mock up for Domain master assignment in the RM Driver<*> The XRDC GUI configurators (Tresos and CT) need to be reviewed to incorporate the feedback from [~nxa14515] and [~nxa21761].

ID	Subtype	Headline and Description
		Update domain configuration follow slide 2&3
ARTD-22454	Bug	[platform] Analysis the consistent between functionalities requirement and driver implementation<*> Situation: During the last minutes of S32K3 1.0.0, we used an owner tool to check the consistent between requirement and source code implementation and found some drivers that have the inconsistent between the functions' requirements and drivers implementation. Something is really to fix in the below scenarios: Miss or redundant parameters. Platform is declared mark for this situation Wrong function name Functions are not expose to Users (in header files) We already fixed in Platform, LIN, MCL, MCU, LIN, SENT, FLS, ADC, SAI drivers. The rests should be analysis and dig into the inconsistent if it is wrong or not. The following 3 categories were found : The functions are declared in "*.h" files of driver code (exported to user) but not included in "ReqExport.txt" file (no requirement are found in Doors > no traceability > no test) The functions are found in "ReqExport.txt" (requirement exists) but the functions are not declared in "*.h" files of driver code (are not present for user) The function name is found in both "ReqExport.txt" and in "*.h" file but there is at least one mismatch on data type, variable name, ... Proposal: With the remaining findings, please to: This ticket should perform after requirement analyis ticket Export all requirement and take a review to conclude the consistent between requirement and implementation. Please take a review on Crucible, the checklist at attachment. In the case there is the needed to update driver or to update requirement, please create a ticket to implement and link to this ticket For each driver, analysis and resolution should be completed with relevant information Reference: Findings from S32K3 1.0.0 release (attachment), as optional Contact SW Testers to provide the latest results for each drivers (it's mandatory input)
ARTD-22537	New Feature	[BASE] Remove release note link in rtd.collateral.release_id.xml file<*> NewWorkDescription: The release notes document link (from Flexera) will be available on RTD Updatesite description !image-2021-12-20-14-48-58-473.png! The release note document file inside Updatesite is no longer exist. So, the old link to release note pushed in itm.<PlatformName>.rtd.collateral.release_id.xml should be removed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-22859	New Feature	Implement XRDC Gui Mock up for Memory region(part 2) in the RM Driver<*> The XRDC GUI configurators (Tresos and CT) need to be reviewed to incorporate the feedback from [~nxa14515] and [~nxa21761]. Add validate check for overlap regions (Start address, end address). 2 regions same memory controller should not overlap address. If yes, raise a warning. using <a:da name="WARNING" type="XPath">
ARTD-22898	New Feature	Implement XRDC Gui Mock up for Memory region(part 3) in the RM Driver<*> The XRDC GUI configurators (Tresos and CT) need to be reviewed to incorporate the feedback from [~nxa14515] and [~nxa21761]. Remove Mrc descriptor field and generate it automatically. Check if configured Mrc is over its number of descriptors.
ARTD-22910	New Feature	[RM] Configure XRDC Sema42 with logical channel instead of hardware sema42 in HLD<*> NewWorkDescription: Feature Xrdc sema42 is using Sema42 hardware to configure in HLD. But Seme42 supports logic channels to configure. Need an update to Xrdc sema42 used logic channels to config !image-2021-12-29-14-04-41-484.png|width=616,height=261! Also, need remove u32XrdcLock}} in define stuct Xrdc_Ip_MemConfigType}} because it's not used Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update interface and codegen for XRDC
ARTD-22902	Bug	[CAN] Can_SetBaudrate still change internal state in case of failure/timeout<*> Detailed description (how to reproduce it): !image-2021-12-29-10-27-41-462.png!

ID	Subtype	Headline and Description
		Can_au16BaudrateIDConfig[Controller]* is being changed unconditionally (without checking eRetVal status => this will cause related api (Can_SetControllerMode will work on unexpected previous config state of {_}*Can_au16BaudrateIDConfig*{_}{_}){_} Please also re-check other similar API Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_1666 Observed behavior: Expected behavior: status of setting api should be checked to make sure not to save non-working configuration, for example, as below expected handler: !image-2021-12-29-10-26-33-630.png! Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-22933	Bug	 [CAN] CAN_BUSOFF_POLLING_SUPPORT is generated differently between S32CT and EB<*> Detailed description (how to reproduce it): Create s32ct / s32k148 project: config CanController_0/ bus-off processing type as POLL config CanController_1/ bus-off processing type as INTERRUPT Make the same settings on EB, then comparing two generated code Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2021-12-31-15-28-51-444.png! Expected behavior: Two generators should generate similar code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-22976	New Feature	 [CAN] implement new timestamp requirements CPR_RTD_00581.can, CPR_RTD_00582.can, CPR_RTD_00583.can, CPR_RTD_00584.can, CPR_RTD_00585.can Part 2 ,,"NewWorkDescription: new requirements need to be implemented: CPR_RTD_00581.can:Service name: Can_GetCurrentTime Syntax: Std_ReturnType Can_GetCurrentTime(uint8 ControllerId, Can_TimeStampType timeStampPtr) Service ID[hex]: 0x13 Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): ControllerId Index of the addresses CAN controller. Parameters (out): timeStampPtr current time stamp Return value: Std_ReturnType E_OK: successful E_NOT_OK: failed Description: Shall return current timestamp for the CAN controller CPR_RTD_00582.can:Service name: Can_EnableEgressTimeStamp Syntax: void Can_EnableEgressTimeStamp (Can_HwHandleType Hth) Service ID[hex]: 0x14 Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): Hth HW-transmit handle used for enabling the time stamp. Description: Shall activate egress time stamping on a dedicated HTH. CPR_RTD_00583.can:Service name: Can_GetEgressTimeStamp Syntax: Std_ReturnType Can_GetEgressTimeStamp (PduIdType TxPduId, Can_HwHandleType Hth, Can_TimeStampType timeStampPtr) Service ID[hex]: 0x15 Sync/Async: Synchronous Reentrancy: Non Reentrant for the same TxPduId. Parameters (in): TxPduId L-PDU handle of CAN L-PDU for returned timestamp Hth HW-transmit handle for the retrieved egress timestamp Parameters (out): timeStampPtr current timestamp Return value: Std_ReturnType E_OK: success E_NOT_OK: failed to read timestamp. Description: Shall read back the egress timestamp on a dedicated message object. This function has to be called within the TxConfirmation() function. CPR_RTD_00584.can:Service name: Can_GetIngressTimeStamp Syntax: Std_ReturnType Can_GetIngressTimeStamp (

ID	Subtype	Headline and Description
		Can_HwHandleType Hrh, Can_TimeStampType timeStampPtr) Service ID[hex]: 0x16 Sync/Async: Synchronous Reentrancy: Non Reentrant for the same Hrh, Reentrant for different Hrh Parameters (in): Hrh HW-receive handle for the retrieved ingress timestamp Parameters (out): timeStampPtr current time stamp Return value: Std_ReturnType E_OK: success E_NOT_OK: failed to read time stamp. Description: Shall read back the ingress timestamp on a dedicated message object and needs to be called within the RxIndication() function. CPR_RTD_00585.can:Name: CanGlobalTimeSupport Parent Container CanGeneral Description Shall enable/disable the Global Time APIs used when hardware timestamping is supported by CAN controller. Multiplicity 1 Type EcucBooleanParamDef Default value – Post-Build Variant Value false Value Configuration Class Pre-compile time X All Variants Link time – Post-build time – Scope / Dependency scope: local Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-22979	Bug	[PORT]Port.h: MemMap include missing<*> Detailed description (how to reproduce it): In the file Port.h a memory section is defined in the lines 317 and 321 by PORT_START_SEC_CONFIG_DATA_UNSPECIFIED and PORT_STOP_SEC_CONFIG_DATA_UNSPECIFIED. But in both cases, the include of the Port_MemMap.h is missing. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In customer's integrator environment, their MemMap is checking the correctness of the memory sections which leads to compiling errors in this case. Expected behavior: Adding the include of the Port_MemMap.h within corresponding section, in order to fix the compiling errors in customer's integrator environment. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23025	Bug	[port] Update missing exclusive areas in BSWMD for S32K3, S32ZSE, SJA11XX ,,"Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with ""Fixed No Action Taken"". Otherwise, proceed with the solutions given in the ""Proposed solution"" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the ""Expected behavior"" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml

ID	Subtype	Headline and Description
		Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-23038	Bug	[RM] Missing some peripherals definition when using multi variant<*> Detailed description (how to reproduce it): With Multivariant, when config 2 Variant with different Configurations, Code Build Fail Preconditions: Enable multi variant configuration, at least 2 variant: VS0 and VS1 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Some definition of peripherals is missing when using multi variant configuration because some peripherals are configuration in VS0 but not in VS0 Expected behavior: Definition of peripherals are generated for all variant Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Generate all definition of all peripherals from resource instead of configuration
ARTD-23039	Bug	[dio] Update missing exclusive areas in BSWMD for SJA1XX, S32K3XX and STRXOneChip ,,"Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with ""Fixed No Action Taken"". Otherwise, proceed with the solutions given in the ""Proposed solution"" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the ""Expected behavior"" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in ""exclusive_areas_to_be_defined_in_bsw_scheduler.dox"" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-23045	Bug	[I2c] Fix different short name node in ecvd file<*> Detailed description (how to reproduce it): [...] Fix different in ecvd file on LPi2c DS !image-2022-01-07-16-18-09-660.png! On HLD DS !image-2022-01-10-10-25-24-930.png!!image-2022-01-10-10-26-05-981.png!!image-2022-01-10-10-29-51-225.png!! image-2022-01-10-10-30-45-638.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23087	New Feature	[FLS] Make the CRC check optional<*> NewWorkDescription:

ID	Subtype	Headline and Description
		The CRC config check happening at Fls_Init takes 6ms, which is not needed as the image has been anyway authenticated. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Make the CRC check optional, with default to OFF, disabled. Document this behavior in the manual, the reason for this change and when this check is needed.
ARTD-23102	Bug	[LIN] Function interface don't matching with function API in driver<*> Detailed description (how to reproduce it): Function interface don't matching with function API in driver Preconditions: !image-2022-01-11-14-58-20-399.png! Test Case ID (internal TC that caught the defect) optional: !image-2022-01-11-14-58-25-115.png! Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23108	Bug	[I2s] Flexio supports only 1 Master or Slave channel<*> On K1, Flexio has 4 shifters/timers. So it can support max 2 masters or 1 slave per derivatives. For K3 it will be higher since it has 8 shifters/timers But configurator support max 1 master or 1 slave for K1. This requires some changes in codegen Fix Master and Slave cannt work if the first resource index number is odd Add devtest to verify the new feature with multiple flexio configuration on K3 Remove I2sNumLogicChn node from configurator
ARTD-23127	Bug	[ADC] Build fail: "unresolved symbols: EndConversionNotification" when configuring transfer types are different between multi VS ,,"Detailed description (how to reproduce it): Build fail: ""unresolved symbols: EndConversionNotification"" when configuring transfer types are different between multi VS Preconditions: VS_0: ADC0: AdcTransferType: ADC_INTERRUPT ADC1: AdcTransferType: ADC_DMA VS_1: ADC0: AdcTransferType: ADC_DMA ADC1: AdcTransferType: ADC_INTERRUPT Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1601 Adc_TS_023 cfg 3VS_PC_DMA Observed behavior: Build fail log: [elxr] (error #412) unresolved symbols: 2 Adc_Ipw_Adc1EndConversionNotification from Adc_Ip_VS_1_PBcfg_c.o Adc_Ipw_Adc0DmaTransferCompleteNotification from Dma_Ip_VS_1_PBcfg_c.o Only ADC_UNIT_1_DMA_TRANSFER_USED and ADC_UNIT_0_END_CONVERSION_NOTIF_USED define in ADC_CfgDefines.h Expected behavior: Build done Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23161	Bug	[SPI] Spi_SyncTransmit with length is 0 not Timeout erorr<*> Detailed description (how to reproduce it): Sync Transmit 1 job / 1 channel with 0 lengh EB. Lpspi_Ip_SyncTransmit: State->RxIndex = State->ExpectedFifoReads =0 not into while loop so not check timeout and return LPSPI_IP_IDLE !image-2022-01-14-16-12-26-000.png|thumbnail! Preconditions: Sync Transmit 1 job / 1 channel with 0 lengh EB: Spi_SetupEB(SpiConf_SpiChannel_007, Spi_TestDataTx[0], Spi_TestDataRx[0], 0) !image-2022-01-14-16-17-47-639.png|thumbnail! Test Case ID (internal TC that caught the defect) optional: Spi_TC_PER_1000 Observed behavior: Lpspi_Ip_SyncTransmit return LPSPI_IP_IDLE Spi_SyncTransmit return E_OK Expected behavior: Lpspi_Ip_SyncTransmit return LPSPI_IP_TIMEOUT Spi_SyncTransmit return E_NOT_OK Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-23199	Bug	[BASE][S32CT] ECVD files containing INDEX elements don't pass the XSD validation<*> Detailed description (how to reproduce it): Generate the ECVD file of a component containing a setting that defines a "requiresIndex" option. Validate the generated ECVD file against the XSD. Preconditions: ECVD file containing an INDEX element Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: ECVD files containing INDEX elements don't pass the validation check of the schema definition (AUTOSAR_00046.xsd) Expected behavior: ECVD files containing INDEX elements pass the validation check of the schema definition (AUTOSAR_00046.xsd) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: INDEX elements should not be generated in the middle of another group's sequence. In particular, for ECUC-CONTAINER-VALUE, the INDEX element shall be placed between SHORT-NAME and DEFINITION-REF elements.
ARTD-23261	Bug	[ADC] Import ECVD with errors from S32ConfigurationTool to Tresos configurator<*> Detailed description (how to reproduce it): [ADC] Import ECVD with errors from S32CT to EBT Steps: # Create new project wizard on S32DS and add component Adc # Generate ECVD for Adc component # Create new project wizard on EBT and add component Adc # Import ECVD and enable auto mapping # Run importer # VERIFICATION_POINT: Run importer without error, no error on EBT project => FAIL !image-2022-01-18-14-50-14-333.png! Workaround: replace AdcUserCfg to Adc in ecvd file !image-2022-01-18-14-54-12-843.png! Preconditions: Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_003 Observed behavior: Expected behavior: Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23275	Bug	[UART] - Build fail on CT IP driver when adding a callback parameter<*> Detailed description (how to reproduce it): Import any IP uart driver CT component in S32DS. Configure a callback parameter. Generate the configuration files. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is a build fail on this configuration Expected behavior: Analyze the Uart Callback Parameter usage. Define a way to define/declare the callback in parameter. Fix build error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23291	Bug	[WDG] Generate fail ECVD for Wdg_43_Instance1 on S32DS<*> Detailed description (how to reproduce it): Step 1: Custom tool [^validate_ip_ecpd.pl] Step 2: Update file [^plugin.xml] Step 3: Update [^Wdg_TS_COT_005.mak] file Step 4: clean generate Wdg_TS_COT_005 CFG_SETS = s32k148_lqfp176 Step 5: Compare all files in original_configuration folder with new_configuration folder Step 6: Import Wdg_43_Instance1.epc at path: " ...\output\S32K1XX_S32K148\wdg \Wdg_TS_COT_005_cfgs32k148_lqfp176\generate_s32ct\output " into S32DS Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Wdg_43_Instance1.ecpd not matching between EB and CT !image-2022-01-19-16-12-00-689.png|width=1042,height=151! Unable to generate .c and .h files related to Wdg_43_instance1 for EB !image-2022-01-19-16-14-39-466.png|width=972,height=221! Error when importing epc file into S32DS !image-2022-01-19-16-13-37-326.png|width=644,height=370! Expected behavior:

ID	Subtype	Headline and Description
		Generate ecvd successfully for Wdg_43_Instance1 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23295	Bug	[ICU][S32K3XX] when configuring eMios channel using masterbus, error in DS IPL ,,"Detailed description (how to reproduce it): When configuring eMios channel using CounterBus in ICU there is an error in DS IPL: In Peripheral Emios_Mcl_Ip -At General Configuration Tab, put the check to “Enable Emios Common Support” At Emios Common Tab, Select MCB_UP_COUNTER to “Master Bus Mode Type” and Set 65535 to “Default Period” and . In Peripheral Emios_Icu At IcuHwInterruptConfigList tab of IcuConfigSet Tab, Enable EMIOS_0_CH_0 At IcueMios Tab of IcuConfigSet Tab, select EMIOS_ICU_BUS_DIVERSE to “IcuEmiosBusSelect” and Select following to “IcuEmiosBusRef”. /Emios_Mcl_Ip_1/EmiosMcl/EmiosCommon_0/EMIOS_0_MasteBus0 pls see attached files Preconditions: use ICU component with configuration for Emios channels that need Couter Bus. Prepare the MCL side settings and try to generate code. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Error issued on generation Expected behavior: No error on generation Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: please see analysis tab
ARTD-23328	Bug	[PORT] Disable the configuration of CommonPublishedInformation container in S32DS<*> Detailed description (how to reproduce it): In S32CT, Port driver still allows user to config all the parameters in CommonPublishedInformation container. It will violate the Autosar expectation. Please refer General Specification of Basic Software Modules AUTOSAR CP Release 4.4.0 documentaion chapter 10.3Published Information Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: Port driver disables the configuration of that container in S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23329	Bug	[DIO] Disable the configuration of CommonPublishedInformation container in S32DS<*> Detailed description (how to reproduce it): In S32CT, Port driver still allows user to config all the parameters in CommonPublishedInformation container. It will violate the Autosar expectation. Please refer General Specification of Basic Software Modules AUTOSAR CP Release 4.4.0 documentaion chapter 10.3Published Information Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: Port driver disables the configuration of that container in S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23332	Bug	[CAN] redundant check pState->mbs[u32MbIdx].isPolling inside FlexCAN_IRQHandlerTxMB<*> Detailed description (how to reproduce it): [...] Preconditions: analysis ccov report (MCDC tab) !image-2022-01-21-14-05-50-639.png|thumbnail! Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: redundant check causes uncovered code in MCDC report !image-2022-01-21-14-12-20-287.png|thumbnail! Expected behavior: analysis redundant code Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: N/A
ARTD-23347	Bug	[CAN] Driver is not compiling when using INFIX<*> Detailed description (how to reproduce it): Driver is not compiling when using INFIX. There are multiple variables that are infixed in some of the places, not in all places. There are 2 methods of adding infix using M4, it is almost impossible to keep track of the infix method based on the file. There is no INFIX in the IP DRIVER. Flex LLCE will use the IP driver data structures in the interface, so it can't compile along FlexLLCE driver on the host side. Preconditions: Generate the driver using infix Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not compiling {_}*Expected behavior:*{_}To compile Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix Compile error. Stick to only one way of adding infix. Add INFIX to IP driver.
ARTD-23359	Bug	[I2C] Wrong variable of I2c_ErrorCallback<*> Detailed description (how to reproduce it): Project: C:\NXP\SW32_RTD_4.4_3.0.0\eclipse\plugins\I2c_TS_T40D11M30I0R0\examples\EBT \I2c_HLD_Transfer_S32G274A_M7 EB treos: DMA was in disable state. Disable I2c_Callback, Enable I2c_ErrorCallback. !image-2022-01-24-11-15-02-761.png|width=515,height=330! I2c_Ipw.c : !image-2022-01-24-11-16-52-969.png|width=878,height=103! I2C_EVENT_DMA_TRANSFER_ERROR_MASTER could not be found in I2c_Ipw.c* file result to building failed. But I found I2C_MASTER_EVENT_DMA_TRANSFER_ERROR in I2c_Ip_Callbacks.h. I2c_Ip_Callbacks.h : !image-2022-01-24-11-42-53-783.png|width=510,height=131! So, I doubt it should be "I2C_MASTER_EVENT_DMA_TRANSFER_ERROR" instead of "I2C_EVENT_DMA_TRANSFER_ERROR_MASTER" in I2c_Ipw.c. Please help to check it. Thanks. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23375	Bug	[LIN] The driver doesn't report error if PID is set incorrectly by user<*> Detailed description (how to reproduce it): A LIN frame was configured with an incorrect PID value, e.g. PID=0x10. However, the driver doesn't report any error in Lin_SendFrame() function, although the frame couldn't be sent at all. Preconditions: A LIN frame was configured with an incorrect PID value. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The LIN driver doesn't report any error in Lin_SendFrame() function Expected behavior: The LIN driver shall report error in Lin_SendFrame() function in case PID was incorrect set by user. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CE's comment: When going down the Lin_SendFrame() path it was seen that the parity was set incorrectly, so Lin_Ipw_CheckFrameInfo() was returning E_NOT_OK. However, TempReturn does not change from initialization in Lin_Ipw_SendFrame(), so eventually Lin_SendFrame() will return E_OK. It was a typical issue of missing “else” condition in the implementation. A possible workaround would be adding the missing “else” condition in the “if” statement. Something like: !image-2022-01-25-14-07-05-171.png!
ARTD-23384	Bug	[WDG]There are some data types mismatch between EBT and CT<*> There are some value mismatches between EBT and CT. Please see for example the attached file. [VALIDATION] Mismatch between the types of EPD:WdgClockValue (ECUC-INTEGER-PARAM-DEF) and CT:WdgClockValue (info) [VALIDATION] EPD:WdgEcucPartitionRef has multiplicity, but CT:WdgEcucPartitionRef is not an array [VALIDATION] EPD:WdgExternalConfiguration has multiplicity, but CT:WdgExternalConfiguration is not an array [VALIDATION] EPD:WdgExternalContainerRef has multiplicity, but CT:WdgExternalContainerRef is not an array Verify EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams .microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-

ID	Subtype	Headline and Description
		ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation
ARTD-23401	Bug	[Gpt] Emios ChannelTickFrequency need update formula<*> Detailed description (how to reproduce it): there are two UC, with different Pre-scaler (16 vs 1). Based on this, the corresponding Gpt channel for EmiosChannel_1 should be 16 times the corresponding GPT channel for EmiosChannel_0. However, both of these GPT channels are having equal clock frequency, after automatically calculated by EB GUI. please see the picture for more details Preconditions: configuration gptEmios same instance have channel with different prescaler. Test Case ID (internal TC that caught the defect) optional: Gpt_TS_001 Observed behavior: Prescaler of emios channels are different but having same clock frequency, after automatically calculated by EB GUI. Check also s32 DesignStudio. Expected behavior: Correct Calculate tick frequency Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: correct Calculate tick frequency
ARTD-23414	Bug	[dio] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23417	Bug	[fee] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23425	Bug	[lin] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23433	Bug	[port] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23438	Bug	[sent] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23442	Bug	[uart] [S32CT] Incorrect enable attributes for ConfigTimeSupport fields<*> Detailed description (how to reproduce it): Manually check the ConfigTimeSupport fields of the S32CT component / template Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: POST_BUILD_VARIANT_USED has enable="false" IMPLEMENTATION_CONFIG_VARIANT has enable="false" Expected behavior: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true"). Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: POST_BUILD_VARIANT_USED has enable="false" if and only if postBuildVariantSupport="false" in the config set's options_expr. IMPLEMENTATION_CONFIG_VARIANT has enable="true" or no enable attribute (which is equivalent to enable="true").
ARTD-23452	Bug	[S32K3][SENT] There are some issues related to Polling mode of SENT<*> Detailed description (how to reproduce it): {*}Issues 1{*}: Serials (Slow) Message cannot be received normally in in case of multi-channel receiving. {*}Issues 2{*}: The Error Notification of different channels seems to be called incorrectly by each other occasionally. {*}Issues 3{*}: When there are multiple channels and Sent_GetSerialMsgData(), which will open interrupt of SENT, is used, if the other edge of a channel comes during the ISR of SENT, the second flag bit triggered by the latter edge may be cleared, resulting in missing an edge. {*}Issues 4{*}: In Sent_GetSerialMsgData(), it is not feasible to process multi-channel data serially, because the buffer of the latter channels are prone to overflow. {*}Issues 5{*}: When reprocessing data, there is a problem with the buffer index continuation. I found some workarounds which is uploaded within the attached Email. I modified some source code of SENT low level driver which can preliminarily solve these issues I mentioned above as I tested, and {+}*just for your reference*{+}. Preconditions: Set SENT work at {+}*Polling mode*{+}, and use Sent_GetFastChannelMsgData(), Sent_GetSerialChannelMsgData(), Sent_GetFastMsgData() and Sent_GetSerialMsgData() to receive multi-sent signals (in my testing it's two SENT channels), respectively. The error notifications of fast and slow message also should be enabled. Test Case ID (internal TC that caught the defect) optional: [...]

ID	Subtype	Headline and Description
		Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23453	New Feature	[S32K3][SENT] Expand the range of Sent Tick Length to less than 3 us.<*> NewWorkDescription: From customer NASN, the Sent Tick Length of their sensor is about 1.65 us that is less than smallest standard tick length 3 us. But obviously the FlexIO module can realize such a Tick Length, so it is better to expand the feature of SENT to cover more situation. Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-23495	Bug	[CAN] s32k342 only support 4 controllers<*> Detailed description (how to reproduce it): s32ct for K342 show more than 4 controllers !image-2022-01-28-11-06-18-789.png|thumbnail! it may come from base component Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: problem in registers.xml file of base module Expected behavior: s32k342 only support 4 controllers Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23518	New Feature	[ETH] Add support for 200Mbps MII on K3<*> NewWorkDescription: According to the latest S32K3 RM & DS, EMAC can work with an overclocked MII at 50 MHz TX/RX_CLK and 200Mbps data rate. Requirement source: S32K3 Reference Manual Rev4 Draft A & Data Sheet Rev 3 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update EthCtrlMacLayerSpeed and the constraints of EthCtrlConfigShaper to handle 200M in MII.
ARTD-23559	Bug	[ITG] [Uart] HLD Transmit and Receive functions need to check both receive and transmit status for reporting det error<*> Detailed description (how to reproduce it): This ticket has been cloned from https://jira.sw.nxp.com/browse/ARTD-17018. In the https://jira.sw.nxp.com/browse/ARTD-19289 the checking on both transmission and reception on HLD for busy channel has been removed because it is not the correct approach on the loopback mode. Due to missing information on the ARTD-17018, we cannot figure out if the both operations checkins are necessary. What we need to do in this ticket bug is analyze if the updates are impacted the other functionality. If the impact exists, update the code in the way that driver works correctly both on internal loopback and normal mode. Another analysis required is that: is the last bug impacting all the platforms? If yes, then let's update the bug according If no, then let's update the code accordingly (maybe an update on the generic file is not correct). Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23581	Bug	[S32K1XX] [Crypto] Missing field CommonPublishedInformation in ECVD file of HLD<*> Detailed description (how to reproduce it): When config HL layer on S32DS , ECVD file missing fied " CommonPublishedInformation" Test Case ID (internal TC that caught the defect) optional: Crypto_TS_COT_007 Observed behavior: When config HL layer on S32DS , ECVD file missing field " CommonPublishedInformation", see detail at attachments site

ID	Subtype	Headline and Description
		Expected behavior: When config HL layer on S32DS, ECVD file have all field Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23609	Bug	[Uart] ECPD: Difference EPC from EBT to CT<*> Detailed description (how to reproduce it): [ECVD files which are generated by EBT and CT have difference as picture !image-2022-02-09-14-41-52-843.png|thumbnail! !image-2022-02-09-14-42-19-290.png|thumbnail!] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Uart_TS_ECPD_01 Observed behavior: NA Expected behavior: ECVD between EBT and CT must be same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-23612	Bug	[MCL] DMA Enable Start option removed for DMA Transfer configuration<*> Changing Enable Start in the configuration tool does not change the generated structure !image-2022-02-09-10-02-10-091.png|thumbnail! !image-2022-02-09-10-02-45-778.png|thumbnail!
ARTD-23625	Bug	[CAN] out-of-range access when CAN_MAX_PARTITIONS < coreid value / multicore platforms<*> Detailed description (how to reproduce it): Create s32k324 project Enable multicore Configure only 1 partition (EcucPartition_0), and mapping it to core value 6 (or > 1) => review the value of CAN_MAX_PARTITIONS Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: review Observed behavior: detail in attachment Expected behavior: out-of-range access should be eliminated Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23630	Bug	[CAN] Driver is not compiling when using INFIX check on S32CT<*> Detailed description (how to reproduce it): Driver is not compiling when using INFIX. There are multiple variables that are infixed in some of the places, not in all places. There are 2 methods of adding infix using M4, it is almost impossible to keep track of the infix method based on the file. There is no INFIX in the IP DRIVER. Flex LLCE will use the IP driver data structures in the interface, so it can't compile along FlexLLCE driver on the host side. Preconditions: Generate the driver using infix Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not compiling {_}*Expected behavior:*{_}To compile Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix Compile error. Stick to only one way of adding infix. Add INFIX to IP driver.
ARTD-23643	Bug	[PORT] Inconsistent file name and component references<*> Detailed description (how to reproduce it): Inconsistent casing between the driver file names and the references from CT components. This makes the build/generate stage fail on Linux environments which are case sensitive. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...]

ID	Subtype	Headline and Description
		Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check and ensure all file names and the places where they are referenced, will use the exact same case. See the attached email for more details.
ARTD-23682	New Feature	[PORT] Change the define names to not contain derivatives name<*> NewWorkDescription: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/port/pull-requests/410/overview?commentId=1104467] [Radu-Andrei Brasoveanu|https://bitbucket.sw.nxp.com/users/nxa19269] i would advise in creating a follow up ticket for entire code and changing the define names to not contain derivatives name. more suitable will be to use something like: FEATURE_PORT_CI_PORT_IP_PCR_MUXING}} Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Change the define names to not contain derivatives name.
ARTD-23704	Bug	[PWM] Long execution time of mc related api<*> Detailed description (how to reproduce it): 4 Motor control(MC)examples were created to test RTD deployment in the most common mc use cases : All examples were created using Low level API: MCSPTE1AK344_BLDC_6Step_hall_ll MCSPTE1AK344_BLDC_6Step_sensorless_ll MCSPTE1AK344_PMSM_FOC_1Sh_ll MCSPTE1AK344_PMSM_FOC_3Sh_ll as well as Autosar API: MCSPTE1AK344_BLDC_6step_hall_as_tr MCSPTE1AK344_BLDC_6Step_sensorless_as_tr MCSPTE1AK344_PMSM_FOC_1Sh_as_tr MCSPTE1AK344_PMSM_FOC_3Sh_as_tr Examples with Autosar API were tested with RTD Beta release (they are being ported to RTM release) Examples with Low Level API has been tested with RTD RTM release. Examples based on Beta release can be found here : [https://nxp1.sharepoint.com/teams/8_8/Shared%20Documents/Forms/AllItems.aspx?RootFolder=%2Fteams%2F8%5F8%2FShared%20Documents%2FGPIS%2F2%29%20GPIS%20Solutions%2F1%29%2E%20Motor%20Control%2FS32K3%2FSW%20example%20%2D%20RTD&FolderCTID=0x012000AA56F78ADAFAF34494EE7E329455794F&View=%7B2A8302C6%2DEA4B%2D4B43%2DA84E%2D646706AB5F7D%7D] Examples based on RTM release can be sent on demand. Note: TCM was not used for RTD functions, Caches were enabled. Execution time of RTD functions was measured using systic timer when motor was spinning at 1000 rpm. Worst-case was captured during 5 minutes window. In case of any question about methodology, project settings or if any additional information is needed please do not hesitate to contact me: tomas.fedor@nxp.com Observed behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5Ij0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Execution time of following API was too long: Emios_Pwm, Emios_Mcl, Adc_Sar_Ip, Bctu_Ip, Lcu_Ip, Emios_Gpt Adc, Pwm, Mcl, Gpt Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Following scenarios within tested examples were identified as the most critical (items are ordered according the priority) 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) MCSPTE1AK344_PMSM_FOC_1Sh_ll & MCSPTE1AK344_PMSM_FOC_1Sh_as_tr In this scenario we have to update 9 channels (if we considered frequency wobbling we would have to update also 2 time base channels). The worst measured execution time of this action was Non Autosar: Measured in application: 31.275 us Calculated from worst-cases of particular functions: 52.23375 us Autosar : Calculated from worst-cases of particular functions: 74.45 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab PWM and Trigger update in PMSM 2) ADC reading and list configuration. There are various caseses across the examples: Execution tine was 2.1375us 4.275us Changing list of conversions 1.84375us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab ADC reading and list config 3)LCU:

ID	Subtype	Headline and Description
		Lcu_Ip_SetSyncOutputEnable 2.8us Mcl_SetLcuSyncOutputEnable 3.1125us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx 4)Timer: Emios_Gpt_Ip_StopTimer 1.15625 us Emios_Gpt_Ip_StartTimer 2.85625 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Expected behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5lj0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Location: Collaboration with RTD team\Motor_control_req_test.xlsx list of all discussed requirements Location: Collaboration with RTD team\jira_ticket_execution_time\MC_REQ_0039.pptx defined requirement Location: Collaboration with RTDteam\jira_ticket_execution_time\MC_REQ_0039_testing_RTM.pptx tested requirement 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) The same action using bare metal approach takes less than 2us{color}. We should get to this number as much as possible. 2) ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. 3) LCU: The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. It is important when we want to disable output. 4) Timer: ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. StopTimer/StartTimer functionality is a push button action. Proposed solution optional: Any solution addressing this issue is welcomed. Just it is necessary to cover Non-Autosar as well as Autosar part. I would follow this principle: We need fast API for registers : Emios UC A, UC B, UC Counter n, Output Update Disable (OUDIS) Modes: OPWMCB, OPWMB,MCB,PEC ADC: Precision Input n Conversion Data (PCDR0 PCDR7) Standard Input n Conversion Data (ICDR0 ICDR23) External Input n Conversion Data (ECDR0 ECDR31) BCTU FIFO Result Data (FIFO1DR FIFO2DR) Trigger Configuration (TRGCFG_0 TRGCFG_71) ADCn Result Data (ADC0DR ADC2DR) LCU Software Override Value (SWVALUE) Overridden Inputs (SWOUT) Output Enable (OUTEN) Discussed potential solutions: Update of the existing API in Existing drivers: This option was discussed in ARTD-14125 and ARTD-14126 but there wasn't significant improvement of the execution time. Adding new API to existing drivers: New specialized functions which are closer to registers/peripheral (less abstraction). Note/idea: Channel role is constant during runtime so macro dispatcher could be considered like in example: #define EMIOS_ChannelWriteA_(module, ch, a) \ EMIOS_##module.A##ch.R = (uint16_t)a Adding new special driver for MC (Autosar as well as non autosar).
ARTD-23706	Bug	 [GPT] Long execution time of mc related api<*> Detailed description (how to reproduce it): 4 Motor control(MC)examples were created to test RTD deployment in the most common mc use cases : All examples were created using Low level API: MCSPTE1AK344_BLDC_6Step_hall_ll MCSPTE1AK344_BLDC_6Step_sensorless_ll MCSPTE1AK344_PMSM_FOC_1Sh_ll MCSPTE1AK344_PMSM_FOC_3Sh_ll as well as Autosar API: MCSPTE1AK344_BLDC_6step_hall_as_tr MCSPTE1AK344_BLDC_6Step_sensorless_as_tr MCSPTE1AK344_PMSM_FOC_1Sh_as_tr MCSPTE1AK344_PMSM_FOC_3Sh_as_tr Examples with Autosar API were tested with RTD Beta release (they are being ported to RTM release) Examples with Low Level API has been tested with RTD RTM release. Examples based on Beta release can be found here :

ID	Subtype	Headline and Description
		[https://nxp1.sharepoint.com/teams/8_8/Shared%20Documents/Forms/AllItems.aspx?RootFolder=%2Fteams%2F8%5F8%2FShared%20Documents%2FGPIS%2F2%29%20GPIS%20Solutions%2F1%29%2E%20Motor%20Control%2FS32K3%2FSW%20example%20%2D%20RTD&FolderCTID=0x012000AA56F78ADAFAF34494EE7E329455794F&View=%7B2A8302C6%2DEA4B%2D4B43%2DA84E%2D646706AB5F7D%7D] Examples based on RTM release can be sent on demand. Note: TCM was not used for RTD functions, Caches were enabled. Execution time of RTD functions was measured using systic timer when motor was spinning at 1000 rpm. Worst-case was captured during 5 minutes window. In case of any question about methodology, project settings or if any additional information is needed please do not hesitate to contact me: tomas.fedor@nxp.com Observed behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5Ij0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Execution time of following API was too long: Emios_Pwm, Emios_Mcl, Adc_Sar_Ip, Bctu_Ip, Lcu_Ip, Emios_Gpt Adc, Pwm, Mcl, Gpt Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Following scenarios within tested examples were identified as the most critical (items are ordered according the priority) 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) MCSPTE1AK344_PMSM_FOC_1Sh_ll & MCSPTE1AK344_PMSM_FOC_1Sh_as_tr In this scenario we have to update 9 channels (if we considered frequency wobbling we would have to update also 2 time base channels). The worst measured execution time of this action was Non Autosar: Measured in application: 31.275 us Calculated from worst-cases of particular functions: 52.23375 us Autosar : Calculated from worst-cases of particular functions: 74.45 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab PWM and Trigger update in PMSM 2) ADC reading and list configuration. There are various caseses across the examples: Execution tine was 2.1375us 4.275us Changing list of conversions 1.84375us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx: tab ADC reading and list config 3)LCU: Lcu_Ip_SetSyncOutputEnable 2.8us Mcl_SetLcuSyncOutputEnable 3.1125us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx 4)Timer: Emios_Gpt_Ip_StopTimer 1.15625 us Emios_Gpt_Ip_StartTimer 2.85625 us Location: Collaboration with RTD team\jira_ticket_execution_time\api_testing.xlsx Expected behavior: All details about collaboration with RTD team can be found here: [https://nxp1-my.sharepoint.com/:f:/g/personal/tomas_fedor_nxp_com/EhB3sgULJt5Ij0YHzEFJN-sBr3dEPgPsgKASAD8qM-N4zA?e=7Js0Xu] Location: Collaboration with RTD team\Motor_control_req_test.xlsx list of all discussed requirements Location: Collaboration with RTD team\jira_ticket_execution_time\MC_REQ_0039.pptx defined requirement Location: Collaboration with RTDteam\jira_ticket_execution_time\MC_REQ_0039_testing_RTM.pptx tested requirement 1) PWM and Trigger update in PMSM singleshunt application (Highest priority) The same action using bare metal approach takes less than 2us{color}. We should get to this number as much as possible. 2) ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. 3) LCU: The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. It is important when we want to disable output. 4) Timer: ADC reading and list configuration. The same action using bare metal approach takes less than 1us{color}.We should get to this number as much as possible. StopTimer/StartTimer functionality is a push button action. Proposed solution optional: Any solution addressing this issue is welcomed. Just it is necessary to cover Non-Autosar as well as Autosar part. I would follow this principle: We need fast API for registers : Emios UC A, UC B, UC Counter n, Output Update Disable (OUDIS) Modes: OPWMCB, OPWMB,MCB,PEC ADC: Precision Input n Conversion Data (PCDR0 PCDR7)

ID	Subtype	Headline and Description
		Standard Input n Conversion Data (ICDR0 ICDR23) External Input n Conversion Data (ECDR0 ECDR31) BCTU FIFO Result Data (FIFO1DR FIFO2DR) Trigger Configuration (TRGCFG_0 TRGCFG_71) ADCn Result Data (ADC0DR ADC2DR) LCU Software Override Value (SWVALUE) Overridden Inputs (SWOUT) Output Enable (OUTEN) Discussed potential solutions: Update of the existing API in Existing drivers: This option was discussed in ARTD-14125 and ARTD-14126 but there wasn't significant improvement of the execution time. Adding new API to existing drivers: New specialized functions which are closer to registers/peripheral (less abstraction). Note/idea: Channel role is constant during runtime so macro dispatcher could be considered like in example: #define EMIOS_ChannelWriteA_(module, ch, a) \ EMIOS_##module.A##ch.R = (uint16_t)a Adding new special driver for MC (Autosar as well as non autosar).
ARTD-23729	Bug	[Port] Hard Fault at port initiation (Port_Init)<*> Detailed description (how to reproduce it): Use PORT_143 for the Plugins Create a random configuration and use Port_Init to initiate that. Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0015 Observed behavior: The program runs into an infinity loop of Hard Fault at the clearing IMCR step (after the for loop at line 480 of Port_Ipw.c) !image-2022-02-17-15-30-09-316.png! !image-2022-02-17-15-30-22-735.png! The macro must be re-corrected according to the header files of the newest base's tag (PVT_BASE_S32K3XX_RTM_200_001). It should be IP_SIUL2_BASE Expected behavior: Port_Init must not run into Hard Fault loop when running through the IMCR clearing step
ARTD-23772	Bug	[I3c] ReadTerminate and Transfer Size seem redundant in transfer structure<*> Detailed description (how to reproduce it): generate and build any test suite (for ex. TS_005 and TS_006) Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: ReadTerminate and TransferSize seem redundant in transfer options structure. For use case master reads from slave, if SlaveTransferSize > MasterTransferSize Complete flag is not set when MasterBufferSize = 0, which leads to STOP not emitted. There are 2 possible scenarios: if ReadTerminate is set to the transfer size, STOP is emitted after ReadTerminate bytes and TERM warning/error is set in Slave error register; however, master receives a number of ReadTerminate bytes, with no error set in master erro register if ReadTerminate is not set, an SDA remains unchanged in a certain frame and Timeout error is set in Master error register Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: remove ReadTerminate from transfer options structure and set it to the transfer size within driver logic when emitting START request when write, do remove operation to set the ReadTerminate
ARTD-23776	New Feature	[ETH]Update driver follow to RM Rev3 updated<*> NewWorkDescription: RM Rev.3 updated. Driver need to update accordingly. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: RM Rev.3 updated. Driver need to update accordingly.
ARTD-23792	Bug	[S32K3 2.0.0][SENT] Wrong behavior when use SentFastFrame in Flexio_Sent_Ip_StartTransfer<*> Detailed description (how to reproduce it): In the function behavior Flexio_Sent_Ip_StartTransfer, it uses SentFastFrame* to get ChannelID and Instance. This is a wrong behavior. Flexio_Sent_Ip_StartTransfer is call from others function: Flexio_Sent_Ip_GetFastChannelMsgData, Flexio_Sent_Ip_GetFastMsgData, Flexio_Sent_Ip_GetSerialChannelMsgData, Flexio_Sent_Ip_GetSerialMsgData. In these functions, SentFastFrame is declared with no specific value so it can be used liked parameter-in in function Flexio_Sent_Ip_StartTransfer:

ID	Subtype	Headline and Description
		!image-2022-02-22-15-31-04-999.png|width=618,height=99! !image-2022-02-22-15-32-05-202.png|width=913,height=56! Preconditions: Enable SentFastErrorNotif in configuration Test Case ID (internal TC that caught the defect) optional: Sent_TS_14 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23822	New Feature	[I3c] Add support to get master and slave status flags<*> NewWorkDescription: Add APIs to get master and slave status flags (MSTATUS and SSTATUS). Requirement source: RM.pdf Proposed solution optional: [...]
ARTD-23825	Bug	[S32K3 2.0.0][SENT] Data[FLEXIO_INSTANCE_NO][ChannelId] always be reset in Flexio_Sent_Ip_GetSerialMsgData function<*> Detailed description (how to reproduce it): In function Flexio_Sent_Ip_GetSerialMsgData, there are some issues: # Data array always be reset before processing fast msg and serial msg. So it never jumps to serial msg processing segment. !image-2022-02-23-17-50-26-323.png|width=848,height=84! # Data's elements (.SerialState and FastMsgCount) must be reset only when a serial msg is captured. If not, it always detect another serial msg after the first serial msg. It should be like this: !image-2022-02-23-17-57-50-239.png|width=605,height=84! 3. Because the change of GetSerialMsgData function, it captures a present serial msg at right after calling this function so there is some variables are unnecessary in Flexio_Sent_Ip_GetSerialMsgData: FastMsgCount[FLEXIO_INSTANCE_NO][ChannelId] can be replaced by Data[FLEXIO_INSTANCE_NO][ChannelId].FastMsgCount. Flexio_Sent_Ip_axFastData[FLEXIO_INSTANCE_NO][ChannelId].TimerbufferIndx should not be used to allocate TimerbufferIndx. 4. Timeout max is currently 65535, This duration is too small to detect a serial msg. So it should equals to 2^16. For more details, please check the attached files. I update some line of code to capture a serial msg. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Sent_TS_14 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check attached file.
ARTD-23826	Bug	[ICU][S32K3XX RTM 2.0.0] [S32DS]The build error with DMA function<*> Detailed description (how to reproduce it): When using channel with DM for signal measurement or timestamp mode, In the file Icu_DmaNotification generated in output, the function DMA does not have the name as following: !image-2022-02-23-17-09-18-405.png! !image-2022-02-23-19-07-48-711.png! Preconditions: Channel is enabled with DMA for signal measurement mode. Test Case ID (internal TC that caught the defect) optional: Icu_TC_FCT_0226 (Icu_TS_110), Icu_TC_WBT_0302 (Icu_TS_031) Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The DMA callback function is generated.
ARTD-23864	Bug	[BASE][S32CT] Code generation failed during RTD - LLCE integration<*> Detailed description (how to reproduce it): While creating a project with multiple drivers, including LLCE modules and Dio, the code generation was failed. Preconditions: Integrating Dio from RTD_3.0.0 and LLCE modules from LLCE_1.0.3 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The following error was shown: !image-2022-02-25-09-39-48-908.png!

ID	Subtype	Headline and Description
		Expected behavior: The project can be generated without any error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: A temporary solution is to add a requireScript in dio_codegenerator.js file. It is needed because "index" was somewhere initiated, and requireScript reimport index function to make sure that Dio can get the correct "index" !image-2022-02-25-09-42-58-349.png!
ARTD-23868	Bug	[gpt] Update missing exclusive areas in BSWMD<*> Detailed description (how to reproduce it): Do a repo sync on bswmd_creator to sync with the manifest (make sure that you've checked out BLN_BSWMD_CREATOR_04.08.03) Compile the plugin passing parameter GENERATE_BSWMD_FILE=ON to the make command (`p s1 b` in ZTH) If the plugin was compiled successfully and there are no errors from bswmd_creator regarding missing or unmapped exclusive areas, then you can close your clone with "Fixed No Action Taken". Otherwise, proceed with the solutions given in the "Proposed solution" section. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing exclusive areas in <Module>_Bswmd.arxml Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Potential Issue #1 Missing exclusive areas for ISRs Solution #1 The bswmd_creator script will automatically fetch ISRs from the source code as long as they're defined with ISR(...). Every ISR mentioned in the "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall also be wrapped in ISR(...). For example: ADC_EXCLUSIVE_AREA_70 is used in function ISR(Ctu_Error_Isr) to protect the updates for CTU_IFR register Potential Issue #2 Missing exclusive areas for IPL functions which are not called by any HLD function Solution #2 # Have the EA mentioned in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" only as used by the IPL function. For example: ADC_EXCLUSIVE_AREA_17 is used in function Adc_Sar_Ip_AbortConversion to protect the updates for ADC_MCR register # Add the IPL function in NonASR_ServiceID.xml Note: Do not use other workarounds like artificially mentioning in .dox that the IPL function is called by an HLD function which is included in NonASR_ServiceID.xml (even though, in reality, it's not)
ARTD-23884	Bug	[ETH] GMAC driver sets wrong value for Tx Queue Size<*> Detailed description (how to reproduce it): For example, configure egress FIFO with buffer size 512 and buffer count 16. This should give an MTL queue size of 16*512/256=32. The MTL_TxQn_Operation_Mode.TQS should be programmed to 31 (0x1F). Observed behavior: MTL_TxQn_Operation_Mode.TQS is programmed to 0 if queue size is 32. Additionally, when using above configuration and TQS=0, GMAC produces an underflow error for frames > 230 bytes. Expected behavior: MTL_TxQn_Operation_Mode.TQS is programmed to (queue size 1).
ARTD-23889	Bug	[S32K3][Crypto] ECVD file miss some field when it is generated from mex file<*> Detailed description (how to reproduce it): When generate file ECVD from mex file of HLD in tag CRYPTO_121, it will be missing field CryptoKeyElementRef in CryptoKeytypes due to gen fail when import ECVD file to EB Test Case ID (internal TC that caught the defect) optional: Crypto_TS_COT_007 Observed behavior: When import ECVD to EB , it report gen fail due to missing CryptoKeyElementRef Expected behavior: EVCD file have mapping with mex file when it gen from S32DS Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23903	New Feature	[PORT] Redo the implementations for Virtual Wrapper for S32K3XX RTM 2.0.0<*> NewWorkDescription: There are 3 new requirements for Virtual Wrapper's implementations: CPR_RTD_00442.port: For each PortPin, the configured PDAC slot for its registers shall be specified using a configuration parameter named VirtWrapper PDAC implemented in the PortPin container. The default value of VirtWrapper PDAC shall be PDAC0 CPR_RTD_00657.port: The configured PDAC slot for Dio and Port registers shall be selectable per pin basis in the configurator if Virt Wrapper support is enabled.

ID	Subtype	Headline and Description
		Rationale: Port and Dio mirrors should be configured even if RM is not available in project. Base address registers for Port and Dio registers depend on the previously configured virtual wrapper assignment. CPR_RTD_00658.port: The configured PDAC slot for Dio and Port registers shall be interrogated from the RM component per pin basis if Virt Wrapper support is enabled and if the RM component is available in the project. Requirement source: CPR_RTD_00442, CPR_RTD_00657, CPR_RTD_00658 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: First of all, create a new parameter in configurator as mentioned in CPR_RTD_00442 Then following the CPR_RTD_00657 and CPR_RTD_00658, the PDACs slot will not be gotten from partitions (multicore) Dio and Port will implement the Virtual Wrapper even if RM is available in the project or not.
ARTD-23904	New Feature	[DIO] Redo the implementations for Virtual Wrapper for S32K3XX RTM 2.0.0<*> NewWorkDescription: There are 3 new requirements for Virtual Wrapper's implementations: CPR_RTD_00442.port: For each PortPin, the configured PDAC slot for its registers shall be specified using a configuration parameter named VirtWrapper PDAC implemented in the PortPin container. The default value of VirtWrapper PDAC shall be PDAC0 CPR_RTD_00657.port: The configured PDAC slot for Dio and Port registers shall be selectable per pin basis in the configurator if Virt Wrapper support is enabled. Rationale: Port and Dio mirrors should be configured even if RM is not available in project. Base address registers for Port and Dio registers depend on the previously configured virtual wrapper assignment. CPR_RTD_00658.port: The configured PDAC slot for Dio and Port registers shall be interrogated from the RM component per pin basis if Virt Wrapper support is enabled and if the RM component is available in the project. Requirement source: CPR_RTD_00442, CPR_RTD_00657, CPR_RTD_00658 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: First of all, create a new parameter in configurator as mentioned in CPR_RTD_00442 Then following the CPR_RTD_00657 and CPR_RTD_00658, the PDACs slot will not be gotten from partitions (multicore) Dio and Port will implement the Virtual Wrapper even if RM is available in the project or not.
ARTD-23906	Bug	[WDG] Generated code by 3rd party tool is incorrect when /ActiveEcuC/Wdg is defined<*> Detailed description (how to reproduce it): Generated code by 3rd party tool is incorrect when /ActiveEcuC/Wdg is defined in the configuration file instead of /Wdg/Wdg. Preconditions: Generated code by 3rd party tool, /ActiveEcuC/Wdg is defined in the configuration file Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generated code by 3rd party tool is incorrect when /ActiveEcuC/Wdg is defined in the configuration file instead of /Wdg/Wdg. Expected behavior: Generated code should be correct regardless the node definitions. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: There was a known issue from MCAL (e.g. MCAL-2875 in which: The autosar path Mod/ELEMENTS/Mod (where Mod is module name, for example Adc, Mcu, Resource etc.) must not be used in code generation templates (Mod_PBcfg.c, Mod_Cfg.c) to reference other nodes. The reason is that this path does not exist if there is used third party configuration tool. This leads to generation errors as node is not found. The solution would be replace the ./../../../Wdg/ELEMENTS/Wdg by: node:refs('ASPathDataOfSchema:/AUTOSAR/Wdg')
ARTD-23911	Bug	[ICU][S32K3] CT reports an error when select a global bus as time base in ICU module<*> Detailed description (how to reproduce it): When the ICU channel selects a global bus as time base, there will be a error in CT. However, the Emios_Mcl_Ip driver was added and configured. Moreover, the configuration code can be generated normally. It was firstly reported in ARTD-12355, but it was closed and this issue has not been solved in RTD 1.0.0. Customer GLB recently reported it to AE. !image-2022-02-28-15-45-53-992.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23915	New Feature	[adc] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i.

ID	Subtype	Headline and Description
		e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).
ARTD-23927	New Feature	[i2c] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).
ARTD-23930	New Feature	[icu] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription:

ID	Subtype	Headline and Description
		Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).
ARTD-23937	New Feature	[platform] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output \eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).

ID	Subtype	Headline and Description
ARTD-23940	New Feature	[pwm] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output\eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var> The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).
ARTD-23948	New Feature	[uart] Adjust range of integer node in EB due to limitation of java<*> NewWorkDescription: Previously, we implement integer node has maximum range from [TPS_GST_00008]: 9223372036854775808 .. 18446744073709551615 but in latest release node of EB28, it state that: Deviating from the AUTOSAR traceable [TPS_GST_00008], the formula language in terpreter of EB tresos Studio supports only the signed 64-bit range for integer values, i. e. from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807). The formula language parser of EB tresos Studio is implemented in Java. It uses the long primitive type for integer values and therefore can only support the restricted range. Requirement source: Please try to generate vsmd report using EB 28.2 if you got no error, please ignore this ticket. If you got some errors, you might see this warning in log prompt from EB on terminal (eg: ADC): This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. WARNING 22-03-08,11:28:58 (23016) The MAX attribute (describing the maximum allowed value for the parameter AdcPowerState with current value 18446744073709551615 defined in file D:\Git_rtd\tools\tresos_plugin_builder\make\..\..\..\output\eclipse\plugins\Adc_TS_T31D53M8I0R0\autosar\Adc_s32e27x_bga975.epd at line 4981) is greater than 64 bit signed integer. This is a restriction of tresos Studio. The value is automatically restricted to 9223372036854775807. {_}*Error EcucSws_1007: For Integer and Float Parameters the MIN values must be >= and the MAX values <= as in the StMD. (see example in VSMD report of ADC in attachment*{_}{*}{{*}} Proposed solution optional: To elimilate warning and error on vsmd report, we need to implement a fix to change the range of integer node adapt with EB example: Before* <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=18446744073709551615"/> <a:tst expr=">=0"/> </a:da> </v:var> Example: After fixed <v:var name="AdcChannelConvTime" type="INTEGER"> <a:da name="INVALID" type="Range"> <a:tst expr="<=9223372036854775807"/> <a:tst expr=">=0"/> </a:da> </v:var>

ID	Subtype	Headline and Description
		The range of all integer nodes should be limit from 0x8000000000000000 (-9223372036854775808) to 0x7fffffffffffffff (9223372036854775807).
ARTD-23956	Bug	[ICU] The function description did not map with autosar spec<*> Detailed description (how to reproduce it): [The Icu_GetTimestampIndex function description did not map with ICU autosar spec. !image-2022-03-01-09-28-19-598.png|thumbnail! Autosar Spec: !image-2022-03-01-09-38-07-824.png|thumbnail! The description is cloned from Icu_GetTimeElapsed. Unfortunately, my application did not work when I used and read the Icu_GetTimestampIndex API. !image-2022-03-01-09-39-00-397.png|thumbnail! Please double-check with other functions. Second Issue: I configure the emios channel. When I select the global bus, the EB require to link EmiosBus reference from MCL module. However, the description did not mention anything for customer by setting emios bus in MCL. That's an issue. !screenshot-1.png|thumbnail!] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [Wrong function description] Expected behavior: [Correct the description] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-23962	Bug	[ICU][S32K3XX RTM 2.0.0] The build fail error with ip Emios file in S32DS<*> Detailed description (how to reproduce it): The file Emios_Icu_Ip_SA_VS_0_PBcfg.c generated in S32DS is empty: !image-2022-03-01-15-11-38-159.png! !image-2022-03-01-16-22-36-039.png! Please check above code section in file Emios config to find the issue. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-23975	New Feature	[adc] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-23977	New Feature	[can] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module:

ID	Subtype	Headline and Description
		System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-23983	New Feature	[dio] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-23994	New Feature	[i2c] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24003	New Feature	[platform] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var".

ID	Subtype	Headline and Description
		## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24005	New Feature	[port] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24006	New Feature	[pwm] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24008	New Feature	[rm] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24012	New Feature	[spi] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:

ID	Subtype	Headline and Description
		What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24014	New Feature	[uart] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24015	New Feature	[wdg] [S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24018	New Feature	[DIO] Change the define names to not contain derivatives name<*> NewWorkDescription: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/port/pull-requests/410/overview?commentId=1104467] [Radu-Andrei Brasoveanu|https://bitbucket.sw.nxp.com/users/nxa19269] i would advise in creating a follow up ticket for entire code and changing the define names to not contain derivatives name. more suitable will be to use something like: FEATURE_PORT_CI_PORT_IP_PCR_MUXING}} Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Change the define names to not contain derivatives name.
ARTD-24022	Bug	[S32K3 2.0.0] Crypto: Include incorrect file "S32K342_MUB.h" on the file Hse_Ip_Cfg.h ,,"Detailed description (how to reproduce it): Build fail test with derivative S32K342 because on the Base header file don't have contain S32K342_MUB.h, it name correct is S32K342_MU.h Preconditions: Build fail test with derivative S32K342 Test Case ID (internal TC that caught the defect) optional: All test build fail Observed behavior: all test build fail with error cannot open source file ""S32K342_MUB.h"" Expected behavior: All test can build success with derivative S32K342

ID	Subtype	Headline and Description
		Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change include ""S32K342_MUB.h"" to ""S32K342_MU.h""
ARTD-24024	Bug	[S32K3 2.0.0][SENT] FXIO_ISR_PROCESS_TIMER_CTRLx shoud be defined in case SentFastNotification<*> Detailed description (how to reproduce it): Since function Flexio_Sent_Ip_GetFastMsgData used interrupt to collect timer value, function Flexio_Sent_Ip_IRQTimerHandler need to declared. So FXIO_ISR_PROCESS_TIMER_CTRL need to define to declare Flexio_Sent_Ip_IRQTimerHandler Preconditions: Using Flexio_Sent_Ip_GetFastMsgData Test Case ID (internal TC that caught the defect) optional: TS_10 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update Flexio_Sent_Ip_Cfg.h [!IF "SentProcessing = 'POLLING'"!] [!LOOP "SentChannelConfig/*"!] [!IF "((node:exists(SentFastNotification) and (SentFastNotification != 'NULL_PTR')) or (node:exists(SentSlowNotification) and (SentSlowNotification != 'NULL_PTR')))"!] [!VAR "ChnlPollingFlag" = "'true'"!] [!BREAK!] [!ENDIF!] [!ENDLOOP!] [!IF "$ChnlPollingFlag = 'true'"!] [!CODE!]#define FXIO_ISR_PROCESS_TIMER_CTRL[!"text:split((node:ref(SentHwControllerRef)/FlexioMclInstances),'_')[2]"!][!CR!][!ENDCODE!] [!ENDIF!] [!ENDIF!]
ARTD-24031	Bug	[MCU] 'STANDBY' can not let S32K3 MCU really enter standby mode<*> Detailed description (how to reproduce it): If we select STANDBY in MCU power component, MCU can not enter standby mode after calling MCU_Set_Mode(STANDBY). If we select SOC_STANDBY in MCU power component, MCU can enter standby mode after calling MCU_Set_Mode(SOC_STANDBY). Many customers have met the issue and I have tested it. If we select STANDBY in MCU power component, MCU can not really enter standby mode after calling MCU_Set_Mode(STANDBY). However, customers hope we can provide MCAL level code to config fast standby exit address. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-24053	New Feature	[icu][S32CT] Update code generation to work in JS strict mode<*> NewWorkDescription: Note: Only Peripherals Tool's components are affected{color}*. There has been an update to the System module: System scripts now run in strict mode and contain include guards to protect against multiple inclusion System utilities / functions have been made read-only Code templates are now evaluated in strict mode so that developers can be aware of overwriting existing variables or using undeclared variables*. Requirement source: Consequence of https://jira.sw.nxp.com/browse/ARTD-23864 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: What you have to do: ## Open S32DS's logging file (swtools.log) or launch the program with console logging activated (e.g. run ".\s32ds.exe consoleLog in CMD/PowerShell) ## Create a new project and instantiate your high-level / low-level component. ## Fix the encountered errors related to your component. Most of them will be along the lines of "ReferenceError: <variable_name> is not defined" or "TypeError: <variable_name> is not a writable property of [object global]"_. Both can be resolved by simply defining the offending variable using "var". ## Remove inclusions of "refsSolver.js" in your code templates or code generator scripts. If there's an API you need from that file which is not provided in codegeneratorUtils.js, please let me know.
ARTD-24054	Bug	[ICU] There are some errors in S32DS with HLD and IP layer<*> Detailed description (how to reproduce it): The file Icu_Cfg.h is generated is empty for high layer : !image-2022-03-03-08-45-26-442.png! In S32DS for IP layer, this error log appears:

ID	Subtype	Headline and Description
		!image-2022-03-03-09-09-15-466.png! In the file Siul2_Icu_Ip_Cfg.h and Wkpu_Ip_Defines.h, the code is empty, please check the file Siul2_Icu_Ip.mex and Wkpu_Ip.mex attached : !image-2022-03-04-08-47-40-530.png! !image-2022-03-04-08-53-12-651.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Icu_TC_FCT_0211 Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-24080	Bug	[CRYPTO] No mechanism is present to clear the receive register when request timeout occurs<*> Detailed description (how to reproduce it): Set a low request timeout value, smaller than the time it takes HSE FW to process the request, and send the request. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The analysis on the driver code revealed that if the timeout is reached the channel will be released from the Crypto driver (IP) point of view but the from the hardware point of view the channel is not fully free until the RR register is read. The RR register can be read after the HSE firmware has finished the service and provided an response in RR. The channel on which the timeout has occurred can not be allocated again even if the firmware has finalized the request. Expected behavior: The channel is freed after the firmware has finished the processing so during the channel allocation request it can be allocated for requests. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: To avoid this situation the RR register can be read during the channel allocation in order to unblock the channels that satisfy the following points: # The Crypto driver has the channel marked as free # FSR bit for the channel is clear # TSR is set
ARTD-24105	New Feature	[CRYPTO] Fix compiler warnings<*> NewWorkDescription: Fix the compiler warnings present in the attached excels. ITG generated(for K3):[^RTD_CRYPTO_Compiler_Warnings (11) (1).xlsx] Develop generated(for G2):[^AUTOSAR_MCAL_CRYPTO_Compiler_Warnings.xlsx] Requirement source: Release Criteria (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Analyze and fix the issues found.
ARTD-24092	Bug	[S32K3XX][s32k3_300] Project can't generate config on S32CT<*> Detailed description (how to reproduce it): Creating new project with platform component on s32ds, Add some config and update code. The project can't generate config Preconditions: PVT_S32K3XX_ARTD_22061_003, Test Case ID (internal TC that caught the defect) optional: Platform_TS_CT_001 Observed behavior: !image-2022-03-04-11-55-59-838.png! Expected behavior: Project generate success. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add var before the variable !image-2022-03-04-12-01-01-620.png!
ARTD-24095	Bug	[PWM] Short-name of some nodes in ECVD file on S32DS are blank<*> Detailed description (how to reproduce it): IPL: Difference when generating between mex file and ecvd file. Some of the container's short names are not generated when generating with mex file but it is generated when generating with ecvd file: <SHORT-NAME>EmiosChIrqCallback</SHORT-NAME> <SHORT-NAME>PwmGeneral</SHORT-NAME> HLD: In the evcd file there is no node PwmChannel Class. When generating the source file, it will take the default value of the node PwmChannelClass. it causes a difference between the source file generate. Please compare folder new_configuration and original_configuration in attach file. Preconditions:

ID	Subtype	Headline and Description
		Compare output when generating with mex file and ecvd file Test Case ID (internal TC that caught the defect) optional: Ip_Emios_TS_ECPD_001 Observed behavior: N/A Expected behavior: The output generated must be the same Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-24117	Bug	[S32K3 2.0.0] Crypto:Fix compiler warnings<*> Detailed description (how to reproduce it): There are some compiler warnings existed in the report on attached file below. Preconditions: Build test with TEST_PARAMS=@LoadTo=flash Tag test":PVT_TEST_CRYPTO_S32K3_RTM_200_V18 Tag Dev VT_CRYPTO_K3_200_HF_V01 Test Case ID (internal TC that caught the defect) optional: Crypto_TS_005 Observed behavior: There are some compiler warning in the report. Expected behavior: There is no compiler warning in the report. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24118	Bug	[S32K3 2.0.0] FLS: fix version checking<*> Detailed description (how to reproduce it): FLS have some file version checking incorrect Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: check report in [http://kara.ea.freescale.net/0/project/custom_file_verchecking/details] need fix all validation Expected behavior: FLS version checking correct Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-24135	Bug	[CRYPTO] Crypto_CancelJob can never report timeout runtime error<*> Detailed description (how to reproduce it): Try to make timeout runtime error for Crypto_CancelJob and Crypto_MainFunction. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Crypto_CancelJob and Crypto_MainFunction can never report timeout runtime error. Expected behavior: Crypto_CancelJob and Crypto_MainFunction can report timeout runtime error. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the low level code to report timeout error to HLD layer (detail on the attached email)
ARTD-24152	Bug	[S32K3][Platform] Update linkers to ensure that .acfls_code_ram section is aligned with cache line<*> Detailed description (how to reproduce it): .acfls_code_ram is not allocated to cacheline-aligned address, so Fls driver cannot work properly Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Fls_TC_FCT_4001 Observed behavior: .acfls_code_ram section is not fully synchronized with cache after calling Fls_LoadAc and Cache_Ip_CleanByAddr Expected behavior: that section must be fully synchronized Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) please see below figures Proposed solution optional: .acfls_code_ram must be aligned with cache line
ARTD-24176	Bug	

ID	Subtype	Headline and Description
		[I3c] Async transfer method doesn't wait for MCTRLDONE after Stop is emitted<*> Detailed description (how to reproduce it): Build any dev tests with Async transfers. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Ascyn transfer method doesn't wait for MCTRLDONE after STOP or Force Exit is emitted. Expected behavior: Ascyn transfer method waits for MCTRLDONE after STOP or Force Exit is emitted. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: wait for MCTRLDONE using Control Done interrupt for I2c legacy transfers, remove delay added in Complete/End Transfer handlers for I2c Bus type, when STOP is emitted, MCONFIG[ODSTOP] must be 1.
ARTD-24262	Bug	[platform][s32k3_200] compiler warning<*> Detailed description (how to reproduce it): Compiler warning detect with K3xx derivative. Preconditions: PVT_S32K3XX_ARTD_22061_004 Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: Excel attachments. Expected behavior: Driver no warning, error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-24263	New Feature	[S32K3 2.0.0] FLS: improve calculate value for "Fls Access Code" ,,"NewWorkDescription: updated calucate value for ""Fls Access Code"" update M4 macro for Fls Access Code less flexible so that sould get FlsAcErase, FlsAcWrite value from Resource Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-24283	New Feature	[BASE] Add support for S32K322 and S32K341 derivative<*> NewWorkDescription: Add support for S32K322 and S32K341 derivative Requirement source: RM rev 3 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:
ARTD-24297	Bug	[I3C] Dma master/slave node is not disabled corresponding to I3cMasterSlaveMode<*> Detailed description (how to reproduce it): [I3C] Dma master/slave node is not disabled corresponding to I3cMasterSlaveMode I3cDmaFeature= true I3cMasterSlaveMode=Slave I3cMasterTransferType=DMA I3cMasterDmaTxChannel and I3cMasterDmaRxChannel are editable Same issue when I3cMasterSlaveMode=Master for I3cSlaveDmaTxChannel and I3cSlaveDmaRxChannel !image-2022-03-09-17-54-38-372.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: I3c_TC_FCT_1000 Observed behavior: [...] Expected behavior: The I3cMasterDmaTxChannel and I3cMasterDmaRxChannel should be editable if I3cMasterSlaveMode != 'SLAVE' and {color}{color:#ce9178}node:value(../I3cMasterTransferType) = 'DMA' Similar for I3cSlaveDmaTxChannel and I3cSlaveDmaRxChannel nodes Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-24300	Bug	“Input Inversion Select” in pin config tool<*

ID	Subtype	Headline and Description
		“Input Inversion Select” item in routing details in pin config tool should be changed to “Output Inversion Select”. I confirmed this on my board. INV bit in MCSR register does not affect the input. Regardless of INV bit, input register GPDI always shows the same logic level as connected to a pin. If a pin is configured as output, level of a pin can be inverted by INV. But also in this case, GPDI still shows the real level of a pin. !invert.jpg!
ARTD-24303	Bug	[icu] [S32K3XX 2.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports Please see the attached file to know more details https://bamboo3.sw.nxp.com/artifact/ARTD-CIICU/BUILDCOV/build-480/MISRA_HIS-XLSX-Reports,-Compiler-Warnings,-Code-Exposure-and-Violations-logs/coverity_artifacts/S32K3XX_4.4_BLN_RTD_4.4_S32K3XX_2.0.0/ *Reference: SOW: https://nxp1.sharepoint.com/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BD1DC93AE-F154-48B3-8D46-A8F7B0725503%7D&file=S32K3%20RTD%20ASR%204.4%202.0.0%20SOW.docx&action=default&mobileredirect=true&cid=e08b347a-ad8c-495e-bed0-64fb8c121547 MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-24321	New Feature	[S32K3XX] Add support for S32K322 and S32K341<*> NewWorkDescription: Add support for S32K322 and S32K341 Requirement source: RM rev 3 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]
ARTD-24371	New Feature	[spi] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24372	New Feature	[sent] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=

ID	Subtype	Headline and Description
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ARTD-24374	New Feature	[uart] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24378	New Feature	[adc] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24382	New Feature	[wdg] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24383	New Feature	[crypto] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx

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ARTD-24384	New Feature	[dio] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24385	New Feature	[port] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24387	New Feature	[icu] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24389	New Feature	[pwm] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx

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ARTD-24338	Bug	[UART][S32K3_200] Fix MISRA violation<*> Detailed description (how to reproduce it): Lpuart violate MISRA rule 10.3 Symbol "Lpuart_Uart_Ip_apStateStructure" is declared more than once and with types that are not identical. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: UART_TC_0001 Observed behavior: This is the struct that is extern to use in the configuration file. Expected behavior: Fix MISRA rule 8.3 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24362	Bug	[I3C] ISR doesn't clear interrupt status flag if the driver is not initialized<*> Detailed description (how to reproduce it): Req ID: CPR_RTD_00011.i3c ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. I3C ISR doesn't clear interrupts status flag if driver is not initialized !image-2022-03-13-23-09-28-929.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: I3c_TC_FCT_0004 Observed behavior: [...] Expected behavior: [...] Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Refer SAI0_IRQHandler in [Source of Sai_Ip.c i2s NXP Bitbucket|https://bitbucket.sw.nxp.com/projects/ARTD/repos/i2s/browse/ip/IP_SAI/src/Sai_Ip.c]
ARTD-24391	Bug	[S32K3XX][PORT] Init value was incorrect when config Analog Input Mode<*> Detailed description (how to reproduce it): Pin PA9 was config ADC0_ADC0_P7 with level: high/low/not change, check initValue Preconditions: use tag PVT_PORT_S32K3XX_2.0.0_V07 Test Case ID (internal TC that caught the defect) optional: Port_TC_FCT_0005 Observed behavior: !image-2022-03-14-11-12-29-810.png! Expected behavior: InitValue = 0/1/2 corresponding config level low/high/notchange Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24392	Bug	[S32K3 2.0.0][SENT] Receiver->TransferErrorDetect is not reset after De-Initialization<*> Detailed description (how to reproduce it): Receiver->TransferErrorDetect[SentFastFrame->ChannelId] = TRUE when driver detects a Calibration Pulse error. But this variable can not be reset when driver De-Initialize. It makes the issue: when initialize driver again, it can not detect error relate to Calibration Pulse. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: TS_19 Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA

ID	Subtype	Headline and Description
ARTD-24419	Bug	[Spi] "OsAppEcucPartitionRefList" is not defined on ds s32k324 ,,"Detailed description (how to reproduce it): ""OsAppEcucPartitionRefList"" is not defined Preconditions: enable multicore with s32k324 on ds Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24433	New Feature	[cryif] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24435	New Feature	[csm] [K3 2.0.0] Support new derivatives<*> [K3 2.0.0] Support new derivatives: S32K341: S32K341_100MQFP, S32K341_172MQFP S32K322: S32K322_100MQFP, S32K322_172MQFP Reference docs: Reference Manual |S32K3xx Reference Manual, Rev. 3, 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive%2FS32K3xx%5FRM%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FArchive] Datasheet |S32K3xx Data Sheet, Rev. 3 — 10/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3Z4S2lrZDFFbTJnQWI0QlctTnpZTkdCNW9sQ3A2UF9aOUdKYnc%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive%2FS32K3xx%5FDS%5FRev3%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FArchive]
ARTD-24436	Bug	[CAN] analysis global variable access in multithreads/multicores scenario<*> Detailed description (how to reproduce it): Case A: !image-2022-03-15-14-32-03-471.png|thumbnail! [...] static ReceivedDataBuffer variable could be accessed simultaneously as below supposed scenario: multithreads: Can_MainFunction_Read_0 is executed on thread_0, Can_MainFunction_Read_1 is executed on thread_1 multicores: core0 and core1 execute on Can_MainFunction_Read(); Case B: !image-2022-03-15-14-39-03-414.png|thumbnail! Can_Ipw_au16TxPduId could be changed during it is being passed to CanIf_TxConfirmation. This case can only happen in multithreads scenario: Can_MainFunction_Write is executed on thread_0, Can_Write is executed on thread_1. !image-2022-03-15-14-48-40-278.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: review Observed behavior: some shared global variable access is not safe Expected behavior: global variables should be analysed Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		N/A

ARTD-24455	Bug	hard fault during flash reading<*>
		
		Detailed description (how to reproduce it):
		I can share the project if it is needed.
		Observed behavior:
		During our MC development we experienced very latent Hard fault.
		I think it might happen due to speculative fetches.
		Expected behavior:
		Fault occurred in Clock_Ip_Init(&Mcu_aClockConfigPB[0]); when optimization was set to O3 (if you set O1 or if you set a break point there on that instruction Hardfault will not occur)
		40563e: f8df 8138 ldr.w r8, [pc, #312] ; 405778 <Clock_Ip_InitClock+0x5cc> caused hard fault
		!image-2022-03-16-09-58-56-799.png|thumbnail!
		Proposed solution optional:
		we discussed this topic with BACH NGUYEN <B.Nguyen@nxp.com>.
		conclusion is that in system.c MPU settings should be changed.
		instead of
		/*Program flash which would extract from linker symbol*/
		rbar[2]=(uint32)__ROM_CODE_START;
		rasr[2]=0x060{color:red}B{color}002BUL;
		There should be(Memory type: Device):
		/*Program flash which would extract from linker symbol*/
		rbar[2]=(uint32)__ROM_CODE_START;
		rasr[2]=0x060{color:red}1{color}002BUL;

ARTD-24498	Bug	[S32K3 2.0.0][SENT] Slow/FastNotification can not be imported from epc to S32DS<*> Detailed description (how to reproduce it): When import epc file fto S32DS, some notification nodes do not appear on S32DS !image-2022-03-17-14-40-04-930.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-24511	Bug	[S32DS][SAF85xx] Build fail with new project on S32DS after updating code<*> Detailed description (how to reproduce it): 1. Install S32DS3.4 with devpackage: com.nxp.s32ds.saf85.update_3.4.4.20220310181914.zip and update_site: S32R_RTD_4_4_EAR_0_8_0_DS_updatesite_2203_signed.zip Wed Mar 16 20:27:12 2022 2. Integrate GHS 202114 and DIAB 7.0.3.0 into S32DS 3. Create new project following steps: Step1: In S32DS choose File > New > S32DS Application project Step2: Fulfil project name and Choose Family/SAF8544 (M7/A53) > Next> Next Step3: Select required tool chain plugin from toolchain tab x number of tools chains Step4: Type a project name(e.g NewProject). Step5: Select SDK version Step6: Click Finish Step7: Build project with RAM and FLASH Step8: Click on Update code Step9: Build project with RAM and FLASH Preconditions: Test Case ID (internal TC that caught the defect) optional: INTEGRATION_TC_017 INTEGRATION_TC_037 INTEGRATION_TC_077 Observed behavior: Build fails after updating code both cores M7 and A53 on all compilers !image-2022-03-17-17-30-18-091.png|width=1003,height=218! Expected behavior: Have no warnings, errors when building new project on all compilers Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-24529	Bug	[S32K3 2.0.0] [OCU] Incorrect autosar minor version in file Ocu.template<*> Detailed description (how to reproduce it): In file Ocu.template using wrong M4 define (M4_XDM_AR_SPEC_VERSION_PATCH) for autosar minor version. Correct M4 is M4_XDM_AR_SPEC_VERSION_MINOR Preconditions: Build test ecpd high layer Test Case ID (internal TC that caught the defect) optional: Ocu_TS_ECPD_001.c Observed behavior:

ID	Subtype	Headline and Description
		Test Ocu_TS_ECPD_001 not pass, there is a different of ArReleaseMinorVersion between new configuration and original configuration (0 and 4) Expected behavior: ArReleaseMinorVersion in new configuation change to 4, test passed Proposed solution optional: NA
ARTD-24548	New Feature	 s32k324 dual core template in a single project<*> NewWorkDescription: Include attached project in Platform examples Requirement source: Customer request Proposed solution optional: Include project in platform
ARTD-24575	Bug	 [S32K3XX] I3c_Init() jumps to hardfault with update from Platform<*> Detailed description (how to reproduce it): I3c_Init() jumps to hardfault with update from Platform !image-2022-03-21-15-43-19-116.png! Change compare PVT_S32K3XX_ARTD_22061_020 vs PVT_S32K3XX_ARTD_22061_016 !image-2022-03-21-15-43-36-430.png! Preconditions: Use Platform with tag PVT_S32K3XX_ARTD_22061_020 Test Case ID (internal TC that caught the defect) optional: I3c_TS_WIR_100 Observed behavior: Program jumps to hardfault Expected behavior: No error when executing test Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-24644	Bug	 [WDG] Missing Wdg_Instance1 for S32K322 derivative from S32ConfigurationTool<*> Detailed description (how to reproduce it): Step 1: Create new project Step 2: Add Wdg and dependencies to new project Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing Wdg_Instance1 for S32K322 derivative !image-2022-03-21-18-11-04-571.png|width=956,height=538! Expected behavior: Add Wdg_Instance1 for K322 derivative Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-25248	Bug	 [Port][S32K342] Incorrect PORT_MAX_UNUSED_PADS_U16 macro value generated from S32CT<*> Detailed description (how to reproduce it): Use tag PVT_PORT_S32K3XX_2.0.0_V15 for the Port plugins Open S32DS and configurate S32K342 with S32K342_100MQFP package. Add random pins to the CTHL and open Port_VS_0_PBcfg.c and Port_Cfg.h One examples .mex was attached for reviewing. Preconditions: PVT_PORT_S32K3XX_2.0.0_V15 Test Case ID (internal TC that caught the defect) optional: Port_TC_COT_0001 Observed behavior: the array Port_aUnusedPads_VS_0 has more elements than the number of elements generated ({*}PORT_MAX_UNUSED_PADS_U16{*}) With the attached .mex, the number of elements is 126 but the macro PORT_MAX_UNUSED_PADS_U16 is 124 Expected behavior: The number of PORT_MAX_UNUSED_PADS_U16 is correct corresponding to the number of the elements of Port_aUnusedPads_VS_0 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: It seems like the resource.txt for S32K342_100MQFP is wrong with the Port.{*}Siul2Instance0NotImplementedMscrs{*}, please re-check.
ARTD-25261	Bug	 [Port][S32K3xx] Untouch IMCR feature doesn't work as expected<*> Detailed description (how to reproduce it): Use tag PVT_PORT_S32K3XX_2.0.0_V15 for the plugins. Create some random configuration with IMCR 188 set in the UntouchedIMCR tab

ID	Subtype	Headline and Description
		Preconditions: PVT_PORT_S32K3XX_2.0.0_V15 Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0009 Observed behavior: At the clearing IMCR step in Port_lpw.c, the driver keeps clearing IMCR 188 even it is set in the UntouchedIMCR tab. !image-2022-03-22-19-30-14-965.png! Expected behavior: No Imcr set in UntouchedIMCR tab are cleared during Port_Init Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [....]
ARTD-25266	Bug	[I3C] MISRA violations of Rule 2.3<*> Detailed description (how to reproduce it): !https://bitbucket.sw.nxp.com/rest/api/1.0/projects/ARTD/repos/i3c/attachments/12639! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Undocumented misra violations Expected behavior: Only accepted misra deviations remain in the report Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-25282	Bug	[UART] Wrong lowerMultiplicity attribute on ecpd<*> Detailed description (how to reproduce it): lowerMultiplicity of UartEcucPartitionRef is wrong, must be 0 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Have unexpected error Expected behavior: No error Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix lowerMultiplicity value of UartEcucPartitionRef to 0
ARTD-25285	Bug	[S32K3XX RTM 2.0.0] Fix warning of example<*> Detailed description (how to reproduce it): In the example IP LAYER{color}, the build warning appear because of Port warning: !image-2022-03-23-14-46-54-680.png! In the example{color:#de350b} Icu_BlinkLed_ASR_Emios_S32K344 and Icu_BlinkLed_ASR_Emios_S32K342{color}, the warning of Mcu apppear: !image-2022-03-23-14-49-19-116.png! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-25301	Bug	[S32K3 2.0.0][RM] Compiler Warning on IAR<*> Detailed description (how to reproduce it): Compiler warnings on IAR: static const uint8 Xrdc_Master[XRDC_COUNT] = XRDC_MASTER_INSTANCE; "d:\ARTD\S32K3XX\output\eclipse\plugins\Rm_TS_T40D34M20I0R0\src\Xrdc_Ip.c",148 Warning[Be006]: possible conflict for segment/section ".mcal_const": variable "Xrdc_Master ".mcal_const"" (declared at line 148 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344_iar/rm/../../eclipse/plugins/Rm_TS_T40D34M20I0R0/src/Xrdc_Ip.c") is an initialized variable (2 more variables like this) variable "Xrdc_Ip_InstanceAddress ".mcal_const"" (declared at line 136 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344_iar/rm/../../eclipse/plugins/Rm_TS_T40D34M20I0R0/src/Xrdc_Ip.c") is a constant (4 more variables like this) const Xrdc_Ip_InstanceConfigType aXrdc_Config_Array[1] = \{&Xrdc_Config_XRDC_INSTANCE0};

ID	Subtype	Headline and Description
		"d:\ARTD\S32K3XX\output\S32K3XX_S32K344\rm\Rm_TS_001_cfg1_CORE0\generate_tresos\src\Xrdc_Ip_PBcfg.c",538 Warning[Be006]: possible conflict for segment/section ".mcal_const_cfg": variable "aXrdc_Config_Array ".mcal_const_cfg"" (declared at line 538 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344/rm/Rm_TS_001_cfg1_CORE0/generate_tresos/src/Xrdc_Ip_PBcfg.c") is an initialized variable variable "Xrdc_Instances_InUsed ".mcal_const_cfg"" (declared at line 150 of "d:/ARTD/S32K3XX/output/S32K3XX_S32K344/rm/Rm_TS_001_cfg1_CORE0/generate_tresos/src/Xrdc_Ip_PBcfg.c") is a constant (5 more variables like this) Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Compiler warning on IAR Expected behavior: No Compiler warning Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-25452	Bug	[I3c] Init functions do not reset state structure to default values<*> Detailed description (how to reproduce it): Preconditions: Test Case ID (internal TC that caught the defect) optional: Observed behavior: I3c_Ip_MasterInit and I3c_Ip_SlaveInit functions do not reset state structures to default values. Also I3c_Ip_MasterDeInit and I3c_Ip_SlaveDeInit should reset registers to their default values. Expected behavior: I3c_Ip_MasterInit and I3c_Ip_SlaveInit functions reset state structures to default values. I3c_Ip_MasterDeInit and I3c_Ip_SlaveDeInit reset registers to their default values. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-25453	Bug	[WDG] The macro SWT_IP_MAP has Multiple Definition<*> Detailed description (how to reproduce it): SWT_IP_MAP has Multiple Definition Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: SWT_IP_MAP define in Swt_Ip_Cfg_Defines.h Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: SWT_IP_MAP delete define in Swt_Ip.c
ARTD-25457	Bug	[FLS][C40][S32K3 2.0.0] Hardfault exception occurs when accessing unaligned address<*> Detailed description (how to reproduce it): Due to the compiler optimized code, some lines of C code that handle the unalignment were cut out. When reading data from unaligned buffer address, instead of read one byte one of unaligned address, it read 4-byte into DataTemp32 due to compiler optimization then Hardfault will occur. (see attached figure for details) Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Fls_TS_051 Observed behavior: Read from unaligned address cause hardfault Expected behavior: Avoid compiler from optimizing Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add the volatile key word for variable uint32 DataTemp32; to prevent optimization
ARTD-25464	New Feature	[Gpt]Update some data test<*> NewWorkDescription: Update test data ecpd due to some module changes for new derivative S32K322, S32K341 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update test data with some test
ARTD-25488	Bug	[S32K3XX 2.0.0][PORT] Fix warning at build for S32K3 example<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		There are warnings related to Siul2_Port driver when build examples for S32K3 platform. Only occurred at IP layer. !image-2022-03-25-14-04-19-748.png|width=660,height=182! Preconditions: Build examples for modules that use Siul2_port driver (ex. Ocu, Icu,...) Test Case ID (internal TC that caught the defect) optional: Emios_Ocu_Example, Emios_Icu_Example, ... Observed behavior: The warnings related to Siul2_port driver appear Expected behavior: No warnings appear Proposed solution optional: NA
ARTD-25494	Bug	[Platform][s3k3xx_200] update linker file<*> Detailed description (how to reproduce it): Linker 344 Preconditions: PVT_S32K3XX_ARTD_22061_033 Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: Linker Expected behavior: Running project multicore on k324 Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: update sizes of ITCM and DTCM are 32K and 64k
ARTD-25529	Bug	[PORT] [S32K3XX_2.0.0] Duplicate the define SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h<*> Detailed description (how to reproduce it): There is a duplicate define about SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There is a duplicate define about SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h Expected behavior: There is no duplication for the defines. Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove one redundant define of SIUL2_MAX_NUM_OF_IMCR_REG in Siul2_Port_Ip.h
ARTD-25606	Bug	[UART] Getting an error when enabling multicore node on S32CT<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Getting an error when enabling multicore node on S32CT !screenshot-1.png|thumbnail! Expected behavior: Update uart component on S32CT Note: in the “Expected behavior” field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

4.10 Change List for 1.0.0

ID	Subtype	Headline and Description
ARTD-3065	New	New Feature [S32K3] Add support for SIUL2 External Interrupts with Config Tools for RTD ,,"There is no SIUL2 External Interrupts Config Tool component. Please add a Config Tool Component that sets, for each external interrupt channel, the action on which each interrupts is triggered (rising edge, falling edge or both edges).

ID	Subtype	Headline and Description
		An approach is to provide callbacks for each channel. (There are 4 interrupts vectors, e.g. IRQ_07_00, each handling 8 input channels. The RTD should implement the interrupts and trigger a callback for each pin state change.) Detailed explanation in the context of MBDT code generation:* The tool allows the user to select the eirq pins for the SIUL2 peripheral. However, I was not able to find structures that allow the user to select which action is going to trigger that interrupt (rising, falling, either edge). More than that, the interrupt block is going to implement and install the interrupt handler assigned to the required pins group (there are 32 external interrupts pins muxed 8 by 8 in 4 handlers) but since there is no interrupt configuration as mentioned above, which block is going to configure that, the interrupt block or is going to be another block for that? Also, we need other blocks that will return the IREER, IFEER registers values, in order to identify which pin and state triggered the interrupts. Test case: S32K / MPC approach: # Single block that performs the following actions: Initialize pin Configure interrupt action (Rising Edge ...) Installs interrupt Handles the interrupt (decides which pin triggered the ISR) Clears the pins interrupt S32K3 Initialize pin (Pins Tool) Configure interrupt action (Rising Edge ...) (*RTD CONFIG TOOL ISR PERIPH* ???) For the Periph tool, we have two requirements: 1. Provide a dedicated tab/setting for each enabled PIN allowing users to set the action that will trigger the interrupt like Rising edge. 2. A tab/setting in which the user must specify the handler name and priority for each interrupt group *IRQ**_07_00* Installs interrupt (Interrupt block) Handles the interrupt (decides which pin triggered the ISR) (Interrupt block) (RTD Function to return *DISR0* register) Clears the pins interrupt (Interrupt block) (RTD Function to reset the interrupt status in DISR0 defined in Siul2_Icu_Ip_Irq.c) We found that there is an implementation in the *Siul2_Icu_Ip_Irq.c* *that access the status* ** *flags* ** but the config tool is not copying the files in the project and no configuration structure for the IFEER/IREER found. "
ARTD-3069	New	New Feature [S32K3] Enhance the EMIOS driver features ,,"In case of EMIOS only the PWM feature is available in the S32DS Config Tools. Please add components for other functionalities like Input capture, Counter bus, etc. Also, please add a way of configuring the eMIOS Global Prescaler. Regarding the PWM, from the current CT initialization, even if you can configure a channel to be driven by a Global counter bus, for example, the Global counter bus A, I was not able to find an option that can configure the Global Counter bus A to count up. "
ARTD-3072	New	New Feature [S32K3] Add RTD example for EMIOS ,,"Since the EMIOS is a complex peripheral which is critical for Motor Control applications, please consider adding RTD examples to demonstrate how to use the driver in various scenarios like:

ID	Subtype	Headline and Description
		PWM generations: asymmetric/symmetric/edge/center align Input Capture"
ARTD-3491	New	 New Feature [RM] Support PID LOCK For XRDC ,," Mpu_M7_Ip_EnableRegion_Privileged is Reentrant, should be marked as NonReentrant per channel, and no EA needed; update also associated req, as the HLD one is Non_Reentrant. Mpu_M7_Ip_SetAccessRight_Privileged is Reentrant, should be marked as NonReentrant per channel, and no EA needed; update also associated req, as the HLD one is Non_Reentrant. Add support for non-supported field LK2 TSM LNUM"
ARTD-3773	New	 New Feature [ADC] Check and update DMA support for S32ConfigurationTool High Level Driver ,,DMA for SW triggered groups and Triggered Mode
ARTD-4422	New	 New Feature [FEE] Add support for bad Sector Management and Sector Retirement (part 1) ,,"NewWorkDescription: Add support for bad Sector Management and Sector Retirement (CPR_RTD_00505.fee). This involves removing Sectors from configuration when they become unusable. Rationale: some flash memory specs have low endurance/write cycles availability, which needs to be improved by the ability to retire bad sectors or locations affected by permanent ECC, at the expense of allocated flash size the endurance being a ppm specification."" Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support to use un-consecutive logical sector addresses."
ARTD-5105	New	 New Feature [sai] [S32CT] Implement EPD/EPC support for HLD and IPLD ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "

ID	Subtype	Headline and Description
ARTD-5234	New	New Feature [ADC] Use HW logical for calling all extension APIs, instead of directly physical id" ,,"Use HW logical for calling all extension APIs, instead of directly physical id Make sure order of generation in the config struct for multiple instances& different logical IDs, is correct also in S32CT
ARTD-6079	Bug	[Port] Pins tool still config MSCR[SRC] bit when driver not support by hardware<*> Detailed description (how to reproduce it): Configuration some pins by pins tool in S32DS. Slew Rate is Slowest setting. Calling Siul2_Port_Ip_Init function with config pins has _Slew Rate is Slowest setting,_ bit MSCR[SRC] not set to 1 (Slowest setting). Test Case ID (internal TC that caught the defect) optional: IP_Port_Siul2_TC_0005 Observed behavior: Some pins has bit MSCR[SRC] default by hardware.
ARTD-6095	Bug	[S32K3XX][RM] XRDC does not trigger exception, cannot configure PIDM when using PID feature ,,"There is no exception when violate accessing memory with config enable PE bits follow 2 fomula below 10b The process identifier is included in the domain hit evaluation as defined by the following expression: partial_domain_hit = (PE == 10b) && ((PID & PIDM) == (PIDn[PID] & PIDM)) 11b The process identifier is included in the domain hit evaluation as defined by the following expression: partial_domain_hit = (PE == 11b) && ((PID & PIDM) == (PIDn[PID] & PIDM)) PIDM can not configure in EB interface Expect behavior: XRDC should trigger exception on wrong PID set up of domain when accessing memory. PIDM is configurable
ARTD-6219	Bug	[MCU] Some nodes are not active in S32 Configuration Tool<*> The following nodes are not active in S32 Configuration Tool: McuNoPLL; McuFxoscUnderMcuControl; McuFircUnderMcuControl; McuPll0UnderMcuControl; McuSxoscUnderMcuControl; McuSircUnderMcuControl. Please see attached file.
ARTD-6298	Bug	[SAI] Wrong transmit data after aborting/timeout transfer<*> Detailed description (how to reproduce it): Wrong transmit data after aborting/timeout transfer.

ID	Subtype	Headline and Description
		Please refer the MAF log and the logic analyzer Sai_Abort_Sending.logicdata: the first transmission is abort at middle, then try to send again !image-2021-01-14-11-07-28-788.png! Initialize SAI driver as master mode, master sends data with I2S protocol Initialize MAF I2S interface: slave mode, receiver and 8-bit word size SAI driver starts an asynchronous transaction on the SAI bus Wait until the SAI transmission status is not SAI_STATUS_BUSY Abort on going transfer Verification Point: The SAI transmission status is SAI_STATUS_ABORTED MAF waits until the transmitting transaction finishes Verify: the MAF return status is E_MAF_OK MAF test the received frames, compare with the passed data array with data in the MAF RX buffer Verification Point: + the MAF return status is E_MAF_OK + The callback counter for SAI_IP_RUN_ERROR event equals 1 SAI driver starts an asynchronous transaction on the SAI bus Wait until the SAI transmission status is not SAI_STATUS_BUSY Verification Point: The SAI transmission status is SAI_STATUS_COMPLETED MAF test the received frames, compare with the passed data array with data in the MAF RX buffer Verification Point: + the MAF return status is E_MAF_OK => Failed at this verification point + The callback counter for SAI_IP_RUN_ERROR event equals 0 DeInitializes the SAI module Preconditions: [...] Observed behavior: Wrong transmit data after aborting/timeout event Expected behavior: Correct transmit data after aborting/timeout event Proposed solution optional:
ARTD-6477	Bug	 [SAI] File version check missing for SchM_Sai header in Sai_Ip.c<*> File version checks
ARTD-6677	New	 New Feature [ADC] Add Memory Mapping ,,"Add memory map according to following guidelines: According Autosar memmap standard (AUTOSAR_SWS_MemoryMapping.pdf) The shortcut \{INIT_POLICY} means the initialization policy of variables. Possible INIT_POLICY postfixes are: NO_INIT*, used for variables that are never cleared and never initialized. CLEARED, used for variables that are cleared to zero after every reset. POWER_ON_CLEARED, used for variables that are cleared to zero only after power on reset. INIT*, used for variables that are initialized with values after every reset. POWER_ON_INIT, used for variables that are initialized with values only after power on reset. All global elements (variable, array, struct) that are initialized with 0 value (NULL,NULL_PTR) should be put in __INIT memory section. For example, following declaration is wrong*:

ID	Subtype	Headline and Description
		#define PORT_START_SEC_VAR**_NO_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" static const Port_ConfigType Port_pConfig = NULL_PTR; #define PORT_STOP_SEC_VAR**_NO_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" Should be corrected : #define PORT_START_SEC_VAR**_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" static const Port_ConfigType Port_pConfig = NULL_PTR; #define PORT_STOP_SEC_VAR**_INIT_**UNSPECIFIED_NO_CACHEABLE #include ""Port_MemMap.h"" Build environment need to update compiler option not to implicitly move zero-initialized elements to BSS-like memory section. Note: in GHS and GCC, bss-zero optimization is applied not in all cases, do not only check map file to find wrong memory mapping placement "
ARTD-7670	Bug	 [S32DS] Functional groups are not working correctly<*> 1. Create project enable RTD for S32G274_Rev2 2. Open Peripherals tool-> Add more functions using function group item on toolbar. 3. Add some components for each function 4. Export html report > each function contains their components information correctly in the content of HTML report. 5. Check source code generated. > There is no function from step 2 added into source code generated for all components. If the function group feature has not been supported yet, it should be disabled or removed from toolbar.
ARTD-7686	New	 New Feature [ADC] Extend HLD examples with DMA usecase ,,"the Adc DMA is a common application for customer, suggest to add a Adc DMA case Extend HLD EBT and S32CT examples with DMA usecase"
ARTD-7928	New	 New Feature [SAI] Optimize interrupt loops ,,"Optimize interrupt loops: Move switch outside while/for loops to avoid checking condition for each data written in FIFO"
ARTD-7938	New	 New Feature [ICU] Improve validation regarding input signals used on LPCMP ,,Analise and add validation based on available input channels used by CMP
ARTD-7964	New	 New Feature [ADC] Avoid sorting HW triggered channels when enabling hw triggered groups ,,"Avoid sorting HW triggered channels when enabling hw triggered groups Sorting is only required for DMA, because BCTU does not support issuing DMA request when conversion list is completed only interrupt. So this is required to trigger

ID	Subtype	Headline and Description
		DMA only after the last adc channel finishes conversion (the largest physical channel id) Ideas to optimize: reorder channels only for DMA but make sure order is same in result for DMA and interrupt, and Autosar requirement generate an array already sorted tbd how affects set channel feature others TBD"
ARTD-8151	New	 New Feature [gpt] Review changes according to Reference Manual (Rev2DraftB) ,,"Review changes according to Reference Manual (Rev2DraftB). [Link|https://nxp1.sharepoint.com/:b:/t/25_43/k344/EcYwLySwZpJNkMY2fbsfreMBsrEqt6vbefT0AM-VaRzIbw?e=UNoWjF] "IP_" prefix was added to all defines from the "Peripheral instance base addresses" section. Please update driver code with the new prefix."
ARTD-8152	New	 New Feature [pwm] Review changes according to Reference Manual (Rev2DraftB) ,,"Review changes according to Reference Manual (Rev2DraftB). [Link|https://nxp1.sharepoint.com/:b:/t/25_43/k344/EcYwLySwZpJNkMY2fbsfreMBsrEqt6vbefT0AM-VaRzIbw?e=UNoWjF] "IP_" prefix was added to all defines from the "Peripheral instance base addresses" section. Please update driver code with the new prefix."
ARTD-8155	New	 New Feature [spi] Review changes according to Reference Manual (Rev2DraftB) ,,"Review changes according to Reference Manual (Rev2DraftB). [Link|https://nxp1.sharepoint.com/:b:/t/25_43/k344/EcYwLySwZpJNkMY2fbsfreMBsrEqt6vbefT0AM-VaRzIbw?e=UNoWjF] "IP_" prefix was added to all defines from the "Peripheral instance base addresses" section. Please update driver code with the new prefix."
ARTD-8091	New	 New Feature [ADC] Add support for enable high speed conversion ,,"ADC_SAR on K3 supports high speed conversion. It is enabled by HSEN field found in AMSIO register. Enabling this allows ADC conversions to use a higher clock speed when doing conversions or calibrations."
ARTD-8098	New	 New Feature [S32K3XX][BASE] Update Header File to RM Rev.2. Draft B ,,Update Header File to latest RM revision: S32K3xx RM Rev.2. Draft B
ARTD-8225	Bug	 [S32K3][MCU] SWT1_RST is not supported in S32K314, S32K344, K312, K311 ,,"According Table 163. Register fields and applicability in S32K3XXRM Reference Manual Rev.2 Draft B, 02/2021. SWT1_RST dose not exist in S32K344 and S32K314

ID	Subtype	Headline and Description
		!image-2021-03-05-16-01-07-325.png! But in driver code supported SWT1_RST, it should be removed. and some macro must be remove SWT1_RST in S32K314 and S32K344 MC_RGM_FES_RWBITS_MASK32 include SWT1 MC_RGM_FES_IRQ_BITS_MASK include SWT1 MC_RGM_FERD_RWBITS_MASK include SWT1
ARTD-8230	Bug	 [PWM] Fix Typos in FlexIO API requirements<*> {code:c} Requirement FLEXIO_PWM_IP_005_001: Service name: Flexio_Pwm_Ip_UpdatePeriodDuty Syntax: Flexio_Pwm_Ip_StatusType Flexio_Pwm_Ip_UpdatePeriodDuty(uint8 instance, uint8 channel, uint ... OK Requirement FLEXIO_PWM_IP_006_001: Service name: Flexio_Pwm_Ip_GetOutputState Syntax: boolean Flexio_Pwm_Ip_GetOutputState(uint8 instanceId, uint8 channel) Sync/Async: Sync Reent ... should use one naming parameter (instance or instanceId) for all of apis to synchronize between the driver code and the requirement The Flexio source code has all APIs defeined with instanceId. FlexIO requirements should be updated to reflect this.
ARTD-8238	New	 New Feature [ICU][CMP] Create example for CMP and RTC-API ,,"Add example for using RTC-API and CMP as depicted in Reference Manual. The example should be as close as possible for manual/user verification (not automated) and included in plugin examples if possible. !image-2021-03-05-14-02-13-002.png|width=415,height=283!"
ARTD-8318	Bug	 [S32CT][LIN] Should not allow to select the same Flexio channel for Lin TX and Lin RX<*> On S32CT, at IPL, the LIN Flexio Rx Channel and LIN Flexio Tx Channel should not be assigned to the same MCL Flexio channel. There should be a error in the Problems view. Please check the attached file.
ARTD-8360	New	 New Feature [ADC] Refactor implementation of DMA stream optimization feature ,,"Refactor implementation of DMA stream optimization feature: implement similarly with DMA streaming without interrupt even if requires to have result reorder enabled. this would avoid the need to have channels consecutive in the group which is more restrictive than result reorder. Also need to remove checks from configurators remove DmaMuxSource and workaround to enable/disable in Adc_Ipw_StartDmaOperation"
ARTD-8365	New	 New Feature [ADC] S32CT IPL standalone mode must generate defines for IP instances used ,,"[ADC] S32CT IPL standalone mode must generate defines for IP instances used !image-2021-03-09-17-20-28-153.png|thumbnail!

ID	Subtype	Headline and Description
		Update also example"
ARTD-8373	Bug	[Adc] Mismatching information between Tresos and S32ConfigurationTool configurators when comparing layout<*> Detailed description (how to reproduce it): Step 1: Repo sync Adc module and dependent module Step 2: compile plugin and generate layout for S32DS Step 3: Config S32CT same with EB Step 4: Compare layout of S32CT with EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing layout CT: missing node *AdcClockSource* EB : redundant AdcHwTrigTimer node ** Some name of nodes different between EB with CT. Detail in *share point link*: https://nxp1.sharepoint.com/:x:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BD9A67063-B22E-47AE-A2C0-5D798377D1D2%7D&file=ADC_Compare_Node.xlsx&action=default&mobileredirect=true Expected behavior: All nodes on EB and CT should be the same
ARTD-8377	Bug	[Platform][S32K3] Code generate between EB and CT is not equivalent when disable interrupt monitoring<*> Detailed description* (how to reproduce it): # On EB and S32DS config Platform component with unchecked "Interrupt Monitoring Enabled" # Compare "Platform_CfgDefines.h" file !image-2021-03-10-14-50-15-113.png! Test Case ID (internal TC that caught the defect):* N/A Observed behavior:*_ The file "Platform_CfgDefines.h" between EB and S32DS is not equivalent Expected behavior: The file "Platform_CfgDefines.h" between EB and S32DS is equivalent
ARTD-8384	Bug	[LIN] Lin driver can't report timeout error caused by hardware error<*> In case run out of timeout, driver can't report timeout the error as requested in the requirements SWS_Lin_00097, SWS_Lin_00218
ARTD-8407	Bug	[S32K3][Mcu-clock] Wrong clocks frequency when disabling clock gating by calling Clock_Ip_DisableModuleClock()<*> Test procedure: Step1: Disables clock gating by calling Clock_Ip_DisableModuleClock() Step2: Check frequency values Expected result: The returned frequency is 0 !image-2021-03-11-14-07-07-392.png|width=757,height=315!
ARTD-8409	New	New Feature

ID	Subtype	Headline and Description
		[FLEXIO-LIN] - Add protocol timeout ,,Add protocol timeout on reception and transmission
ARTD-8420	Bug	 [GPT] Cannot start Pit with countValue set to maximum<*> Call of Gpt_StartTimer with Pit channel and argument value set to MAX value, it fails in function Pit_Ip_StartChannel on check: DevAssert(PIT_MAX_VALUE > countValue);}} It should be possible to use MAX value. The check should be updated to:}} DevAssert(PIT_MAX_VALUE >= countValue);}}{{}} Same check is used also in Stm_Ip_StartCounting and Ftm_Gpt_Ip_StartCounting. It should be fixed also there, if the hardware supports using maximal value.}}
ARTD-8427	Bug	 [SENT] Follow up - fix HIS and MISRA warnings<*> Detailed description (how to reproduce it): Fix HIS and MISRA warnings Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8429	Bug	 [RM] Add Ip level parameter input checks<*> Detailed description (how to reproduce it): Do not check input parameters of functions yet Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Do not check input parameters of functions yet Expected behavior: Check input parameters of functions Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check input parameters of functions
ARTD-8453	Bug	 [GPT] Case sensitive include file should be fixed<*> Detailed description (how to reproduce it): On Pit_Ip_Cfg.h , there is

ID	Subtype	Headline and Description
		#include "Pit_Ip_BOARD_INITPERIPHERALS_PBcfg.h" instead of #include "Pit_Ip_BOARD_InitPeripherals_PBcfg.h" (notice case sensitive) This should be fixed at it will not compile on Linux env. Picture attached Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8455	New	 New Feature [RM][S32K3XX] Fix and comment static analysis violations (MISRA + HIS + CERT-C) ,,"All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] "
ARTD-8461	Bug	 no pinmux configuration for CLKOUT in S32_CT<*> Detailed description (how to reproduce it): [...] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] - There is no pinmux configuration for CLKOUT in Pins of S32_CT
ARTD-8466	Bug	 [LIN] - Driver can't change status to LIN_TX_BUSY after Lin_SendFrame function called<*> Detailed description (how to reproduce it): Driver can't change status to LIN_TX_BUSY after Lin_SendFrame and Lin_GetStatus function called. Preconditions: In Lin_SendFrame driver set Lin_Ipw_au8LinChFrameStatus[u8Channel] = LIN_CH_READY_STATE; but if Lin_Ipw_au8LinChFrameStatus[u8Channel] = LIN_CH_READY_STATE then when function Lin_GetStatus called, it will return LIN_OPERATION status.

ID	Subtype	Headline and Description
		It must return LIN_TX_BUSY status. Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_1007 Observed behavior: Lin_GetStatus will return LIN_OPERATION status Expected behavior: Lin_GetStatus will return LIN_TX_BUSY status Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-8467	Bug	[LIN] The length of wake-up pulse generated by Flexio IP longer than standard<*> Detailed description (how to reproduce it): The length of wake-up pulse generated by Flexio IP is 23.53ms over LIN standard from 250 Amicros to 5ms Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Lin_TS_021 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8478	Bug	[LIN] Driver's autobaud rate feature fail<*> Detailed description (how to reproduce it): Driver's autobaud rate feature fail. Preconditions: Driver use Osif timer to check baudrate but It don't enable bit interrupt enable. So, driver can't goto interrupt handler function. Test Case ID (internal TC that caught the defect) optional: Ip_Lpuart_TC_FCT_0002 Observed behavior: Baudrate calculator incorrect Expected behavior: Baudrate calculator correct Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-8495	Bug	[PWM]: Correct and update Pwm driver for S32K1XX<*> Update Pwm driver for S32K1XX IPV FTM : Update the dithering is unavailable on the instance 0 in S32K1XX Flexio: Add Flexio_Pwm_Ip_GetPeriod() api Update the features are not supported for S32K1XX IPW

ID	Subtype	Headline and Description
		Integrate Flexio in IPW S32K1XX Update the validation functions in IPW HLD Add the validation api to check the SetOutputToIdle is not supported in FLEXIO channel in S32K1XX Correct Pwm driver for S32K1XX Correct the resource for S32K1XX Correct the CT to align with EBT
ARTD-8546	Bug	[SPI][FLEXIO] flexio driver cannot work when using flexio_logic_channel 3 4 5 6<*> Detailed description (how to reproduce it): the flexio driver cannot work when using flexio_logic_channel 3 4 5 6 for spi, but it can work when using flexio_logic_channel 0 1 2 3. !image-2021-03-16-14-48-01-287.png! Preconditions: flexio is enabled. Test Case ID (internal TC that caught the defect) optional: Int_TC_FCT_0301 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8551	Bug	[RM] Should not be select Physical core when disable multicore on S32CT and EBT<*> Detailed description (how to reproduce it): 1. Should not be select Physical core when disable multicore on S32CT and EBT. Please check the attached file. 2. The Region number on S32CT should be configurable. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Rm_TC_COT_0001 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8571	Bug	[MCU] Difference LABEL of nodes between S32CT and EB<*> Detailed description (how to reproduce it): Add MCU component on S32CT and EB Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior:

ID	Subtype	Headline and Description
		The description between S32CT and EB is the difference(see attached file) Expected behavior: Synchronize description between S32CT and EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-8579	Bug	[MCL-LCU][Tresos] Should check IcuLogicInput_UsingSwOverride before generate SwSynMode, SwValue ,,"Detailed description (how to reproduce it): [Tresos] Should check IcuLogicInput_UsingSwOverride before generate SwSynMode, SwValue Observed behavior: When IcuLogicInput_UsingSwOverride = false*, SwSynMode, SwValue still generated the value which is configured by user. Expected behavior: When IcuLogicInput_UsingSwOverride = false*, SwSynMode, SwValue should be generated the default value: <code> / boolean SwSynMode / LCU_IP_SW_SYNC_IMMEDIATE,\n</code> <code> / uint8 SwValue / LCU_IP_SW_OVERRIDE_LOGIC_LOW,\n</code> Only When IcuLogicInput_UsingSwOverride = true*, SwSynMode, SwValue generate the value which is configured by user. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8586	Bug	[ICU][S32K3XX] The ICU_GET_INPUT_LEVEL_API macro does not change according to the state of the button on the DS<*> Detailed description (how to reproduce it): The ICU_GET_INPUT_LEVEL_API macro does not change according to the state of the button on the DS. pls see attach file. Preconditions: Use DS3.4 project. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The ICU_GET_INPUT_LEVEL_API macro does not change according to the state of the button on the DS. pls see attach file. Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-8590	Bug	[CAN] #include <stdint.h> in FlexCAN_Ip_HwAccess.h when CCOPT+=-DNO_STDINT_H<*> Detailed description (how to reproduce it): Build CAN_TS_WIR_100 with CCOPT+=-D*NO_STDINT_H* on ghs compiler Preconditions:

ID	Subtype	Headline and Description
		ghs compiler Test Case ID (internal TC that caught the defect) optional: CAN_TS_WIR_100 with CCOPT+=-D*NO_STDINT_H is added to makefile Observed behavior: A build fail error: !image-2021-03-17-16-30-32-132.png! NOTE_*_: Inclusion should be investigated and being fixed if if is implemented in wrong way !image-2021-03-17-16-30-01-692.png! Proposed solution optional: [...]
ARTD-8591	Bug	 [ICU][S32K3XX] Value 'true' is generated in DS project configuration<*> Detailed description (how to reproduce it): Still has the value 'true' in the generation file in DS. pls see attach file Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8614	Bug	 Lpi2c CT generated code error<*> Detailed description (how to reproduce it): in s32ds 3.4, configuration tool, add lpi2c module into the new project, update code. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There are only two header files included in the generated file "Lpi2c_Ip_Cfg.h" #include "Mcal.h" #include "OsIf.h" Expected behavior: #include "Mcal.h" #include "OsIf.h" #include "Lpi2c_Ip_BOARD_InitPeripherals_PBcfg.h" Note:*_ Proposed solution optional: Add the line into "Lpi2c_Ip_Cfg.h" #include "Lpi2c_Ip_BOARD_InitPeripherals_PBcfg.h"
ARTD-8617	Bug	

ID	Subtype	Headline and Description
		[GPT] Pit_Ip_StartChannel reading CVAL value while timer is disabled doesn't follow Reference Manual<*> Detailed description (how to reproduce it): In S32K3 RTD 0.8.1 GPT driver, these below piece of code in Pit_Ip_StartChannel: !image-2021-04-02-15-45-01-973.png! After writing to RTI_LDVAL, driver will wait for PIT to copy value configured in RTI_LDVAL to RTI_CVAL by polling RTI_CVAL in Pit_Ip_GetCounterValue(). However, in previous state, (Gpt_Init()), timer was disabled, and reading RTI_CVAL is not recommended due to the fact that RTI_CVAL will not return a correct value, as shown in S32K3 reference manual. Preconditions: Gpt_StartTimer() is called, channel PIT is used Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Driver is reading RTI_CVAL while timer is disabled, which is not recommended by RM. Expected behavior: Implementation follows with RM Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-8625	New	 New Feature [ADC] Extend resolution to allow reading 15b register value for similar format as DMA transferred data ,,"NewWorkDescription: Implement method for the user to get raw register value, instead of value calculated based on the resolution set in the configurator. This is necessary since DMA will bypass any resolution conversions that are done in the driver and the module will always write 15-bits to the data register. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-8636	Bug	 [S32K3xx][RM] Cortex- M7_1 only supports on S32K32x<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: RM_TC_0010 Observed behavior: Cortex M7_1 only supports on S32K32x, so resource of S32K33x and S32K31x need to remove Cortex M7_1 Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A

ID	Subtype	Headline and Description
ARTD-8652	Bug	[S32G2XX][S32K344][S32K1XX][Example] OCU: Duplicate number of paragraphs in 'description.txt' file of some example project<*> Precondition:* Open S32SD3.4 update1 which installed package SW32_RTD_4.4_1.0.0_HF01_D2102_DS_Updatesite.zip! Step: 1.Import all example project for S32G: 2. Open description.txt then check content Observed behavior: Duplicate number of catalogue " 3.2 Compiling the application" and " 3.2 Running the application on the board" Wdg_Example_IPL_DS Wdg_Example_HLD_DS Uart_HLD_S32G_DS_Example Linflexd_Uart_Ip_S32G_DS Spi_IP_example_CT_S32G Spi_HLD_example_CT_S32G Qdec_Ip_example_DS Qdec_example_DS Port_example_DS Ocu_Ftm_example_DS Ocu_example_DS Ocotp_IP_Example Ocotp_AUTOSAR_Example Lin_example_IPV Lin_example_HLD Icu_Siul2_Wkpu_example Icu_Ftm_example Icu_ASR_example I2c_S32G274A_IP_DS I2c_S32G274A_HLD_DS Example_S32G2XX_DS_Qspi_Ip Example_S32G2XX_DS_Fls Fee_Example_S32G2 Eth_Example_DS_002 Eth_Example_DS_001 Example_S32G2XX_DS_Eep Dio_example_DS_S32G Hse_Ip_Read_Hse_Attr Hse_Ip_Aes_Enc_Async_Irq Crypto_Hash Crypto_Cmac_Gen_Ver Crypto_Aes_Enc_Dec FlexCAN_example_CT CAN_example_CT Adc_example_DS_IP Adc_example_DS Expected behavior: Number of catalogue is updated correctly
ARTD-8648	Bug	[ADC] ADC_ReadGroup when called for group with DMA does not return result masked according to resolution<*> Detailed description (how to reproduce it): ADC_ReadGroup when called for group with DMA, does not return result masked according to resolution

ID	Subtype	Headline and Description
		Instead returns result on 15bits Observed behavior: Result is returned on 15bits Expected behavior: Result is returned masked according to selected resolution Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update Adc_Ipw_MaskConvResult
ARTD-8646	Bug	[ADC] Fix VSMD error EcucSws_1008 for AdcChannelId node and update Adc channel names stated by RM or IOMUX<*> Detailed description (how to reproduce it): Add AdcChannelName which is an ENUMURATION node having value is channel name stated in RM or IOMUX sheet. Fix VSMD error EcucSws_1008 by changing the attribute of AdcChannelId node from ENUMURATION to INTEGER. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8661	Bug	[ETH][S32CT] The value for .enableCtrl (in generated code) should be upper case<*> Detailed description (how to reproduce it): When CCOPT+=-DNO_STDINT_H is enabled, the tests failed due to .enableCtrl value (in Gmac_Ip_BOARD_InitPeripherals_PBcfg.c file) is lower case (false/true). Please check the attached file. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Eth_TS_COT_001 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8680	Bug	[ADC] Build failed with ADC group software trigger, when no HW triggers configured ,,"Detailed description (how to reproduce it): Build failed with ADC group software trigger In EB tresos, create new project and add ADC module

ID	Subtype	Headline and Description
		Configure a simple group with trigger source is software(please refer the xdm file in the attachment) Generate code Build project with GHS compiler => Error: S32K3XX/eclipse/plugins/Adc_TS_T40D34M9I0R0/include/Adc_Ipw_Types.h"", line 395: error #94: the size of an array must be greater than zero const uint8 au8HwTriggIndex[ADC_MAX_HARDWARE_TRIGGERS]; /**< Hardware trigger sources in configuration array / make: [Makefile:325: Adc.o] Error 1 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Build error with GHS compiler with ADC group software trigger Expected behavior: No error when compiling with ADC group software trigger Note: in the ""Expected behavior"" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8710	Bug	[ICU] Align HLD and IPL for Signal Measurement and Timestamp<*> Detailed description (how to reproduce it): Align HLD and IPL for Signal Measurement and Timestamp. Allow HLD DMA only in HLD side to be configured and serviced. IPL DMA should be only on IPL side to be handled by user notification. Processing of Signal Measurement and Timestamp should be done on IPL level and use pointers to variables to get the results on HLD. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8726	Bug	[LIN] a redundant pulse sent before sending break<*> Detailed description (how to reproduce it): A redundant pulse is sent before break field when using IPV FlexIO as the image attached Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior:

ID	Subtype	Headline and Description
		[...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8749	Bug	[ICU] DMA notification handlers function is not generated in DS<*> Detailed description (how to reproduce it): DMA notification handlers function (IcuChannel_0_MclDmaTransferCompletionNotif) is not generated in DS. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8841	New	New Feature [can] Remove TypeReferenceDef in .component ,,"All uses of TypeReferenceDef (i.e. element <reference></reference>) shall be removed in favor of the structure described in [this presentation| https://nxp1.sharepoint.com/sites/Zebra/_layouts/15/Doc.aspx?OR=teams&action=edit&sourcedoc=%7B28A51BA3-C452-40F5-ABB6-A6933671DCD3%7D]. In a nutshell, each TypeReferenceDef element shall be replaced with the referenced type."
ARTD-8780	New	New Feature [BUILD_ENV] Update compiler options to enable hardware FPU, remove short-enums, optimize zero initializers" ,,"We need to update the list of compiler options and memmap implementation following the compiler options alignment accross sw products: use hard fp remove short-enums remove no_discard_zero_init Changes should be applied for all compilers Source: https://nxp1.sharepoint.com/:x:/s/Zebra/EU7fT8Ur1jZAsou6FoOO-3MBrWTd1WdnvcVdNuqwLzncxg?e=LvE8aL
ARTD-8795	Bug	[LIN][FLEXIO] - Lin bus is not idle after the transfer has completed successfully.<*> Detailed description (how to reproduce it): After the transfer is completed successfully the node state is not IDLE Preconditions: [...]

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Flexio_Lin_Ip_GotoIdleState must be called after reporting via the callback that the transfer is completed without errors.
ARTD-8799	New	 New Feature [SPI][FLEXIO] Improve configuration of hardware resources follow new mcl update. ,,"NewWorkDescription: Mcl will update to add one more pin selection in each flexio channel because SPI want to select PINs for both Shifter and Timer registers which were lock per Flexio channel. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Mcl will update to add one more pin selection in each flexio channel because SPI want to select PINs for both Shifter and Timer registers which were lock per Flexio channel."
ARTD-8801	Bug	 [ADC] Adc_ValidateQueueNotFull is redundant with HW trigger groups<*> Detailed description (how to reproduce it): Hw queue is removed completely in ARTD-2316 then no need to check queue full for HW trigger groups. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove ADC_E_QUEUE_FULL_LIST input param when calling Adc_ValidateExtraParams in Adc_EnableHardwareTrigger and Adc_DisableHardwareTrigger
ARTD-8809	New	 New Feature [MCL] TRGMUX multicore support ,,"NewWorkDescription: Add multicore support for TRGMUX IP. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add multicore support for TRGMUX IP in driver code EBT S32CT."
ARTD-8823	Bug	

ID	Subtype	Headline and Description
		[S32K3][LIN-FLEXIO] Work only with channel 0 configured for Rx<*> Detailed description (how to reproduce it): When configured Rx channel different 0, LIN driver can not work Preconditions: configured Rx channel different 0 Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8874	Bug	[S32XX][DIO] Not run test when write to Port K on S32R45<*> Detailed description (how to reproduce it): Execute(generate, build, run) Dio_TS_701 from repo test_dio When invoke Dio_MaskedWritePort() or Dio_WriteChannelGroup() with PortId=9 (port K) =>stop by hard fault When write value to Port 9 by MAF, Dio_ReadPort() is working incorrect: these two lines need to swap in Dio_ReadPort() PortLevel = (Dio_PortLevelType)(PortLevel & Dio_aAvailablePinsForRead[PortId]); PortLevel = (Dio_PortLevelType)(PortLevel & Dio_Ipw_ReverseBits(Dio_aAvailablePinsForRead[PortId])); Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: TS: Dio_TS_701 TC: Dio_TC_FCT_0214 Dio_TC_FCT_0205 Observed behavior: Test not run when write to Port K: Dio_TC_FCT_0214: line 181, using Dio_MaskedWritePort() with PortId=9 (port K) Dio_TC_FCT_0205: line 134, using Dio_WriteChannelGroup() with ChannelGroupIdPtr.port=9 (port K) Expected behavior: Write successfully, no error
ARTD-8890	Bug	[FLEXIO_Sent][CT] Wrong component name and duplicate component in Manager SDK Components tab<*> Detailed description (how to reproduce it): Step 1: Create new project. Step 2: Select project > right click > S32 Configuration tool > Manage SDK components Step 3: Check all components that there are no duplicate component name Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Wrong component name and duplicate component in Manager SDK Components tab.

ID	Subtype	Headline and Description
		Detail was attached. Expected behavior: Remove an instance and update the component's name from Flexio to Flexio_Sent*
ARTD-8960	Bug	 [MCU] FXOSC not stable when set GM_SEL = 0000b<*> Detailed description (how to reproduce it): The description of field GM_SEL have note: - In Crystal mode FXOSC will not function with zero transconductance (GM_SEL = 0000b). - For details on how to set this field, see Initializing FXOSC. But in configuration user can configure GM_SEL = 0000b in Crystal mode. that is root cause FXOSC not stable Preconditions: Crystal overdrive protection = 0 Test Case ID (internal TC that caught the defect) optional: 1001 Observed behavior: FXOSC not stable Expected behavior: FXOSC stable Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In Crystal mode make an invalid in configuration when user configure Crystal overdrive protection (GM_SEL) = 0000b In Single-Input Bypass mode write 0000b to Crystal overdrive protection (GM_SEL)
ARTD-8963	Bug	 [LIN] The requirement CPR_RTD_00311.lin is not covered<*> Detailed description (how to reproduce it): The requirement CPR_RTD_00311.lin is not covered by driver. "In order to provide support for importing configuration information from different formats (i.e. DBC, LDF, FIBEX, AUTOSAR system description ARXML), the so-called ComImporter shall be registered in the CAN/LIN/FlexRay/Eth driver module's plugin.xml file." Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: ComImporter is not registered in plugin.xml Expected behavior: ComImporter is registered in plugin.xml Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: PLG_USE_COMIMPORTER is set to true in Lin.mak
ARTD-8961	Bug	 [CAN][S32XX] Wrong HwObjectID in CanTxTimestampNotification() when using interrupt mode<*> Detailed description (how to reproduce it): Configure CAN as below: The first hw object is HRH, the second Hw object is HTH

ID	Subtype	Headline and Description
		In case of Tx processing is set to Interrupt mode, the driver code always uses _Can_pHwObjectConfig_ ptr (this specifies the first HRH) to notify timestamp for the current transmission , so the timestamp notification is wrong for the hw transmit object. !image-2021-03-30-10-47-11-829.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8964	Bug	[SENT] Checking invalid channel of sent HLD layer is incorrect<*> Detailed description (how to reproduce it): Using channelId is equal with number of sent channel as parameter of Sent_GetFastChannelMsgData and Sent_GetSerialChannelMsgData, driver should report DET error of invalid channel id but actually not. Preconditions: Using channelId is equal with number of sent channel as parameter of Sent_GetFastChannelMsgData and Sent_GetSerialChannelMsgData Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Driver should report DET error of invalid channel Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change this condition (u8ChannelId > SENT_NUMBER_CONFIGURED_CHANNELS) to (u8ChannelId >= SENT_NUMBER_CONFIGURED_CHANNELS) Tester should create a new testcase to cover this case
ARTD-9016	New	New Feature [MCU] Support configuration for CMU on S32CT ,,"In the generated clock settings file ""Clock_Ip_PBcfg.c"", there is a huge structure ""Clock_Ip_ClockConfigType Mcu_aClockConfigPB[1]"". In this structure, there is one sub-structure called ""Clock_Ip_CmuConfigType"". There are 3 elements in this structure definition but there are 6 data provided in the generated code. So there is compiler warning ""../board/Clock_Ip_PBcfg.c:1568:21: warning: excess elements in struct initializer"" Can we fix this? And I didn't see any CMU related settings in the clock diagram view in S32DS CT. Is there plan to add CMU support in the RTD configuration?"
ARTD-9052	Bug	[icu] Fix all M4, TABs, duplicated UUIDs

ID	Subtype	Headline and Description
		,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://kara.ea.freescale.net/0/project/custom_plugincheck/details http://adriatic.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.03.31 baseline.
ARTD-9034	New	 New Feature [ADC] Updates for ctu hardware trigger optimization ,,"NewWorkDescription: The feature should be updated for K3 release because it was partially updated in ARTD-1434 Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-9136	Bug	 [crypto] Fix file version checking<*> Detailed description (how to reproduce it): Fix all violation version checking Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: [...] Expected behavior: No file version checking errors. Please ensure all violations fix for your driver, reference link: [http://kara.ea.freescale.net/0/project/custom_file_verchecking/details] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] - NewWorkDescription: Fix all file version checking for RTD drivers Requirement source: Attachment baseline report on 2021.04.01 Proposed solution optional: [...]
ARTD-9131	Bug	 [ADC] DMA group with limit check enabled, still get status stream complete with out of range voltage

ID	Subtype	Headline and Description
		,,"Detailed description (how to reproduce it): DMA hw trigger group with out of range voltage still get status stream complete Preconditions: Dma hw trigger group config with AN_2: Range between 1000 and 3000 Voltage for AN_2: 1.8V (4095) Transfer by DMA with interrupt Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1401 Observed behavior: Set voltage to AN_2: 1.8V Enable hw trigger group and trigger Wait status as stream complete Expected: Timeout occurred Real status: time out was not reached and group status is stream complete Expected behavior: Group can not get status as stream complete because out of range voltage Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-9201	Bug	s32k3 QSPI pin direction type<*> Detailed description (how to reproduce it): QSPI IO0 IO3 shoud be configuread as input/output for its direction property. Observed behavior: QSPI IO0 IO3 can be configured in S32DS CT as either input or output. But they cannot be configured as input/output. Proposed solution optional: It would be good that these pins can be configured as input/output and it would be good to add an "input/output" option in the attached dialog box.
ARTD-9208	Bug	[ADC] DMA HW trigger single one shot normal group with only 1 channel and with interrupt, is not working ,,"Detailed description (how to reproduce it): DMA HW trigger single one shot normal group transfer wrong place in data buffer Preconditions: Using DMA HW trigger one shot normal group Group have 1 channel Optimize streaming reorder off without interrupt = off Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0102 Adc_TC_FCT_0107 Adc_TC_FCT_0109 (Adc_TS_014 cfg 3) Observed behavior: Enable hw trigger dma 1 channel group Loop to trigger 3 times Read group in each trigger Status: Read group buffer did not update after 3 triggers Result buffer data have 3 elements after 3 triggers

ID	Subtype	Headline and Description
		Expected behavior: Read group buffer update after 3 triggers Result buffer data have 1 elements after 3 triggers Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-9209	New	 New Feature [adc] [S32CT] Implement EPD/EPC support for HLD and IPL S32K3 ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "
ARTD-9210	Bug	 ADC] CT ADC_SAR_IP missing the generated struct for ADC1<*> Detailed description (how to reproduce it): In CT, create the configuration for ADC0 and ADC1 then generate code => Missing the struct configuration for Adc_sar_1 !image-2021-02-26-15-37-57-027.png! Test Case ID (internal TC that caught the defect) optional: Adc_sar_TC_FCT_0001 Observed behavior: Missing the struct configuration for Adc_sar_1 Expected behavior: Can generate the struct configuration for Adc_sar_1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-9211	Bug	 [Platform][S32CC] S32CT generate redundancy Platform_Ipw_NonCoreConfigType structs when dissable S32K3XX_MSCM_CFG<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		1. Creating new project for Platform on S32CT, add Platform, Ecuc, Os component to project. 2. Generate code with default config (*dissable generic interrupt settings configurable). 3. Opening Platform_Ipw_Cfg.c , Platform_Ipw_NonCoreConfigType structs is redundancy, Because When MSCM dissable Platform_Init not Initializes Platform_Ipw_InitNonCore. Opening IntCtrl_Ip_Cfg.c IntCtrl_Ip_GlobalRouteConfigType structs is redundancy. 4. Compare config generate CT and EB is different with config dissable MSCM. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: !image-2021-04-02-16-05-42-884.png! !image-2021-04-02-16-06-13-135.png! !image-2021-04-02-17-13-41-755.png! Expected behavior: Remove Platform_Ipw_NonCoreConfigType structs if dissable MSCM on S32CT const Platform_Ipw_NonCoreConfigType ipwNonCoreConfig = { NULL_PTR } ; In IntCtrl_Ip_Cfg.c : Remove IntCtrl_Ip_GlobalRouteConfigType structs and IntCtrl_Ip_IrqRouteConfigType structs Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9204	Bug	CLONE - [SPI][FLEXIO] Shifter error flag set after latest frame is sent in slave mode<*> Shifter error flag set after latest frame is sent in slave mode. Currently, driver have added a workaround to prevent this issue. So it should be investigated to get the root cause of issue
ARTD-9225	Bug	[ADC] Error appears in S32ConfigurationTool when AdcEnableThresholds is checked on a channel but AdcEnableWatchdogApi is disabled<*> Detailed description (how to reproduce it): 1. Create a DS project 2. Add Adc component 3. Enable AdcEnableWatchdogApi 4. Enable AdcEnableThresholds on any channel on any hardware unit 5. Disable AdcEnableWatchdogApi Observed behavior: This error is shown: "This Unit has configured some Channels that have enabled the watchdog feature and need to use interrupts, so the associated Watchdog interrupt must be enabled in Adc/AdcInterrupts container." Expected behavior: No error should be shown. Proposed solution optional: Whenever AdcEnableThresholds value is checked, it's enable state must also be checked.
ARTD-9226	New	New Feature

ID	Subtype	Headline and Description
		[ADC] ADC_SAR IPL add support in configurator for ADC DMAEN and DMAR ,,"NewWorkDescription: ADC_SAR IPL add support in configurator for ADC DMAEN and DMAR Currently ADC SAR IP has support for updating DMAEN and DMAR only at runtime via dedicated functions. Support needs to be added also in configurator Requirement source: Improvement Proposed solution optional: Add checkbox in AdcHwUnit container: Enable DMA for End of Channel. If chain interrupts do not work in parallel with DMAEN true, then consider instead of checkbox, to add Adc Transfer Type enum ADC_INTERRUPT/ADC_DMA as in HLD (to make DMA vs INTERRUPT mutual exclusive) Add checkbox in channel configurator: End of conversion DMA enable. Update Adc_Sar_Ip_Init function "
ARTD-9227	Bug	[ADC] DMA Clear Source cannot be configured in low-level driver configurator<*> Detailed description (how to reproduce it): DMA Clear Source cannot be configured in IPL configurator Adc Transfer Type is always ADC_INTERRUPT for ADC Unit, so DMA Clear Source is always disabled Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: DMA Clear Source cannot be configured in IPL configurator Expected behavior: DMA Clear Source can be configured in IPL configurator Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: DMA Clear Source must always be configurable, Remove also Adc Transfer Type from IPL configurator, because it is not used, and Adc Sar Ip driver currently only offers support to configure DMAEN and DMAR using runtime functions. When ARTD-9226 is implemented, DMA Clear Source will become read-only when DMA is disabled.
ARTD-9233	New	New Feature [FLS] Support configuration of PFCR4[BLK4_PS] bitfield for C40 ,,"NewWorkDescription: Add support for the PFCR4[BLK4_PS] bitfields to allow the user to select the pipe to be used for accessing the flash block 4. !image-2021-04-04-15-03-19-551.png|thumbnail! Requirement source: S32K3xx_RM_Rev2DraftB.pdf (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add list to select"
ARTD-9231	Bug	[ICU] Code generator of ICU_GET_INPUT_LEVEL_API incorrect<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Logic S32CT code generation of macro ICU_GET_INPUT_LEVEL_API is wrong. When comparing to S32CT code generation EMIOS_ICU_GET_INPUT_LEVEL_API Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-04-03-21-04-39-946.png! !image-2021-04-03-21-05-48-189.png! Expected behavior: !image-2021-04-03-21-06-17-434.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9315	Bug	[ADC] Build fail: "DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS" is undefined when using adc group with 1 channel, without scatter gather ,,"Detailed description (how to reproduce it): Build fail: ""DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS"" is undefined when using adc group with 1 channel, without scatter gather Preconditions: Adc 0 using transfer type ADC_DMA and groups have only 1 channel Disable dmaLogicChannel_EnableScatterGather on mcl driver Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0101 Observed behavior: Build fail error: e:/gitwork_rt/output/S32XX_S32G2XX/adc/Adc_TS_014_cfg3_CORE4/generate_tresos/src/Adc_Ipw_VS_0_PBcfg.c"", line 270: error #20: identifier ""DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS"" is undefined .au32DmaNumSgaElement = { DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS, DMA_LOGIC_CH_1_NOF_CFG_SGA_ELEMENTS }, Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-9415	New	New Feature [adc] Updated module to fully support CPR_RTD_00563 ,,"NewWorkDescription: Implement requirement: CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions: In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.

ID	Subtype	Headline and Description

		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		
		The requirement was already partially supported by ADC module, only update required to fully support this requirement is to update the way ADC_PRECOMPILE_SUPPORT is generated. Instead of it being generated only when precompile support is enabled, it will be always generated and will have STD_ON value when precompile support is enabled and STD_OFF when precompile support is disabled. The other change needed will be to update Adc_Init to throw {{ADC_E_PARAM_POINTER}} error instead of
		{ADC_E_PARAM_CONFIG}} when the wrong config parameter is given."

ARTD-9430	New	 New Feature [lin] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile ,,"NewWorkDescription:

ID	Subtype	Headline and Description

		Implement requirement:
		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ARTD-9436	New	 New Feature [port] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile ,,"NewWorkDescription: Implement requirement:

ID	Subtype	Headline and Description

		CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:
		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ARTD-9437	New	 New Feature [pwm] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile ,,"NewWorkDescription: Implement requirement: CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:

ID	Subtype	Headline and Description

		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ARTD-9440	New	 New Feature [sai] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile ,,"NewWorkDescription: Implement requirement: CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:

ID	Subtype	Headline and Description

		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ARTD-9441	New	 New Feature [sent] Implement CPR_RTD_00563 to allow NULL_PTR at Init at precompile ,,"NewWorkDescription: Implement requirement: CPR_RTD_00563: If the parameter checking for the Initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions:

ID	Subtype	Headline and Description

		In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value.
		In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR.
		If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Default Error Tracer (Det)
		Requirement source:
		AUTOSAR_SRS_BSWGeneral
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Generate the defined <MIP>_PRECOMPILE_SUPPORT in <Driver>_Cfg.h
		EBT Tresos:
		{code:c}
		#define <MIP>_PRECOMPILE_SUPPORT [!IF ""(IMPLEMENTATION_CONFIG_VARIANT != 'VariantPostBuild') and (variant:size() <= 1)""!](STD_ON)[!ELSE!](STD_OFF)[!ENDIF!]
		UCT:
		{code:c}
		[!
		var configSet = this[0];
		var functionalGroupsList = this[2];
		var implementationConfigVariant = configSet.getChildById(""ConfigTimeSupport.IMPLEMENTATION_CONFIG_VARIANT"").getValue();
		!]
		...
		#define <MIP>_PRECOMPILE_SUPPORT ($((implementationConfigVariant != ""VARIANT-POST-BUILD"") && (functionalGroupsList.length <= 1))? ""STD_ON"" : ""STD_OFF""$)
		In <Driver>.c the code that contained parameter checking for init function shall be:
		{code:c}
		#if (STD_ON == <MIP>_PRECOMPILE_SUPPORT)
		if (NULL_PTR != pConfigPtr)
		#else
		if (NULL_PTR == pConfigPtr)
		#endif / <MIP>_PRECOMPILE_SUPPORT /
		Note:
		The Module implementation prefix <Mip> shall be formed in the following way: <Ma>[_<vi>_<ai>] Where <Ma> is the Module abbreviation of the BSW Module (SWS_BSW_00101), <vi> is its vendorId and <ai> is its vendorApiInfix. The sub part in square brackets [_<vi>_<ai>] is omitted if no vendorApiInfix is defined for the BSW Module. For Complex Drivers and transformers, the <Mip> is directly derived from the apiServicePrefix.
		The Capitalized module implementation prefix <MIP> is the Module implementation prefix completely written in upper case.
		"

ARTD-9345	Bug	[CRC] When Dma Feature is enable, need to check that CrcDmaLogicChannelName is assigned value or not ,,"Preconditions: DMA feature is enable User did not configure dma channel Observed behavior: When generate code, user get an error without any guideline to fix it

ID	Subtype	Headline and Description
		Expected behavior: Need to check that CrcDmaLogicChannelName is assigned value or not. If not, need to show: why user get the error how to fix it Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9346	Bug	[S32CC][CRC] When multi cores enable, CrcPartitionRefOfChannel must be assigned. ,,"Preconditions: Step 1: Enable Multi cores feature Step 2: Add a Partition for CrcEcucPartitionRef Step 3: Add 2 configuration for Crc Channels Configuration Step 4: Only configure CrcPartitionRefOfChannel for 1st channel Observed behavior: Although 2nd channel was not configured CrcPartitionRefOfChannel But Configurator still generate configuration file successfully without error or generate an error without guideline for user about this issue (why issue happen, how to fix it) Expected behavior: Need to raise error this case
ARTD-9359	Bug	S32K3 CLKOUT_RUN is not mapped to PINs configuration<*> Detailed description (how to reproduce it): When configuring the pins, we found that CLKOUT_RUN and CLKOUT_STANDBY are not mapped to the desired pins. For example, PTD14, ALT7 function should be CLKOUT_RUN. But it's not present in PTD14 function options in the pins configuration tool. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: N/A
ARTD-9398	Bug	[ADC] Wrong generated code for 'presampling internal voltage' when 'AdcBypassSampling' is 'false'<*> Detailed description (how to reproduce it): [ADC] Wrong generated code for 'presampling internal voltage' when 'AdcBypassSampling' is 'false' In EBT, Disable AdcBypassSampling Select AdcPresamplingInternalSignal0 is VREFH Select AdcPresamplingInternalSignal1 is VREFH Click generate code Verification Point: the presampling voltage is VREFH => FAILED The generated code is

ID	Subtype	Headline and Description
		.aPresamplingSource = { ADC_SAR_IP_PRESAMPLE_VREFL, ADC_SAR_IP_PRESAMPLE_VREFL } The issue also occurs on S32CT. !image-2021-04-07-18-28-52-920.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-9456	New	
		New Feature
		
		[fls] Include the platform in a single point based on generated data
		,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons.
		The proposal is to use a generated header file like: <Ip>_Ip_CfgDefines.h and centralize all platform header includes in it.
		Example for EB Tresos generator:
		[!NOCODE![!// Include specific header file
		[!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""![!//
		[!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""![!//
		[!CODE![!WS ""0""!]#include ""S32K344_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""![!//
		[!CODE![!WS ""0""!]#include ""S32G274A_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""![!//
		[!CODE![!WS ""0""!]#include ""S32R45_PIT.h""[!CR![!ENDCODE![!//
		[!ENDIF![!//
		[!ENDIF![!//
		[!ENDNOCODE![!//
		Example for UCT as generator:
		[!
		if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3""))
		{
		<code>#include ""S32K344_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2""))
		{
		<code>#include ""S32G274A_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45""))
		{
		<code>#include ""S32R45_PIT.h""\n</code>
		}
		!]
		"

ARTD-9458	New	

ID	Subtype	Headline and Description

		New Feature
		
		[gpt] Include the platform in a single point based on generated data
		,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons.
		The proposal is to use a generated header file like: <lp>_lp_CfgDefines.h and centralize all platform header includes in it.
		Example for EB Tresos generator:
		[!NOCODE![!// Include specific header file
		[!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""![!//
		[!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""![!//
		[!CODE![!WS ""0""!]#include ""S32K344_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""![!//
		[!CODE![!WS ""0""!]#include ""S32G274A_PIT.h""[!CR![!ENDCODE![!//
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""![!//
		[!CODE![!WS ""0""!]#include ""S32R45_PIT.h""[!CR![!ENDCODE![!//
		[!ENDIF![!//
		[!ENDIF![!//
		[!ENDNOCODE![!//
		Example for UCT as generator:
		[!
		if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3""))
		{
		<code>#include ""S32K344_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2""))
		{
		<code>#include ""S32G274A_PIT.h""\n</code>
		} else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45""))
		{
		<code>#include ""S32R45_PIT.h""\n</code>
		}
		!]
		"

ARTD-9460	New	New Feature [icu] Include the platform in a single point based on generated data ,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons. The proposal is to use a generated header file like: <lp>_lp_CfgDefines.h and centralize all platform header includes in it. Example for EB Tresos generator: [!NOCODE![!// Include specific header file [!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""![!// [!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""![!// [!CODE![!WS ""0""!]#include ""S32K344_PIT.h""[!CR![!ENDCODE![!// [!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""![!// [!CODE![!WS ""0""!]#include ""S32G274A_PIT.h""[!CR![!ENDCODE![!//

ID	Subtype	Headline and Description
		[!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""!][!// [!CODE!][!WS ""0""!]#include ""S32R45_PIT.h""[!CR!][!ENDCODE!][!// [!ENDIF!][!// [!ENDIF!][!// [!ENDNOCODE!][!// Example for UCT as generator: [! if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3"")) { <code>#include ""S32K344_PIT.h""\n</code> } else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2"")) { <code>#include ""S32G274A_PIT.h""\n</code> } else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45"")) { <code>#include ""S32R45_PIT.h""\n</code> } !] "
ARTD-9469	New	New Feature [rm] Include the platform in a single point based on generated data ,,"Generate the platform header include based on generated data. This way the platform name and specifics are centralized in one point only and to avoid using the compiler option define which is subject to change due to objective reasons. The proposal is to use a generated header file like: <lp>_Ip_CfgDefines.h and centralize all platform header includes in it. Example for EB Tresos generator: [!NOCODE!][!// Include specific header file [!IF ""node:exists(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative)""!][!// [!IF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ResourceSubderivative, 's32k3')""!][!// [!CODE!][!WS ""0""!]#include ""S32K344_PIT.h""[!CR!][!ENDCODE!][!// [!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32g2')""!][!// [!CODE!][!WS ""0""!]#include ""S32G274A_PIT.h""[!CR!][!ENDCODE!][!// [!ELSEIF ""contains(as:modconf(""Resource"")[1]/ResourceGeneral/ ResourceSubderivative, 's32r45')""!][!// [!CODE!][!WS ""0""!]#include ""S32R45_PIT.h""[!CR!][!ENDCODE!][!// [!ENDIF!][!// [!ENDIF!][!// [!ENDNOCODE!][!// Example for UCT as generator: [! if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32K3"")) { <code>#include ""S32K344_PIT.h""\n</code> } else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32G2"")) { <code>#include ""S32G274A_PIT.h""\n</code> } else if (scriptApi.getProfile().getMcuInfo().getPartNumber().contains(""S32R45"")) { <code>#include ""S32R45_PIT.h""\n</code> }

ID	Subtype	Headline and Description
		!] "
ARTD-9523	Bug	[ADC] Compilation error when ADC EOC interrupt disabled and all configured groups are having without interrupt optimization enabled S32K3<*> NewWorkDescription: Compilation error when ADC EOC interrupt disabled and all configured groups are having without interrupt optimization enabled, because .pfEndOfNormalChainNotification = Adc_Ipw_Adc0EndNormalChainNotification, is generated in Adc_Sar_Ip_PBcfg.c Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: When all groups are configured with "without interrupt" feature enabled and ADC EOC interrupt is disabled in AdcInterrupts tab, .pfEndOfNormalChainNotification must be generated as NULL_PTR
ARTD-9538	Bug	[ICU] Measurement properties and channel edge alignment are incorrectly generated for Autosar in DS<*> Detailed description (how to reproduce it): In ICU_MODE_SIGNAL_MEASUREMENT mode, when config channel's measurement property is ICU_DUTY_CYCLE, the output file is generated ICU_LOW_TIME. And in ICU_MODE_EDGE_COUNTER mode, when config a channel's edge alignment is ICU_BOTH_EDGES, the output file is generated ICU_FALLING_EDGE. Preconditions: Set up 2 channels of the same name but on 2 different instances of emios, when changing the properties of the second channel, the generate file does not change Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: When changing the properties of the second channel, the generate file does not change Expected behavior: The generate file must change according to the change of the channel Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change Macro_GetLogicChannelInfo(EmiosChannelConfig.getChildById("Name").getValue()) to Macro_GetLogicChannelInfo(searchStr)
ARTD-9543	Bug	[ADC] Generating errors with BctuDevErrorDetect, BctuTimeoutMethod and BctuTimeoutValue when enabling Config Time Support ,,"Detailed description (how to reproduce it): Generating errors appear with BctuDevErrorDetect, BctuTimeoutMethod and BctuTimeoutValue when enabing config time support and click apply button !image-2021-03-31-08-57-12-099.png|thumbnail! !image-2021-03-31-09-00-18-136.png|thumbnail! The log disappears right away and no generating errors when click ""generate"" button or generate test by cmd

ID	Subtype	Headline and Description
		Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9537	Bug	[ICU][S32DS] Errors are reported when configuring multiple variants in DS<*> There are two mainly problem with S32DS when configuring many variant: Firstly, when i switch between variants (VS0,VS1, VS2) the node in IcuGeneral section in S32DS interface also change. This section should be not changeable when user switch to other VS. Secondly, some error with output configuration as the attached picture. Adittionally, checking with test suite Icu_TS_DS_M04 contains 10 config set.
ARTD-9548	Bug	[BASE][BUILD_ENV] Some compiler options are not the same between SOW and S32CT<*> Detailed description (how to reproduce it): Step 1: Create new project. Step 2: Select project > right click > Properties > C/C Build > Settings Step 3: Check compiler options and compare with SOW file Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Some compiler options are not the same between SOW and S32CT : Linker: Duplicate: mcpu=cortex-m7 in RTD_Compiler_Option.xlsx In file *SOW*: Map*=<map_file_name>* but *CT* is: Map* Expected behavior: Update compiler option for CT the same with compiler option in SOW file.
ARTD-9557	Bug	[PORT] Clock out pin configuration generated wrong<*> Clock out pin configured wrong. Pls see attached.
ARTD-9596	Bug	[ADC] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD

ID	Subtype	Headline and Description
		!image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml and <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the validation steps: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example:

ID	Subtype	Headline and Description
		<SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRIFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https://confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9598	Bug	[MCU] Generate different paths of Clock_Ip_Cfg_Defines.h between enable SDK and no enable SDK on S32DS<*> Preconditions: S32DS 3.4 Update 1 (B210204) SW32_RTD_4.4_1.0.0_HF01_D2102_DS_Updatesite Test Case 1 1. Create project without enable S32CT and SDK 2. Open Configuration Tools a+' Update code 3. Create project with enable S32CT and SDK 4. Open Configuration Tools a+' Update code 5. Compare path of file Clock_Ip_Cfg_Defines.h between project at step 2 and project at step 4 Observed behavior: 5. Different path: Step 2: path="generate/include/Clock_Ip_Cfg_Defines.h Step 4: path="board/Clock_Ip_Cfg_Defines.h" Expected behavior: 5. Same path
ARTD-9599	Bug	[RTD_4.4_S32CC_2.0.0] Could not open S32 RTD AUTOSAR 4.4 D2104 Release Notes on getting started page<*> Detailed description (how to reproduce it): 1. Open S32DS

ID	Subtype	Headline and Description
		2. Help > Getting Started Page > EXTENSIONS\RESOURCES tab. Select "S32 RTD AUTOSAR 4.4 D2104" package 3. Click on "S32 RTD AUTOSAR 4.4 D2104 Release Notes" to open Release Note Observed behavior: 3." Your file couldn't be accessed " because name of file is not match with name in itm.s32xx.rtd.collateral.PlatformSDK_S32G_2021_04.xml (Please see attached file) Expected behavior: 3. Open file successfully
ARTD-9675	Bug	[adc] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4:

ID	Subtype	Headline and Description
		The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9676	Bug	[can] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4:

ID	Subtype	Headline and Description
		All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9681	Bug	[eep] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9682	Bug	

ID	Subtype	Headline and Description
		[eth] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9683	Bug	[fls] OsIf timeout implementation is non-uniform across drivers<*> Issue #1:

ID	Subtype	Headline and Description
		The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9614	Bug	[S32XX] Project show duplicate file and folder after updating code with project which not attach SDK RTD<*> Precondition:* Open S32SD3.4 update1 which installed package S32CC_RTD_4_4_RTM_2_0_0_DS_updatesite_2104.zip Step: 1.Create project for S32R45/S32G2

ID	Subtype	Headline and Description
		2. Select Project > Open configuration by click to "Open S32 Configuration" icon in the toolbar 3. In Create a new configuration window, select core for processor > Finish 4. Update code 5. Import any example for S32R45/ S32G2 6. Open S32CT tool then update code Observed behavior: Project show duplicate file and folder in 'generate/include' ,'generate/src' and 'generate' Expected behavior: Project show only one 'generate' folder
ARTD-9643	New	 New Feature CLONE - [SPI] Improvement SpiPhyUnit configuration can be stored to a pointer in Ip_StateStructure variable ,,"SpiPhyUnit configuration can be stored to a pointer in Ip_StateStructure variable. So, No need to copy many variables value to Ip_StateStructure in Ip_Init() anymore."
ARTD-9644	New	 New Feature CLONE - [SPI] Improvement External device configuration can be stored to a pointer in Ip_StateStructure variable ,,"External device configuration can be stored to a pointer in Ip_StateStructure variable. So, No need to copy many variables value to Ip_StateStructure in Ip_SyncTransmit() or Ip_AsyncTransmit() anymore."
ARTD-9653	Bug	 [ADC] Adc_ReadGroup does not re-enable Dma HW Request and update destination address if limit check failed for Group Without Interrupt<*> Detailed description (how to reproduce it): Adc_ReadGroup does not re-enable Dma HW Request and update destination address if limit check failed for Group Without Interrupt. So the Dma Internal Buffer was not up to date at triggering second time Preconditions: Group hardware trigger oneshot Without interrupt = on Transferring by dma with 1 channel Limit check is enable range between from 1000 to 3000 Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1407 Adc_TC_FCT_1408 (Adc_TS_013 cfg 8) Observed behavior: Set voltage for ADC0 AN_2 as 1.8V (0xfff) Adc_EnableHardwareTrigger(t_u16AdcGroupType); Start trigger first time Loop until read group return E_OK Expect time out occured Set voltage for ADC0 AN_2 as 1V (0x93B) Start trigger second time Loop until read group return E_OK Expect time out not occured Real status time out occured because buffer u32DmaNoIrqBuffer was not updated

ID	Subtype	Headline and Description
		Expected behavior: Buffer u32DmaNoIrqBuffer was updated Time out not occured with voltage in range Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Adc_TC_FCT_1408 is sw continuous group with same sequence and have the same issue: Buffer u32DmaNoIrqBuffer was not updated Proposed solution optional: NA
ARTD-9659	Bug	[ICU] The MAX_PARTITIONS value and Icu_Config variable wrong in DS in HL<*> Detailed description (how to reproduce it): The MAX_PARTITIONS value is wrong in DS in HL. In EB tresos: MAX_PARTITIONS = maxcoreId 1 Icu_Config is declared as const Icu_ConfigType const Icu_Config [MAX_PARTITIONS] but in DS: MAX_PARTITIONS = size of 'IcuEcucPartitionRef' Icu_Config is declared as const Icu_ConfigType const Icu_Config [size of 'IcuEcucPartitionRef'] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: MAX_PARTITIONS = size of 'IcuEcucPartitionRef' Icu_Config is declared as const Icu_ConfigType const Icu_Config [size of 'IcuEcucPartitionRef'] Expected behavior: MAX_PARTITIONS = maxcoreId 1 Icu_Config is declared as const Icu_ConfigType const Icu_Config [MAX_PARTITIONS] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update generate code for MAX_PARTITIONS in Icu_Cfg.h
ARTD-9661	Bug	[EB] All examples S32R45 but CORTEXM are S32G2XXM7<*> Detailed description (how to reproduce it): Step 1. Open the Windows command prompt window Step 2. Change the current directory to the example application folder Step 3. To generate the Tresos project of the example, execute the following command to build: make generate Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: All examples S32R45 but CORTEXM are S32G2XXM7. Detail was attached Expected behavior: CORTEXM update is S32R45XM7 for R45 of all examples Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9672	Bug	

ID	Subtype	Headline and Description
		[GPT] Disable the GptTimeoutMethod feature if it's not used<*> Detailed description (how to reproduce it): in case that GptTimeoutMethod features is not used should be readonly Preconditions: using a ds configuration Test Case ID (internal TC that caught the defect) optional: Ip_Pit_TC_FCT_0001 Observed behavior: GptTimeoutMethod feature is enabled in ds Expected behavior: GptTimeoutMethod feature should be disabled as it is in ebt Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: disable GptTimeoutMethod feature if it s not necessary
ARTD-9708	Bug	[RM][S32K3XX] Add Ip level parameter input checks<*> Detailed description (how to reproduce it): Do not check input parameters of functions yet Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Do not check input parameters of functions yet Expected behavior: Check input parameters of functions Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check input parameters of functions
ARTD-9705	Bug	[ADC] Adc_ReadGroup can return E_OK and result for uncomplete current group channel without interrupt if we did not read previous group<*> Detailed description (how to reproduce it): Adc_ReadGroup can return E_OK and result for uncomplete current group channel if we did not read previous group Preconditions: Limit check is enable Group without interrupt Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1410 Adc_TS_013 cfg 1 Observed behavior: Set voltage for AN_2 in range and data passing through limit check and not implement Adc_ReadGroup Adc_EnableHardwareTrigger(t_u16AdcGroupType); T_ADC_StartTrigger(t_u16AdcGroupType); T_TIMER_DelayMs(T_ADC_DELAY_VALUE); T_ADC_StopTrigger(t_u16AdcGroupType); Adc_DisableHardwareTrigger(t_u16AdcGroupType); Set voltage for AN_2 out of range Adc_EnableHardwareTrigger(t_u16AdcGroupType);

ID	Subtype	Headline and Description
		EU_ASSERT(E_OK != Adc_ReadGroup(t_u16AdcGroupType, t_readGroupBuffer)); Adc_DisableHardwareTrigger(t_u16AdcGroupType); Expected: Adc_ReadGroup return E_NOT_OK because not triggering for current group Real status: Adc_ReadGroup return E_OK Expected behavior: Adc_ReadGroup return E_NOT_OK because not triggering for current group Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) CPR_RTD_00049.adc: Adc_ReadGroup shall return conversation results only if all channels of the triggered group have completed their conversion This issue related to ARTD-5796: [ADC] Using Adc_Sar_Ip_GetConvData for checking conversion is completed, based on valid bit, will not wait for conversion to finish if previously completed conversion wasn't read already Proposed solution optional: NA
ARTD-9685	Bug	 [gpt] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3:

ID	Subtype	Headline and Description
		All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9697	Bug	[sai] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY"] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM

ID	Subtype	Headline and Description
		OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9699	Bug	[spi] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example:

ID	Subtype	Headline and Description
		Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9701	Bug	[uart] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"

ID	Subtype	Headline and Description
ARTD-9702	Bug	[wdg] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4: All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9737	Bug	[crypto] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the

ID	Subtype	Headline and Description
		note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https://confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9745	Bug	[i2c] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution

ID	Subtype	Headline and Description
		Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2

ID	Subtype	Headline and Description
		Make sure exclusive areas are available in generate_swcd\swcd \<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/ AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY" >/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https:// confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9750	Bug	[S32XX RTM][S32K1 EAR][S32K3 RTM] OCU: Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions

ID	Subtype	Headline and Description
		2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/ NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</ SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/ Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd \<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/ AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL>

ID	Subtype	Headline and Description
		<IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY" >/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https://confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9754	Bug	[port] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup.

ID	Subtype	Headline and Description
		ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https://confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9755	Bug	[pwm] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions:

ID	Subtype	Headline and Description
		N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs.

ID	Subtype	Headline and Description
		Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https://confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9758	Bug	[sai] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1

ID	Subtype	Headline and Description
		Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml:

ID	Subtype	Headline and Description
		<EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/ AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY" >/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https:// confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9763	Bug	[wdg] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration

ID	Subtype	Headline and Description
		2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3

ID	Subtype	Headline and Description
		Validate the <Driver>_Bswmd.arxml file following steps from: https://confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-9800	Bug	 [ETH][S32CT] Incorrect constraint for EthEcucPartitionRefDef<*> Detailed description (how to reproduce it): # Enabled multicore (EthMulticoreSupport = true) # Configure 2 controllers and use the same partition for both controllers. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: An error is incorrectly reported by "EthEcucPartitionRefDef": "The referenced ECUC partition isn't used by any ETH controller (i.e. EthConfigSet/EthCtrlConfig/EthCtrlEcucPartitionRef)" even though it is used by 2 controllers. Expected behavior: No error is reported as it is a valid use case to have multiple controller assigned to the same partition. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: For node "EthEcucPartitionRefDef", the constraint counting the number of controllers referencing the partition should be changed to:{code:java} <constraint level="error" cond_expr="countOccurrences(system::getChildrenByASPath(`/AUTOSAR/EcucDefs/Eth/EthConfigSet/EthCtrlConfig/EthCtrlEcucPartitionRef`), x > (x.getValue() == $this.getValue())) >= 1" description="The referenced ECUC partition isn't used by any ETH controller (i.e. EthConfigSet/EthCtrlConfig/EthCtrlEcucPartitionRef)"/>
ARTD-9727	New	 New Feature [GPT] Trigger Support for LPCMP ,,"The RTC configuration doesn't support the TRIGGER functionality for the LPCMP operation in STANDBY mode (section ""56.1.6 Interaction with RTC API to cause wakeup"" of the RM). For now, It has to be manually ""Ored"" in the application code. RTC->RTCC = RTC_RTCC_TRIG_EN_MASK;"
ARTD-9731	Bug	 [S32DS] Problematic Default Project<*> Detailed description (how to reproduce it): When creating a new empty project with the RTDs v0.9.0, it doesn't compile by default. To fix it, the user needs to Open the Peripherals CT, Add the Siul2Port component, and Update code and rebuild. The same conflict appears when creating a project from an Example, in this case, all the missing components have to be added. Preconditions: New S32DS Application Project, or New S32DS Project from Example. Observed behavior:

ID	Subtype	Headline and Description
		Errors (3 items) fatal error: SchM_Mcu.h: (No such file or directory) Expected behavior: No Errors.
ARTD-9732	Bug	[crypto] OsIf timeout implementation is non-uniform across drivers<*> Issue #1: The names of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Crypto, Pmic, Fls have "<Module>TimeoutOsifCounterType" Eep has "timeoutCounterType" Uart has "UartTimeoutType" The rest of them have "<Module>TimeoutMethod" Solution #1: All drivers shall rename the node introduced by ARTD-2232 to "<Module>TimeoutMethod". For example: CryptoTimeoutMethod FlsTimeoutMethod UartTimeoutMethod EepTimeoutMethod ... Issue #2: The names of the enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eep, Pmic have ["SYSTEM", "CUSTOM", "DUMMY'] Crypto has ["SYSTEM", "CUSTOM", "TICKS"] Fls has ["SYSTEM", "CUSTOM", "LOOP] Adc, Lin, Ocotp, Spi have ["SystemTimer", "CustomTimer", "DummyTimer"] Gpt has ["OSIF_COUNTER_SYSTEM, "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_NOT_USED"] The rest of them have ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM", "OSIF_COUNTER_DUMMY"] Solution #2: All drivers shall rename the enumeration values of the node introduced by ARTD-2232 as follows: DummyTimer/Dummy/Ticks/etc > OSIF_COUNTER_DUMMY SystemTimer/System/etc >OSIF_COUNTER_SYSTEM CustomTimer/Custom/etc > OSIF_COUNTER_CUSTOM Issue #3: The available enumeration values of the node introduced by ARTD-2232 are inconsistent across drivers. For example: Eth, Fr, I2c have only two enumeration values: ["OSIF_COUNTER_SYSTEM", "OSIF_COUNTER_CUSTOM" Solution #3: All drivers shall define the following three enumeration values for the node introduced by ARTD-2232: OSIF_COUNTER_DUMMY OSIF_COUNTER_SYSTEM OSIF_COUNTER_CUSTOM Issue #4: The default enumeration value of the node introduced by ARTD-2232 is inconsistent across drivers. For example: Eth, I2c, Uart have a default value of "OSIF_COUNTER_SYSTEM" Solution #4:

ID	Subtype	Headline and Description
		All drivers shall set the default value of the node introduced by ARTD-2232 to "OSIF_COUNTER_DUMMY"
ARTD-9833	New	New Feature [S32K3XX] Update MPU start end address format ,,"During configuring the MPU component in S32DS CT, the start address, end address and size of a region are in decimal format. It would be good if change its default format to hex value. See attached figures."
ARTD-14705	Bug	[BASE] "hasExclusiveOwnership" always throws error when the calling component is disabled ,,"Preconditions: S32DS 3.4 U1 B210415 S32CC_RTD_4_4_RTM_2_0_0_DS_updatesite_2104 (210413) Test Case ID (internal TC that caught the defect) optional: 1. Create project for S32R45 enable RTD 2. Open Peripherals tool 3. Add GMAC component 4. Disable GMAC component Observed behavior: The errors are still showed when disable component. The configurations in EthGeneral tab is still light. Expected behavior: The error should be disappeared and the configuration should be gray when disable component.
ARTD-9844	Bug	[CAN] [ds compared] wrong generated code for FifoWarnNotif/FifoOverflowNotif callbacks<*> Detailed description (how to reproduce it): CAN_TS_095 / S32K148 make generate for EB and S32CT => Verification point: two output should be similar => fail at this step code generated for fifo in all controllers (enhanced & legacy) in controller configuration array will be similar with latest controller. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_0950 Observed behavior: !image-2021-04-16-14-52-34-442.png! Expected behavior: generated code of s32ct should be similar as EB's one Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9852	Bug	[PORT] The BSWMD cannot link to the Non-ASR function<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		The PORT_EXCLUSIVE_AREA_04 do not linked to any API in after generate plugin with GENERATE_BSWMD_FILE=ON. The attachments are the output's BSWMD file and the exclusive input's .dox file. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The PORT_EXCLUSIVE_AREA_04 do not linked to any API in after generate plugin with GENERATE_BSWMD_FILE=ON Expected behavior: The PORT_EXCLUSIVE_AREA_04 need to linked to Port_ResetPinMode Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-9905	Bug	[ADC]Header files found in src folder<*> For the components mentioned in the issue title, there are some header files misplaced under src folder and not under include folder. In Model-Based Design Toolbox for MATLAB and Simulink, we generate the projects automatically and need to copy all the dependencies. We explect to find only header files in the include and src files in src folder. This pattern is satisfied for all other modules but not for the mentioned ones. Also, the RTD veresion is 0.9.0 released on 26th of March, but in Jira I was not able to find this version marked as "Released". !image-2021-04-19-11-50-22-549.png!!image-2021-04-19-11-53-11-912.png! !image-2021-04-19-11-57-04-010.png! !image-2021-04-19-11-58-12-914.png!
ARTD-9911	New	New Feature [ADC] Improve documentation for Adc Set Clock Mode API ,,"NewWorkDescription: [ADC] Improve documentation for Adc Set Clock Mode API Add a separate chapter in ""Driver usage and configuration tips"" For details please see attached email thread."
ARTD-9944	Bug	[CAN] Wrong constraint implementation for ECUC_Can_00113<*> Detailed description (how to reproduce it): Create S32K148 project Check range for Can Timeout Duration field in EB and S32CT Expected range: Range [1E-6 .. 65.535] (0.000001 > 65.535) EB range: 0.01 > 65.535 => uncorrect S32CT range: 0.00001 > 65.535 => uncorrect Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: detail in attached file Expected behavior: the range of EB and CT should be corrected as ECUC_Can_00113 srs

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-9991	New	
		New Feature
		
		[adc] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344

ID	Subtype	Headline and Description
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES))) EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE) endif To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"". 3. Caveats: For this to work properly, you need to: # Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and core folders, where applicable) if the same example spans multiple derivatives (e.g. ""make/DS/S32R45/M7/Crc_Ip_Example.mak"" and ""make/DS/S32G274A/M7/Crc_Ip_Example.mak""). Consequently, EXAMPLE_LIST will also have to be changed accordingly (e.g. ""EXAMPLE_LIST = Crc_Ip_Example_S32R45_DS Crc_Ip_Example_S32G274A_DS"" > ""EXAMPLE_LIST = DS/S32R45/M7/Crc_Ip_Example DS/S32G274A/M7/Crc_Ip_Example"" !screenshot-1.png|thumbnail! # Set the makefile variable(s) EXAMPLE_DERIVATIVE (and EXAMPLE_CORE_TYPE, where applicable) before setting EXAMPLE_NAME # Use immediate assignment (":=" instead of "=") for the makefile variable EXAMPLE_NAME"
ARTD-9995	New	New Feature [crypto] Example project's name shall respect naming convention ,,"1. What to do: All example projects shall respect the following naming convention: EBT Example Naming Convention: {code}<module_name>_<short_description>_<target> S32DS Example Naming Convention: HLD: {code}<module_name>_<short_description>_<target> Unshared IP: {code}<ip_name>_Ip_<short_description>_<target> Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target> Where: <target> = <derivative> on platforms with a single core type <target> = <derivative>_<core_type> on platforms with multiple core types HLD Naming Examples: Eth_InternalLoopback_S32G274A_M7 for S32G2 Eth_InternalLoopback_S32K148 for S32K1 Eth_InternalLoopback_S32K344 for S32K3 IP Naming Examples: Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2 Enet_Ip_InternalLoopback_S32K148 for S32K1 Gmac_Ip_InternalLoopback_S32K344 for S32K3 2. How to do: To avoid having to manually maintain this, all the example makefiles shall contain the following: S32CC (where S32G274A will be replaced by the derivative you are targeting in that example): EXAMPLE_DERIVATIVE := S32G274A EXAMPLE_CORE_TYPE := M7 ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES))) EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)

ID	Subtype	Headline and Description

		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_
		$(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"",
		then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that
		example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword
		$(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_
		$(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"",
		then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that
		example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword
		$(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_
		$(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"",
		then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of
		the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak"").
		This will force you to create separate configurator and derivative folders (and
		core folders, where applicable) if the same example spans multiple derivatives
		(e.g. ""make/DS/S32R45/M7/Crc_Ip_Example.mak"" and ""make/DS/S32G274A/
		M7/Crc_Ip_Example.mak""). Consequently, EXAMPLE_LIST will also have to be
		changed accordingly (e.g. ""EXAMPLE_LIST = Crc_Ip_Example_S32R45_DS
		Crc_Ip_Example_S32G274A_DS"" > ""EXAMPLE_LIST = DS/S32R45/M7/
		Crc_Ip_Example DS/S32G274A/M7/Crc_Ip_Example""
		!screenshot-1.png|thumbnail!
		# Set the makefile variable(s) EXAMPLE_DERIVATIVE (and EXAMPLE_CORE_TYPE,
		where applicable) before setting EXAMPLE_NAME
		# Use immediate assignment (":=" instead of "=") for the makefile variable
		EXAMPLE_NAME"

ARTD-9998	New	 New Feature [eth] Example project's name shall respect naming convention ,,"1. What to do: All example projects shall respect the following naming convention: EBT Example Naming Convention: {code}<module_name>_<short_description>_<target> S32DS Example Naming Convention: HLD: {code}<module_name>_<short_description>_<target> Unshared IP: {code}<ip_name>_Ip_<short_description>_<target> Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target> Where: <target> = <derivative> on platforms with a single core type <target> = <derivative>_<core_type> on platforms with multiple core types

ID	Subtype	Headline and Description

		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and core folders, where applicable) if the same example spans multiple derivatives (e.g. ""make/DS/S32R45/M7/Crc_Ip_Example.mak"" and ""make/DS/S32G274A/M7/Crc_Ip_Example.mak""). Consequently, EXAMPLE_LIST will also have to be changed accordingly (e.g. ""EXAMPLE_LIST = Crc_Ip_Example_S32R45_DS Crc_Ip_Example_S32G274A_DS"" > ""EXAMPLE_LIST = DS/S32R45/M7/Crc_Ip_Example DS/S32G274A/M7/Crc_Ip_Example""
		!screenshot-1.png|thumbnail!

ID	Subtype	Headline and Description
		# Set the makefile variable(s) EXAMPLE_DERIVATIVE (and EXAMPLE_CORE_TYPE, where applicable) before setting EXAMPLE_NAME # Use immediate assignment (":=" instead of "=") for the makefile variable EXAMPLE_NAME"
ARTD-9983	Bug	 s32k3 FLS AutosarExt core selection<*> Detailed description (how to reproduce it): Create an S32K3 RTD SDK project and add the component "Fls", we can see the settings in "Fls Configuration => AutosarExt => Fls Using Core" is with wrong information. The core select pull-down list is not correct for S32K344 or S32K324 It still lists the CM33 core which is for s32k2tv not for s32k3xx See attached figure. Proposed solution optional: It should be FLS_CM7_CORE for S32K344 It should be FLS_CM7_CORE_0 or FLS_CM7_CORE_1 for S32K324
ARTD-9985	Bug	 s32k324 s32ds project cannot add Fee component<*> Detailed description (how to reproduce it): Create an S32K324 project in S32DS3.4 with RTD 0.9.0. Try to add the component Fee, but it's missing in the list. I can see Fls but cannot see Fee. If creating an S32K344 project, it's able to add Fee component. Proposed solution optional: Add Fee component support for S32K324
ARTD-10020	New	 New Feature [sai] Example project's name shall respect naming convention ,,"1. What to do: All example projects shall respect the following naming convention: EBT Example Naming Convention: {code}<module_name>_<short_description>_<target> S32DS Example Naming Convention: HLD: {code}<module_name>_<short_description>_<target> Unshared IP: {code}<ip_name>_Ip_<short_description>_<target> Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target> Where: <target> = <derivative> on platforms with a single core type <target> = <derivative>_<core_type> on platforms with multiple core types HLD Naming Examples: Eth_InternalLoopback_S32G274A_M7 for S32G2 Eth_InternalLoopback_S32K148 for S32K1 Eth_InternalLoopback_S32K344 for S32K3 IP Naming Examples: Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2 Enet_Ip_InternalLoopback_S32K148 for S32K1 Gmac_Ip_InternalLoopback_S32K344 for S32K3 2. How to do: To avoid having to manually maintain this, all the example makefiles shall contain the following:

ID	Subtype	Headline and Description

		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak"").
		This will force you to create separate configurator and derivative folders (and core folders, where applicable) if the same example spans multiple derivatives (e.g. ""make/DS/S32R45/M7/Crc_Ip_Example.mak"" and ""make/DS/S32G274A/M7/Crc_Ip_Example.mak""). Consequently, EXAMPLE_LIST will also have to be changed accordingly (e.g. ""EXAMPLE_LIST = Crc_Ip_Example_S32R45_DS Crc_Ip_Example_S32G274A_DS"" > ""EXAMPLE_LIST = DS/S32R45/M7/Crc_Ip_Example DS/S32G274A/M7/Crc_Ip_Example""
		!screenshot-1.png|thumbnail!
		# Set the makefile variable(s) EXAMPLE_DERIVATIVE (and EXAMPLE_CORE_TYPE, where applicable) before setting EXAMPLE_NAME
		# Use immediate assignment (":=" instead of "=") for the makefile variable EXAMPLE_NAME"

ARTD-10021	New	New Feature [sent] Example project's name shall respect naming convention ,,"1. What to do: All example projects shall respect the following naming convention: EBT Example Naming Convention:

ID	Subtype	Headline and Description

		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"".
		S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K344
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"".
		3. Caveats:
		For this to work properly, you need to:
		# Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and

ID	Subtype	Headline and Description
		core folders, where applicable) if the same example spans multiple derivatives (e.g. ""make/DS/S32R45/M7/Crc_Ip_Example.mak"" and ""make/DS/S32G274A/M7/Crc_Ip_Example.mak""). Consequently, EXAMPLE_LIST will also have to be changed accordingly (e.g. ""EXAMPLE_LIST = Crc_Ip_Example_S32R45_DS Crc_Ip_Example_S32G274A_DS"" > ""EXAMPLE_LIST = DS/S32R45/M7/Crc_Ip_Example DS/S32G274A/M7/Crc_Ip_Example"" !screenshot-1.png|thumbnail! # Set the makefile variable(s) EXAMPLE_DERIVATIVE (and EXAMPLE_CORE_TYPE, where applicable) before setting EXAMPLE_NAME # Use immediate assignment (":=" instead of "=") for the makefile variable EXAMPLE_NAME"

ARTD-10058	New	
		New Feature
		
		[gpt] Example project's name shall respect naming convention
		,,"1. What to do:
		All example projects shall respect the following naming convention:
		EBT Example Naming Convention:
		{code}<module_name>_<short_description>_<target>
		S32DS Example Naming Convention:
		HLD: {code}<module_name>_<short_description>_<target>
		Unshared IP: {code}<ip_name>_Ip_<short_description>_<target>
		Shared IP: {code}<ip_name>_<module_name>_Ip_<short_description>_<target>
		Where:
		<target> = <derivative> on platforms with a single core type
		<target> = <derivative>_<core_type> on platforms with multiple core types
		HLD Naming Examples:
		Eth_InternalLoopback_S32G274A_M7 for S32G2
		Eth_InternalLoopback_S32K148 for S32K1
		Eth_InternalLoopback_S32K344 for S32K3
		IP Naming Examples:
		Gmac_Ip_InternalLoopback_S32G274A_M7 for S32G2
		Enet_Ip_InternalLoopback_S32K148 for S32K1
		Gmac_Ip_InternalLoopback_S32K344 for S32K3
		2. How to do:
		To avoid having to manually maintain this, all the example makefiles shall contain the following:
		S32CC (where S32G274A will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32G274A
		EXAMPLE_CORE_TYPE := M7
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)
		else
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE)_$(EXAMPLE_CORE_TYPE)
		endif
		To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32G274A_M7"".
		S32K1XX (where S32K148 will be replaced by the derivative you are targeting in that example):
		EXAMPLE_DERIVATIVE := S32K148
		ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES)))

ID	Subtype	Headline and Description
		EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE) endif To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K148"". S32K3XX (where S32K344 will be replaced by the derivative you are targeting in that example): EXAMPLE_DERIVATIVE := S32K344 ifeq ($(firstword $(SUPPORTED_CORE_TYPES)),$(lastword $(SUPPORTED_CORE_TYPES))) EXAMPLE_NAME := $(basename $(notdir $(lastword $(MAKEFILE_LIST))))_ $(EXAMPLE_DERIVATIVE) endif To illustrate this, if your example's makefile is named ""Eth_InternalLoopback.mak"", then EXAMPLE_NAME will be evaluated to ""Eth_InternalLoopback_S32K344"". 3. Caveats: For this to work properly, you need to: # Remove the platform/derivative name and configurator name from the filename of the makefile (e.g. ""Crc_Ip_Example_S32R45_DS.mak"" > ""Crc_Ip_Example.mak""). This will force you to create separate configurator and derivative folders (and core folders, where applicable) if the same example spans multiple derivatives (e.g. ""make/DS/S32R45/M7/Crc_Ip_Example.mak"" and ""make/DS/S32G274A/M7/Crc_Ip_Example.mak""). Consequently, EXAMPLE_LIST will also have to be changed accordingly (e.g. ""EXAMPLE_LIST = Crc_Ip_Example_S32R45_DS Crc_Ip_Example_S32G274A_DS"" > ""EXAMPLE_LIST = DS/S32R45/M7/Crc_Ip_Example DS/S32G274A/M7/Crc_Ip_Example"" !screenshot-1.png|thumbnail! # Set the makefile variable(s) EXAMPLE_DERIVATIVE (and EXAMPLE_CORE_TYPE, where applicable) before setting EXAMPLE_NAME # Use immediate assignment (":=" instead of "=") for the makefile variable EXAMPLE_NAME"
ARTD-10104	Bug	[CAN] EPCtoDS importer fail when "Check ECUC-MODULE-DEF value" is selected ,,"Detailed description (how to reproduce it): Create a project on S32K148 Generate any configuration to get CAN.epc file Import to S32CT the above CAN.epc file (""Check ECUC-MODULE-DEF value"" is enabled by default) => error as in attached file Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: I see only CAN has this error. Expected behavior: No error when importing CAN.epc Proposed solution optional: [...]
ARTD-10125	Bug	[PWM] eMIOS channel prescaler (clock divider) and prescaler clock source is not initialized when prescaler is disabled<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description

		The PWM driver does not initialize the eMIOS channel prescaler (UCEXTPRE) and eMIOS channel prescaler clock source (UCPRECLK) is case the prescaler clock (UCPREN) is disabled ("Clock prescaler" configuration parameter configured to EMIOS_PWM_CLOCK_NONE). The code which skips the initialization is as follows in Emios_Pwm_Ip_InitChannel:
		/ Configure internal prescaler /
		if (_EMIOS_PWM_CLOCK_NONE != userChCfg->internalPs)
		{
		Emios_Pwm_Ip_SetExtendedPrescaler(base, userChCfg->channelId, userChCfg->internalPs);
		Emios_Pwm_Ip_SetPrescalerSource(base, userChCfg->channelId, userChCfg->internalPsSrc);
		Emios_Pwm_Ip_SetPrescalerEnable(base, userChCfg->channelId, TRUE);
		}
		This is needed for the use case to have the PWM channel clock disabled after Pwm_Init() until it will be enabled by application.
		Preconditions:
		Prescaler clock disabled in eMIOS channel configuration.
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		eMIOS channel prescaler (UCEXTPRE) and eMIOS channel prescaler clock source (UCPRECLK) is not initialized by Pwm_Init() in case the prescaler clock (UCPREN) is disabled ("Clock prescaler" configuration parameter configured to EMIOS_PWM_CLOCK_NONE).
		Expected behavior:
		eMIOS channel prescaler (UCEXTPRE) and eMIOS channel prescaler clock source (UCPRECLK) is initialized by Pwm_Init() in case the prescaler clock (UCPREN) is disabled.
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Allow to initialize both prescaler (clock divider) and prescaler clock source even if prescaler is disabled.

ARTD-10133	Bug	[can] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1

ID	Subtype	Headline and Description
		Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL) ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml:

ID	Subtype	Headline and Description
		<EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/ AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY" >/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https:// confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-10157	New	New Feature [LIN][LPUART] update driver code according to all old requirements which have updates ,,"NewWorkDescription: There are an proposal changes for requirements on LPUART in Compare_Lpuart_Lin_lp_Reqs_V2.xlsx(check latest version on https://crucible1.sw.nxp.com/cru/R-ARTD-496) file attached. The driver code should be updated according to all old requirements which have updates. All requirements removed and added, they will be implemented in other tickets. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-10160	Bug	[CanIf] EPCtoDS importer fail when "Check ECUC-MODULE-DEF value" is selected ,,"Detailed description (how to reproduce it): similar issue with https://jira.sw.nxp.com/browse/ARTD-10104, but for CANIF component Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-04-26-15-41-31-752.png! Expected behavior: !image-2021-04-26-15-42-23-609.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-10177	Bug	[CAN] CanControllerBaudrateConfig elements is generated in unexpected order<*> Detailed description (how to reproduce it): CAN_TS_189: make generate => Can.epc, CanIf.epc import above .epcs to s32ct, generate code and run test => fail when using setBaudrate API with BaudRateConfigID param the generated order of baudrate array 's elements is unexpected Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_1890 Observed behavior: please perform a comparation between attached output files Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-10178	Bug	[FLS]: When read data, sometime it will cause align error.
		
		,,"Detailed description (how to reproduce it):
		when I read a uint16 type variable, it will cause align problem and system will go to hard fault.
		After debug, I found the code implementation is not appropriate in file: C40_Ip.c, function: C40_Ip_Read_ProcesssData(). In this function, it will judge whether the address is alignment, but before the judgement, there has one sentence to initial the point, it will cause error when the address is not align with 4 bytes. so we need change the code.
		original code:
		uint32 u32ReadLength;
		uint32 u32TmpData = (uint32*)C40_Ip_u32ReadAddressPtr;
		suggest code:
		uint32 u32ReadLength;
		uint32 u32TmpData;
		/ Checking source is align/unaligned /
		u32CheckSourceAddress = ...;
		if (...)
		{
		/ Store data of source address /
		u32TmpData = (uint32*)C40_Ip_u32ReadAddressPtr;
		(uint32*)Fls_u32DestAddressPtr = u32TmpData;
		u32ReadLength = (uint32)FLS_SIZE_4BYTE;
		}
		else / unaligned or remain 4 bytes /
		{
		/ Store data of source address /
		u32TmpData = (uint8*)C40_Ip_u32ReadAddressPtr;
		(uint8*)Fls_u32DestAddressPtr = (uint8)u32TmpData;
		u32ReadLength = (uint32)FLS_SIZE_1BYTE;
		}
		Preconditions:
		NA

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: when We read a uint16 type variable, it will cause align problem and system will go to hard fault. Expected behavior: There are no hard fault when We read a uint16 type variable Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-10219	Bug	 [CAN][EPC2CT importer] fifo filters list should have REQUIRE-INDEX option<*> Detailed description (how to reproduce it): CAN_TS_665 on S32K148 make generate GENERATOR := tresos => Can.epc, CanIf.epc import above .epcs to S32CT run the test => fail After comparing, many differences between two outputs (please take a look at attached files) This might relate to the absence of *REQUIRE-INDEX option on EB !image-2021-04-28-09-16-26-990.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: CAN_TS_665 Observed behavior: testcase can not run after import .epc to S32CT tool Expected behavior: Note:*_ ** I think it is better to add REQUIRE-INDEX option for all node that have type as list. for example: hw_objects, when mapping from EB to CT => the layout (appearance order on CT) is changed. The generated code is quitely identical but the look on CT-GUI is very different Proposed solution optional: [...]
ARTD-10220	New	 New Feature [ADC] Fix and comment static analysis violations (MISRA + HIS + CERT-C) and VSMD reports S32K3XX ,,"Create MISRA, HIS & CERT-C reports VSMD reports Fix all violations for HIS MISRA VSMD reports Get LDRA static analysis report from ITG testing Fix all violations if any are found. Everything needs to be fixed (CCM <= 20, HIS LEVEL <= 6) in the code or commented in Coverity if it cannot be fixed. *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]

ID	Subtype	Headline and Description
		RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-09-02-06-22-02-364.png! Guideline following: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]"
ARTD-10265	New	 New Feature [ADC] Update SetChannel feature ,,"NewWorkDescription: Implement/check SetChannel feature support on K1. Part of changes is checking if input channel is configured at initialization which impacts other platforms (K3 and G2) After implementing/checking the feature, requirements for it must be marked as 'fulfilled in': CPR_RTD_00328.adc CPR_RTD_00329.adc Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-10279	Bug	 [ICU][S32DS] The global driver variable generated with invalid 'static' keyword when configuring precompile mode in high layer<*> when driver in precompile mode and selecting no multicore , the building error appears as the output driver variable contains invalid keyword, the error as the following : !image-2021-05-04-13-33-25-860.png! this is due to the static is invalid as below: !image-2021-05-04-13-34-17-764.png!
ARTD-10287	New	 New Feature [LIN] Flexio_lp should be configured frame size 8 bits for LIN frame ,,"NewWorkDescription: Currently, LIN driver over Flexio_lp is configured frame size 16 bits to transfer LIN frame. So, It can lead to total delay of LIN frame greater than normal as calculated in LIN specification: THeader_Maximum= 1.4 THeader_Nominal TResponse_Maximum= 1.4 TResponse_Nominal To transfer a break length, we can configure with frame size in TIMCMP register according to break length which is configured on EB or CT GUI. After break length was transferred, TIMCMP can be re-configured with frame size 8 bits. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-10298	Bug	

ID	Subtype	Headline and Description
		[WDG] Wrong generated code of some nodes (WdgEnableDirectService, WdgEnableClearResetRequest,..) ,,"Detailed description (how to reproduce it): Step 1: Prepare test with these config: WdgEnableDirectService of Instance 0 = false WdgEnableDirectService of Instance 1 = true Step 2: Generate the test Step 3: Check in generated file #define WDG_DIRECT_SERVICE_INSTANCE0 (STD_OFF) #define WDG_DIRECT_SERVICE_INSTANCE1(STD_ON) #define WDG_DIRECT_SERVICE (STD_ON) This issue is same with ClearResetRequest, WdgVersionInfoApi*. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Wrong generated code with these config, this will make build fail because Wdg_43_Instance0_SetTriggerCondition guarded by WDG_DIRECT_SERVICE_INSTANCE0 define but Wdg_ChannelSetTriggerCondition guarded by WDG_DIRECT_SERVICE Expected behavior: Right generated code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10304	Bug	[CAN] Wrong MaxMbs in case of CanRamBlockSpecified<*> Detailed description (how to reproduce it): can_ts_1055 / s32K148 make generate GENERATOR:=tresos => Can.epc Import Can.epc to S32CT => build, run test fail Please see attached file for comparation between EB and S32CT Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-05-05-16-24-16-199.png! Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10323	Bug	[CAN] [EB/CT compare] many significant differences for CAN_TS_066<*> Detailed description (how to reproduce it): CAN_TS_066 / S32K148

ID	Subtype	Headline and Description
		. make generate GENERATOR:=tresos => CAN.epc, CANif.epc . import aboves epc(s) to S32CT . build run test fail => see attached output files for detail specific ramblock will be generated wrongly for controllers with id > 0 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: !image-2021-05-07-15-07-23-996.png! Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10326	Bug	[FLS] In CT, Fls module under MCAL component, when the sector number more than 10, it will report error ,,"Detailed description (how to reproduce it): In CT, Fls module under MCAL component, when the sector number more than 10, it will report error. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: For example: I created Fls_sector0 Fls_sector9, and the fls physical sector is mapped from FLS_DATA_ARRAY_0_BLOCK_4_S0000 FLS_DATA_ARRAY_0_BLOCK_4_S0009. It works normal. Then I add one more sector named Fls_sector10. it will report error. and the physical sector mapped to FLS_DATA_ARRAY_0_BLOCK_4_S0010. I try to change the physical sector to FLS_DATA_ARRAY_0_BLOCK_4_S0011, then the error disappear, and i change back to FLS_DATA_ARRAY_0_BLOCK_4_S0010, it works ok. it's strange. Expected behavior: add more than 10 sectors according to the chip's real data flash size. example, if the chip data flash size is 128K, and each sector size is 8K, we should be add 16 sectors. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-10329	Bug	[ADC] Missing S32CT ADC configuration in IPL when only configuring ADC1 and incorrect DmaMuxSource in HLD<*>
		
		Detailed description (how to reproduce it):
		Issue 1: In ADC IPL with CT component, when configuring only ADC1 in UI
		There is no configuration for ADC1 is generated
		Issue 2: in ADC HLD with CT component, when ADC Dma counting node has no element, au8Adc_TransferringDmaMuxSource should be 0U as below
		#if (STD_ON == ADC_OPTIMIZE_DMA_STREAMING_GROUPS)
		.au8Adc_TransferringDmaMuxSource = \{ 0U, DMA_IP_REQ_MUX0_SARADC0 },

ID	Subtype	Headline and Description
		#endif / (ADC_OPTIMIZE_DMA_STREAMING_GROUPS == STD_ON) / Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Missing ADC1 configuration Expected behavior: all configuration must be generated if configured Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10355	Bug	 [PWM] Fix HIS_PARAM and OVERRUN violation<*> Detailed description (how to reproduce it): HIS_PARAM|Measured value of PARAM metric 6.00 is higher than maximum value 5.00 allowed by the HIS metrics policy.|/ARTD-CIPWM-96/sources/S32CC_4.4/output/eclipse/plugins/Pwm_TS_T40D11M20I0R0/src/Pwm.c|Pwm_ValidateParamsPeriodDuty Misra report has the overrun violation as attached picture: Overrunning array "Ftm_Pwm_Ip_NotifIrq[instance]" of 12 bytes at byte offset 12 using index "channel 1U" (which evaluates to 6). Overrunning callee's array of size 6 by passing argument "channel 1U" (which evaluates to 6) in call to "Ftm_Pwm_Ip_UpdateChnInt". Overrunning callee's array of size 6 by passing argument "channel 1U" (which evaluates to 6) in call to "Ftm_Pwm_Ip_DisableCmpIrq". Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: HIS_PARAM violation Expected behavior: Has no HIS_PARAM violation Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix HIS_PARAM violation
ARTD-10371	Bug	 [I2c] I2c driver should support to transfer with buffer size up to uint16<*> For HLD, the u8BufferSize field from I2c_RequestType structure should be changed to type uint16.
ARTD-10373	Bug	 [CRYPTO] Add Multiplicity related information to optional node HseKeyHandle in custom C01 xdm file<*> Add Multiplicity related information to optional node HseKeyHandle in custom C01 xdm file. Please update the following lines of the HseKeyHandle attribute: From: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS">

ID	Subtype	Headline and Description
		<icc:v vclass="PreCompile">VariantPreCompile</icc:v> </a:a> To: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS"> <icc:v mclass="PreCompile">VariantPreCompile</icc:v> <icc:v vclass="PreCompile">VariantPreCompile</icc:v> </a:a>
ARTD-10386	New	 New Feature [ETH]Some functions have HIS_PARAM > 5 ,,"NewWorkDescription: Some functions have HIS_PARAM > 5: Gmac_Ip_MDIOReadMMD Gmac_Ip_MDIOWriteMMD GMAC_WriteManagementFrame Eth_Transmit Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-10441	Bug	 [S32K3] PlatformSDK - missing include dir "board" for GHS ,,"S32K3 RTD SDK does not add the ""board"" dir in the S32DS include paths for the GHS compiler. The compilation then fails on missing header file Clock_Ip_Cfg.h. If I manually add the ""board"" dir in the include paths, the build succeeds (see attached screenshot).
ARTD-10403	New	 New Feature [LIN] Update driver following PascalCase coding rule ,,"NewWorkDescription: remove pre fix in all variable following PascalCase except global variables Requirement source: PascalCase coding rule (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update driver"
ARTD-10404	New	 New Feature [LIN]Improve send/detect the wake up pulse ,,"NewWorkDescription: 1. For both LPUART_Lin_Ip and FLEXIO_Lin_Ip: For send wakeup pulse, we will no need to use timer to measure length of pulse. We just send 0xF0 or 0xF8, 0xFC, 0xFE, 0xFF(consider that 1 Start bit 0 is included in wakeup pulse). This way will allow us to generate a wake up pulse in 250us->5ms(we should generate maximum length if possible) To detect wakeup pulse longer 150us(we should detect minimum length if possible), we also check data received 0xFC or 0xFE or 0xFF(consider that 1 Start bit 0 is included

ID	Subtype	Headline and Description
		in wakeup pulse). Frame error may be occurred and can be ignored if wakeup pulse received greater than the time of a frame. The LIN Baudrate from 1kbps->20kbps. So, the pulse always ensure in that range. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Calculate number of bit in wakeup signal byte to send/receive depend on baudrate"
ARTD-10406	New	 New Feature [LIN] Improve the way send or detect break field ,,"NewWorkDescription: 1. For FLEXIO_Lin_Ip only: For sending a break field, We will set frame size equal break length 13bits then framesize=12, Start bit 12bits data Stop bit(1bit break delimiter), so data=0x000. For detection break field in Slave mode. We will set frame size equal break length which is configured in ChannelList. To ensure the driver received correct break field, driver needs to compare with 0x00. And of course, break frame aways generate frame error when external master send break length greater than normal 11 bits of break detection. Frame size can be set via TIMCMPn register 2. For LPUART_Lin_Ip: the LPUART hardware already has mechanism to send or detect break field, so no need to improve. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-10456	Bug	 [ICU] The eMIOS_ICU cannot run into overflow callback function.<*> Detailed description (how to reproduce it): Create a project in which set an eMIOS channel to work in ICU signal measurement mode. You may select either global time base or channel internal counter for ICU channel. In both cases, overflow callback function cannot be accessed. In Emios_Icu_Ip_IrqHandler(), the variable bOverflow is set to FALSE and no any check in subsequent process and leads to unreachable overflow callback function. When using internal counter as ICU time base, the overflow callback function will be unconfigurable, like follow: !image-2021-05-13-11-01-35-146.png! Preconditions: S32DS 3.4 RTD 0.9.0 Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The eMIOS_ICU cannot run into overflow callback function whenever overflow happen or not. Expected behavior: Overflow callback function should be accessible in ICU_MODE_SIGNAL_MEASUREMENT mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10465	Bug	

ID	Subtype	Headline and Description
		[GPT][S32DS] Stm_Ip_u32NextTargetValue undefined when config GPT change next timeout<*> When config GPT HLD on s32ct, enable GPT change next time out without enable ISR i got the build fail: !image-2020-12-18-15-09-38-225.png! [^Gpt.mex]
ARTD-10468	New	 New Feature [CRC] Add support for CRC64 ,,"Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: CRC driver code and configuration files do not support CRC64 mode Expected behavior: CRC driver code and configuration files must support CRC64 mode Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A"
ARTD-10482	Bug	 [ICU] Not able to configure eMIOS IPM mode for IcuUserModeForDutycycle parameter<*> Detailed description (how to reproduce it): For our application it is needed to use eMIOS IPM mode for ICU channel. We have seen in code that IPM low level function is available as follows: static inline void Emios_Icu_Ip_SignalMeasurementWithIPMMode (const uint8 u8ModuleIdx, const uint8 u8ChannelIdx, boolean bOverflow) { But in configuration of IcuUserModeForDutycycle parameter the IPM mode is missing. Preconditions: Using eMIOS channel IPM mode. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not possible to configure eMIOS IPM mode for ICU channel Expected behavior: It is possible to configure eMIOS IPM mode for ICU channel Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add IPM mode into configuration of IcuUserModeForDutycycle parameter.
ARTD-10483	Bug	 [PWM] eMIOS FEN bit always cleared while changing duty cycle for channels with DMA<*>

ID	Subtype	Headline and Description

		Detailed description (how to reproduce it):
		We configure PWM channel which triggers DMA request (Flag Event response as EMIOS_PWM_DMA_REQUEST). After changing duty cycle we see that FEN bit is always cleared so no DMA request is generated.
		In "Emios_Pwm_Ip_SetDutyCycleOpwfmb" there is called "Emios_Pwm_Ip_SetInterruptRequest" before update of Reg A. The function Emios_Pwm_Ip_SetInterruptRequest checks if Emios_Pwm_Ip_aCheckEnableNotif[instance][channel] is set (in our case [0][9]) is "1", otherwise FEN is cleared:
		else
		{
		Emios_Pwm_Ip_aNotif[instance][channel] = (uint8)0U;
		Emios_Pwm_Ip_SetInterruptRequest(base, channel, (Emios_Pwm_Ip_aCheckEnableNotif[instance][channel] == 0U)? FALSE : TRUE);
		}
		The issue is that Emios_Pwm_Ip_aCheckEnableNotif[instance] [channel] is set to 1 only if function Emios_Pwm_Ip_SetFlagRequest (INSTANCE_0, 9, EMIOS_PWM_INTERRUPT_REQUEST) is called with parameter EMIOS_PWM_INTERRUPT_REQUEST. If it is called with EMIOS_PWM_DMA_REQUEST it will not be set and as such the FEN will then be cleared always while duty cycle is changed.
		Is there any way how to keep FEN enabled while changing duty cycle if the channel require DMA request (EMIOS_PWM_DMA_REQUEST)?
		Preconditions:
		Using eMIOS channel to generate DMA request (EMIOS_PWM_DMA_REQUEST).
		Test Case ID (internal TC that caught the defect) optional:
		N/A
		Observed behavior:
		FEN flag is always cleared while changing duty (no DMA request).
		Expected behavior:
		FEN flag is not cleared while changing duty cycle (so DMA request is generated).
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Do not clear FEN bit so that DMA request is generated.

ARTD-10497	Bug	[SPI] FLEXIO does not work with AsyncTransmit when configure number instance of FLEXIO same to LPSPI<*> Detailed description (how to reproduce it): FLEXIO does not work with AsyncTransmit when configure number instance of FLEXIO same to LPSPI. As picture below, when I want to use FLEXIO_0, LPSPI configured must differ to instance 0. Note: This isssue can be occured on all of derivatives (K116, K118, K142, K144, K144W, K146, K148) !image-2021-05-17-09-24-31-276.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: [...]
ARTD-10556	New	 New Feature [LIN] Driver will generate a error if clock source too fast to refer ,,"NewWorkDescription: If clock source of any lin channel is too fast to refer, a error should be proposed to notify to user Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add a checking clock source"
ARTD-10574	Bug	 [mcu] Mcu_DistributePllClock function always returns E_NOT_OK when McuDevErrorDetect node is disabled<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mcu_TC_FCT_0091 Observed behavior: Mcu_DistributePllClock function always returns E_NOT_OK when McuDevErrorDetect node is disabled Expected behavior: Need to update driver to return E_OK when McuDevErrorDetect node is disabled Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-10713	Bug	 [SPI] Many variables are having wrong naming.<*> Detailed description (how to reproduce it): Many variables are having wrong naming. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: None error Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-10733	Bug	 [PWM] Critical AUTOSAR configuration parameter disabled and not usable<*> Detailed description (how to reproduce it): PWM configuration is not AUTOSAR compliant.

ID	Subtype	Headline and Description
		Reference PwmMcuClockReferencePoint parameter is no longer used (being disabled in Pwm.xdm). This parameter is critical to determine PWM frequency based on the clock source in MCU. At application level this parameter is mandatory since without it correctly determining the frequency becomes problematic. This is not a catastrophic issue but is a serious issue, nevertheless... Preconditions: [none] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [see description] Expected behavior: [see description] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Enable reference to MCU clock parameter, use this parameter and divider from IP configuration to determine the number of tick. Autocalculate option should be enabled in XDM.
ARTD-10736	Bug	 [OCU][PWM][ICU][GPT] Timer drivers should have reference to MCL and MCU common configurations<*> _*Detailed description (how to reproduce it): When drivers use common resources from other drivers, these resources should be accessed via references to those drivers. For instance in case OCU, PWM and ICU when configured to use eMIOS IP, they might use a common bus configured in MCL. The configuration of each drivers should reference the bus configuration to access certain parameters that may be needed in their internal logic (number of configured counter ticks, dividers etc). Using a reference might also insure that invalid configuration of the bus are not exported to driver. Internal references which are NOT configured by the user SHOULD not be used since they might mask problems. PWM, OCU and GPT drivers should always use references to MCU driver even in cases where AUTOSAR does not require it since a reference to MCU clock will make much easier to determine the frequency of the given channel... For ICU this is not needed since in all cases the result of the ICU measurement is in ticks. Preconditions: [none] Test Case ID (internal TC that caught the defect) optional: [none] Observed behavior: [see description] Expected behavior: [see description] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-10779	New	 New Feature [GPT] Add clarification in manuals if driver have conditional reentrant APIs ,,"There are APIs like ""Lptmr_Icu_Ip_EnableInterrupt with Reentrancy: Cond-Reentrant""

ID	Subtype	Headline and Description
		We need to add in manual clarification that this is related to EAs implementation to be used. The APIs are re-entrant as long as EAs are correctly implemented quarding the shared resource accessed in RMW operation."
ARTD-10783	Bug	 [gpt] Errors and missing exclusive areas in Bswmd.arxml<*> Detailed description (how to reproduce it): Exclusive areas not available in <Module>_Bswmd.arxml Incorrectly formatted <Module>_Bswmd.arxml Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A. Observed behavior: Missing exclusive areas in Davinci after integrating RTD !image-2021-04-12-19-29-09-321.png|thumbnail! Expected behavior: All exclusive areas are included in <Module>_Bswmd.arxml <Module>_Bswmd.arxml is valid Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution Fix the following issues and perform all the verification steps*: Issue #1 Some exclusive areas are missing because "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files are not using the pattern expected by bswmd_creator script: "is used in function" Solution #1 From https://jira.sw.nxp.com/browse/AMPT-5710, bswmd_creator is parsing files "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" and it's looking up for the "is used in function" pattern. Therefore, "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" files shall use the following pattern for describing each exclusive area: <MODULE>_EXCLUSIVE_AREA_09 is used in function <Module>_StartChannel ... Issue #2 Missing exclusive areas mapped to IPL functions 2.1 Exclusive areas not referenced by any function in Adc_Bswmd.arxml, missing: <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA"> E.g.:{code:java} ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration 2.2 Exclusive areas missing completely from Adc_Bswmd.arxml E.g.:{code:java} ADC_EXCLUSIVE_AREA_73 is used in function Ctu_Ip_SetFifoThreshold Solution #2 The integration manual shall map exclusive areas to public HLD functions (*no internal functions should be mentioned*). This is done by adding in "exclusive_areas_to_be_defined_in_bsw_scheduler.dox" all the public HLD functions that are using an exclusive area via calls to IPL functions. For example: ADC_EXCLUSIVE_AREA_12 is used in function Adc_Calibrate to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_Init to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. ADC_EXCLUSIVE_AREA_13 is used in function Adc_SelfTest to protect the ADC_MCR register from read/modify/write operation in Adc_Sar_Ip_Powerup. [...] Exclusive Areas implemented in Low level driver layer (IPL)

ID	Subtype	Headline and Description
		ADC_EXCLUSIVE_AREA_12 is used in function Adc_Sar_Ip_DoCalibration to protect the updates for: ADC_MCR register ADC_EXCLUSIVE_AREA_13 is used in function Adc_Sar_Ip_Powerup to protect the updates for: ADC_MCR register This adds in "Adc_Bswmd.arxml" the ADC Exclusive Area 12 for Adc_Calibrate and ADC Exclusive Area 13 for Adc_Init and Adc_SelfTest. It also keeps the note in Integration Manual about the EAs being used by IPL API functions Adc_Sar_Ip_Powerup and Adc_Sar_Ip_DoCalibration. Issue #3 Using uppercase hexadecimals for non-autosar API service IDs. Solution #3 Non-autosar API service IDs shall be converted to lowercase in "*generic/doc/NonASR_ServiceID.xml*" to be compliant with AUTOSAR schema file (otherwise, the file is not valid and cannot be loaded). For example: <SERVICE-ID>0x2C</SERVICE-ID> must be changed to <SERVICE-ID>0x2c</SERVICE-ID> Verification #1 After fixing, please generate plugin with GENERATE_BSWMD_FILE=ON (more details in https://nxp1.sharepoint.com/:p:/s/Zebra/Ecuug60PLRlFv7JI1xLByAABrR3E2qa0txuqVbp4II2-IQ?e=GeSbhP) there must not be any errors generated by the script. Verification #2 Make sure exclusive areas are available in generate_swcd\swcd\<Driver>_Bswmd.arxml: <EXCLUSIVE-AREA> <SHORT-NAME>ADC_EXCLUSIVE_AREA_13</SHORT-NAME> </EXCLUSIVE-AREA> and referred by functions <BSW-CALLED-ENTITY> <SHORT-NAME>Adc_Init</SHORT-NAME> <CAN-ENTER-EXCLUSIVE-AREA-REFS> <CAN-ENTER-EXCLUSIVE-AREA-REF DEST="EXCLUSIVE-AREA">/AUTOSAR_Adc/BswModuleDescriptions/Adc/InternalBehavior_0/ADC_EXCLUSIVE_AREA_13</CAN-ENTER-EXCLUSIVE-AREA-REF> </CAN-ENTER-EXCLUSIVE-AREA-REFS> <MINIMUM-START-INTERVAL>0.0</MINIMUM-START-INTERVAL> <IMPLEMENTED-ENTRY-REF DEST="BSW-MODULE-ENTRY">/AUTOSAR_Adc/BswModuleEntrys/Adc_Init</IMPLEMENTED-ENTRY-REF> </BSW-CALLED-ENTITY> Verification #3 Validate the <Driver>_Bswmd.arxml file following steps from: https://confluence.sw.nxp.com/display/AUTORD/BSWMD Verification #4 Regenerate IM if task for updating documentation has been already resolved.
ARTD-10899	New	New Feature [RM][S32K3][S32G] Analyze reentrancy of all apis and add support exclusive area for RM ,," Scan all IP: XRDC, MPU_M7, SEMA42, VIRT, AXBS, XBIC, PFLASH Analyze and update reentrancy NonASR_ServiceID.xml Xrdc_Ip_SetProcessID_Privileged is probably re-entrant function and need EA added. Look like MPU require interrupt disable to update regions need to analyze to add isr disable or add exernal assumption for customer"

ID	Subtype	Headline and Description
ARTD-10911	Bug	[S32K3 RTM] OCU: Clock source and prescaler configuration do not match eMIOS ones<*> Detailed description (how to reproduce it): OCU eMIOS channel configuration has two parameters to describe clock sources: OcuClockSource (enum with the following labels OCU_SYSTEM_CLOCK, OCU_EXTERNAL_CLOCK, OCU_FIXED_FREQ_CLOCK) OcuEmiosBusSelect (enum with labels corresponding to buses: A, B/C/D, F or internal)Only the second parameter is usable but both parameters can be enabled and configured which is confusing. The bigger issues comes from the configuration of the prescaler which only allows DIV_1 to DIV_4 which limits the frequency ranges. The maximum divider should be DIV_16. I can assume that this is a porting issues since the used parameters exist on FTM IPs. Preconditions: none Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Invalid frequency output. Expected behavior: see above Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Use only one clock/bus parameter (OcuClockSource) and update divider enum labels.

ARTD-10925	Bug	[GPT] S32K3 PIT RTI generated code issue<*>
		
		Detailed description (how to reproduce it):
		Add PIT component and add both PIT timer channel and PIT RTI channel into the configuration.
		When code is generated for "Pit_Ip_Cfg_Defines.h":
		#define PIT_IP_RTI_USED (STD_ON)
		#define PIT_IP_REPORT_ERROR_STATUS (STD_OFF)
		In the generated code Pit_Ip_xxx_PBcfg.c, we can see that:
		Pit_Ip_ChannelConfigType PIT_0_ChannelConfig_PB[4U] =
		{
		/**@brief PitChannel_0 /
		{
		/ brief PIT Channel Id /
		0U,
		#if ((defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON)) && (PIT_IP_REPORT_ERROR_STATUS == STD_ON)_*)
		/**< brief errorReportCallBack /
		NULL_PTR,
		#endif
		/ brief PIT Enable Interrupt /
		(boolean)(TRUE),
		/ brief PIT callback name /
		&Pit0_Ch0_Callback,
		/ brief PIT callbackparam /
		(uint8)0U
		}
		.....

ID	Subtype	Headline and Description
		In above code, there is the macro "*_PIT_IP_REPORT_ERROR_STATUS " used in the structure. But in "Pit_Ip_Type.h", this macro is not used: typedef struct { uint8 hwChannel; /**< brief Timer channel number / #if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON)) errorReportCallBackType errorReportCallBack; /**< brief errorReportCallBack / #endif boolean enableInterrupt; /**< brief Enable interrupt generation / Pit_Ip_CallbackType callback; /**< brief callback / uint8 callbackParam; /**< brief callbackParam / } Pit_Ip_ChannelConfigType; So there will be compiling error. Proposed solution optional: I think the macro "*_PIT_IP_REPORT_ERROR_STATUS " should not be used in the generated code "Pit_Ip_xxx_PBcfg.c.
ARTD-10923	Bug	[SAI] Tx and Rx can not work in the same time like duplex mode.<*> Detailed description (how to reproduce it): [When implement a new SAI Async transfer after starting a SAI Async receive with the same instance, test the Tx status, the issue happens, vice versa.] Preconditions: [RTD version 0.9.0, S32DS 3.4(GCC 9.2), SAI(master) communicate with codec sgtl5000(slave) in I2S protocol, both Tx and Rx used the same SAI instance, Rx work in Async mode, Tx work in Sync with other.] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [capture the Tx data line ,find nothing, Frame Sync has no signal, debug and find that the TE bit is not enabled at all, vice versa.] Expected behavior: [Tx and Rx can work well independent while another one is working, like duplex mode.] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [Remove the Rx status checking when prepare to implement Tx, vice versa.]
ARTD-10962	Bug	[ADC] Adc_ReadRawData read data from control channel index (SC index) instead of physical channel id<*> Detailed description (how to reproduce it): Adc_ReadRawData read data from control channel index (SC index) instead of physical channel id Preconditions: Adc_ReadRawData is enable Adc 0 group with channel SE6_ADCH6, SE14_ADCH14 Test Case ID (internal TC that caught the defect) optional: Adc_TC_1801 Adc_TS_021 Observed behavior: Start group of adc 0 Wait until complete flag of SC1 channel set Adc_ReadRawData with channel array {6, 14} Real status: wrong data in buffer read group {0 , 0}

ID	Subtype	Headline and Description
		Complete flag check failed because input parameter is physical channel Expected behavior: Read group buffer matching with {0xE35, 0xE7C} Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-10967	New	 New Feature [SAI] SAI IP generate defines with instance number ,,"NewWorkDescription: SAI IP generate defines with instance number Update IPL example to replace defines from main.c: #define INST_SAI0 0U #define INST_SAI1 1U Requirement source: Usability improvement Proposed solution optional: name proposal (caps of configuration name)_(functional group name)_INSTANCE !image-2021-05-25-15-50-56-879.png|thumbnail! [...]"
ARTD-10970	Bug	 [FLS] Initialization sequence needs to comply with HW timing restrictions.<*> Per attached discussions with design, the AHB domain / Serial Flash domain reset must meet certain timing restrictions. Also after this reset the DLL chain must be reconfigured.
ARTD-10996	Bug	 [PORT] Pad keep enable (PKE) bit can't be set when PortPin Pull Keeper option is selected<*> Detailed description (how to reproduce it): Pad keep enable bit is not set when PortPin Pull Keeper option is selected, and the generation code is _.pullKeep = PORT_PULL_KEEP_DISABLED, Preconditions: Select _PortPin Pull Keeper in PORT configuration Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Pad keep enable bit is not set when PortPin Pull Keeper option is selected Expected behavior: Pad keep enable bit should be set when PortPin Pull Keeper option is selected Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CE's comment: in _generate_PB/Siul2_Port_Ip_PBcfg.c_, the Pull keep option is fixed, without any condition check from EB tresos parameter: [!VAR "pullKeep_IP" = "'PORT_PULL_KEEP_DISABLED'"!][!// There should have a condition to check whether _PortPin Pull Keeper_ is selected.
ARTD-11010	New	 New Feature

ID	Subtype	Headline and Description
		[S32K3XX][PORT] (ITG) Create test case to check PKE/DFE/IFE bit in MSCR register ,,"Detailed description (how to reproduce it):* in MSCR register, which was have many bits, but the test case did not cover the operation of all bit, it is missing test to check PKE, DSE, IFE bit Test Case ID (internal TC that caught the defect) optional:* NA Observed behavior: !image-2021-05-27-14-48-41-848.png! Expected behavior: update/ create test case to check the operation of this bit, it need to be work correctly Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA"
ARTD-11038	Bug	[FLS] Update code and data sections for S32K312 derivatives<*> Detailed description (how to reproduce it): Issues might appear because of different block arrangement of S32K314 derivatives. Please analyze the attached email related to this issue. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: No issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-11037	Bug	[CRYPTO] Memory placement not respected by GCC with -O0<*> Detailed description (how to reproduce it): This seems to be a GCC toolchain issue impacting RTD drivers. When the optimization is set to O0, the #pragma GCC section directives from the MemMap files have no effect when applied to uninitialized variables defined with the "static" storage class and instead the variable is linked to the default section (bss). One consequence in Crypto driver with S32K344 is that when using the default linker file and MPU settings from the RTD package, the variable Crypto_aHseSrvDescriptor is linked to cacheable memory and the Crypto_Exts_FormatKeyCatalogs function fails with error code CRYPTO_RET_INVALID_PARAM if the data cache is enabled (D_CACHE_ENABLE macro defined in preprocessor settings). Issue noticed with Crypto, but could affect other modules. Observed behavior: #pragma GCC section directive not effective for "static" uninitialized variables when optimization = O0 Expected behavior: Variable section applied according to the pragma directive
ARTD-11048	Bug	[ICU] Cannot configure mode for ICU channel when IPV name does not contain IPV name<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): This clone is for tracking the CI build for linked issue. Driver changes are in place but need build to pass incorporating the latest changes for examples in plugin generation. Please see details also on cloned ticket.
ARTD-11072	New	 New Feature [ADC] Add overwrite enable to high level configurator ,,"NewWorkDescription: Add overwrite enable to high level configurator !image-2021-05-28-19-29-32-180.png|thumbnail! Currently can be configured by LowLevel configurator MCAL did not support this in the past Requirement source: N.A. Proposed solution optional: [...]"
ARTD-11073	Bug	 [SAI] Driver does not support disabling clock after transmission (BCE)<*> Detailed description (how to reproduce it): the bit clock continues to be generated even after transmission has been complete this has impact on power consumption. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Proposed solution optional: Possible solution would be to clear BCE from last interrupt (need to decide how to implement when using DMA) Add support for BCE disable clock after transmission To decide if parameter is per instance or transmission
ARTD-11075	Bug	 [MCU] IPs functions should not be visible at HLD layers<*> Detailed description (how to reproduce it): According requirement: CPR_RTD_00227.mcu*: The BSW modules header file <module name>.h shall only export these interfaces which are absolutely required by upper layers. Rationale: E.g. internal interfaces shall not be visible at upper layers. => IPs functions should not be visible at HLD layers But in mcu driver including follow: Mcu.h > Mcu_IPW_Types.h > Clock_Ip.h Mcu.h > Mcu_IPW_Types.h > Power_Ip.h Mcu.h > Mcu_IPW_Types.h > Ram_Ip.h Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: IPs functions visible at HLD layers Expected behavior: IPs functions should not be visible at HLD layers

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change the include <Ip>_Ip.h into <module>_IPW.c

ARTD-11130	Bug	
		[MCL][LCU] All SetSync function need to avoid hardfault when users only use only one instance (Precondition:enable only clock for this instance)<*>
		
		Detailed description (how to reproduce it):
		Initialize Mcu and enable clock for only one instance
		initialize only one instance
		Call all set_sync functions
		Observed behavior:
		Go to Hardfault when go over the command to set value for the remaining instance
		Expected behavior:
		All set sync functions can work correctly without any errors.
		Proposed solution optional:
		My first proposal is to have a runtime check for each instance:
		if(0U != MaskValue[LCU_IP_HW_INST_0])
		{
		}
		if(0U != MaskValue[LCU_IP_HW_INST_1])
		{
		}
		
		My second proposal is to have a precompile #define that is generated based on the configuration:
		if nothing is configured for an instance, then that instance shall not be used during runtime.
		#if (LCU_INSTANCE_COUNT >= 1U)
		#if (LCU_INSTANCE0_IS_CONFIGURED == STD_ON)
		RegValue = g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_0]->OUTEN;
		RegValue &= MaskValue[LCU_IP_HW_INST_0];
		RegValue = DataValue[LCU_IP_HW_INST_0];
		g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_0]->OUTEN = RegValue;
		#endif
		#endif
		#if (LCU_INSTANCE_COUNT >= 2U)
		#if (LCU_INSTANCE1_IS_CONFIGURED == STD_ON)
		RegValue = g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_1]->OUTEN;
		RegValue &= MaskValue[LCU_IP_HW_INST_1];
		RegValue = DataValue[LCU_IP_HW_INST_1];
		g_ptLcuBaseInstPtrArray[LCU_IP_HW_INST_1]->OUTEN = RegValue;
		#endif
		#endif

ARTD-11141	Bug	 [UART] Not possible to configure 460800 for DesireBaudrate parameter<*> Detailed description (how to reproduce it): Baudrate 460800 is missing in configuration of DesireBaudrate parameter, see here the possible values in Uart.xdm where 460800 is missing: <v:var name="DesireBaudrate" type="ENUMERATION"> .... <a:da name="RANGE"> <a:v>LPUART_UART_BAUDRATE_1200</a:v>

ID	Subtype	Headline and Description
		<a:v>LPUART_UART_BAUDRATE_2400</a:v> <a:v>LPUART_UART_BAUDRATE_4800</a:v> <a:v>LPUART_UART_BAUDRATE_7200</a:v> <a:v>LPUART_UART_BAUDRATE_9600</a:v> <a:v>LPUART_UART_BAUDRATE_14400</a:v> <a:v>LPUART_UART_BAUDRATE_19200</a:v> <a:v>LPUART_UART_BAUDRATE_28800</a:v> <a:v>LPUART_UART_BAUDRATE_38400</a:v> <a:v>LPUART_UART_BAUDRATE_57600</a:v> <a:v>LPUART_UART_BAUDRATE_115200</a:v> <a:v>LPUART_UART_BAUDRATE_230400</a:v> Missing baudrate 460800 here <a:v>LPUART_UART_BAUDRATE_921600</a:v> <a:v>LPUART_UART_BAUDRATE_1843200</a:v> </a:da> </v:var> Preconditions: Application requires to use baudrate 460800. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not possible to configure baudrate 460800. Expected behavior: Allow to configure baudrate 460800. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add baudrate 460800 for DesireBaudrate parameter.
ARTD-11168	Bug	[FLS]Header files found in src folder<*> For the components mentioned in the issue title, there are some header files misplaced under src folder and not under include folder. In Model-Based Design Toolbox for MATLAB and Simulink, we generate the projects automatically and need to copy all the dependencies. We explect to find only header files in the include and src files in src folder. This pattern is satisfied for all other modules but not for the mentioned ones. Also, the RTD veresion is 0.9.0 released on 26th of March, but in Jira I was not able to find this version marked as "Released". !image-2021-04-19-11-50-22-549.png!!image-2021-04-19-11-53-11-912.png! !image-2021-04-19-11-57-04-010.png! !image-2021-04-19-11-58-12-914.png!
ARTD-11169	Bug	[SAI]Header files found in src folder<*> For the components mentioned in the issue title, there are some header files misplaced under src folder and not under include folder. In Model-Based Design Toolbox for MATLAB and Simulink, we generate the projects automatically and need to copy all the dependencies. We explect to find only header files in the include and src files in src folder. This pattern is satisfied for all other modules but not for the mentioned ones. Also, the RTD veresion is 0.9.0 released on 26th of March, but in Jira I was not able to find this version marked as "Released". !image-2021-04-19-11-50-22-549.png!!image-2021-04-19-11-53-11-912.png! !image-2021-04-19-11-57-04-010.png! !image-2021-04-19-11-58-12-914.png!

ID	Subtype	Headline and Description
ARTD-11182	New	New Feature [SAI] S32ConfiguratorTool and Tresos remove .members from structs (for C90 compliance), keep generated files bit-exact with Tresos" ,,"Tresos and S32CT file generation remove .members from structs (for C90 compliance) Validate dev_tests after changes Validate that IPL example is still compiling after changes.
ARTD-11221	Bug	[ecum] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-11223	Bug	[base] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		N/A
ARTD-11224	Bug	[can] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-11227	Bug	[pwm] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see: The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-11229	Bug	[platform] Compiler warning with several module.<*> Detailed description (how to reproduce it): Please see:

ID	Subtype	Headline and Description
		The [link|https://community.nxp.com/t5/S32K3-Internal-Community/S32K3-RTD-MCAL-Removing-Compiler-warnings-and-MISRA-compliance/td-p/1251888] for detail information. I also try to compile one of our example(eclipse\plugins \Lin_TS_T40D34M9I0R0\examples\EBT\Lin_Example_EBT_Lpuart) in the package SW32K3_RTD_4.4_0.9.0 and it also have many compiler warning. Please see attached file for more information. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Our driver still have compiler warning. Expected behavior: Fix all compiler warning in our RTD driver. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-11204	New	 New Feature [I2C] Lpi2c should receive more than 256 bytes per transfer ,,Lpi2c receive function is limited to receive 256 bytes per transfer. The number of bytes that could be received in one transfer should be increased.
ARTD-11205	Bug	 cannot support MII mode configuration in S32_CT<*> Detailed description (how to reproduce it): [.The TXD2 & TXD3 and RXD2 & RXD3 signals required by EMAC MII mode cannot be allocated in S32_CT, as they have only one signal name for TXD2&TXD3(txd), and RXD2&RXD3(rxd)]!image-2021-06-03-15-21-05-193.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [The TXD2 & TXD3 and RXD2 & RXD3 signals required by EMAC MII mode can be allocated in S32_CT successfully as RM descripted] !image-2021-06-03-15-24-24-948.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-11248	Bug	 [LIN] Update autobaud rate feature for K3<*> Detailed description (how to reproduce it): Need update driver to can start input capture from FTM time and stop it when get timer between a rising and falling edge on the sync byte is done.
ARTD-11374	Bug	 [SPI] Jump to hardfault in Spi_JobTransferFinished is called twice<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): If Job result is failed but the Spi_Cancel is called in case don't know the job result. An hard fault will available because AsyncCrtSequenceState is assigned to null (The Spi_JobTransferFinished is called twice in both interrupt and Spi_Cancel) Preconditions: First Sequence is pending, after that call Spi_Cancel. But in this time, the tranferring job is failed. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-11382	Bug	[PWM] Remove ASR specific validation from NonAsr component<*> Detailed description (how to reproduce it): build the plugins and s32ct component for PWM Create a new example for K3XX and add Emios_pwm_ip compoenent to the project A lot of errors are thrown in the error log because validation of some nodes require the HLD nodes to be present. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Errors are thrown in the error log of S32DS from invalid validation constraints. !image-2021-06-08-16-39-47-179.png|thumbnail! After a look in the template file it seems that this impacts all IPs of PWM driver. Expected behavior: No errors are present for any of the IPL components. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Guard in the template file the validations that are using nodes from ASR mode. This should be done for all available IPs.
ARTD-11406	Bug	[FEE] Fix compiler warnings<*> Detailed description (how to reproduce it): See the attached file for more details Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: iar warnings Expected behavior: no warnings Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-11448	New	 New Feature [SAI] Add the check for shared pins between Transmitter and Receiver ,,Add the check at configuration time that TX and RX do not use same lines simultaneously if full duplex mode is set
ARTD-11528	New	 New Feature [FEE] If these conditions are not satisfied. The Fee_Init() return FEE_E_INIT_FAILED ,,"NewWorkDescription: CPR_RTD_00563.fee:If the parameter checking for the driver's initialization function is enabled, the Configuration pointer argument shall be checked with the following conditions: In the supportedConfigVariants VariantPreCompile and VariantLinkTime if only one configuration variant set is used, the initialization function does not need nor evaluate the passed argument. Thus the Configuration pointer shall have a NULL_PTR value. In the supportedConfigVariant VariantPostBuild or if multiple configuration variant sets are used, the initialization function requires the passed argument. Thus the Configuration pointer shall be different from NULL_PTR. If these conditions are not satisfied, a Development error with type <MIP>_E_INIT_FAILED shall be reported to Development Error Tracer (Det) Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-11644	New	 New Feature [I2C] CPR_RTD_00190 regarding disabling Dem_SetEventStatus should be implemented ,,"CPR_RTD_00190.i2c should be implemented. All modules which need to call Dem module shall provide a configuration parameter for disabling all calls of Dem_SetEventStatus. If this parameter is activated, no call of Dem_SetEventStatus must be performed. Per default, the call of Dem_SetEventStatus shall be allowed."
ARTD-11663	Bug	 [WDG] Some functions missing in UM chapter 6.2<*> Detailed description (how to reproduce it): Some functions missing in UM chapter 6.2 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		[...]
ARTD-11664	Bug	[I2C] Channel ID and channel index are not match on CT configuration<*> Detailed description (how to reproduce it): Channel ID and channel index are not match on CT configuration, it cause some problem if user config like that Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add a constraint to check match between channel id and channel index
ARTD-11700	Bug	[PWM] Mismatch the macro definition<*> Detailed description (how to reproduce it): Mismatch the macro definition in Flexio IP layer #if (defined(FLEXIO_PWM_IP_HAS_PIN_OVERRIDE) && (FLEXIO_PWM_IP_HAS_PIN_OVERRIDE == STD_ON)) #if (defined(FLEXIO_PWM_IP_HAS_PIN_OVERRIDE) && (FLEXIO_PWM_IP_HAS_PIN_OVERRIDE == TRUE)) There are drivers that use '#if' preprocessor directives like follow: '#if (COMPILING_CONDITION == TRUE)' or '#if (COMPILING_CONDITION == STD_ON)', or both See also the discussions on this https://teams.microsoft.com/l/message/19:664e0ee3787240d2b4cbd1f568eaab8b@thread.tacv2/1623815330575?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1623815330575&teamName=Zebra&channelName=Group%206&createdTime=1623815330575 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Need to align the macro definition Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Replace in the code 'COMPILING_CONDITION == TRUE' by 'COMPILING_CONDITION == STD_ON' for consistency; this will also help us to fix violations of 'MISRA Rule 10.3' and to avoid the issues reported in this PR https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/pull-requests/520/overview?commentId=861452
ARTD-11763	New	

ID	Subtype	Headline and Description
		New Feature [GPT] Improve Predefine Timer functionality in Design Studio ,,"NewWorkDescription: PredefTimer functionality should automatically calculate the prescaler based on mcu clock reference and selected period value(1us or 100us) Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-11761	New	New Feature [FLS] Investigate to remove unused configurations in the driver ,,"NewWorkDescription: Investigate the two unused nodes in FlsSectorList: *FlsProgrammingSize & *FlsPhysicalSectorUnlock If they are temporarily unused, they should be greyed out to notice to the users. In case of removing, these items should be considered: Check and remove the related constraint with other nodes Check and remove the corresponding resources in the resource files Remove generated code in *Fls_PBcfg.c and the corresponding structures in *Fls_Types.h*: paSectorUnlock Fls_ProgSizeType Remove the related CRC calculation in both generated code and the driver code Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add list to select"
ARTD-11772	Bug	[PORT] Re-check all the bitfields in MSCR registers<*> Detailed description (how to reproduce it): Re-check all the bitfield in MSCR registers. Check one by one if that bitfield can be enabled/disabled when user using Port_Init and other functions. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Re-check all the bitfield in MSCR registers. Check one by one if that bitfield can be enabled/disabled when user using Port_Init and other functions. Expected behavior: All bitifields in MSCRs/PCRs should work correctly Proposed solution optional: All bitifields in MSCRs/PCRs should check again in the code
ARTD-11781	Bug	[ICU] Prescaler configuration do not match eMIOS ones<*> Detailed description (how to reproduce it): The bigger issues comes from the configuration of the prescaler which only allows DIV_1 to DIV_4 which limits the frequency ranges. The maximum divider should be DIV_16. I can assume that this is a porting issues since the used parameters exist on FTM IPs.

ID	Subtype	Headline and Description
		Preconditions: none Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Invalid frequency output. Expected behavior: see above Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update divider enum labels.
ARTD-11786	Bug	[PWM] Error sequence of function Pwm_ipw_SetPeriodAndDuty.<*> Detailed description (how to reproduce it): According to S32K3 Reference Manual Rev 2 DraftC p1878 "59.5.3.7.1 Overview", you must configure AS1, BS1, AS2, and BS2 before exiting GPIO mode.(BS1/BS2 are for period and AS1/AS2 are for duty when used as PWM mode in MCAL.) In MCAL PWM Driver's Pwm_ipw_SetPeriodAndDuty(), they are configured as follows: aeuroeuroaeuroeuroEmios_Pwm_Ip_SetOutputToNormal() aeuroeuroaeuroeuroEmios_Pwm_Ip_SetPeriod() aeuroeuroaeuroeuroEmios_Pwm_Ip_SetDutyCycle() Because mode is changed before configuring period and duty, it is not following description in Reference Manual. This issue also the same with function Pwm_Ipw_SetDutyCycle, Pwm_Ipw_SetDutyCycle_NoUpdate, Pwm_Ipw_SetPeriodAndDuty_NoUpdate. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The sequence in the Pwm_ipw_SetPeriodAndDuty is not following description in Reference Manual Expected behavior: The sequence in the Pwm_ipw_SetPeriodAndDuty should follow description in Reference Manual Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-12099	Bug	[MCL] Prescaler configuration do not match eMIOS ones<*> Detailed description (how to reproduce it): The bigger issues comes from the configuration of the prescaler which only allows DIV_1 to DIV_4 which limits the frequency ranges. The maximum divider should be DIV_16. I can assume that this is a porting issues since the used parameters exist on FTM IPs. Preconditions: none Test Case ID (internal TC that caught the defect) optional: none Observed behavior: Invalid frequency output. Expected behavior:

ID	Subtype	Headline and Description
		see above Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update divider enum labels.
ARTD-12116	Bug	[UART][FLEXIO_UART] Timer Status Flag should be clear if there is no more data to transfer, transmission after the last byte are sent ,,"Detailed description (how to reproduce it): !screenshot-1.png|thumbnail! Link: https://community.nxp.com/t5/Kinetis-Microcontrollers/Understanding-FlexIO/ta-p/1115419 As above information Timer Status Flag (TIMSTAT) should be clear in Flexio_Uart_Ip_CheckTxOperation function to write new data to the SHITBUF register to start the transaction. Preconditions: [...]N/A Test Case ID (internal TC that caught the defect) optional: [...]N/A Observed behavior: [...] Timer Status Flag was not cleared in Flexio_Uart_Ip_CheckTxOperation function Expected behavior: [...] Timer Status Flag should be clear in Flexio_Uart_Ip_CheckTxOperation function by Flexio_Mcl_Ip_ClearTimerStatus Proposed solution optional: [...]
ARTD-12134	Bug	[WDG] The Gpt timer may be stop wrongly<*> Problem detailed description (how to reproduce it): Depending of the WD timeout configured at Tresos and the execution rate of the function that requests the WD refresh, the WD driver can request to stops the refreshment without a real timing issue. Issue scenario: From background, the function Wdg_ChannelSetTriggerCondition(...) is executed to request or not the next watchdog refresh using the Gpt_StopTimer(). The Wdg_ChannelSetTriggerCondition(...) gets the time elapse from the last watchdog refresh using the Gpt_GetTimeElapse (it's done in an isr from a hw timer) and evaluates against a variable Wdg_au32Timeout. The variable Wdg_au32Timeout is also recalculated inside of the function Wdg_ChannelTrigger(...). This function is executed at the hw's timer isr, the one that refresh the watchdog. If the Wdg_ChannelTrigger(...) is executed in the middle of the Wdg_ChannelSetTriggerCondition(...), just after get the time elapsed and before enters at the exclusive area, depending of the times configured at Tresos and the execution rate of our function, the 'if' can stop the timer and don't refresh the watchdog anymore. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional [...] Trigger: [...]

ID	Subtype	Headline and Description
		Observed behavior: The GPT timer is incorrectly stopped Expected behavior: The GPT timer is not stopped Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution (Optional): CE's comment: Gpt_GetTimeElapse should be put in the same ciritical section with the if condition so that it should not be interrupted by GPT ISR or Wdg_ChannelTrigger. The issue was fixed in MCAL legacy: MCAL-18638
ARTD-12179	Bug	[fr] Fix inconsistency related to using 'TRUE' or 'FALSE' instead of 'STD_ON' or 'STD_OFF' for '#if' preprocessor directives<*> Detailed description : There are drivers that use '_*#if*_' preprocessor directives like follow: '_#if (COMPILING_CONDITION == TRUE*)_' or '_#if (COMPILING_CONDITION == STD_ON*)_', or both See also the discussions on this [post.|https://teams.microsoft.com/l/message/19:664e0ee3787240d2b4cbd1f568eaab8b@thread.tacv2/1623815330575?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1623815330575&teamName=Zebra&channelName=Group%206&createdTime=1623815330575] Proposed solution*: Replace in the code '_COMPILING_CONDITION == TRUE*_' by '_COMPILING_CONDITION == STD_ON*_' for consistency; this will also help us to fix violations of '_MISRA Rule 10.3_' and to avoid the issues reported in this [PR|https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/pull-requests/520/overview?commentId=861452]
ARTD-12145	Bug	[LIN] While loop does not end in dummy timer<*> Detailed description (how to reproduce it): In dummy TimeoutTick = timeoutUs !image-2021-06-24-16-46-20-356.png! And ElaspseTime cannot lager or equal to TimeoutTicks [!image-2021-06-24-16-47-05-151.png|width=1065,height=204,id=x_0-weu-d9-48f34d87019cb538a178648310d33971!|https://eu-prod.asyncgw.teams.microsoft.com/v1/objects/0-weu-d9-48f34d87019cb538a178648310d33971/views/imgo] because ElapsedTime always assigned to 1 [!image-2021-06-24-16-47-25-926.png|width=845,height=117,id=x_0-weu-d6-fb6611fd73346c7fc5b2caf3c1de9e5e!|https://eu-prod.asyncgw.teams.microsoft.com/v1/objects/0-weu-d6-fb6611fd73346c7fc5b2caf3c1de9e5e/views/imgo] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior:

ID	Subtype	Headline and Description
		[...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12185	Bug	 [BUILD_ENV] Enum size inconsistency<*> Detailed description (how to reproduce it): Inconsistency found between GHS and GCC compilers regarding enum size. Due to the fact that enum size is compiler dependent, I found that GHS build generates 4bytes for a simple enum, and GCC generates only 1 byte*. This breaks the order of the members in my structures, thus adding unnecessary padding. Unlike GCC 6.3, it seems that GCC 9.2 has short_enum built-in , thus keeping its size as small as possible according to the enum values. (empirical observation, not found in documentation) Preconditions: Enum example typedef enum { CAN_43_LLCE_RECEIVE = 0U, /**< @brief Regular Receive */ CAN_43_LLCE_RECEIVE_AF, /**< @brief Receive with Advanced Features*/ CAN_43_LLCE_TRANSMIT /**< @brief Transmit MB */ } Can_43_LLCE_ObjType; Test Case ID (internal TC that caught the defect) optional: Observed behavior: enums doesn't have the same size between ghs and gcc (versions corresponding to reported version) Expected behavior: enums having the same size Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Possible solutions: # Add short_enum to GHS cfg.mak => 1 byte # Add fno-short-enums to GCC cfg.mak => 4 bytes # Use attribute__((packed)) as an alternative to short_enum. I know this is compiler dependent, but the chances are that it's well understood by many compilers. GHS and GCC have the same understanding on this keyword for sure. If the keyword is understood the same by all your release compilers, it's an alternative.
ARTD-12202	New	 New Feature [MCU] Add support callback notification when using the IPL only ,,"NewWorkDescription: Now Mcu doesn't support callback notification function at IPL. some callback function should be supported when using IP layer only. ex: POWER_IP_VLPSA_NOTIFICATION Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support callback notification at IPL"

ID	Subtype	Headline and Description
ARTD-12226	New	New Feature [adc] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12230	New	New Feature [crypto] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections.

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		For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12231	New	New Feature [dem] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
		static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12232	New	New Feature [det] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12234	New	New Feature [ecum] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation.

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		For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12236	New	 New Feature [eth] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
		>#define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12240	New	New Feature [fls] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"

ID	Subtype	Headline and Description
		static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12225	New	 New Feature [ICU] Improve generation for K3 after ZSE update of SIUL2 IP files ,,"Detailed description (how to reproduce it): [Current generation of SIUL2 IP files(updated to support multiple instances of SIUL2 for ZSE) will conduct to a error in generation and build.] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [Successfully generation and build.] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]"
ARTD-12242	New	 New Feature [gpt] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN

ID	Subtype	Headline and Description
		#include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12243	New	 New Feature [i2c] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12245	New	 New Feature [icu] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example:

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ARTD-12249	New	 New Feature [ocu] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" >

ID	Subtype	Headline and Description
		#define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12251	New	 New Feature [port] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/

ID	Subtype	Headline and Description
		#define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12252	New	 New Feature [pwm] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12255	New	 New Feature [rte] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections:

ID	Subtype	Headline and Description
		"These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12258	New	New Feature [sent] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections.

ID	Subtype	Headline and Description
		For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12259	New	 New Feature [spi] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12262	New	 New Feature

ID	Subtype	Headline and Description
		[wdg] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-12290	Bug	[LIN] - Flexio irq handler channel parameter is not correct<*> Detailed description (how to reproduce it): A flexio lin channel contains 2 hw flexio channels (pairs of shiftertimer) Configure a flexio lin channel. Use another Mcl Flexio channel than 0 and 1. Driver don't check driver is initialized in ISR of IPV Flexio Preconditions: Follow req CPR_RTD_00011.lin: ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. This requirement is implemented from Lpuart !image-2021-07-09-09-39-22-271.png! Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: In this case, the Mcl Flexio Irq is called using the shifter+timer pair channel number. Inside Flexio Lin driver, there is different scheme of channels which are using the pairs of shifter timer. This is why the wrong channel is addressed.

ID	Subtype	Headline and Description
		Expected behavior: In Flexio Lin Irq, the correct channel must be addressed. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add an easing mapping between the Mcl Flexio channels (hardware channels) and Flexio Lin channels (driver channels)
ARTD-12330	Bug	[ICU]: When add ICU module, it rely on MCL module even I didn't add emios CH ,,"Detailed description (how to reproduce it): I add ICU module in my project, and in ICU module I didn't add any EMIOS channel. But when generate code, EB Tresos Studio report error related with EMIOS. I need add MCL module, in MCL module, I didn't configure any item, just keep default value, then that error disappeared. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12333	New	New Feature [gpt] RTD Clock source selection duplication in RTC and clock component ,,RTD Clock source selection duplication in RTC and clock component. More details please see the attachment.
ARTD-12350	Bug	[GPT][eMIOS] The GPT channel prescaler doesn't support Extended Prescaler.<*> Detailed description (how to reproduce it): The GPT channel prescaler is up to 4, not the available max value 16 described in RM. (Extended Prescaler not support) !image-2021-07-01-11-18-21-749.png! Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Extended Prescaler (up to 16 frequency division) support for GPT channel. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12352	Bug	

ID	Subtype	Headline and Description
		[S32K3 RTM] OCU: The master bus of OCU channel will be wrongly changed to MC mode.<*> Detailed description (how to reproduce it): In ConfigTools, we must set the master bus of OCU channel to MCB up counter mode, or it will report an errors like follow: !image-2021-07-01-12-46-51-520.png! However, the API Emios_Ocu_Ip_Init() in Emios_Ocu_Ip.c sets the master bus to MC up counter mode. It's inconsistent. !image-2021-07-01-12-50-27-320.png|width=1305,height=440! Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: The master bus of OCU should be set to MCB mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12356	New	 New Feature [ICU]: The channel number of WKPU will mislead customers ,,"In S32K3, there are total 64 wake up channels, and the first four channels are a special internal wake up source, start from the fifth wake up source are from external pin pads. In the Port module and the in the reference document, the number for internal and external are indepdent. This cause the number which configured in ICU module are not equal to document and which in port module, this will let customer confused. Is there any method to import it. Like we can change to drop-down box. This problem also exist for the interrupt isr name in ICU module, it named for 0 to 63, but in the reference document, the external source from 0 to 59, and the internal source have a special name for each one. !image-2021-07-01-15-16-20-716.png! !image-2021-07-01-15-15-57-316.png! !image-2021-07-01-15-15-34-451.png!"
ARTD-12353	Bug	 [PWM][eMIOS] The restoration operation of Interrupt is not carried out when using DAOC PWM mode.<*> Detailed description (how to reproduce it): When we using RTD to configure PWM, the interrupt will be disabled and global variable Emios_Pwm_Ip_aNotif of corresponding channel will be set to 1 if 0% or 100% duty is required. Normally, the restoration operation of interrupt will be carried out when set to other duty. Just for explanation, take the OPWMT PWM mode as an example like follow: !image-2021-07-01-13-56-39-589.png! However, when using DAOC PWM mode, the restoration operation of Interrupt is not carried out: !image-2021-07-01-13-44-20-879.png! Besides, in the config structure generated by Emios_Pwm component, if it is DAOC PWM mode, the generated mode is incorrect, it should be EMIOS_PWM_MODE_DAOC_FLAG: !image-2021-07-01-14-03-46-346.png!

ID	Subtype	Headline and Description
		Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix the restoration operation of interrupt for DAOC PWM mode when set to non-zero and non-hundred duty. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12354	Bug	[PWM][eMIOS] The DAOC PWM mode of RTD generates wrong PWM signal.<*> Detailed description (how to reproduce it): In the DAOC mode of PWM, the Period is gray and cannot be configured, but in Emios_Pwm_Ip_Irq.c, Emios_Pwm_Ip_IrqDaocHandler() will use this value, and this value is not the actual period (the actual period is related to the selected bus). This will cause the generated PWM to be incorrect. See follow pictures for more imformation: !image-2021-07-01-14-20-10-564.png! !image-2021-07-01-14-20-19-518.png! !image-2021-07-01-14-21-22-260.png! !image-2021-07-01-14-21-35-725.png! Preconditions: S32DS3.4 RTD v0.9.0, LLD Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix the period configuration of DAOC PWM mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12355	Bug	[ICU][eMIOS] There are some problems when using ICU component in CT.<*> Detailed description (how to reproduce it): 1. DMA doesn't support for ICU component in RTD 0.9.0 Beta 2. When the ICU channel selects a global bus as time base, there will be a error in CT. However, the Code can be generated normally. !image-2021-07-01-14-51-37-717.png! 3. The ICU channel prescaler is only up to 4, not the available max value 16 described in RM. (Extended Prescaler not support) !image-2021-07-01-14-52-52-624.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior:

ID	Subtype	Headline and Description
		[...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-12401	New	New Feature [S32K3 RTM] Driver activities for S32K3XX ,,"IPs list: [see SOW for details|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&id=%2Fsites%2FZebra%2FShared%20Documents%2FProject%20Management%2FProjects%20Planning%2FSW32K3%5FRTD%5F4%2E4%5F1%2E0%2E0%2FSchedule] "
ARTD-12610	New	New Feature [S32K3 RTM] Driver activities for DEM ,,"IPs list: [see SOW for details|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&id=%2Fsites%2FZebra%2FShared%20Documents%2FProject%20Management%2FProjects%20Planning%2FSW32K3%5FRTD%5F4%2E4%5F1%2E0%2E0%2FSchedule] "
ARTD-12619	New	New Feature [S32K3 RTM] Driver activities for BASE ,,"IPs list: [see SOW for details|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?viewid=49fc7681%2D6f70%2D4be1%2Dbc92%2Dc033431dbf2d&id=%2Fsites%2FZebra%2FShared%20Documents%2FProject%20Management%2FProjects%20Planning%2FSW32K3%5FRTD%5F4%2E4%5F1%2E0%2E0%2FSchedule] "
ARTD-12990	Bug	[UART] While loop is infinity in dummy timer<*> Detailed description (how to reproduce it): In Osif Dummy counter mode, OsIf_GetCounter always returns 0, then Uart_Ip_CheckTimeout always return FALSE Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-13000	Bug	[S32K1XX RTM] SPI: DMA Fast mode transmit with wrong default data<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): DMA Fastmode transmit with wrong default data When setup EB TX buffer with NULL_PTR for transmit with default data which configured at channel transferred on EB tresos. The data transmit from master is not correct. I have solution to fix, please take a look on that and fix this bug: in Lpspi_Ip_DmaFastConfig() function: !image-2021-07-02-17-56-45-437.png! in Lpspi_Ip_TxDmaTcdSGConfig() function: !image-2021-07-02-17-58-03-914.png! !image-2021-07-02-17-57-51-916.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Spi_TC_FCT_10134 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-13155	New	New Feature [FEE] Add support for bad Sector Management and Sector Retirement (part 2) ,,"NewWorkDescription: Add support for bad Sector Management and Sector Retirement (CPR_RTD_00505.fee). This involves removing Sectors from configuration when they become unusable. Rationale: some flash memory specs have low endurance/write cycles availability, which needs to be improved by the ability to retire bad sectors or locations affected by permanent ECC, at the expense of allocated flash size the endurance being a ppm specification."" Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: # Add support to manage sectors status and retire the bad ones # Add support to remove Sectors from configuration Update Fee_GetRunTimeInfo to include the sectors information Analyze the solution and add the method/scenario to users can replace bad sectors from configuration"
ARTD-13165	Bug	[CAN] Controller remains bus-off state and cannot participate on CAN bus after restarting engine<*> Detailed description (how to reproduce it): After Bus-off event occurred, ESR1[FLTCONF] will be set to 11b (indicates bus-off state), Can_MainFunction_Busoff() or bus-off ISR will set the CAN controller to stop mode. Call Can_SetControllerMode(CAN_CS_STARTED) to exit bus-off state and starting transmit a new message but the data cannot be transmitted.

ID	Subtype	Headline and Description
		ESR1[FLTCONF] still remains 11b even Can_SetControllerMode(CAN_CS_STARTED) has been executed successfully. !image-2021-07-06-11-16-02-886.png|width=1306,height=695! I have tried to request soft reset by asserting MCR[SOFTRST] before set controller to start mode and then the data can be transmitted successfully. It means that we should have a soft reset in restart the CAN controller after bus-off event occurred (as known is manual recover bus-off). Preconditions: Don't use auto bus-off recovery. Test Case ID (internal TC that caught the defect) optional: Can_TC_FCT_1012 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-13167	New	 New Feature [PORT] The Exclusive Areas should be reviewed and updated for S32K3/S32XX/ S32ZSE platforms ,,"NewWorkDescription: The Exclusive Areas for K1 platform are incorrect. Some of them are redundant (need to be removed), and the rest need to be renamed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove/Add/Renaming the Exclusive Areas in code for K1. From IPW to IPL. All exclusives should be existed in IPL. The ones in IPW should be removed. Update the UM/IM if needed Check and update RTE if needed"
ARTD-13171	Bug	 [S32CC][S32K3XX] Crypto driver doesn't raise an error when CryptoPrimitives configuraion fails<*> Detailed description (how to reproduce it): When config CryptoPrimitiveService is decrypt or encrypt , CryptoPrimitiveAlgorithmSecondaryFamily should be CRYPTO_ALGOFAM_NOT_SET or CRYPTO_ALGOFAM_CUSTOM but acctually ,config is CRYPTO_ALGOFAM_RNG or CRYPTO_ALGOFAM_AES When config CryptoPrimitiveService is decrypt or encrypt , driver EB not raise generate error . I try config same parameter on CT and Driver gen fail CRYPTO_ALGOFAM_RNG or CRYPTO_ALGOFAM_AES. You can see picture i cap screen bellow attachments site Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Driver not generate fail when config CryptoPrimitiveService is encrypt or decrypto and CryptoPrimitiveAlgorithmSecondaryFamily is CRYPTO_ALGOFAM_RNG or CRYPTO_ALGOFAM_AES at the same time Expected behavior:

ID	Subtype	Headline and Description
		Driver raise gen fail when config fail Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-13193	New	 New Feature [S32K3XX] Replace "NO_INIT" with "CLEARED" in memory section macros" ,,"1. Replace "NO_INIT" with "CLEARED" in the memory section identifiers of both source code files and documentation. For example: <MIP>_START_SEC_VAR_NO_INIT_UNSPECIFIED > <MIP>_START_SEC_VAR_CLEARED_UNSPECIFIED <MIP>_STOP_SEC_VAR_NO_INIT_32 > <MIP>_STOP_SEC_VAR_CLEARED_32 ... 2. In file "sections_to_be_defined_in_memmaph.dox", perform the following replacement in the description field of the "CLEARED" (formerly "NO_INIT") sections: "These variables are never cleared and never initialized by start-up code." > "These variables are cleared to zero by start-up code." 3. Move all zero-initialized variables into the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_INIT_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" 4. Remove all explicit zero-initializers in the "CLEARED" memory sections. For example: #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed = (boolean)FALSE; / explicit zero initialization / #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" > #define FEE_START_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h" static boolean bSwapToBePerformed; / implicit zero initialization*/ #define FEE_STOP_SEC_VAR_CLEARED_BOOLEAN #include "Fee_MemMap.h"
ARTD-13728	New	 New Feature [MCU] Add support for warm resetting the A53/M7 cores on S32XX ,,"NewWorkDescription: Add support for warm resetting the A53/M7 cores on S32XX Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:

ID	Subtype	Headline and Description
		Add support for warm resetting the A53/M7 cores on S32XX"
ARTD-13727	Bug	[PORT] Missing section memory for Port_Config pointer in S32K3XX<*> Detailed description (how to reproduce it): !image-2021-07-07-15-11-39-210.png! This array need to be placed into PORT_START/STOP_SEC_CONFIG_DATA_UNSPECIFIED Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Missing section memories for Port_Config array Expected behavior: Port_Config should be placed into a section memory Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-13826	New	New Feature [ICU] Evaluate if <IP>_Icu_Ip_EnableNotification and <IP>_Icu_Ip_DisableNotification are needed ,,"NewWorkDescription: Pls see [comment|https://bitbucket.sw.nxp.com/projects/ARTD/repos/icu/pull-requests/264/overview?commentId=873554] for more details Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-13827	Bug	[CRYPTO] Fix issue with define CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT not activated in EBT Crypto_Cfg.h file<*> Detailed description (how to reproduce it): When configuring CryptoKeyElements that are having the HSE Key Export checkbox ticket, the value of the define CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT in Crypto_Cfg.h is generated with STD_OFF value Preconditions: There is no keyElement configured with HSE Encrypted Key Import or HSE Authenticated Key Import options activated Test Case ID (internal TC that caught the defect) optional: Problem was discovered while building a new example application Observed behavior: CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT in Crypto_Cfg.h is generated with STD_OFF value Expected behavior: CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT in Crypto_Cfg.h is generated with STD_ON value Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		The CRYPTO_ENABLE_ENC_AUTH_KEY_EXPORT wrongly uses an internal variable computed for key import. Only need to update the variable to be the one computed for key export.
ARTD-13851	New	New Feature [ADC] Support External Dma for without Interrupts ,,"Consider to support AdcExtDMAChanEnable when AdcWithoutInterrupts is enabled. Proposed Solution: An alternative solution might be to use in this case the buffer registered by the user with Adc_SetupResultBuffer()"
ARTD-13951	Bug	[CRYPTO] Remove descriptor feeding feature code for the platforms without HSE firmware<*> Detailed description (how to reproduce it): At build time for S32K1XX platform warnings will be reported for {color:#172b4d}CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT macro because it is not defined. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT is undefined. Expected behavior: CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT usage and the code incapsulated by the macro will be removed from plugin code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CRYPTO_ENABLE_FEED_HSE_DESC_SUPPORT usage and the code incapsulated by the macro should be removed from plugin code with M4 tags.
ARTD-13954	New	New Feature [MCU][S32K3XX][BASE] SleepOnExit incompatible with current approach on supervisor/user mode ,,"NewWorkDescription: Problem: Sleep On Exit bit from System Control Register can only be written in supervisor mode The behavior is that at the exit from the next interrupt the core goes to sleep !image-2021-07-21-09-48-39-401.png|width=776,height=121! When the driver is called in user mode context writing this bit will do the following: SVC_GoToSupervisor Write SLEEPONEXIT SVC_GoToUser Because SVC_GoToUser is currently implemented using the svc handler (which is an interrupt) the result is that the core goes in sleep immediately after going back to user mode For detail please the email attached. Requirement source: CPR_RTD_00447.mcu Req Text*: The MCU driver shall offer support to control the exception return behavior of the currently executing core on a wake-up event triggered during SLEEP. The function void Mcu_SleepOnExit (boolean enableSleepOnExit) will enable/disable the automatic sleep entry on exception return.

ID	Subtype	Headline and Description
		Requirement ticket: AAI-498 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 2 step must be done in Base, platform and mcu driver to avoid this issue 1. Base and Platform will implement the transition from supervisor mode to user mode without using the SVC Handler? Instead, just writing the CONTROL bit? !image-2021-07-21-09-49-10-553.png|width=801,height=141! 2. Mcu driver implementation: Add another function to the API to enable/disable calling Power_Ip_EnableSleepOnExit in the driver right before the WFI. Note that a pre-compile switch might not be enough since the application could choose not to enable SleepOnExit before every sleep cycle."

ARTD-13969	Bug	
		Remove warning when don't use D_CACHE_ENABLE macro<*>
		
		Detailed description (how to reproduce it):
		Warning happen when don't use D_CACHE_ENABLE macro
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		[...]
		Expected behavior:
		There aren't warning when don't use D_CACHE_ENABLE macro
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Move those line
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		into
		
		#ifdef D_CACHE_ENABLE
		uint32 ccsidr = 0U;
		uint32 sets = 0U;
		uint32 ways = 0U;
		...
		#endif

ARTD-14027	New	 New Feature CLONE - [SPI] Create SPI feature for 1/2/4/8-bit half duplex mode ,,"NewWorkDescription: Implement 4-bit half duplex mode according requirements # The Spi driver shall be able to transfer in half duplex mode supporting 2/4/8-bit parallel transmission or reception on each clock edge. # A vendor specific pre-compile boolean configuration parameter SpiHalfDuplexModeSupport shall enable/disable this functionality. # By default this optional functionality and configuration parameters shall be disabled. ITWG ticket: https://jira.sw.nxp.com/browse/AAI-632 Requirement source: [...]

ID	Subtype	Headline and Description
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-14029	Bug	 [WDG] Instance 1 code was incorrectly generated<*> Detailed description (how to reproduce it): Generation code in Wdg_43_Instance_1 was mismatched compares to the configuration values. Preconditions: Wdg_43_Instance_1 is added. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generation code in Wdg_43_Instance_1 was mismatched compares to the configuration values. Expected behavior: Generation code in Wdg_43_Instance_1 should be correct compares to the configuration values. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In Swt_43_Instance1_Ip_PBcfg.c when WdgModeConfig and WdgModeConfig are executed the WdgNo is empty : [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsSlow'","WdgNo" = """!] [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsFast'","WdgNo" = """!] this should be change to : [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsSlow'","WdgNo" = "'_43_Instance1'"!] [!CALL "WdgModeConfig","WdgMode" = "'WdgSettingsFast'","WdgNo" = "'_43_Instance1'"!] Same issue is present in Wdg_43_Instance1_PBcfg.c for WdgTriggerPeriod call. In Wdg_PluginMacros.m for WdgTriggerSourceClock variable also is not used the instance in path : [!VAR "WdgTriggerSourceClock" = "num:i(node:value(node:ref(./../../../Wdg/ELEMENTS/Wdg/WdgSettingsConfig/WdgExternalTriggerCounterRef)/GptChannelTickFrequency)div 1000)"!] this should be changed to : [!VAR "WdgTriggerSourceClock" = "num:i(node:value(node:ref(node:value(concat('./../../../Wdg',$WdgNo,'/ELEMENTS/Wdg/WdgSettingsConfig/','WdgExternalTriggerCounterRef')))/GptChannelTickFrequency)div 1000)"!]
ARTD-14044	Bug	 [SAI] Compile error with generation code with no EcuC<*> Detailed description (how to reproduce it): When generating code with no EcuC and no variant, the code can't be compiled: !image-2021-07-15-20-07-49-835.png! Preconditions: SAI generating code with no EcuC Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiled error with configuration code Expected behavior: Code can be compiled

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In CDD_Sai_PbCfg.h, the below code is generated: #define SAI_CONFIG_PB \ extern const Sai_ConfigType Sai_Config;\ #define SAI_STOP_SEC_CONFIG_DATA_UNSPECIFIED #include "Sai_MemMap.h" It can be compiled if adding a blank line: #define SAI_CONFIG_PB \ extern const Sai_ConfigType Sai_Config;\ #define SAI_STOP_SEC_CONFIG_DATA_UNSPECIFIED #include "Sai_MemMap.h"
ARTD-14119	Bug	[OS] OsApplicationCoreRef and OsAppEcucPartitionRef shall be implemented as parameters<*> Detailed description (how to reproduce it): In SW32K3_RTD_4.4_0.9.0_D2103 MCAL, many drivers use OsAppEcucPartitionRef and OsApplicationCoreRef as reference, for instance in Eth driver: [!LOOP "as:modconf('Os')[1]/OsApplication/*/OsAppEcucPartitionRef/*"!] [!IF "node:value(.) = $EcucPartitionRef"!] [!IF "node:refvalid(../../OsApplicationCoreRef/*[1])"!] [!VAR "CoreId" = "num:i(node:value(node:ref(../../OsApplicationCoreRef/*[1])/EcucCoreId))"!] In this case the OsAppEcucPartitionRef and OsApplicationCoreRef are used as an list. According with Autosar specification these two containers is EcucReferenceDef, which can be only one parameter, and they shall not be a list, which contains one or more parameters (see attachment). Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In customer's OS, the OsAppEcucPartitionRef and OsApplicationCoreRef are implemented as parameter, while Eth driver is used as lists. As a result, the configuration and generation are failed. Expected behavior: OsApplicationCoreRef and OsAppEcucPartitionRef shall be implemented as parameters, instead of lists Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-14120	Bug	[PWM] Unknown path with $pluginPath and unknown derivate when S32K3XX is not used<*> Detailed description (how to reproduce it): 1. In PWM, generators file is used path for ".m" file like : [!INCLUDE "?concat($pluginPath,'/generate_PB/Pwm_NotifyCheck_Src.m')"!]

ID	Subtype	Headline and Description
		During customers integration, they created their own plugin and reference the generator from NXP delivered plugins. In this case, when MCAL is integrated, pluginPath will point to different location and Pwm_NotifyCheck_Src.m cannot be used. 2. With this piece of code [!IF "$derivate = 'S32K3XX'"!] #include "S32K344_EMIOS.h"[!ENDIF!] In customer's case the derivate is S32K34X so the include will not be generated. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Generation error regarding the path incorrect. Compile error regarding the mismatch derivate Expected behavior: Pwm_NotifyCheck_Src.m can be included when code generating. #include "S32K344_EMIOS.h" can be added in generation code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-14125	New	 New Feature [PWM][EMIOS] Investigate SetPhaseShif time improvements ,,"NewWorkDescription: According to the performance measurement done on PWM EMIOS IPL APIs the Emios_Pwm_Ip_SetPhaseShift can take up to 3.5 us to execute at default core/ pheripheral clock. Investigate if there are any improvements that can be done in the code to reduce the time needed to perform the update. Check if merging the phaseShift and dutyCycle will have a notable improvement. Investigate cases where safety checks can be omitted for a new specific motor control API. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: One solution could be to not read form hw the current dutyCycle."
ARTD-14126	New	 New Feature [PWM][EMIOS] Investigate SetDutyCycle time improvements ,,"NewWorkDescription: According to the performance measurement done on PWM EMIOS IPL APIs the Emios_Pwm_Ip_SetDutyCycle can take up to 3.5 us to execute at default core/ pheripheral clock. Investigate if there are any improvements that can be done in the code to reduce the time needed to perform the update. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-14172	Bug	 [UART] - ISR does not check if driver is initialized for Flexio Ip<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Preconditions: Follow req CPR_RTD_00011.lin: ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. Eventhough the Flexio Mcl Common Irq checks if the macro corresponding the Uart channels configured before the Flexio_Uart_Ip_Irq function is called, the Flexio_Uart_Ip_Init() may not have been initialized on the channel in use, This must be checked in the Flexio_Uart_Ip_IrqHandler. Lpuart driver approach can be applied. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Check if driver has been initialized for the channel in use. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check driver state structure to be different than NULL_PTR
ARTD-14173	New	New Feature [PWM][EMIOS] Implement missing checks in S32CT generation ,,"NewWorkDescription: The S32CT pwm emios generation on K3 platform is missing the checks for mcl counter bus. These checks must be added in the S32CT component as these are present in the EBT plugin. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-14220	Bug	[ADC] Adc_SetChannel function prototype does not match with requirement because of const qualifiers<*> Detailed description (how to reproduce it): Some function prototypes do not match with requirement Preconditions: Review new interface requirements Test Case ID (internal TC that caught the defect) optional: Review requirement Observed behavior: CPR_RTD_00329.adc: The optional API prototype shall be: void Adc_SetChannel(Adc_GroupType Group, Adc_GroupDefType Channel, #if (ADC_DELAY_AVAILABLE == STD_ON) uint16 Delays, uint32 ChannelUpdateMask, #endif / (ADC_DELAY_AVAILABLE == STD_ON) / Adc_ChannelIndexType NumberOfChannel); In driver:

ID	Subtype	Headline and Description
		void Adc_SetChannel(const Adc_GroupType Group, const Adc_GroupDefType Channel, const uint16 Delays, const uint32 ChannelUpdateMask, const Adc_ChannelIndexType NumberOfChannel) SWS_Adc_00082: Service name: IoHwAb_AdcNotification - Syntax: void IoHwAb_AdcNotification(void) - In driver: Not found comment in ticket ARTD-14077 Expected behavior: Matching between requirement and driver Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14236	New	 New Feature CLONE - [S32K1 RTM] SPI: Improve IPL code to improve decision coverage when using DevAssert() ,,"NewWorkDescription: As IPL function below, we can not test with cases which go into conditions such as ExternalDevice=NULL_PTR. So, we need to change the implement way for these sketch. !image-2021-07-15-15-19-01-921.png! Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-14240	Bug	 [UART] Conflict if using common callback in the same channel<*> Detailed description (how to reproduce it): If user uses the common callback in channel for his program, it will cause conflict, bcs the declaration of callback functions will generate several times in EB/CT generated code. It can cause the compiler warning for dupplicate declaration. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14242	Bug	 [UART] In Abort case, Complete Send/Receive internal functions need to wait for finishing of current byte transmission ,,"Detailed description (how to reproduce it): In Abort function, Complete Send/Receive internal functions are called to finish the current transmission. But they need to wait for finishing of current byte transmission and afterward disable TE and RE. Preconditions:

ID	Subtype	Headline and Description
		[...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14255	Bug	 [ADC] aAdcUnitSupportCtuControlMode and aHwLogicalId are generated incorrectly on EB<*> Detailed description (how to reproduce it): aAdcUnitSupportCtuControlMode and aHwLogicalId are generated incorrectly aHwLogicalId: when only 1 ADC is configured then only 1 element is generated for this array instead of equal to max ADC unit aAdcUnitSupportCtuControlMode is always generated as 1 = unit enabled but actually unit is disabled Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: aAdcUnitSupportCtuControlMode and aHwLogicalId are generated correctly Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14286	Bug	 [ADC] Configure channel limit check with set channel feature is not working<*> Detailed description (how to reproduce it): Need to note that set limit check channel for group only in case this group configured with limit check channel Preconditions: Group configured with normal channel Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1401 Adc_TS_006 cfg 7 Observed behavior: Calling set channel to new channel with range ADC_RANGE_UNDER_LOW, AdcChannelLowLimit is 0 Set voltage for this new channel as 4V Enable Hw trigger group Start trigger Expected: group status is not streaming complete and timeout occurred Stop trigger Disable Hw trigger group Real status: group status is stream complete because in ISR AdcGroupLimitCheck variable set as FALSE Expected behavior:

ID	Subtype	Headline and Description
		Timeout because of out range voltage Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14292	New	 New Feature [ADC] Merge containers for channel configuration for chains and channel configuration array into single one for Adc_Sar_Ip component ,,"NewWorkDescription: In IPL, there are 2 containers for channel configurations that might confuse users when configuring for channels. Propose to merge them into single one Requirement source: Improvement Proposed solution optional: NA !image-2021-07-22-18-19-34-566.png!"
ARTD-14428	Bug	 [GPT] Check and update the functions that don't match the requirements<*> Detailed description (how to reproduce it): Some function in "ReqExport.txt" file but does not include in "*.h" files of driver code pls see attached files for more details Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check and update for all APIs
ARTD-14306	New	 New Feature [CAN] re-analysis Exclusive Area ,,"NewWorkDescription: some code changed, need to re-analyze EA Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-14304	Bug	 Power_Ip_GetResetReason can not return MCU_WAKEUP_REASON<*> Detailed description (how to reproduce it): Power_Ip_GetResetReason API can not return MCU_WAKEUP_REASON after occurring reset event during standby mode. Because all registers of MC_ME will be reset after occurring reset event during standby mode, so Power_Ip_MC_ME_GetPreviousMode can not return

ID	Subtype	Headline and Description
		POWER_IP_SOC_STANDBY_MODE which result Power_Ip_GetResetReason API can not return MCU_WAKEUP_REASON. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14312	Bug	 RTC TRIG_EN can not be configurated by any API<*> Detailed description (how to reproduce it): K3 MCAL does not provide any API to configure RTC's TRIG_EN bit. If using LPCMP to wake up MCU, RTC will cyclically[^RTC_Trigger_LPCMP_bug.pptx] trigger the LPCMP sample. If the voltage input is bigger than expected, MCU will be awakened. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14322	New	 New Feature [RM] [S32K3XX] Improve coding convention for Xbic Ip ,,"NewWorkDescription: File's name are not follow coding convention. XBIC_IP_ should change to Xbic_ip. Ex: XBIC_IP_Types.h change to Xbic_Ip_Types.h Remove useless file: XBIC_Ip_Cfg_Defines.h Update to include correct file's name after updating above. Update .mak file (for gen plugin) to correct file's name after updating above. Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: As description"
ARTD-14347	New	 New Feature [BASE] Add header files for S32K312 ,,"NewWorkDescription: Add header files for S32K312 Requirement source: RM rev 2 Draft B

ID	Subtype	Headline and Description
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-14362	New	 New Feature [RESOURCE] Add resource for S32K312 and S32K311 ,,"NewWorkDescription: Add resource for S32K312 and S32K311. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-14373	Bug	 [Adc] UM does not specify that groups with 1 channel do not use DMA scatter gather<*> Detailed description (how to reproduce it): UM does not specify that groups with 1 channel do not use DMA scatter gather so this must be disabled in DMA channel config Expected behavior: UM contains all details regarding DMA config for this case Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add note in "DMA transfer" chapter from 3.6 Driver usage and configuration tips Check if any other DMA scenarios/configs are not described by this chapter
ARTD-14375	Bug	 [ADC] ADC_VALIDATE_APP_BUFFER_ALIGNMENT is never defined<*> Detailed description (how to reproduce it): ADC_VALIDATE_APP_BUFFER_ALIGNMENT is never defined, resulting in Adc_ValidateSetupBufferAlignment() never being actually called. Proposed solution optional: Check if this check is still needed/working, also in MCAL If needed define should be generated by config. Otherwise function code removed
ARTD-14381	New	 New Feature [MCU] SleepOnExit incompatible with current approach on supervisor/user mode ,,"NewWorkDescription: Problem: Sleep On Exit bit from System Control Register can only be written in supervisor mode The behavior is that at the exit from the next interrupt the core goes to sleep !image-2021-07-21-08-44-11-091.png|width=816,height=126! When the driver is called in user mode context writing this bit will do the following: SVC_GoToSupervisor Write SLEEPONEXIT SVC_GoToUser Because SVC_GoToUser is currently implemented using the svc handler (which is an interrupt) the result is that the core goes in sleep immediately after going back to user mode For detail please the email attached. Requirement source: CPR_RTD_00447.mcu

ID	Subtype	Headline and Description
		Req Text*: The MCU driver shall offer support to control the exception return behavior of the currently executing core on a wake-up event triggered during SLEEP. The function void Mcu_SleepOnExit (boolean enableSleepOnExit) will enable/disable the automatic sleep entry on exception return. Requirement ticket: AAI-498 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 2 step must be done in Base, platform and mcu driver to avoid this issue 1. Base and Platform will implement the transition from supervisor mode to user mode without using the SVC Handler? Instead, just writing the CONTROL bit? !image-2021-07-21-08-46-09-719.png|width=800,height=151! 2. Mcu driver implementation: Add another function to the API to enable/disable calling Power_Ip_EnableSleepOnExit in the driver right before the WFI. Note that a pre-compile switch might not be enough since the application could choose not to enable SleepOnExit before every sleep cycle."
ARTD-14384	New	New Feature [ETH]Fix build failed on K3 ,,"NewWorkDescription: Fixed build failed caused by general files Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Fixed build failed caused by general files"
ARTD-14400	Bug	[S32K3XX][RM] Mpu_M7 can't getResource on S32DS<*> Mpu_M7 can't getResource on S32DS, see on attach picture
ARTD-14413	Bug	[SAI] Unfixed MISRA violations of rule 8.13<*> Detailed description (how to reproduce it): Unfixed MISRA violations for rule 8.13, outside list of accepted project level deviations (MISRA violations for Rules are only accepted in cases specified by column D with disclaimer from column E for document with project level deviations): aData is assigned to pData in the state structure which is used for both TX and RX, so cannot be const This ticket is raised to analyze and confirm if code can be refactored to avoid these violations. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14409	New	

ID	Subtype	Headline and Description
		New Feature [BUILD_ENV] Add support for S32K312 and S32K311 derivative ,,"NewWorkDescription: Add new derivatives. Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-14436	Bug	 [ADC] Reset sample index in ISR and bRuntimeUpdated status if runtime channels are updated by Adc_SetChannel<*> Detailed description (how to reproduce it): Reset sample index if runtime channels updated by Adc_SetChannel, before ISR is called or in extra notification Preconditions: NA Expected Voltage: Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1101 Adc_TS_017 cfg 3channelsBeforeStart Observed behavior: NA Real status: Wrong data in notification Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14474	New	 New Feature [RM] Add prefix "XRDC" for some definitions of Xrdc ip" ,,"NewWorkDescription: Some define of Xrdc don't have prefix "XRDC". it can make duplicate in header files !image-2021-07-29-14-48-04-296.png! Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add prefix XRDC
ARTD-14478	New	 New Feature [RM][S32K3XX] Fix gen fail in CT for Ip Pflash,Abxs,Xbic,Xrdc,VirtualWapper" ,,"NewWorkDescription: Update generating code of IP PFlash, Abxs, Xbic, Xrdc, Virtual Wrapper for S32K3XX in CT Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove enable attribute of corresponding node
ARTD-14481	Bug	

ID	Subtype	Headline and Description
		[MCU] The function Mcu_Ipw_CmuClearClockFailIrqFlags isn't called in HLD<*> Detailed description (how to reproduce it): The function Mcu_Ipw_CmuClearClockFailIrqFlags didn't be called in HLD !image-2021-07-29-17-18-43-915.png! Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The function Mcu_Ipw_CmuClearClockFailIrqFlags didn't be called in HLD Expected behavior: Remove the function Mcu_Ipw_CmuClearClockFailIrqFlags in driver code Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-14485	Bug	[ADC] Configurator generates multiple times the notification prototype, when same notification is used for multiple groups
		
		,,"Detailed description (how to reproduce it):
		Tresos configurator generates multiple times the notification prototype, when same notification is used for multiple groups
		To check if also S32CT has same issue
		Preconditions:
		Have a configuration with multiple groups that use the same notification.
		Test Case ID (internal TC that caught the defect) optional:
		TS_Shared_000
		Observed behavior:
		Each notifications declared in the EB config is generated more than once:
		/
		brief ADC Notification functions.
		details ADC Nofification functions defined inside the Plugin.
		/
		extern void Notification_0(void);
		extern void Notification_1(void);
		extern void T_ADC_Notification(void);
		extern void T_ADC_Notification(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void T_ADC_Notification(void);
		extern void T_ADC_Notification(void);
		extern void Notification_4(void);
		extern void Notification_5(void);
		extern void T_ADC_Notification(void);
		extern void Notification_1(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		extern void Notification_0(void);
		Expected behavior:

ID	Subtype	Headline and Description
		Each notification must be declared only once. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14487	Bug	 [ADC] IPW notification prototype is defined both in driver code as well as generated code<*> Detailed description (how to reproduce it): IPW notification prototype is defined both in Adc_Ipw_Irq.c file as well as Adc_Ip_PBCfg.h generated file. Preconditions: Use a HLD config that is using interrupts. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: IPW notification prototype is defined both in driver code as well as generated code. Expected behavior: IPW notification should be defined only once. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove IPW notification prototype from Adc_Ipw_Irq.c.
ARTD-14490	Bug	 [Mcl] error in field dmaLogicInstance_ConfigType of xdm file<*> Detailed description (how to reproduce it): In SW32K3_RTD_4.4_0.9.0_D2103 MCAL in Mcl schema file for dmaLogicInstance_ConfigType list is used this path on invalid check: <a:tst expr="(../../MclGeneral//MclDma/MclEnableDma ='true') ..... <a:tst expr="(../../MclGeneral//MclDma/MclEnableDma ='true') Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: express is MclGeneral//MclDma Expected behavior: express is MclGeneral/MclDma Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-14495	Bug	 [CAN] ecvd/Ip_FlexCAN fails to export data for multiple controllers<*> Detailed description (how to reproduce it): A*> add more than one controllers to s32k148/Ip_FlexCAN (IPL layer) projects with default configuration (fix all errors if have) export ecvd import ecvd => error as below:

ID	Subtype	Headline and Description
		!image-2021-07-30-10-51-10-710.png! B*> !image-2021-07-30-10-56-02-840.png! C>* **_ please re-check if all required nodes are exported (e.g. pe_clock_frequency) !image-2021-07-30-11-05-31-694.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14535	New	 New Feature [port] Update pin signal configuration resources for S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14503	New	 New Feature [crypto] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https://nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14507	New	

ID	Subtype	Headline and Description
		New Feature [fls] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14508	New	New Feature [gpt] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14509	New	New Feature [i2c] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14511	New	New Feature

ID	Subtype	Headline and Description
		[icu] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14515	New	New Feature [ocu] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14517	New	New Feature [port] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14521	New	New Feature [sent] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription:

ID	Subtype	Headline and Description
		Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14522	New	 New Feature [spi] Update resources via RM S32K3xx Rev. 2 Draft D ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14534	Bug	 [S32K3XX] [PORT] Driver missing config IFE bit when declare Port_Init<*> Detailed description (how to reproduce it): in S32K3XX, use Plugin_2872021.zip, config channel (only PTA5) with IFE = 1, check the status IFE bit in MSCR = 5 Preconditions: Port_Init need to support config all bit in MSCR if have Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0015 Observed behavior: Port_Init did not have any action to config IFE bit !image-2021-07-30-13-52-25-522.png! Expected behavior: Driver need to be update config for IFE bit in MSCR Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14587	Bug	 [S32K3XX] [RM] Correct API prototypes to match the requirements<*> Detailed description (how to reproduce it): There are some wrong interfaces between requirement and driver. Detail in attachment file.

ID	Subtype	Headline and Description
		Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: different APIs prototype between driver and requirement Expected behavior: No different APIs Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update Driver or/and requirement
ARTD-14615	Bug	[PWM] Stuck in interrupt function when re-enable notification for Flexio<*> Detailed description (how to reproduce it): When re-enable notification for channel flexio is 0 and 1, the stuck occurs in the interrupt function: Initilize 2 channels flexio 0 and 1 Loop for enable notification 2 channels. timerIrqMask variable will be set to 3(0x11) when re-enable notification for channel 0 timerIrqMask = timerIrqMask & ((uint8)0x01U << userCfg->timerId) in Flexio_Pwm_Ip_UpdateInterruptMode function will set timerIrqMask to 2(0x10)-> value 0 for channel 0. But interrupt still occur, it causes the program to get stuck in the interrupt function Preconditions: Build with GCC compiler Test Case ID (internal TC that caught the defect) optional: Pwm_TC_FCT_0213 Flexio Observed behavior: get stuck in the interrupt function Expected behavior: No stuck in the interrupt function Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14664	Bug	[S32K3XX] [PORT] Driver generate error due to missing define INMUX in S32K312<*> Detailed description (how to reproduce it): in PVT_ARTD_PORT_V146, config test in derivative S32K312. Preconditions: driver will be support generate configuration successfully Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0036/Port_TS_016 Observed behavior: driver for K312 can support till INMUX= 372 ==> ok !image-2021-08-03-10-30-51-332.png! But Port_PBcfg.c still declare to INMUX373 !image-2021-08-03-10-32-43-534.png! ==>make error !image-2021-08-03-10-29-37-452.png! Expected behavior: driver need to be update to generate config successfully in S32K312

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14680	Bug	[LIN][BASE] - Update name of Ds component for Lin<*> Detailed description (how to reproduce it): The actual component name for Lin is Lin_43. It should be updated to Lin. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: HLD component should be named Lin. Not Lin_43. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In base driver we should update for S32K1 platform from Lin_43 to Lin in the modules.h file. For Lin driver the makefile, the sdk_manifest the generation files should be updated in order to change the name for Lin component in Lin
ARTD-14681	Bug	[GPT] GptChannelTickFrequency need auto calculate by the prescaler and McuClockReferencePointFrequency<*> Detailed description (how to reproduce it): GptChannelTickFrequency can not calculate correct the frequency if have 2 instance of ipv (like FTM STM Emios) Preconditions: always get the prescaler of the 1st instance of the list. Test Case ID (internal TC that caught the defect) optional: GPT_TS_001 Observed behavior: GptChannelTickFrequency incorrect Expected behavior: Auto calculate the GptChannelTickFrequency by the prescaler and the mcu reference Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: need correct the node GptChannelTickFrequency to calculate the frequency
ARTD-14677	Bug	[Platform] Build failed at IntCtrl_Ip on S32K324<*> e:/Zebra/ARTD_S32K3_NOSASW/output/S32K3XX_S32K324_gcc/mcl/../../eclipse/plugins/Platform_TS_T40D34M9I0R0/src/IntCtrl_Ip.c: In function 'IntCtrl_Ip_GenerateDirectedCpuInterruptPrivileged': e:/Zebra/ARTD_S32K3_NOSASW/output/S32K3XX_S32K324_gcc/mcl/../../eclipse/plugins/Platform_TS_T40D34M9I0R0/src/IntCtrl_Ip.c:534:17: error: 'MSCM_IRCPnIRx' undeclared (first use in this function); did you mean 'MSCM_IRCPnIRx_Type'? 534 MSCM_IRCPnIRx->IRCPnIRx[core][irqId].IGR = 0x1U; MSCM_IRCPnIRx_Type

ID	Subtype	Headline and Description
ARTD-14679	Bug	[ADC] mismatch EB and S32CT when comparing code generation<*> Detailed description (how to reproduce it): There is some information that does not match EB and S32CT when comparing code generation. Generating the following devtest can reproduce the issue TS009 cfg2 with Dma configuration TS001 PC configuration to be fixed under ARTD-14726 from Ecuc Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing code generation. Expected behavior: EB and S32CT codegen must be indentical Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14684	Bug	[FLS] the SPTRCLR need clear after the driver sets BFGENCR to the appropiate LUT index<*> Detailed description (how to reproduce it): The default LUT id for AHB reads is zero as BFGENCR reset value is 0 (actually this is why LUT[0] has a reset value 0818_0403h, 2400_1C08h since its a "common" read sequence for most flash chips). In the Fls module, the QSPI_IP_AHB_LUT is defined as 1, and while the driver sets BFGENCR to the appropriate LUT index, it forgets to follow the RM recommendation: If the sequence pointer differs in the new and the previous sequences, you should reset it. See sequence pointer clear register for more information. This means that the driver should W1C into SPTRCLR.BFPTRC for the peripheral to operate correctly. the customer was having issues because of this, in their environment instead of implementing this, they exchanged QSPI_IP_AHB_LUT and QSPI_IP_COMMAND_LUT so QSPI_IP_AHB_LUT stays at 0. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: N/A Expected behavior: The the sequence pointers must be cleared in the initialization phase. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-14687	New	New Feature [CRC][Optimize] Update bit reversal using tables ,,"NewWorkDescription:

ID	Subtype	Headline and Description
		The CRC driver needs optimizations for bit reversal and table/software calculation. Proposed solution optional: 1. Update bit reversal using tables."
ARTD-14703	Bug	[ADC] Adc_Ipw_MapCTUTriggerIndex has invalid trigger index of trigger source array<*> Detailed description (how to reproduce it): When control mode is enabled, Adc_Ipw_MapCTUTriggerIndex might not query all members of array or point to out of range of array if number of hwtrigger is not equal to number of trigger in control mode The Adc_EnableCTUTrigger function is intended for trigger mode but Adc_Ipw_MapCTUTriggerIndex wrapping between trigger mode and control mode. This seems confusing users When supporting trigger mode, it points to AdcConfigSet/AdcHwTrigger }} but this array also contains trigger source directly to ADC not via BCTU/CTU while the name of function is Enable CTU trigger? Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: compile error Expected behavior: compiler no error Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-14702	Bug	[S32K3XX] [PORT] Do not have any notification when config unavailable channel in S32K312<*> Detailed description (how to reproduce it): 1. with tag BLN_PORT_060, config test Port_TS_015 in S32K312, try to config channel PTA23 (not available in S32K312 Q172) 2. Cannot choose mode for channel Preconditions: if config not available channel, EB need to shown error about this driver need to support all available mode of channel Test Case ID (internal TC that caught the defect) optional: Port_TC_WBT_0010/Port_TS_015 Observed behavior: don't have any warning or error about this issue: !image-2021-08-04-17-23-26-354.png! don't see any mode: !image-2021-08-05-10-59-42-134.png! Expected behavior: driver need to be update to fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14726	New	New Feature

ID	Subtype	Headline and Description
		[EcuC] Add requiresIndex to EcucPartition ,,"Detailed description (how to reproduce it): ADC get the list Partition from EcucPartitionCollection/EcucPartition array. When importing epc output from Ecuc of EB tresos to S32DS S32DS import the partition order following ""Name"" field but the order in EB following ""index"" column. this makes ADC has different in generated code bw Eb and CT !image-2021-08-05-14-46-19-370.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: ADC_TS_001 DevTest Observed behavior: [...] Expected behavior: generated code is indentical Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Use <REQUIRES-INDEX> attribute as the post in team [https://teams.microsoft.com/dl/launcher/launcher.html?url=%2F_%23%2Fl%2Fmessage%2F19%3Ae451c595d3ba410c8f9c1f5efc19a8a3%40thread.tacv2%2F1618569101137%3FtenantId%3D686ea1d3-bc2b-4c6f-a92c-d99c5c301635%26groupId%3Df9decd68-7b74-4101-a4d2-ad54e86f727f%26parentMessageId%3D1618569101137%26teamName%3DZebra%26channelName%3DConfiguration%2520(code%252C%2520DS%252C%2520EB%252C%2520etc)%26createdTime%3D1618569101137&type=message&deeplinkId=7af9cc4b-4bf4-4f14-8e9c-c1a7f75cf125&directDl=true&msLaunch=true&enableMobilePage=true&suppressPrompt=true]"
ARTD-14734	Bug	[CRYPTO] Remove unsupported key types from the NVM and RAM key catalogs<*> Detailed description (how to reproduce it): HSE_KEY_TYPE_SHARED_SECRET key group can only be used for RAM key catalog HSE_KEY_TYPE_RSA_PAIR key group can only be used for NVM key catalog. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Can configure select SHARED_SECRET from NVM key catalog Can configure select SHARED_SECRET from NVM key catalog Expected behavior: Remove SHARED_SECRET from NVM key catalog Remove RSA_PAIR from RAM key catalog Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14750	Bug	[RM] Missing validate in configuration MPU M7<*> Detailed description (how to reproduce it): Missing validate in configuration MPU M7 => Missing define variable "Mpu_M7_Config" => Build fail

ID	Subtype	Headline and Description
		Preconditions: Node "RM Enable MPU_M7 Support " is ON. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: variable "Mpu_M7_Config" is called but hasn't been define. Expected behavior: Define variable "Mpu_M7_Config" if using "RM Enable MPU_M7 Support " Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14756	Bug	 [S32K3XX] [PORT] Port_SetPinMode affected to PKE value in MSCR<*> Detailed description (how to reproduce it): use tag PVT_ARTD_PORT_V150, config PKE enable in channel with MSCR = 80, check PKE bit after declare Port_SetPinMode to INOUT MODE 1 Preconditions: Port_SetPinMode just config mode (SSS value), not affect to PKE bit Test Case ID (internal TC that caught the defect) optional: Port_TS_005/Port_TC_WBT_0015 Observed behavior: Port_SetPinMode affect to PKE bit, 0x80001 was turn off PKE bit !image-2021-08-06-16-44-11-991.png! Expected behavior: Driver need to be update to fix this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14757	Bug	 [SPI] Different in SpiFlexioEnable node location between EB and CT<*> Detailed description (how to reproduce it): In EB, the SpiFlexioEnable is located in SpiAutosarExt container but in CT it is SpiGeneral. Must be synchronous between them Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: SpiFlexioEnable is in different container in EB and HLD CT Expected behavior: in same container Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Synchronous them
ARTD-14824	New	 New Feature [FEE] Add support for bad Sector Management and Sector Retirement (part 3) ,,"NewWorkDescription:

ID	Subtype	Headline and Description
		Add support for bad Sector Management and Sector Retirement (CPR_RTD_00505.fee). This involves removing Sectors from configuration when they become unusable. Rationale: some flash memory specs have low endurance/write cycles availability, which needs to be improved by the ability to retire bad sectors or locations affected by permanent ECC, at the expense of allocated flash size the endurance being a ppm specification."" Requirement source: cPRD (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: # Update CT part # Update User manual to introduce the feature"
ARTD-14835	Bug	 [S32K3XX][PORT] Build fail on S32K312 due to Tspc_Port_Ip_Types.h include wrong file<*> Detailed description (how to reproduce it): When build wiring test for dio on S32K312, Tspc_Port_Ip_Types.h still include S32K344_TSPC.h => build fail !image-2021-08-09-17-02-36-007.png! !image-2021-08-09-17-03-36-352.png! Preconditions: Plugin from PVT_ARTD_PORT_V150 Test Case ID (internal TC that caught the defect) optional: Dio_TC_WIR_00100 Dio_TC_WIR_00201 Observed behavior: Build fail dio wiring test on S32K312 (using port module) Expected behavior: ext test build pass on S32K312 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-14836	Bug	 [BASE] OsIf_GetCoreID function always returns 0 with CORE_SETS is 1<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Crc_TC_FCT_0721 Observed behavior: OsIf_GetCoreID function always returns 0 with CORE_SETS is 1 because OSIF_ENABLE_MULTICORE_SUPPORT macro is only enabled in base module !image-2021-08-09-16-57-38-072.png|thumbnail! Expected behavior: Update driver code to return 1 when CORE_SETS is 1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-14852	New	 New Feature

ID	Subtype	Headline and Description
		[RM][S32K3XX] Improve for XBIC Ip ,,"NewWorkDescription: Create interface. Update function's name follow requirement improve code better update code for user mode support part Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: update follow description"
ARTD-14861	Bug	[Platform][S32K3xx_RTM1.0.0] Build Failed on IAR with "Relocation failed" ,,"Detailed description (how to reproduce it): During build test either IAR8.40 or IAR8.50.1.0, got this log : Error[Lp002]: relocation failed: value out of range or illegal: 0xffff'ffff'ffff'd882 Kind : R_ARM_THM_JUMP11[0x66] Location: 0x40'49d6 ""SVC_Handler"" 0xe Module: e:\workspace\RTD_K3_RTM100\output\S32K3XX_S32K344_iar\fls \Fls_TS_000_cfgCORE0\out\exceptions_c.o Section: 8 (.mcal_text) Offset: 0xe Target : 0x40'225d ""SVCHandler_main"" Module: e:\workspace\RTD_K3_RTM100\output\S32K3XX_S32K344_iar\fls \Fls_TS_000_cfgCORE0\out\exceptions_c.o Section: 14 (.mcal_text) Offset: 0x1 Aslo, build failed existing when build on GCC_10.2 , please see the below log file attached . Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Build Failed Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14858	Bug	[S32K3XX] [PORT] Driver generate incorrect value OBE index when TSPC configuration<*> Detailed description (how to reproduce it): with tag BLN_PORT_063, port driver was generate incorrect OBE index of pins config TSPC enable Preconditions: Pins config TSPC enable need to have correct value in obe index Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Port_TC_WBT_0024/Port_TS_007 Observed behavior: in generate TSPC of pins config: !image-2021-08-10-10-33-18-264.png! if value = 65535 (or 0xFFFF), the condition never was occur==> never enable OBE index for config pins: !image-2021-08-10-10-34-46-233.png! Expected behavior: Driver need to be update generate file of pins which was config TSPC enable Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-14859	New	 New Feature [RM] Review and update VIRT_WRAPPER IP ,,Review and update VIRT WRAPPER IP
ARTD-14862	Bug	 [SPI] Add condition related to must enable pin configuration for Flexio on CT<*> Detailed description (how to reproduce it): Now, CT tool does not raise any an error if not configure for spi pins of flexio Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: No error is raised to notification for user Expected behavior: An error if pins is not configured Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Add an constraint on CT template file
ARTD-14897	Bug	 [Mcl] Static_Dma_Ip_SetLogicChannelScatterGatherInit: can not return DMA_IP_STATUS_WRONG_CONFIG<*> Detailed description (how to reproduce it): Use config scatter/gather config and try to return DMA_IP_STATUS_WRONG_CONFIG but EB and CT just only support max is 256 scatter/gather > Can't config more than 256 So can not create test script for return case DMA_IP_STATUS_WRONG_CONFIG Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Function: Static_Dma_Ip_SetLogicChannelScatterGatherInit !image-2021-08-10-18-08-25-330.png! Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-14898	New	New Feature [pinTool] supports parsing TSPC information in pin signal configuration generation ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: S32K3xx Reference Manual, Rev. 2 Draft D, 07/2021, [Link|https:// nxp1.sharepoint.com/:b:/r/sites/Zebra/Shared%20Documents/Documents/Platforms/ S32K3xx/RM/S32K3xx_RM_Rev2DraftD.pdf?csf=1&web=1&e=6kLAfr] Proposed solution optional: Update driver resources"
ARTD-14899	Bug	[ADC] Adc_Sar_Init should disable channels/features if not enabled/configured<*> There are some features/channels that are considered as disabled in generated configuration but when calling Adc_Sar_Init function, it does not disable these ones on hardware and keep them as default or previous state Proposal to disable them if not used
ARTD-14978	New	New Feature [ADC] Remove per Group indexation of pResultsBufferPtr ,,"NewWorkDescription: Remove per Group indexation of pResultsBufferPtr, because it is part of Adc_GroupConfigurationType, so can already be accessed per group: Adc_pCfgPtr[u32CoreId]->pGroups[GroupIndex].pResultsBufferPtr[Group] "
ARTD-15056	Bug	S32K3 CT Pins ID Length Issue<*> Detailed description (how to reproduce it): If the PIN ID in the configuration tool is set with a long string, the generated pin name MACRO might be with error in "Siul2_Port_Ip_Cfg.h". Please see attached figure for an example. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Proposed solution optional: Either limit the pin ID length or change the generated MACRO in header file.
ARTD-15057	Bug	[Base] ADC_AMSIO bit is in correct in ADC Header<*>

ID	Subtype	Headline and Description
		The latest RM Rev2 DraftD chapter 57.5.2.66 Analog Miscellaneous In/Out register (AMSIO) AMSIO_HSEN has 2 bit but current header file show only 1 bit #define ADC_AMSIO_HSEN_MASK (0x20000U) #define ADC_AMSIO_HSEN_SHIFT (17U) #define ADC_AMSIO_HSEN_WIDTH (1U) It must be: #define ADC_AMSIO_HSEN_MASK (0x60000U) #define ADC_AMSIO_HSEN_SHIFT (17U) #define ADC_AMSIO_HSEN_WIDTH (2U) This is document issue. Please refer to attachment if needed !image-2021-08-11-15-31-59-192.png!
ARTD-15059	Bug	[RM] Missing validate in configurating PFlash<*> Detailed description (how to reproduce it): Missing configuration "PflashMasterProtection_0" =>Define array " Pflash_Config_VS_0[0]" with size = 0 => Build Fail => Build fail Preconditions: Node "RM Enable Plfash Support" ON. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15062	Bug	[LIN] Features Lin Frame Timeout Disable only applied with case node is slave.<*> Detailed description (how to reproduce it): About features Lin Frame Timeout Disable, Now driver only applied with case node is slave, lacking with case node is master for LPUART Driver don't need to checking timer out when master node transmits header frame for FLEXIO Preconditions: !image-2021-08-11-17-17-53-703.png! Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_0019 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15070	Bug	ICU: The header file included for derivative 312 is not correct for IPs used<*> Detailed description (how to reproduce it): Header file included for derivative 312 is the one for 344.

ID	Subtype	Headline and Description
		!image-2021-08-11-16-59-53-745.png|width=369,height=98! !image-2021-08-11-17-00-18-696.png|width=418,height=111! !image-2021-08-11-17-00-53-075.png! Preconditions: use 312 derivative for EBT test or DS example Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Incorrect derivative header file used Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15076	Bug	[S32K312] [PORT] Driver was generated redundant unavailable pins<*> Detailed description (how to reproduce it): execute tag: BLN_PORT_064, run test internal test port, over the Port_Init function Preconditions: Port_Init will be config all used pins and unused pins of derivative, which was available in IOMUX for K312 Test Case ID (internal TC that caught the defect) optional: Port_TS_006/Port_TC_WBT_0018 Observed behavior: The pin 148 was generate unavailable but still write GPDO==> hard fault when execute Port_Init !image-2021-08-12-10-24-49-156.png! !image-2021-08-12-10-26-53-760.png! Expected behavior: Driver need to be update unused pin available according IOMUX Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15082	Bug	[I2c] Fix driver build fail on S32K312<*> Detailed description (how to reproduce it): [...] !image-2021-08-12-11-40-42-244.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15088	New	New Feature

ID	Subtype	Headline and Description
		[S32K3xx] add dummy value into some fields of Port resources ,,"NewWorkDescription: Add one dummy value into the following resources of Port for CT using: Port.Siul2InstanceMscrIdxStart Port.Siul2InstanceMscrIdxEnd Port.Siul2MaxNumConfiguredMscrs Port.Num16PinsBlocks Requirement source: Development (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15115	Bug	[S32K3][SPI] Build fail relate to include S32K324_[IPV].h<*> Detailed description (how to reproduce it): When use resource S32K324 to build test, Flexio_Spi_Ip_Cfg.h and Lpspi_Ip_Cfg.h are including S32K324_FLEXIO.h and S32K324_LPSPI.h. But both of headers don't exist in base/header. Currently, base/header includes S32K344 and S32K312 only. Preconditions: Using resource S32K324 Test Case ID (internal TC that caught the defect) optional: Spi_TS_009 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15101	New	New Feature [icu] Create dev tests to be run on the target ,," NewWorkDescription: Create functional development tests that can be run on the target and that test the main functionality of the driver. The purpose of the development tests is to validate that the driver does not have S1 and S2 bugs. The dev tests will be executed on remote setups from Bamboo when running the EXECUTE CI option from ManifestValidator*, when applying a new TAG in the manifest. Implementation Notes The tests should be designed in a way such that no external hardware is required. Use as much as possible the features of the boards that we have available, by using internal loopback or connecting pins to each other on the same board*. The intent is to have one identical setup for all the drivers that can run the development tests, triggered from Bamboo. Also, this will make it easier to duplicate the setup for debugging, without keeping the board used by Bamboo busy. For that, update the wiring information in the shared document ([https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared%20Documents/Testing/Dev_tests/DevTests_Wiring.xlsx?d=we0b72309cbad4044960d6c095a90de5c&csf=1&web=1&e=CLWKeW)|

ID	Subtype	Headline and Description
		https://nxp1.sharepoint.com/:x:/r/sites/Zebra/Shared %20Documents/Testing/Dev_tests/DevTests_Wiring.xlsx? d=we0b72309cbad4044960d6c095a90de5c&csf=1&web=1&e=CLWKeW]. Group test cases in test suites. Define different test suites when a different configuration is needed (either for your driver or for dependencies). Tests with multiple configurations (M4 tags in configuration) are allowed and can be used for variating certain configuration options, when needed. If possible, reusing the shared configuration, the test used for static analysis, or parts of the examples is encouraged as it will reduce maintenance effort. However, if this is not possible, it is not mandatory to reuse configurations or code. The wiring used for examples should be the same as for the development tests. Exceptions will be discussed, but the intent is to have the same hardware setup for both dev tests and examples. Before closing this activity you should: # Update the wiring information here: [https://nxp1.sharepoint.com/:x:/r/sites/ Zebra/Shared%20Documents/Testing/Dev_tests/DevTests_Wiring.xlsx? d=we0b72309cbad4044960d6c095a90de5c&csf=1&web=1&e=CLWKeW] # Inform the PE team, or a person in RTD with admin privileges on the Bamboo plans to update the list of development tests to be run on the hardware # Test the development tests, first by using the remote hardware setups, then by using the Bamboo custom builds or even the manifest validator Extra notes The remote run support from beart is used for running the tests from Bamboo on the boards. Running the tests on the board is a skippable step, as for now we have no support for pre-silicon run (like running on the simulator) from Bamboo. This activity will be started on K3, as a pilot. For the rest of the platforms, the ""_*Development tests and execution*_"" ticket raised by the PM will be used for porting these tests. Wiki for dev tests: [https://confluence.sw.nxp.com/display/AUTORD/Development+test] (Work In Progress, any input is appreciated) Requirement source: G0 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: See description"
ARTD-15128	New	 New Feature [S32K3XX][PORT] Separate the functions in IP layer ,,"NewWorkDescription: There are some functions in IP layer which do not represent for any requirements in IP layer. They are used for HLD. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Move these functions to IPW "
ARTD-15133	Bug	 [RM] Wrong generation code for MPU M7 IP<*> Detailed description (how to reproduce it): Wrong generation code for MPU_M7's Region config Preconditions: [...] Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		[...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15136	Bug	[S32K3xx][RTM100][Port] DSE fields are not available for some pins<*> Detailed description (how to reproduce it): Use the newest tag of PORT (PVT_ARTD_PORT_V152) to generate plugins. Open tresos and use resource s32k314_mapbga257 in Resource module then open Port module. Add some mscr pins whose DSE's field are available mentioned in K344_ioMux (23, 114, 156, 158, 164, 167, 168, 174, 180, 181, 185, 188, 189, 191, 198, 199, 200, 205, 207, 208, 209, 210, 211, 212, 213, 214, 215, 216, 217, 218, 219) Observed behavior: DSE's field of those pins are not available to configurate !image-2021-08-13-12-03-38-672.png|width=536,height=350! Expected behavior: Those pins' DSE field must be configurable according to IOMux Proposed solution optional: It looks like that the resource mentioned in Port drivers excluded those pin mscr number so that the drivers does not let users configurate DSE's field. !image-2021-08-13-12-08-01-921.png|width=1411,height=741!
ARTD-15148	Bug	[BASE] Some wizard data files are missing the copyright header<*> Detailed description (how to reproduce it): At least Clock_Ip_Cfg_Defines.h, Clock_Ip_Cfg_Defines.c, Clock_Ip_PBcfg.c, Clock_Ip_PBcfg.h, Clock_Ip_Cfg.c, Clock_Ip_Cfg.h, Siul2_Port_Ip_Cfg.c, Siul2_Port_Ip_Cfg.h are missing the comment header block including the copyright Preconditions: None Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Missing copyright Expected behavior: Comment header block should be there Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Review the files in Base and add the comment header block
ARTD-15151	Bug	[Uart] Update code follow new changes of requirement<*> Detailed description (how to reproduce it): Update code follow req changes on ticket: https://jira.sw.nxp.com/browse/AAI-907 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		[...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15155	Bug	[S32K3][SPI] Issue with Spi_Ipw_au8LpspiHWUnitMapping array<*> Detailed description (how to reproduce it): In the function Spi_Ipw_Init, we use Spi_Ipw_au8LpspiHWUnitMapping to allocate HWUnitId which is compatible with HWUnit->Instance: !image-2021-08-13-17-16-12-567.png|width=450,height=89! But size Spi_Ipw_au8LpspiHWUnitMapping (LPSPI_IP_NUMBER_OF_INSTANCES) is the number of configured LPSPI instance: static Lpspi_Ip_StateStructureType Lpspi_Ip_axStateStructure[LPSPI_IP_NUMBER_OF_INSTANCES]; !image-2021-08-13-17-19-26-295.png|width=475,height=174! This causes: when we configure 2 instances (LPSPI0, LPSPI2), we can't allocate HWUnitId of LPSPI2. Because Spi_Ipw_au8LpspiHWUnitMapping's size is 2 (_LPSPI_IP_NUMBER_OF_INSTANCES = 2) and it needs the 3rd element for LPSPI2 (HWUnit->Instance = 2) Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Spi_TS_003 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15144	Bug	[ADC] ADC group INTERRUPT contains only one channel cannot be converted, in case both INTERRUPT and DMA method are used in ADC HW Unit ,,"Detailed description (how to reproduce it): When ADC_DMA_SUPPORTED parameter is configured as TRUE and configure at least one group uses INTERURPT and one group uses DMA method, then a conversion is started for a group using INTERRUPT me that contains only 1 channel, the system crashes although that specific group is not configured for a HW Unit that uses DMA as transfer type. Preconditions: ADC_DMA_SUPPORTED parameter is configured as TRUE. Create two HW instance, one uses INTERRUPT (e.g. HwUnit_0) and one uses DMA (e.g. HwUnit_1). Configure one group (e.g. Adc0Group0) with only one channel in HwUnit_0 and one group in HwUnit_1 (e.g. Adc1Group0). Start group conversion with Adc0Group0 Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior:

ID	Subtype	Headline and Description
		After finished conversion for Adc0Group0 (the group uses INTERRUPT method and contains only one channel), the code hit ISR then jumped to Adc_Ipw_UpdateGroupState(). When executing this piece of code: !dma_adc.jpg|width=743,height=230! the system was crashed. Expected behavior: In case both INTERRUPT and DMA are considered for ADC group conversion, the conversion for group uses INTERRUPT method and only contains one channel shall be successful, without any system crashed. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15156	New	 New Feature [ICU][S32K3XX] Error for callback in timestamp mode ,,"In timestamp mode, the function Icu_ReportEvents is used for overflow notification but it is also calling the function Timestamp1_Notification : !image-2021-08-13-17-55-40-559.png! In the init function for emios, the notification enable variable is turned, so the callback function is always called when not calling the function notification to enable first. !image-2021-08-13-18-01-57-071.png! And the master bus A is initialized into internal bus as due to this value : !image-2021-08-13-18-03-51-099.png! !image-2021-08-13-18-04-36-038.png! "
ARTD-15275	New	 New Feature [icu] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx %5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx %5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FDS]

ID	Subtype	Headline and Description
		Proposed solution optional: Update driver resources"
ARTD-15283	New	New Feature [rm] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx %5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx %5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FDS] Proposed solution optional: Update driver resources"
ARTD-15286	New	New Feature [spi] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: DS: update baudrate configuration follow 12.1.1 LPSPI section: S32K314, S32K324, S32K344, S32K322, and S32K342 supports data rate up to 20 Mbps, S32K312 and S32K311 supports data rate up to 15 Mbps. Only one LPSPI instance support 20 MHz in loopback mode that is LPSPI0 All LPSPIs supports a minimum a 10 MHz data rate on standard plus pads and 7.5 MHz on standard pads. Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx %5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?

ID	Subtype	Headline and Description
		originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx %5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FDS] Proposed solution optional: the range of baudrate will be handle by some variables in resource files to be compatible with each instance"
ARTD-15287	New	 New Feature [uart] Update resources via RM S32K3xx Rev2 ,,"NewWorkDescription: Update resource for your driver following below derivatives for this release: S32K312: S32K312_172MQFP, S32K312_100MQFP S32K314: S32K314_257MAPBGA, S32K314_172MQFP S32K324: S32K324_257MAPBGA, S32K324_172MQFP S32K344: S32K344_257MAPBGA, S32K344_172MQFP Requirement source: Reference Manual|S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx %5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FRM] Datasheet|S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https:// nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx? originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3 %5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared %20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx %5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents %2FDocuments%2FPlatforms%2FS32K3xx%2FDS] Proposed solution optional: Update driver resources"
ARTD-15216	Bug	 [CAN] EB/S32CT comparation fail at can_ts_1455<*> Detailed description (how to reproduce it): build/run can_ts_1455 for EB and S32CT / s32k344 can_ts_1455 fail with S32CT Please look at attached output for analysis Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: CAN_TC_FCT_14550 Observed behavior: difference between generated code of two tools Expected behavior: same generated code between s32ct and EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: N/A
ARTD-15217	New	 New Feature [S32K3xx] Dio add support Virtual Wrapper into Dio HLD CT ,,"NewWorkDescription: Virtual wrapper has been supported on EB tresos from release K3 beta, but it's not available on S32CT > Add Virtual Wrapper functionality into Dio HLD CT The changes included: update code generation for Virtual Wrapper update configuration and node validation for Virtual Wrapper Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15219	Bug	 [ICU] The ICU of eMIOS will get wrong Signal Measurement if bus counter is used.<*> Detailed description (how to reproduce it): In Emios_Icu_Ip_Irq.c, there are two static functions which cannot work as expected and lead to wrong Signal Measurement result when bus counter is used. static inline uint32 Emios_Icu_Ip_GetChannelClockMode*(): !image-2021-08-16-09-22-26-072.png! The OR operation should be AND operation to get the right channel clock mode. static inline uint32 Emios_Icu_Ip_ReadCounterBus*() This function is used to get the period of bus counter. When Bus Diverse, Bus A or Bus F is selected, this function will get channel clock mode first (mentioned above) and then check whether it is equal to EMIOS_ICU_MCB_INT_CLOCK_U32 or not. Just take case Bus F as an example: !image-2021-08-16-09-45-37-474.png! In this process, there are two wrong points: # The clock mode is wrong as mentioned above. # The u32Period will be wrong if the clock mode is not equal to* EMIOS_ICU_MCB_INT_CLOCK_U32 because there is no any bus counter mode which uses Register B as period register (refer to RM 59.5.3.14 and 59.5.3.15). As a consequence, the ICU of eMIOS will get wrong Signal Measurement result if bus counter is used. Preconditions: This issue will happen only when IcuEmiosBusSelect is set to Bus A, Bus F or Bus Diverse. !image-2021-08-16-10-57-28-438.png! Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15226	Bug	 [Spi] No error raise when SpiMaxDmaFastTransfert not enable and Dma Fast transfer support<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): To support Dma Fast transfer, SpiPhyUnit is used by External Device in Job must has SpiMaxDmaFastTransfer enabled. Preconditions: SpiEnableDmaFastTransfer is True SpiEnableDmaFastTransferSupport is True SpiGlobalDmaEnable is True Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Raise an error
ARTD-15229	New	New Feature [RM][S32K3XX] Improve XRDC driver code related to PID ,,"NewWorkDescription: Update master cores which are available for PID. Use of PIDm[PID] can be aborted if a core already had a built-in PID register (indicated in HWCFG2 register) Fix build warning in S32DS Requirement source: (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-15220	New	New Feature [S32K3XX][DIO] The Exclusive Areas should be reviewed and updated ,,"NewWorkDescription: The Exclusive Areas for K3 platform are incorrect. Some of them are redundant (need to be removed), and the rest need to be renamed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove/Add/Renaming the Exclusive Areas in code for K1. From IPW to IPL. All exclusives should be existed in IPL. The ones in IPW should be removed. #include SchM_Dio.h should be moved from IPW to IPL Update the UM/IM if needed Check and update RTE if needed"
ARTD-15227	New	New Feature [RM] [S32K3] Fix build fail on S32DS ,,"NewWorkDescription: Build fail on DS as below: !image-2021-08-16-10-48-10-464.png! Requirement source:

ID	Subtype	Headline and Description
		NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Correct generated files"
ARTD-15295	Bug	 [WDG] Incorrect generated code between Instances<*> Detailed description (how to reproduce it): I compared generated code between instance and saw some incorrect generated value. I note in excel file in the attachment. Please review it and update generated code. If there are any nodes that you will not update, please comment the reason why. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Incorrect generated code between instances. Please see attach files to more details. Expected behavior: Correct generated code. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15296	Bug	 S32K3 Port Configuration<*> In the SPI example, the port (SIUL2) is initialized by baremetal code, not by Port_Init(). Is there any limitation in using Port ? I tried to configure a different SPI example, but found that the port is not set as I desired. For example, I set PTE1 (MSCR129) as LPSPI0_SCK. The MSCR_SSS value for this port (MSCR129) is 2. It's no problem But the MSCR_OBE should be 1. I can see in the generated code that MSCR129 value is 2 instead of 0x00200002. So when I run the code, I found that MSCR129 is set to LPSPI0_SCK output but the MSCR_OBE bit is 0. So the SPI cannot run properly. Could you please advise what might be wrong or missing in my PORT settings?
ARTD-15301	Bug	 [S32K3XX][S32K3XX_100] Initialization handler interrupt fail by Platform InstallIrqHandler function<*> Detailed description (how to reproduce it): Installing interrupt handler by Platform_Init funcition or Platform_InstallIrqHandler funcition and Enable interrupt, after that generate interrupt trigger. The driver can't into interrupt handler. Maybe handler funciton initaization failed. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: N/A Expected behavior: The diver install handler funcition successful Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: N/A
ARTD-15306	Bug	[RM] Wrong syntax when call function Mpu_M7_Ip_Deinit_Privileged()<*> Detailed description (how to reproduce it): Missing () when call function Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix syntax call function
ARTD-15307	Bug	[S32K3XX] Failure at building on S32K312 with GHS, GCC compilers ,,"Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Failure at building on S32K312 with GHS, GCC compilers because ram overflow(http://ceram.ea.freescale.net/1/project/ar_int_crc_ghs/details) Expected behavior: Build success on S32K312 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-15311	Bug	[WDG] Findings need to fix follow to Code Checklist Review<*> Detailed description (how to reproduce it): Something didn't follow to coding rule (checklist in ticket: https://jira.sw.nxp.com/browse/ARTD-9123) Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Need to fix

ID	Subtype	Headline and Description
ARTD-15312	Bug	[SAI] Fix code review and UML review check list items failed<*> Detailed description (how to reproduce it): Fix code review and UML review check list items failed Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15313	New	New Feature [BASE] Update header files for S32K344 corresponding RM rev 2 ,,"NewWorkDescription: Update header files for S32K344 corresponding RM rev 2 Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15318	Bug	[BASE] Templating engine does not correctly report Java exceptions<*> Detailed description (how to reproduce it): 1. Make the setup from UCT-4375 2. The error message is undefined As we analyzed it, this is from a bug in templatingengine.js file. !image-2021-08-16-17-38-59-868.png! error.stack doesn't exist. error variable is from class *IllegalFormatConversionException, so you can use the next variant: scriptApi.logError(error);* ** (the result will be like in next print) !image-2021-08-16-17-38-23-705.png!
ARTD-15325	Bug	[S32K3XX][S32K3XX_100] The project build fail by some base pointer incorrect<*> Detailed description (how to reproduce it): Create test for platform module, add platform, base to project, clean generate, parse build, some base pointer is incorrect Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: !image-2021-08-17-09-52-15-708.png! Expected behavior:

ID	Subtype	Headline and Description
		Modifier base pointer Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-15329	Bug	 [CRYPTO] EB Tresos doesn't raise error when CryptoKeyElementRefs are duplicated<*> Detailed description (how to reproduce it): In CryptoKeyType category , CryptoKeyElementRef column selects 2 same Refs But EB Tresos dosen't raise any error when CryptoKeyElementRefs are duplicated Preconditions: tag CRYPTO_078 Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: CryptoKeyElementRefs can be duplicated and not raise any error Expected behavior: [EB Tresos raises an error "*A reference to a CryptoKeyElement with the same CryptoKeyElementId already exists in the reference list "when CryptoKeyElementRefs are duplicated Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15337	Bug	 [S32K312] I3C clock is not enabled on AIPS_0<*> Detailed description (how to reproduce it): [...] Run I3C test on K312 board Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] I3C clock is not enabled in sys_init function. Expected behavior: [...] I3C clock is enabled in sys_init function. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] Change value of PRTN0_COFB1_CLKEN_REQ_MASK_U32 to 0x000137DFU
ARTD-15393	New	 New Feature [S32K3XX][FLS] Update code after performing review Code_Review_Checklist and Design_Review_Checklist ,,"NewWorkDescription: Update code after performing review code_review_checklist and design_review_checklist report. Requirement source:

ID	Subtype	Headline and Description
		NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"

ARTD-15396	Bug	
		[GPT]Marco PIT_0_CHANNELS_NUMBER is generated incorrectly when not using channel PIT_0_CH_RTI<*>
		
		Detailed description (how to reproduce it):
		When not using PIT_0_CH_RTI channel but using other channels of PIT_0 to run the test, I got the following problem:
		marco PIT_0_CHANNELS_NUMBER always generates 5 so the loop of Pit_Ip_GetInterruptBit function with channel equal to 4 was incorrect resulting in hard_fault error because we don't have the resource PIT_0_CH_4
		static inline uint32 Pit_Ip_GetInterruptBit(uint8 instance, uint8 channel)
		{
		uint32 returnFlag = 0U;
		#if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON))
		if (RTI == channel)
		{
		returnFlag = ((pitBase[instance]->RTI_TCTRL & PIT_RTI_TCTRL_TIE_MASK) >> PIT_RTI_TCTRL_TIE_SHIFT);
		}
		else
		#endif
		{
		returnFlag = ((pitBase[instance]->TIMER[channel].TCTRL & PIT_TCTRL_TIE_MASK) >> PIT_TCTRL_TIE_SHIFT);
		}
		return returnFlag;
		}
		#endif
		Preconditions:
		When not using PIT_0_CH_RTI channel but using other channels of PIT_0
		Test Case ID (internal TC that caught the defect) optional:
		Gpt_TC_FCT_3016(Gpt_TS_303)
		Observed behavior:
		marco PIT_0_CHANNELS_NUMBER was incorrectly generated causing the loop in the Pit_Ip_GetInterruptBit function to be incorrect
		Expected behavior:
		marco PIT_0_CHANNELS_NUMBER is correctly generated so that the loop in the Pit_Ip_GetInterruptBit function is correct
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		marco PIT_0_CHANNELS_NUMBER has a value of 4 when the channel PIT_0_CH_RTI is not used

ARTD-15445	Bug	 [I2c] Fix build fail driver due Mcl update<*> Detailed description (how to reproduce it): [...] !image-2021-08-18-10-39-52-742.png! Preconditions: [...] N/A

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: [...] I2c_TS_WIR_001 Observed behavior: [...] test case build fail Expected behavior: [...] Test case build pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15473	New	 New Feature [BASE] Add support for linker flash in S32K312 ,,"NewWorkDescription: Add support for linker flash in S32K312 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-15475	New	 New Feature [BASE] Update header files for S32K312 corresponding RM rev 2 ,,"NewWorkDescription: Update header files for S32K312 corresponding RM rev 2 Requirement source: RM rev 2 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-15466	New	 New Feature [BUILD_ENV] Create subchapter in IM about User mode configuration in AutosarOS ,,"NewWorkDescription: Create subchapter in IM about User mode configuration in AutosarOS. This will help user understand our User Mode approach and know what needs to be done in AutosarOS. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Create subchapter in IM about User mode configuration in AutosarOS."
ARTD-15470	New	 New Feature [RM][S32K3XX] Derivative S32K312 does not support IP Sema42 ,,"NewWorkDescription: S32K312 does not support IP Sema4, but DS and EB tresos still allow user to config Sema4 on this derivative.

ID	Subtype	Headline and Description
		Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Raise an error when user try to config Sema4 on derivative S32K312"
ARTD-15474	Bug	 [ETH] Update driver according to S32K3xx Reference Manual & Datasheet (Rev2)<*> Detailed description (how to reproduce it): Driver needs changing due to changes of new RM (S32K3xx Reference Manual, Rev. 2, 08/2021). Changes have been reviewed in ARTD-15242 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Driver changes according to new RM Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update driver code according to new header files (S32K344_EMAC.h...)

ARTD-15483	New	
		New Feature
		
		[RM][S32K3XX] add XBIC APIs to enable/disable per Slave/Master Port of integrity checking on runtime
		,,"NewWorkDescription:
		Add new APIs:
		For HLD
		void Rm_XbicEnableMasterFeedbackCheck(uint32 xbicInstance, uint8 masterPort, boolean bFeedbackCheckEnable);
		void Rm_XbicEnableSlaveEDCCheck(uint32 xbicInstance, uint8 slavePort, boolean bEDCCheckEnable);
		For Ip:
		void Xbic_Ip_EnableMasterFeedbackCheck(uint32 xbicInstance, uint8 masterPort, boolean bFeedbackCheckEnable);
		void Xbic_Ip_EnableSlaveEDCCheck(uint32 xbicInstance, uint8 slavePort, boolean bEDCCheckEnable);
		Requirement source:
		NA
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		NA"

ARTD-15484	New	 New Feature [SPI] Synchronous between Spi.component and Spi.xdm ,,"NewWorkDescription: Some node in xdm and component is different type that is prescribed in NXP_RTD_AUTOSAR_S32CT.pptx as SpiChannelHalfDuplexSupport Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:

ID	Subtype	Headline and Description
		Remove node of component is not available in xdmd Change to array with node having optional attribute "
ARTD-15491	Bug	 [Wdg] Some DEM error nodes are redundant<*> Detailed description (how to reproduce it): Step 1: Run command: Clean generate any TS in list test of WDG Step 2: Check interface Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Some DEM error nodes are redundant: WDG_E_CORRUPT_CONFIG, WDG_E_UNLOCKED, WDG_E_INVALID_PARAMETER, WDG_E_FORBIDDEN_INVOCATION, WDG_E_INVALID_CALL Please see the attached file for more detail. Expected behavior: Remove all Dem node not use Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15529	New	 New Feature [MCU] Support configuration for Callback Notification in IPL ,,"NewWorkDescription: Now Mcu doesn't support callback notification function at IPL. some callback function should be supported when using IP layer only. ex: POWER_IP_VLPSA_NOTIFICATION Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support callback notification at IPL"

ARTD-15536	Bug	
		[WDG] Issue with unlock - lock sequence when config WdgOsifTimeoutVal = 0<*>
		
		Detailed description (how to reproduce it):
		I created a test can cover the case Wdg can not unlock with config like this
		WdgOsifTimeoutVal: = 0 and this can help cover the error case in Swt_Ip_Unlock
		if(ElapsedTicks >= TimeoutTicks)
		{
		ret = SWT_IP_STATUS_ERROR;
		}
		My test step is:
		Step 1: Init Wdg with SlowMode*: WdgOsifTimeoutVal: = 0 and
		WdgSettingsSlow_WdgSoftLockConfiguration := true
		Step 2: After Init, Bit Softlock (SLK) will set to 1
		Step 3: Call SetMode to set new mode FastMode
		(WdgSettingsFast_WdgSoftLockConfiguration: true)
		Step 4: SetMode will still return error in Swt_Ip_Unlock but bit SLK is also clear to 0
		(that mean Wdg can unlock) and wdg is not lock again after SetMode function.

ID	Subtype	Headline and Description
		Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Swt_Ip_Unlock return error but bit SLK can still clear to 0 means Wdg can unlock and Wdg is also not lock again Expected behavior: Swt_Ip_Unlock return error show the correct status of Wdg and Wdg can lock again Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Issue Wdg can not lock again !image-2021-08-20-09-42-21-628.png|thumbnail! Ip function will check Unlock first, with WdgOsifTimeoutVal: = 0 and current lock mode is Softlock, Swt_Ip_Unlock will return error and it can not go to the Swt_Ip_Lock

ARTD-15539	Bug	[WDG] Swt_Ip_ClearResetRequest return error but RRR bit can still clear<*>
		
		Detailed description (how to reproduce it):
		Step1: Init with Slowmode WdgOsifTimeoutVal:=0,
		Also config MC_RGM to use feature SwtResetOnly
		Step2: Wait until Reset Request Flag (RRF) is set (can delay until timeout or use while until RRF is set)
		Step3: RRF bit is 1, Call ClearResetRequest function
		Step4: With current config WdgOsifTimeoutVal:=0, Swt_Ip_ClearResetRequest will return error at
		if(ElapsedTicks >= TimeoutTicks)
		{
		ret = SWT_IP_STATUS_TIMEOUT;
		}
		But after ClearResetRequest function, RRF bit is also can clear although Swt_Ip_ClearResetRequest return error
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		[...]
		Observed behavior:
		Swt_Ip_ClearResetRequest return error but RRF bit can clear
		Expected behavior:
		Driver show the correct status
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		[...]

ARTD-15545	Bug	[OCU] Registers of eMios master reset after call Ocu_Deintit function, not report error when config channel matches materbus channel config ,,"Detailed description (how to reproduce it): PVT_OCU_ARTD_12352_V01 in branch ARTD-12352-s32k3-rtm-ocu-the-master-bus-of-ocu-channel-will-be-wrongly-changed-to-mc-mode When config channel in EB, we choose eMios0_ch0 for materbus in Mcl and after choose it for Ocu channel config but EB not report error

ID	Subtype	Headline and Description
		We called Mcl_Init function to config selected materbus, and call in test suite before come in test case, when come test case and call Ocu_Deinit function it reset all registers of materbus had config Test Case ID (internal TC that caught the defect) optional: OCU_TC_FCT_0041 in Ocu_TS_002 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15555	New	 New Feature [FLS] Update code following to Rule 29 of Naming Convention ,,"NewWorkDescription: Update local variables, function parameters and struct members using only PascalCase naming, without any special prefix Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15554	Bug	 [S32K3 RTM] UART: An internal Error occurred when add Flexio_Uart component in S32DS3.4<*> Detailed description (how to reproduce it): The problem found when adding Flexio_Uart in S32DS3.4 for S32K344 derivative. I saw that in Flexio component file the parameter pass into hasExclusiveOwnership function is LPUART !image-2021-08-20-14-59-50-324.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: An internal Error occurred when add Flexio_Uart component in S32DS3.4 !image-2021-08-20-14-56-12-258.png|thumbnail! Expected behavior: Flexio_Uart component can be added without error in S32DS3.4 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-15561	Bug	 [S32K3XX][S32K3XX_100] IntCtrl_Ip_Init function should clear pending interrupt status before enabling any IRQ interrupt<*> Detailed description (how to reproduce it): Calling IntCtrl_Ip_Init function need clear pending before Enable IRQ interrupt. For example: By some way, Some pending are turned on after that User call IntCtrl_Ip_Init, and then it enable IRQ interrupt, because handler_interrupt not install yet, So Project will handfault, test not run. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Platform_TS_001 Observed behavior: Run over IntCtrl_Ip_Init function, some pending interrupt are set. It makes the pointer into undefine_handler Expected behavior: Clear pending Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add Clear pending function !image-2021-08-23-15-07-03-363.png!
ARTD-15564	Bug	[LIN]Lin_GetStatus() returns incorrect status for S32K3XX<*> Detailed description (how to reproduce it): The device is master node. The device sent a frame on the bus. Use other device(CANoe) to disturb the stop bit of data byte to create a error frame. Call Lin_GetStatus() function to check status after have an error on the TX frame. Observed behavior: Lin_GetStatus() has return LIN_RX_ERROR. Expected behavior: Lin_GetStatus() has return LIN_TX_ERROR. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Define node state events where frame error interrupt can occur. In FrameError Irq handler, call GotoIdleState function, it will stop transfer and save current node state to previous note state variable. In GetStatus function, for each Node state, we return the appropriate status.

ARTD-15565	Bug	[LIN] Lpuart_Lin_Ip_GetStatus returns the cause of the error incorrect when have frame error for K3XX<*>
		
		Detailed description (how to reproduce it):
		The device is master node.
		The device receive a frame on the bus.
		Use other device(CANoe) to disturb the stop bit of data byte to create a error frame(framing error).
		Call Lpuart_Lin_Ip_GetStatus() function to check status after have an error on the RX frame.
		Observed behavior:
		Lpuart_Lin_Ip_GetStatus() returns LPUART_LIN_IP_STATUS_RX_HEADER_ERROR
		Expected behavior:
		Lpuart_Lin_Ip_GetStatus() returns LPUART_LIN_IP_STATUS_RX_ERROR
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:
		Please recheck the condition when check the cause of frame error:
		case LPUART_LIN_IP_FRAME_ERROR:
		/ Found cause of the error from header or reponse /
		if (LPUART_LIN_IP_NODE_STATE_RECV_DATA{color:#de350b} != LinCurrentState->PreviousNodeState)
		_{
		_RetStatus = LPUART_LIN_IP_STATUS_RX_ERROR;
		_}

ID	Subtype	Headline and Description

		else
		{
		RetStatus = LPUART_LIN_IP_STATUS_RX_HEADER_ERROR;
		}

ARTD-15567	New	 New Feature [OS] Add S32K312 to sdk_manifest_os.xml ,,"NewWorkDescription: Add S32K312 to sdk_manifest_os.xml Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-15578	New	 New Feature [S32K3XX][PORT] Some functions in IP layer which do not appear on requirement should be reviewed and updated ,,"NewWorkDescription: The Exclusive Areas for K3 platform are incorrect. Some of them are redundant (need to be removed), and the rest need to be renamed. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove/Add/Renaming the Exclusive Areas in code for K1. From IPW to IPL. All exclusives should be existed in IPL. The ones in IPW should be removed. #include SchM_Dio.h should be moved from IPW to IPL Update the UM/IM if needed Check and update RTE if needed"
ARTD-15597	Bug	 [CAN] FlexCAN_ConfigTimestampModule should not have write access directly to DCMRWF1 causing impacting to other modules<*> Detailed description (how to reproduce it): as implemented in driver: !image-2021-08-23-12-15-12-607.png! this will overwrite other bits: !image-2021-08-23-12-15-36-020.png! Preconditions: Review code Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: FlexCAN_ConfigTimestampModule writes directly to DCMRWF1 Expected behavior: FlexCAN_ConfigTimestampModule will read modify write to DCMRWF1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: change to RMW instead of Write to DCMRWF1 register
ARTD-15587	Bug	 [MCU]have some error when build CT and EBT example mcu module<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): [have some error and warning when build all mcu example by platform and base module] Preconditions: PVT_DEM_S32K3_1.0.0_V01 PVT_DET_S32K3_1.0.0_V01 PVT_OS_S32K3_1.0.0_V01 PVT_BASE_S32K3_1.0.0_V17 PVT_S32K3XX_S32K3_ARTD_14610_V16 feature/ARTD-12393-s32k3-rtm-mcu-tresos-and-ds-examples Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: please check in all example. !image-2021-08-23-10-26-09-724.png! !image-2021-08-23-10-26-48-288.png! Expected behavior: not error for base,platform module when build mcu example Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15596	Bug	[Mcl] Emios_Mcl_Ip_VS_0_PBcfg.h of EB generate missing macro<*> Detailed description (how to reproduce it): In the MCL module enable emios ip. In the file Emios_Mcl_Ip_VS_0_PBcfg.h of S32CT have generate macro MCL_EMIOS_LOGIC_CH0 but in the EB not generate this macro. I need this macro for test some function for mcl look like Mcl_Emios_SetReloadInterval, Mcl_Emios_SetCounterBusPeriod Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: MCT_TS_402 Observed behavior: In the EB not generate macro MCL_EMIOS_LOGIC_CH0 Expected behavior: The EB generate macro MCL_EMIOS_LOGIC_CH0 in Emios_Mcl_Ip_VS_0_PBcfg.h file look like CT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15602	New	New Feature [RM][S32K3XX] Disable AXBS for derivative S32K312 which is not supported ,,"NewWorkDescription: Disable AXBS for derivative S32K312 which is not supported Requirement source: NA Proposed solution optional: Disable, AXBS for derivative S32K312 which is not supported"

ID	Subtype	Headline and Description
ARTD-15603	New	New Feature [RM][S32K3XX] Improve AXBS driver code ,,"NewWorkDescription: Update code for user mode support Recheck resource follow RM Requirement source: NA Proposed solution optional: update follow description"
ARTD-15606	New	New Feature [RM][S32K3XX] Add corresponding header files for S32K314, S32K324 derivatives" ,,"NewWorkDescription: Include header file for S32K314 and S32K324 derivative Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: K314 and K324 share the same header file with K344

ARTD-15610	New	New Feature
		
		[FLS] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when using user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);

ID	Subtype	Headline and Description
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions. 3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support) List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx All functions should be listed out in the table like: Function syntax||Description||Available via void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h 4. Subchapter """*User Mode configuration in AutosarOS*""" needs to be added in IM: !image-2021-08-19-09-26-20-823.png|thumbnail! In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466). In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from """*User Mode support*"" to """*User Mode configuration in the module*""". Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD. For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers. Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"
ARTD-15609	New	New Feature [FLS] Reduce parameters of functions which violated HIS_PARAM checker for C40_Ip layer ,,"NewWorkDescription: Reduce parameters of functions which violated HIS_PARAM checker Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-15659	Bug	[ICU][S32K3XX] The Standby mode for WKPU need supported in Wkpu_Ip_Init() function<*> Detailed description (how to reproduce it): The platform S32K3XX has WKPU HW available for standby feature. This feature is a requirement (CPR_RTD_00403.icu) as following: The Icu driver shall provide an optional configuration parameter to support wakeup IP operation across STANDBY. Per default this optional functionality and configuration parameters shall be disabled,. If the configuration parameter is enabled, the following shall be respected:

ID	Subtype	Headline and Description
		The driver shall NOT CLEAR the interrupt flag or the interrupt enable bit, after a wakeup event. The driver shall make sure it will correctly service the wakeup event, if this event occurred before init. This is done to support the hardware functionality of IP's that may have flags set after the occurred wakeup event that leads to a memory clear." Preconditions: ICU_WKPU_STANDBY_WAKEUP_SUPPORT = STD_ON Test Case ID (internal TC that caught the defect) optional: Icu_TC_WBT_0040 Observed behavior: [...] Expected behavior: The driver WKPU shall NOT CLEAR the interrupt flag or the interrupt enable bit, after a wakeup event follow to the req CPR_RTD_00403.icu. Proposed solution optional: when mode standby for wkpu hardware is turned on in EB, In the function Wkpu_Ip_Init() need to check the condition ICU_WKPU_STANDBY_WAKEUP_SUPPORT to implement this feature.
ARTD-15668	Bug	[ADC] Fix findings from code review checklist<*> Detailed description (how to reproduce it): Fix findings according to code checklist Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15669	Bug	[CAN] re-implement SWS_Can_00384<*> Detailed description (how to reproduce it): SWS_Can_00384|Each time the CAN controller state machine is triggered with the state transition value CAN_CS_STARTED, the function Can_SetControllerMode shall re-initialize the CAN controller with the same controller configuration set previously used by functions Can_SetBaudrate or Can_Init. but as implemented in the code. driver just switch from stopped state (disable mode) to started state(normal mode) => a re-init (reset all then init again) is necessary to reset buffers, fifo, bus-off,.. Test Case ID (internal TC that caught the defect) optional:__*Preconditions: NA Observed behavior: driver didn't re-init controller when started state required Expected behavior: driver does re-init controller when started state required Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: call FlexCan_Ip_Init at Ipw_SetcontrollertoStart and re-configure baudrate by

ID	Subtype	Headline and Description
		Can_au16ControllerBaudRateSel and Can_lpw_eClockMode which are saved at runtime

ARTD-15693	New	New Feature
		
		[adc] Enable ECPD generation for IP components (CPR_RTD_00544)
		,,"Note:
		This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"".
		How to implement:
		# Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below.
		# To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows:
		{code:javascript}
		if (configComponent.isOptionSet(""ecucDefinitionCollection"") &&
		(configComponent.getId() === ""Gmac"")) {
		where you can replace ""Gmac"" with the ID of your IP component.
		# Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview.
		How to validate:
		# Manually create an EBT plugin using the previously generated ECPD. To achieve this:
		## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository.
		## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component.
		# Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK)
		CHECKPOINT 1: The module should have been successfully imported into the project.
		# Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""):
		{panel}!screenshot-1.png!
		# Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_.
		# Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button)
		# Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer)
		CHECKPOINT 2: The ECVD file should have been successfully applied to your module.
		# Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation.
		CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc)

ID	Subtype	Headline and Description
		# Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value >
CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component.
Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_.
Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.
CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files.
Requirements covered by this ticket:
CPR_RTD_00544
EA_RTD_00107
EA_RTD_00108
References:
https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template
https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"")
Legend:
EPD ECU Parameter Definition (Schema) Used by EBT
ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT
EPC ECU Parameter Configuration (Configuration File) Used by EBT
ECVD ECU Configuration Value Description (Configuration File) Used by S32CT
"
ARTD-15699	New	New Feature

[eth] Enable ECPD generation for IP components (CPR_RTD_00544)
,,"Note:
This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"".
How to implement:
Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below.
To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows:
{code:javascript}
if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) {
where you can replace ""Gmac"" with the ID of your IP component.
Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview.
How to validate:
Manually create an EBT plugin using the previously generated ECPD. To achieve this:
Unzip https://jira.sw.nxp.com/secure/attachment/828304/lp_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. |

ID	Subtype	Headline and Description
		## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15700	New	

ID	Subtype	Headline and Description
		New Feature [fls] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the

ID	Subtype	Headline and Description
		current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15703	New	New Feature [i2c] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK)

ID	Subtype	Headline and Description
		CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15709	New	 New Feature [ocu] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note:

ID	Subtype	Headline and Description
		This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component.

ID	Subtype	Headline and Description
		# Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15711	New	New Feature [platform] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project.

ID	Subtype	Headline and Description
		# Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15715	New	 New Feature [rm] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"".

ID	Subtype	Headline and Description

		How to implement:
		# Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below.
		# To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows:
		{code:javascript}
		if (configComponent.isOptionSet(""ecucDefinitionCollection"") &&
		(configComponent.getId() === ""Gmac"")) {
		where you can replace ""Gmac"" with the ID of your IP component.
		# Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview.
		How to validate:
		# Manually create an EBT plugin using the previously generated ECPD. To achieve this:
		## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository.
		## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component.
		# Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK)
		CHECKPOINT 1: The module should have been successfully imported into the project.
		# Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""):
		{panel}!screenshot-1.png!
		# Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_.
		# Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button)
		# Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer)
		CHECKPOINT 2: The ECVD file should have been successfully applied to your module.
		# Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation.
		CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc)
		# Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value >
		CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component.
		# Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_.
		# Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.

ID	Subtype	Headline and Description
		CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15716	New	 New Feature [sai] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png!

ID	Subtype	Headline and Description
		# Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15717	New	 New Feature [sent] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below.

ID	Subtype	Headline and Description

		# To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows:
		{code:javascript}
		if (configComponent.isOptionSet(""ecucDefinitionCollection"") &&
		(configComponent.getId() === ""Gmac"")) {
		where you can replace ""Gmac"" with the ID of your IP component.
		# Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview.
		How to validate:
		# Manually create an EBT plugin using the previously generated ECPD. To achieve this:
		## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository.
		## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component.
		# Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK)
		CHECKPOINT 1: The module should have been successfully imported into the project.
		# Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""):
		{panel}!screenshot-1.png!
		# Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_.
		# Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button)
		# Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer)
		CHECKPOINT 2: The ECVD file should have been successfully applied to your module.
		# Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation.
		CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc)
		# Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value >
		CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component.
		# Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_.
		# Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set.
		CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files.
		Requirements covered by this ticket:
		CPR_RTD_00544
		EA_RTD_00107

ID	Subtype	Headline and Description
		EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15718	New	 New Feature [spi] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_.

ID	Subtype	Headline and Description
		# Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15720	New	 New Feature [uart] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript}

ID	Subtype	Headline and Description
		if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button) # Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template

ID	Subtype	Headline and Description
		# https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15721	New	 New Feature [wdg] Enable ECPD generation for IP components (CPR_RTD_00544) ,,"Note: This feature must be implemented by all the modules for which this ticket was cloned (including CDDs). No clone shall be closed with ""Not Applicable"" or ""No Action Taken"". How to implement: # Add ""options_expr"" tags (containing all the necessary options) for the fields of the IP component(s). Please refer to the slides covering ""EPD Generation"" in Reference #2 below. # To ensure that the ECPD is generated only for your component, modify line 512 in ""mcu_data/components/PlatformSDK_S32K3_2021_08/system/codegenerator.js"" as follows: {code:javascript} if (configComponent.isOptionSet(""ecucDefinitionCollection"") && (configComponent.getId() === ""Gmac"")) { where you can replace ""Gmac"" with the ID of your IP component. # Check that there are no errors reported in the Problems view and that the ECPD has been generated in Code Preview. How to validate: # Manually create an EBT plugin using the previously generated ECPD. To achieve this: ## Unzip https://jira.sw.nxp.com/secure/attachment/828304/Ip_TS_T40D34M10I0R0.zip in the ""output/eclipse/plugins"" folder of your K3 work tree / repository. ## Open ""Ip_TS_T40D34M10I0R0/plugin.xml"" and replace all occurrences of ""Gmac"" with the ID of your IP component. # Create an EBT project (File > New > Configuration Project > Project Name: TstIp > Next > ECU ID: someId; Target: CORTEXM/S32K3XX > Finish) and add the previously created module (Right click on TstIp in Project Explorer > Module Configurations... > Double click on your module > OK) CHECKPOINT 1: The module should have been successfully imported into the project. # Go to S32DS and create a valid project using your IP component (or use an already existing one). Please assign a value other than the default value to each setting to avoid default values in this configuration{color}*. Rename your IP component instance and discard the ""_1"" prefix (e.g. ""Gmac_1"" > ""Gmac""): {panel}!screenshot-1.png! # Generate the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere to avoid overwriting them in a later step. We'll call this set of files OriginalGenerateFiles_. # Generate the ECVD file for your IP component instance (Global Settings > EcvdGenerationMethod = INDIVIDUAL > EcvdOutputPath = <EcvdOutputDir> > Click on the ""Generate Configuration"" button)

ID	Subtype	Headline and Description
		# Import the previously generated ECVD file in your EBT project (Right click on TstIp in Project Explorer > Im and Exporters... > Green Button > Next > File Name: <Browse and select the ECVD file> > Next > Enable path mapping > Finish > Run Importer) CHECKPOINT 2: The ECVD file should have been successfully applied to your module. # Save (CTRL S) and generate the project (Right click on TstIp in Project Explorer > Generate Project) to trigger the EPC generation. CHECKPOINT 3: The EPC file should have been successfully generated (TstIp/output/output/<Ip>.epc) # Import the previously generated EPC file in your S32DS project (File > Import > Import ECU Configuration > Path: <EpcOutputDir> > Check ""Merge into current configuration"" > Check ""Check ECUC-MODULE-DEF"" value > CHECKPOINT 4: The EPC file should have been successfully imported into your S32DS project. If you get the error ""The required modules are not available for the current configuration"" it means that the ECUC-MODULE-DEF check has failed and you're not properly using M4_XDM_AR_PKG_NAME in your IP component. # Generate again the [LT/PB]Cfg.h/.c files of your IP component and save them somewhere without overwriting the previous set of files. We'll call this new set of files ImportedGenerateFiles_. # Compare the OriginalGenerateFiles set with the ImportedGenerateFiles set. CHECKPOINT 5: The comparison should be binary identical. There should be no single difference between the two set of files. Requirements covered by this ticket: CPR_RTD_00544 EA_RTD_00107 EA_RTD_00108 References: # https://jira.sw.nxp.com/secure/attachment/828307/Ethernet.template # https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=erB0sH (Relevant chapters: ""9. EPD Importer Replacing the lost GNU M4 macros"", ""10. EPD Generation"", ""11. EPC Importer"", ""12. EPC Generation"") Legend: EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT "
ARTD-15732	Bug	 [Platform] Exceptions.c build at failed in GCC 10.2<*> Detailed description (how to reproduce it): The exceptions.c file build at failed only in GCC 10.2 compiler in line number 53: ASM_KEYWORD(".section .mcal_text"); !image-2021-08-25-13-13-54-525.png! [^build_cmd.txt] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Uart_TS_WIR_0001 Observed behavior: Error message: D:\Tools\cygwin64\tmp\ccxI35gv.s: Assembler messages: D:\Tools\cygwin64\tmp\ccxI35gv.s:30: Error: changed section attributes for .mcal_text D:\Tools\cygwin64\tmp\ccxI35gv.s:40: Error: changed section attributes for .mcal_text D:\Tools\cygwin64\tmp\ccxI35gv.s:43: Error: changed section attributes for .mcal_text

ID	Subtype	Headline and Description
		D:\Tools\cygwin64\tmp\ccxI35gv.s:50: Error: changed section attributes for .mcal_text Expected behavior: Build at passed in GCC 10.2 compiler Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15735	Bug	 [PORT] Fix violation rules of code and design checklist<*> Detailed description (how to reproduce it): After review checklist, there is some violation rule, refer to linked ticket Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: After review checklist, there is some violation rule Expected behavior: All violation need to be fixed Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-15740	Bug	 [SENT][S32CT] Cannot update code for Sent on CT<*> Detailed description (how to reproduce it): Create a project for Sent on peripheral tool. After the configurating completed without error on any component->choose update code button >Error occurred and the code couldn't be generated. !image-2021-08-25-15-34-06-104.png! !image-2021-08-25-15-34-59-400.png! This issue happens on both HLD and IPL. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15734	New	 New Feature [RM][S32K3XX] Update RM Configuration and codegen for CT ,,"NewWorkDescription: Update configuration file for RM module (add some validation related to Sema4 and memory region control) Requirement source: [...]

ID	Subtype	Headline and Description
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Attach below "
ARTD-15737	Bug	 [ICU][S32K3XX] Build error for CCOV<*> The error due to the macro is not generated as below: Notice for 2 ipv Silu2 and LPCMP: !image-2021-08-25-15-33-43-997.png!
ARTD-15744	Bug	 [LIN] Function Lin_GetStatus return status LIN_RX_ERROR in case master send a incorrect response with IPV: FLEXIO<*> Detailed description (how to reproduce it): Create a error in stop bit of data byte 1 while a response is transmitting, driver will return status LIN_RX_ERROR. Preconditions: Because IPV FlexIO don't support hardware detect frame error. Thus, when a error in stop bit of data byte occurred (IPVs LPUART or LinFLexD support hardware detect frame error always generate a frame error in same case), with IPV FlexIO driver handle this error by function Flexio_Lin_Ip_ErrInterruptHandler and set LinCurrentState->CurrentEventId = FLEXIO_LIN_IP_RX_OVERRUN_ERROR. Function Lin_Getstatus will check LinCurrentState->CurrentEventId = FLEXIO_LIN_IP_RX_OVERRUN_ERROR and return value status in function Flexio_Lin_Ip_GetStatusFromRxOverrunError. But in this function driver only implemented with case RX error occur. Thus, driver will return status LIN_RX_ERROR. !image-2021-08-25-16-50-49-124.png|width=695,height=256! Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_0214 Observed behavior: return LIN_RX_ERROR Expected behavior: return LIN_TX_ERROR Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15824	Bug	 [crypto] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png!

ID	Subtype	Headline and Description
		Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15826	Bug	[eth] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15827	Bug	[fee] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx]

ID	Subtype	Headline and Description
		[https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15828	Bug	[fls] [S32K3 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15830	Bug	[i2c] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15832	Bug	[icu] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...]

ID	Subtype	Headline and Description
		All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15838	Bug	 [port] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15840	Bug	 [rm] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png!

ID	Subtype	Headline and Description
		Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15844	Bug	[uart] [S32K 1.0.0] Fix all violations (HIS + MISRA + VSMD reports)<*> Detailed description (how to reproduce it): Create HIS MISRA VSMD reports Fix all violations for HIS MISRA VSMD reports *Reference: MISRA Deviation List: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/SW%20Development/RTD%20MISRA%20Deviations.xlsx] [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] RTD Quality Criteria: [https://bitbucket.sw.nxp.com/projects/ASPA/repos/real_time_drivers/browse/Generic/Quality%20Assurance/RTD%20AASWS%20Gate%20and%20Release%20Criteria.xlsx] VSMD report: 0 warning, 0 error for RTM release MISRA report: 0 unjustified MISRA violations HIS report: !image-2021-08-30-12-26-52-249.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] All violations fix and follow RTD Quality Criteria Proposed solution optional: Fix all MISRA, HIS, VSMD violations
ARTD-15846	Bug	[ADC] Fix all duplicated UUIDs<*> Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs.

ID	Subtype	Headline and Description
		# Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15856	Bug	[i2c] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15858	Bug	[icu] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15863	Bug	[platform] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.

ID	Subtype	Headline and Description
ARTD-15866	Bug	[rm] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15870	Bug	[uart] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15871	Bug	[wdg] [S32K3 1.0.0] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. # Fix all violation that reports at PluginsCheck report: [http://somov.ea.freescale.net/1/project/custom_plugincheck/details] Refer attachment for 2021.08.30 baseline.
ARTD-15762	Bug	[ICU][S32K3XX] Build error when using DMA with signal measurement mode<*> In function Icu_SignalMeasurementDmaProcessing(), the variable ChannelIndex is declared twice and sub function Icu_Ipw_GetPWandPeriod() is not declared in ipw file :

ID	Subtype	Headline and Description
		!image-2021-08-26-16-13-49-316.png! The function Icu_Ipw_GetPWandPeriod() need to be declared in IPW Layer is to get the value of period and pulse width after calculating with DMA.
ARTD-15765	Bug	 [WDG] SWT_IP_CLEAR_RESET_REQUEST node not available but generate code still = STD_ON in S32CT<*> Detailed description (how to reproduce it): Step 1: Create new project into S32CT Step 2: Add Swt_Ip_1 component into project and Step 3: Config " Swt Disable Allowed" node is OFF, same as my picture ! image-2021-08-26-17-18-12-327.png! Step 4: Update code and Check code generated Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: SWT_IP_CLEAR_RESET_REQUEST node not available but generate code still = STD_ON !image-2021-08-26-17-20-24-477.png! Expected behavior: When the SWT_IP_DEINIT node is OFF the SWT_IP_CLEAR_RESET_REQUEST node must also be OFF Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-15773	New	 New Feature [BASE] Add support for REQUIRES-INDEX in generateEcpd.js ,,"NewWorkDescription: Add support for REQUIRES-INDEX in generateEcpd.js Requirement source: AUTOSAR_TPS_ECUConfiguration (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add support for REQUIRES-INDEX in generateEcpd.js"
ARTD-15779	Bug	 [LIN] Driver should clear all bit values that do not belong in the actual data bitfield when reading the data register<*> Detailed description (how to reproduce it): Before recording the data read from a register, the driver shall filter the value read from the data register clearing all bit values that do not belong in the actual data bitfield. Configured data alignment in the register shall also be considered Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15786	Bug	 [S32K3XX][FLEXIO_I2C]send stop frame after FLEXIO_I2C_IP_DMA_ERROR_STATUS make bus busy<*> Detailed description (how to reproduce it): [...] set up Maf send use Flexio_I2c_Ip_MasterReceiveData to receive with InValid_Rx_buffer adress to raise an DMA error after Driver get DMA_IP_CH_ERROR_STATE in Flexio_I2c_Ip_MasterDmaTransferErrorHandler(), Driver will send a stop bit with value 0 make bus busy. Flexio_I2c_Ip_WriteShifterBuffer(BaseAddr, TX_SHIFTER(ResourceIndex), (((uint32)FLEXIO_I2C_IP_STOP_BYTE_VALUE_U32)<<24U), FLEXIO_SHIFTER_RW_MODE_BIT_SWAP); Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] Ip_Flexio_TC_FCT_2023 Observed behavior: [...] after Driver get DMA_IP_CH_ERROR_STATE in Flexio_I2c_Ip_MasterDmaTransferErrorHandler(), Driver will send a stop bit with value 0 make bus busy. Flexio_I2c_Ip_WriteShifterBuffer(BaseAddr, TX_SHIFTER(ResourceIndex), (((uint32)FLEXIO_I2C_IP_STOP_BYTE_VALUE_U32)<<24U), FLEXIO_SHIFTER_RW_MODE_BIT_SWAP); Expected behavior: [...] after Driver get DMA_IP_CH_ERROR_STATE in Flexio_I2c_Ip_MasterDmaTransferErrorHandler(), Driver need stop transfer Flexio_I2c_Ip_MasterStopTransfer() Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: [...]N/A
ARTD-15787	Bug	 [ICU][S32K3XX] Fix bug wrong DMA macro generation in DS<*> Detailed description (how to reproduce it): When enable Icu DMA support, DS generate wrong macro EMIOS_ICU_MODE_WITHOUT_DMA instead EMIOS_ICU_MODE_WITH_DMA. Reason is get wrong id as follow image: !image-2021-08-27-11-29-48-041.png|width=1110,height=67! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Icu_TC_WBT_0302 Observed behavior:

ID	Subtype	Headline and Description
		[...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Correct ID
ARTD-15795	Bug	[ETH]Error occurred for Timestamp nodes in Post build mode<*> Detailed description (how to reproduce it): Postbuild with multiple variants enabled. because EthTimeStampRequiredAccuracy with multiple variant = false refer to node McuClockReferencePointFrequency has multiple variant. Preconditions: Postbuild with multiple variants enabled. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: error reported at INVALID of node EthTimeStampRequiredAccuracy Expected behavior: No error reported Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change nodes EthTimeStampRequiredAccuracy and EthTimeStampReferenceClock with: <a:a name="POSTBUILDVARIANTVALUE" value="true"/> <a:a name="POSTBUILDVARIANTMULTIPLICITY" value="true"/>
ARTD-15792	Bug	[DIO] Missing rte_dio dependency in sdk_manifest<*> Detailed description (how to reproduce it): In sdk_manifest, platform.driver.siul2_dio is missing the dependency platform.driver.rte_dio Expected behavior: platform.driver.siul2_dio should have the dependency platform.driver.rte_dio Proposed solution optional: correct sdk_manifest
ARTD-15797	Bug	[S32K3] S32DS driver raise error incorrectly<*> Detailed description (how to reproduce it): When config key on S32DS with key_export = true but key_type in key_catalog is no in group (AES, HMAC, TDES) e.g ECC_PAIR , driver still raise error " HSE Key Export is enabled requiring CryptoKeyElement with CryptoKeyElementId = 99 " Preconditions: NA Observed behavior: Driver raise error " HSE Key Export is enabled requiring CryptoKeyElement with CryptoKeyElementId = 99 " when config key_export=true and key_type = ECC_PAIR Expected behavior: Driver doesn't raise error when config key_export=true and key_type in group (ECC_PAIR, ECC_PUB, RSA_PAIR, RSA_PUB) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: NA
ARTD-15801	Bug	[WDG] Correct error codes in Wdg_Channel.c<*> Detailed description (how to reproduce it): 1. In Wdg_Channel.c, in Wdg_ChannelClearResetRequest, the Det_ReportRuntimeError API is called with error id WDG_E_PARAM_TIMEOUT, which is related to the timeout parametere of the Wdg_SetTriggerCondition api. 2. WDG_E_PARAM_CONFIG should be used to report that the accessed resource is not available on the current core. Some Det's use this error id instead of WDG_E_PARAM_MODE: in Wdg_ChannelInit in the line1363 valid = Wdg_ChannelValidateMode(Wdg_apConfigPtr[Wdg_Instance]->Wdg_DefaultMode, WDG_INIT_ID, WDG_E_PARAM_CONFIG, Wdg_Instance); In Wdg_VadidateHardwareSetting() Proposed solution optional: 1. Add a new error code WDG_E_STATUS_TIMEOUT = 0x16, to be used by the Wdg_ClearResetRequest() API. This define should be guarded by the same #ifdefs as the API. 2. Replace WDG_E_PARAM_CONFIG with WDG_E_PARAM_MODE where mentioned. 3. Update the error codes descriptions as in the Requirement SWS_Wdg_00010 as described in https://crucible1.sw.nxp.com/cru/R-ARTD-1027.
ARTD-15900	Bug	[RM] Diff output CT and EB for Virt Wrapper<*> Detailed description (how to reproduce it): diff output EB and CT for Virt_Wrapper See more attachments Preconditions: generate output EB and CT then compare Test Case ID (internal TC that caught the defect) optional: Rm_TC_FCT_0002 Observed behavior: diff output EB and CT for Virt_Wrapper Expected behavior: same output EB and CT for Virt_Wrapper Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: same output EB and CT for Virt_Wrapper
ARTD-15916	Bug	[GPT] RTC GptChannelTickFrequency is not matched with GPT clock sources<*> Detailed description (how to reproduce it): The RTC GptChannelTickFrequency is mismatched when choosing different clock sources: RTC_IP_CLOCK_SOURCE_2 (FIRC 48M), but GptChannelTickFrequency is 128000 RTC_IP_CLOCK_SOURCE_1 (SIRC 32K), but GptChannelTickFrequency is 16000000 RTC_IP_CLOCK_SOURCE_3 (FXOSC 8-40M, dynamic value), but GptChannelTickFrequency is always 32000 Preconditions: Choose RTC as GPT channel hw Test Case ID (internal TC that caught the defect) optional: Ip_Rtc_TC_FCT_0001(Ip_Rtc_TS_001)

ID	Subtype	Headline and Description
		Observed behavior: RTC GptChannelTickFrequency is mismatched when choosing different clock sources Expected behavior: Correct RTC GptChannelTickFrequency when choosing different clock sources. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-15917	Bug	[Port][CTHL] Wrong register's bit setting for unused pins<*> Detailed description (how to reproduce it): Use Plugin_2882021 and generate the layout for S32DS. Add Port component and config for NotUsedPortPin as below: PortPin Pull Enable = True PortPin Pull Select = True Update source code and find Port_xxx_PBcfg.c Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The register setting for the PortPin Pull Select was wrong, It must be set on 11th bit. !image-2021-08-30-18-05-59-304.png! In this case, it must be 0x00082800 Expected behavior: The register must be set correctly.
ARTD-15915	Bug	[ADC] Internal buffer u32DmaNoIrqBuffer was not cleared after read group of previous test case in DMA without interrupt feature<*> Detailed description (how to reproduce it): Internal buffer u32DmaNoIrqBuffer was not cleared after read group of previous test case in DMA without interrupt feature Preconditions: Transfer type DMA Group sw injected oneshot without interrupt Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0111 Adc_TS_007 cfg 2 Observed behavior: Start injected oneshot group Wait until read group return E_OK Real status: Read group always reuturn E_OK because internal buffer u32DmaNoIrqBuffer still have valid data from previous test case Expected behavior: u32DmaNoIrqBuffer was cleared or make data invalid after read group and deinit Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15924	Bug	[UART] Driver should clear all bit values that do not belong in the actual data bitfield when reading the data register<*> Detailed description (how to reproduce it): Before recording the data read from a register, the driver shall filter the value read from the data register clearing all bit values that do not belong in the actual data bitfield. Configured data alignment in the register shall also be considered

ID	Subtype	Headline and Description
		Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-15931	Bug	[RM] [S32K3] Function Sema42_Ip_GetResetGateIndex is missing return SEMA42_RESET_GATE_ALL<*> Detailed description (how to reproduce it): Please check Requirement SEMA42_IP_009_001 Function Sema42_Ip_GetResetGateIndex is missing return SEMA42_RESET_GATE_ALL if all gates have been targetted for reset. !image-2021-08-31-10-28-32-582.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16026	Bug	[S32K3 RTM] Functions ArrayIntegrityCheck and UserMarginReadCheck should return an error when calling them with the wrong DomainID<*> Detailed description (how to reproduce it): Step1: Call C40_Ip_MainInterfaceWrite or C40_Ip_MainInterfaceSectorErase with wrong DomainID Step2: Call C40_Ip_ArrayIntegrityCheck or C40_Ip_UserMarginReadCheck with correct param, the return status will be Error Test Case ID (internal TC that caught the defect) optional: Ip_C40_TC_1012 Observed behavior: variable C40_Ip_CurrentTicks is not reset before use C40_Ip_ArrayIntegrityCheck or C40_Ip_UserMarginReadCheck return error in this case Expected behavior: variable C40_Ip_CurrentTicks is reset before use C40_Ip_ArrayIntegrityCheck or C40_Ip_UserMarginReadCheck will return success in this case
ARTD-16222	New	New Feature [RM] S32K3 Validate values from hardware before return.

ID	Subtype	Headline and Description
		,,"NewWorkDescription: Update driver follow Measure Applied in FMEA report in attachment. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-16263	Bug	[UART] Flexio receiver function not work when using DMA<*> Detailed description (how to reproduce it): In the Flexio_Uart_Ip.c file, seem that _Flexio_Uart_Ip_CompleteReceiveUsingDma() function has been suspended in while loop that is used to check for the data is completely shifted out of shift register. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Test case Uart_WBT_TC_0010.c Observed behavior: [...] Expected behavior: While loop should be executed to get timer status instead of shifter status to avoid suspend. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16266	Bug	[Mcl] S32CT not generate configuration structure for routing interrupt<*> Detailed description (how to reproduce it): Create new project and add MCL. In to project using EMIOS and enable multicore. Enable interrupt for emios in platform for both core 0 and 1. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: MCL_TS_430, MCL_TS_431 Observed behavior: In the file IntCtrl_Ip_Cfg.h defined struct intRouteConfigEcucPartition_0 but in the IntCtrl_Ip_Cfg.c, I don't see it. That gives error when i build test: !image-2021-09-01-10-14-09-159.png! Expected behavior: Struct intRouteConfigEcucPartition_0 generated in IntCtrl_Ip_Cfg.c like when generate with EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16268	Bug	[FLS][S32K3XX_RTM_100] Diff output CT and EB<*> Detailed description (how to reproduce it): See more pictures in attachments Preconditions: N/A Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		N/A Observed behavior: Diff output EB and CT Expected behavior: Same output when generating by EB and CT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Same output when generating by EB and CT
ARTD-16271	Bug	[ICU][S32K3XX] Error for DMA configuration in S32DS<*> In configuration in DS, there are 2 channel configured for DMA mode (Emios0_CH1 and Emios1_CH22 as config file attached), but the output generation generate until 3 channel with DMA mode. !image-2021-09-01-11-36-44-548.png! The test name in testing side folder: Icu_TS_DS_031 with the mex file attached.
ARTD-16281	Bug	[Port][CTHL] Unexpected warning occurs after configurating some pins<*> Detailed description (how to reproduce it): Use Plugin_192021 and generate the S32DS layout. Create a new project and add Port component. Choose randomly PortPin MSCR from 128 to 219, set PortPin Mode to any Input mode (mentioned in Io_mux) Case ID (internal TC that caught the defect) optional: N/A Observed behavior: A warning is shown up as follow: !image-2021-09-01-14-58-20-903.png! Its applied for the last pin configurated in one container (the bigger container number takes this warnings), that means something like this: multi container: !image-2021-09-01-15-05-24-668.png! one container: !image-2021-09-01-15-05-44-803.png! Expected behavior: No wrong warnings are shown up.
ARTD-16286	Bug	[ETH] DET error shall not be reported if Eth driver is un-initialized in Eth_MainFunction<*> Detailed description (how to reproduce it): In Eth_MainFunction, DET error is reported in case Eth driver is un-initialized. According with Autosar requirements if the module is not initialized and the main function is executed no error should be reported. !SWS_BSW_00037.png|width=618,height=98! Preconditions: Eth_MainFunction() is called before Eth_Init(), or Eth_Init() is called without success. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In case driver is un-initialized, Eth_MainFunction() raises DET report. Expected behavior:

ID	Subtype	Headline and Description
		In case driver is un-initialized, Eth_MainFunction() shall not raise DET report and return immediately. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: CE's comment: as workaround from customers, they have disabled the Det from Eth configuration. Their major issue is that Eth variables that are used in Eth_MainFunction are initialized in Eth_Init. Since the Eth_MainFunction is executed before Eth_Init there will be an exception reported by the Os because the accessed variables are not initialized. !Eth_apCtrlConfig_undefined.png! Please consider also this aspect when analysis.
ARTD-16289	New	 New Feature [icu] Increase code exposure numbers ,,"NewWorkDescription: Expose as much of the driver code as possible (this will be checked with the code exposure tool). Code exposure target is minimum 90% Code exposure for gpt driver is around 72% in this moment Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16296	Bug	 [Port][CTHL] No constrain for VirtWrapperSupport feature<*> Detailed description (how to reproduce it): Use Plugin_192021 and generate the S32DS layout. Add Port component and configurate the setting for VirtWrapperSupport (It will need to enable PortMulticoreSupport and dependency modules such as Os, ECuC,...) Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The project running with VirtWrapperSupport enabled in Port component can be generated and built successfully with both below scenarios: # Rm component isn't added # Rm component is added but the RmVirtWrapperConfigurable node isn't enabled Expected behavior: If Port component enables the VirtWrapperSupport, Rm component must be added and RmVirtWrapperConfigurable node must be enabled. Proposed solution optional: Add constrains for Virtual Wrapper feature.
ARTD-16335	Bug	 [adc] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions:

ID	Subtype	Headline and Description
		Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16336	Bug	[base] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16337	Bug	[can] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions:

ID	Subtype	Headline and Description
		Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16340	Bug	[crypto] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16342	Bug	[eth] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions:

ID	Subtype	Headline and Description
		Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16345	Bug	 [gpt] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16299	New	 New Feature [BASE] Update Can_GeneralTypes.h with SWS_CanTrcv_00164 and SWS_CanTrcv_00165 ,,Update Can_GeneralTypes.h with SWS_CanTrcv_00164 and SWS_CanTrcv_00165
ARTD-16346	Bug	 [i2c] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files!

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16352	Bug	[ocu] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16354	Bug	[platform] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files!

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16355	Bug	[port] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16359	Bug	[sai] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files!

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16361	Bug	[spi] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16363	Bug	[uart] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files!

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16364	Bug	[wdg] [EBT] OsApplicationCoreRef and OsAppEcucPartitionRef shall be accessed as parameters<*> Note: This issue is only affecting EBT configuration and source files! Detailed description (how to reproduce it): Our OS stub configuration defined OsAppEcucPartitionRef and OsApplicationCoreRef as lists, but the AUTOSAR specification defines them as optional parameters. We fixed this in the OS module, but now all the other modules that depend on OS to implement multicore features are affected. Preconditions: Create a multicore configuration. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as lists. As a result, the configuration and generation are failing. Expected behavior: OsAppEcucPartitionRef and OsApplicationCoreRef are accessed as parameters. As a result, the configuration and generation are successful. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: # Replace all occurrences of {code}OsApplicationCoreRef/*[1] with {code}OsApplicationCoreRef # Replace all occurrences of {code}OsAppEcucPartitionRef/*[1] with {code}OsAppEcucPartitionRef Warning: Do not forget to adjust relative paths if needed (e.g. in SELECT-expressions).
ARTD-16387	Bug	[crypto] [SWS_BSW_00037] Main functions of un-initialized modules shall return immediately<*> !SWS_BSW_00037.png|width=620,height=100!

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): In Mdl_MainFunction, according to SWS_BSW_00037, if the module is not initialized and the main function is executed then no error shall be reported and the main function shall return immediately. Preconditions: Mdl_MainFunction() is called before Mdl_Init() or Mdl_Init() is called without success. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In case the driver is un-initialized, Mdl_MainFunction() raises a DET error or doesn't return immediately. Expected behavior: In case the driver is un-initialized, Mdl_MainFunction() doesn't raise a DET error and returns immediately. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In the main function(s), check if the module has been initialized and return immediately if not. Don't rely on the values of un-initialized variables (besides the global driver state).
ARTD-16393	Bug	 [fls] [SWS_BSW_00037] Main functions of un-initialized modules shall return immediately<*> !SWS_BSW_00037.png|width=620,height=100! Detailed description (how to reproduce it): In Mdl_MainFunction, according to SWS_BSW_00037, if the module is not initialized and the main function is executed then no error shall be reported and the main function shall return immediately. Preconditions: Mdl_MainFunction() is called before Mdl_Init() or Mdl_Init() is called without success. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: In case the driver is un-initialized, Mdl_MainFunction() raises a DET error or doesn't return immediately. Expected behavior: In case the driver is un-initialized, Mdl_MainFunction() doesn't raise a DET error and returns immediately. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: In the main function(s), check if the module has been initialized and return immediately if not. Don't rely on the values of un-initialized variables (besides the global driver state).
ARTD-16381	New	 New Feature [S32K3XX][S32K3XX] (ITG) Add fault label to support testing side create test fault ,,"NewWorkDescription: The CPXNUM register has 32 bitfields but the actual data value is only 2 bit => The data filed from CPXNUM register is masked before data is recorded by MSCM_CPXNUM_CPN_MASK The value read from the CPXNUM register is always 2 bit, so testing side need a support form driver to check MSCM_CPXNUM_CPN_MASK by add a fault label in driver code.

ID	Subtype	Headline and Description
		Requirement source: Requirement [CPR_RTD_00285]: Before recording the data read from a register, the driver shall filter the value read from the data register clearing all bit values that do not belong in the actual data bitfield. Configured data alignment in the register shall also be considered. (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: after reading the value from the CPXNUM register add fault lable: MCAL_FAULT_INJECTION_POINT(<manual_name>); mask by MSCM_CPXNUM_CPN_MASK Note: MCAL_FAULT_INJECTION_POINT defined in ""Mcal.h"" Eg: !image-2021-09-06-11-00-10-769.png! Change to: !image-2021-09-06-11-01-33-671.png!"
ARTD-16382	Bug	[RM] Diff output CT and EB<*> Detailed description (how to reproduce it): See more pictures in attachment Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: diff output of EB with CT Expected behavior: Same output of EB with CT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Fix for same output between EB and CT !image-2021-09-06-10-37-33-889.png|thumbnail! !image-2021-09-06-10-43-52-052.png|thumbnail! ! image-2021-09-06-10-45-36-157.png|thumbnail! !image-2021-09-06-10-50-48-077.png|thumbnail! !image-2021-09-06-10-58-06-267.png|thumbnail! ! image-2021-09-06-11-00-39-791.png|thumbnail! !image-2021-09-06-11-01-23-997.png|thumbnail! !image-2021-09-06-11-01-52-012.png|thumbnail! ! image-2021-09-06-11-02-30-654.png|thumbnail!
ARTD-16373	Bug	[S32K3XX][I2C][S32CT] do not accept NULL_PTR value in I2c Callback and I2c Error Callback node on S32CT as Ebt<*> Detailed description (how to reproduce it): [...] create a K3XX project on S32DS and add I2c_cdd module. and enable I2c callback and i2c error callback too. Expect: In fields of them don't accept NULL_PTR value as EBT Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] N/A Observed behavior: [...] In fields of them accept NULL_PTR value

ID	Subtype	Headline and Description
		Expected behavior: [...] Expect: In fields of them don't accept NULL_PTR value as EBT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: [...]N/A
ARTD-16375	Bug	[CAN] Ip_Flexcan fails to return out-of-range status / enabled fd / s32k312<*> Detailed description (how to reproduce it): Initialize Flexcan_0/s32k312/IPL with invalid maxmb value: payload 16, maxmb = 43 Verificaition point: FlexCAN_Ip_Init return FLEXCAN_STATUS_BUFF_OUT_OF_RANGE => fail at this step Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_FlexCAN_TC_FCT_2080 Observed behavior: behavior does not match requirement Expected behavior: driver should return out-of-range status Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16402	Bug	[SENT] Fix run fail on sent example<*> Detailed description (how to reproduce it): There are some sent example failed on run Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: All example are passed Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Debug and investigate problem of sent example
ARTD-16399	Bug	[ADC] Update driver according to some requirements with Verification Criteria is "Review" implemented differently ,,"After complete to Review all the requirements with Verification Criteria is ""Review"", I found some requirement implemented different to the expectation due to the description did not match, missing condition to check dependency node, attribute was set to ReadOnly... Check the excel for further information and fixed if needed

ID	Subtype	Headline and Description
ARTD-16405	New	New Feature [BASE] Add new header files for S32K314 and S32K324 ,,"NewWorkDescription: Add new header files for S32K314 and S32K324 Requirement source: RM rev 2 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:"
ARTD-16409	Bug	[ICU][S32K3XX] The function Icu_GetPulseWidth is not working<*> In the function Icu_GetPulseWidth, the sub function Icu_ValidateSignalMeasureWithoutInterrupt is to check the condition of node IcuSignalMeasureWithoutInterrupt, when this node is ON but the macro ICU_GET_PULSE_WIDTH_API guarded to use the function Icu_GetPulseWidth still be STD_OFF. So this function can not be used. !image-2021-09-06-17-12-59-734.png! And the function Icu_GetPulseWidth is misssing the ipw layer function Icu_Ipw_GetPulseWidth. o user can not use it. !image-2021-09-06-17-19-31-292.png!
ARTD-16425	New	New Feature [crypto] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16427	New	New Feature [eth] Review changes according new Header files (S32K314/S32K324, RM Rev.2)"

ID	Subtype	Headline and Description
		,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16430	New	New Feature [gpt] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16431	New	New Feature [i2c] Review changes according new Header files (S32K314/S32K324, RM Rev.2)"

ID	Subtype	Headline and Description
		,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16433	New	New Feature [icu] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16438	New	New Feature

ID	Subtype	Headline and Description
		[platform] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16439	New	New Feature [port] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16443	New	New Feature

ID	Subtype	Headline and Description
		[sent] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16444	New	New Feature [spi] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23 Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16449	New	New Feature

ID	Subtype	Headline and Description

		[base] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=IpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.

ID	Subtype	Headline and Description
		Refer to the implementation example on FLS:* ARTD-15610 Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16450	New	
		New Feature
		
		[platform] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env:
		user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).

ID	Subtype	Headline and Description
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"". Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD. For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers. Refer to the implementation example on FLS:* ARTD-15610 Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16456	New	New Feature
		
		[spi] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:

ID	Subtype	Headline and Description
		Function syntax||Description||Available via void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h 4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM: !image-2021-08-19-09-26-20-823.png|thumbnail! In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466). In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"". Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD. For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers. Refer to the implementation example on FLS:* ARTD-15610 Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16457	New	New Feature
		
		[i2c] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:

ID	Subtype	Headline and Description
		Declare all trusted functions with ""extern"" keyword like: extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector); Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions. 3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support) List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx All functions should be listed out in the table like: Function syntax||Description||Available via void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h 4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM: !image-2021-08-19-09-26-20-823.png|thumbnail! In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466). In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"". Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD. For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers. Refer to the implementation example on FLS:* ARTD-15610 Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16458	New	
		New Feature
		
		[lin] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);

ID	Subtype	Headline and Description

		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16460	New	New Feature [uart] All trusted functions should NOT defined as static or inline functions and should listed out in IM ,,"NewWorkDescription: There are some points that need to be checked in each modules: 1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers. Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params]. Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.

ID	Subtype	Headline and Description

		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env:
		user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610
		Requirement source:
		RTD implementation
		(e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...)
		Proposed solution optional:
		Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16464	New	New Feature

ID	Subtype	Headline and Description

		[rm] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=IpbnNC] to understand more about User mode implementation in RTD.
		For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers.
		Refer to the implementation example on FLS:* ARTD-15610

ID	Subtype	Headline and Description
		Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16466	New	
		New Feature
		
		[adc] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h
		4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM:
		!image-2021-08-19-09-26-20-823.png|thumbnail!
		In order to add this subchapter, there are 2 files added in build_env:
		user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466).
		In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"".

ID	Subtype	Headline and Description
		Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD. For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers. Refer to the implementation example on FLS:* ARTD-15610 Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16476	New	
		New Feature
		
		[icu] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions.
		3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support)
		List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx
		All functions should be listed out in the table like:
		Function syntax||Description||Available via
		void C40_Ip_SetLockProtect(
		C40_Ip_VirtualSectorsType Fls_VirtualSector

ID	Subtype	Headline and Description
		)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h 4. Subchapter ""*User Mode configuration in AutosarOS*"" needs to be added in IM: !image-2021-08-19-09-26-20-823.png|thumbnail! In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466). In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from ""*User Mode support*"" to ""*User Mode configuration in the module*"". Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD. For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers. Refer to the implementation example on FLS:* ARTD-15610 Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"

ARTD-16477	New	New Feature
		
		[ocu] All trusted functions should NOT defined as static or inline functions and should listed out in IM
		,,"NewWorkDescription:
		There are some points that need to be checked in each modules:
		1. All trusted functions should NOT defined as static or inline functions*, so OS Application can be able to call them from outside RTD drivers.
		Check in driver code all IP functions that needs to be called as trusted functions using macros OsIf_Trusted_Call[_Return][1-6params].
		Ensure these functions are defined without ""static"" or ""inline"" keywords, so OS Application can use ""extern"" keyword to declare and call them outside RTD drivers.
		For example:
		a. OsIf_Trusted_Call1param(*Adc_Sar_ClrUserAccessAllowed*, pBase);
		Adc_Sar_ClrUserAccessAllowed() function should be defined without ""static"" or ""inline"" as:
		void Adc_Sar_ClrUserAccessAllowed(const ADC_Type const pBase)
		{
		CLR_USER_ACCESS_ALLOWED((uint32)pBase, SAR_ADC_PROT_MEM_U32);
		}
		b. OsIf_Trusted_Call_Return1param(*C40_Ip_SetLockProtect*, Fls_VirtualSector);
		C40_Ip_SetLockProtect() function should be defined without ""static"" or ""inline"" as:
		C40_Ip_StatusType C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)
		{
		}
		2. Create a new separate header file <IpName>_Ip_TrustedFunctions.h for each IPV has trusted functions, the AutosarOS just needs to include this new header file when user mode is used.
		In <IpName>_Ip_TrustedFunctions.h:
		Declare all trusted functions with ""extern"" keyword like:
		extern void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector);

ID	Subtype	Headline and Description
		Include all header files contain the definition of all types which are used by parameters or return type of those trusted functions. 3. All these trusted functions need to be configured in OS, so they must be clearly listed in the driver IM (chapter 5.7 User Mode Support) List these functions follow guiding mentioned in slide 17 Coding RTD_RunningInUserMode.pptx All functions should be listed out in the table like: Function syntax||Description||Available via void C40_Ip_SetLockProtect(C40_Ip_VirtualSectorsType Fls_VirtualSector)|Set lock bit for flash sectors|C40_Ip_TrustedFunctions.h 4. Subchapter """*User Mode configuration in AutosarOS*""" needs to be added in IM: !image-2021-08-19-09-26-20-823.png|thumbnail! In order to add this subchapter, there are 2 files added in build_env: user_mode_support.dox, user_mode_config_in_autosar_os.dox (added on the ticket ARTD-15466). In module repository, each module needs to rename from user_mode_support*.dox to user_mode_config_in_module*.dox and also its title from """*User Mode support*""" to """*User Mode configuration in the module*""". Please refer the silde [Coding RTD_RunningInUserMode.pptx|https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/General/Zebra%20Training/Coding%20-%20RTD_RunningInUserMode.pptx?d=w21c9578fff794ff387db07a106880274&csf=1&web=1&e=lpbnNC] to understand more about User mode implementation in RTD. For Testing side*: Ensure that we have test scenarios mentioned from slides 22->25 Coding RTD_RunningInUserMode.pptx. Follow slide 23 to ensure we have one test suite to check all trusted functions able to call from outside RTD drivers. Refer to the implementation example on FLS:* ARTD-15610 Requirement source: RTD implementation (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Follow Coding RTD_RunningInUserMode.pptx"
ARTD-16417	Bug	[ICU] There are some issues in ICU module of RTD 1.0.0 CD01.<*> Detailed description (how to reproduce it): The ICU eMIOS channel cannot select bus counter except internal counter as its bus reference. It seems that only PWM eMIOS channel can select global bus counter. !image-2021-09-07-10-04-13-272.png! When ICU eMIOS channel selects internal counter as its bus reference, the IcuEmiosBusRef should be empty, but there will be a warning. !image-2021-09-07-10-08-16-135.png! The ICU module support WKPU NMI (non-Maskable Interrupt). However, if we add an ICU channel using WKPY NMI channel before an other type ICU channel, the declaration of notification function of latter one will not be generated. That will cause errors when compile the generated code. !image-2021-09-07-10-25-33-633.png! !image-2021-09-07-10-29-29-351.png! If the NMI channel is behind the ICU eMIOS channel, the declaration of notification function will be generated normally. !image-2021-09-07-10-37-16-575.png! !image-2021-09-07-10-38-35-320.png! In Icu.c*, the is a *Icu_GetPulseWidth*() API. However, it seems that it cannot be turn on in EB. !image-2021-09-07-10-43-24-862.png! !image-2021-09-07-10-48-08-751.png!

ID	Subtype	Headline and Description
		Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16418	Bug	[FEE] Fee_DeserializeBlockHdr returns wrong block status<*> Detailed description (how to reproduce it): cannot recover all blocks Preconditions: virtual page size = 1, foreign feature is enabled Test Case ID (internal TC that caught the defect) optional: Fee_TS_502 Observed behavior: This function returns wrong block status Expected behavior: all blocks are recovered when invoking Fee_Init Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16448	Bug	[Platform] Investigate cache issues when running multi core tests<*> Detailed description (how to reproduce it): 2 cores will be trapped in Eunit due to cache issue. See more in a picture, !image-2021-09-07-13-02-11-989.png|thumbnail! Preconditions: Enable multi core feature Test Case ID (internal TC that caught the defect) optional: Rm_TC_MUL_0101 Observed behavior: trap in Eunit Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check configuration of MPU in startup
ARTD-16480	Bug	[ETH] Wrong address of DMA channel control registers in Gmac_Ip_Device_Registers.h<*> Detailed description (how to reproduce it): Wrong address of DMA_CHx_CONTROL_ADDR16 in Gmac_Ip_Device_Registers.h Preconditions: NA

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: Eth_TC_FCT_0079 Eth_TC_FCT_0087 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The address of DMA control register should be: #define DMA_CH0_CONTROL_ADDR16 0x1100U #define DMA_CH1_CONTROL_ADDR16 0x1180U
ARTD-16447	Bug	[ICU][CT] There are some text matching problems causing wrong configuration.<*> Detailed description (how to reproduce it): To reproduce this issue, please follow blow steps: Add two ICU eMIOS channels named as *Icu_Channel and *Icu_Channel_Alt* respectively in IcueMios tab. Other names are also possible, but please make sure that the beginning of the second name has the same string as the first name. !image-2021-09-07-13-06-25-911.png! Add two logic channels in IcuChannels tab. The first channel select Icu_Channel_Alt as its reference and work in Signal Measurement mode, and the second channel select Icu_Channel as its reference and work in Edge Detect mode. !image-2021-09-07-13-26-27-384.png! Then, we can generate the configuration code of eMIOS ICU by pushing Update Code. We will find that the second channel is wrongly configured to Signal Measurement mode, not Edge Detect mode. See following picture: !image-2021-09-07-13-32-29-434.png! I think this issue is caused by incorrect text matching. Due to the beginning string of configured channels' names are the same, the Icu_Channel_Alt* will be wrongly regarded as *Icu_Channel when ConfigTools generates code. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16491	Bug	[Spi] On DS can generate LPSPI_TCR_CONT(1) even though SpiCsSelection is disabled<*> Detailed description (how to reproduce it): On DS can generate LPSPI_TCR_CONT(1) even though SpiCsSelection is disabled Preconditions: SpiCsContinous is True SpiCsSelection is disable Code generate LPSPI_TCR_CONT(1)

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16487	New	New Feature [Rm] Remove unused variables in DS generated files ,,"- NewWorkDescription: Some variables get from resource are not use. see picture for more detail. !image-2021-09-07-15-00-06-182.png|width=844,height=289! Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove unused variable"
ARTD-16493	Bug	When PTE13 work as VRC_CTRL, it shouldn't work as other functions ,,"In S32CT, when external BJT is used, the base pin(LMBCTLEN) of the external BJT which generates 1.5V should be enabled in the power module. But when this pin works as VRC_CTRL, it should not be able to set to other function such as GPIO, but in Pins configuration it can still be set to other functions. I think the configuration of the pin PTE13 should be invalid when it works as VRC_CTRL.
ARTD-16623	New	New Feature [icu] Review changes according new Header files (S32K344, RM Rev.2)" ,,"Review changes according to new header files for S32K344 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base: pull-request: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/pull-requests/665/overview] / branch: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/browse?at=refs%2Fheads%2Ffeature%2FARTD-16542-base-update-new-header-files-for-s32k344] Platform tag: PVT_S32K3XX_S32K3_ARTD_16571_V01 Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared

ID	Subtype	Headline and Description
		%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16499	Bug	[S32K3XX][S32K3XX][RTM 1.0.0] Build failed on K312 with GHS with Ip_Clock<*> Detailed description (how to reproduce it): During update test for Timeout test with Counter Type by SYystem_Timer (using CLock initialized by MCU) Build failed found on GHS (either ver 202114 or 202014), on K312 derivative. build failed log on ceram: http://ceram.ea.freescale.net/1/project/ar_int_fls_ghs/details Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Fls_TC_FCT_7000 Observed behavior: N/A Expected behavior: N/A Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16502	Bug	[S32K3XX][i2C]master code of highspeed mode is not correct with i2c protocol<*> Detailed description (how to reproduce it): master code of highspeed mode is not correct with i2c protocol: driver need send 0b00001XXX instead 0b00000XXX. With XXX is high-speed master code Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: master code of highspeed mode is not correct with i2c protocol: driver send 0b00000XXX. Expected behavior: driver send 0b00001XXX Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: N/A
ARTD-16509	Bug	[S32K3XX][S32K3XX_100] compiler warning<*> Detailed description (how to reproduce it): 1. Build project test for platform module by Gcc compiler some warning detect in system_Ip.c Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001

ID	Subtype	Headline and Description
		Observed behavior: N/A Expected behavior: Checking excel file got the station for k344barents.ea.freescale.net/0/project/custom_compilerwarning/details Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16514	New	 New Feature [ICU] Change Process Interrupt function to using "for" instead of using "while"" ,,"NewWorkDescription: ChangeProcess Interrupt function to using "for" instead of using "while" for Siul2 and Wkpu Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA
ARTD-16516	Bug	 [FLS][S32K3XX] Fls_CheckLoadAc condition-check is missing in case Multiple Sectors configured<*> Detailed description (how to reproduce it): During check ccov test hardfault , it showed: Due to LDRA build characteristic: It required to make an custom linker to build acc_code_rom to map to a sector at BLOCK_3, this make sure to test could run with access_code_load to Ram feature without Read-While_Write due to auxiliary files was generated (and mapped to code sectors of Block1) If configures Multiple sector (02 sectors in test case) in boundary location(from BLOCK2_SECTOR_383 the ending sector of Block2): driver shall check the next sector (BLOCK3_SECTOR_384) is satisfied CheckLoadAc() condition and implement load access-code to RAM section, but now, it doesn't. Preconditions: LDRA build run test. Test Case ID (internal TC that caught the defect) optional: Fls_TC_FCT_1000 Observed behavior: hardfault occur due to Read-While-Write condition. Expected behavior: CheckLoadAC shall be ensure such in case multiple sectors configured , especially in Boundary configured use-case (sector from Block1 to Block2, Block2 to Block3, ...) as long as sector to test stays on the same block of AccessCode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16506	Bug	 [UART] Timeout error in function ABORT is raised same as DMA_ERROR<*> Detailed description (how to reproduce it): [Timeout Error in function ABORT is raised same as DMA_ERROR. This is not a clear status. It's confusing in the exact error detection] Preconditions:

ID	Subtype	Headline and Description
		[N/A] Test Case ID (internal TC that caught the defect) optional: [Uart_TC_WBT_0016, Uart_TC_WBT_0017] Observed behavior: [N/A] Expected behavior: [N/A] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-16522	Bug	[S32K3XX][PORT] Generate type Siul2_Port_Ip_PinSettingsConfig missing extern const not according driver<*> Detailed description (how to reproduce it): execute test with Plugin_792021.zip, run test IP_Port_Siul2_TS_002 in IAR compiler Preconditions: the result of this test need to be same IAR, GHS, GCC (GHS, GCC pass) Test Case ID (internal TC that caught the defect) optional: IP_Port_Siul2_TC_0004/IP_Port_Siul2_TS_002 Observed behavior: Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16525	Bug	[ADC] Need to add constraint when AdcConvTimeOnce is enable and container AdcNormalConvTimings is disable<*> Detailed description (how to reproduce it): Need to add constraint when AdcConvTimeOnce is enable and container AdcNormalConvTimings is disable Preconditions: AdcConvTimeOnce is enable Tab Hw unit container AdcNormalConvTimings is disable More detail in attachment Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0001-Adc_TS_009 Observed behavior: AdcConvTimeOnce is enable container AdcNormalConvTimings is disable => Real status: generate pass Expected behavior: Generate fail beacause in this case users can not configure sample time value and what the values in sample time register after calling Adc_Init Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16526	Bug	[ADC] Hard fault error when calling Adc_SetClockMode(ADC_ALTERNATE) with AdcEnableDualClockMode is enable and AdcAlternateConvTimings is disable<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Hard fault error when calling Adc_SetClockMode(ADC_ALTERNATE) with AdcEnableDualClockMode is enable and AdcAlternateConvTimings is disable Preconditions: AdcEnableDualClockMode is enable Tab hw unit container AdcAlternateConvTimings is disable Case 1: AdcConvTimeOnce is enable (Adc_TS_008) Case 2: AdcConvTimeOnce is disable (Adc_TS_009) More detail in attachment Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0002 Adc_TS_008 Adc_TC_FCT_0001 Adc_TS_009 Observed behavior: Calling Adc_SetClockMode(ADC_ALTERNATE) > Real status: Hard fault error in all 2 cases Expected behavior: no hard fault error Case 1: AdcConvTimeOnce is enable > calling Adc_SetClockMode(ADC_ALTERNATE) return e_not_ok or add constraint between AdcEnableDualClockMode and container AdcAlternateConvTimings (Adc_ts_008) Case 2: AdcConvTimeOnce is disable > calling Adc_SetClockMode(ADC_ALTERNATE) return ok because configure in group tab (Adc_ts_009) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16531	Bug	[CRC] The input data changed on IAR compiler is different from generated file<*> Detailed description (how to reproduce it): Initialize CRC module with multicore node is enabled and 2 channels CRC16ARC non-autosar for 2 cores(see Crc.xdm file) Call the Crc_SetChannelCalculate function with CRC16ARC for two cores VERIFICATION_POINT:Data as expected Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Crc_TC_FCT_0716 Observed behavior: The input data changed on IAR compiler is different from generated file(8.50.10 version) compiler(see IAR.png file). On GHS the input data is the same from generated file(see GHS.png file) Expected behavior: The input data is the same from generated file on IAR compiler Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16538	Bug	[SPI]Can not config Tx, Rx, Cs, Clk channel for Flexio, DMA ,,"Detailed description (how to reproduce it): [SPI]Can not config Tx, Rx, Cs, Clk channel for Flexio, DMA Preconditions:

ID	Subtype	Headline and Description
		NA Test Case ID (internal TC that caught the defect) optional: Ip_Flexio_Spi_TS_001, Ip_Flexio_Spi_TS_002, Ip_Flexio_Spi_TS_003 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16544	Bug	[ICU][S32K3XX] Error relating to Emios reference in DS interface ip layer<*> The path to refer to master bus of Emios channel is not working. !image-2021-09-09-11-18-52-970.png!
ARTD-16542	New	New Feature [BASE] Update new header files for S32K344 ,,"NewWorkDescription: Update new header files for S32K344 Requirement source: RM Rev 2 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: N/A"
ARTD-16549	Bug	[S32K312] I3C clock is not enabled on AIPS_0<*> Detailed description (how to reproduce it): [...] Run I3C test on K312 board Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] I3C clock is not enabled in sys_init function. Expected behavior: [...] I3C clock is enabled in sys_init function. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...] Change value of PRTN0_COFB1_CLKEN_REQ_MASK_U32 to 0x000137DFU
ARTD-16548	Bug	[ADC] "Adc Optimize DMA Streaming Groups" is still EDITABLE when "Adc Enable DMA support" is disabled

ID	Subtype	Headline and Description
		,,"Detailed description (how to reproduce it): This node ""AdcOptimizeDmaStreamingGroups"" is EDITABLE still when ""Adc Enable DMA support"" is disabled Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_001_cfg2 Observed behavior: This node ""AdcOptimizeDmaStreamingGroups"" is EDITABLE still when ""Adc Enable DMA support"" is disabled Expected behavior: This node is EDITABLE only if ""Adc Enable DMA support"" is enabled. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16569	Bug	[S32K3][S32DS][OCU] Incorrect behavior in OcuHWSpecificSettings<*> Detailed description (how to reproduce it): Create a project for S32K312 and add OCU (HL) or Emios_OCU(IP) component into the project, Add and configure channel 1 and channel 10 In OcuHWSpecificSettings, change channel 1's OcuEmiosBusSelect to each of the Counter Bus change channel 10's OcuEmiosBusSelect to each of the Counter Bus Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Ip_Emios_TS_001 Observed behavior: When both channel 1 and channel 10 are in the configuration, changing channel 1's OcuHWSpecificSettings does make any change to it's generated configuration, both in Code Preview and the generated file after updating code. See picture below !image-2021-09-09-15-36-25-337.png|thumbnail! However, changing channel 10's OcuHWSpecificSettings will make changes for both channel 1 and channel 10 !image-2021-09-09-15-40-56-461.png|thumbnail! !image-2021-09-09-15-42-52-049.png|thumbnail! This behavior will persist if settings for channel 1 and channel 10-19 exist in the same configuration. It will cease if there's only channel 1. This apply to channel 2 and channel 20-23 Expected behavior: Changing settings for a specific channel should not affect the other
ARTD-16571	New	New Feature [platform] Review changes according new Header files (S32K314/S32K324, RM Rev.2)" ,,"Review changes according to new header files for S32K314 and S32K324 Update drivers (if needed) Remember to update on UM/ IM in quality documentation ticket Reference: Base tag: *PVT_BASE_S32K3_1.0.0_V23

ID	Subtype	Headline and Description
		Base commit: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/commits/91fb682863c2717eba1fc8e0135cbf9f7549a5f6] Reference Manual document: S32K3xx Reference Manual, Rev. 2, 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM%2FS32K3xx%5FRM%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FRM] S32K3xx Data Sheet, Rev. 2 - 08/2021, [Link|https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?originalPath=aHR0cHM6Ly9ueHAxLnNoYXJlcG9pbnQuY29tLzpmOi9zL1plYnJhL0V1ZWNqSGJPX3%5FcnRpbWU9YXBPTHkxUXAyRWc&id=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS%2FS32K3xx%5FDS%5FRev2%2Epdf&parent=%2Fsites%2FZebra%2FShared%20Documents%2FDocuments%2FPlatforms%2FS32K3xx%2FDS]
ARTD-16574	Bug	[S32K3 RTM] OCU: EB generate code not corect<*> Detailed description (how to reproduce it): Tag: OCU_110 Branch: develop When code generate from EB, OcuPrescale_Alternate value generated is not correct Test Case ID (internal TC that caught the defect) optional: Ocu_TC_FCT_219 in Ocu_TS_101 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-16572	New	New Feature [S32CT][ECPD] Create a "literals" option for enumerations represented by dynamic_enums" ,,"NewWorkDescription: Create a "literals" option for enumerations represented by dynamic_enums. If it exists, then the values for the ECUC-ENUMERATION-LITERAL-DEF nodes will be taken from this option. Otherwise, the values will be taken from the "items" expression of the dynamic_enum. This option represents a list of "fallback" values. Update the following presentation: https://nxp1.sharepoint.com/:p:/r/sites/Zebra/Shared%20Documents/Configuration%20(code,%20DS,%20EB,%20etc)/NXP_RTD_AUTOSAR_S32CT_V2.pptx?d=w28a51ba3c45240f5abb6a6933671dcd3&csf=1&web=1&e=s8y7Hc Requirement source: N/A (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update generateEcpd.js to implement the described behaviour.
ARTD-16573	Bug	[S32K3XX] Compilation failed on S32K314<*> Detailed description (how to reproduce it): Compilation failed on S32K314 due to undeclared variable.

ID	Subtype	Headline and Description
		c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K314_gcc/adc/../../eclipse/plugins/Platform_TS_T40D34M10I0R0/startup/src/system.c: In function 'SystemInit': c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K314_gcc/adc/../../eclipse/plugins/Platform_TS_T40D34M10I0R0/startup/src/system.c:421:32: error: 'MSCM_IRSPRC_M7_1_SHIFT' undeclared (first use in this function); did you mean 'MSCM_IRSPRC_M7_0_SHIFT'? 421 coreMask = (1UL << MSCM_IRSPRC_M7_1_SHIFT); MSCM_IRSPRC_M7_0_SHIFT c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K314_gcc/adc/../../eclipse/plugins/Platform_TS_T40D34M10I0R0/startup/src/system.c:421:32: note: each undeclared identifier is reported only once for each function it appears in Makefile:1041: recipe for target `system_c.o' failed Preconditions: Build a project. Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Compilation error. Expected behavior: No compilation error. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16638	Bug	[Uart] Callback for Dma transfer should be enable for using<*> Detailed description (how to reproduce it): [...] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16684	Bug	[CRYPTO] Key derivation service fills wrong descriptor parameter<*> Detailed description (how to reproduce it): Wrong descriptor parameter is used when X963 key derivation is requested. The bug is cosmetic because the descriptor parameter that is currently used has the same type as the descriptor parameter to be used. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: The derivation service is filling the descriptor for X963 with a hash used as pseudo random function in the {{hmacHash}} instead of hash}} parameter.

ID	Subtype	Headline and Description
		Expected behavior: The X963 derivation function supports only hash as pseudo random function: !image-2021-09-10-16-08-16-808.png! Because a generic type ({{hseKdfCommonParams_t}}) is used for multiple KDFs, there are more parameters than needed for X963. !image-2021-09-10-16-11-47-908.png! Even if the current code works, because the prfAlgo}} is a union and hmacHash}} has the same type as hash}}, see picture below, the code should be updated to use the right parameter hash}}. !image-2021-09-10-16-13-54-928.png! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Swap the parameter hmacHash}} with hash}}.
ARTD-16650	New	 New Feature [ICU][S32K3XX] Add file version checking ,,"NewWorkDescription: Add file version checking. Attach file shown files version have not checked yet. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16647	New	 New Feature [RM] Update driver follow update from requirements ,,"NewWorkDescription: Some requirements are updated. code need to be updated as well Ticket: AAI-940 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-16648	New	 New Feature [FLS] Update code following to Rule 29 of Naming Convention ,,"NewWorkDescription: Update local variables, function parameters and struct members using only PascalCase naming, without any special prefix Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16659	Bug	 [ICU][S32K3XX] Bug directive position wrong<*> Detailed description (how to reproduce it): #endif directive position is wrong in Icu_Ipw.h

ID	Subtype	Headline and Description
		!image-2021-09-10-11-51-04-365.png|width=789,height=441! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16667	Bug	[ICU] Update and Fix after review code / design checklist<*> Detailed description (how to reproduce it): Perform review UML design/ code review against checklist. The UML checklist/ code review template and guideline are enclosed in the attachment. Preconditions: Check and update code if have violation Test Case ID (internal TC that caught the defect) optional: N/a Observed behavior: N/a Expected behavior: all violation has update Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/a
ARTD-16677	Bug	[ADC] Tresos identifier "New Data DMA enable mask(dynamic range)" can't be configured. ,,"Detailed description (how to reproduce it): [The Tresos identifier ""New Data DMA enable mask(dynamic range)"" in Adc component can't be configured, and I did not find any option to enable this configuration.] Preconditions: [Enable DMA operation when new data is available in ADCnDR register of BCTU module.] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [The Tresos identifier ""New Data DMA enable mask(dynamic range)"" in Adc component can't be configured] Expected behavior: [The Tresos identifier ""New Data DMA enable mask(dynamic range)"" in Adc component can be modified] !Capture.PNG! Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		[...]
ARTD-16687	Bug	[PWM] Emios_Pwm_Ip_SyncUpdate does not sync the master buses<*> Detailed description (how to reproduce it): As part of the CPR_RTD_00511.mcl MCL requirement for synchronously updating the channels and master buses. The PWM is responsible for resetting the OUDIS bit for the master buses that it controls as well. Looking at the Emios_Pwm_Ip_SyncUpdate function code, the master buses are not cleared along with the channels. No specific section for master bus search is present and master buses are not added to Emios_Pwm_Ip_aCheckState to be able to appear in the final mask variable. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: Emios_Pwm_Ip_SyncUpdate at the end of the function both pwm channels and corresponding master busses OUDIS bits are cleared. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: At init add the master bus of channels that use it and have pwm exclusive access enabled as initialized in the Emios_Pwm_Ip_aCheckState Or when looping through all the channels of the instance, when encountering a channel type that uses the master buses, check the master bus also
ARTD-16689	New	New Feature [MCL][Emios] Extend the requirement(s) for SyncUpdate ,,"NewWorkDescription: In order for the PWM to fully implement the synchronous update of the channels parameters an update needs to be done in MCL Emios. The problem is as follows. The user updates the master bus period using Mcl_Emios_SetCounterBusPeriod with syncUpdate=TRUE. After that updates the needed chanels dutyCycle as desired using syncUpdate=TRUE as well. At the end PWM_Sync is called and all the channels should update at the next reload point. This has a problem as the dutyCycle value is computed based on the master bus period, which is not yet updated in the register at the time. The MCL should add a new API in IPL to allow the PWM to read most updated master bus value. For this the master bus periods should be kept internal to the driver and updated every time a new value is written the register as well. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Add a global variable for storing the master bus periods. At every point where the period register is written, the global variable should be updated as well. Add a new API uint16 Emios_Mcl_Ip_GetCounterBusPeriod(uint8 hwInstance, uint8 hwChannel) that will return the period of the master bus form the global variable."

ID	Subtype	Headline and Description
ARTD-16691	New	New Feature [PWM][EMIOS] Update Emios_Pwm_Ip_GetCounterBusPeriod ,,"NewWorkDescription: As described in ARTD-16689 the MCL will add a new API to get the updated master bus period. Update all Emios_Pwm_Ip_GetCounterBusPeriod instances to the new MCL API to always get the updated period. Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-16696	Bug	[MCL] Compiler warning report has some warnings with Emios Ip<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Compiler warning report has some warnings(pls see attached file) Expected behavior: Compiler warning report no warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16704	New	New Feature [GPT] Different declaration of functions in ReqExport and header files ,,"NewWorkDescription: List function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code: void Gpt_SetMode(Gpt_ModeType Mode) void Gpt_Notification_(void) void Pit_Ip_Init(uint8 instance, const Pit_Ip_InstanceConfigType const config) Pit_Ip_StatusType Pit_Ip_InitChannel(uint8 instance, const Pit_Ip_ChannelConfigType chnlConfig) void Pit_Ip_StopChannel(uint8 instance, uint8 channel, uint32 countValue) uint64 Pit_Ip_GetLifetimeTimerCount(uint8 instance) void Rtc_Ip_Init(uint32 instance, const Rtc_Ip_ConfigType const initConfig) void Rtc_Ip_Deinit(uint32 instance) void Rtc_Ip_StartCounter(uint8 instance, uint32 value) Rtc_Ip_StatusType Rtc_Ip_SetTimeDate(uint8 instance, Rtc_Ip_TimedateType const timeDate) Rtc_Ip_StatusType Rtc_Ip_ConfigureAlarm(uint8 instance, Rtc_Ip_AlarmConfigType const alarmConfig) void Rtc_Ip_ConvertSecondsToTimeDate(uint32 const seconds, Rtc_Ip_TimedateType const timeDate) void Rtc_Ip_ConvertTimeDateToSeconds(Rtc_Ip_TimedateType const timeDate, uint32 const seconds) void Rtc_Ip_StopCounter(uint8 instance)

ID	Subtype	Headline and Description
		void Stm_Ip_StartCounting(uint8 instance, uint32 channel, uint32 compareValue) void Stm_Ip_SetClockMode(uint8 instance, prescalerModeType prescalerMode) void Emios_Gpt_Ip_SetClockMode(uint8 instance, uint8 channel, prescalerModeType prescalerMode) Please see in attach file Requirement source: ReqExport.txt (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Check function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code"
ARTD-16707	Bug	[S32K3][CRYPTO] Fix findings after code review<*> Detailed description (how to reproduce it): Deviation from code guideline: Check attached excel, "Detailed_Findings" tab. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Deviation from code guideline for rules: 6, 10, 19, 22, 23, 24, 29, 37, 43, 45, 46, 47, 85, 110 more detail check attached file, "Detailed_Findings" tab. Expected behavior: All findings are fixed. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16709	Bug	[SENT] Generated code on S32CT and EBT are different<*> Detailed description (how to reproduce it): During comparation the generated code on EBT and S32CT, I saw that there are many differences between them. Please take a look the compare_output_files.docx and generated files in attached file for more detail. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: header files, src files generated by EBT and CT should be the same. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16724	Bug	[ADC] Not return warning error when DMA channel be shared among configurations<*> Detailed description (how to reproduce it): When using the same DMA channel for configurations, it does not give an error warning.

ID	Subtype	Headline and Description
		Configure ADC module select DMA channel (node: AdcDmaChannelId): dmaLogicChannel_Type_0 Configure CTU FIFO select DMA channel (Node: BctuFifoDmaChannelId): dmaLogicChannel_Type_0 Preconditions: Use EB Tresos. Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0701 of Adc_TS_012_cfgdma Observed behavior: When using the same DMA channel for configurations, it does not give an error warning Expected behavior: When using the same DMA channel for configurations, it does give an error warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16727	Bug	[RM] Fix Compiler Warning<*> Detailed description (how to reproduce it): Fix compiler warning > see more details in attachment Preconditions: Build all tests Test Case ID (internal TC that caught the defect) optional: all test cases Observed behavior: compiler warning Expected behavior: no compiler warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: fix compiler warning
ARTD-16728	Bug	[ADC] There is some information that does not match EB and S32CT when comparing code generation<*> Detailed description (how to reproduce it): Step 1: clean generate Adc_TS_COT_001 for EB and Adc_TS_COT_101_CT for CT Step 2: Compare include folder and src folder of S32CT with EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing code generation. Detail in share point link: [https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/Forms/AllItems.aspx?RootFolder=%2Fsites%2FZebra%2FShared%20Documents%2FGroup%204%2FEBvsS32CT%2FADC] File: "Compare Config S32CT and EB Tresos_EPC_S32K3xx.xlsx" Expected behavior: EB and S32CT need to generate the same file. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: [...]
ARTD-16731	Bug	[Uart] Uart_apConfig and Uart_Ipw_apChnConfig should'nt be NULL if driver is not de-initialized successfully<*> Detailed description (how to reproduce it): [Uart_apConfig and Uart_Ipw_apChnConfig should be kept values if driver is not de-initialized successfully. Driver should check status return by IPL layer !image-2021-09-13-17-56-03-969.png|width=303,height=130! !image-2021-09-13-17-57-26-625.png|width=305,height=112!] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [N/A] Observed behavior: [N/A] Expected behavior: [Driver should check status return by IPL layer] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-16733	Bug	[Uart] Lpuart_Uart_Ip_Deinit only check LPUART_UART_IP_TX_COMPLETE<*> Detailed description (how to reproduce it): [Currently function Lpuart_Uart_Ip_Deinit only check LPUART_UART_IP_TX_COMPLETE before implement de-initialize. Need to mention reception status. !image-2021-09-13-18-31-44-015.png|width=416,height=168!] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [Review] Observed behavior: [N/A] Expected behavior: [Before de-initialization, driver should mention both Tx and Rx status] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-16735	Bug	[RM] Typo in macro definitions with XRDC GVLD bit<*> Detailed description (how to reproduce it): There is a typo in definition of XRDC GVLD bit macros (GLVD used instead of GVLD): #define XRDC_CR_GLVD_MASK ((uint32)0x00000001UL) #define XRDC_CR_GLVD_ENABLE ((uint32)0x00000001UL) #define XRDC_CR_GLVD_DISABLE ((uint32)0x00000000UL) Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A

ID	Subtype	Headline and Description
		Observed behavior: The name of GVLD bit is not the same as defined in reference manual. Expected behavior: The name of GVLD bit is the same as defined in reference manual. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Modify the above definitions to be as follows (GLVD replaced by GVLD in the macro names): #define XRDC_CR_GVLD_MASK ((uint32)0x00000001UL) #define XRDC_CR_GVLD_ENABLE ((uint32)0x00000001UL) #define XRDC_CR_GVLD_DISABLE ((uint32)0x00000000UL) Plus modify all these macros where used in code.
ARTD-16758	Bug	 [S32K3 RTM] OCU: Ocu_SetClockMode can't set for channel if channel used mater bus<*> Detailed description (how to reproduce it): Tag: OCU_112 Branch: develop When config channel in EB, we choose channel used materbus. But call Ocu_SetClockMode function driver intervened for channel register Test Case ID (internal TC that caught the defect) optional: OCU_TC_FCT_0219 in Ocu_TS_101 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16740	New	 New Feature [SPI] Improve DMA mode to increase the performance ,,"NewWorkDescription: DMA mode is taking more CPU load so it should be improved as proposal in ticket: AAI-946 Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: 1. Add a new feature to support to configure 1 DMA channel (TX/RX) per transmit. 2. Move all TCD elements reconfigure which is constant to Init function. For detail: see AAI-946"
ARTD-16753	New	 New Feature [ICU] verify test example ,,"NewWorkDescription: need to re-check generate, build for test example for release Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:

ID	Subtype	Headline and Description
		[...]"
ARTD-16761	Bug	[S32K3XX][Crypro] Hse Ip generates the incorrect Hse.ecvd file<*> Detailed description (how to reproduce it): 1*. Modify line 512 in "mcu_data/components/PlatformSDK_S32K3_2021_09/system/codegenerator.js" as follows: !image-2021-09-14-11-35-09-510.png! This ensures that the ECPD is generated only for Hse Ip 2. Create a project in S32DS and add Hse Ip. Then generate Hse.ecvd file and Hse_s32k344_257bga.ecpd file. These files are attached. 3. This is generated Hse.ecvd file !image-2021-09-14-11-36-29-777.png! I see that SHORT-NAME is Crypto. This leads to import fail Hse.ecvd file to EB tresos if I don't enable path mapping and automatically caculated path mapping !image-2021-09-14-11-40-21-245.png! If I enable 2 these buttons, EB will automatic calculate path mapping and this file will be import successfully. But this leads to test fail automation with makefile. !image-2021-09-14-11-11-50-398.png! 4. I have try changing Crypto become Hse in Hse.ecvd file, and This is success for both manual and automatic test. Preconditions: tag CRYPTO_082 Test Case ID (internal TC that caught the defect) optional: Ip_Hse_TS_COT_001.mak Observed behavior: Importing fail Hse.ecvd file to EB tresos if we don't enable path mapping and automatically caculated path mapping buttons. Expected behavior: Importing success Hse.ecvd file to EB tresos if we don't enable path mapping and automatically caculated path mapping buttons. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: File generated Hse.ecvd file : Crypto > Hse in line 8
ARTD-16805	Bug	[LIN][LPUART] Report LIN_ERR_HEADER to LinIf when a frame error occurs in the header part of the frame<*> Detailed description (how to reproduce it): Driver is missing LIN_ERR_HEADER report to LinIf when a frame error occurs in the header part of the frame Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16814	Bug	[UART] Remove duplicate callback name if user configured with same name<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		If user config 1 callback name for 2 or more channel of Uart, duplicate name will happen !image-2021-09-14-23-12-45-227.png|thumbnail! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Remove duplicate callback name if user configured with same name Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16817	Bug	 [Wdg] There is some information that does not match EB and S32CT when comparing code generation<*> Detailed description (how to reproduce it): Step 1: clean generate Wdg_TS_COT_001 for EB and Wdg_TS_COT_101 for CT on S32K324 Step 2: Compare include folder and src folder of S32CT with EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: There is some information that does not match EB and S32CT when comparing code generation. There is issue at generate code on CT. When configuring Multicore node = ON but CORE ID is still 0xFFFF !image-2021-09-15-09-30-53-030.png! Detail in *share point link*: https://nxp1.sharepoint.com/:x:/r/sites/Zebra/_layouts/15/Doc.aspx?sourcedoc=%7BB20CD393-7B19-4F45-9E5A-CE2632F02AD3%7D&file=Wdg_Compare%20Config%20S32CT%20and%20EB%20Tresos.xlsx&action=default&mobileredirect=true Expected behavior: EB and S32CT need to generate the same file. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16819	Bug	 [RM] Update examples follow update from dependent drivers<*> Detailed description (how to reproduce it): Generate fail example on EB Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Generate fail example on EB Expected behavior: gen build run success example

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update configuration for dependent driver as Platform
ARTD-16831	Bug	 [LIN] Failure at generating on S32DS<*> Detailed description (how to reproduce it): Open S32DS and error log(see attached file) !image-2021-09-15-15-15-00-517.png|thumbnail! Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Can not generate code on S32DS due to LIN module Expected behavior: Can generate code on S32DS Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-16833	New	 New Feature [RM][S32K3XX] Fix misra violations ,,"NewWorkDescription: Misra rule 10.8 violations appeared after updating header files and needed to be checked Reduce rule 2.5 violations Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16838	Bug	 [CRC] No error observed when CrcEnableUserModeSupport is enabled and undefined MCAL_ENABLE_USER_MODE_SUPPORT<*> Detailed description (how to reproduce it): N/A Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Crc_TC_COT_0001.c Observed behavior: No error observed when CrcEnableUserModeSupport is enabled and undefined MCAL_ENABLE_USER_MODE_SUPPORT Failure at building IAR compiler Missing Crc_Ip_CfgDefines.h in Crc_Ip_TrustedFunctions.h file Expected behavior: Error observe when CrcEnableUserModeSupport is enabled and undefined MCAL_ENABLE_USER_MODE_SUPPORT Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: 1. Include "Mcal.h" file into Crc_Ip_Types.h Swap "Mcal.h" position with "Crc_Ip_CfgDefines.h" 2. Add prototype for SpecificSetUserAccessAllowed function
ARTD-16841	Bug	[Rm] Rm_pConfig is allocated to wrong section<*> Detailed description (how to reproduce it): N/A Preconditions: Run with precompile option Test Case ID (internal TC that caught the defect) optional: Fee_TS_191 Observed behavior: This variable is not cleared before the init function is called Expected behavior: this is cleared to NULL_PTR Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: allocate to SEC_VAR_CLEARED_UNSPECIFIED
ARTD-16843	Bug	[SAI] Generated code mismatch between EB and CT<*> Detailed description (how to reproduce it): Generate code with EBtresos Import EPC to S32DS and generate code Compare generated code between DS and EB Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Sai_TS_200 Observed behavior: Different in *Sai_Ip_VS_0_PBcfg.c*: Missing type of member (See detail in below image) Different in *CDD_Sai_VS_0_PBcfg.c*: Still have ".member" in struct (See detail in below image) Expected behavior: Generated code between EB and CT should be mapping Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16846	Bug	[ADC] Build fail: "implicit declaration of function 'Adc_ReportDetError'" when AdcHwTriggerApi is enable and AdcDevErrorDetect is disable ,,"Detailed description (how to reproduce it): Build fail: ""implicit declaration of function 'Adc_ReportDetError'"" when AdcHwTriggerApi is enable and AdcDevErrorDetect is disable Preconditions: AdcHwTriggerApi is enable and AdcDevErrorDetect is disable Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Adc_TS_COT_011 cfg 10 Observed behavior: Build fail log: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M10I0R0/src/Adc.c: In function 'Adc_CheckSetChannelCtuTriggers': STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M10I0R0/src/Adc.c:3466:13: error: implicit declaration of function 'Adc_ReportDetError'; did you mean 'Det_ReportError'? [-Werror=implicit-function-declaration] STDERR: 3466 Adc_ReportDetError(ADC_SETCHANNEL_ID, (uint8)ADC_E_PARAM_GROUP); Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16847	Bug	[BASE] Build failed with AutosarOs<*> Detailed description (how to reproduce it): [BASE] Build failed with AutosarOs OsIf_Cfg.c: OsCounter_0{color:#de350b}*U Os_cfg.h: OsCounter_0 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Observed behavior: Expected behavior: Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16867	Bug	[SENT] Fix compiler warnings<*> Detailed description (how to reproduce it): compiler warning report is generated at here: [http://flores.ea.freescale.net/0/project/custom_compilerwarning/20210915111230923000/details] Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-16871	Bug	[RM] Missing validate in configurating PFlash on DS<*> Detailed description (how to reproduce it): Enable Pflash but not configurate it => Generate an array with 0 element => Build fail.

ID	Subtype	Headline and Description
		Please fix both HLD and IP. Preconditions: Enable Pflash in DS Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16874	Bug	 [UART] Specific header file wasn't included separatetly for S32K3xx derivatives<*> Detailed description (how to reproduce it): Specific header file wasn't included separatetly for S32K3xx derivative in generated files that lead to failed at build step. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Header files should be added individually for each S32K3xx derivative. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16887	New	 New Feature [SENT] Change implementation of SENT when using DMA to improve the performance ,,"NewWorkDescription: Currently, Sent implementation needs interrupt for every frame (DMA interrupt with DMA mode), so it's not good performance Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Try to use interrupt once when at end of frame when using DMA mode"
ARTD-16880	Bug	 [S32K3 RTM] FLS: Missing fls user mode check when defined MCAL_ENABLE_USER_MODE_SUPPORT<*> Detailed description (how to reproduce it): 1. enable fls user mode and not define MCAL_ENABLE_USER_MODE_SUPPORT 2. disable fls user mode and define MCAL_ENABLE_USER_MODE_SUPPORT No error generated in both case. Observed behavior: No error generated in both above case. Expected behavior: An error will generated in both above case. Proposed solution optional:

ID	Subtype	Headline and Description
		[...]
ARTD-16882	Bug	[Uart][FLEXIO] FlexIO missing enable error shifter when DMA using<*> Detailed description (how to reproduce it): [FlexIO missing enable error shifter when DMA using] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [Uart_TS_0014] Observed behavior: [N/A] Expected behavior: [N/A] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [N/A]
ARTD-16891	New	New Feature [FLS][S32K3 1.0.0] Remove unused Qspi resources ,,"NewWorkDescription: There are some unused Qspi stuffs that should be removed from the driver code: QSPI_IP_READ_MODE_INTERNAL_DQS and QSPI_IP_READ_MODE_LOOPBACK_DQS FlsQspiSectorCh node configuration FlsHwUnitPageProgramBoundary* node configuration Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16930	Bug	[ADC]Content of example description is incorrect<*> Step: 1.Import all ADC example projects for S32K3: 2. Open description.txt then check content Observed behavior: Content of description isn't correctly, debugger not support for S32K3 Configuration Name Description $(example)_debug_ram_{color:red}s32debugger Debug the RAM configuration using{color:red} S32 Debugger $(example)_debug_flash_{color:red}s32debugger Debug the FLASH configuration using S32 Debugger Expected behavior: Content of description should be updated correctly with PE micro debugger
ARTD-16932	Bug	[S32K3xx][Crypto] Content of description is incorrectly<*> Step: 1.Import all Crypto example projects for S32K3: 2. Open description.txt then check content Observed behavior:

ID	Subtype	Headline and Description
		Content of description isn't correctly, debugger not support for S32K3 Configuration Name Description $(example)_debug_ram_{color:red}s32debugger Debug the RAM configuration using{color:red} S32 Debugger $(example)_debug_flash_{color:red}s32debugger Debug the FLASH configuration using S32 Debugger Expected behavior: Content of description should be updated correctly with PE micro debugger
ARTD-16926	Bug	[RTD_4.4_S32K3x_1.0.0] Warning "Invalid project path: Missing project folder or file: \...\include for Source path" displayed after detach RTD for NPW project ,," Install S32DS 3.4 SP2.EAR1 release and S32K3XX_RTD_4_4_RTM_1_0_0_DS_updatesite_2109_RC4.zip Test Case: # Create NPW for S32K3XX enable RTD 1.0.0 # Select project > SDKs > Detach RTD 1.0.0 # Check Problem view Observed behavior: There is a warning message displayed: ""_*Invalid project path: Missing project folder or file: \\{project_name}\include for Source path*_"" after detach RTD 1.0.0 Expected behavior: No warning message displayed
ARTD-16927	Bug	[I2c] Fix driver build fail with iar when use dma<*> Detailed description (how to reproduce it): [...] Fix driver build fail with iar when use dma for both lpi2c and flexio !image-2021-09-17-14-46-56-600.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16941	Bug	[I2c] There isn't description with some example project I2C<*> Step: 1. File > New > S32DS project from example 2. Select all I2c example projects for S32K3> check description.txt I2c_IP_HLD_FLEXIO_Transfer_S32K312/S32K344 I2c_IP_HLD_LPI2C_Transfer_S32K312/S32K344 Observed behavior: There is no description Expected behavior: Should add description

ID	Subtype	Headline and Description
ARTD-16947	New	New Feature [FLS][S32K3 1.0.0] Remove unused configurations ,,"NewWorkDescription: There are some unused configurations and macros that should be removed or hidden from the driver code: FlsAbortOwnedDomainsTimeout and its macro *FLS_ABT_DOMAINS_TIMEOUT FlsMCoreBusyWaitTimeout FlsProtection Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-16949	Bug	[SENT] DMA buffer depth feature was not implemented<*> Detailed description (how to reproduce it): [...] Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16952	Bug	[S32K3] CRYPTO DS examples cannot run with FLASH target<*> Detailed description (how to reproduce it): Crypto DS examples cannot run with FLASH target due to HSE disabled default configuration, while the user can select an alternative FLASH programming algorithm within Advanced Options dialog. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Crypto DS examples cannot run with FLASH target. Expected behavior: Crypto DS examples can run with FLASH target. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-16974	Bug	[S32K3XX][I2C]fix warning - genfail - run fail on example of I2C<*> Detailed description (how to reproduce it): [...]

ID	Subtype	Headline and Description
		Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] fix all warning of EBT example, and run fail on k312 Expected behavior: [...]alll examples run normally and have no warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) N/A Proposed solution optional: [...]N/A
ARTD-16995	Bug	 [LIN] [DS] Missing to set default for some node in template file<*> Detailed description (how to reproduce it): Some nodes in template file don't set to default value to NULL_PTR as: LinLpuartStartTimerNotification LinLpuartStopTimerNotification LinFlexioStartTimerNotification LinFlexioStopTimerNotification Update max value to 160MHz for LinClockRef node Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17012	New	 New Feature [FLS] Update Fls_DataAddressType to fix Misra 11.6 ,,"NewWorkDescription: Fix Misra 11.6 ""A cast should not be performed between pointer to void and an arithmetic type."" Requirement source: Misra 2012 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Update Fls_DataAddressType to uint32 to avoid conversions from pointer to void to uint32."
ARTD-17018	Bug	 [Uart] HLD Transmit and Receive functions need to check both receive and transmit status for reporting det error<*> Detailed description (how to reproduce it): [...]

ID	Subtype	Headline and Description
		Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17021	Bug	[ICU][S32K3XX] Fix warning of example and update add example for S32K312<*> Detailed description (how to reproduce it): Have a warning when build with EB example for S32K344, but it is related to Platform module. Update example for S32K312 and additional example with all IPV for S32K344. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17023	Bug	[Uart] Compiler warning S32K3<*> Detailed description (how to reproduce it): [Compiler warning exists in driver] Preconditions: [N/A] Test Case ID (internal TC that caught the defect) optional: [None] Observed behavior: [None] Expected behavior: [No Compiler warning] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [None]
ARTD-17025	Bug	[RM] Mpu M7 : Wrong validation in calculating Region Size<*> Detailed description (how to reproduce it): Wrong calculated Region Size in Mpu M7 => Import or create new project which using Mpu M7 become fail. Please check both HLD and IP. Preconditions:

ID	Subtype	Headline and Description
		[...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Check validation in Rm.component and Mpu_M7.component
ARTD-17026	Bug	 [SENT] Some requirements are not fully covered<*> Detailed description (how to reproduce it): There are some requirement have been added, some of them aren't fully covered by SENT driver. SWS_CDD_Sent_00057, SWS_CDD_Sent_00058, SWS_CDD_Sent_00059 Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: SWS_CDD_Sent_00057 and SWS_CDD_Sent_00059: only ignoring the entire message, not declaring to user that these errors have occurred. SWS_CDD_Sent_00059: Get all msg functions are using detecting timeout from each channel, so timeout expire case only occur when last channel has timeout error Expected behavior: Follow the requirement Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Using a user notification to inform to user when any above error occurred
ARTD-17031	Bug	 [I2c] Ip Flexio can not transfer when use interrupt<*> Detailed description (how to reproduce it): [...] Ip Flexio can not transfer when use interrupt, the test is blocking in this funcition !image-2021-09-21-14-26-43-518.png! !image-2021-09-21-14-27-28-158.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Ip_Flexio_ts_200 Observed behavior: [...] Ip Flexio can not transfer when use interrupt Expected behavior: [...] Ip Flexio can transfer when use interrupt Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-17050	Bug	[UART] ECPD generate fail for HLD layer<*> Detailed description (how to reproduce it): ECPD generate fail for HLD layer NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: ECPD generate success for HLD layer Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17055	Bug	[I2c] Fix build fail example after update template file on DS<*> Detailed description (how to reproduce it): [...] Fix build fail example after update template file on DS Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17061	Bug	[S32K3XX 4.4] OCU: Clock prescale of internal counter incorrect<*> Detailed description (how to reproduce it): The channel divider uses an internal counter of DIV_1, but when debugging it is DIV_4 Preconditions: The channel using internal counter Test Case ID (internal TC that caught the defect) optional: Ocu_TS_101 Observed behavior: Prescale of internal counter is wrong when debugging Expected behavior: Prescale of internal counter is correct when debugging Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17065	Bug	[S32K3XX][S32K3xx_100] import ecpd from CT to EB fail<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		follow ARTD-15711 ticket generate ecpd from s32ct. on s32ct create new project then add IntCtrl_Ip for project, after that export ecpd file and ecvd from s32ct. Open EB and create new project with plugin _*[^Ip_TS_T40D34M10I0R0.zip]*_ to project, then import ecvd gene rate from s32ct. Preconditions: follow ARTD-15711 ticket Test Case ID (internal TC that caught the defect) optional: Ip_Platform_TS_COT_001 Observed behavior: missing opption on eb !image-2021-09-22-17-35-06-172.png! 2. Compare file generate by EB on CT have some ! image-2021-09-22-17-38-18-269.png! Expected behavior: Add more opption on EB Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-17066	New	 New Feature [PORT] Remove the PTA24 from S32K3x4_172mqfp package ,,"NewWorkDescription: !image-2021-09-23-10-43-46-373.png|width=827,height=406! From the latest request from customer, the PTA24 should not be existed from the Port configurations. Please refer to the email attachment for more details (Susan Sun) Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Remove the PTA24 from Port configuration."
ARTD-17073	Bug	 [PORT] An error should be raised when configure the not available pins in CT HLD<*> Detailed description (how to reproduce it): There are some types of pins like this: !image-2021-09-23-11-11-49-494.png|width=606,height=333! There is an error should be raise when user configure those pins for the affected packages. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There is no error was raised when user configure the not available pins Expected behavior: There is an error should be raised when user configure the not available pins Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17078	Bug	 [S32K3 RTM][FEE] fix CMM MISRA violations<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		there is CCM MISRA violations in Fee_JobErrorNotification Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: there is CCM MISRA violations in Fee_JobErrorNotification Expected behavior: there is not CCM MISRA violations in Fee_JobErrorNotification Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17079	Bug	[WDG][S32K3XX] Reset value of TO register is incorrect<*> Detailed description (how to reproduce it): Reset value of TO register isnt matching with S32k3xx_RM_Rev2 In Swt_Ip_FeatureDefines.h: #define SWT_IP_TO_RESET_VALUE_U32 (0x0073FDE0U) In RM (or check attached file) : !image-2021-09-23-13-13-45-777.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Reset value of CS register isnt matching with S32k1xx_RM_Rev13 Expected behavior: update #define SWT_IP_TO_RESET_VALUE_U32 (0x00000320U) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17102	Bug	[ICU] Fix index of array node in ecpd<*> Detailed description (how to reproduce it): EPD ECU Parameter Definition (Schema) Used by EBT ECPD ECU Configuration Parameter Definition (Schema) Used by S32CT EPC ECU Parameter Configuration (Configuration File) Used by EBT ECVD ECU Configuration Value Description (Configuration File) Used by S32CT Index of array IcuHwConfiguration sort by name. attached 2 file epc and ecvd see the diffirent Preconditions: Index of array GptHwConfiguration sort by name. Test Case ID (internal TC that caught the defect) optional: Observed behavior: when import epc to DS .Index of array IcuHwConfiguration sort by name. Expected behavior: import epc file to DS the array same when import to EB. Can import export (EBT-DS) No violations VSMD. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional: modify template file and xdm
ARTD-17109	New	 New Feature [OCU] Different declaration of functions in ReqExport and header files ,,"NewWorkDescription: List function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code: Ocu_ProcessChannelNotification(uint16 Channel) Emios_Ocu_Ip_ValueType Emios_Ocu_Ip_GetCounter(uint8 InstNum, uint8 ChNum) Emios_Ocu_Ip_ReturnType Emios_Ocu_Ip_SetAbsoluteThreshold(uint8 InstNum, uint8 ChNum, Emios_Ocu_Ip_ValueType ReferenceVal, Emios_Ocu_Ip_ValueType AbsoluteVal) Emios_Ocu_Ip_ReturnType Emios_Ocu_Ip_SetRelativeThreshold(uint8 InstNum, uint8 ChNum, Emios_Ocu_Ip_ValueType RelativeValue) Please see in attach file Requirement source: ReqExport.txt (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Check function in ""ReqExport.txt"" file but does not include in ""*.h"" files of driver code"
ARTD-17116	Bug	 [FLS] FlsCallCycle parameter is 0 and cannot be configured<*> Detailed description (how to reproduce it): FlsCallCycle parameter is 0 and cannot be configured. This parameter is used by Fls driver in bswmd file (eclipse\plugins\Fls_TS_T40D11M20I0R0\generate_swcd\swcd \Fls_Bswmd.arxml) as follows: <PERIOD>[!IF "node:exists(FlsConfigSet/FlsCallCycle)"![!"FlsConfigSet/FlsCallCycle"!][!ELSE!]0[!ENDIF!]</PERIOD> As a result the generated value for Fls main function PERIOD in bswmd file is always 0 and this results in error in Autosar RTE as 0 is not a valid period of main function. Preconditions: FLS driver used together with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Not able to generate Autosar RTE because the Fls main function period in bswmd file is 0 Expected behavior: To be able to generate Autosar RTE (period is not 0 in bswmd file) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Make the FlsCallCycle parameter configurable by these changes in Fls.xdm file: original FlsCallCycle definition: <v:var name="FlsCallCycle" type="FLOAT_LABEL"> <a:a name="LABEL" value="Fls Call Cycle"/> <a:a name="DESC"> .... Cycle time of calls of the flash driver main function Note: Not supported by the driver. .... </a:a> ....

ID	Subtype	Headline and Description
		<a:da name="DEFAULT" value="0.0"/> .... <a:da name="READONLY" value="true"/> </v:var> Fixed definition (modified type of parameter from FLOAT_LABEL to FLOAT, modified DESC field to remove note that not supported by driver, modified default value from 0 to 0.01 and removed READONLY attribute): <v:var name="FlsCallCycle" type="FLOAT"> <a:a name="LABEL" value="Fls Call Cycle"/> <a:a name="DESC"> .... Cycle time of calls of the flash driver main function .... </a:a> .... <a:da name="DEFAULT" value="0.01"/> .... </v:var> Find attached the updated Fls.xdm file.
ARTD-17128	Bug	 [CAN] inital segments generated by auto calculation baudrate in FlexCAN_Ip_PbCfg.c is not same with the ones in HLD<*> Detailed description (how to reproduce it): with input paramaters: Can_CLK = 24Mhz and !image-2021-09-24-18-32-47-140.png! segments generated in IPL (FlexCAN_Ip_PbCfg.c) !image-2021-09-24-18-34-19-636.png! segments generated in HLD (Can_PbCfg.c) !image-2021-09-24-18-34-54-919.png! => NOT identical. so affter Can_Init called, segments generated by IP used => not works need to check for S32CT code also. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: segments generated by HLD and IP are not identical Expected behavior: segments generated by HLD and IP are identical Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17130	Bug	 [RM] Remove redundant characters<*> Detailed description (how to reproduce it): Some redundant character which make build fail CCOV test !image-2021-09-25-15-45-45-138.png|width=805,height=238! Preconditions: setup run CCOV test Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		Rm_TS_COV_001 Observed behavior: Build fail test: !image-2021-09-25-15-43-45-143.png|width=890,height=240! Expected behavior: build successful Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove the "\" character.
ARTD-17137	Bug	[I2c] Driver can not link to channel Ecuc partition on EB 27.1<*> Detailed description (how to reproduce it): [...] Driver can not link to channel Ecuc partition on EB 27.1 !image-2021-09-27-10-29-05-288.png! Preconditions: [...] N/A Test Case ID (internal TC that caught the defect) optional: [...] I2c_TS_MUL_001 Observed behavior: [...] Driver can not link to channel Ecuc partition on EB 27.1 Expected behavior: [...] Driver can link to channel Ecuc partition on EB 27.1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17140	Bug	[Mcl] Flexio_Ip_baIpIsInitialized was created of incorrect memory<*> Detailed description (how to reproduce it): Run IPV Flexio in core 1, driver don't go to function Flexio_Lin_Ip_IrqHandler Preconditions: Because module Mcl was init in core 0 => Flexio_Ip_baIpIsInitialized will equal TRUE in core 0. But Flexio run in core 1. Flexio_Ip_baIpIsInitialized allocated in MCL_START_SEC_VAR_CLEARED_BOOLEAN of memap. ! image-2021-09-27-11-30-35-458.png! => core 1 can't access to Flexio_Ip_baIpIsInitialized in core 0. Test Case ID (internal TC that caught the defect) optional: Lin_TC_WBT_0005 Observed behavior: Test fail Expected behavior: Test pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Change MCL_START_SEC_VAR_CLEARED_BOOLEAN to MCL_START_SEC_VAR_CLEARED_BOOLEAN_NO_CACHEABLE ! image-2021-09-27-15-12-10-063.png!

ID	Subtype	Headline and Description
ARTD-17142	New	New Feature [SPI] Add How to use half duplex mode in UM ,,"NewWorkDescription: Add How to use half duplex mode in UM Requirement source: NA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-17141	Bug	[Rm] Fix description and readme Example<*> Detailed description (how to reproduce it): 1. In description of all Example_S32K312, please modify to has only Debug Flash. (In picture attachment). 2. And Name in line 40-41 of Rm_Example_S32K312's description, should we change them into "Rm_Example_S32K312_Debug_FLASH_PNE" (in S32DS screen, using this name)? 3. In Mpu Example, in section1 Example Description, please fix "Xrdc" into "Mpu". Detail in attachment. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17150	Bug	[S32K3XX] [PORT] Fix compiler warning<*> Detailed description (how to reproduce it): in file compiler warning report: [http://solomon.ea.freescale.net/1/project/custom_compilerwarning/details] Preconditions: all warning need to be run out Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: !image-2021-09-27-15-39-45-811.png! Expected behavior: driver need to be update to resolve this issue Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17200	Bug	[WDG] WDG_EXCLUSIVE_AREA_00 is missing in bswmd file<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		WDG_EXCLUSIVE_AREA_00 is not missing in bswmd file resulting in an issue that the exclusive area is not generate by Autosar RTE leading to compiler error. Preconditions: Wdg driver used with Autosar RTE Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Exclusive area 00 is not generated by Autosar RTE Expected behavior: Exclusive area 00 is generated by Autosar RTE Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Update the exclusive_areas_to_be_defined_in_bsw_scheduler.dox file and NonASR_ServiceID.xml to map the exclusive area to a function which is generated into bswmd file by bswmd_creator script. Find attached updated files with one possible solution (adding Wdg_Cbk_GptNotification0/1/2/3/4/5/6 functions into NonASR_ServiceID.xml and then mapping the WDG_EXCLUSIVE_AREA_00 to Wdg_Cbk_GptNotification0/1/2/3/4/5/6 in exclusive_areas_to_be_defined_in_bsw_scheduler.dox).).
ARTD-17214	Bug	[LIN] Missing case LIN_DUAL_CLOCK_MODE with IPV FlexIO<*> Detailed description (how to reproduce it): Missing case LIN_DUAL_CLOCK_MODE with IPV FlexIO Preconditions: Missing case LIN_DUAL_CLOCK_MODE with IPV FlexIO Test Case ID (internal TC that caught the defect) optional: Lin_TC_FCT_0003 Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: add case LIN_DUAL_CLOCK_MODE with IPV FlexIO
ARTD-17264	Bug	[S32K3 RTM] [I2C] Fixing HIS_CYCLE warning<*> Detailed description (how to reproduce it): There is are HIS_CYCLE appeared in report. Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: Remove the HIS_CYCLE is required Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17269	Bug	

ID	Subtype	Headline and Description
		[WDG] Error in configuration of Example<*> Detailed description (how to reproduce it): The "max wdg timeout" is 2s in EB configuration , so the maximum value which we can push in the Wdg_43_Instance0_SetTriggerCondition is 2000. But the Wdg_43_Instance0_SetTriggerCondition(0xFD00) is called in the main.c Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: The example run to reset Expected behavior: The example do not run to reset Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-17272	Bug	[I2c] [Example] Update description and rename example<*> Detailed description (how to reproduce it): [...] Update description example and correct name of example Edit connection description, update connector register !image-2021-09-28-17-18-53-878.png! !image-2021-09-28-17-23-12-469.png! !image-2021-09-28-17-20-07-624.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17279	Bug	[BASE] No need to declare trusted functions in OsIf_Timer_Systick_TrustedFunctions.h when AutosarOS used<*> Detailed description (how to reproduce it): When AutosarOS used, the functions OsIf_GetCounter() and OsIf_GetElapsed() will call corresponding to GetCounterValue() and GetElapsedValue() in Os.h if enable OsIfUseSystemTimer. So, the functions OsIf_Timer_System_Internal_Init(), OsIf_Timer_System_Internal_GetCounter() and OsIf_Timer_System_Internal_GetElapsed() will only called when using OS_FREERTOS or OS_BAREMETAL. AutosarOS will not called these functions. So OsIf_Timer_Systick_TrustedFunctions.h file can be removed. Preconditions:

ID	Subtype	Headline and Description
		NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: In OsIf_Timer_System.c: the functions OsIf_Timer_System_Internal_Init(), OsIf_Timer_System_Internal_GetCounter() and OsIf_Timer_System_Internal_GetElapsed() are not called when AutosarOS is used(USING_OS_AUTOSAROS defined). Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Remove OsIf_Timer_Systick_TrustedFunctions.h and update the subchapter User mode in IM
ARTD-17276	Bug	[S32K3XX][S32k3xx_100] function in "ReqExport.txt" not mapping "*.h" files of driver code: ,,"Detailed description (how to reproduce it): checking for mapping between ReqExport.txt and "" .h "" files in driver code. Some functions not mapping. Checking S32K3XX_result.txt attached file Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Platform_TS_001 Observed behavior: !image-2021-09-28-18-47-12-970.png! Expected behavior: Modify Platform_GetIrqMonitorStatus function in driver code to mapping ReqExport Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-17294	Bug	[BASE] Fix compiler warning for S32K3XX RTM 1.0.0<*> Detailed description (how to reproduce it): Fix compiler warning for S32K3XX RTM 1.0.0. Please see the attachment for more detail. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: There is a compiler warning. Expected behavior: There is no compiler warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-17301	Bug	[S32K324] DS multicore project does not build<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Create new multicore project in S32DS for S32K324 Build the project Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Project does not build due the not updated multicore linker files Expected behavior: project builds, uploads to the board and executes on both cores Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-17352	Bug	[LIN] Driver and requirement are inconsistent<*> Detailed description (how to reproduce it): Driver and requirement are incompatible as below: No||Function name||Remark||_*Solution 1|void Flexio_Lin_Ip_GotoIdleState(const uint8 Channel);|Different name "Reqexport.txt" : "Flexio_Lin_Ip_GoToIdleState" " .h " file : "Flexio_Lin_Ip_GotoIdleState"|Change from Flexio_Lin_Ip_GotoIdleState to Flexio_Lin_Ip_GoToIdleState 2|void Lin_GetVersionInfo (Std_VersionInfoType VersionInfo);|Different name "Reqexport.txt" : "versioninfo" " .h " file : "VersionInfo"|The parameter in Lin_GetVersionInfo function need to be updated from VersionInfo to versioninfo. 3|void Lpuart_Lin_Ip_GotoIdleState(const uint8 Instance);|Different name "Reqexport.txt" : "Lpuart_Lin_Ip_GoToIdleState" " .h " file : "Lpuart_Lin_Ip_GotoIdleState"|Change from Lpuart_Lin_Ip_GotoIdleState to Lpuart_Lin_Ip_GoToIdleState 4|void Lpuart_Lin_Ip_TimerExpiredService(uint8 Instance);|Lacking const "Reqexport.txt" : "(const uint8 Instance);" " .h " file : "(uint8 Instance);"|The Instance parameter type in Lpuart_Lin_Ip_TimerExpiredService function should be changed to const. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Driver and requirement are inconsistent Expected behavior: Driver and requirement are consistent Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17366	Bug	[RM] Fix Pin error and Clock warning in Example<*> Detailed description (how to reproduce it): 1. Pin Error : Pins initialization requires the PINS Driver in the project. Detail in attachment.

ID	Subtype	Headline and Description
		2. Clock Warning : Please check in Clock >Choose tab Code Preview > Double click in "Code generated with warnings". Detail warning in attachment. 3. Pin error is existed in all example of DS. Clock Warning is existed in example Rm HLD of DS. Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17421	Bug	[UART] [DS] S32K3XX Examples have some warning in Clock configuration<*> Detailed description (how to reproduce it): There is warning from Clock tab for DS Example Preconditions: Open the Clock tab > Click on the Code Preview tab > Double click on the Code generated with warnings Test Case ID (internal TC that caught the defect) optional: S32K3XX Examples Observed behavior: S32K3XX Example warning Expected behavior: Fix S32K3XX Example warning Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17465	Bug	[S32K3][SENT] Incorrect SENT_MAX_PARTITIONS generation in Sent_Cfg.h<*> Detailed description (how to reproduce it): In Sent_Cfg.h, SENT_MAX_PARTITIONS is generated: [!VAR "maxCoreDefConfig" = "num:i(1)"!] [!IF "SentGeneral/SentMulticoreSupport = 'true'"!] [!IF "node:exists(as:modconf('EcuC')[1]/EcucPartitionCollection/*[1]/EcucPartition)"!] [!VAR "maxCoreDefConfig" = "num:i(count(as:modconf('EcuC')[1]/EcucPartitionCollection/*[1]/EcucPartition/*))"!] [!ENDIF!] [!ENDIF!] [!ENDNOCODE!] #define SENT_MAX_PARTITIONS[!WS "4"!][!"num:i($maxCoreDefConfig)"!]U But *SentMulticoreSupport doesn't exist in sent.xdm. So SENT_MAX_PARTITIONS always equal to 1. Preconditions: Enable multicore Test Case ID (internal TC that caught the defect) optional: Sent_TS_011 Observed behavior: NA

ID	Subtype	Headline and Description
		Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Chane SentMulticoreSupport to *SentEnableMulticoreSupport* in Sent_Cfg.h
ARTD-17470	Bug	 [RM] Rm_Example_S32K312 fail<*> Detailed description (how to reproduce it): Rm_Example_S32K312 fail in gMpuErrorDetected with DS Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17515	New	 New Feature [RESOURCE] Requirement CPR_RTD_00220.resource has changed to non-traceable ,,"NewWorkDescription: CPR_RTD_00220.resource has changed to non-traceable, so ""@implement ResourceSubderivative_Object"" in Resource.xdm should be removed. Requirement source: cPRT (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: NA"
ARTD-17530	Bug	 [I2C] Add report review check list<*> Detailed description (how to reproduce it): NA Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: NA Expected behavior: NA Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-17597	Bug	 [ICU][S32K3XX] Update test after code freeze<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): Update Req for Icu_TC_FCT_1302 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

4.11 Change List for 0.9.0

ID	Subtype	Headline and Description
ARTD-990	New	New Feature [LIN][S32K3XX] - Add timeout checking for a frame reception ,,The LIN driver shall check if reception occurs in a limited period of time configured by user. A timeout checking shall be implemented in order to not wait forever for the frame reception
ARTD-1115	New	New Feature [ADC] Add support for streaming results reorder ,,"Details in CPR_RTD_00490.adc The adc driver shall support streaming access mode functionality with the possibility to arrange the adc results as multiple sets of group result buffer. E.g.: for a group with channels {CH1 Ch5 CH7} the resulting stream buffer shall be: {CH1, Ch5, CH7, CH1, Ch5, CH7, CH1, Ch5, CH7} instead of {CH1,CH1,CH1,CH5,CH5,CH5,CH7,CH7,CH7} like supported by autosar standard. This feature extension shall be enabled by using a parameter named Stream Result Grouping at group level. The default value of this parameter shall be False and shall only be editable when streaming access mode is selected for its group. Implement also in Tresos and S32CT"
ARTD-1426	New	New Feature [ADC] Double buffering optimization - optimize DMA streaming ,,"Add dev test to validate double buffering optimization. Investigate and fix any eventual issue CPR_RTD_00384: The ADC driver shall provide an optional configuration parameter for reducing the number of interrupts required for processing the conversions of Adc Groups that consist of one or more channels (depending on HW capabilities) and which are configured as ADC_ACCESS_MODE_STREAMING. This parameter shall be available only when DMA transfer is used. When this feature is enabled, only one interrupt will be raised after the completion of all stream conversions (as configured by AdcStreamingNumSamples parameter). An additional interrupt to be raised after half of the stream is converted shall also be configurable.

ID	Subtype	Headline and Description
		"
ARTD-1670	New	New Feature [CAN][FD/TDC] non-identical prescalers need to be supported ,,"Creating a simple testcase for sending an BRS frame with enabled TDC with bitrate 500Kbps 4000 Kbps. > after investigation, only a bitrate configuration (get from SDK) is working, others can work (but with many errors). This reflect that the TDC bitrate configuration is strictly depend on users environment > this raise the requirement for flexible bitrate configuration. CAN_TC_FCT_7590 can only send frame without errors with below bitrate configuration for 500Kbps-4Mbits: { (uint8)7U, (uint8)4U, (uint8)1U, (uint16)*9*, (uint8)1U } , /*values for CBT baudrate .bitrate_cbt*/ { (uint8)15U, (uint8)1U, (uint8)1U, (uint16)*0*, (uint8)1U } , The TDC offset exactly base on rm's expression: (proseg phase_seg1 2) == 15 1 2 == 18 => this relfect that identical prescalers does not help in this situation, instead limit the bitrate configuration! Expectation: non-identical prescalers should be support. and in this case, a warning can be raised for reflecting the recommendation in rm"
ARTD-1952	New	New Feature [S32K344] ICU_GET_PULSE_WIDTH_API is hardcoded as STD_OFF ,,Please see ticket AMNG-8589
ARTD-1958	Bug	[PWM][IPV_EMIOS] Spike with PWM duty cycle 0% in OPWMB mode<*> Detailed description (how to reproduce it): An issue has been reported by Sumimoto when they're trying to generate PWM signal on S32K2. They observe a spike during Pwm_Init(), with PWM duty cycle 0% on OPWMB mode. Note: This is the cloned ticket from MCAL legacy, the code in Zebra has been changed. However, as it's an issue from IPV_EMIOS, which is available on K3, the ticket is created to avoid the similar issue. Preconditions: # PWM channel configuration EMIOS 0 channel 1, default duty cycle: 0, Polarity: PWM_HIGH, Idle state: PWM_LOW EMIOS 0 channel on OPWMB mode, BUS A selected. Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Before entering OPWMB mode, PWM driver will set the EMIOS channel to GPDO mode with default Idle state => the output signal will be set to LOW When entering OPWMB mode, A and B registers are updated according to duty cycle and period, then EDPOL is set as polarity PWM_HIGH: REG_RMW32 (EMIOS_CCR_ADDR32(u8ModuleIdx, u8ChannelIdx), (CCR_MODE_MASK_U32 CCR_EDPOL_MASK_U32),

ID	Subtype	Headline and Description
		((u32CtrlRegVal & CCR_MODE_MASK_U32) (u32PolarityBit & CCR_EDPOL_MASK_U32)) => After that output signal will be set to HIGH Force match on the 1^st edge by writing to FORCEB bit: REG_BIT_SET32(EMIOS_CCR_ADDR32(u8ModuleIdx, u8ChannelIdx), CCR_FORCMB_MASK_U32); Because the duty cycle is 0 => the output signal will be set to LOW => A spike occurred. Expected behavior: This is a bug because Autosar requires not to have any spikes. It might impacts to other eMios platforms like Cobra, Rainier, Calypso, Mamba, Castor,... Also, we need to avoid spike in all APIs, so other PWM mode should be carefully tested. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Spike can be avoid by setting polarity after setting mode OPWMB entry, instead of setting both of them at same time.
ARTD-1966	New	 New Feature [ADC] Implement ADC_BYPASS_CONSISTENCY_LOOP ,,"ADC: implement and rename ADC_BYPASS_CONSISTENCY_LOOP When enabled, Adc_Ipw_StopCurrentConversion does not wait for the actual conversion to finish. To support this, a new parameter should be added to Adc_Sar_Ip_AbortChain boolean Blocking. When set to false, this function should not wait until the conversion is actually completed. Update IPL requirement Consider renaming the feature. If renamed, update also in tresos, ct, and doc "
ARTD-2020	Bug	 [ADC] Adc_EnableHardwareTrigger set MODE to ONESHOT mode so sw continuous group can not run as expected<*> Test sequence: / Start ADC SW Normal continuous group conversion / Adc_StartGroupConversion(t_u8AdcSWNormalGroup); / Enable hardware trigger for ADC HW Injected group conversion / Adc_EnableHardwareTrigger(t_u8AdcHWInjectedGroup); / Verify: There is no DET error / EU_ASSERT(T_Adc_Det_TestNoError()); T_ADC_HWInjectedProcess(t_u8AdcHWInjectedGroup, t_u8HwUnitIndex); T_ADC_SWNormalProcess(t_u8AdcSWNormalGroup, t_u8HwUnitIndex); Adc_EnableHardwareTrigger set MODE to ONESHOT mode so t_u8AdcSWNormalGroup can not run as expected
ARTD-2039	Bug	 [ADC] Adc_ReadGroup always resets user result buffer index<*> Detailed description (how to reproduce it): Adc_ReadGroup always resets user result buffer index Verify group conversion with normal group: hw, injected, oneshot, streaming circular Test sequence: 1. Adc_Init with number of streaming sample = 10 2. Adc_SetupResultBuffer: t_setupResultBuffer

ID	Subtype	Headline and Description

		3. Adc_EnableHardwareTrigger
		4. Loop to generate ADC trigger several times that equals number of sample
		4.1 T_ADC_StartTrigger
		4.2 Wait until Adc_GetGroupStatus is ADC_COMPLETED, end of loop when status is ADC_STREAM_COMPLETED
		4.3 T_ADC_StopTrigger
		4.4 Adc_ReadGroup(group, t_readGroupBuffer) returns E_OK
		4.5 Verify conversion result in "t_readGroupBuffer"
		5. Verify conversion result in user result buffer: t_setupResultBuffer
		=> Fail at step 5: the "t_setupResultBuffer" has only 1 sample
		Observed behavior: After calling Adc_ReadGroup function, the user result buffer index always resets to 0
		Adc_ReadGroup
		{
		Adc_UpdateStatusReadGroupInt
		{
		if (ADC_COMPLETED == Adc_aGroupStatus[Group].eConversion){
		Adc_aGroupStatus[Group].ResultIndex = 0U;
		}
		}
		}
		=> The "t_setupResultBuffer" is overwritten at the first index
		Preconditions:
		[...]
		Test Case ID (internal TC that caught the defect) optional:
		Adc_TC_FCT_0107, refer: https://bitbucket.sw.nxp.com/projects/ARTD/repos/test_adc/browse/generic/src/Adc_TC_FCT_0107.c
		Observed behavior:
		After calling Adc_ReadGroup function, the user result buffer index always resets to 0
		Expected behavior:
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
		Proposed solution optional:

ARTD-2250	New	New Feature [SPI] Improvement data configuration structure for multicore should be split for each core ,,"The theory(and req) says: ""ALL the configuration data parsed by the Init() function is to be split into different configuration structures, allocat*able in different memory regions to ensure HW isolation. If you have common runtime data, that needs to stay into an array indexed by the core ID"". In practice, we did not fully implement the Memory Mapping support yet, and we decided still that we want to split the data completely if possible, into independent structures, to better cope with it when we will add the MemMap support. Currently, SPI has common structure configuration for all cores. To follow the problem mentioned above. The elements in arraysChannels, Jobs, Sequences, ExternalDevices, HWUnit which are not allocated to that core will be NULL pointer."
ARTD-2384	Bug	[ADC] Adc_ReadRawData need to have more Det checking<*> 1, Adc_ReadRawData does not raise Det error with condition "NumItems is greater than the maximum number of channels available"- CPR_RTD_00508.adc 2, ADC_SAR_CDR_COUNT (48u) in driver but in RM only have physical channel from 0 to 39

ID	Subtype	Headline and Description

ARTD-2534	New	New Feature
		
		[can] Handling timeout implementation using OsIf
		,,"Add a referenceable enum in Tresos for OsIf that can be used by other drivers to allow selection only of available osif counter types
		
		In each module configuration that needs to implement a timeout add the following field
		<v:var name=""<Module>TimeoutMethod"" type=""ENUMERATION""><v:var name=""<Module>TimeoutMethod"" type=""ENUMERATION"">
		<a:a name=""LABEL"" value=""<Module> Timeout Method""/><a:a name=""LABEL"" value=""<Module> Timeout Method""/>
		<a:a name=""DESC""><a:a name=""DESC"">
		<a:v><a:v>
		<![CDATA[EN:
		<html>
		 <Module>TimeoutMethod
		 Configures the timeout method.
		 Based on this selection a certain timeout method from OsIf will be used in the driver.
		 Note: If SystemTimer or CustomTimer are selected make sure the corresponding timer is enabled in OsIf General configuration.
		Note: Implementation Specific Parameter.
		</html>
		]]>
		</a:v>
		</a:a>
		<a:a name=""IMPLEMENTATIONCONFIGCLASS"" type=""IMPLEMENTATIONCONFIGCLASS"">
		<icc:v vclass=""PreCompile"">VariantPreCompile</icc:v>
		<icc:v vclass=""PostBuild"">VariantPreCompile</icc:v>
		</a:a>
		<a:a name=""ORIGIN"" value=""M4_XDM_AR_MODULE_ORIGIN""/>
		<a:a name=""SCOPE"" value=""LOCAL""/>
		<a:a name=""SYMBOLICNAMEVALUE"" value=""false""/>
		<a:a name=""UUID"" value=""ECUC:7228a335-4003-4639-8e1a-bb3d9f762a7b""/>
		<a:a name=""DEFAULT"" value=""DummyTimer""/>
		<a:da name=""INVALID"" type=""XPath"">
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseCustomTimer') = 'false' and node:fallback(.,'DummyTimer') = 'CustomTimer'"" true=""Custom Timer is not enabled in OsIf (OsIfGeneral/OsIfUseCustomTimer checkbox)""/>
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseSystemTimer') = 'false' and node:fallback(.,'DummyTimer') = 'SystemTimer'"" true=""System Timer is not enabled in OsIf (OsIfGeneral/OsIfUseSystemTimer checkbox)""/>
		</a:da>
		<a:da name=""RANGE"">
		<a:v>DummyTimer</a:v>
		<a:v>SystemTimer</a:v>
		<a:v>CustomTimer</a:v>
		</a:da>
		</v:var>
		Based on its configuration generate an enum field of the type OsIf_CounterType (which is defined in OsIf.h and described below)
		// This is defined in OsIf.h
		typedef enum
		{
		OSIF_COUNTER_DUMMY, /**< dummy counter /

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		#if (OSIF_USE_SYSTEM_TIMER == STD_ON)
		OSIF_COUNTER_SYSTEM, /**< system counter /
		#endif / (OSIF_USE_SYSTEM_TIMER == STD_ON) /
		#if (OSIF_USE_CUSTOM_TIMER == STD_ON)
		OSIF_COUNTER_CUSTOM /**< custom counter /
		#endif / (OSIF_USE_CUSTOM_TIMER == STD_ON) /
		} OsIf_CounterType;
		Use the generated value of the type described above to use the OsIf APIs for implementing timeouts:
		// Defined in OsIf.h
		/*!
		brief Get the current value counter
		This function returns the current value of the counter.
		param[in] SelectedCounter the type of counter to use
		return the current value of the counter
		/
		uint32 OsIf_GetCounter(OsIf_CounterType SelectedCounter);/*!
		brief Get the elapsed value from a reference point
		This function returns the delta time in ticks compared to a reference, and updates the reference.
		param[inout] CurrentRef reference counter value, updated to current counter value
		param[in] SelectedCounter the type of counter to use
		return the elapsed time
		/
		uint32 OsIf_GetElapsed(uint32 const CurrentRef, OsIf_CounterType SelectedCounter);/*!
		brief Set a new frequency used for time conversion (microseconds to ticks)
		This function stores a new timer frequency used for time conversion computations
		param[in] Freq the new frequency
		param[in] SelectedCounter the type of counter to use
		/
		void OsIf_SetTimerFrequency(uint32 Freq, OsIf_CounterType SelectedCounter);/*!
		brief Convert microseconds to ticks
		This function converts a value from microsecond units to ticks units.
		param[in] Micros microseconds value
		param[in] SelectedCounter the type of counter to use
		return the equivalent value in ticks
		/
		uint32 OsIf_MicrosToTicks(uint32 Micros, OsIf_CounterType SelectedCounter);
		Implementation example from GMAC (only an example, not a guideline)
		/*FUNCTION
		Function Name : GMAC_StartTimeout
		Description : Checks for timeout condition
		END**********/
		void GMAC_StartTimeout(uint32 startTimeOut,
		uint32 elapsedTimeOut,
		uint32 timeoutTicksOut,
		uint32 timeoutUs)
		{
		startTimeOut = OsIf_GetCounter(GMAC_TIMEOUT_TYPE);
		elapsedTimeOut = 0U;
		timeoutTicksOut = OsIf_MicrosToTicks(timeoutUs, GMAC_TIMEOUT_TYPE);
		}/*FUNCTION
		Function Name : GMAC_TimeoutExpired
		Description : Checks for timeout expiration condition
		END**********/
		boolean GMAC_TimeoutExpired(uint32 startTimeInOut,
		uint32 elapsedTimeInOut,

ID	Subtype	Headline and Description

		uint32 timeoutTicks)
		{
		elapsedTimeInOut = OsIf_GetElapsed(startTimeInOut, GMAC_TIMEOUT_TYPE);
		return ((*elapsedTimeInOut >= timeoutTicks)? TRUE : FALSE);
		}
		/ Usage /
		uint32 startTime, elapsedTime, timeoutTicks;
		uint32 timeoutUs = 100U;
		/ Wait for completion /
		GMAC_StartTimeout(&startTime, &elapsedTime, &timeoutTicks, timeoutUs);
		do
		{
		if ((base->MAC_MDIO_ADDRESS & GMAC_MAC_MDIO_ADDRESS_GB_MASK) == 0U)
		{
		status = GMAC_STATUS_SUCCESS;
		break;
		}
		} while (!GMAC_TimeoutExpired(&startTime, &elapsedTime, timeoutTicks));
		
		"

ARTD-2569	New	 New Feature [uart] How to handle Det files in DS+CT projects ,,"Det files need to be added in a DS+CT project when HLD components are used so the drivers can be compiled when the development errors detection is enabled. The Det stub already has a manifest associated to it, so each driver that needs Det for a successful build should add Det as a dependency in its manifest. Example from the Adc driver: <component id=""platform.driver.adc"" full_name=""Adc"" brief=""Adc Component"" dependency=""platform.driver.det"" name=""Adc"" type=""driver"" devices=""S32K314 S32K324 S32K344 S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Adc_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""*.c""/> <files mask=""Adc_Sar_Ip_HwAccess.h""/> </source> <source path=""Adc_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""*.h""/> </source> </component> "
ARTD-2663	Bug	 [ADC] Group sw trigger injected transfer by DMA can not stream complete<*> Group sw trigger injected transfer by DMA can not stream complete because of jumping to isr handler with IMR register configured Adc_TS_014
ARTD-2799	Bug	 [WDG] Example displays some warnings when generating code or building<*> Detailed description (how to reproduce it): Step 1: pull code from tag WDG_016 and compile wdg plugin Step 2: open cygwin command and cd to project example path in WDG plugin folder Step 3: make generate; make build Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Display some warings when generating code or building

ID	Subtype	Headline and Description
		Build warning ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c: In function 'EcuM_ValidateWakeupEvent': ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c:180:86: warning: unused parameter 'events' [-Wunused-parameter] 180 FUNC(void, ECUM_CODE) EcuM_ValidateWakeupEvent(VAR(EcuM_WakeupSourceType, AUTOMATIC) events) ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c: In function 'EcuM_CheckWakeup': ../../../..//EcuM_TS_T40D11M9I0R0/src/EcuM.c:193:78: warning: unused parameter 'wakeupSource' [-Wunused-parameter] 193 FUNC(void, ECUM_CODE) EcuM_CheckWakeup(VAR(EcuM_WakeupSourceType, AUTOMATIC) wakeupSource) ../../../..//Gpt_TS_T40D11M9I0R0/src/Gpt_lpw.c:333:12: warning: unused variable 'tempValue' [-Wunused-variable] 333 uint32 tempValue = 0U; ../../../..//Gpt_TS_T40D11M9I0R0/src/Gpt_lpw.c:332:12: warning: unused variable 'counterValue' [-Wunused-variable] 332 uint32 counterValue = 0U; ../../../..//Gpt_TS_T40D11M9I0R0/src/Gpt_lpw.c:331:12: warning: unused variable 'compareValue' [-Wunused-variable] 331 uint32 compareValue = 0U; generate/src/Wdg_43_Instance0_VS_0_PBcfg.c:101:5: warning: initialization discards 'const' qualifier from pointer target type [-Wdiscarded-qualifiers] 101 &Wdg_lpw_OffModeSettings_0_VS_0 generate/src/Wdg_43_Instance0_VS_0_PBcfg.c:109:5: warning: initialization discards 'const' qualifier from pointer target type [-Wdiscarded-qualifiers] 109 &Wdg_lpw_SlowModeSettings_0_VS_0 generate/src/Wdg_43_Instance0_VS_0_PBcfg.c:117:5: warning: initialization discards 'const' qualifier from pointer target type [-Wdiscarded-qualifiers] 117 &Wdg_lpw_FastModeSettings_0_VS_0 generate warning: WARNING 20-10-27,11:15:32 (1159) Node /TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:32 (1159) Node /Wdg_43_Instance1_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance2_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance3_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance4_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance5_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:33 (1159) Node /Wdg_43_Instance6_TS_T40D11M9I0R0/Wdg/WdgGeneral/WdgEcucPartitionRef defines two attributes with the same name "EDITABLE" which could not be merged. Removing one of the attributes WARNING 20-10-27,11:15:32 (95021) Only variables and references may have the attributes postBuildVariantValue and valueConfigClass. Detail was attached. Expected behavior: The project generate and build no errors, warnings

ID	Subtype	Headline and Description
ARTD-2826	Bug	[ADC] DMA have wrong result value when using streaming group<*> DMA test have wrong result value when configuring streaming group-Adc_TS_014
ARTD-2827	Bug	[ADC] driver can not stop continuous group configured without interrupt<*> In Adc_TS_019 CFG_SETS=2, group 5 is continuous without interrupt group, when calling stop group, this group can not stop and raising error time out. More detail in attachment

ARTD-2935	Bug	[GPT] Problem with getting index of channel for each core used for channel initialization<*>
		
		When i config multicore in EB, for instance i config 2 channel (index 0, 1) with core 4 and 2 channel with core 5 (index 2,3). I found that channel 2,3 will not be initialized because:
		for (ChannelIndex = 0U; ChannelIndex < Gpt_pConfig[coreID]->channelCount; ChannelIndex++)
		{ channel = Gpt_ConvertChannelIndexToChannel(ChannelIndex, coreID); ...; Gpt_lpw_Init(((*(Gpt_pConfig[coreID]->Gpt_pChannelConfig))[channel].Gpt_lpw_HwChannelConfig)); }
		This section in Gpt_Init() function will init channel in order of each core. when init core 5 , if the ChannelIndex is 0 then channel is 2 , it needs the index 2 in channel configuration array generated in output. But the channel config in output just have 2 elements:
		Gpt_lpw_HwChannelConfigType Gpt_lpw_ChannelConfig_PB_VS_0_P_EcucPartition_Cinque[2U];
		So it cannot get the thirst element in this array.
		I think this function should return valid index for channel, it means when channel configuration of core 5 have 2 element, the channel index will be 0 or 1.
		channel = Gpt_ConvertChannelIndexToChannel();

ARTD-2945	Bug	S32K3 RTD SIUL PTC22 Input<*> When configure S32K344 pins in S32DS, there is an error reported when PTC22 is set as eMIOS input. But actually it can be configured as input according to S32K3 ref manual.
ARTD-3015	Bug	[S32DS 3.3 Update 1] Two settings with the same ID defined, and one has a wrong type, "REFERENCE" ,,"Create a configuration for any S32G2 derivative, go to Peripherals Tool and check the log file. There will be a message related to some settings that couldn't be found: !ENTRY com.nxp.swtools.periphs.model.data 4 0 2020-10-27 12:48:51.333 !MESSAGE An instance of ArraySetting with ID DioEcucPartitionRef contains an unresolvable reference with ID DioEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio !MESSAGE An instance of ArraySetting with ID DioChannelEcucPartitionRef contains an unresolvable reference with ID DioChannelEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio !MESSAGE An instance of ArraySetting with ID DioChannelGroupEcucPartitionRef contains an unresolvable reference with ID DioChannelGroupEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio

ID	Subtype	Headline and Description
		!MESSAGE An instance of ArraySetting with ID DioPortEcucPartitionRef contains an unresolvable reference with ID DioPortEcucPartitionRef to a setting in component with ID Dio and config-set with ID Dio Check in the component file the settings and there will be some structs and arrays defined like: <struct id=""DioEcucPartitionRef""> <array id=""DioEcucPartitionRef"" type=""REFERENCE""> <description></description> <!--Tressos XPath for REFERENCE: ASPathDataOfSchema:/AUTOSAR/EcucDefs/EcucC/EcucPartitionCollection/EcucPartition--> </array> </struct>
ARTD-3038	Bug	[CRYPTO] uint32_t is redefined in std_type defs.h<*> Description: uint32_t is redefined in std_type defs.h Vector are using Crypto module of the MCAL SW32K3_RTD_4.4_0.8.0_P02 with IAR compiler. The Crypto needs the hse interface. And now they get the following error messages: "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external\ThirdParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Base_TS_T40D34M8I0R0\include\BasicTypes.h",52 Error[Pe256]: invalid redeclaration of type name "uint32_t" (declared at line 80 of "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external\ThirdParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Crypto_TS_T40D34M8I0R0\examples\EBT\Crypto_Example_001\include\std_type defs.h") "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external\ThirdParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Base_TS_T40D34M8I0R0\include\BasicTypes.h",100 Error[Pe256]: invalid redeclaration of type name "int32_t" (declared at line 79 of "D:\usr\usage\Delivery\CBD20x\CBD2000733\DELIVERY41653\external\ThirdParty\Mcal_S32k\Supply\SW32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Crypto_TS_T40D34M8I0R0\examples\EBT\Crypto_Example_001\include\std_type defs.h") For explanation: they do not have the included #include <stdint.h> #include <stdbool.h> #include <stddef.h> Proposal solution*: Remove the define of int8_t, uint8_t , int16_t , uint16_t, int32_t, uint32_t, uint64_t in file "W32K3_RTD_4.4_0.8.0_P02\eclipse\plugins\Crypto_TS_T40D34M8I0R0\examples\EBT\Crypto_Example_001\include\std_type defs.h"
ARTD-3506	New	New Feature [CRYPTO]Exclusive Area analysis and update ,,Perform in depth analysis of the necessity of exclusive areas for global variables that remained unanalyzed after S32G2 Beta 090 release.
ARTD-3509	Bug	[CAN][S32DS/HLD] Initialize default valid configuration for CAN<*> To prepare for testing S32ds, please set high priority for this task. Expectation: simplest/default configuration on EB and S32DS should be the same

ID	Subtype	Headline and Description
		Steps: on EB: add CAN from from scratch add only one rx hw object, fix all errors on DS: same as above step minimum the changes of default values at above steps generate codes and comparing output => ds generate many invalid default values some default values are different from EB's one Expected behaviors: default values of S32DS can be valid and be same as EB's one => same start point when using both tools attached .xdm, .mex and output of two tools.
ARTD-3552	Bug	[CAN][S32G2] Fix compiler warning<*> Please refer to the attached file for more detail about warnings. They should be fixed in next release !
ARTD-3581	Bug	[CAN] Improve Cyclomatic Complexity<*> Please reduce cyclomatic complexity below 20 level thread should for functions FlexCAN_Ip_Init_Privileged FlexCAN_IRQHandler Can_Ipw_InitRx Can_Ipw_MainFunction_Read
ARTD-3603	Bug	[uart] - Fix traceability warnings<*> The cprt requirements need to be analyzed and if they are not implemented they should be There are many warnings in traceability reports, so they should be checked and corrected.
ARTD-3610	New	New Feature [IP_Flexcan] status will be retuned only if FLEXCAN_DEV_ERROR_DETECT is ON. ,,"""The major change that will impact the code is that the return status like BUFF_OUT_OF_RANGE and some times the ERROR need to be guarded by (FLEXCAN_DEV_ERROR_DETECT == STD_ON)*""" Many requirements relate to above were applied but the implementation is not in place Expectation: The implementation, review should be done List of APIs have same this srs: *FlexCAN_Ip_SetBitrate* FlexCAN_Ip_SetBitrateCbt FlexCAN_Ip_SetRxFifoGlobalMask FlexCAN_Ip_SetRxIndividualMask FlexCAN_Ip_Init FlexCAN_Ip_SendBlocking FlexCAN_Ip_Send FlexCAN_Ip_ConfigRxMb FlexCAN_Ip_Receive, FlexCAN_Ip_SetTxArbitrationStartDelay, FlexCAN_Ip_SetTDCOffset"

ID	Subtype	Headline and Description
ARTD-3636	New	New Feature [SPI] Move SpiDataWidth, SpiTransferStart, SpiDefaultData nodes from SpiPhyUnit to SpiExternalDevice for IP driver" ,,"Each PCS in the same SPI unit can be used to control one external slave. They can be required to have different value of SpiDataWidth, SpiTransferStart or SpiDefaultDta. Currently, for IP driver, these nodes are pushed into SpiPhyUnit container in IP component file. So it is not supported to change these value for each external Slave device. So, these nodes should be moved to SpiExternalDevice container for IP driver.
ARTD-3673	Bug	[CAN] handle the Det_ReportError inside Can_Init<*> Please look at the case When Can_Ipw_Init/Can_Ipw_InitRx fail: Can_Init will return with: Can_eControllerState[u8ControllerID] = CAN_CS_STOPPED; Can_eDriverStatus[u32CoreId] = CAN_READY; => this cause the next call of Can_Init or Can_SetControllerMode alway fail TC_ID: CAN_TC_FCT_*2662
ARTD-3696	New	New Feature [Ip_Flexcan][FLEXCAN_IP_014_001] Implementation for FlexCAN_Ip_ReceiveBlocking ,,"FLEXCAN_IP_014_001 > FLEXCAN_IP_014_006 will be cover by FlexCAN_Ip_*ReceiveBlocking. The implementation for FlexCAN_Ip_ReceiveBlocking should be done FlexCAN_Ip_*SendBlocking* should note if this api does not support *Interrupt*. This api accepts TxInfo type"
ARTD-3698	New	New Feature [Ip_Flexcan] implementation for FlexCAN_Ip_RxFifoBlocking ,,"FLEXCAN_IP_017_001 => FLEXCAN_IP_017_009 relate to FlexCAN_Ip_RxFifoBlocking. Implementation for *FlexCAN_Ip_RxFifoBlocking should be done. Blocking method APIs now support POLL only?. This should be considered to add to doc/srs "
ARTD-3705	New	New Feature [ADC] Exclusive areas on ADC SAR and BCTU. Avoid multiple use also for CTU ,,"Implement exclusive areas

ID	Subtype	Headline and Description
		https://nxp1.sharepoint.com/:p:/s/Zebra/EehFcYqIlpVJkmyNp8pcae4BNyizwm47eVxbN_s7u30Tzg?e=gTPmi7 Analyze and try to move in IPL, to have exclusive areas as small as possible. See details in presentation and recording"
ARTD-3722	Bug	[CAN][SWS_Can_00273] Bus-off handler need to cancel pending Tx<*> Can_Init Can_Write PduInfo0 with bus-off Recover from bus-off Can_Write PduInfo1 => PduInfo0 was not canceled, instead going to MAF Can_Write PduInfo1 always return BUSY interrupt should be checked also SWS_Can_*00273*:After bus-off detection, the Can module shall cancel still pending messages TC_ID: CAN_TC_FCT_*1681* [POLLing]
ARTD-3731	New	New Feature [LIN][S32K3XX] Add synchronization transmission and reception ,,"Follow requirement # SyncSendData LPUART_LIN_008_001: Service name: Lpuart_Lin_Ip_SyncSendData Syntax: Lpuart_Lin_Ip_statusType Lpuart_Lin_Ip_SyncSendFrameData (uint32 u32Instance, const uint8 pTxBuff, uint8 u8TxSize); Sync/Async: Sync Reentrancy: Non Reentrant Parameters: [in] u32Instance LIN Hardware Interface u32u32Instance number [in] pTxBuff source buffer containing 8-bit data chars to send [in] u8TxSize the number of bytes to send Return value: STATUS_SUCCESS The transmission is successful STATUS_TIMEOUT The transmission has timeout Description: This function sends a frame using a synchronous method LPUART_LIN_008_002: his function shall send frame data out through the LIN Hardware Interface module using a blocking method. The function does not return until the transmission is completed. LPUART_LIN_008_003: This function shall return STATUS_SUCCESS, if the transmission is complete successfully. LPUART_LIN_008_004: This function shall return STATUS_TIMEOUT, if timeout has occurred. # SyncReceive LPUART_LIN_011_001: Service name: Lpuart_Lin_Ip_SyncReceiveFrameData Syntax: Lpuart_Lin_Ip_statusType Lpuart_Lin_Ip_SyncReceiveFrameDatas(uint32 u32Instance, uint8 pRxBuff,

ID	Subtype	Headline and Description
		uint8 u8RxSize); Sync/Async: Sync Reentrancy: Non Reentrant Parameters: [in] u32Instance LIN Hardware Interface u32Instance number [out] u8RxBuff A pointer to the buffer containing 8-bit received data [in] u8RxSize The number of bytes to receive Return value: STATUS_SUCCESS The receives frame data is successful. STATUS_TIMEOUT The checksum is incorrect. STATUS_BUSY Bus busy flag is true. STATUS_ERROR Operation failed due is equal to 0 or greater than 8 or node's current state is in SLEEP mode Description: This function receives a frame in a synchronous manner. LPUART_LIN_011_002: This function shall get (receive) data from the LIN Hardware Interface module using a blocking method (This function shall not return until the receive is completed) LPUART_LIN_011_003: This function shall return STATUS_SUCCESS, if the transmission is complete successfully. LPUART_LIN_011_004: This function shall return STATUS_TIMEOUT, if timeout has occurred. "
ARTD-3750	Bug	[UART] Fix compiler warnings<*> Fix compiler warnings
ARTD-3755	New	New Feature [LIN] Fix MISRA and CW ,,Fix MISRA and CW
ARTD-3767	Bug	[CAN][SWS_Can_00373] Can_Mainfunction_Mode shall call the function CanIf_ControllerModeIndication<*> A> Look inside Can_Ipw_MainFunction_Mode, obviously see that no call of CanIf_ControllerModeIndication is in place! => Need to be implemented as the srs: SWS_Can_*00373*: The function Can_Mainfunction_Mode shall call the function CanIf_ControllerModeIndication to notify the upper layer about a successful state transition of the corresponding CAN controller referred by abstract CanIf ControllerId, in case the state transition was triggered by function Can_SetControllerMode. B>* Can_SetControllerMode(Controller, CAN_CS_STARTED*); always return E_OK (see the implementation of FlexCAN_Ip_SetStartMode for detail) TC_ID: CAN_TC_FCT_*1685
ARTD-3770	New	New Feature [ADC] Add support for TempSense ,,Add support for TempSense functions as mentioned by requirements available in CPRT
ARTD-3777	New	New Feature

ID	Subtype	Headline and Description
		[LIN][S32K3XX] Add exclusive areas ,,Add exclusive area
ARTD-3780	Bug	[SPI] Make sure total frames in TX FIFO and RX FIFO lower than FIFO size<*> 1. For Ip_SyncTransmit(): After driver code read all frames in RX FIFO, if there are still some frames in TX FIFO, at the time before driver code check number of frames available in TX FIFO to prepare to fill TX FIFO. At that time, interrupt occurred, and the time to process interrupt is longer than the time to transfer all frames in TX FIFO. So TX FIFO will be empty and some frames received in RX FIFO, then the program is returned from interrupt and fill TX FIFO until full. And there is a interrupt occurred after that before read all frames in RX FIFO, and the time to process interrupt is longer than the time to transfer all frames in TX FIFO. So, RX FIFO can be overflow. 2. For Ip_AsyncTransmit(): The same situation with Ip_SyncTransmit() can be occurred. In SPI interrupt function Ip_TransferProcess(), after driver code read all frames in RX FIFO, if there are still some frames in TX FIFO, at the time before driver code check number of frames available in TX FIFO to prepare to fill TX FIFO. At that time, another interrupt occurred and preemptive current interrupt, and the time to process that interrupt is longer than the time to transfer all frames in TX FIFO. So TX FIFO will be empty and some frames received in RX FIFO, then the program is returned from that interrupt and fill TX FIFO until full and exist SPI interrupt function. And if there is a interrupt occurred with higher priority of SPI interrupt and the time to process that interrupt is longer than the time to transfer all frames in TX FIFO. So, RX FIFO can be overflow due to SPI interrupt function is not serviced to read RX FIFO.
ARTD-3787	Bug	[CAN] Driver does not prevent CanControllerDefaultBaudrate from being referenced to another controller's baud-rate configuration on tresos<*> Test configuration: Controller 0: The baud rate is configured to enable FD mode. (_ctrl0_bdr_cfg0_) Controller 1: The baud rate is configured to disable FD mode. (_ctrl1_bdr_cfg0_) Can Controller Default Baudrate (in controller 1) is referred to ctrl0_bdr_cfg0 Code generated successfully. This results in even if ctrl1_bdr_cfg0 is configured in normal-mode, but ram-block configuration is allowed and leading to some other undesired action. !image-2020-11-09-15-23-15-419.png!
ARTD-3815	Bug	[Adc] Group conversions started after a Self-Test will have ADC_BUSY as group status<*> Detailed description (how to reproduce it): Adc group status can not change to ADC_STREAM_COMPLETED after implement self test because: Set up voltage: AN_2: 1V AN_5: 2V After group convert completely in ISR, AN_2 cdr register don't have valid bit and value is 0 as in attachment Preconditions: Enable self test feature Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_301

ID	Subtype	Headline and Description
		Observed behavior: / Execute self-test function / t_u8SelfRet = Adc_SelfTest(t_u8HwUnitIndex); / Start ADC group conversion / Adc_StartGroupConversion(t_u16AdcGroupType); / Expected STREAM_COMPLETE group / EU_ASSERT(ADC_STREAM_COMPLETED == Adc_GetGroupStatus(t_u16AdcGroupType)); Real status: ADC_BUSY Expected behavior: Group status is ADC_STREAM_COMPLETED Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-3821	Bug	 [WDG] Configurator does not display any warning when Wdg_au32Timeout [Wdg_Instance] is overflowed<*> Detailed description (how to reproduce it): Step 1: Config ' Wdg configuration: AutosarExt: Wdg Enable Direct Service: FALSE Wdg Disable Allowed: TRUE Wdg Initial Timeout [s]: 0, 0.001, 32.0, 64.534, 65.535 Default mode setting: Wdg Timeout Period[s]: 1.0) Other mode WdgTimeoutPeriod: 10.0 Step 2: Call Gpt_Init function Step 3: Call Wdg_Init function Step 4: Delay-> Verification Point: The program is not reset Step 5: De-Initialize WDG Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Wdg_TC_FCT_1006 Observed behavior: When Wdg_au32Timeout [Wdg_Instance] is overflowed but doesn't have any warning display for user: with Wdg_au16CfgInitialTimeout = 64.534 or 65.535 and Wdg_u32TriggerSourceClock = 80000 Detail was attached. Expected behavior: Displays warning to user when the Wdg_au32Timeout [Wdg_Instance] is overflowed Check also S32CT component
ARTD-3825	New	 New Feature [S32K344] OCU: Align eMIOS IRQ code with MCL ,,"Align driver code with MCL eMIOS common interrupt handler implementation. MCL code will treat the common handler interrupt point and will route to driver that uses the corresponding channel."
ARTD-3838	New	 New Feature

ID	Subtype	Headline and Description
		[PORT] Add support for touch senses feature for S32K3XX ,,"TSPC_PORT_001_001*: ""A function, named Siul2_Port_Ip_EnableOBEGroup shall enable the specified group whose pads are participating in simultaneous transition"" TSPC_PORT_001_002: The specifications for the Siul2_Port_Ip_EnableOBEGroup function shall be: Service name: Siul2_Port_Ip_EnableOBEGroup Syntax: void Siul2_Port_Ip_EnableOBEGroup(uint8 group); Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): group->number of the OBE group that has to be enabled Parameters (inout): None Parameters (out): None Return value: None Description: This function enables the specified group whose pads are participating in simultaneous transition. Available via: Tspc_Port_Ip.h TSPC_PORT_002_001*: ""A function, named Siul2_Port_Ip_ConfigureOBEGroup shall configure which channels participate in the OBE group."" TSPC_PORT_002_002: The specifications for the Siul2_Port_Ip_ConfigureOBEGroup function shall be: Service name: Siul2_Port_Ip_ConfigureOBEGroup Syntax: void Siul2_Port_Ip_ConfigureOBEGroup(uint8 group, uint32 groupValue_p); Sync/Async: Synchronous Reentrancy: Non Reentrant Parameters (in): group->number of the OBE group that has to be enabled Parameters (in): groupValue_p->Pointer to the first word of the OBE group configuration Parameters (inout): None Parameters (out): None Return value: None Description: This function enables the specified group whose pads are participating in simultaneous transition. Available via: Tspc_Port_Ip.h CPR_RTD_00439.port*: ""The Touch Sensing Pin Coupling support shall be enabled/disabled using a parameter named TSPC Support Implemented in the PortGeneral container. The default value of this Parameter shall be FALSE"" CPR_RTD_00440.port*: ""The Group Output Buffer Select functionality shall be configurable for each Port Pin that supports this feature. For this, a parameter named OBE Group Select shall be implemented in the PortPin container. The OBE Group Select parameter can have the following values NO_OBE_GROUP, OBE_GROUP1, OBE_GROUP2 ... . The default value for the OBE Group Select shall be NO_OBE_GROUP (no simultaneous OBE transition). This parameter shall be editable only when TSPC Support is configured as TRUE"""
ARTD-3930	Bug	[ADC] The notification field is not defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. ,,"Detailed description (how to reproduce it): The notification field is not defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. Preconditions: Check ADC use BCTU mode. Observed behavior:

ID	Subtype	Headline and Description
		The notification field is not defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. Expected behavior: The notification field is defined for use in the Adc_CtuEnableNotification, Adc_CtuDisableNotification function. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ARTD-3935	Bug	[SPI] Do nothing and return E_NOT_OK when set LSB and Frame size fail<*>
		
		in Spi_Ipw_SyncTransmit :
		Before call IP_Sync function to perform transmission for the channel, LSB and Framesize setup function were called but after that, it call Ip_Sycn function without check the status return of those fucntion. it should be like:
		Status = Lpspi_Ip_UpdateFrameSize();
		if(Status = OK)
		{
		Status = Lpspi_Ip_UpdateLsb();
		if(Status = OK)
		{
		status = Lpspi_Ip_SyncTransmit();
		}
		}

ARTD-3938	Bug	[SPI] The number of bytes transfer of channel should be configured corresponding to frame size of channel<*> Currently, SPI driver is supporting transfer with frame size is 4 to 32 bits. The design of driver now will lose some bytes of each channel if it don't have the compatible configuration: Details: If framesize is 16, number of bytes transfer is not divisible by 4 then all surplus bytes (%4) will be lost and missed. the same for 32 bits mode Solving: IB: In configuration, update a invalid expression to prevent user configure wrong number of bytes transfer for each channel. (example on EB tresos: SpiIbNBuffers and SpiDataWidth must be compatible) EB: Should be added a detect error for this case in Spi_SetupEB() function. Take a note in UM document to mention user can has valid channel configuration
ARTD-4000	Bug	[uart] Update the used schema for all the .component files to 8.0 version<*> The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"
ARTD-4008	Bug	[qd] Update the used schema for all the .component files to 8.0 version<*>

ID	Subtype	Headline and Description
		The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"
ARTD-4027	Bug	[ICU] Review attached reported errors images and correct<*> Review attached images on the parent ticket and conclude if fixes are done. <<Follow up for issues reported on EAR phase and update code and configuration see attachement and <[test team link https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/onedrive.aspx?id=%2fpersonal%2fviet_nguyen_nxp_com%2fDocuments%2fNotebooks]>> # [[FIXED] BUG_ICU_010: Some functions have no prototype|#BUG_ICU_010%20Some%20functions%20have%20no%20&section-id=612f7f9c-f779-4595-a0f6-1e81015370f8&page-id=6086406f-bef7-49a1-ad89-194e6e25e07d&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/Doc.aspx?sourcedoc=\{d858b9ba-6641-4816-9d4a-2223dcea36f5}&action=edit&wd=target%28ICU.one%7C612f7f9c-f779-4595-a0f6-1e81015370f8%2FBUG_ICU_010%20Some%20functions%20have%20no%20%7C6086406f-bef7-49a1-ad89-194e6e25e07d%2F%29&wdorigin=703&wdpreservelink=1]) > For this bug we have to eliminate Emios_Icu_Ip_EnableChannel() an Emios_Icu_Ip_DisableChannel() from ICU EMIOS IP code and use functions from MCL: Emios_Mcl_Ip_EnableChannel() and Emios_Mcl_Ip_DisableChannel(). # [[FIXED] [DevReview]BUG_ICU_009: The Masterbus counter is turned off when transmitting the Icu_DeInit () function.|#%5BDevReview%5DBUG_ICU_009%20The%20&section-id=612f7f9c-f779-4595-a0f6-1e81015370f8&page-id=f6a0bc77-192c-46d4-82ff-5fdf37d3d3ef&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/Doc.aspx?sourcedoc=\{d858b9ba-6641-4816-9d4a-2223dcea36f5}&action=edit&wd=target%28ICU.one%7C612f7f9c-f779-4595-a0f6-1e81015370f8%2F%5BDevReview%5DBUG_ICU_009%20The%20%7Cf6a0bc77-192c-46d4-82ff-5fdf37d3d3ef%2F%29&wdorigin=703&wdpreservelink=1]): No driver should change global configuration of EMIOS without assuring it using all the instance or all the channels for a specific MusterBus, for this we have MCL functions to change the global configuration. # [[FIXED] BUG_ICU_011: Max counter is not set in Edge count function|#BUG_ICU_011%20Max%20counter%20is%20not%20&section-id=612f7f9c-f779-4595-a0f6-1e81015370f8&page-id=088f5935-19df-48df-89a2-e8745fb3e9ab&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/15/Doc.aspx?sourcedoc=\{d858b9ba-6641-4816-9d4a-2223dcea36f5}&action=edit&wd=target%28ICU.one%7C612f7f9c-f779-4595-a0f6-1e81015370f8%2FBUG_ICU_011%20Max%20counter%20is%20not%20%7C088f5935-19df-48df-89a2-e8745fb3e9ab%2F%29&wdorigin=703&wdpreservelink=1]) Spoke again with tester about this BUG. VERIFY THAT ALL FUNCTIONS CAN BE USED IN BOTH MODES: AUTOSAR AND IPL standalone.
ARTD-4054	Bug	

ID	Subtype	Headline and Description
		[ADC] Adc group status can not change to ADC_STREAM_COMPLETED when using Module clock frequency / 8<*> Detailed description (how to reproduce it): Adc group status can not change to ADC_STREAM_COMPLETED when using Module clock frequency / 8 because: Set up voltage: AN_48: presampling, by pass pre sampling 0V AN_95: presampling, by pass pre sampling 3.3V After group convert completely in ISR, AN_48 cdr register don't have valid bit and value is 0 as in attachment In RM there are some conflicts: MCR_ADCLKSEL select Module clock frequency / 8 is valid but in chapter 23 clock source for div8 is not valid as attachment Preconditions: Using ADCLKSEL = 0x3 (Module clock frequency / 8) Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0301 Observed behavior: / Start ADC group conversion / Adc_StartGroupConversion(t_u16AdcGroupType); / Expected STREAM_COMPLETE group / EU_ASSERT(ADC_STREAM_COMPLETED == Adc_GetGroupStatus(t_u16AdcGroupType)); Real status: ADC_BUSY Expected behavior: Group status is ADC_STREAM_COMPLETED Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-4370	Bug	[S32K3][EMIOS][MCL] Enabling EmiosMclLowPowerMode will prevent user from creating config channels in Emios Master Buses tab<*> Enabling EmiosMclLowPowerMode will prevent user from creating config channels in Emios Master Buses tab !MicrosoftTeams-image.png|thumbnail!
ARTD-4393	Bug	[S32K3][MCL] Cannot use the IRQ function in Emios_Mcl_Ip_Irq.c file<*> There's MCL_EMIOS_0_CH_X_ISR_USED(Emios_Mcl_Ip_Irq.c file). But i don't see it generated or defined anywhere, user cannot use the IRQ function
ARTD-4397	Bug	[CAN] Can_SetControllerMode shall cancel pending msg in case of Rx mailbox/ POLL<*> !image-2020-11-19-11-01-47-182.png! IIn case of POLL Rx processing type, abort will not work because FLEXCAN_MB_RX_BUSY == state->mbs[mb_idx].state only be satified if main_function_read was called All flags should be cleared before module enter stop mode, if not, Main_function API that can be called after that and executing processing in stop-mode can cause unexpected behavior IC_ID: CAN_TC_FCT_*1584

ID	Subtype	Headline and Description
		CAN_TC_FCT_5552 => for FIFO
ARTD-4401	Bug	[GPT] The Standby wakeup feature of Gpt does not work correctly according to the requirement<*> After calling Gpt_Init function, I found that the counter bit and interrupt bit of RTC IPW is cleared. So this does not match with the requirement as following: The Gpt driver shall provide an optional configuration parameter to support wakeup IP operation across STANDBY. Per default this optional functionality and configuration parameters shall be disabled. If the configuration parameter is enabled, the following shall be respected: The driver shall NOT CLEAR the interrupt flag, the interrupt enable bit and also should not disable the counter, during init, after a wakeup event. Please refer to the image attached to see error.
ARTD-4418	Bug	[SPI] Expression to check maximum "instance" is not correct ,,"if (instance > LPSPI_INSTANCE_COUNT) Should be replaced by if (instance >= LPSPI_INSTANCE_COUNT)
ARTD-4427	Bug	[BASE] OsIf_Internal.h may not found the macro USING_OS_AUTOSAROS<*> OsIf_Internal.h has the follwoing section: #if defined(USING_OS_AUTOSAROS) #include "Os.h" #endif / defined(USING_OS_AUTOSAROS) / But OsIf_Cfg.h is not included so that USING_OS_AUTOSAROS is never defined.
ARTD-4439	Bug	[SPI] SPI module use wrong function name for exclusive area<*> Spi uses defines like SchM_Enter_Spi_EXCLUSIVE_AREA_00(); It should be SchM_Enter_Spi*_SPI*_EXCLUSIVE_AREA_00()
ARTD-4446	Bug	[S32K3][EMIOS_MCL] Refactor EMIOS functions with respect to requirements<*> The following APIs should be merged in one to respect for the ZTH arhitecture: Emios_Mcl_Ip_InitChannel Emios_Mcl_Ip_InitInstance => Emios_Mcl_Ip_Init() which will respect the next requirement: EMIOS_MCL_IP_001_001 Emios_Mcl_Ip_DinitChannel Emios_Mcl_Ip_DeinitInstance => Emios_Mcl_Ip_Deinit() which will respect the next requirement: EMIOS_MCL_IP_002_001
ARTD-4457	Bug	[S32K3XX][GPT] The return value of PIT RTI Timer is wrong after starting timer<*> After starting timer PIT RTI by calling function Gpt_StartTimer with the target timer value as a parameter, in term of requirement, the value of elapsed time must to be 0 because Timer just start to running. But when i debug this, the real elapsed value of timer equals the target timer value. I saw in debug interface that the counter of PIT RTI Timer after calling Gpt_StartTimer function, the counter of RTI has not yet started because some issue related to the delay of counter. I think this problem maybe is referred to some information in RM but i am not sure.

ID	Subtype	Headline and Description
		I attached an image when i debugged this, please refer to it to see the problem more details.
ARTD-4468	Bug	[WDG] The S32CT example project has warnings<*> Detailed description (how to reproduce it): Step 1: Import example project into S32DS Step 2: Open Peripherals tab and Update code Step 3: Build code Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The example project issues warnings at generation and build stage Actually, only one of these warning caused by swt_ip component which's "WDG_RAM undefined" Detail was attached. Expected behavior: The project no warnings, errors after generate and build code Fix typos in description.txt: *application, through
ARTD-4470	Bug	[S32K3XX][I2C] I2c baudrate at I2cHighSpeedModeConfiguration container always check I2c prescaler<*> I2c baudrate at I2cHighSpeedModeConfiguration container always check I2c prescaler in Master Mode
ARTD-4472	Bug	[PORT] Not all GPI mode were defined as Only input mode in Port driver for S32K3XX<*> The GPI mode are configuring as Only Input mode in csv files. It is incorrect
ARTD-4485	New	New Feature [S32K3XX][I2C] Should add Det to avoid the StartListening is called when SlaveListening is true ,,Should add Det to avoid the StartListening is called when SlaveListening is true
ARTD-4498	New	New Feature [UART] - Fix memory sections ,,The memory sections shall be added/fixed in the lpuart and flexio drivers.
ARTD-4502	Bug	[S32K3XX][MCU][S32CT][EXAMPLE] Compiler warning on S32CT when build for gcc<*> Detailed description (how to reproduce it): Step 1: Import example project into S32DS Step 2: Open Peripherals tab and Update code Step 3: Build code Preconditions: [...] Test Case ID (internal TC that caught the defect) optional:

ID	Subtype	Headline and Description
		[...] Observed behavior: All examples use MCU when build code is warning after updating the code. Detail was attached. Expected behavior: The project no warnings, errors after build code. Readme for clock and power is incorrect
ARTD-4505	Bug	[Uart] First byte is wrong when transmit data after using Abort function<*> First byte is wrong when transmit data after using Abort function: Expect sending data : 0x01; 0x02;0x03;0x4;0x05;0x06;0x07;0x08 Reception data : 0xff; 0x01; 0x02;0x03;0x4;0x05;0x06;0x07
ARTD-4510	Bug	[PWM] Cannot update duty cycle value at runtime when newDutyCycle is greater than old period value<*> In Emios_Pwm_Ip_SetDutyCycle function, Register B not update intermediate at runtime, so when we gets the value from reg B , it still return old period value. It cause EMIOS_PWM_STATUS_ERROR when newDutyCycle value is greater than old period value.
ARTD-4520	Bug	[PWM] Check DevAssert is not correct in Emios_Pwm_Ip_InitEdgePlacementMode function<*> in OPWMB mode, selected counter bus should be MCB Up counter. So, condition: DevAssert(EMIOS_IP_MCB_UP_DOWN_COUNTER == Emios_Pwm_Ip_GetCounterBusMode(instance, userChCfg->channelId, userChCfg->timebase)); is not correct. It should be compare with EMIOS_IP_MCB_UP_COUNTER In Emios_Pwm_Ip_GetCounterBusPeriod function, you are using Emios_Mcl_Ip_GetCounterBusMode, and input channel parameter is eMios channel that configured in PWM. It will get counter bus mode = 0, because we haven't configured it yet. So, it is always equal to the BUS_A value. it is not correct. it should be channel that configured by MCL to check using counter bus
ARTD-4522	Bug	[PWM] Pwm_SetPeriodAndDuty function cannot run with input period value = 0<*> When use Pwm_SetPeriodAndDuty function with eMios ipv Emios_Pwm_Ip_SetPeriod function, we cannot pass condition: DevAssert(EMIOS_PWM_MIN_CNT_VAL <= newPeriod); when EMIOS_PWM_MIN_CNT_VAL =1; Please follow requirement: SWS_Pwm_00150: If the period is set to zero the setting of the duty-cycle is not relevant. In this case the output shall be zero (zero percent duty-cycle) for Pwm_SetPeriodAndDuty function
ARTD-4526	Bug	[WDG] The Tresos example project issue warnings at generation stage<*> Detailed description (how to reproduce it): Step 1: Compile plugin Step 2: Use cmd command to "E:\Zebra\Repo\S32K3XX\output\eclipse\plugins\Wdg_TS_T40D34M8I1R0\examples\EBT\Wdg_Example" Step 3: make clean generate Step 4: make build Step 5: make run Preconditions:

ID	Subtype	Headline and Description
		[...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: The project generate code display some warnings Fix typos in wdg_example_readme.txt* (EB) and description.txt (S32CT): aplication, throguh, instalation Detail was attached. Expected behavior: The project generate code no warnings, errors Fix typos in description.txt: *application, through, installation
ARTD-4533	Bug	[I2c][S32K3XX] Interrupt flag should be cleared for spurious interrupts<*> Interrupt flag should be cleared for spurious interrupts.
ARTD-4535	Bug	[S32K3XX] FLS Missing declare variable ProgrammedData in C40_Ip.c<*> the 'pProgrammedData' variable is undefine at line 1064 of C40_Ip.c when :below nodes to be set such as: (STD_ON == C40_ATERNATE_INTERFACE_ENABLED) and (C40_ERASE_VERIFICATION_ENABLED = STD_ON) and (STD_OFF == C40_PROGRAM_VERIFICATION_ENABLED) and (STD_OFF == C40_IP_SYNCRONIZE_CACHE)
ARTD-4540	Bug	[CAN] Multicore issue with K3 platform, with enabled cache ,,"Multicore can not be executed See attached file for details. if put global array to non-cache region. issue can be solved TC_ID: CAN_TC_MC_0560
ARTD-4550	Bug	[SPI] Fix misra violation on DSPI and FLEXIO<*> Fix misra violation
ARTD-4555	Bug	[ADC] Fix remaining static analysis violations (MISRA + HIS + CERT-C)<*> All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]
ARTD-4558	New	New Feature [SENT] Fix VSMD warnings ,,"The following warnings from the VSMD reports must be fixed :

ID	Subtype	Headline and Description
		Rule A205: Reference 'Sent/SentConfigSet/SentControllerConfig/SentControllerEcucPartitionRef' has no 'ECUC-VALUE-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentFastCRCErrorNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentSlowCRCErrorNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentFastNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A205: Parameter 'Sent/SentConfigSet/SentControllerConfig/SentChannelConfig/SentSlowNotification' has no 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' elements. Rule A207: 'Empty string' should not be used as default value of parameter 'Sent/CommonPublishedInformation/VendorApiInfix'. Rule A220: UUID 'ECUC:4e05c426-67f4-4e47-b644-7749e78ec98d' is not unique for 'SentTimeout'"
ARTD-4560	Bug	 [CAN] implement Dma Error notification for enhance fifo & Missing 'ECUC-MULTIPLICITY-CONFIGURATION-CLASS' for optional Node (TpsEcuc_08037)<*> CanEnhanceFiFoDmaRef is an optional node, => need to have ECUC-MULTIPLICITY-CONFIGURATION-CLASS. need to update: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS"> <icc:v vclass="PreCompile">VariantPreCompile</icc:v> <icc:v vclass="PreCompile">VariantPostBuild</icc:v> </a:a> to: <a:a name="IMPLEMENTATIONCONFIGCLASS" type="IMPLEMENTATIONCONFIGCLASS"> <icc:v vclass="PreCompile">VariantPreCompile</icc:v> <icc:v vclass="PreCompile">VariantPostBuild</icc:v> <icc:v mclass="PreCompile">VariantPreCompile</icc:v> <icc:v mclass="PreCompile">VariantPostBuild</icc:v> </a:a>
ARTD-4599	New	 New Feature [ADC] ADC_SAR IPL S32CT add a more user-friendly method for enabling the channels in each chain ,,"If my assumption is correct, for now, in order to enable ADC channels in either Normal or INJECTED chain, user must compute an type the masks for the desired channels. This forces the user to read the ADC chapter from the Reference Manual, to get the channels mapping, identify the correct registers and compute the values. This complicates too much the process for the end user. !image-2020-11-25-17-15-15-003.png! This process can be simplified for the end user by replacing the above fields with some checkboxes for each channel. My suggestion is to have a look on the S32SD for Power Architecture PEX options for the ADC, because the MPC5744P has a very similar ADC peripheral.

ID	Subtype	Headline and Description
		More than that, why the Channel configuration array should have at leas one element if, for example I don't want to have the below notifications enabled for none of the channels enabled in the above fields, only the end of chain notification? !image-2020-11-25-17-41-06-410.png|width=545,height=133! To have an idea on why we request this, let me explain the following scenario: In Model-Based Design Toolbox, we create blocks for Simulink that will generate C code automatically. If a user needs an ADC conversion, he/she will add an ADC block. The block will open Config Tools. Now the user must read the RM, understand how the ADC works, compute registers values and then set the other proper settings. While he could just open the Config Tools, enable every channel with one click, and that's it."
ARTD-4600	Bug	[I2C][S32K3XX] Fix MISRA violations for I2c driver<*> All MISRA errors should be fixed/motivated for I2c driver.
ARTD-4601	New	New Feature [ICU] Provide API for reading the comparator status ,,"NewWorkDescription: The Icu driver shall provide an API for reading the comparator status It shall allow the user to pool for the status on selected comparator and return a value for distinguishing if comparator was triggered or not. Icu_GetInputState(logic_channel); Considered that this ticket should not add new HLD requirement at this point. The API should be implemented and requested on IP level as Cmp_Ip_TriggerStateType Cmp_Ip_GetStatus(cmp_channel); Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API as in NW Description. The API will return if the current selected CMP resource was triggered or not and will clear the status after reading."
ARTD-4602	Bug	[ICU] Align eMios icu CT component generation to ebt ip generation<*> Update and correct emios generation in ct for icu. Perform a check with DS example and build emios icu with new mcl.
ARTD-4605	Bug	[SAI] Fix remaining static analysis violations (MISRA + HIS + CERT-C)<*> All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230

ARTD-4618	Bug	[WDG] Does not return error status when the unlock sequence is not successful after a timeout loop<*>
		
		Should return status error when software unlock is not successful after timeout loop.
		/* Soft lock */
		if ((base->CR & SWT_CR_SLK_MASK) != 0U)
		{
		/* Unlocks sequence */
		base->SR = SWT_SR_WSC(SWT_IP_UNLOCK_VALUE1);
		base->SR = SWT_SR_WSC(SWT_IP_UNLOCK_VALUE2);

ID	Subtype	Headline and Description

		/* Waits unlock complete */
		while (((base->CR & SWT_CR_SLK_MASK) != 0U) && (timeout-- > 0))
		{
		/* Do nothing */
		}
		}

ARTD-4625	Bug	[SPI][LPSPI] IER register was clearing twice in Lpspi_Ip_AsyncTransmit function<*> in Lpspi_Ip_AsyncTransmit, if current master mode is Polling, it is clearing IER register twice.

ARTD-4626	Bug	[PWM]Emios_Pwm_Ip_GetCounterBusPeriod confused with Emios_Ip_GetCounterBusMode<*>
		
		The function "Emios_Pwm_Ip_GetCounterBusPeriod" called "Emios_Ip_GetCounterBusMode" because it needs to know the counter bus type.
		The following line of code is of problem:
		chBusMode = Emios_Ip_GetCounterBusMode(instance, channel);
		chBusMode is "Emios_Pwm_Ip_CounterBusSourceType";
		But function "Emios_Ip_GetCounterBusMode" returns "Emios_Ip_MasterBusModeType". They are different.
		
		Maybe we should add another API function as following:
		Emios_Pwm_Ip_CounterBusSourceType Emios_Ip_GetCounterBusSource(uint32 instance, uint8 channel)
		{
		eMIOS_Type base = Emios_Ip_Bases[instance];
		return (base->CH.UC[channel].C & eMIOS_C_BSL_MASK) >> eMIOS_C_BSL_SHIFT;
		}

ARTD-4639	Bug	[ADC] The value config class of node "BctuFifoDmaBuffer", "BctuFifoDmaChannelId" is invalid ,,"Detailed description (how to reproduce it): Use EB Tresos config with case variant = 3. The nodes BctuFifoDmaBuffer"", ""BctuFifoDmaChannelId"" have the value config class is Precompile but when configuring, the values in other variants will not change. Preconditions: NA Observed behavior: when configuring, the values in other variants will not change. Expected behavior: when configuring, the values in other variants will change. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-4641	Bug	[S32K344 BETA] GPT compiler warnings<*> Please refer to the attached file to see the detail error
ARTD-4648	Bug	

ID	Subtype	Headline and Description
		[ADC] The function "Adc_ReportDetError" declared implicitly when configuration AdcEnableReadRawDataApi is true and AdcDevErrorDetect is false ,,"Detailed description (how to reproduce it): when configuration AdcEnableReadRawDataApi is true and AdcDevErrorDetect is false => the build fails Adc_TS_COT_003 CFG_SETS=81. Preconditions: N/A Observed behavior: ...\output\eclipse\plugins\Adc_TS_T40D34M8I1R0\src\Adc.c"",4519 Error[Pe223]: function ""Adc_ReportDetError"" declared implicitly Expected behavior: In this case, it will build success. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-4652	New	New Feature [S32K3XX][PWM] Fix and comment static analysis violations (MISRA + HIS + CERT-C) ,,"All static analysis need to be fixed for the BETA release. Everything needs to be fixed in the code or commented in Coverity if it cannot be fixed. The following wiki is work in progress, but it will be updated with all needed information: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230] "
ARTD-4653	Bug	[PWM] Pwm_Notification has no prototype<*> STDERR:"C:\vv_tools\eb\EB_tresos_Studio_27.1.0_b200625-0900_02\plugins\Pwm_TS_T40D34M8I1R0\src\Pwm.c",2253 Error[Pa045]: function "Pwm_Notification".mcal_text"" has no prototype. It causes a build error with IAR compiler.
ARTD-4667	New	New Feature [FLS] Remove all redundant code relate to IRQ mode ,,"Since Fls driver no longer supports IRQ mode, all redundant code should be removed"
ARTD-4669	Bug	[PWM] Fix Compiler warning for S32K3XX EAR 0.8.1<*> Fix Compiler warning for PWM S32K3XX EAR 0.8.1. Please see in attach file.
ARTD-4679	Bug	[PWM] Pwm_SetOutputToIdle function is not working as expected<*> Pwm_SetOutputToIdle function is not working as expected. It just sets the required PWM pin state for current cycle and continues with normal PWM operation from next cycle. Due Force Match bit is always automatically returned the field to 0.
ARTD-4682	New	New Feature

ID	Subtype	Headline and Description
		[SPI] Change SpiPhyUnitAsyncMethod to boolean node SpiPhyUnitAsyncUseDma ,,"Meaning of SpiPhyUnitAsyncMethod node is to select Asynchronous mechanism with DMA or not. So, that node can operate as an boolean node SpiPhyUnitAsyncUseDma. if SpiPhyUnitAsyncUseDma = false, the AsyncTransmit can be operated with interrupt or polling of SPI transfer flags. if SpiPhyUnitAsyncUseDma = true, the AsyncTransmit can be operated with interrupt or polling of DMA done flag."
ARTD-4715	Bug	[SPI] CS will be cleared during continues transfer<*> 1, CS will be cleared during continues transfer if second command with CONT =1 and CONTC =1 is written immediately after first command with CONT =1 and CONTC =0. Seem second command will be delayed to updated. =>So, In continuous CS, only set new command with CONTC=1 for next channel in Job(first command for first channel in Job should have CONTC = 0). 2, In slave mode, if data is filled into TX FIFO then reset TX FIFO by CR[RTF]=1 will not clear shifter. => So, Ip_Cancel() function must use software reset bit CR[RST] to clear old data in shifter. 3, In Master mode and under debug mode, CR[DBGEN] = 0, CS will be cleared automatically when CPU halt at breakpoint regardless of TCR[CONT]=1 or TCR[CONTC]=1. => CR[]BGEN] should be enabled to ensure CS will be kept when CPU halts at breakpoint.
ARTD-4773	Bug	[ADC] Data conversion should not be recorded for disabled channels<*> Data conversion should not be recorded for disabled channels Limit check is still checked even for channels that are disabled via ADC_ENABLE_CH_DISABLE_CH_NONAUTO_API
ARTD-4836	Bug	[Uart] Macro in driver does not observed description in requirement<*> Driver is using naming macro "UART_E_INVALID_COREID" But in requirement, this macro must be UART_E_PARAM_CONFIG CPR_RTD_00420.uart|If DET error reporting is enabled, the UART will check upon each API call if the requested resource is configured to be available on the current core, and in case of error will return UART_E_PARAM_CONFIG.
ARTD-4833	New	New Feature [PORT] Add Port_SetAsUnusedPin and Port_SetAsUsedPin functionality for S32K3XX ,,"NewWorkDescription: Implement requirements: CPR_RTD_00425.port: The function void Port_SetAsUnusedPin(Port_PinType Pin) shall configure the referenced pin with all the properties specified in the NotUsedPortPin container. CPR_RTD_00426.port: If Det is enabled, the function Port_SetAsUnusedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE CPR_RTD_00427.port: The function void Port_SetAsUsedPin(Port_PinType Pin) shall configure the referenced pin with all the properties that where set during the Port_Init operation.

ID	Subtype	Headline and Description
		CPR_RTD_00428.port: If Det is enabled, the function Port_SetAsUsedPin shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE. CPR_RTD_00429.port: Port_SetAsUnusedPin and Port_SetAsUsedPin functionalities will be enabled/disabled by using a boolean precompile parameter named ""Port Set As Unused Pin API"" Requirement source: CPR_RTD_00425.port, CPR_RTD_00426.port, CPR_RTD_00427.port, CPR_RTD_00428.port, CPR_RTD_00429.port (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:"
ARTD-4844	Bug	[GPT] The channel number checking of PIT in driver is wrong result to hardfault error<*> With resource of S32G274, The number channel of PIT 0 is not equal to PIT 1. So the number channel checked in interrupt function must to be diferrent each other between PIT 0 and PIT1. In addition, in case the PIT instance contains RTI channel, it should be checked to differentiate between some chip. Please refer to attached image to see the issue.
ARTD-4849	New	New Feature [ADC]: CTU Trigger Mode support with HW triggered groups on multiple cores ,,"Multicore support for CTU Trigger Mode (CTU HW triggered groups must be configured and used only on a single core) Implemented on Tresos and S32CT."
ARTD-4850	Bug	[S32K3][MCL][EMIOS] Add EMIOS support in MCL HLD CT configuration<*> Need to add EMIOS files generation in CT.
ARTD-4872	Bug	[ADC] (ITG) Generate fail when configuring AdcLogicalUnitId at first place<*> Detailed description (how to reproduce it): Generate fail when configuring AdcLogicalUnitId at first place Preconditions: NA Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0101 Observed behavior: Generate fail: [e:\gitwork_rt\output\eclipse\plugins\Adc_TS_T40D11M10I0R0/generate_PB/Adc_RegOperations.m:2026]: Logical IDs must mach the element number in the HwUnit List container (node) Expected behavior: generate pass Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-4886	New	New Feature [PORT] Add support for UntouchedIMCR for S32K3XX

ID	Subtype	Headline and Description
		,,"Add support for UntouchedIMCR. Two things need to be checked: Check in Tresos configuration: out of range, configure one IMCR in both PortPin list and UntouchedIMCR list then Tresos should raise 1 error. Check in runtime: for example: Configure UntouchedIMCR 147 > call Port_Init() > then the IMCR147 should be keep its value "
ARTD-4891	New	 New Feature [PORT] Add Port_ResetPinMode functionality for S32K3XX ,,"NewWorkDescription: Implement Port_ResetPinMode functionality CPR_RTD_00422.port: The Port driver shall provide a autosar extension API with the prototype: void Port_ResetPinMode(Port_PinType Pin) . The function Port_ResetPinMode shall revert the port pin mode of the referenced pin to the value that was set by Port_Init operation. CPR_RTD_00423.port: If Det is enabled, the function Port_ResetPinMode shall report PORT_E_MODE_UNCHANGEABLE error and return without any other action, if the parameter PortPinModeChangeable is set to FALSE CPR_RTD_00424.port: Port_ResetPinMode functionality will be enabled/disabled by using a boolean precompile parameter named ""Port Reset Pin Mode API Per default this optional functionality and the configuration parameters shall be disabled Requirement source: CPR_RTD_00422.port, CPR_RTD_00423.port, CPR_RTD_00424.port (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional:"
ARTD-4916	Bug	 [S32DS3.4] Add dependencies between development package and SDK package for S32K3<*> Detailed description (how to reproduce it): 1. Help > S32DS Extensions and Updates 2. Click Go Preferences > Add update site for S32K3 3. Wait until package are loaded. Select SDKs package S32K3 4.4 RTD 0.8.1 then press "Next" button 4. Observe dependencies package in the next page 5. Finish Observed behavior: 4. Development packages do not show 5. Only SDK pack is installed Expected behavior: 4. Development packages should show as dependencies package 5. Dev pack & SDK pack are installed
ARTD-4915	Bug	 [S32DS3.4] Uninstall SW32 S32K3 RTD package should also remove SDK & all relevant<*> # Install SW32 S32K3 RTD package via MI # Uninstall SW32 S32K3 RTD package via MI # Go to the layout: <install_dir>\S32DS\integration <install_dir>\S32DS\software # Open S32DS on new workspace > SDK Management Observed behavior: 3. All relevant of S32K3 RTD still exist 4. SDK for S32K3 still exist

ID	Subtype	Headline and Description
		Expected behavior:* Uninstall SW32 S32K3 RTD package should also remove SDK & all relevant Note: This issue also occurs with RTD for SW32G2 version 1.0.0, & RTD for S32R45 version 2.0.0
ARTD-4902	New	 New Feature [S32DS 3.4] Should update detail description for RTD for S32K3 0.8.1 ,,"Steps: # Open S32DS, add update site for S32K3 dev package & S32K3 SDK package (com.nxp.s32ds.dev.packages.internal_3.4.0.20201203234449.zip) # Open S32DS Extension and Updates > Select S32K3 SDK package then observes overview # Install S32K3 SDK then open Installation Details > Installed software , select RTD S32K3 Observed behavior: 2. RTD for S32K3 version 0.8.1 3. RTD for S32K3 0.8.1 Expected behavior: 2 . Should update detail description for S32K3 SDK ex:** _**_ The S32 Software Development Kit (S32 SDK) is an extensive suite of peripheral drivers, RTOS, stacks and middleware designed to simplify and accelerate application development on NXP S32K3 ARM based microcontrollers. This S32 SDK supports development with the following devices: S32K314 S32K324 S32K334 3. Should update more detail, ex: ""S32 RTD SDK for S32K3xx Version 0.8.1"" "
ARTD-4920	Bug	 [PWM] Invalid type of generated code in PWM_DRIVER_STATE_INITIALIZATION<*> Vector got this error when compiling PWM code: CC Pwm.o "../../../external/ThirdParty/Mcal_S32k/Supply/SW32K3_RTD_4.4_0.8.1/eclipse/plugins/Pwm_TS_T40D34M8I1R0/src/Pwm.c", line 197: error #144: a value of type "void " cannot be used to initialize an entity of type "boolean" static Pwm_DriverStateType Pwm_aState[1U] = PWM_DRIVER_STATE_INITIALIZATION; As the pwmChannelIdleState[PWM_CONFIG_LOGIC_CHANNELS] has type as boolean, but generated code is "NULL_PTR".
ARTD-4931	New	 New Feature [SPI] Update driver according to requirements ,,Update driver according to requirements added to the ticket AAI-650
ARTD-4932	New	 New Feature

ID	Subtype	Headline and Description
		[SPI][FLEXIO_SPI] Move SpiDataWidth, SpiTransferStart, SpiDefaultData nodes from SpiPhyUnit to SpiExternalDevice for IP driver" ,,"Each PCS in the same SPI unit can be used to control one external slave. They can be required to have different value of SpiDataWidth, SpiTransferStart or SpiDefaultDta. Currently, for IP driver, these nodes are pushed into SpiPhyUnit container in IP component file. So it is not supported to change these value for each external Slave device. So, these nodes should be moved to SpiExternalDevice container for IP driver.
ARTD-4933	Bug	[GPT] The number of PIT channel deinitialized in ip layer is not exactly for PIT 1<*> I found an problem with debugging, when i call function Gpt_DeInit to reset module, then it will call the ip layer and i checked the number channel deinitialized of PIT instance. I found that the number channel deinitialized of PIT 1 excess the actual channel number is 1 channel, it might lead to some error when access this non-existed channel. I found the issue with this code section in file Pit_Ip.c: !image-2020-12-06-19-23-06-449.png! In this code, the number channel of PIT 0 and PIT 1 is equal, it should be differrent.
ARTD-4954	New	New Feature [SPI] Improve LPSPI IP driver code on S32K3 ,,"S32K3XX is using new version of LPSPI IP. This new LPSPI IP version has difference behavior with old version on S32K1XX: For S32K1XX, In the case CS continue, last frame can be only pushed into RX FIFO if another frame is initialized or CONT bit is cleared. But this behavior is not appeared on S32K3XX, It means last frames received will be pushed immediately into RX FIFO and no need to initialized another frame or CONT bit is cleared. Currently, LPSPI IP driver code on S32K3XX is implemented according to old LPSPI IP version behavior. The information of next channel in Job is always gave to IP driver when IPW initializes to transfer a channel in Job. And IP driver code is implemented complex more due to next channel must be initialized at the end of previous channel to have last received frame in RX FIFO. So, LPSPI IP driver on S32K3XX can be improved to reduce complexity."
ARTD-4958	New	New Feature [SPI][FLEXIO] Update driver according to requirements ,,Update driver according to requirements added to the ticket AAI-650
ARTD-4959	New	New Feature [SPI] Use reference node to get frequency value from MCU for CT ,,Use reference node to get frequency value from MCU for CT.
ARTD-5008	Bug	[gpt] DS Examples should use description.txt instead of readme.txt for readme details<*> Test Case : 1. Open S32DS 2. Open S32DS Project from Example wizard 3. Select example then observes description

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		FlexCAN_example_CT Crc_Example_DS Dio_example_DS Eth_Example_DS_001 FLS_IP_QSPI_Example_001 Gpt_example_DS Icu_example_DS Lpuart_Lin_example_CT Mcl_Example_CT Clock_Ip_Example_CT Power_Ip_Example_CT Port_example_DS Pwm_example_DS Ip_Lpspi_example_DS Lpuart_Uart_Ip_example_UCT Observed behavior: 3. Description is empty, could not loaded (If I rename file readme.txt to description.txt, Description can be loaded success) Expected behavior: 3. Load success
ARTD-5011	Bug	[mcu] DS Examples should use description.txt instead of readme.txt for readme details<*> Test Case : 1. Open S32DS 2. Open S32DS Project from Example wizard 3. Select example then observes description FlexCAN_example_CT Crc_Example_DS Dio_example_DS Eth_Example_DS_001 FLS_IP_QSPI_Example_001 Gpt_example_DS Icu_example_DS Lpuart_Lin_example_CT Mcl_Example_CT Clock_Ip_Example_CT Power_Ip_Example_CT Port_example_DS Pwm_example_DS Ip_Lpspi_example_DS Lpuart_Uart_Ip_example_UCT Observed behavior: 3. Description is empty, could not loaded (If I rename file readme.txt to description.txt, Description can be loaded success) Expected behavior: 3. Load success
ARTD-4997	Bug	[SPI][S32CC] Function Spi_SetupEB have an issue with length param<*> When frame size is 8 and length is 1, function Spi_SetupEB was dev error
ARTD-5024	Bug	[FLS] Slow access on nodes using // from xdm<*>

ID	Subtype	Headline and Description
		The XDM schema file (_i.e. plugins\Icu_TS_T2D35M10I0R0\config\Icu.xdm_) contains several XPath expressions for INVALID attributes which start with '//...'. This kills the performance of the model verification in bigger projects, as such expressions do a lookup in the whole model tree. For example, this expression: _<a:da name="INVALID" type="XPath"> <a:tst expr="((.='ICU_MODE_EDGE_COUNTER') and (//IcuEdgeCountApi='false'))" true="If IcuMeasurementMode = 'ICU_MODE_EDGE_COUNTER', IcuEdgeCountApi switch should be set to ON"/> will take a search for IcuEdgeCountApi in the whole project, as described in Tresos development guide. Also, there is a note to warn that using double slash can lead to performance problems: !image-2020-12-08-17-32-44-359.png|width=419,height=182! Therefore the complete system model will be verified independent of the module. Depending at the ECU project, this will lead to many minutes of additional, unnecessary verification time. Changes the pattern to absolute or relative expressions, in order to reduce the performance problem, where possible.
ARTD-5092	New	 New Feature [ICU] [S32CT] Implement EPD/EPC support for HLD and IPLD ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "
ARTD-5093	New	 New Feature [lin] [S32CT] Implement EPD/EPC support for HLD and IPLD ,,"Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation "

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ARTD-5050	New	New Feature [GPT] Add support for Predefined Timers in S32DS ,,Add support for Predef functionality in DS as it is in EBT
ARTD-5065	Bug	[Ip_Flexcan] FlexCAN_Ip_GetBitrateFD return empty value in case of enabled enhanced bit-time<*> FlexCAN_Ip_GetBitrateFD need to support when enabled enhanced bitrate Similar as FlexCAN_Ip_GetBitrate API See attached file for detail behavior TC_ID: Ip_FlexCAN_TC_*FCT_2200
ARTD-5068	Bug	[S32K3] Build fails for S32K314 and S32K324 when PIT component is used<*> # Create a new S32DS S32K314/S32K324 project. # Add PIT component, add GptPit and GptPitChannels configuration, and select Pit Channel CH_0 !image-2020-12-09-13-37-42-169.png! # Press the Update code button. # Build the project. The build will fail. I attached pit_log.txt file with the output of the build. This build fails because S32K344_PIT.h header file is not added in Pit_Ip_Cfg_Defines.h. !image-2020-12-09-13-47-40-543.png! It seems that config tool will add this include only for S32K344. This condition is used in other files too, so I expect the build to fail when those components are used: Emios_Gpt_Ip_Cfg_Defines.h Emios_Pwm_Ip_Cfg.h Rtc_Ip_Cfg_Defines.h Stm_Ip_Cfg_Defines.h
ARTD-5070	Bug	[S32K3] Build fails when PIT channel CH_RTI is used<*> # Create a new S32DS S32K314/S32K324 project. # Add PIT component, add GptPit and GptPitChannels configuration, and select Pit Channel CH_RTI. !image-2020-12-09-15-05-05-845.png! # Press the Update code button. # Build the project. The build will fail. I attached pit_rti_log.txt file with the output of the build.
ARTD-5130	New	New Feature [CAN] FlexCAN_Ip_Send should take no action/or return error when it is called while module is not in ready/normal mode ,,"Situation: From HLD, users can call Can_Write cyclically.

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		And the controller mode can be changed in the meantime. (by bus-off handling, or set_controler_to_stop, ...) => i think users would not want to check the controller_mode before they call Can_Write => Can_Write can be accidentally call in stop mode, from HLD, a Tx sw state will be changed to TX_BUSY permanently without notification (users can not see this behavior from HLD due to a HTH can includes many HW objects, if this issue happen with some of them, Can_Write can still work but with some resources was locked with TX_BUSY state) Expectation: A boolean (e.g isReady*) static variable can be created to store operation mode information then FlexCAN_StartSendData will check it "
ARTD-5137	New	 New Feature [MCL] Implement CPR_RTD_00521 support for synchronous start of Emios Counter Buses ,,"NewWorkDescription: CPR_RTD_00521*: The Mcl driver shall allow configuration of eMIOS Counter Buses that have hardware support and can be shared. The static configuration for eMIOS Counter Buses shall allow, if hardware supports, setting up a value for counter as starting point (that can be considered an offset shift between Counter Buses). Requirement source: Customer Request (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Requirement text} The Mcl driver shall allow configuration of Emios Counter Buses that have hardware support and can be shared. The static configuration shall allow, if hardware supports, setting up a value for counter as starting point (that can be considered an offset shift between Counter Buses) The Counter Buses shall be started all at once. For the motor control use case, Counter Buses with offset and PWM channels driven by Counter Buses, the following sequence may apply: Mcl_Init() Pwm_Init() / with 0% or 100% Duty Cycle / Pwm_SetDutyCycleNoUpdate() / for each channel used this will assure that on next cycle all channels will start synchronous using the CBes; / Pwm_SyncUpdate()"
ARTD-5143	Bug	 [CAN]Add Enanced FIFO generation + others for HLD CT component<*> Please add generation of Enhaced Fifo for FlexCAN Ip Pbcfg.c in the Can UCT component. this need to be synced with the component from EBT. Now is added a dummy version only for compilation. Refer to the build log files for CT to fix some warnings also.
ARTD-5145	New	 New Feature [ICU][OCU][MCL] Implement CPR_RTD_00522 restrictions and updates in CPR_RTD_00511

ID	Subtype	Headline and Description
		,,"NewWorkDescription: Updates according to the updates in the requirement: *CPR_RTD_00511 CPR_RTD_00522*: Drivers capable of using Counter Buses shall not allow selection of an Counter Bus with exclusive access granted to PWM. The check will be performed at configuration time. Applicable only for Icu, Ocu, on eMIOS Requirement source: Customer Request CPR_RTD_00511 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API that will update (buffered change expected) the match/reload value for the counter selected."
ARTD-5150	Bug	[GPT] The RTC IP Layer lacks the overflow interrupt<*> The user need to check when overflow interrupt is going to occur, but in driver has not supported this feature in RTC ip , so the user cannot check overflow interrupt. I find some issue related to this as following: RTC, in high layer, does not need callback function for overflow interrupt. In ip layer for RTC , it currently does not have some function enable interrupt overflow and in the interrupt function, it does not check overflow condition Some requirement in ip layer need to check over flow interrupt for RTC. So driver should support this feature.
ARTD-5162	Bug	[S32K3]PWM example not working, counter register is not incremented ,,"I tried to run the Pwm_example_DS project in S32DS 3.3 but was unable to get any PWM signal on output pin. Since the example configures the Emios0_Ch0 I used the PTD15 but the pin remains in low state. While investigating the issue, found following problems with example and peripheral: # [PWM] Emios_Pwm_Ip headers and sources are copied in the project under ""SDK"" folder, not ""RTD"" !1.JPG! # [PWM] The bus selector register remains on Select counter bus A, even the structure timebase in set on EMIOS_PWM_BUS_Internal. !2.JPG! # [PWM] The counter remains 0, see the register settings below. !3.JPG! # [Example] no physical pin used for the actual PWM signal output. # [Example] No clock initialization found and a typo line 88 and bad description !4.JPG! # [Example]The test passes even if the functionality is not working. Example runs until one of the count variables reaches the MAX_COUNT_PULSE. The issue is that the test is successful in both cases because the actual pin remains in low state over the entire run period. !5.JPG! # [Example]Readme has no indication on how to validate the example. The installation steps refers to some S32K2 boards.
ARTD-5163	New	New Feature [ADC] S32ConfigurationTool Multicore support for HLD ,,"Multicore support for S32CT HLD (SW triggered groups and HW Triggered groups in Trigger Mode)

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		Generation must be identical as for Tresos for TS_001"
ARTD-5165	New	New Feature [ADC] S32ConfigurationTool DMA support for HLD (Triggered and Control Mode) and IPL ,,Generation must be identical as for Tresos for TS_002
ARTD-5167	New	New Feature [PORT] Add the "Add required elements" in Tresos for UnTouchedPortPin" ,,"There should be a way to help the user add all required elements for UnTouchedPortPin container by !image-2020-12-11-09-30-44-174.png! After this improvement was implemented and user clicked on that button, does user can be add more pins into UnTouchedPortPin? If not, this improvement should not be applied.
ARTD-5169	Bug	[Platform] The functions get/clear pending interrupt do not work correctly with interrupt related to MSI<*> The purpose of the function IntCtrl_Ip_GetPending is to retrieve pending interrupt from external. It should not get status bit related to MSI. Another API should be supported to return status of interrupt of MSI. The function GetPending should return status of ISPR bit in NVIC. When there is a request interrupt from other cores, the corresponding bit in ISRPR is also raised if it has not yet served. !image-2020-12-11-09-31-51-907.png!
ARTD-5184	Bug	[ICU] Redesign IPL side for Timestamp measurement and Signal Measurement<*> Current design makes almost impossible for IPL user application to access all data provided by signal measurement and timestamp measurement. Proposal of design should be first described on: [OneNote page|https://nxp1.sharepoint.com/sites/Zebra/_layouts/OneNote.aspx?id=%2Fsites%2FZebra%2FSiteAssets%2FZebra%20Notebook&wd=target%28Group6.one%7C580E1A51-92D1-406A-ADA2-8FE4F6905B40%2FSIGNAL%20measurement%20for%20IPL%20case%7C386DB79B-D571-445D-B336-ABF25FB591A0%2F%29] Implementation should fit both eMIOS and FTM IPs as supported for actual platforms and allow extending for other new ones.
ARTD-5197	Bug	[S32K3][ICU][EMIOS] Emios specific configuration bugs<*> # If we have an instance of EMIOS on ICU which use a master bus not configured in MCL we don't receive an error(be aware of the MCL configuration). [NOT REPRODUCTIBLE] # When Signal Measurement API is checked on K3 on EMIOS IP we got an error. [NOT REPRODUCTIBLE] # If we start Timestamp Measurement without enabling the notification container we got an error when we are trying to generate. [RESOLVED]

ID	Subtype	Headline and Description
		# Master bus must be configured exclusive in MCL when is used by this driver, ICU should not modify any CHs configured by MCL as master buses.(see generation for EMIOS on ICU) [NOT REPRODUCTIBLE] # Verify this attached email thread. [THIS EMAIL IS FOR MCL, FOLLOW UP IN ANOTHER TICKET]
ARTD-5199	Bug	[ICU] Code implementation generates 'MISRA C-2012 Rule 11.5'<*> Implementation for IPW layer uses cast through void for different structure types mapping on each IP emios, ftm, wkpu, siul2 Re-factor the code for not triggering the MISRA rule violation.
ARTD-5214	Bug	[Platform][IntCtrl] Can not configure System Handler Priority Register (SHPR) with function IntCtrl_Ip_SetPriorityPrivileged<*> With the current implementation in driver for two function *IntCtrl_Ip_SetPriorityPrivileged, IntCtrl_Ip_GetPriorityPrivileged, There is no way for user can get/set System Handler Priority. As in below picture, the value of parameter eIrqNumber is always checked with value must greater than 1, so the highlight code can not be executed when DET is ON. !image-2020-12-13-17-27-26-277.png! !image-2020-12-13-17-34-22-388.png!
ARTD-5202	Bug	[Ip_Flexcan] ConfigEnhancedRxFifo and ConfigRxFifo and dev_assert<*> A>* FlexCAN_Ip_ConfigEnhancedRxFifo can work in normal mode (internally enter_freeze mode) B> FlexCAN_Ip_ConfigRxFifo (do nothing in case of normal mode), no error reporting C>* FlexCAN_Ip_ConfigEnhancedRxFifo can not work in normal mode when disableing dev_error_detect but still work when enabled dev_error_detect (because freeze mode is entered when turn of dev_detect) => enabled/disable dev_error_detect should impact to error reporting, should not change flow of code/functionality Expectation: FlexCAN_Ip_ConfigRxFifo and FlexCAN_Ip_ConfigEnhancedRxFifo should return ERROR while module is in normal mode and does not force module to freeze mode in this case => same approach as other api (e.g FlexCAN_Ip_SetRxFifoGlobalMask_Privileged)
ARTD-5211	Bug	[Ip_Flexcan] Rx FIFO Poll should have same mb_idx approach as interrupt/dma<*> Expect to move to next release, the fix can impact to HLD! Ip_FlexCAN_TC_FCT_*3055 Init flexcan with Legacy rx fifo, POLLing transfer type. FlexCAN_Ip_MainFunctionRead with mb_idx=0 will not work Expectation: same approach for poll/interrupt/dma (same hw abstraction mb_idx=0 value for legacy rxfifo), same mb_idx value when using set of APIs (FlexCAN_Ip_MainFunctionRead and FlexCAN_Ip_GetTransferStatus) Additionally: overflow/fifo_warning should be reported automatically (user should not need manually poll event with hw-dependency number as mb_idx=6 and mb_idx=7*)

ID	Subtype	Headline and Description
		=> hw abstraction need to be implemented for IP player. Documentation in this case will cause hard to use/error prone for application layer!)
ARTD-5217	Bug	[s32k3][Ip_Flexcan] Stuck in error irq loop when enabling only FLEXCAN_IP_INT_RX_WARNING<*> Init Flexcan with Installed error callback FlexCAN_Ip_SetErrorInt(u8Inst, FLEXCAN_IP_INT_RX_WARNING, TRUE); => producing Rx warning interrupt => stuck in error irq due to Rx warning is not handled by driver !image-2020-12-08-19-13-24-289.png!
ARTD-5233	Bug	[S32DS 3.4] Warning: Invalid project path: Include path not found when attach SDK RTD for S32G2xx, S32K3xx, S32R4xx ,,"STEPS: # Create project S32G2xx/S32K3xx SDK RTD # Check problem view # Create project S32R4xx S32R4xx RTD # Check problem view Observed behavior: 2. There is warning displayed: Invalid project path: Include path not found (C:\Users\loandt \workspaceS32DS.3.4\B201211_2\g234\g234_M7_0\include) Invalid project path: Include path not found (C:\Users\loandt \workspaceS32DS.3.4\B201211_2\k3\include). 4. There is warning: Invalid project path: Include path not found (C: \NXP\S32DS.3.4\B201211_RC2\S32DS\software \PlatformSDK_S32R_2020_12\SW32_RTD_4_4_1_0_0_D2012\Platform_TS_T40D11M10I0R0\startu Expected behavior: No warning
ARTD-5247	Bug	[GPT][S32DS] Build fail with ghs compiler<*> S32ct Build fail with ghs compiler: !image-2020-12-14-15-41-31-619.png!
ARTD-5318	New	New Feature [CRYPTO] Fix compiler warnings ,,Fix reported compiler warnings.
ARTD-5319	Bug	[SPI][S32CC] Change node type of SpiBaudrate in S32CT<*> Change node type of SpiBaudrate from integer to float
ARTD-5329	Bug	[S32DS 3.3 Update 1] Wrong id used in the component files for component_id attribute<*>

ID	Subtype	Headline and Description
		Also, all the used ids are case sensitive. Check the attached log file for more details. Also, a similar message is caused because the name and Csub attributes doesn't match with the .component id, in the sdk_components.xml file: !MESSAGE Could not find any matching component for type Gpt representation in the sdk_components.xml file: <sdk_component Cbundle="RTD" name="gpt" id="platform.driver.gpt" Cvendor="NXP" Cclass="Device" Cgroup="RTD Driver" Csub="gpt" version="1.0.0" prj_file="Gpt.c" version_prj_files="Gpt.h" />
ARTD-5334	New	New Feature [SPI] Support for SpiSequence with multiple jobs without CPU intervention ,,"NewWorkDescription: Customer has the following SPI use case: SPI: Assume 4 slaves, all configured with same data phase and clock polarity, say with a 4MHz clockrate, each slave with 8 channels, each slave with their own chip select. At initialization, configure high side driver (transmit 2 individual 1-byte commands, no reply expected from slave) On demand, set driver outputs (transmit a single 1-byte command, no reply expected from slave) Once initialized, poll at a fixed interval to read feedback from driver IC (transmit 2 bytes per slave, receive 2 bytes from slave). Ideally we'd be able to group these reads, issue them in a sequence and let the SPI controller do the work, dumping the received data into a per-channel fixed offset in a buffer and notifying the software when the batch read is done. As a summary customer wants to send multiple transmissions to different slaves without SW intervention and get only one interrupt at the end to notify that all slave communications are finished. Requirement source: [...] (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-5337	Bug	[Crypto][S32G-RTM] CT component cannot configuration for CryptoEcucPartitionRef node<*> 1. Create a project on S32DS.3.4. 2. Add Crypto and EcUc component config all nodes for EcUc component. 3. Configuration for Crypto component node: CryptoEcucPartitionRef => Errors will appear, detail: attach file => Crypto configuration cannot generated config code.
ARTD-5339	New	New Feature [CRYPTO] Reduce cyclomatic complexity larger than 20 for driver functions ,,The cyclomatic complexity of the Crypto_ProcessJob() is over 20.
ARTD-5356	Bug	[SPI][S32CC] Error with SpiEcucPartitionRef on S32CT<*>

ID	Subtype	Headline and Description
		If node Spi Multicore Support is TRUE, error will raise as below although it had used by SpiExternalDevice : Issue: The partition referred in SpiEcucPartitionRef is not used by any SpiExternalDevice. Level: Error Type: Tool problem Tool: Peripherals Origin: Peripherals:BOARD_InitPeripherals Resource: Spi_1 Information: The partition referred in SpiEcucPartitionRef is not used by any SpiExternalDevice.
ARTD-5359	Bug	[CAN] enhanced rx fifo dma with underflow event<*> Init can with enhanced rx fifo, enabled dma Maf send two frames Call FlexCAN_Ip_RxFifoBlocking => the second frame loss due to underflow event TC_ID: Ip_FlexCAN_TC_FCT_5202 Investigation: Run any test case (for example CAN_TS_614), i check in debug that underflow event always happen. for example you can try below sequence: Init can with enhanced rx fifo, enabled dma call rx_fifo to start dma for receiving one frame maf send only one frame, aslo => see that underflow event will always manifest expectation: we should not let underflow event happen else this will cause un-determined bahavior, very hard to investigate if users encounter this issue Note: happen on S32G, not happen on S32K ! !image-2020-12-16-11-50-28-609.png!
ARTD-5468	New	New Feature [S32K344 BETA] Update and review driver for ICU ,,"IPs list: eMIOS, SIUL2, WKPU "
ARTD-5479	New	New Feature [S32K344 BETA] Update and review driver for OCU ,,"IPs list: eMIOS "
ARTD-5490	New	New Feature [S32K344 BETA] Update and review driver for GPT ,,"IPs list: eMIOS, PIT, STM, RTC "
ARTD-5501	New	

ID	Subtype	Headline and Description
		New Feature [S32K344 BETA] Update and review driver for PWM ,,"IPs list: eMIOS, Flexio_PWM "
ARTD-5679	New	New Feature [ETH]Fix HIS violations ,,"Fix HIS violations This ticket will be resolved in the ticket ARTD-5921"
ARTD-5680	New	New Feature [S32K344] OCU: Create EBT and DS Examples ,,"IPs list: Ftm and eMIOS Create EBT abd DS examples for available EVB boards. See [here|https://confluence.sw.nxp.com/display/AUTORD/Examples] how to create an example; the second method is recommended to create the examples automatically together with the plugins"
ARTD-5683	Bug	[ADC] Adc_Sar_Ip_GetConvData always returns 0 when called from EndOfConversion notification<*> Adc_Sar_Ip_GetConvData always returns 0 when called from EndOfConversion notification Environment: Board : S32G-VNP-EVB (Rev 2) S32 Design Studio version v.3.3 S32G2_S32DS_3.3.1_D2009 SW32G2_RTD_4.4_0.9.0_D2011_updatesite Customer configured ADC using S32DS Configuration Tool. After they configured Callback_EndOfConversionNotification function for end of channel conversion notification, they tried to read AD result in the function but all they can read is 0. I also reproduced this issue in my S32DS3.3, then I found a workaround as red box below. It means not clear the ECO_CHn of CEOCFR0 before read CDATA of PCDRa. Otherwise it can not enter the first if in Adc_Sar_Ip_GetConvData function. And you can see after read CDATA of PCDRa, it will clear the ECO_CHn of CEOCFR0. Finally, attached is the sample project provided by customer.
ARTD-5689	Bug	[SPI]Old frames will be included on next synctransmit session<*> When timeout occur, old frame will include on next synctransmit
ARTD-5703	Bug	[CAN] remove multiple definition of FlexCAN_Ip_ExitFreezeMode<*> Remove double definition of the function macro FlexCAN_Ip_ExitFreezeMode from FlexCAN_Ip.h
ARTD-5721	Bug	[GPT][S32DS] Stm_Ip_u32NextTargetValue undefined when config GPT change next timeout<*>

ID	Subtype	Headline and Description
		When config GPT HLD on s32ct, enable GPT change next time out without enable ISR i got the build fail: !image-2020-12-18-15-09-38-225.png! [^Gpt.mex]
ARTD-5724	Bug	[GPT] The RTC calculates wrong number of tick per seconds<*> The number of tick in case user need to use low frequency clock is currently wrong. For instance, user config clock with frequency equal 32 Khz, clock divider factor div32 = 1 and div 512 = 1. So the number of ticks per second is calculated have to be 1.953125 ticks. But in output configuration, this value is rounded to 1 ticks. So the time application will not operate accurately. I think this value should be freeze, not rounded, to create a time per second exactly. !image-2020-12-18-15-49-51-351.png!
ARTD-5730	Bug	[S32K3][ICU] IcuDmaNotification.c file is not generated for DS<*> IcuDmaNotification.c file should be generated with respect to the existing generation from EBT.
ARTD-5731	New	New Feature [ADC] Implement Adc_Sar_Ip_DisableChannelDmaAll ,,"Implement Adc_Sar_Ip_DisableChannelDmaAll and use from HLD if required Remove from requirement and code comments Adc_Sar_Ip_DisableChannelDmaAll, ONLY if it is not required to be called from Ipw function mentioned in ADC_SAR IP ZEBRA sheet from https://teams.microsoft.com/l/file/ C97A8AE3-1D29-46CB-838A-B277B6FA1DD3?tenantId=686ea1d3- bc2b-4c6f-a92c-d99c5c301635&fileType=xlsx&objectUrl=https%3A%2F %2Fnxp1.sharepoint.com%2Fsites%2FZebra%2FShared%20Documents%2FGroup %204%2FADC_Requirements%2FADC_API_Analysis.xlsx&baseUrl=https %3A%2F%2Fnxp1.sharepoint.com%2Fsites %2FZebra&serviceName=teams&threadId=19:dea2a7f1858a42deaa0c3362b0318b93@thread.tacv2 a4d2-ad54e86f727f"
ARTD-5746	Bug	[PWM] Issue with float casting goes to Hardfault<*> Accessing float statement goes to HardFault. emiosChDuty = (uint16)(emiosChPeriod ((float)dutyCycle / 0x8000U));
ARTD-5748	Bug	[DS] There's an issue related to indexer on S32DS<*> There are some errors and warning appeared before compilation when click any file on the DS project to open on S32DS. But it will not presented at compilation.
ARTD-5749	New	New Feature [ADC] DMA without interrupts ,,"CPR_RTD_00488.adc:The adc driver shall support dma transfer for groups that have the ""Without Interrupt"" optimization enabled.

ID	Subtype	Headline and Description
		For these types of groups a dedicated DMA channel shall be used. Activities: Implement Add dev test add short description in UM remove limitation from UM that it was not supported Mark fulfilled in in Doors "
ARTD-5751	New	 New Feature [WDG] Add restriction for Dem configuration and DisableDemErrorReports ,,Add restriction for the Wdg module so that all wdg instances will need to have the same settings applied for Dem Events and WdgDisableDemErrorReport. (same as for the multicore option).
ARTD-5753	Bug	 [PORT] Incorrect placement of Port_pConfig structure pointer<*> The pointer to structure Port_pConfig in Port.c is defined in section: PORT_START_SEC_VAR_NO_INIT_UNSPECIFIED_NO_CACHEABLE I believe it should be as it was for S32K1 and S32K2 MCAL in section: PORT_START_SEC_VAR_INIT_UNSPECIFIED The placement as it is right now causes an IAR linker error for customer Magna as next: Error[Lp005]: placement includes a mix of sections with content (example "rw data section .mcal_bss_no_cacheable in Port.o") [suitable for placement in ROM] and sections without content (example "zi section .mcal_bss_no_cacheable C:\Projects\SAM_K3_Test\linker_flash.icf 153 Please confirm and fix in next release.
ARTD-5771	New	 New Feature [ICU] integrate cmp IPL files into ICU driver ,,"Integrate ICU IPL driver into ICU driver. include in xdm for EB Tresos; include in .component for S32DS; generate ipl code for both worlds; map functionality ASR-IPL; review IPL DOORs requirements; Last known state of IPL is found on : feature/ARTD-419-icu-cmp commit id: d0a64491d4a2723fef92d4aa009ba2184c44e7bf"
ARTD-5779	New	 New Feature [CRYPTO] Multiple definition of a macro ,,"CRYPTO_JOB_QUEUE_NONE_U32 is defined in Crypto_Util.h and Crypto_Hse.c. The define from Crypto_Hse.c. should be remved."
ARTD-5825	Bug	 [RTD][MCL]De-init function shall clear logic channel status<*> Detailed description (how to reproduce it): Init Mcl module(with no IRQ error) Set a error to dma channel Call De-init function

ID	Subtype	Headline and Description
		Check value of CH error register > CH error register is not be clear Try to set again the transfer list with some commands All commands return DMA_IP_STATUS_ERROR > De-init function should support to clear HW error of channel Observed behavior: All HW error status of channel is not be cleared after de-init called Expected behavior: De-init function should support to clear all error status of channel
ARTD-5839	New	 New Feature [SPI] Dem error can be reported in AsyncTransmit when HW errors occur ,,"Dem error can be reported in AsyncTransmit when HW errors occur. This can be implemented in Ipw_Callback function. And some requirements below can be also applied for AsyncTransmit, not only SyncTransmit as current implementation. SWS_Spi_00267 SWS_Spi_00383 SWS_Spi_00385 SWS_Spi_00386 SWS_Spi_00293"
ARTD-5853	Bug	 [GPT] Rtc_Ip_IsCounterSync API can not be used because Rtc_Ip_ModeType is not defined<*> Rtc_Ip_IsCounterSync API can not be used by the user because the Rtc_Ip_ModeType is not defined in Rtc_Ip_Types.h proposal: Rtc_Ip_ModeType should be added in driver
ARTD-5879	New	 New Feature [SAI] DMA support ,,"DMA support in tresos and s32ct. Add dev test"
ARTD-5911	Bug	 [platform] Checking the number of configured interrupt is not correct for the function Platform_Ipw_InitIntCtrl<*> 1. I'm trying to improve code coverage for the function Platform_Ipw_InitIntCtrl. I see that the pointer *pIntCtrlCtrlConfig which is a parameter of the function is passed from HDL, that was generate by configuration tool. So there is no way to create invalid configuration by configuration then check in this function. However, in the case there is error in generation configuration, the checking in this function maybe reasonable. But the checking seem to be incorrect. !image-2020-12-24-16-00-48-354.png! Suppose that there are 183 interrupt vector but the maximum interrupt number is 225. So if the value *pIntCtrlCtrlConfig->u32ConfigIrqCount (line 62) is 184, its is still valid. But indexing to the array aIrqConfig[irqIdx] at the line 71 is out of boundary, then probably cause hardfault.* 2. With assumption about there probably error in generating configuration causes incorrect generated code. There is a lack of checking for the function Platform_Ipw_InitNonCore !image-2020-12-24-16-18-06-869.png!

ID	Subtype	Headline and Description
		Please check this issue.
ARTD-5904	Bug	[S32K3 BETA][SENT] Undefine value in Sent_VS_0_PBcfg.c and Flexio_Ip_VS_0_PBcfg.c<*> Issue When SentControllerActivation = false, Controller HW offset is (uint8)SENT_NULL_OFFSET_U8 in Sent_VS_0_PBcfg.c and Flexio_Ip_VS_0_PBcfg.c. [!IF "SentControllerActivation = 'true'"!] (uint8)[!"num:i(text:split(SentHwController,'_')[2])"!]U, [!ELSE!] (uint8)SENT_NULL_OFFSET_U8, [!ENDIF!] But this value has not been defined: STDERR:"e:/gitwork/Zerba/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344/sent/Sent_TS_COT_007_cfg1/generate_tresos/src/Flexio_Ip_VS_0_PBcfg.c", line 216: error #20: STDERR: identifier "SENT_NULL_OFFSET_U8" is undefined STDERR: (uint8)SENT_NULL_OFFSET_U8,
ARTD-5917	New	New Feature [SPI] Add a note in UM about limitation in Slave mode ,,"There is an note in RM sub-chapter "" 49.5.4.5 Continuous selection format "": !image-2020-12-24-17-13-27-965.png! In Slave mode and continuous CS, TFUF bit will be set when previous frame sent out but TX FIFO empty and CS signal was not de-asserted. In this situation, if external master still send next frame then previous frame was still sent out 1 time regardless of new frames filled into TX FIFO after that immediately. And TFUF bit is still set for each frame initialized by external master from that time until CS de-asserted. So the note should be added in UM sub-chapter ""Driver Limitations"" like: # In Slave mode and continuous CS, to avoid underflow error, the maximum number of byte to be sent is 32767 if DMA used and SpiDataWidth <= 8. Rationale: the maximum of BITER(Major Iteration Count) is 32767 and DMA major interrupt is processing when last entry in the TX FIFO is completely transmitted. # In Slave mode and use interrupt mode without DMA, the application needs to make sure Slave's interrupt service is not delayed to avoid errors underflow and overflow occur. Note (2) can be applied for platforms use LPSPI."
ARTD-5921	Bug	[S32R45-ETH] Generate failed when configure two controllers<*> Can not configure two controllers for S32R45 as the image attached
ARTD-5922	New	New Feature [SPI][FLEXIO] Support slave mode ,,Support slave mode
ARTD-5925	Bug	[ADC] There is a typo for Adc_sar component<*>

ID	Subtype	Headline and Description
		Test Case ID (internal TC that caught the defect) optional: 1. Create project enable RTD for S32G274_Rev2 2. Open Peripherals tool-> Add Adc_Sar_Ip component 3. Open Adc_Sar component in Editor view > Channel configurations array > Enable "Threshold Enable" > Error shows in "Watchdog Threshold Register Index" (see pic 1) 4. In Watchdog threshold configurations array-> add one Register Observed behavior: The error in "Watchdog Threshold Register Index" is not resolved because there is a typo of default name missing "h": *AdcTresholdControl_0 It should be "**AdcThresholdControl_0**"
ARTD-5926	Bug	[SPI][FLEXIO] Add FLEXIO support macro to reduce code expose when FLEXIO is not selected<*> Add FLEXIO support macro to reduce code expose when FLEXIO is not selected
ARTD-5930	Bug	[S32K3 BETA][SENT] Wrong type and description with SentTimeout in Flexio.component<*> Issue 1. In Flexio.component, id SentTimeout has wrong type and information <integer id="SentTimeout" label="Sent Timeout (0->65535)" type="uint8_t"> <description>Defines the depth of the DMA buffer</description> </integer> 2. In CDD_Sent.component, it has no SentTimeout node.
ARTD-5933	Bug	[S32K3 BETA][SENT] Duplicate and wrong some definitions in Sent_BOARD_INITPERIPHERALS_PBcfg.h<*> Issue 1 build fail as below: C:/Users/trungdm1/workspaceS32DS.3.4/test_sent_01/generate/include/Sent_BOARD_INITPERIPHERALS_PBcfg.h:26: error: unterminated #ifndef 26 #ifndef SENT_BOARD_INITPERIPHERALS_PBCFG_H > Issue comes from duplicating: #ifdef cplusplus extern "C"{ #endif and in Sent_PBcfg.h on S32DS #ifndef SENT_[!<code>$variantName$</code>!]_PBCFG_H #define SENT_[!<code>$variantName$</code>!]_PBCFG_H Issue 2 In Sent_Cfg.h has wrong definition: / On/Off PreCompile switches / #define SENT_CONFIG_EXT SENT_CONFIG_BOARD_INITPERIPHERALS_PB > Sent_Cfg.h should update: <code> / On/Off PreCompile switches / </code> <code>#define SENT_CONFIG_EXT \\\n</code>

ID	Subtype	Headline and Description

		if(variantName)
		{
		<code>
		SENT_CONFIG_$variantName$_PB \\\n
		</code>
		}
		else
		{
		<code>
		SENT_CONFIG_PB \\\n
		</code>
		}

ARTD-5947	Bug	[ADC] Missing constraints for S32CT component<*> Add constraints for found issues on ADC CT all constraints <constraint cond_expr="(($this.getValue() == ``) isCIdentifier($this.getValue()))" must remove ($this.getValue() == ``) condition adcGroupdefineitionArray must raise error if no channel is configured for that group Hw trigger source should not be available when ADC_HW_TRIGGER_API = OFF
ARTD-5995	Bug	[CRYPTO] Crypto_Hse.c: u32StreamId should be converted from uint32 to uint8<*> Crypto_Hse.c: u32StreamId should be converted from uint32 to uint8
ARTD-6018	Bug	[S32K3 BETA][SENT] Redefine Channel Id macros on Sent_Cfg.h<*> Issue Sent_Cfg.h and Flexio_Ip_Cfg.h define Channel ID macros, this one causes redefine error. Solution Remove channel ID macros in Sent_Cfg.h
ARTD-6019	Bug	[S32K3 BETA][SENT] Wrong Fast notification declaration in Flexio_Ip_PBCfg. c and Sent_PBcfg.c<*> Issue: STDERR:"e:/gitwork/Zebra/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344/sent/Ip_Sent_TS_COT_001_cfgs32k314_mqfp100/generate_s32ct/generate/src/Flexio_Ip_BOARD_InitPeripherals_PBcfg.c", line 162: error #144:STDERR:"e:/gitwork/Zebra/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344/sent/Ip_Sent_TS_COT_001_cfgs32k314_mqfp100/generate_s32ct/generate/src/Flexio_Ip_BOARD_InitPeripherals_PBcfg.c", line 162: error #144:STDERR: a value of typeSTDERR: "void (Flexio_Sent_Ip_StatusType, Flexio_Sent_SerialMsgType)"STDERR: cannot be used to initialize an entity of typeSTDERR: "const Sent_pFastNotificationType"STDERR: &FlexSent_FastNotif, Solution: Update in Sent_PBcfg.c and Flexio_Ip_PBCfg.c <code> extern void $sent_chConfigChildren[idx2].getChildById("SentFastNotification").getValue()$ (Flexio_Sent_Ip_StatusType status, Flexio_Sent_FastMsgType pSent_FastMsg); </code>
ARTD-6026	New	

ID	Subtype	Headline and Description
		New Feature [SPI][FLEXIO] CS continuous mode only support with CPHA=1 with SLAVE mode ,,"RM said that: For CPHA=1, the select can remain asserted for multiple transfers and the timer status flag can be used to indicate the end of the transfer. So, Driver will not allow user configure CS continuous mode with CPHA is 1 with SLAVE mode "
ARTD-6029	New	New Feature [SPI][FLEXIO] CS non-continuous mode only is supported when TIMCFG[TIMDIS] is 0 ,,"Currently, FLEXIO driver Master mode is supporting to configure SPI baudrate by 3 mode in TIMCFG[TIMDIS] field bits but only TIMCFG[TIMDIS] is 0 then CS non-continuous can be supported. So, The configuration file should be updated like: Add the condition expression like ""SpiCsContinous is FALSE only SpiBaudrateFlexio1 is selected"" a ticket to add the limitation of FLEXIO SPI in UM document will be created."
ARTD-6030	New	New Feature [SPI][FLEXIO] The delay value which will be configured by EB/CT tools is not used by FLEXIO ,,"FLEXIO don't have any registers to configure the delay timing. So the delay field configuration (SpiTimeClk2Cs, SpiTimeCs2Clk, SpiTimeCs2Cs) in Externaldevice should be disabled when FLEXIO is selected. That will not make user feel confuse when they setup their config"
ARTD-6049	Bug	[Ip_Flexcan] Timestamp for K3 build fail<*> A> build fail at IPL when enabling timestamp !image-2021-01-06-14-44-35-185.png! B>* timestamp is not available on EB / HLD => *CPR_RTD_00529.can, CPR_RTD_00528.can can not be tested now S1 (priority) because this need to be fixed and to be tested soon TC_ID: in-process
ARTD-6050	Bug	[BASE] The inter-module disable version check in "Devassert.h" is missed ,,"Devassert.h includes ""PlatformTypes.h"", however the DISABLE_MCAL_INTERMODULE_ASR_CHECK guard defined encapsulation is missed, leads to the compile error in VECTOR integrator.
ARTD-6052	Bug	[S32K3 BETA][SENT] SentDmaChannelReference and SentCpuClockRef need to refer to MCL and MCU in HL<*> Issue*: In CDD_Sent.component, SentCpuClockRef and SentDmaChannelReference are not refering to MCL and MCU. Solution*:

ID	Subtype	Headline and Description
		Update 2 node SentCpuClockRef and SentDmaChannelReference. Update code generation. Add new node SentControllerActivation to synchronize with EBtresos.
ARTD-6056	New	 New Feature [SPI][FLEXIO] Add the limitation of SPI FLEXIO to UM document ,,"FLEXIO Limitation CS continous mode only supports with CPHA=1 CS non-continous mode of master mode only support with TIMCFG[TIMDEC] = 000 (SpiBaudrateFlexio1 is selected) FLEXIO don't support to configure the timing delay on master mode. "
ARTD-6059	Bug	 [MCl][Emios] Build fail because the EMIOS_MCL_IP_DEV_ERROR_DETECT variable is undefined<*> Initializes the MCL module with configurations on EB tresos The bug: Build fail because the error appeared: Please, see the attached Bug_emios.PNG file for more detail. The root cause: The EMIOS_MCL_IP_DEV_ERROR_DETECT variable is defined in Emios_Mcl_Ip_CfgDefines.h file, but this file is not called anywhere in drive. I tried to include "Emios_Mcl_Ip_CfgDefines.h" in Emios_Mcl_Ip_Types.h file, the test build passed. Also, EMIOS_MCL_IP_DEV_ERROR_DETECT variable in Emios_Mcl_Ip_CfgDefines.h file is missing a space !MicrosoftTeams-image.png|thumbnail! Test Case ID (internal TC that caught the defect) optional: Test case: Mcl_TC_FCT_0201 Test suite: Mcl_TS_CC01 Observed behavior:*_ N/A Expected behavior:*_ N/A Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-6060	Bug	 [S32K3][MCU]Mcu_ResetType did not folow req SWS_Mcu_00252<*> According requirement SWS_Mcu_00252: !image-2021-01-06-17-04-40-018.png|width=793,height=269! But in driver code declared: typedef Power_Ip_ResetType Mcu_ResetType; so we must update Mcu_ResetType follow req
ARTD-6062	Bug	 [ICU][S32K3XX] The ICU_START_SEC_CODE and ICU_STOP_SEC_CODE macros are defined in wrong file.<*> The ICU_START_SEC_CODE and ICU_STOP_SEC_CODE macros are defined in src file. They should be defined in header file. pls see attach file.
ARTD-6072	Bug	 [S32K3]IAR linking issues<*> There has been linker errors with having the placement of sections with mixed content errors, I have the two that I am aware of below. The solution has been to change the section names in the cfg C files to correct the linker error:

ID	Subtype	Headline and Description
		a. Error[Lp005]: placement includes a mix of sections with content (example "rw data section .mcal_bss in Adc_PBcfg.o") [suitable for placement in ROM] and sections without content (example "rw code section .ramcode in C:\Projects\SAM_K3_Test \linker_flash.icf 150 b. Error[Lp005]: placement includes a mix of sections with content (example "rw data section .mcal_bss_no_cacheable in Port.o") [suitable for placement in ROM] and sections without content (example "zi section .mcal_bss_no_cacheable C:\Projects \SAM_K3_Test\linker_flash.icf 153
ARTD-6077	Bug	[GPT][S32DS] Gpt got undefined error<*> Gpt got undefined error in PBcfg.c file for Pit, Stm and Emios, file generate is empty: See more detail in log file as in attachment !image-2021-01-07-13-33-18-812.png!
ARTD-6080	Bug	[S32K3xx_Beta][Port] EB tresos still config PortPin Slew Rate bit when driver not support by hardware<*> Detailed description (how to reproduce it): Configuration some pins by pins tool in S32DS. Slew Rate is Slowest setting. Some pins with config PortPin Slew Rate is Slowest setting, bit MSCR[SRC] not set to 1 (Slowest setting). Test Case ID (internal TC that caught the defect) optional: N/A Observed behavior: Some pins has bit MSCR[SRC] default is not available by hardware.
ARTD-6082	Bug	[ICU] IcuDMAChannelRef has to be configured even if DMA is not used<*> In ICU driver, the parameter IcuDMAChannelRef has a multiplicity of 1:1 in the epd file. Thus, it has to be configured even if DMA is not used. The issue can be resolved, by adding OPTIONAL attribute for these parameters (refer to the attachment)
ARTD-6089	Bug	[S32K344 BETA][SENT] Some nodes need to refer from resource table in CDD_Sent/ Flexio.component<*> Issue*: 1. There are some node are hard code in CDD_Sent/Flexio.component files. flexio_sent_cfg_channelHwOffset items="toArray(`CHANNEL_0`,`CHANNEL_1`,`CHANNEL_2`,`CHANNEL_3`,`CHANNEL_4`,`CHANN flexio_sent_cfg_sentPinSelection items="toArray(`PIN_0`,`PIN_1`,`PIN_2`,`PIN_3`,`PIN_4`,`PIN_5`,`PIN_6`,`PIN_7`,`PIN_8`,`PIN_9`,`P flexio_sent_cfg_ControllerHwOffset items="toArray(`FLEXIO_0`,`FLEXIO_1`) 2. Disable node which does not support in K3: SentDmaBufferDepth 3. SentDmaChannelReference need to be enabled when SentDmaActivation=true.
ARTD-6092	Bug	[MCL][CACHE] Cache_Ip_InvalidateByAddr(CACHE_IP_INSTRUCTION) doesn't invalidate entire length<*> Detailed description (how to reproduce it): Configure for Mcl drive with EB tool:

ID	Subtype	Headline and Description
		The bug : The funtion Mcl_CacheCleanByAddr and Mcl_CacheInvalidateByAddr function can not invalidate or clean correct when the buffer is unalign with 32 byte. Please, see the attached Bug_cache1.PNG and Bug_cache file for more detail. Preconditions: N/A Test Case ID (internal TC that caught the defect) optional: Mcl_TC_FCT_0802.c Mcl_TC_FCT_0804.c Observed behavior: N/A Expected behavior: N/A Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-6098	Bug	[S32K3XX] [PORT] Issue about IBE register value of Port_Init with Analog mode<*> Detailed description (how to reproduce it): When Port_Init pin analog mode, value IBE=1, but after that, declare function Port_ResetPinMode, ==>value IBE=0 Test Case ID (internal TC that caught the defect) optional: Port_TC_FCT_0033 Observed behavior: Call Port_Init: !image-2021-01-08-14-13-48-554.png! After Port_ResetPinMode: !image-2021-01-08-14-15-09-961.png! Expected behavior: Port_Init pins need to fix value IBE = 0, we declare function Port_ResetPinMode, register IBE need to be keep same value with init
ARTD-6100	Bug	Pins not configurable as Input/Output<*> When setting the direction of a pin as Input, in the Routed Pins table, included in the Pins Tool (S32 Configuration Tools), the following input options are set in the configuration structure (input.png). When changing the direction of the pin as Output, the .mux field changes, but the previously shown input settings are not kept (output.png). The Siul2 component should offer the functionality of keeping both Input and Output settings when configuring a pin (e.g: inputMux[0] = PORT_INPUT_MUX_ALT1, inputMuxReg[0] = 217u and also .mux = PORT_MUX_ALT4). Currently, one selection cancels the settings made for the other. This functionality has an application inside the LPI2C example. There, the LPI2C pins must have both Input and Output settings. Currently, to ensure the example functionality, these settings are made by using an additional function Init_Pins, where the corresponding values are written inside MSCR and IMCR registers. (lpi2c_example.png) However, this approach does not use the Siul2_Port_Ip_Init function, since the pins configurations are not available from the Pins tool in Configuration Tools, as previously shown. To avoid writing values into specific registers, the workaround for the encountered issue is to configure the pins as an Input using the Pins Tool from CT (configuration.png), and then to add the output settings using the SetOutputBuffer API (code.png).

ID	Subtype	Headline and Description
		However, we would like to be able to use the API functions for Pins initialization since this workaround assumes that the Pins initialization must be done every time the user wants to modify a pin of a specific functionality. Moreover, the IO Signal Table must be opened to find the appropriate MUX_ALT option, instead of just simply calling the Siul2_Port_Ip_Init function.
ARTD-6101	Bug	Siul2 PORT defines<*> The PORT[A-G] defines, in Siul2_Port_Ip_Defines.h (siul2_defines.png) assume that each PORT has 16 pins, instead of 32, as specified in the Reference Manual of S32K3 (ports_definition.png). Thus, for configuring for example the pin PTC6, the specified port must be PORTE (since PORTA covers the first 16 pins of the first port, PORTB the next 16 bits of the first port, PORTC the first 16 bits of the second port and so on). Moreover, for configuring for example PTF20, no define comes in hand (considering the same logic as previously described), and the address of the port needs to be computed as (PORT_Type)(SIUL2_MSCR_BASE 0xB0). Attached is an example (example.png) of using the Siul2_Port_Ip_SetOutputBuffer function for configuring output settings for the PTF20, PTF21, PTC6 and PTC7 pins. If the first argument is replaced to the appropriate defines (PORTF for the first 2 functions and PORTC for the next ones), hard faults will occur when these functions are executed.
ARTD-6102	Bug	[ADC] Naming convention: generated files <MSN>_PBCfg.h/c must change to <MSN>_PBcfg.h/c<*> Naming of generated files <MSN>_PBCfg.h/c should change to <MSN>_PBcfg.h/c in order to correctly generate the files for each variant within the list of functional groups.
ARTD-6112	Bug	[GPT][S32CT] Cannot refer to the GptModuleRef node, and after workaround the project, the build code fails in GHS and IAR compiler ,,"Detailed description (how to reproduce it): Step 1: Pull code from tag PVT_GPT_ARTD_5492_V04, compile plugin and generate layout Step 2: Config for GPT and dependent module Step 3: Run command: make clean generate and make build Preconditions: [...] Observed behavior: Cannot refer to the GptModuleRef node, and after workaround the project, the build code fails in GHS and IAR compiler. Detail was attached. Expected behavior: The project no warnings, errors after generate and build code
ARTD-6116	Bug	[ICU][S32K3XX] Some macros are not generated at the IPL in eMios module<*> The EMIOS_ICU_DEINIT_API macro and some macros about feature are generated at the IPL in eMios module (eg: EMIOS_ICU_EDGE_COUNT_API). And in the DS interface there is no nodes to select these features. pls see attach file.
ARTD-6109	Bug	[S32K3XX][PWM] Emios_Pwm_Ip_ChannelConfigType type is undefined in Emios_Pwm_Ip_VS_0_PBcfg.h file<*>

ID	Subtype	Headline and Description
		Build error: Emios_Pwm_Ip_ChannelConfigType type is undefined in Emios_Pwm_Ip_VS_0_PBcfg.h file. Emios_Pwm_Ip_ChannelConfigType type is defined in Emios_Pwm_Ip_Types file. But if you include Emios_Pwm_Ip_Types.h in this file, it will be included repeatedly (Emios_Pwm_Ip_Cfg.h > Emios_Pwm_Ip_VS_0_PBcfg.h > Emios_Pwm_Ip_Types.h-> Emios_Pwm_Ip_Cfg.h). I think you should create a new file to define this structure and include this file.
ARTD-6110	Bug	[S32K3XX][PWM] Define Emios_Pwm_Ip_DeInitChannel function do not match the requirement<*> Define function in driver code: void Emios_Pwm_Ip_DeInitChannel(uint8 instance, uint8 channel, Emios_Pwm_Ip_OutputStateType safeState) And in the requirement: void Emios_Pwm_Ip_DeInitChannel(uint8 instance, uint8 channel) Please update one of the 2 so they are in sync.
ARTD-6115	Bug	[S32K3XX][MCL] Missing line break when config Emios_Mcl_Ip with S32CT<*> When config Emios_Mcl_Ip and enable interrupt in S32CT, 3 define ISR_USED in Emios_Mcl_Ip_CfgDefines.h file do not have line break. It cause fail at build. Please see in attach file.
ARTD-6123	Bug	[S32K3XX BETA] DMA Transfer using Channel Link doesn't work for the second transfer<*> Behavior: there are some bit fields are depended on DONE flag (MAJORELINK, ESG in TCDn_CSR). So for the next transfer if this register is updated while DONE=1; MAJORELINK and ESG will be forced to 0. !image-2021-01-08-18-31-42-227.png|thumbnail! Solution: DMA DONE flag should be cleared each time transfer complete in IRQHandler to avoid unexpected behavior
ARTD-6125	New	New Feature [CRYPTO]AES key generation improvement ,,"The AES key length can be taken from CryptoKeyElementSize(xdm configuration) filled in Tresos configurator, which translates to u32CryptoKeyElementMaxSize(Crypto_Cfg.c) instead of pu32CryptoElementActualSize(Crypto_Cfg.c) which must be set by calling Crypto_KeyElementSet(). The change in code: u32KeyLength = Crypto_aKeyElementList[u32KeyMaterialKeyElemIdx].pu32CryptoElementActualSize; to u32KeyLength = Crypto_aKeyElementList[u32KeyMaterialKeyElemIdx].u32CryptoKeyElementMaxSize;"
ARTD-6126	Bug	[GPT] Code generation error "config class PostBuild which is not allowed in this context"

ID	Subtype	Headline and Description
		,,"Detailed description (how to reproduce it): GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.
ARTD-6127	Bug	[SPI] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): SPI has consistent errors when using Post Build Variants (even with generic XDM). SPI module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the SPI.xdm file. Error messages: Invalid XPath-expression for Attribute ""RANGE"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiExternalDevice/MMIC_1_SPI_40_MHz_Device/SpiCsIdentifier"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiExternalDevice/MMIC_1_SPI_40_MHz_Device/SpiHwUnit with config class PostBuild which is not allowed in this context Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiJob/MMIC_1_40MHz_Job/SpiChannelList"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Spi/ELEMENTS/Spi/SpiDriver/SpiExternalDevice/MMIC_1_SPI_40_MHz_Device/SpiHwUnit with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing (in INVALID, or in RANGE tag) a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project.

ID	Subtype	Headline and Description
		Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.
ARTD-6155	Bug	[gpt] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. Summary: Plugin*|*No. of duplicated UUIDs Eth.xdm | 1 Gpt.xdm | 2 Lin.xdm | 2 Platform.xdm | 17 Port.xdm | 1 Rm.xdm | 158 Rm_s32k314_mapbga257.xdm | 23 Rm_s32k314_mqfp100.xdm | 79 Rm_s32k314_mqfp172.xdm | 79 Rm_s32k324_mapbga257.xdm | 79 Rm_s32k324_mqfp172.xdm | 79 Rm_s32k344_mapbga257.xdm | 79 Rm_s32k344_mqfp172.xdm | 79 Sai.xdm | 22 Uart.xdm | 8 Wdg.xdm | 197 *Keyword* | *Hits* \t | 2330 M4_ | 54 *File* | *Hits* Dma_Ip_Hw_Access.c | 293 main.c | 192 Lpi2c_Ip.c | 176 Dma_Ip_Hw_AccessInline.h | 175 Uart_Ipw.c | 130 FlexCAN_Ip.c | 126 Dma_Ip.h | 112 Cache_Ip_HwAcc_ArmCoreMx.h | 97 Cache_Ip.c | 78 Dem_stub.c | 71 I2c_Ipw.c | 57

ID	Subtype	Headline and Description
		Dma_Ip_Irq.c | 53 FlexCAN_Ip_HwAccess.h | 49 Clock_Ip_Private.h | 48 Dma_Ip_Cfg_Defines.h | 40 FlexCAN_Ip_Types.h | 40 Det_stub.c | 39 Uart_Ipw.h | 38 FlexCAN_Ip_HwAccess.c | 35 Lpuart_Lin_Ip_Irq.c | 32 sys_init.c | 29 S32K344_AXBS_LITE.h | 28 Dma_Ip_Driver_State.c | 28 Clock_Ip_Monitor.c | 27 FlexCAN_Ip.h | 27 Mpu_M7_Ip.c | 23 Lpi2c_Ip_Types.h | 21 system.c | 19 IntCtrl_Ip_TypesDef.h | 17 Lpuart_Uart_Ip_Irq.c | 16 Trgmux_Ip_HwAcc.h | 16 Clock_Ip_IntOsc.c | 15 Eth_PBcfg.h | 13 FlexCAN_Ip_DeviceReg.h | 12 Clock_Ip_ProgFreqSwitch.c | 12 Clock_Ip_Types.h | 11 Gmac_Ip_PBcfg.h | 9 Dma_Ip_RegOperations.m | 8 Trgmux_Ip_Types.h | 8 Gmac_Ip_PBcfg.c | 8 Power_Ip_RegOperations.m | 8 I2c_Ip_Callbacks.h | 7 Dma_Ip_Multicore.c | 7 Dma_Ip_Driver_State.h | 6 Lpi2c_Ip_Irq.c | 6 FlexCAN_Ip_Wrapper.h | 5 Flexio_Ip_Types.h | 5 Power_Ip.c | 5 Clock_Ip_Pll.c | 5 Flexio_I2c_Ip_Types.h | 5 Dma_Ip_Hw_Access.h | 5 Dma_Ip_Hwv3_Regs.h | 5 Clock_Ip_S32K3XX.h | 5 S32K344_STCU.h | 4 Lpi2c_Ip_Cfg.h | 4 Trgmux_Ip_Devassert.h | 4 Trgmux_Ip_RegOperations.m | 4 Trgmux_Ip_Cfg_Defines.h | 4 Cache_Ip_Devassert.h | 4 Can_Irq.c | 4 Dma_Ip_Devassert.h | 4 Cache_Ip.h | 3 Lpuart_Uart_Ip_Defines.h | 3 Uart_Defines.h | 3 Lpi2c_Ip_PBcfg.c | 3 Mcu_IPW.c | 2 Gmac_Ip.c | 2 FlexCAN_Ip_Irq.h | 2 Lpuart_Uart_Ip.c | 2

ID	Subtype	Headline and Description
		Can.c | 2 Xrdc_Ip.c | 2 CDD_Mcl.h | 2 Flexio_I2c_Ip_Cfg.h | 2 Flexio_I2c_Ip.c | 2 Gmac_Ip_Types.h | 1 Clock_Ip_S32K3XX.c | 1 Gpt_Ipw.c | 1 Dma_Ip_Types.h | 1 CDD_Mcl_PBcfg.h | 1 Flexio_Ip_Common.c | 1 Mcl_Example_EBT_OVER_LCU.h | 1 Mcl_Example_EBT.h | 1 Dma_Ip_Devices.h | 1 Dma_Ip_Irq.h | 1 Emios_Mcl_Ip.c | 1 Trgmux_Ip_Devices.h | 1 S32K344.h | 1 Lin.h | 1 CDD_I2c_Cfg.h | 1 Emios_Mcl_Ip_Types.h | 1 Lpuart_Uart_Ip_Types.h | 1 Dem_stub.h | 1 Lin_PBcfg.c | 1 Lin_Types.h | 1
ARTD-6157	Bug	[sai] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. Summary: Plugin*|*No. of duplicated UUIDs Eth.xdm | 1 Gpt.xdm | 2 Lin.xdm | 2 Platform.xdm | 17 Port.xdm | 1 Rm.xdm | 158 Rm_s32k314_mapbga257.xdm | 23 Rm_s32k314_mqfp100.xdm | 79 Rm_s32k314_mqfp172.xdm | 79 Rm_s32k324_mapbga257.xdm | 79 Rm_s32k324_mqfp172.xdm | 79 Rm_s32k344_mapbga257.xdm | 79 Rm_s32k344_mqfp172.xdm | 79 Sai.xdm | 22 Uart.xdm | 8 Wdg.xdm | 197

ID	Subtype	Headline and Description
		Keyword | *Hits* \t | 2330 M4_ | 54 *File* | *Hits* Dma_Ip_Hw_Access.c | 293 main.c | 192 Lpi2c_Ip.c | 176 Dma_Ip_Hw_AccessInline.h | 175 Uart_Ipw.c | 130 FlexCAN_Ip.c | 126 Dma_Ip.h | 112 Cache_Ip_HwAcc_ArmCoreMx.h | 97 Cache_Ip.c | 78 Dem_stub.c | 71 I2c_Ipw.c | 57 Dma_Ip_Irq.c | 53 FlexCAN_Ip_HwAccess.h | 49 Clock_Ip_Private.h | 48 Dma_Ip_Cfg_Defines.h | 40 FlexCAN_Ip_Types.h | 40 Det_stub.c | 39 Uart_Ipw.h | 38 FlexCAN_Ip_HwAccess.c | 35 Lpuart_Lin_Ip_Irq.c | 32 sys_init.c | 29 S32K344_AXBS_LITE.h | 28 Dma_Ip_Driver_State.c | 28 Clock_Ip_Monitor.c | 27 FlexCAN_Ip.h | 27 Mpu_M7_Ip.c | 23 Lpi2c_Ip_Types.h | 21 system.c | 19 IntCtrl_Ip_TypesDef.h | 17 Lpuart_Uart_Ip_Irq.c | 16 Trgmux_Ip_HwAcc.h | 16 Clock_Ip_IntOsc.c | 15 Eth_PBcfg.h | 13 FlexCAN_Ip_DeviceReg.h | 12 Clock_Ip_ProgFreqSwitch.c | 12 Clock_Ip_Types.h | 11 Gmac_Ip_PBcfg.h | 9 Dma_Ip_RegOperations.m | 8 Trgmux_Ip_Types.h | 8 Gmac_Ip_PBcfg.c | 8 Power_Ip_RegOperations.m | 8 I2c_Ip_Callbacks.h | 7 Dma_Ip_Multicore.c | 7 Dma_Ip_Driver_State.h | 6 Lpi2c_Ip_Irq.c | 6 FlexCAN_Ip_Wrapper.h | 5 Flexio_Ip_Types.h | 5 Power_Ip.c | 5 Clock_Ip_Pll.c | 5 Flexio_I2c_Ip_Types.h | 5 Dma_Ip_Hw_Access.h | 5 Dma_Ip_Hwv3_Regs.h | 5

ID	Subtype	Headline and Description
		Clock_Ip_S32K3XX.h | 5 S32K344_STCU.h | 4 Lpi2c_Ip_Cfg.h | 4 Trgmux_Ip_Devassert.h | 4 Trgmux_Ip_RegOperations.m | 4 Trgmux_Ip_Cfg_Defines.h | 4 Cache_Ip_Devassert.h | 4 Can_Irq.c | 4 Dma_Ip_Devassert.h | 4 Cache_Ip.h | 3 Lpuart_Uart_Ip_Defines.h | 3 Uart_Defines.h | 3 Lpi2c_Ip_PBcfg.c | 3 Mcu_IPW.c | 2 Gmac_Ip.c | 2 FlexCAN_Ip_Irq.h | 2 Lpuart_Uart_Ip.c | 2 Can.c | 2 Xrdc_Ip.c | 2 CDD_Mcl.h | 2 Flexio_I2c_Ip_Cfg.h | 2 Flexio_I2c_Ip.c | 2 Gmac_Ip_Types.h | 1 Clock_Ip_S32K3XX.c | 1 Gpt_Ipw.c | 1 Dma_Ip_Types.h | 1 CDD_Mcl_PBcfg.h | 1 Flexio_Ip_Common.c | 1 Mcl_Example_EBT_OVER_LCU.h | 1 Mcl_Example_EBT.h | 1 Dma_Ip_Devices.h | 1 Dma_Ip_Irq.h | 1 Emios_Mcl_Ip.c | 1 Trgmux_Ip_Devices.h | 1 S32K344.h | 1 Lin.h | 1 CDD_I2c_Cfg.h | 1 Emios_Mcl_Ip_Types.h | 1 Lpuart_Uart_Ip_Types.h | 1 Dem_stub.h | 1 Lin_PBcfg.c | 1 Lin_Types.h | 1
ARTD-6158	Bug	[wdg] Fix all M4, TABs, duplicated UUIDs ,,"Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: # Replace all TABs with 4 spaces. # Update your text editor settings to always use 4 spaces instead of a TAB # Replace duplicated UUIDs. Summary:

ID	Subtype	Headline and Description
		Plugin*|*No. of duplicated UUIDs Eth.xdm | 1 Gpt.xdm | 2 Lin.xdm | 2 Platform.xdm | 17 Port.xdm | 1 Rm.xdm | 158 Rm_s32k314_mapbga257.xdm | 23 Rm_s32k314_mqfp100.xdm | 79 Rm_s32k314_mqfp172.xdm | 79 Rm_s32k324_mapbga257.xdm | 79 Rm_s32k324_mqfp172.xdm | 79 Rm_s32k344_mapbga257.xdm | 79 Rm_s32k344_mqfp172.xdm | 79 Sai.xdm | 22 Uart.xdm | 8 Wdg.xdm | 197 *Keyword* | *Hits* \t | 2330 M4_ | 54 *File* | *Hits* Dma_Ip_Hw_Access.c | 293 main.c | 192 Lpi2c_Ip.c | 176 Dma_Ip_Hw_AccessInline.h | 175 Uart_Ipw.c | 130 FlexCAN_Ip.c | 126 Dma_Ip.h | 112 Cache_Ip_HwAcc_ArmCoreMx.h | 97 Cache_Ip.c | 78 Dem_stub.c | 71 I2c_Ipw.c | 57 Dma_Ip_Irq.c | 53 FlexCAN_Ip_HwAccess.h | 49 Clock_Ip_Private.h | 48 Dma_Ip_Cfg_Defines.h | 40 FlexCAN_Ip_Types.h | 40 Det_stub.c | 39 Uart_Ipw.h | 38 FlexCAN_Ip_HwAccess.c | 35 Lpuart_Lin_Ip_Irq.c | 32 sys_init.c | 29 S32K344_AXBS_LITE.h | 28 Dma_Ip_Driver_State.c | 28 Clock_Ip_Monitor.c | 27 FlexCAN_Ip.h | 27 Mpu_M7_Ip.c | 23 Lpi2c_Ip_Types.h | 21 system.c | 19 IntCtrl_Ip_TypesDef.h | 17 Lpuart_Uart_Ip_Irq.c | 16 Trgmux_Ip_HwAcc.h | 16 Clock_Ip_IntOsc.c | 15 Eth_PBcfg.h | 13 FlexCAN_Ip_DeviceReg.h | 12 Clock_Ip_ProgFreqSwitch.c | 12

ID	Subtype	Headline and Description
		Clock_Ip_Types.h | 11 Gmac_Ip_PBcfg.h | 9 Dma_Ip_RegOperations.m | 8 Trgmux_Ip_Types.h | 8 Gmac_Ip_PBcfg.c | 8 Power_Ip_RegOperations.m | 8 I2c_Ip_Callbacks.h | 7 Dma_Ip_Multicore.c | 7 Dma_Ip_Driver_State.h | 6 Lpi2c_Ip_Irq.c | 6 FlexCAN_Ip_Wrapper.h | 5 Flexio_Ip_Types.h | 5 Power_Ip.c | 5 Clock_Ip_Pll.c | 5 Flexio_I2c_Ip_Types.h | 5 Dma_Ip_Hw_Access.h | 5 Dma_Ip_Hwv3_Regs.h | 5 Clock_Ip_S32K3XX.h | 5 S32K344_STCU.h | 4 Lpi2c_Ip_Cfg.h | 4 Trgmux_Ip_Devassert.h | 4 Trgmux_Ip_RegOperations.m | 4 Trgmux_Ip_Cfg_Defines.h | 4 Cache_Ip_Devassert.h | 4 Can_Irq.c | 4 Dma_Ip_Devassert.h | 4 Cache_Ip.h | 3 Lpuart_Uart_Ip_Defines.h | 3 Uart_Defines.h | 3 Lpi2c_Ip_PBcfg.c | 3 Mcu_IPW.c | 2 Gmac_Ip.c | 2 FlexCAN_Ip_Irq.h | 2 Lpuart_Uart_Ip.c | 2 Can.c | 2 Xrdc_Ip.c | 2 CDD_Mcl.h | 2 Flexio_I2c_Ip_Cfg.h | 2 Flexio_I2c_Ip.c | 2 Gmac_Ip_Types.h | 1 Clock_Ip_S32K3XX.c | 1 Gpt_Ipw.c | 1 Dma_Ip_Types.h | 1 CDD_Mcl_PBcfg.h | 1 Flexio_Ip_Common.c | 1 Mcl_Example_EBT_OVER_LCU.h | 1 Mcl_Example_EBT.h | 1 Dma_Ip_Devices.h | 1 Dma_Ip_Irq.h | 1 Emios_Mcl_Ip.c | 1 Trgmux_Ip_Devices.h | 1 S32K344.h | 1 Lin.h | 1 CDD_I2c_Cfg.h | 1 Emios_Mcl_Ip_Types.h | 1 Lpuart_Uart_Ip_Types.h | 1 Dem_stub.h | 1 Lin_PBcfg.c | 1

ID	Subtype	Headline and Description
		Lin_Types.h | 1
ARTD-6129	Bug	S32K3 RTD CT Pins Config ADC Standard Input<*> When I select more than one ADC standard channels within on ADC module in S32DS Configuration Tool Pins configure, there are be errors reported. It looks like the Pins configure support only one standard input for one ADC module. But there are actually 16 standard channels within one ADC module.
ARTD-6130	Bug	S32K3 CT Pins Initial Values<*> We are not able to configure a pin's initial value if we configure it as SIUL GPIO output. We can manually add .initValue in the generated file "Siul2_Port_Ip_Cfg.c". Is it possible to add this feature into the configuration tool?
ARTD-6163	Bug	[S32K3XX]icu: Missing Emios instance 3 in S32DS<*> Missing Emios instance 3 in S32DS !image-2021-01-11-14-45-58-237.png|thumbnail!
ARTD-6165	Bug	[ETH] Hard fault happened with function Eth_GetCurrentTime<*> a hard fault happens Eth_GetCurrentTime with parameter timeQualPtr = NULL_PTR The cause from code line: return ((ETH_VALID == timeQualPtr*) ? (Std_ReturnType)E_OK : (Std_ReturnType)E_NOT_OK);
ARTD-6167	Bug	[S32XX][SENT] Wrong convert value from integer to hex for u8SentPin in Flexio_Ip_PBcfg.c<*> When test for S32CT, Flexio_Ip_PBCfg.c generate wrong u8SentPin value / Flexio pin to use as SENT Pin / / Flexio pin to use as SENT Pin / (uint8)0x $pinSelection$U, pinSelection is integer type, so can not put 0x before $pinSelection$U, Solution Delete "0x" in both Flexio_Ip_PBcfg.c and Sent_PBcfg.c for S32CT
ARTD-6168	Bug	[S32XX][SENT] Missing generating FXIO_ISR_PROCESS_TIMER_CTRL0 definition when driver is in POLLING mode<*> When test S32CT with Serial message with POLLING mode, driver will use interrupt to handle compare value by using interrupt with FXIO_ISR_PROCESS_TIMER_CTRL0. But Flexio_Ip_Cfg.h did not generate FXIO_ISR_PROCESS_TIMER_CTRL0 to use Flexio_Sent_Ip_IRQTimerHandler function. It causes Serial message did not work. Solution: FXIO_ISR_PROCESS_TIMER_CTRL0 need to defined incase driver is in POLLING mode
ARTD-6172	Bug	[S32XX][SENT] Build fail when run test on IP for S32CT<*> There are some build fail errors when compile test for S32CT on IP. 1. Flexio_Ip_Irq.c and Flexio_Sent_Ip_Types.h include Sent_Cfg.h 2. Flexio_Sent_Ip_Types.h used some definition from HL.

ID	Subtype	Headline and Description
		#if(STD_ON == SENT_DMA_FEATURE_ENABLE) const uint8 u8SentDmaChannel; /*!< Reference to the DMA Channel configure for the Request / #endif #if(STD_ON == SENT_DMA_FEATURE_ENABLE) uint8 sentDmaChannel; /*!< Reference to the DMA Channel configure for the Request / #endif
ARTD-6174	New	New Feature [ADC] Port DMA for CTU Control Mode ,,"# DMA for Control Mode to be moved in IPL # only for FIFOs, not also for result regs # use DMA IPL # use same configuration members in FIFO config as from BCTU mcal configuration dma channel as input. Buffer allocated by user # use code from Adc_Bctu_SetupDma and Adc_Ipw_BctuFifoXDmaComplete # Support Transferring FIFO RAW DATA and only result DATA (Full FIFO and only CDATA field) for K3. Similar with S32G RTM 1.0.0 Update Tresos and S32CT components Create dev test for basic validation Refer to S32G RTM 1.0.0"
ARTD-6194	Bug	[S32K3XX]icu: Missing Emios_Icu_Ip_GetCaptureRegValue function in driver code<*> Missing Emios_Icu_Ip_GetCaptureRegValue in driver code. On the other hand, Emios_Icu_Ip_EnableInterrupt and Emios_Icu_Ip_DisableInterrupt must not in static inline return type.
ARTD-6195	Bug	[GPT][S32DS] RTC Ip got undefined error in code generate with s32ct<*> RTC Ip got undefined error as below: !image-2021-01-12-09-45-12-470.png! In code generated with s32ct, Rtc_Ip_BOARD_InitPeripherals_PBcfg.c file is empty !image-2021-01-12-09-47-23-609.png! See more detail in attachment files.
ARTD-6193	New	New Feature [S32K344 BETA] [UART] - Fix memory sections for FlexIO ,,The memory sections shall be added/fixed in the lpuart and flexio drivers.
ARTD-6208	Bug	[ICU][S32K3XX] macro EMIOS_ICU_CONFIG_VS_0_PB was created incorrectly<*> macro EMIOS_ICU_CONFIG_VS_0_PB was created incorrectly. If configuration is not used eMios channel then the generation file still has EMIOS_ICU_CONFIG_VS_0_PB macro and WKPU channel (channel is used) is not generated.
ARTD-6215	Bug	[S32K3][Crypto][CT] An error has occurred when adding new 'CryptoKeyElement' and then disable 'Use HSE Key'<*> Detailed description (how to reproduce it): # Open S32DS3.4

ID	Subtype	Headline and Description
		# Add Crypto component # Add KeyCatalogs # Add CryptoKeyElements # Click on the 'Authenticated Key Export' tab # In General tab, disable 'Use HSE Key' Test Case ID (internal TC that caught the defect): Crypto_TS_Eq_Cot_01 Observed behavior: When user adding new 'CryptoKeyElement' and then disable 'Use HSE Key', an error has occurred Expected behavior: No error has occurred, when adding CryptoKeyElement
ARTD-6222	Bug	 [GPT][S32CT] Build code error in IAR compiler<*> Detailed description (how to reproduce it): Step 1: Pull code from tag GPT_012, compile plugin and generate layout Step 2: Config for GPT and dependent module Step 3: Run command: make clean generate and make build Preconditions: [...] Observed behavior: Build code error in IAR compiler. Detail was attached. Expected behavior: The project no warnings, errors after generate and build code
ARTD-6224	Bug	 [Ip_FlexCAN][FLEXCAN_IP_014_002] FlexCAN_Ip_ReceiveBlocking can not return FLEXCAN_STATUS_BUSY<*> Call FlexCAN_Ip_Receive Call FlexCAN_Ip_ReceiveBlocking => Verification point: FlexCAN_Ip_ReceiveBlocking return BUSY => fail due to it return TIMEOUT !image-2021-01-12-17-32-41-604.png!
ARTD-6231	New	 New Feature [ADC] CTU Hardware Trigger Optimization ,,"Implement feature Add dev test for basic validation CPRT requirement: ""It shall be possible to configure the CTU/BCTU channel lists only once at initialization in order to reduce cpu load when calling the Adc_EnableHardwareTrigger and Adc_EnableCtuTrigger APIs. When enabling this optimization the Adc_SetChannel service cannot be used, and the maximum size of groups cannot exceed the size of the entire command list divided by the number of adc hardware units triggered by the CTU/BCTU. This optimization can be enabled or disabled using a Boolean configuration parameter named CTU Enable Hardware Trigger Optimization. Per default this optional optimization shall be disabled."" "
ARTD-6239	Bug	 [S32K3XX][GPT] [EB_S32DS]The total number of channel of PIT instance 0 is extra without enable PIT RTI channel<*>

ID	Subtype	Headline and Description

		I find that when user want to use PIT_RTI channel, this section is declared in file Pit_Ip_Types.h:
		#if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON))
		#define RTI ((uint8)4)
		#endif
		So in case user does not enable RTI channel, the macro PIT_IP_RTI_USED will be STD_OFF, the RTI macro is not generated, so the total number of channel of PIT 0 is checked in interrupt function(PIT_0_CHANNELS_NUMBER) must not to be included RTI channel :
		ISR(PIT_0_ISR)
		{
		uint8 instance = 0U;
		uint8 channel;
		uint32 temp = 0;
		for (channel = 0U; channel < PIT_0_CHANNELS_NUMBER{color}; channel++)
		{
		temp = Pit_Ip_GetInterruptFlags(instance, channel);
		if (1U == temp)
		{
		Pit_Ip_ProcessCommonInterrupt(instance, channel);
		}
		}
		}
		The matter is PIT_0_CHANNELS_NUMBER is always defined is 5 channel. So this results hardfault when checking index channel 4 (RTI)

ARTD-6240	Bug	[GPT] Add missing PIT_2 AND STM_1 instance from resource on S32K314<*> when configuring pit and stm channels I saw a lack of resources for s32k314 This RM has described very clearly
ARTD-6243	Bug	[S32K3][SENT] Missing Usemode, DevErrorDetect in IPL for S32DS ,,"In IPL for S32DS, flexio.component is missing Usermode, DevErrorDetect node. 2 nodes should be added to Flexio.component file.
ARTD-6250	Bug	[ADC] Hard fault error when calling Adc_EnableCTUTrigger, Adc_DisableCTUTrigger before Adc_Init ,,"Detailed description (how to reproduce it): Hard fault error when calling Adc_EnableCTUTrigger, Adc_DisableCTUTrigger before Adc_Init Preconditions: Calling Adc_EnableCTUTrigger, Adc_DisableCTUTrigger before Adc_Init Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Adc_TS_045 Observed behavior: Calling Adc_EnableCTUTrigger before Adc_Init Expected det error uninit (requirement: CPR_RTD_00038.adc) Real status: Hard fault because calling const Adc_GroupConfigurationType const pGroupConfig = &(Adc_pCfgPtr[u32CoreId]->pGroups[Group]); before init Expected behavior: det error uninit

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6251	Bug	[ADC] Adc_EnableCTUTrigger, Adc_DisableCTUTrigger need to validate if TriggerSource is not configured ,,"Detailed description (how to reproduce it): Adc_EnableCTUTrigger, Adc_DisableCTUTrigger need to validate if TriggerSource is not configured for the group Preconditions: Adc_EnableCTUTrigger, Adc_DisableCTUTrigger with trigger source out of trigger source configured Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Adc_TS_045 Observed behavior: Calling Adc_Init Calling Adc_EnableCTUTrigger with trigger source is 95 (out of configuration 12) Expected det error (requirement: CPR_RTD_00038.adc) Real status: Hard fault error because implement with wrong trigger source Expected behavior: det error wrong bctu trigger source (requirement: CPR_RTD_00038.adc) Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6263	Bug	[ADC] Adc_DisableCTUTrigger report wrong det error Api ID<*> Detailed description (how to reproduce it): Adc_DisableCTUTrigger report wrong det error Api ID Preconditions: Adc_DisableCTUTrigger with sw trigger group Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Adc_TS_045 Observed behavior: Invoke Adc_DisableCTUTrigger() but the Group is sw trigger group Verification point: Det error ADC_E_WRONG_TRIGG_SRC Real status: Det error with api id ADC_ENABLECTUTRIGGER_ID Expected behavior: EU_ASSERT_FATAL(Det_TestLastReportError(ADC_MODULE_ID, 0U, ADC_DISABLECTUTRIGGER_ID, ADC_E_WRONG_TRIGG_SRC)); Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6300	Bug	[WDG][CT] EB supports multicore for 1 instance, but CT doesn't support ,,"Detailed description (how to reproduce it): Step 1: Pull code from tag WDG_045_V02, compile plugin and generate layout Step 2: Config S32CT and dependent modules Step 3: make clean generate and make build

ID	Subtype	Headline and Description
		Preconditions: [...] Observed behavior: EB supports multi-core for 1 instance, but CT doesn't support. Expected behavior: Update CT support for 1 instance to users still can configure multicore in 1 instance
ARTD-6310	Bug	 [ADC] Hard fault error when starting group using dma by fixing hard code DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS<*> Detailed description (how to reproduce it): Hard fault error when starting group using dma by fixing hard code DMA_LOGIC_CH_0_NOF_CFG_SGA_ELEMENTS Preconditions: Starting group using DMA transfer Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0101 Adc_TS_014 Observed behavior: Starting sw trigger group using DMA Verify conversion result Real status: Hard fault error as attachment because generated array by mcl driver only have 2 elements but adc driver access to the third element Expected behavior: No Hard fault error Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6313	Bug	 [platform] Pending interrupts are not clear after invoking Platform_Init in multicore context<*> Pending interrupt on all cores are not cleared except the one setting MSCM. For example: Config routing interrupt is responsible by core 0, so the pointer for core 1 is NUL, so pending interrupts will not be cleared on core 0. !image-2021-01-14-16-26-21-549.png!
ARTD-6320	Bug	 [S32K3XX]icu: Difference between header and generated file in S32DS<*> !screenshot-1.png|thumbnail! Difference of eMios_Icu_Ip_ConfigType; between generated file and header file by missing #if (EMIOS_ICU_OVERFLOW_NOTIFICATION_API == STD_ON) as attached picture
ARTD-6321	New	 New Feature [SAI] File version checks ,,File version checks
ARTD-6322	New	 New Feature [SAI] Multicore support ,,Multicore support in EBT and S32CT

ID	Subtype	Headline and Description
ARTD-6323	New	New Feature [SAI] Exclusive areas ,,Exclusive areas
ARTD-6324	New	New Feature [SAI] Variant and pre-compile support for Tresos configurator ,,"Add dev test, fix any issues Check/add also precompile support (allowing calls to Init(NULL_PTR))"
ARTD-6325	New	New Feature [SAI] S32ConfigurationTool use functional group name as variant ,,S32ConfigurationTool use functional group name as variant (workaround instead of actual variant support)
ARTD-6344	Bug	[SAI] Wrong register reset value after using Sai_DeInit service<*> Detailed description (how to reproduce it): Wrong register reset value after using Sai_DeInit service After using Sai_DeInit service the TCSR register has wrong reset value, see the yellow highlight below: Wrong reset value 'SR' field in TCSR register Wrong RX register in Sai_Ip_RxDeInit function !image-2021-01-15-11-03-11-377.png! !image-2021-01-15-13-28-13-425.png! The Sai_DeInit service will disable the SAI module and configure the registers to their reset values. ID: 5 Req ID: SWS_SAI_00201 Master Req ID: Remarks: Comments (not visible in TM): Functionality / Item: Sai_DeInit Req Type: Functional Product: S32K3XX Fulfilled In: S32K3XX Req State: Approved Verification Criteria: Test Case Preconditions: [...] Observed behavior: Wrong register reset value after using Sai_DeInit service Expected behavior: Correct register reset value after using Sai_DeInit service Proposed solution optional:
ARTD-6351	Bug	[ICU] Update version checking for driver<*> Update version checking based on the attached violation report.
ARTD-6352	Bug	[PWM] Update version checking for driver<*>

ID	Subtype	Headline and Description
		Update version checking based on the attached violation report.
ARTD-6354	Bug	[OCU] Update version checking for driver<*> Update version checking based on the attached violation report.
ARTD-6355	Bug	[GPT] Update version checking for driver<*> Update version checking based on the attached violation report.
ARTD-6358	Bug	[platform] Compile error when installing NULL_PTR to interrupt handler.<*> There is error in compiling when config interrupt handler is NULL_PTR. !image-2021-01-15-15-13-26-929.png! !image-2021-01-15-15-14-22-419.png! The driver should add checking to not allow config NULL_PTR or NULL. However this limit ability to setting interrupt handler to NULL pointer.
ARTD-6364	Bug	[GPT] the macro EMIOS_GPT_IP_ENABLE_DISABLE_NOTIFICATION_API should not be guarded for using interrupt of EMIOS<*> If user does not enable notification function in autosar, the macro EMIOS_GPT_IP_ENABLE_DISABLE_NOTIFICATION_API = STD_OFF, so the interrupt function will not be declared. This results to error when user enable Emios hardware. !image-2021-01-15-17-06-50-414.png!
ARTD-6367	New	New Feature [SAI] Configurable BIT_CLK_SWAP and PACK_MODE ,,"Implement BIT_CLK_SWAP and PACK_MODE Add dev test for validation"
ARTD-6378	New	New Feature [SAI] Masking support ,,"Implement masking support preferably add as member in Sai_RequestType (and call Sai_Ip_SetNextMaskWords set Master Req ID in Doors Sai IP) or add new function at HLD layer to wrap Sai_Ip_SetNextMaskWords "
ARTD-6381	Bug	[S32K3xx][MCL] Array configuration is always NULL_PTR on S32DS<*> S32CT: Enable EMIOS common support is enabled in general tab but MCL array configuration is always NULL_PTR !image-2021-01-17-10-08-40-737.png|thumbnail! Two configs created with the same name !image-2021-01-17-11-17-22-821.png|thumbnail! Default period should be updated to be greater than offset at start value when user adds a new configuration Need to add a warning when user configuration is incorrect: Two configs with the same EMIOS instance Default period is greater than 65535

ID	Subtype	Headline and Description
		EB tresos: Add description for EmiosMclMasterBusModeType on EB !screenshot-1.png|thumbnail! Need to add a warning when user configuration is incorrect: Default period is less than or equal to offset at start value !screenshot-2.png|thumbnail!
ARTD-6383	Bug	[S32K344][S32CT] Wrong maximum number of ADC channels in the BCTU command list<*> Detailed description (how to reproduce it): Use S32DS config for BCTU. In List command: The value maximum for list is 24. However, in RM is 32 Preconditions: Use S32DS config for BCTU. Observed behavior: !image-2021-01-18-08-37-20-120.png! Expected behavior: The value maximum of List command is 32. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-6393	Bug	[ICU][S32K3XX] SIUL2 and WKPU couldn't test Edge Detection with DS.<*> SIUL2 and WKPU don't have Notice, so Edge Detection can't be tested using DS.
ARTD-6425	Bug	[GPT] The prescaler of Emios channel is not changed accurately<*> When i change the prescaler of emios channel from value 2 to 3, the value of prescaler register need to be changed from 1 to 2. In fact in debug interface, I see the register change from 1 to 3. !image-2021-01-18-15-49-18-977.png! And configuration in EB as below : !image-2021-01-18-15-51-00-528.png! The reason for this is the old prescaler value in register is not cleared before writing the new value. !image-2021-01-18-15-55-07-552.png!
ARTD-6446	Bug	[S32K344 BETA][SENT] Timer Compare Register can not be updated when run on CORE_1<*> Issue*: When run test Sent_TS_100, Sent_TS_101 on CORE_1 or Multicore testing, Timer Compare Register can not be updated in both POLLING and INTERRUPT mode. Solution: Issue comes from Debug Enable bit (FlexIO Control Register). Timer Compare Register can be updated only when set Debug Enable bit.
ARTD-6458	Bug	[S32K344 BETA][SENT] Improve CYCLOMATIC COMPLEXITY<*> Issue: Sent has a function which CYCLOMATIC COMPLEXITY > 20.

ID	Subtype	Headline and Description
		It comes from Flexio_Sent_Ip_GetSerialMsgData (with CYCLOMATIC COMPLEXITY = 22) Please improve Flexio_Sent_Ip_GetSerialMsgData to have CYCLOMATIC COMPLEXITY < 20.
ARTD-6457	New	 New Feature [ETH]Fix misra(continue) ,,"Fix misra rule 10.4, 5.6"
ARTD-6460	Bug	 [SPI] Update driver code to reduce CYCLOMATIC COMPLEXITY and HIS metrics<*> Please update the driver to reduce CYCLOMATIC COMPLEXITY and HIS metrics for some functions: Event Description|Function Measured value of LEVEL metric 7.00 is higher than maximum value 4.00 allowed by the HIS metrics policy.|Lpspi_Ip_TransferProcess Measured value of LEVEL metric 5.00 is higher than maximum value 4.00 allowed by the HIS metrics policy.|Spi_Ipw_EndChannelCallback Measured value of LEVEL metric 7.00 is higher than maximum value 4.00 allowed by the HIS metrics policy.|Lpspi_Ip_SyncTransmit Measured value of CCM metric 25.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|Lpspi_Ip_SyncTransmit Measured value of CCM metric 27.00 is higher than maximum value 10.00 allowed by the HIS metrics policy.|Lpspi_Ip_TransferProcess
ARTD-6468	Bug	 [S32K3XX][PWM] Cyclomatic complexity of Emios_Pwm_Ip_SetDutyCyclefunction higher than 20<*> Emios_Pwm_Ip_SetDutyCycle functions have complexity higher than 20, need to update to less than 20
ARTD-6464	Bug	 [S32K3XX][ETH] The Gmac_Ip_ProvideRxBuff function does not work as expected with GCC compiler<*> The Gmac_Ip_ProvideRxBuff function does not work as expected with GCC compiler. Steps to reproduce: Initialize the GMAC module with reception ring size is 4, MAC loopback mode Send and Read the 4 prepared Ethernet frames => all frames are received successfully (and all the buffers in the receive ring are full) Provide the a new buffer pointing to a new memory area, then it will be used by the driver for further reception because all the buffers in the receive ring are full (call Gmac_Ip_ProvideRxBuff) Send and Read the fifth Ethernet frame Expected behavior:* When all the buffers in the receive ring are full, reading new frames will not work anymore; thus, by calling this function to provide a new buffer which is not used anymore pointing to a new memory area, the new frame will be received Actual behavior:* The frame is not received in run mode (it only received when run debug step by step for Gmac_Ip_ProvideRxBuff function)
ARTD-6475	Bug	 [SAI] Warnings in compiler warning report<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		There are some warnings in the Compiler Warnings report. For more details, please refer the report.[^RTD_SAI_Compiler_Warnings.xlsx] Preconditions: [...] Observed behavior: warnings in the Compiler Warnings report Expected behavior: No warnings in the Compiler Warnings report Proposed solution optional:
ARTD-6478	Bug	[S32K3XX][PWM] Missing extern call back function in Emios PBcfg.c file and define Emios ISR_USED<*> Missing extern call back function in Emios PBcfg.c file. It cause fail at build. If call back function is NULL_PTR, we can not pass dev essert: DevAssert(NULL_PTR != userChCfg->userCallback.cbFunction) and fail at run. Missing define EMIOS ISR_USED. It is used in process the interrupt function in Emios_Mcl_Ip_Irq.c file. If not defined, the function will not execute anything
ARTD-6491	Bug	[ICU] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): For GPT I received this ticket I think you should check in your driver too. GPT's issue: GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. !image-2021-01-20-10-21-42-289.png|width=564,height=385! Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.
ARTD-6494	Bug	[S32K3XX][S32XX] OCU: Code generation error "config class PostBuild which is not allowed in this context"

ID	Subtype	Headline and Description
		,,"Detailed description (how to reproduce it): For GPT I received this ticket I think you should check in your driver too. GPT's issue: GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. !image-2021-01-20-10-21-42-289.png|width=564,height=385! Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.
ARTD-6506	Bug	[CRYPTO] Spelling error<*> There is a spelling error in CRYPTO module. CYRPTO*_KE_KEYEXCHANGE_SHAREDVALUE CRYPTO spelling needs to be corrected to get the build through with the definition as expected by CSM upper module.
ARTD-6523	Bug	[SIUL2][ICU]:config tools generate "0" numChannel in configuration struct ,," Siul2_ICU initial process didn't work: In Siul2_Icu_Ip_Config_BOARD_INITPERIPHERALS the numChannels always be 0, didn't change by the config tools, and resulting SIUL_ICU initial failed without return any error. Location : Siul2_Icu_Ip_StA_BOARD_InitPeripherals_PBcfg.c !image-2021-01-21-16-27-35-791.png!
ARTD-6526	Bug	[ICU][S32DS] Correct version checking added on DS generated files<*> Newly added version check of files does not take into account that for \ in DS generator we need to put \\\.

ID	Subtype	Headline and Description
		All lines are generated without line concatenation so we have build error in DS. Also remove not used file Cmp_Ip_Defines.h from git repo
ARTD-6528	Bug	 [port] Fix MISRA violations<*> Detailed description (how to reproduce it): There are some misra violation which need to be fixed or comment. Please refer the attachment for more detail Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There are some misra violation Expected behavior: There is no misra violation Proposed solution optional:
ARTD-6525	Bug	 [SIUL2][ICU]:ICU ISR is blocked<*> The SIUL2 ISR is always blocked, the config tools didn't generate the correct DEFINES AND MACROS. Location : Siul2_Icu_Ip_Irq.c !image-2021-01-21-16-38-05-697.png! !image-2021-01-21-16-46-02-068.png! Location : Siul2_Icu_Ip_Cfg.h !image-2021-01-21-16-38-48-782.png!
ARTD-6538	Bug	 [CRYPTO]Crypto_Hse_ExportCipherScheme() called with NULL pointer parameter<*> If the configured CryptoKeyElement is used for symmetric key export without enabling the export, not ticking _HSE Key Export_, the configuration structure will generate with `pHseExportCipherScheme` as null pointer and the export request done via Crypto_KeyElementGet() API will call Crypto_Hse_ExportCipherScheme() with null pointer.
ARTD-6541	Bug	 Number of LPSPI External Devices<*> When configuring LPSPI for S32K344 in s32ds3.4 CT, I can add 5 external devices at the most. If add one more external device in the LPSPI configuration, there are errors reported. See attached figure. And the mex file is with errors even after removing the LPSPI module in CT.
ARTD-6542	Bug	 s32k344 emios icu module issue<*> When configuring s32k344 in s32ds3.4, after adding Emios_Icu_Ip module into the project, the generated code is with problem. The Emios_Icu_Ip_ChannelConfigType structure generated in "Emios_Icu_Ip_StA_BOARD_InitPeripherals_PBcfg.c" doens't match this structure type definition in "Emios_Icu_Ip_Types.h" const Emios_Icu_Ip_ChannelConfigType Emios_Icu_Ip_0_ChannelConfig_PB_BOARD_INITPERIPHERALS[1U] = { / brief IcueMios_0_Channel_0 /

ID	Subtype	Headline and Description

		{
		/ brief Emios HW Module and Channel used by the Icu channel /
		0U,
		/ brief Emios Channel Freeze bit /
		FALSE,
		/ brief Emios Prescaler value /
		EMIOS_PRESCALER_DIVIDE_1,
		/ brief Emios Alternate Prescaler value /
		EMIOS_PRESCALER_DIVIDE_1,
		/ brief Emios IcuEmiosDigitalFilter value /
		EMIOS_DIGITAL_FILTER_BYPASSED,
		/ brief Emios IcuEmiosBusSelect value /
		EMIOS_BUS_INTERNAL_COUNTER,
		/ brief Emios IcuUserModeForDutycycle value /
		SAIC,
		/ brief Emios IcuSignalMeasureWithoutInterrupt bit /
		FALSE,
		/ brief Callback Pointer /
		NULL_PTR,
		/ brief Callback Param1*/
		0U
		}
		};
		
		typedef struct
		{
		uint8 hwChannel; /*!< Channel Id /
		eMios_Icu_Ip_UCModeType ucMode; /*!< eMios UC mode of operation /
		eMios_Icu_Ip_ModeType chMode; /*!< eMios module mode of operation /
		eMios_Icu_Ip_SubModeType chSubMode; /*!< eMios specific name of operation to execute /
		eMios_Icu_Ip_MeasType measurementMode; /*!< Measurement Mode for signal measurement*/
		eMios_Icu_Ip_EdgeType edgeAlignement; /*!< Edge alignment Mode for signal measurement*/
		boolean FreezeEn; /*!< Freeze enable /
		eMios_Icu_Ip_PrescalerType Prescaler; /*!< Channel Prescaler /
		eMios_Icu_Ip_PrescalerType AltPrescaler; /*!< Channel Alternate Prescaler /
		eMios_Icu_Ip_FilterType Filter; /*!< Channel Digital Input Filter /
		eMios_Icu_Ip_BusType CntBus; /*!< Channel Counter bus selection /
		boolean bWithoutInterrupt; /*!< Measurement of ICU signal property without using interrupt /
		CallbackFunctionTimestamp callbackTimestamp; /*!< The callback function for timestamp events /
		eMios_Icu_Ip_SignalMeasurementCallbackType callbackSM; /*!< The callback function for channels signal measurement /
		eMios_Icu_Ip_CallbackType callback; /*!< The callback function for channels edge detect events /
		uint8 callbackParams; /*!< The parameters of callback functions for channels events /
		} eMios_Icu_Ip_ChannelConfigType;

ARTD-6543	Bug	[Wdg] Wdg_ChannelClearResetRequest must raise det instead of return code<*> Swt_Ip_RequestedReset must return SWT_IP_STATUS_TIMEOUT (instead of ERROR) if timeout occurred. Update also in SWT IP req in doors Wdg_ChannelClearResetRequest must raise det instead of return code: raise WDG_E_PARAM_TIMEOUT for SWT_IP_STATUS_TIMEOUT

ID	Subtype	Headline and Description
		raise WDG_E_DRIVER_STATE when Swt_Ip_RequestedReset returns SWT_IP_STATUS_ERROR
ARTD-6545	Bug	[ADC] Adc_SetPowerState does not power down/up also BCTU when configured<*> [ADC] Adc_SetPowerState must power down/up also BCTU if configured
ARTD-6551	Bug	[S32K3XX] icu: Build fail due to some Define names are not correct with DS<*> !image-2021-01-22-11-27-27-906.png|thumbnail! Build fail due to some Define names are not correct with DS as picture
ARTD-6566	Bug	[S32K3xx][MCL] DEV_ASSERT should be added in driver code<*> EMIOS module on S32K344 only supports 3 instances and 24 channels so DEV_ASSERT should be added in driver code to check invalid input parameter for all functions as below: Emios_Mcl_Ip_Init Emios_Mcl_Ip_EnableChannel Emios_Mcl_Ip_DisableChannel Emios_Mcl_Ip_ComparatorTransferEnable Emios_Mcl_Ip_ComparatorTransferDisable Emios_Mcl_Ip_GetInstanceStatus Emios_Mcl_Ip_GetDebugMode Emios_Mcl_Ip_GetCounterBusMode Emios_Mcl_Ip_GetCounterBusPeriod
ARTD-6563	Bug	[ADC] Hard fault error when calling Adc_GetStreamLastPointer before Adc_Init<*> Detailed description (how to reproduce it): Hard fault error when calling Adc_GetStreamLastPointer before Adc_Init Preconditions: Calling Adc_GetStreamLastPointer before Adc_Init Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1201 Adc_TS_018 Observed behavior: Calling Adc_GetStreamLastPointer before Adc_Init Expected det error uninit (requirement: CPR_RTD_00038.adc) Real status: Hard fault because calling const Adc_GroupConfigurationType pGroupPtr = &(Adc_pCfgPtr[u32CoreId]->pGroups[GroupIndex]); Expected behavior: det error uninit Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-6570	Bug	[GPT][RTC] Hardfault error when change the variable in output config as placing it in flash memory sector<*> When user use the Alarm feature. First user need to call function Rtc_Ip_ConfigureAlarm In this function, the pointer alarmConfig inside Rtc_Ip_u32ChState is pointed to the value of output alarm configuration . So the value of alarmConfig is not able to changed, because it is allocating in the flash memory.

ID	Subtype	Headline and Description
		!image-2021-01-22-17-05-45-660.png! And in the interrupt funtion, a ointer variable is declared again and it is pointed to the alarm config pointer inside Rtc_Ip_u32ChState. So it means the variable alarmConfiguration in interrupt function is pointing to the address of the output alarm configuration. !image-2021-01-22-17-10-28-489.png! When have a change in value of pointer variable alarmConfiguration, it will result to a hardfault error as below: !image-2021-01-22-17-11-49-982.png! Because the alarm configuration generated is in a memory that is not changeable. !image-2021-01-22-17-13-09-405.png!
ARTD-6571	Bug	[GPT] Build fail when enable Gpt Timeout Dem Error<*> When I used the PIT_0_CH_RTI channel and turned on the GPT_E_TIMEOUT feature, the test encountered a build error. (uint16)DemConf_DemEventParameter_DemEventParameter_0}; "d:\cc_work\zebra\S32K3XX_4.4\output\S32K3XX_S32K344\gpt\Gpt_TS_301_cfg2\generate_tresos\src\Gpt_Cfg.c",72 Error[Pe020]: identifier "DemConf_DemEventParameter_DemEventParameter_0" is undefined Errors: 1 Warnings: none make: [Makefile:1041: Gpt_Cfg_c.o] Error 1
ARTD-6578	New	New Feature [S32K3XX][PWM][FLEXIO] Implement PWM over FLEXIO ip ,,"EBT 3-7d xdm user interface generation templates vsmd check only check existing example to not have issues Resource files to be used on EBT and DS as well. 1d DS 3-5d component user interface generation templates and manifest updates/addition epd/epc compliance check only check existing example to not have issues Requirements definition in separate xls file 1d IPL static code create/update/review 5d Update plugin makefile IPW code update/review 1d Dev test create/update to contain FLEXIO channels 1d Review xls of requirements for DOORS upload 1d Design update for flexio requirements Sharing strategy and implementation into MCL Example code for IPL and HLD as a separate branch from the code branch 2d Very rough estimatation: 2.5w 4w"
ARTD-6588	Bug	[S32K3XX][PWM] Pwm_GetChannelState function can not work in IDLE state<*> In the IDLE state, the channel mode will be changed to the GPO mode. If call Pwm_GetChannelState function then and this function call Emios_Pwm_Ip_GetDutyCycle function, It cannot check the correct mode in use and go to DevAssert(FALSE); And if using recalculate duty based on period and duty of Emios.

ID	Subtype	Headline and Description
		emiosChDuty = Emios_Pwm_Ip_GetDutyCycle(ipConfig->channelInstanceId, ((Emios_Pwm_Ip_ChannelConfigType)ipConfig->channelConfig)->channelId); / Get the period of the chanel / emiosChPeriod = Emios_Pwm_Ip_GetPeriod(ipConfig->channelInstanceId, ((Emios_Pwm_Ip_ChannelConfigType)ipConfig->channelConfig)->channelId); / Calculate new duty value in ticks / dutyCycle = (uint16)(0x8000U ((float)emiosChDuty / emiosChPeriod)); it will cause the error. This is not correct for tick units
ARTD-6592	Bug	[GPT] The function Pit_Ip_ChainMode does not work correctly<*> !image-2021-01-25-13-29-22-065.png! The chainmode channel need to count from 1.
ARTD-6595	Bug	[SAI] DBGE not configurable<*> DBGE not configurable Check if other bits/functionalities are not added in configuration (except one for which ticket is already raised)
ARTD-6599	New	New Feature [ETH]Fix HIS LEVEL ,,Some functions have nesting level > 4.
ARTD-6590	Bug	[GPT] Fix compiler warning S32K3XX<*> Fix compiler warning for S32K3xx
ARTD-6600	Bug	[SAI] CPR_RTD_00011 ISR function did not fully check the initialization status<*> Detailed description (how to reproduce it): CPR_RTD_00011 ISR function did not check initialization status. ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately.ISR shall check whether its respective driver is initialized. If the driver is not initialized, the ISR shall only clear interrupt status flag and return immediately. ID: 11 Req ID: CPR_RTD_00011 Currently, the ISR function only check callback field, there may be a case when the default initialization value is not NULL_PTR. Preconditions: [...] Observed behavior: Expected behavior: Proposed solution optional: Refer to LPI2C driver static Lpi2c_Ip_SlaveStateType g_lpi2cSlaveStatePtr[LPI2C_INSTANCE_COUNT] = \{

ID	Subtype	Headline and Description

		NULL_PTR}
		
		;
		Lpi2c_Init()
		{
		
		g_lpi2cSlaveStatePtr[instance] = userConfigPtr->slaveState;
		}

ARTD-6607	Bug	[ADC] The Adc_CtuSetListPointer() API does not keep value of other bits in BCTU.MCR Register<*> Detailed description (how to reproduce it): When use the Adc_CtuSetListPointer() function reconfigure position of the first channel of the command list, it affect some bit in register BCTU_TRGCFG Preconditions: Details review test case Adc_TC_FCT_0708 Observed behavior: When use the Adc_CtuSetListPointer() function reconfigure affect some bit in BCTU_TRGCFG register. In test case Adc_TC_FCT_0708, when calling the Adc_CtuSetListPointer() the bits TRGCFG_DATA_DEST, ADC_SEL0 are affected. Expected behavior: When using the Adc_CtuSetListPointer () function, reconfiguration does not affect some of the bits in the previously configured BCTU_TRGCFG register. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-6610	Bug	[platform] S32DS Compile error when installing NULL_PTR to interrupt handler.<*> There is error in compiling when config interrupt handler is NULL_PTR. !image-2021-01-15-15-13-26-929.png! !image-2021-01-15-15-14-22-419.png!

ID	Subtype	Headline and Description
		The driver should add checking to not allow config NULL_PTR or NULL. However this limit ability to setting interrupt handler to NULL pointer.
ARTD-6604	Bug	[SAI] Wrong mapping data type between EBT and S32CT<*> Detailed description (how to reproduce it): There are some fields on S32CT that are not mapping the data type between EBT and S32CT [^SAI_NodeToM4.xlsx] Refer link: [https://nxp1.sharepoint.com/:p:/s/Zebra/EaMbpShSxPVAq7amkzZx3NMB1LWDlRvDlnrzP1m0TZ9elQ?e=TJtb0O] Slide 19 Preconditions: [...] Observed behavior: warnings in the Compiler Warnings report Expected behavior: No warnings in the Compiler Warnings report Proposed solution optional:
ARTD-6631	Bug	[GPT] Example EBT cannot generate due to MCU<*> Gpt EBT Example cannot generate due to Mcu error: !image-2021-01-26-09-37-18-619.png!
ARTD-6675	Bug	PIT RTI support<*> The S32_CT cannot generate correct PIT configuration for PIT_RTI after enable PIT_RTI feature(PIT_IP_RTI_USED = STD_ON): typedef struct { uint8 hwChannel; /**< brief Timer channel number / Pit_Ip_UnitModeType periodUnit; /**< brief Period value unit / #if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON)) errorReportCallBackType errorReportCallBack; /**< brief errorReportCallBack / #endif boolean enableInterrupt; /**< brief Enable interrupt generation / Pit_Ip_CallbackType callback; /**< brief callback / uint8 callbackParam; /**< brief callbackParam / } Pit_Ip_ChannelConfigType_; typedef struct { boolean chInit; /**< brief chInit / #if (defined (PIT_IP_RTI_USED) && (PIT_IP_RTI_USED == STD_ON)) errorReportCallBackType errorReportCallBack; /**< brief errorReportCallBack / #endif Pit_Ip_CallbackType callback; /**< brief callback / uint8 callbackParam; /**< brief callbackParam / } Pit_Ip_State; No configuration of *errorReportCallBack* for the above two structures.

ID	Subtype	Headline and Description
ARTD-6678	New	New Feature [PORT] Update the name of Touch Sense function to follow the requirements ,,"There are 2 functions which need to be renamed in the driver to follow the requirements: From: Tspc_Port_Ip_Enable*OBE*Group Tspc_Port_Ip_Configure*OBE*Group To: Tspc_Port_Ip_Enable*Obe*Group Tspc_Port_Ip_Configure*Obe*Group"
ARTD-6682	Bug	[wdg] CR->STP allowed for configuration even if not supported on SWT_1<*> CR->STP not supported on SWT_1 Make readonly in configurators (EBT and CT) using a new resource variable
ARTD-6688	Bug	[S32K344] MCL: TC build fail with multi-variant on CT<*> TC build fail with multi-variant on CT !image-2021-01-26-15-43-59-696.png!
ARTD-6690	New	New Feature [S32K344 BETA] OCU: Implement CPR_RTD_00522 restrictions and updates in CPR_RTD_00511 ,,"NewWorkDescription: Updates according to the updates in the requirement: *CPR_RTD_00511 CPR_RTD_00522*: Drivers capable of using Counter Buses shall not allow selection of an Counter Bus with exclusive access granted to PWM. The check will be performed at configuration time. Applicable only for Icu, Ocu, on eMIOS Requirement source: Customer Request CPR_RTD_00511 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API that will update (buffered change expected) the match/reload value for the counter selected."
ARTD-6698	Bug	[S32K3XX][PWM] Fix the compiler warning and failed building in DS examples<*> The DS example has compiler warning and failed building with Pwm_Example_Ds
ARTD-6695	Bug	[S32K344][LIN] When header transmit and have a error occurred, driver doesn't return LIN_TX_HEADER_ERROR. ,,"When header transmit and have a error occurred, IRQ function will return linCurrentState->currentEventId = LPUART_LIN_IP_READBACK_ERROR and in callback function will return Lin_Ipw_au8LinChFrameErrorStatus[u8Channel] = LIN_TX_ERROR_U8. When function Lin_GetStatus called funciton Lin_Ipw_ErrorGetStatus will check and return LIN_TX_HEADER_ERROR if

ID	Subtype	Headline and Description
		Lin_lpw_au8LinChFrameErrorStatus[u8Channel] = LIN_TX_HEADER_ERROR_U8 but it equal *LIN_TX_ERROR_U8* then driver doesn't return LIN_TX_HEADER_ERROR
ARTD-6707	Bug	[SAI] State structures allocated for all instances even if not used<*> State structures allocated for all instances even if not used Update also EBT and S32CT
ARTD-6710	Bug	[DIO] Fix MISRA violations<*> Detailed description (how to reproduce it): There are some misra violation which need to be fixed or comment. Please refer the attachment for more detail Preconditions: NA Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: There are some misra violation Expected behavior: There is no misra violation Proposed solution optional:
ARTD-6716	Bug	[ETH] Fix compiler warning for S32K3XX BETA 0.9.0 release<*> There are 2 warning when compile the driver code with GCC and IAR compiler. Please check the attached file.
ARTD-6725	Bug	[BASE] UM missing stub file information<*> The Base UM should include the information about the stub files, to be clear which file can be changed or not by an integrator, customer. For Reference, check the attached manual and screenshot. !image-2021-01-27-11-47-11-574.png!

ARTD-6728	Bug	[ADC][EXAMPLE] Some example description should be updated<*>
		
		Detailed description (how to reproduce it):
		In EBT example description*, I think you should add the expected output like this:
		If the result is correct, the program will go through to the end of code without stuck in loop with bStatus variable is set as "True"
		In Adc_example_DS_IP description*, the expected output is :
		If all conditions are correct, the code goes to the end of program without stuck in loop
		In the main.c of Adc_example_DS_IP
		for(;;)
		{
		if(exit_code != 0)
		{
		break;
		}
		}

ID	Subtype	Headline and Description
		When debug example, the program is stuck in this for loop, although that means example works normally but I think there is a conflict with description "the code goes to the end of program without stuck in loop" Preconditions: [...] Observed behavior: Some description are missing and not matching with code. Expected behavior: Right example description. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-6751	Bug	[CAN] Driver may call CanIf_TxConfirmation with wrong swhandler with TxProcessing is INTERRUPT<*> Driver may call CanIf_TxConfirmation with wrong swhandler with TxProcessing is INTERRUPT In Can_Write, PduInfo->swPduHandle should be saved before FlexCAN_Ip_Send is triggered, else in case of the transmission was complete sooner (before PduInfo->swPduHandle is saved), the unexpected value will be reported to CanIf_TxIndication. !image-2021-01-28-08-44-07-176.png! Expectation:
ARTD-7080	Bug	[STM]:config tools can't generate source code<*> Config tools "problems" found errors !image-2021-01-28-14-35-02-418.png! The file "Stm_Ip_BOARD_InitPeripherals_PBcfg.c" didn't generated any contents. !image-2021-01-28-14-35-09-563.png!
ARTD-7083	Bug	[CRYPTO] Missing MU instance parameter in Hse_Ip_GetHseStatus function<*> Function "*Hse_Ip_GetHseStatus*" can't get status from other MU instance except "0U" Is "*Hse_Ip_GetHseStatus*" could have a parameter like "*_u8MuInstance_*" to get status of other MU instances? !image-2021-01-28-14-39-47-562.png!
ARTD-7084	Bug	[S32DS 3.4] Has an error "Path to collateral manifest does not exist ${eclipse_home}../S32DS/software/PlatformSDK_S32K3_2021_02/itm.s32k3.rtd.collateral.PlatformSDK_S32K3_2021_02.xml" after finishing the installation ,,"Detailed description (how to reproduce it): Step 1: Install package: S32DS: S32DS.3.4_b201217_win32.x86_64.exe Development package: SW32K3_S32DS_3.4.0_D2012.zip and com.nxp.s32ds.s32r45.update_3.4.1.20210115121654.zip Update site: S32K3XX_RTD_4_4_BETA_0_9_0_DS_updatesite_2101.zip Preconditions:

ID	Subtype	Headline and Description
		[...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Has an error ""*Path to collateral manifest does not exist ${eclipse_home}../S32DS/software/PlatformSDK_S32K3_2021_02/itm.s32k3.rtd.collateral.PlatformSDK_S32K3_2021_02.xml*"" after finishing the installation Detail was attached. Expected behavior: After finishing the installation there was no warning or error
ARTD-7088	Bug	[PINS][S32CT] Cannot configure direction Input_Output for for PTD16 (EMAC_MDIO)<*> When I test example for ETH module (Eth_Example_DS_001 for IPL) on S32CT (([S32K3XX_RTD_4_4_BETA_0_9_0_DS_updatesite_2101.zip| http://transgateway.nxp.com/cgi-bin/trans/index.pl?path=/Transcend_Gateway/RTD/S32K3XX/4_4/BETA_0_9_0/S32K3XX_RTD_4_4_BETA_0_9_0_DS_updatesite_2101.zip] Wed Jan 27 19:22:31 2021), There is an issue for PTD16: it cannot be configured direction as Input_Output. Please check the attached screen-shot.
ARTD-7097	Bug	[ADC] Build fail when not configuring anything in BctuHwUnit tab<*> Detailed description (how to reproduce it): Build fail when not configuring anything in BctuHwUnit tab Preconditions: AdcEnableCtuControlModeApi is enable Add BctuHwUnit_0 by default (click on add icon in tab BctuHwUnit) Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 45 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:"e:/S32K3/output/S32K3XX_S32K344/adc/Adc_TS_COT_011_cfg45/generate_tresos/src/Bctu_Ip_VS_0_PBcfg.c", line 157: error #1981-D: STDERR: empty initializer is non-standard STDERR: }; STDERR: STDERR: More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7093	Bug	[BASE] Some compiler options are not the same between SOW and S32CT<*> Detailed description (how to reproduce it): Step 1: Create new project. Step 2: Select project > right click > Properties > C/C Build > Settings Step 3: Check compiler options and compare with SOW file

ID	Subtype	Headline and Description
		Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Some compiler options are not the same between SOW and S32CT : Compiler: Missing : fno-zero-initialized-in-bss Linker: Duplicate: mcpu=cortex-m7 In file SOW*: Map=<map_file_name> and -mfloat-abi=soft but CT is: Map and -mfloat-abi=softfp Expected behavior: Update compiler option for CT the same with compiler option in SOW file.

ARTD-7099	Bug	[ADC] Adc_Ipw_StopCurrentConversion uses incorrect channel index resulting in hardfault<*>
		
		Adc_Ipw_StopCurrentConversion uses incorrect channel index resulting in hardfault (for example for ChIndex=18)
		#if (ADC_SETCHANNEL_API == STD_ON)
		ChIndexTemp = Adc_aRuntimeGroupChannel[Group].pChannel[ChTemp];
		#else
		ChIndexTemp = Adc_pCfgPtr[u32CoreId]->pGroups[GroupIndex].pAssignment[ChTemp];
		#endif
		(void)Adc_Sar_Ip_GetConvData(Unit, ChIndexTemp);
		Must be:
		(void) Adc_Sar_Ip_GetConvData(Unit, (uint32)Adc_pCfgPtr[u32CoreId]->pAdcIpwConfig->apAdcConfig[LogicalHwUnitId]->pChannelConfigs[ChIndexTemp].u8ChannelIndex);
		Like in Adc_Ipw_ClearValidBit. Consider using this function

ARTD-7123	Bug	[I2C][S32K3XX] Fix some function which has HIS violation<*> Some functions have HIS_LEVEL above 4.00 Refer to attached file to see detail and fix all of them
ARTD-7192	Bug	[ADC] Build fail: "implicit declaration of function 'Adc_Ipw_IsChannelEnable and 'ChannelExist' undeclared" in Adc_Ipw.c ,,"Detailed description (how to reproduce it): Build fail: ""identifier ""ChannelExist"" is undefined"" Preconditions: Compiler gcc Using function Adc_Ipw_HwResultReadGroup (ADC_ENABLE_CTUTRIG_NONAUTO_API = ON) ADC_ENABLE_CH_DISABLE_CH_NONAUTO_API = ON ADC_READ_GROUP_API = OFF Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 05 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c: In function 'Adc_Ipw_HwResultReadGroup':

ID	Subtype	Headline and Description
		STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:2147:29: error: implicit declaration of function 'Adc_Ipw_IsChannelEnable' [-Werror=implicit-function-declaration] STDERR: 2147 ChannelEnable = Adc_Ipw_IsChannelEnable(LogicalHwUnitId, GroupId, ChIndex, u32CoreId); STDERR: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:2150:49: error: 'ChannelExist' undeclared (first use in this function); did you mean 'ChannelCount'? More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7193	Bug	[ADC] Tresos Build fail: "identifier "Dma_Ip_LogicChannelTransferListType" is undefined in Bctu_Ip.c with PreCompile enabled and Variant Size <= 1 ,,"Detailed description (how to reproduce it): Build fail: ""identifier ""Dma_Ip_LogicChannelTransferListType"" is undefined in Bctu_Ip.c Preconditions: CtuEnableDmaTrasferMode is enable Using VariantPreCompile Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_011 cfg 03 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:""e:/S32K3/output/S32K3XX_S32K344_ghs/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Bctu_Ip.c"", line 1318: error #20: STDERR: identifier ""Dma_Ip_LogicChannelTransferListType"" is undefined STDERR: Dma_Ip_LogicChannelTransferListType LocTransferList[12U]; More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7213	Bug	[WDG] SWT_1 must not be accessed by customers on S32K344 and S32K314<*> [WDG] SWT_1 must not be accessed by customers on S32K344 and S32K314 According to RM rev2Draft A supported for 0.9.0 release !image-2021-01-29-13-06-37-271.png|thumbnail!
ARTD-7215	Bug	[ETH]Fix build failed<*> Used \\\ instead of cause failure.
ARTD-7218	New	New Feature

ID	Subtype	Headline and Description
		[ADC] Add support for XSTRGEN external start feature ,,"Add support for XSTRTEN external start feature Integrate in IPL and HLD configurator. No new API is required. !screenshot-1.png|thumbnail! !screenshot-2.png|thumbnail! This must be used via TRGMUX"
ARTD-7219	Bug	[SAI] Wrong memory section<*> Wrong memory section for callback functions in Sai_Ip_PBcfg.h Functions should be in SAI_START_SEC_CODE / SAI_STOP_SEC_CODE.
ARTD-7225	Bug	[ADC] Build fail: implicit declaration of function 'Adc_ValidateQueueNotFull' in Adc.c<*> Detailed description (how to reproduce it): Build fail: implicit declaration of function 'Adc_ValidateQueueNotFull' in Adc.c Preconditions: Compiler gcc ADC_ENABLE_START_STOP_GROUP_API = OFF ADC_HW_TRIGGER_API = ON Test Case ID (internal TC that caught the defect) optional: Adc_TS_COT_010 cfg 4 Observed behavior: Generate step was passed but build step was failed Build fail log: STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc.c: In function 'Adc_ValidateExtraParams': STDERR:e:/S32K3/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/ Adc_TS_T40D34M9I0R0/src/Adc.c:1244:9: error: implicit declaration of function 'Adc_ValidateQueueNotFull'; did you mean 'Adc_ValidateStateNotIdle'? [- Werror=implicit-function-declaration] STDERR: 1244 Adc_ValidateQueueNotFull(&ValidationStatus, u8ServiceId, Group, u32CoreId); STDERR: STDERR: Adc_ValidateStateNotIdle More detail in attachment report Expected behavior: Build done Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7234	New	New Feature [S32K344 BETA] OCU: Implement CPR_RTD_00522 restrictions and updates in CPR_RTD_00511 on S32DS ,,"NewWorkDescription: Updates according to the updates in the requirement: *CPR_RTD_00511 CPR_RTD_00522*: Drivers capable of using Counter Buses shall not allow selection of an Counter Bus with exclusive access granted to PWM. The check will be performed at configuration time. Applicable only for Icu, Ocu, on eMIOS Requirement source: Customer Request

ID	Subtype	Headline and Description
		CPR_RTD_00511 (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Provide an API that will update (buffered change expected) the match/reload value for the counter selected."
ARTD-7237	Bug	[SPI]Struct "<unnamed>" has no field "pCmdDmaFast" ,,"The errors occurred in the case of SpiEnableDmaFastTransferSupport = true and SpiGlobalDmaEnable = false: 1. Struct ""<unnamed>"" has no field ""pCmdDmaFast"", ""rxDmaChannel"", ""txDmaChannel"". 2. Lpspi_Ip.c Function ""Lpspi_Ip_TxDmaTcdSGConfig"" was referenced but not defined static void Lpspi_Ip_TxDmaTcdSGConfig(uint8 u8Instance, uint8 u8TCDSGIndex, uint8 u8DisHwReq);
ARTD-7240	Bug	[S32K3XX] port: Cannot use pin PTC6 for Wakeup Input mode in DS<*> Open Icu_example_DS_eMios_Siul_Wkpu project, Configure pin PTC6 to Wakeup Input mode, Update code. Observed: Pin PTC6 was not generated and IBE was not enable in register. Propose: Update PTC6 as default value when enter Wakeup Input mode according to RM.
ARTD-7311	New	New Feature [gpt] Create CERT-C report and fix violations ,,"Create CERT-C report Fix all violations if any are found Guideline following: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]"
ARTD-7318	New	New Feature [crypto] Create CERT-C report and fix violations ,,"Create CERT-C report Fix all violations if any are found Guideline following: [https://confluence.sw.nxp.com/pages/viewpage.action?pageId=133734230]"
ARTD-7276	Bug	[crypto][S32DS][S32G]Missing component description for Gmac, Hse,Suil2_Dio, Suil2_Port in select component window ,,"Test Case ID (internal TC that caught the defect) optional: 1. Create project enable RTD for S32G274_Rev2 2. Open Peripherals tool-> Click to add component Observed behavior: Missing Component description for some components in Select component window:

ID	Subtype	Headline and Description
		Gmac, Hse,Suil2_Dio, Suil2_Port Expected behavior: There should have component description for these components: Gmac, Hse,Suil2_Dio, Suil2_Port
ARTD-7282	Bug	[S32K3xx][MCL] Failure at building on S32CT<*> Failure at building on S32CT, because Emios_Mcl_Ip_BOARD_InitPeripherals_PBcfg.c file included Emios_Mcl_Ip_PBcfg.h file, compiler cannot find this file !image-2021-02-03-10-50-27-006.png|thumbnail!
ARTD-7287	Bug	[S32K3XX][SENT][EXAMPLE] S32CT example not be display in S32DS project from Example box<*> Issue*: Can not find Sent example when create new project from example om S32DS Solution*: for each example, It needs to register to Base module, in this file: https://bitbucket.sw.nxp.com/projects/ARTD/repos/base/browse/specific/S32K3XX/integration/swm.rtd.s32k3.release_id.xml
ARTD-7284	Bug	[GPT][S32K3XX] Stm_Ip_u32InstanceState is undefined when set clock mode = OFF<*> I got build fail with STM as in attachment files, please help me check
ARTD-7332	Bug	[MCL] Store Destination Address overwrites Source Signed Last Address Adjustment<*> 1. At initialization, Store Destination Address overwrites the Source Signed Last Address Adjustment. 2. Update C termination "At the end of the CDD_MCL header file the ifdef cplusplus is missing and always needs to be added manually."
ARTD-7595	Bug	[SAI] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it): Error when generating project with SAI project: INFO 21-02-04,10:32:41 (11136) Project ""TestProject"" was created with different version of the tool. Migrating project. ERROR 21-02-04,10:32:47 (1803) Code generation (mode: ""generate"") Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration/SaiConfiguration_0/SaiTxRxConfiguration with config class PostBuild which is not allowed in this context ERROR 21-02-04,10:32:47 (13028) Code generation (mode: ""generate"") Project ""TestProject"" has errors, see Problems View ERROR 21-02-04,10:32:47 (1803) Code generation (mode: ""generate"") Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration"": (1822) Attempt to read value of

ID	Subtype	Headline and Description
		node /AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/SaiConfiguration/SaiConfiguration_0/SaiTxRxConfiguration with config class PostBuild which is not allowed in this context ERROR 21-02-04,10:32:47 (13028) Code generation (mode: ""generate"") Project ""TestProject"" has errors, see Problems View Unattended wizard ""Execute multiple tasks(GenerateAllVariants)(GenerateAllVariants)"" exited with errors. WARNING 21-02-04,10:32:41 (1648) Created required node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Sai/ELEMENTS/Sai/GeneralConfiguration/SaiEnableUserModeSupport"" in container ""/Sai/Sai/GeneralConfiguration""Errors ""4"" Warnings ""1"" Makefile:658: recipe for target `/cygdrive/d/zebra/repo_s32k3/output/S32K3XX_S32K344/sai/Sai_TS_WIR_001_cfgCORE0/generate_tresos/generate_timestamp' failed make: [/cygdrive/d/zebra/repo_s32k3/output/S32K3XX_S32K344/sai/Sai_TS_WIR_001_cfgCORE0/generate_tresos/generate_timestamp] Error 1 !image-2021-02-04-11-09-19-670.png! Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Observed behavior: Generate project failed Expected behavior: Generate project successfully Proposed solution optional: Refer the fix from ARTD-6494
ARTD-7598	Bug	[GPT] Code generation error "config class PostBuild which is not allowed in this context" ,,"Invalid XPath-expression for Attribute ""INVALID"" of node ""ASPath:/Gpt/Gpt/GptChannelConfigSet/GptChannelConfiguration_0/GptWakeupConfiguration"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptChannelConfiguration/GptChannelConfiguration_0/GptEnableWakeup with config class PostBuild which is not allowed in this context
ARTD-7606	Bug	[platform]The platform driver build faild when system interrupt not initialized<*> The platform driver build faild when system interrupt not initialized !image-2021-02-04-18-19-53-026.png!
ARTD-7607	Bug	[ETH]Fix generate failed when Config Time enabled<*> When config time enabled, some nodes are precompile but refer to post build node will generate failed.
ARTD-7612	New	New Feature [CRYPTO]Update code to follow HSE_IP_014_001 requirement ,,"HSE_IP_014_001 states the following: ""The type Hse_Ip_StatusType shall be an enumeration that describes the status of the execution of the Hse Ip driver's APIs"".

ID	Subtype	Headline and Description
		The IP implementation is done using _status_hse_ip_t structure instead of _Hse_Ip_StatusType_. Additionally the enum values can be updated: `STATUS_HSE_IP_SUCCESS` to `HSE_IP_STATUS_SUCCESS` `STATUS_HSE_IP_ERROR` to `HSE_IP_STATUS_ERROR`"
ARTD-7613	New	 New Feature [ADC] Add configurable resolution ,,"Add configurable resolution: CALBISTREG->RESN Add in IPL and HLD configurators at group level Mask accordingly the read result operations Validate feature by checking if converted value for bandgap is correct for all supported resolutions (not required to add dev test) Add requirement for new IPL function"
ARTD-7631	Bug	 [ADC] Multicore should not be supported on S32K344 and S32K314 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] Multicore on S32K314 and S32K344 derivative should be not supported, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: Resource configured as S32K314 or S32K344 derivative Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore should be not supported on S32K314 and S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7633	Bug	 [BASE][OSIF] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: [...] Observed behavior: Multicore is enable for all derivative

ID	Subtype	Headline and Description
		Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-7622	Bug	[S32K3XX][S32XX][GPT] Missing UM/IM path in the <Mdl>.mak file<*> Missing user manuals doc path in the <Module>.mak file SRC_FILES = $(MODULE_PATH)/specific/$(S32K3XX_NAME)/doc/user_manuals/RTD_GPT_IM.pdf@outdir=doc,bin=y \ $(MODULE_PATH)/specific/$(S32K3XX_NAME)/doc/user_manuals/RTD_GPT_UM.pdf@outdir=doc,bin=y
ARTD-7626	Bug	[S32K3xx][MCL] Generate file is missing some variables<*> I see that generate file form S32CT is missing some variables(Pls see as below) !image-2021-02-05-12-40-26-548.png|thumbnail! Redundant config variant in configTimeSupport. I think it is not necessary at IP layer !screenshot-1.png|thumbnail!
ARTD-7647	Bug	[platform][S32DS]The platform driver build faild when system interrupt not initialized<*> The platform driver build faild when system interrupt not initialized !image-2021-02-04-18-19-53-026.png!
ARTD-7671	New	New Feature [GPT] S32K344 is selected on Tresos/CT, the multicore feature should be disabled" ,,"Please see the topic below : [Vlad Lionte: K344 single core |https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] posted in Zebra / 00. S32K3XX_BETA_0.9.0 (S32K3) at Feb 4, 2021 5:50 PM In the conclusion, when the chip K344 is selected on Tresos/CT, the multicore feature should be disabled in these tools For multicore testing, we should use the support for K324, tested on a K344 with lockstep disabled. P/s: Please check carefully if the multicore nodes were disabled but the value are still true. In this case, seems that the multicore can be run anyway.
ARTD-7675	Bug	[S32K3XX][CRYPTO] Missing array store value actual length of the key element has ID is 1 on array Crypto_au8VolatileKeyElemValues<*> Detailed description* (how to reproduce it): Problem when generate config file with S32DS,when config a Kelement have Id is 1 and referent it to RamKeyCatalog, but when generate array Crypto_au8VolatileKeyElemValues on file Crypto_Cfg.c don't have value of actual length of the key element has ID is 1. Observed behavior*: Missing array store value actual length of the key element has ID is 1 on array Crypto_au8VolatileKeyElemValues Expected behavior:

ID	Subtype	Headline and Description
		if(KeyElement.getChildById("UseHseKey").getValue() == true && KeyElement.getChildById("HseKeyCatalogGroupRef").*getValue()*.contains*("/RamKeyCatalog/*")) should be change : " else if(KeyElement.getChildById("UseHseKey").getValue() == true && deref*(KeyElement.getChildById("HseKeyCatalogGroupRef")).*getId()*.contains("*RamKeyCatalog*")
ARTD-7678	New	New Feature [ADC] Hw Triggered Mode DMA with streaming, without interrupts and group streaming results reorder" ,,"DMA without interrupts, with streaming and with group streaming results reorder: after each group conversion is finished transfer results using SG in an internal buffer use counting DMA channel to copy from this internal buffer into buffer setup via Adc_SetupResultBuffer counting DMA channel must be configurable in ct and hld when ADC is configured for DMA, without interrupt and streaming Group streaming results reorder is required to allow using a single DMA channel without SG for transfering results into the result buffer. Otherwise, a single DMA without SG cannot move result from internal buffer into a circular result buffer arranged as per Autosar requirement: internal buffer Ch0,Ch1,Ch2 > result buffer Ch0,Ch0,Ch0;Ch1,Ch1,Ch1;Ch2,Ch2,Ch2 (because cannot be solved with DMA modulo feature, or minor loop destination/source offset would be required to support different values for destination and source) But this can be achieved: Ch0,Ch1,Ch2 > result buffer Ch0,Ch1,Ch2;Ch0,Ch1,Ch2;Ch0,Ch1,Ch2 Other updates: same implementation to be used also for double buffering optimization
ARTD-7684	Bug	[Wdg] cmm filename is wrong in example readme.txt<*> cmm filename is wrong in example readme.txt Please correct it, also check for other wrong information in example readme
ARTD-7695	New	New Feature [SPI][FLEXIO] Add support for FLEXIO common ,,"Add Mcl common code and configurator for FLEXIO IP to be used by drivers: PWM, I2C, LIN, UART, SENT, SPI See links of ticket for start-up."
ARTD-7706	New	New Feature [S32K3XX][PWM][FLEXIO] PWM over FLEXIO: EBT support ,,"EBT 3-7d xdm user interface generation templates vsmd check only check existing example to not have issues Resource files to be used on EBT and DS as well. 1d "
ARTD-7707	Bug	[ARTD] _end symbol not properly defined for heap memory section<*> The heap section is not properly defined in linker file (linker_ram.ld) and the allocation of dynamic memory will fail. The '_end' symbol need to be inside the heap section.

ID	Subtype	Headline and Description
		Steps: # create a Design Studio 3.4 project # Allocate memory using malloc (void p = (void)malloc(79);) immediately after the beginning of main() # Observe that it will jump into Hard_Fault (screenshots attached) Possible fix solution (I attached my new linker file): move the '_end symbol inside the heap section
ARTD-7708	New	New Feature [S32K3XX][PWM][FLEXIO] PWM over FLEXIO: DS configuration ,,"DS 3-5d component user interface generation templates and manifest updates/addition epd/epc compliance check only check existing example to not have issues Resource files to be used on EBT and DS as well. 1d"
ARTD-7709	New	New Feature [S32K3XX][PWM][FLEXIO] PWM over FLEXIO: Static code create/add ,,"Requirements definition in separate xls file 1d IPL static code create/update/review 5d Update plugin makefile IPW code update/review 1d Dev test create/update to contain FLEXIO channels 1d Review xls of requirements for DOORS upload 1d Design update for flexio requirements Sharing strategy and implementation into MCL "
ARTD-7714	Bug	[S32K3] Lin and Uart can't be used in the same application<*> It both Lpuart_Uart and Lpuart_Lin components are used in an application, the build will fail due to redeclarations of enums. Starting from the Lpuart_Lin_Example, which uses LPUART_IP_0 as the Lin Hardware Channel, we also added a Lpuart_Uart component. This component configures LPUART_1 as the UartHwChannel, therefore a different instance of the peripheral. The build of the application fails as some enumerators are declared both in the Lpuart_Uart_Ip_HwAccess and inside the Lpuart_Lin_Ip_Hw_Access header files. A screenshot of the S32 Design Studio build console is attached.
ARTD-7722	New	New Feature [S32K3XX][PWM][EMIOS] Add Exclusive Areas for Emios IPL ,,Exclusive Areas must be added in the Emios IPL.
ARTD-7737	Bug	[ICU] Code generation error "config class PostBuild which is not allowed in this context" ,,"Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		For GPT I received this ticket I think you should check in your driver too. GPT's issue: GPT has consistent error when using Post Build Variants (even with generic XDM). GPT module complains that PostBuild is not allowed in this context, but there is no post build configuration set up here. I have verified that there is no post build variants in the GPT.xdm file. Error message: Invalid XPath-expression for Attribute ""INVALID"" of node ""/AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels"": (1822) Attempt to read value of node /AUTOSAR/TOP-LEVEL-PACKAGES/Gpt/ELEMENTS/Gpt/GptChannelConfigSet/GptPit/GptPit_Ecu_Sync_Timer_Device/GptPitChannels/GptPitChannel_0/GptPitChannel with config class PostBuild which is not allowed in this context It seems the error is reported because the configuration parameter of config class precompile is referencing in INVALID tag a parameter which is postbuild. As a workaround the checkbox ""Enable Config Time support"" in properties of Tresos project can be disabled. !image-2021-01-20-10-21-42-289.png|width=564,height=385! Preconditions: Checkbox "Enable Config Time support" is enabled in properties of Tresos project. Observed behavior: Code generation error. Expected behavior: No code generation error. Proposed solution*: Modify the configuration class of configuration parameter in xdm file so that both parameters are of the same configuration class.
ARTD-7754	Bug	[S32K3][SENT] Flexio channel needs to be assigned follow by HW channel from configuration<*> Issue: Currently, Flexio channels were allocated automatically in SENT module. Driver will allocate Flexio channel to which one is free. > This implementation is incorrect. It needs to follow HW channel from configuration.
ARTD-7757	Bug	[S32K344][LIN] Driver can't receive data to buffer in case receive response<*> Driver can't receive data to buffer in case receive response. I predicted DATA register might be read 2 time continuous makes value in data buffer receive equal = 0. First time read in function Lpuart_Lin_Ip_FrameIrqHandler line 1928 make value in DATA register return 0 then second time in function Lpuart_Lin_Ip_GetBytetoBuffer called by function Lpuart_Lin_Ip_ProcessReceiveFrameData.
ARTD-7758	Bug	[S32K344][LIN] Driver need check case fail when config node Multicore support = ON and resource different S32K324<*> Driver need check case fail when config node Multicore support = ON and resource different S32K324. Check topic: [Vlad Lionte: K344 single core |https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-

ID	Subtype	Headline and Description
		ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] posted in Zebra / 00. S32K3XX_BETA_0.9.0 (S32K3) at Feb 4, 2021 5:50 PM
ARTD-7761	New	 New Feature [ICU] [S32XX]][S32CT] Implement EPD/EPC support for HLD and IPLD ,,"<this is a follow up for solving build errors and re-check the epd epc script on CC platform> Implement EPD/EPC support for HLD and IPLD. Please refer to [this post on Teams https://teams.microsoft.com/l/message/19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2/1606904026692?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1606904026692&teamName=Zebra&channelName=Configuration%20(code%2C%20DS%2C%20EB%2C%20etc)&createdTime=1606904026692] for additional details. From the presentation, the main focus should be on the following sections: Mapping XDM to Component EPD Importer EPD Generation EPC Importer EPC Generation"
ARTD-7783	Bug	 [S32K3][SENT] Multicore supports on S32K324 only<*> Since S32K3 has derivative S32K324 support multicore, S32K314 and S32K344 do not have multicore. Therefore, driver need to update in order to enable multicore support on S32K324 only, other ones need to disable. (S32K344 and S32K314)
ARTD-7777	Bug	 [ICU] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] [Multicore is disabled on S32K344|https://teams.microsoft.com/l/message/19:b5f29bf74fdc497491f31257ffdf916c@thread.tacv2/1612491947574?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=0c20671d-eae6-4fd5-8fd2-7cc683861979&parentMessageId=1605838003935&teamName=FPT%20Zebra%20Team&channelName=General&createdTime=1612491947574] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ID	Subtype	Headline and Description
		Proposed solution optional:
ARTD-7778	Bug	[PWM] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] [Multicore is disabled on S32K344|https://teams.microsoft.com/l/message/19:b5f29bf74fdc497491f31257ffdf916c@thread.tacv2/1612491947574?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=0c20671d-eae6-4fd5-8fd2-7cc683861979&parentMessageId=1605838003935&teamName=FPT%20Zebra%20Team&channelName=General&createdTime=1612491947574] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-7779	Bug	[OCU] Multicore should be disabled on S32K344 derivative<*> Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] [Multicore is disabled on S32K344|https://teams.microsoft.com/l/message/19:b5f29bf74fdc497491f31257ffdf916c@thread.tacv2/1612491947574?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=0c20671d-eae6-4fd5-8fd2-7cc683861979&parentMessageId=1605838003935&teamName=FPT%20Zebra%20Team&channelName=General&createdTime=1612491947574] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-7780	Bug	[GPT] Multicore should be disabled on S32K344 and S32K314 derivative<*>

ID	Subtype	Headline and Description
		Detailed description (how to reproduce it): As new information (click the links for more information) [Single core on S32K344|https://teams.microsoft.com/l/message/19:0bd08d52409848849e868ba689b329c0@thread.tacv2/1612435813929?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&groupId=f9decd68-7b74-4101-a4d2-ad54e86f727f&parentMessageId=1612435813929&teamName=Zebra&channelName=00.%20S32K3XX_BETA_0.9.0%20(S32K3)&createdTime=1612435813929] Multicore on S32K344 derivative is disabled, so driver should update follow this. Multicore is only available on S32K324 derivative Preconditions: NA Observed behavior: Multicore is enable for all derivative Expected behavior: Multicore is disabled on S32K344, only available on S32K324 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-7792	Bug	[S32K3][SENT] Remove instance parameter from polling functions<*> The parameter 'instance' needs to be remove from the following HLD functions, since these functions will poll all the channels available: Std_ReturnType Sent_GetFastMsgData(uint8 instance) Std_ReturnType Sent_GetSerialMsgData(uint8 instance)
ARTD-7795	Bug	[S32K3xx][EMIOS] Some functions in high layer should check coreID<*> Mcl_Emios_SetReloadInterval and Mcl_SetEmiosCounterBusPeriod functions should check for coreID before writing to register, because EB tresos is configuring that each instance will refer to Ecuc partition Ref. If condition is not met then the function will raise a DET error. !image-2021-02-18-17-27-35-072.png|thumbnail! Similar to IRQ in Emios_Mcl_Ip_Irq file
ARTD-7794	Bug	[platform][S32DS]The platform driver build faild when system interrupt not initialized<*> The platform driver build faild when system interrupt not initialized !image-2021-02-04-18-19-53-026.png!
ARTD-7807	Bug	[S32K3XX] Icu: Number of instance is not correct<*> Step to reproduce: 1: Create a project on S32DS 2: Add cmp module at IP level 3: Edit the field of IcuLpCmp > ICU CMP IP instance number => add value 3 but have no error here, Meanwhile max of instance of S32K344 is 2(0, 1, 2)
ARTD-7811	Bug	[ICU] WKPU_IP_64_CH_USED does not define for S32K3XX<*> S32K3XX have 64 channels for WKPU but WKPU_IP_64_CH_USED does not define for S32K3XX
ARTD-7812	Bug	

ID	Subtype	Headline and Description
		[S32K3] Lin and Uart can't be used in the same application<*> It both Lpuart_Uart and Lpuart_Lin components are used in an application, the build will fail due to redeclarations of enums. Starting from the Lpuart_Lin_Example, which uses LPUART_IP_0 as the Lin Hardware Channel, we also added a Lpuart_Uart component. This component configures LPUART_1 as the UartHwChannel, therefore a different instance of the peripheral. The build of the application fails as some enumerators are declared both in the Lpuart_Uart_Ip_HwAccess and inside the Lpuart_Lin_Ip_Hw_Access header files. A screenshot of the S32 Design Studio build console is attached.
ARTD-7818	Bug	[S32K3][ICU] The EMIOS_ICU component in RTD0.8.1 cannot work correctly.<*> The configuration variables generated by CT are totally different from their definitions in Emios_Icu_Ip_Types.h_, including spelling mistakes. Besides, there are AutoSar version error, vendor error and Software version error in Emios_Icu_Ip.h_ and the _Icu_Types.h is missing. For more information see attachments.
ARTD-7856	Bug	[WDG] Plugin contains xdm file duplicated in EBT folder<*> Plugin contains xdm file duplicated in EBT folder Check also for other differences in plugin ouput folders/files vs another driver (e.g. eth)
ARTD-7858	Bug	[SAI] Det_ReportRuntimeError is guarded by SAI_DEV_ERROR_DETECT<*> Det_ReportRuntimeError in Sai_SyncTransmit is guarded by #if(SAI_DEV_ERROR_DETECT == STD_ON) Also Sai_ValidateCore (added for 0.9.0 release) is used only when (SAI_DEV_ERROR_DETECT == STD_ON), so function definition must also be guarded
ARTD-7869	Bug	[ETH][S32T] The multicore should not be supported for IPL<*> The multicore should not be supported at IPL on S32CT when only the IPL was used for the project.
ARTD-7871	New	New Feature [LIN][LPUART] - Add a check in configuration for the Hw instance ,,Add a check in EBT and CT for LIN and UART components over LPUART which will signal a duplicated hw instance usage.
ARTD-7874	Bug	[SAI] Driver always busy in receiver mode when setting both transmitter and receiver<*> Detailed description (how to reproduce it): Driver always busy in receiver mode when setting both transmitter and receiver in EB SAI configuration, create 2 configuration, one for transmitter and one for receiver, both of them is master, interrupt, async mode. Init driver and start receiving data Call Sai_AsyncTransmit with receiver request wait until the driver status is completed => driver status is always busy Preconditions: [...]

ID	Subtype	Headline and Description
		Observed behavior: Can not receive data successfully Expected behavior: Receive data successfully Proposed solution optional:
ARTD-7877	Bug	Missing define in generated file triggers compilation error<*> GPT_START_SEC_CONST_UNSPECIFIED is not defined in generated file Gpt_BOARD_InitPeripherals_PBcfg.c RTD version used: PlatformSDK_S32K3_2021_03 !image-2021-02-22-17-57-33-704.png|thumbnail!
ARTD-7882	Bug	[ETH][S32CT] The multicore should be supported for ETH HLD on S32K324<*> On S32CT, the ETH module (HLD) should support Multicore feature on S32K324. Steps to reproduce: # Create a S32DS application project with S32K324 # Add Eth module (HLD) # Enable Multicore support for ETH module Observed behavior: When EthMulticoreSupport check box is selected, the Problems view shows: "This derivative doesn't support multicore" Expected behavior: There is not any error when EthMulticoreSupport check box is selected.
ARTD-7887	Bug	[S32K3XX][MCL] Cannot initialize EMIOS with Ecuc Partition ref is core 1<*> Sequence of test case: Initialize EMIOS module (core 0 with EMIOS instance 0 and core 1 with EMIOS instance 1) on core 0 Delay a period of time for the IRQ to occur Get ISR trigger Multicore of MCL module is type 3(Initialization is performed on a single, designated core), but I see that in driver code, condition at line 96(if (configCore == CoreId) of Emios_Mcl_Ip.c file cannot be satisfied.
ARTD-7888	Bug	[ETH][K3XX] Error when config Shaper<*> There is an error when configure Eth Shaper. Please check the attached screen-shot.
ARTD-7894	Bug	[ADC] Function Adc_Sar_Ip_SetExternalTrigger calling in Adc_Ipw_EnableCtuTrigger is redundant<*> Detailed description (how to reproduce it): Function Adc_Sar_Ip_SetExternalTrigger calling in Adc_Ipw_EnableCtuTrigger is redundant Preconditions: AdcEnableCtuTrigAutosarExtApi is enable Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_0120 Observed behavior: Trigger sources passing to Adc_EnableCtuTrigger are always different from EXT_TRIG so Adc_Sar_Ip_SetExternalTrigger calling in Adc_Ipw_EnableCtuTrigger is redundant More detail in attachment report

ID	Subtype	Headline and Description
		Expected behavior: No need to call this function Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7917	Bug	[S32K3XX][Dio][S32CT] The Multicore did not raise any error when the chip K314, K344 is selected ,,"Detailed description (how to reproduce it): 1. Creating project for S32DS (derivative S32K344 or S32K314) 2. Open Peripheral 3. Import .mex file with <setting name=""DioMulticoreSupport"" value=""true""/> (attach Dio_multicore_support.mex for S32K344) 4. Update code Test Case ID (internal TC that caught the defect):* NA Observed behavior:*_ generate code successfully, no Error Expected behavior: error occurred in ""Problem"" box or generate fail because multicore enable
ARTD-7953	Bug	[ADC] CT ADC_SAR_IP missing the generated struct for ADC_SAR_1<*> Detailed description (how to reproduce it): In CT, create the configuration for ADC0 and ADC1 then generate code => Missing the struct configuration for Adc_sar_1 !image-2021-02-26-15-37-57-027.png! Test Case ID (internal TC that caught the defect) optional: Adc_sar_TC_FCT_0001 Observed behavior: Missing the struct configuration for Adc_sar_1 Expected behavior: Can generate the struct configuration for Adc_sar_1 Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-7957	New	New Feature [SPI][FLEXIO] Update CT for FLEXIO following new approach ,,Update CT for FLEXIO following new approach
ARTD-7968	New	New Feature [RTD][LIN] Mark some requirements as External requirement ,,"NewWorkDescription: There is a standard requirements of LIN which need to be marked as External requirements because it was done by BASE module. !image-2021-02-26-20-34-40-367.png! Requirement source:

ID	Subtype	Headline and Description
		ASR SWS (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: [...]"
ARTD-7971	New	 New Feature [S32K3XX][PWM] Integrate FLEXIO IPL in PWM ASR Driver ,,"IPW code update/review 1d Dev test create/update to contain FLEXIO channels 1d Sharing strategy and implementation into MCL Update IPL Flexio to use MCL driver."
ARTD-7994	Bug	 [CRYPTO] Function Crypto_Hse_Init always return E_OK<*> Detailed description (how to reproduce it): Function Crypto_Hse_Init always return E_OK.It ,must return E_NOT_OK when Hse_Ip_Init() != HSE_IP_STATUS_SUCCESS Observed behavior: Missing return E_NOT_OK when Hse_Ip_Init() != HSE_IP_STATUS_SUCCESS Expected behavior: Add return E_NOT_OK when Hse_Ip_Init() != HSE_IP_STATUS_SUCCESS
ARTD-8034	Bug	 [S32K344] [PORT] Issue in INMUX when implement Virtual Wrapper feature<*> Detailed description (how to reproduce it): when delare Port_Init, the pin with config INPUT mode, turn on Virtual Wrapper, core 1 (PDAC1), the hard fault occur in step Write to Input Multiplexed Signal Configuration Register (IMCR) Test Case ID (internal TC that caught the defect): Port_TC_FCT_2001 Observed behavior:* !image-2021-03-02-18-02-23-244.png|width=1185,height=226!! image-2021-03-02-18-04-39-923.png! Expected behavior:* resolve hard fault in Port_Init
ARTD-8065	Bug	 [Platform][S32K3xx_090] Platform_SystemIrqConfigType struct missing when config two McmConfig on S32CT<*> Detailed description (how to reproduce it): # Create new project with resource s32k324 # Enable multi core # Enable system setting with two instance Partition_0 and Partition_1 # Generate code # Checking Platform_Ipw_Cfg.c missing Platform_SystemIrqConfigType struct for Partition_1 Test Case ID (internal TC that caught the defect):* Platform_TS_MUL_002 Observed behavior:* Missing Platform_SystemIrqConfigType struct for Partition_1 when add some instance !image-2021-03-03-10-29-26-142.png! Expected behavior:* Add Platform_SystemIrqConfigType for Partition_1.
ARTD-8085	Bug	 [SPI] SPI DMA notification function is not called by DMA interrupt in DMA fast transfer mode<*>

ID	Subtype	Headline and Description
		In DMA transfer fast mode, driver is configurated using sequence of DMA ScatterGather TCD. There is one fail case: To support to transfer a Spi SEQUENCE has number of Channels <= 3. The sequence of ScatterGather is configured for SpiPhyRxDmaChannel in MCL: TCDScatterGather0->TCDScatterGather1->TCDScatterGather2. TCDScatterGather0: ESG=1, DREQ=0, INTMAJOR=0 TCDScatterGather1: ESG=1, DREQ=1, INTMAJOR=1 TCDScatterGather2: ESG=0, DREQ=1, INTMAJOR=0 If the SEQUENCE has 2 Channels is used for transferring then Spi Dma notification function is not called by MCL. Because TCDScatterGather2 is loaded immediately by HW after TCDScatterGather1 Done. So INTMAJOR will be set back to 0. So, when CPU jump to DMA interrupt function, MCL understood it is spurious interrupt(Done flag = 1 but INTMAJOR = 0). This will lead to SPI Dma notification is not called after that.
ARTD-8082	Bug	[GPT] Pit_Ip_SetCounterValue sets the period of timer one tick more<*> Detailed description (how to reproduce it): We are using PIT timer to generate periodic interrupt and we need to set the period of the interrupt exactly 50ms. The PIT timer is clocked by 60MHz so the period in ticks is 50e-3/(1/60e6) = 3000000 = 0x2dc6c0. Then we call the function to start the timer with this period: Pit_Ip_SetCounterValue(uint8 instance, uint8 channel, uint32 countValue); The interrupt is generated periodically after 0x2dc6c0+1 ticks which is not correct (the period is one clock tick more than expected). As per reference manual the value written to PIT LDVAL register shall be computed as follows (with minus 1): LDVAL trigger = (period / clock period) 1 Preconditions: PIT timer used Test Case ID (internal TC that caught the defect) optional: Ip_Pit_TC_003 Observed behavior: Wrong period set by Pit_Ip_SetCounterValue() Expected behavior: Correct period is set by Pit_Ip_SetCounterValue() Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: The PIT LDVAL register must be written with period 1 to generate correctly the period (timeout). So the value passed to Gpt_StartTimer() shall be decremented by 1 before writing to LDVAL register.
ARTD-8131	Bug	S32_CT cannot generate both Tx and Rx configuration for the same SAI instance<*> S32K344 SAI0 is used to connect with audio codec sgtl5000 via I2S mode. Thus we need to configurate SAI0 Tx and Rx param both, via the Configuration Tools. There is a "Hardware Unit" Param in the Sai component Configuration Array, which indicates the SAI instance. However, each SAI instance can only appear once in each configuration array. That means, if I configure SAI_0 for Rx, then I can't add another configuration for SAI_0 anymore, even though SAI_0 Tx should be accepted to configure meanwhile. It is interested that the "Hardware Unit", which the SAI instance, actually not generated in the Param structure after Update Code, so I can select SAI_1 temporarily for Tx configuration. But if I do, the SAI_1 instance configuration can not be added.

ID	Subtype	Headline and Description
ARTD-8207	Bug	[ADC] Compilation error when using DMA without results reorder or dma stream optimization<*> The following compilation error occurs on Dev Test Suites 007 and 008: c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c: In function 'Adc_Ipw_StartDmaOperation': c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:1012:49: error: 'u32AdcCountingDmaLogicChId' undeclared (first use in this function); did you mean 'u32AdcDmaLogicChId'? 1012 LocTransferList[13].Value = u32AdcCountingDmaLogicChId; u32AdcDmaLogicChId c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:1012:49: note: each undeclared identifier is reported only once for each function it appears in c:/Users/nxf47222/Documents/artd-repo/output/S32K3XX_S32K344_gcc/adc/../../eclipse/plugins/Adc_TS_T40D34M9I0R0/src/Adc_Ipw.c:1031:13: error: 'CountingDmaLocTransferList' undeclared (first use in this function) 1031 CountingDmaLocTransferList[0].Param = DMA_IP_CH_SET_SOURCE_ADDRESS;
ARTD-8218	Bug	SAI component can't generate the Bit Clock correctly when use External Master Clock.<*> When use S32DS 3.4 Configuration Tool to configure the SAI component of S32K3xx RTD version 0.9.0, if we choose Master Clock Source as EXTERNAL_CLKi1/4OEthen the Sai Sample Rate can not be edit anymore, however, the SAI driver only calculate the Clock Divider for Internal Master Clock, therefore, the SAI BCLK and Frame Sync are not works as our expected frequency.
ARTD-8219	Bug	[S32K3][CLOCK] Correct the number of elements generated when the under MCU control node is false<*> The number of elements generated is wrong when the under MCU control node is false
ARTD-8221	Bug	[GPT] Update Example DS/EB<*> Update example Add example HLD on DS Update MCU on EB
ARTD-8224	Bug	[DIO]The address of MPGPDO works incorrectly<*> The address calculation of MPGPDO register works incorrectly when it is MPGPDO1->MPGPDOmax Expected behaviour: The address calculation of MPGPDO register will work correctly Step: Update the address calculation of MPGPDO
ARTD-8228	Bug	[S32K3-LIN] Wakeup feature issue with Flexio IP<*> LIN doesn't wake up when MAF sends wakeup signal
ARTD-8237	Bug	

ID	Subtype	Headline and Description
		[S32K3][SENT] SENT refers to wrong DMA channel from MCL<*> CDD_Sent.component needs update as bellow: <dynamic_enum id="SentDmaChannelRef_t" label="Sent Dma Channel Reference name" items="system::makeRefs(system::getChildrenByASPath(`/AUTOSAR/EcucDefs/Mcl/MclConfig/dmaLogicChannel_Type`))"> <description><![CDATA[EN:<html>Reference to the DMA Channel configure for the Request. </html>]]></description> </dynamic_enum>
ARTD-8270	Bug	[PWM][S32K3XX] Update Pwm_SyncUpdate API for taking into account multiple channels<*> Implement SyncUpdate functionality to be able to apply the settings for multiple channels from same instance. Please also consider the corner cases that were identified on former MCAL and AMNG implementations. See Pwm_eMios_SyncUpdate in that codebase. !image-2021-03-05-18-54-41-572.png|width=381,height=170!
ARTD-8276	Bug	s32k3 RTD SDK SIUL2 ICU issue<*> When configuring SIUL2 ICU module in s32ds configuration tool, the callback function name always reports with error: "Name must be a valid C identifier." See attached figure. Please provide a workaround.
ARTD-8279	Bug	[SAI] Incorrect name of variable types as coding guideline<*> We has met some issues, when they define NO_STDINT_H: Nomal test, Example, Compile only d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h: In function 'Sai_Ip_IsTxChannelEnabled': d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h:117:16: error: 'true' undeclared (first use in this function) 117 bRet = true; d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h:117:16: note: each undeclared identifier is reported only once for each function it appears in d:\s32_zebra\repo_k3xx_beta\output\eclipse\plugins\sai_ts_t40d34m9i0r0\src \Sai_Ip_HwAccess.h:121:16: error: 'false' undeclared (first use in this function) 121|bRet = false; As our coding guideline, I supposed *NULL_PTR*, *boolean* and *TRUE* should be used, instead of *NULL*, *bool* and *true
ARTD-8280	Bug	[WDG] Incorrect name of variable types as coding guideline<*> Detailed description (how to reproduce it): Now, driver code has some errors about coding rules when define CCOPT+=-DNO_STDINT_H Build error log: "d:/Zebra/S32K3XX_BETA/output/S32K3XX_S32K344_ghs/wdg/../../eclipse/plugins/Wdg_TS_T40D34M9I0R0/src/Swt_Ip.c", line 411: error #20: identifier "NULL" is undefined DevAssert(Swt_Ip_pConfig != NULL);

ID	Subtype	Headline and Description
		"d:/Zebra/S32K3XX_BETA/output/S32K3XX_S32K344_ghs/wdg/../../eclipse/plugins/Wdg_TS_T40D34M9I0R0/src/Swt_Ip.c", line 538: error #20: identifier "NULL" is undefined DevAssert(Swt_Ip_pConfig != NULL); Preconditions: [...] Observed behavior: Incorrect name of variable types as coding guideline Expected behavior: Correct name of variable types as coding guideline Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-8273	New	 New Feature [Platform]Fix some warning errors ,,"Detailed description (how to reproduce it): # Build test platform on station # check compilerwarning # dowload RTD_S32K3XX_Compiler_Warnings and check log file Test Case ID (internal TC that caught the defect):* N/A Observed behavior:* still some warning errors in the [MISRA Reports XLSX|https://bamboo1.sw.nxp.com/browse/ARTD-CIP136-6/artifact/BUILDCOV/MISRA-Reports-XLSX/] Expected behavior:* fix all warning errors"
ARTD-8294	Bug	 [S32K3XX][PORT] Build fail when add -DNO_STDINT_H in makefile<*> Detailed description (how to reproduce it): When add CCOPT+=-DNO_STDINT_H we can not build test due to in Siul2_Port_Ip.c did not define NULL Test Case ID (internal TC that caught the defect): IP_Port_Siul2_TC_0001 Observed behavior:* !image-2021-03-08-15-35-14-211.png! Expected behavior:* can build successfully, we must use NULL_PTR instead of NULL
ARTD-8286	Bug	 [S32K344][LIN] Function Lpuart_Lin_Ip_GetReceiveStatus return value pBytesRemaining incorrect.<*> Function Lpuart_Lin_Ip_GetReceiveStatus return value pBytesRemaining incorrect. After receiver response OK, Lpuart_Lin_Ip_GetReceiveStatus still return value pBytesRemaining equal 1.
ARTD-8299	Bug	 [S32K3][MCU] Hardfault error when call Mcu_InitClock on Sent_example_DS<*> Issue In function Mcu_InitClock, I got hardfalut error when execute NOT_UNDER_MCU_CONTROL_A with clkState[PLL_CLK]: !image-2021-03-08-16-26-39-356.png|thumbnail!
ARTD-8303	Bug	 [CRYPTO] Compiler warnings<*> Detailed description (how to reproduce it):

ID	Subtype	Headline and Description
		Compiler warning report have waring on GCC sheet (attached file below) link station: http://somov.ea.freescale.net/2/project/custom_compilerwarning/details Test Case ID (internal TC that caught the defect)*: N/A Observed behavior: C:/vv_tools/eb/EB_tresos_Studio_27.1.0_b200625-0900_06/plugins/Crypto_TS_T40D34M9I0R0/include/Crypto_ASRExtension.h 130 "CRYPTO_ENABLE_TLS12_DERIVE_SUPPORT" is not defined, evaluates to 0 [-Wundef]@56 130 #if (STD_ON == CRYPTO_ENABLE_TLS12_DERIVE_SUPPORT) Expected behavior: No warning in compiler warning report
ARTD-8308	Bug	[S32XX][S32K3XX] Crypto: CT configuration does not check Max value of key slot and same key ID<*> Detailed description (how to reproduce it): # Can configure the maximum number of key slot for a groups key catalog is 256 but each group key have specific value maximum # When configure CryptoKelement for CryptoKeyType , user can configure 2 key same ID , need add condition a CryptoKeyTyppe doesn't configure 2 keyelement same ID Expected behavior: # Add check the maximum allowed number of configured groups in both Nvm and Ram key catalogs # Add check a CryptoKeyElement with the same CryptoKeyElementId already exists in the reference list when configure CryptoKelement for CryptoKeyType

ARTD-8309	Bug	[S32K3][MCL][Design] Redesign requirement CPR_RTD_00511.mcl<*>
		
		Change of period should be supported for an active/initialized eMIOS counter bus assigned exclusively to PWM.
		The MCL driver shall provide an API for updating the period at run time for eMIOS counter bus channels exclusively assigned to PWM.
		The API name shall be:
		void Mcl_eMiosSetCounterBusPeriod(CounterBus, Period, SyncUpdate);
		The implementation should validate the API parameters channel range and period range.
		Per default this optional API and functionality shall be disabled.
		Drivers capable of using Counter Buses shall check on configuration time and not allow selection of an Counter Bus with exclusive access granted to PWM.
		
		Note:
		The runtime flow for sync update will be:
		
		void Mcl_eMiosSetCounterBusPeriod(CounterBus, Period, SyncUpdate=TRUE);
		clear OUDIS with specific MCL API;

ARTD-8328	Bug	[SAI] Can not continue receiving data after DMA receiver error<*> Detailed description (how to reproduce it): Can not continue receiving data after DMA receiver error Prepare SAI receiver buffer data, declare as const to make driver can not write to buffer data and generate DMA error event Setup MAF to send data Setup SAI is master, receiver mode Call Sai_AsyncTransmit and wait until the driver status is not BUSY Verification Point: Driver returns SAI_STATUS_ERROR Repeat step to setup MAF and SAI driver

ID	Subtype	Headline and Description
		Verification Point: Driver returns SAI_STATUS_COMPLETED => FAIL{color}*, driver stucks in Dev_assert function. !SAI_DMA_ERROR.png! Preconditions: [...] Observed behavior: Can not receive data successfully Expected behavior: Receive data successfully Proposed solution optional:
ARTD-8331	Bug	[S32K3_0.9.0][Tresos] Compilation failed with both ICU and OCU in project<*> I am facing a compilation issue when using both ICU and OCU - Tresos plugins of RTD_S32K3_BETA_0.9.0 In Emios_Ocu_Ip_Types.h and Emios_Icu_Ip_Types.h, you are having same macros naming but with different types of definitions. For example: <Emios_Ocu_Ip_Types.h> #define EMIOS_BUS_A (0x0U) <Emios_Icu_Ip_Types.h> typdef enum \{EMIOS_BUS_A 0} Which causes the compilation issue when using both of them in Tresos project.
ARTD-8340	Bug	[GPT] Compile_Only tests will fail because 'true' is used instead of 'TRUE'<*> !image-2021-03-09-10-37-33-788.png|thumbnail! usage of 'true' instead of 'TRUE' leads to a build failed
ARTD-8342	Bug	[MCU] Lack implement requirement RAM_IP_001_002<*> Follow requirement RAM_IP_001_002*: The function Ram_Ip_GetRamState shall be available to the user if the pre-compile parameter McuGetRamStateApi is set to TRUE. Instead, if the former parameter is set to FALSE, this function shall be disabled(e.g. the hardware does not support this functionality). Solution*: in Ip layer define a macro "RAM_IP_GET_RAM_STATE_API" and guard function Ram_Ip_GetRamState
ARTD-8347	Bug	[ADC] Incorrect name of variable types as coding guideline<*> Detailed description (how to reproduce it): Now, ADC example has some incorrect name of variable types as coding guideline (NULL) Platform_InstallIrqHandler(ADC0_IRQn, Adc_Sar_0_Isr, NULL); Platform_InstallIrqHandler(BCTU_IRQn, Bctu_0_Isr, NULL); Preconditions: [...] Observed behavior: Incorrect name of variable types as coding guideline Expected behavior: Correct name of variable types as coding guideline Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-8344	Bug	LCU output filter<*>

ID	Subtype	Headline and Description
		The LCU_FILT_LUT_RISE_FILT_MASK should be removed. Otherwise, the filter value writes to LCx_FILTy will always keep zero.
ARTD-8366	Bug	s32k3 siul2 icu callback function type<*> When configuring siul2_icu, the callback funtion is declaration generated in "Siul2_Icu_Ip_SA_BOARD_InitPreipherals_PBcfg.c" is void (void) type. But actually this callback funtion type is "Siul2_Icu_Ip_CallbackType", that is void (uint16, boolean). So there will be compiling warnings here since the generated function type doesn't match the callback function type definition. Also, I don't know why the callback function has two parameters. The second boolean parameter is not used according to Siul2_Icu_Ip.c source code "Siul2_Icu_Ip_Callback()" function definition.
ARTD-8367	Bug	[S32K3XX][PWM] Fix and comment static analysis violations after adding FlexIO ipv (MISRA + HIS + CERT-C)<*> After adding FlexIO ipv in Pwm driver, it has some misra violation and HIS that need to be fixed or commented . Please see attached file below :
ARTD-8381	Bug	[GPT] Lacking misra violation<*> !image-2021-03-10-15-11-14-772.png|thumbnail! please see the picture
ARTD-8386	Bug	[S32K][MCL-LCU] Correct Lcu_Ip_LogicInputInit function.<*> Update HwAcc_Lcu_AsyncSetInputSwSyncMode(HwLcu, LocHwLcInputId, (pConfig->SwSynMode & 1U) << LocHwLcInputId); to HwAcc_Lcu_AsyncSetInputSwSyncMode(HwLcu, LocHwLcInputId, (pConfig->SwSynMode & 1U));
ARTD-8393	Bug	[S32K3][MCL] TRGMUX Output Names for LCU need to be updated<*> Update the TRGMUX Output Names for: LCU_0_{color:#DE350B}-lc1-{color}_inp_i1 -> TRGMUX_IP_OUTPUT_LCU0_I0 LCU_0_{color:#DE350B}-lc1-{color}_inp_i2 -> TRGMUX_IP_OUTPUT_LCU0_I1 LCU_0_{color:#DE350B}-lc1-{color}_inp_i3 -> TRGMUX_IP_OUTPUT_LCU0_I2 LCU_0_{color:#DE350B}-lc1-{color}_inp_i4 -> TRGMUX_IP_OUTPUT_LCU0_I3 LCU_0_{color:#DE350B}-lc2-{color}_inp_i1 -> TRGMUX_IP_OUTPUT_LCU0_I4 LCU_0_{color:#DE350B}-lc2-{color}_inp_i2 -> TRGMUX_IP_OUTPUT_LCU0_I5 LCU_0_{color:#DE350B}-lc2-{color}_inp_i3 -> TRGMUX_IP_OUTPUT_LCU0_I6 LCU_0_{color:#DE350B}-lc2-{color}_inp_i4 -> TRGMUX_IP_OUTPUT_LCU0_I7 LCU_0_{color:#DE350B}-lc3-{color}_inp_i1 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}8 LCU_0_{color:#DE350B}-lc3-{color}_inp_i2 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}9 LCU_0_{color:#DE350B}-lc3-{color}_inp_i3 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}10

ID	Subtype	Headline and Description
		LCU_0_{color:#DE350B}-lc3-{color}_inp_i4 -> TRGMUX_IP_OUTPUT_LCU0_I{color:#57D9A3}11 Same for LCU1.
ARTD-8402	New	New Feature [ETH]Revert Gmac_Cfg.h caused by merged Kinetis code ,,Gmac_Ip_Cfg.h changed when merged Kinetis driver. Have to revert.
ARTD-8406	New	New Feature [S32K3XX][VNV_CONFIG] Update wiring for PWM ,,"Update wiring for PWM as below: Test point MCU pin Jump MAF_TP_PWM0_1 PTC31 J181.1 MAF_TP_PWM0_5 PTD24 J184.11"
ARTD-8416	Bug	[MCU] FXOSC bypass bit(FXOSC_CTL[OSC_BYP]) will not be generated appropriately<*> Description: SWS reported that FXOSC Bypass configuration in McuFXOSC will not be applied to generated source code. As you can see in the figure below, even when FXOSC Bypass's checkbox is cleared, XOSC bypass option in Clock_I_PBcfg.c will be 0. #if CLOCK_XOSCS_NO > 0U { FXOSC_CLK, / Clock name associated to xosc / 40000000U, / External oscillator frequency. / 1U, / Enable xosc. / 157U, / Startup stabilization time. / 0U, / XOSC bypass option / This value is always 0 0U, / Comparator enable / 12U, / Crystal overdrive protection / }, Proposal solution: Update the code(By*P*ass to By*p*ass) of in the file Clock_Ip_RegOperations.m from: [!MACRO "GetXoscBypass","Name"!][!// [!NOCODE!] [!VAR "capitalName" = "text:replace($Name,substring($Name,2),text:tolower(substring($Name,2)))"!] [!VAR "bypassPath" = "concat('Mcu',$Name,'/Mcu',$capitalName,'ByPass')"!] to: [!MACRO "GetXoscBypass","Name"!][!// [!NOCODE!] [!VAR "capitalName" = "text:replace($Name,substring($Name,2),text:tolower(substring($Name,2)))"!] [!VAR "bypassPath" = "concat('Mcu',$Name,'/Mcu',$capitalName,'Bypass')"!]
ARTD-8424	Bug	[SAI] Missing check in configurator for Element Size to be larger than Sai Word Width<*> Add check in configurator for this note from RM:

ID	Subtype	Headline and Description
		70.3.4.2 FIFO pointers When writing to a Transmit Data Register (TDRn), the Write FIFO Pointer (WFP) of the corresponding Transmit FIFO Register (TFRn) increments after each valid write. The SAI supports 8-bit, 16-bit, and 32-bit writes to the Transmit Data Register and the FIFO pointer increments after each individual write. Note that 8-bit writes should only be used when transmitting up to 8-bit data; 16-bit writes should only be used when transmitting up to 16-bit data. Also clarify description and node name: Sai_RequestType: /**< brief Buffer Size : The number of words for reading or writing of each channel. / uint32 bufferSize; The word size from here is actually defined by number of bytes in "Sai Element Size", not the SAI word width. I suggest renaming to "Sai Buffer Element Size" and adding a comment for bufferSize, to clarify this: "The number of words for reading or writing of each channel. The size of each buffer word element is "Sai Buffer Element Size" selected in configurator. /
ARTD-8432	Bug	[S32K3XX][PWM] The name of the configuration structure for PB is not correct<*> Detailed description (how to reproduce it): Naming of the configuration structure for PB is not correct. If post-build variants exist, then the configuration structure used for initialization must be named as <Mip>_Config_<PredefinedVariant.shortName>. Otherwise, the name is <Mip>_Config. But now, the generated name of configuration structure is Pwm_Config[!"$postBuildVariantNameUnderscore"!]_PB; We need remove "_PB" there. Preconditions: IMPLEMENTATION_CONFIG_VARIANT = VariantPostBuild Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8435	Bug	[ICU][S32K3XX] Generate failed in DS in Icu module about masterbus<*> Detailed description (how to reproduce it): Icu ASR component using EMIOS IP with CounterBus selection in Mcl issues error on generation. Preconditions: Create project in DS with emios using counter bus. Define the counterbus in Mcl component. Try to generate and build the project. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: Multiple issues reported in Problems View. Expected behavior: Code generation works and build of project can be done.

ID	Subtype	Headline and Description
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: Generate failed in DS in Icu module about masterbus. pls see attach file

ARTD-8444	Bug	s32k3 rtd lpspi drv source code issue<*>
		
		In the source code "Lpspi_lp.c", line 1254, the code is:
		if (state != NULL_PTR)
		while it should be like this:
		if (state == NULL_PTR)

ARTD-8446	Bug	[S32DS] Generated file for S32DS high layer missing some parameter in config<*> Please refer to the attached image to see the error of the parameter. It is need to generate same as in EB Tresos. !image-2021-03-12-17-11-23-353.png!
ARTD-8459	Bug	[ICU][S32K3XX] Generate with ECUM string in DS in Icu<*> Detailed description (how to reproduce it): Icu ASR component using channels with wakeup is generating with fix string on wakeup source. Preconditions: Create project in DS with channels with wakeup capabilities. Try to generate and build the project. Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: !image-2021-03-12-17-48-22-090.png! Expected behavior: Code generation works and build of project can be done. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: correct wakeup source generation.
ARTD-8463	Bug	[S32K3XX] PWM: The failed building with CT when using the interrupt<*> Detailed description (how to reproduce it): Cannot generate the Prototypes of PWM channels User Notifications in HLD in CT Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]

ID	Subtype	Headline and Description
ARTD-8465	New	New Feature [S32K344] [PORT] (ITG)Adding new req relate to execute test with supervisor mode and user mode ,,"NewWorkDescription: new reqs about run test with user mode and supervisor mode: CPR_RTD_00395.port: The RTD drivers shall be able to run in a privileged processor mode (e.g. Supervisor mode). All known related constraints shall be documented. CPR_RTD_00352.port: The Real Time Drivers shall be able to run in a non-privileged processor mode (e.g. User mode). All known related constraints shall be documented. A vendor specific pre-compile boolean configuration parameter PortEnableUserModeSupport \{PORT_ENABLE_USER_MODE_SUPPORT}shall be created for each driver to activate the specific implementation for non-privileged mode. By default, 'PortEnableUserModeSupport' field shall be disabled. Requirement source: CPR_RTD_00395.port, CPR_RTD_00352.port (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: add on Port_TC_WBT_0036"
ARTD-8472	Bug	[MCU][S32CT] Wrong condition of RAM DEFAULT VALUE<*> Condition of RAM DEFAULT VALUE is incorrect on S32CT. RAM DEFAULT VALUE have range is 0 > 255. But when i add 255 to McuRamDefaultValue, S32CT display error "The Ram base address must be 4 byte aligned" Detail in attached files
ARTD-8491	Bug	[GPT] Duplicate UUIDs<*> Coding convention implies that no TAB is to be used in the code source files we deliver. (to avoid inconsistent displays of code alignment if TAB size is defined differently) Replace all duplicated UUIDs, to avoid generation crashes on customer side. Proposed solution: Replace all TABs with 4 spaces. Update your text editor settings to always use 4 spaces instead of a TAB Replace duplicated UUIDs. Summary: Plugin No. of duplicated UUIDs Eth.xdm 1 Gpt.xdm 1 Lin.xdm 2 Rm.xdm 236 Rm_s32k314_mapbga257.xdm 2 Rm_s32k314_mqfp100.xdm 118 Rm_s32k314_mqfp172.xdm 118 Rm_s32k324_mapbga257.xdm 118 Rm_s32k324_mqfp172.xdm 118 Rm_s32k344_mapbga257.xdm 118 Rm_s32k344_mqfp172.xdm 118 Sai.xdm 1 Sent.xdm 2

ID	Subtype	Headline and Description
ARTD-8494	Bug	[GPT] Re-Align code for run TraceabilityMatrix<*> Some line of code not match with implement Do Not change line of code
ARTD-8498	Bug	[ADC] Adc_ConfigVariantPredefined placed in different memory section in .h vs .c<*> Detailed description (how to reproduce it): Adc_ConfigVariantPredefined placed in different memory section in .h vs .c .h: #ifdef ADC_PRECOMPILE_SUPPORT #define ADC_START_SEC_VAR_NO_INIT_UNSPECIFIED #include "Adc_MemMap.h" extern const Adc_ConfigType const Adc_ConfigVariantPredefined[ADC_MAX_PARTITIONS]; #define ADC_STOP_SEC_VAR_NO_INIT_UNSPECIFIED #include "Adc_MemMap.h" #else in .c is placed in ADC_START_SEC_CONFIG_DATA_UNSPECIFIED The variable ends up alocated in mcal_const_cfg with gcc and iar. So functionality is correct Expected behavior: same memory section used for function declaration and definition
ARTD-8543	New	New Feature [S32K344] [PORT] (ITG)Fix issue relate to StandardType ,,"NewWorkDescription: Build fail when execute test IPL relate to undefine some variables when have condition NO_STDINT_H Requirement source: NA Proposed solution optional: IP_Port_Siul2_TC_0001, ...-> IP_Port_Siul2_TC_0006"
ARTD-8558	Bug	[ICU][S32K3XX] The array length for instance configuration is wrong<*> Detailed description (how to reproduce it): There are 2 items to address: in file Icu_Ipw_VS_0_PBcfg.c; array size for instance configuration is wrong (see picture attached) the generation for the case where the reference ECUM wakeup info is missing is rising error in tool even if the wakeup capability is not enabled for the channel this is a regression from previous TAG. Preconditions: use attached mex file for configuring an example in DS Test Case ID (internal TC that caught the defect) optional: NA Observed behavior: with latest icu tag there are errors on generation and also if the errors are corrected in generation the size of instances array is wrong. The array length contains the instance configuration is error in file Icu_Ipw_VS_0_PBcfg.c. In the attach file, the configuration has 3 instances, but the length array is 5. Expected behavior:

ID	Subtype	Headline and Description
		generation is not depending on wakeup capability and size of array should be correct. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:
ARTD-8566	Bug	[K3XX][ETH] Fix "true" -> "TRUE" in Eth_Ipw_SetCorrectionTime ,,"Detailed description (how to reproduce it): When the option CCOPT+=-DNO_STDINT_H is enabled on .mak file. The compile only tests for HLD failed at build. In Eth_Ipw.c, line 523, please fix: ""true"" > ""TRUE"" STDERR:C:/vv_tools/eb/EB_tresos_Studio_27.1.0_b200625-0900_06/plugins/Eth_TS_T40D34M9I0R0/src/Eth_Ipw.c:523:85: error: 'true' undeclared (first use in this function) Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: Eth_TS_035 Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8572	New	New Feature [S32K344] [PORT] (ITG)Fix issue relate to StandardType ,,"NewWorkDescription: Build fail when execute test IPL relate to undefine some variables when have condition NO_STDINT_H Requirement source: NA Proposed solution optional: IP_Port_Siul2_TC_0004"
ARTD-8575	Bug	[Wkup]: The error of "selected core does not support NMI" has always existed in s32ds3.4+RTD0.9.0.<*> Detailed description (how to reproduce it): [No matter how you modify the Wkup configuration, the error of "selected core does not support NMI" has always existed in s32ds3.4+RTD0.9.0.] !RTD_Wkup_error.png! : [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: [...] Expected behavior: [...] Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional:

ID	Subtype	Headline and Description
		[...]
ARTD-8582	New	New Feature [S32K344 BETA][CF3] GPT: Test code update ,,"IPs list: eMIOS, PIT, STM, RTC. Tests implementation. 100% requirements coverage. Update test code for Ip layer"
ARTD-8595	Bug	[SAI] S32CT can not config data line when use interrupt and mux_mem mode<*> Detailed description (how to reproduce it): Create new SAI project with S32DS Select INTERRUPT and MUX_MEM mode Enable Sai Data Line 0, 1, 2 Preconditions: [...] Test Case ID (internal TC that caught the defect) optional: [...] Observed behavior: Appear an error: "In memory mux mode and interrupt, enable at least two datalines." Expected behavior: Project have no error when enable at least 2 data line in memory mux mode and interrupt Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-8596	New	New Feature [S32K344 BETA] Crypto: Update driver FMEA ,,"NewWorkDescription: Update *Driver source code and *Driver requirements FMEA fields with the latest souce code tag and requirements. Requirement source: FMEA (e.g.cPRD,gMRD, Customer Request, Quality, ASR SWS, RM.pdf, Errata.pdf...) Proposed solution optional: Driver source code: *CRYPTO_043 Driver requirements:*10.0 BLNREQ_CRYPTO_RTD_4.4_S32K3XX_0.9.0"

ARTD-8599	Bug	[ADC] Normal Software group cannot run in parallel with Injected HW group with DMA enable<*>
		
		Detailed description (how to reproduce it):
		Normal Software group cannot run in parallel with Injected HW group with DMA enable, because StartGroupConversion reprograms DMA channel.
		ExternalDma cannot be used as workaround for ADC Sw group, because in Adc_Ipw_StartNormalConversion all DMA channels are disabled before enabling again the DMA channel for Sw group:
		#ifdef ADC_DMA_SUPPORTED
		if (ADC_DMA == Adc_pCfgPtr[u32CoreId]->pAdcIpwConfig->Mapping.u8Adc_DmaInterruptSoftware[Unit])
		{

ID	Subtype	Headline and Description

		Adc_Sar_Ip_DisableChannelDmaAll(Unit);
		Adc_Sar_Ip_EnableChannelDma(Unit,pGroupPtr->LastCh);
		Adc_Sar_Ip_EnableDma(Unit);
		if((uint8)STD_OFF == pGroupPtr->u8AdcExtDMAChanEnable)
		{
		/ Configure DMA in MCL module /
		Adc_Ipw_StartDmaOperation(Unit, Group, u32CoreId);
		}
		}
		else
		Preconditions:
		Adc_EnableHardwareTrigger for injected group with DMA must be called before calling SW group
		Test Case ID (internal TC that caught the defect) optional:
		N.A.
		Expected behavior:
		Sw Group can work in parallel with or without interrupt or with dma
		Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)

ARTD-8609	Bug	[GPT][S32K3XX] Add volatile keyword for variable testcase multicore to avoid hardfault error when compiler is optomized<*> Avoid compiler optimization with variable in testcase sometime lead to hardfault error.
ARTD-8621	Bug	[ADC] DMA streaming without interrupts is not working simultaneously on multiple ADCs because u32DmaNoIrqBuffer is shared between ADCs<*> Detailed description (how to reproduce it): DMA streaming without interrupts is not working simultaneously on multiple ADCs because u32DmaNoIrqBuffer is shared between ADCs Preconditions: N.A. Test Case ID (internal TC that caught the defect) optional: N.A> Observed behavior: DMA streaming without interrupts is not working simultaneously on multiple ADCs because u32DmaNoIrqBuffer is shared between ADCs Expected behavior: DMA streaming without interrupts works simultaneously on multiple ADCs Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.)
ARTD-8634	New	New Feature [GPT] [S32K3XX] Remove config Emios for test multicore external because of some unknown hardfault when running with GCC compiler ,,"When i run test configured for Emios with 2 parabell core at once, Error hardfault occurred but it is not clear. This error happen is random at any location while running test. But if turning off compiler optimization, this will not happen anymore. With other compiler GHS and IAR, test is good and stable, and also with internal test without running with MAF, for Emios hardware, running test wit Emios is absolutely stable. So i think this error maybe due to MAF or some issue with optimization of compiler. So i will remove config for Emios in test for testsuite Gpt_TS_300 to avoid this error effect to the result of test and document collection."

ID	Subtype	Headline and Description
ARTD-8651	Bug	[CRYPTO][CT Examples] Duplicate number of catalogue in description.txt of some example projects<*> Precondition:* Open S32SD3.4 update1 which installed package SW32_RTD_4.4_1.0.0_HF01_D2102_DS_Updatesite.zip! Step: 1.Import all example project for S32G: 2. Open description.txt then check content Observed behavior: Duplicate number of catalogue " 3.2 Compiling the application" and " 3.2 Running the application on the board" Wdg_Example_IPL_DS Wdg_Example_HLD_DS Uart_HLD_S32G_DS_Example Linflexd_Uart_Ip_S32G_DS Spi_IP_example_CT_S32G Spi_HLD_example_CT_S32G Qdec_Ip_example_DS Qdec_example_DS Port_example_DS Ocu_Ftm_example_DS Ocu_example_DS Ocotp_IP_Example Ocotp_AUTOSAR_Example Lin_example_IPV Lin_example_HLD Icu_Siul2_Wkpu_example Icu_Ftm_example Icu_ASR_example I2c_S32G274A_IP_DS I2c_S32G274A_HLD_DS Example_S32G2XX_DS_Qspi_Ip Example_S32G2XX_DS_Fls Fee_Example_S32G2 Eth_Example_DS_002 Eth_Example_DS_001 Example_S32G2XX_DS_Eep Dio_example_DS_S32G Hse_Ip_Read_Hse_Attr Hse_Ip_Aes_Enc_Async_Irq Crypto_Hash Crypto_Cmac_Gen_Ver Crypto_Aes_Enc_Dec FlexCAN_example_CT CAN_example_CT Adc_example_DS_IP Adc_example_DS Expected behavior:

4.12 Change List for EAR 0.8.1

ID	Subtype	Headline and Description
ARTD-952	Bug	[MCL] VSMD Report: Warnings and Errors<*>

ID	Subtype	Headline and Description
		RTD_MCL_VSMDReport.html contains warnings and errors which need to be resolved/ commented.
ARTD-971	New	New Feature [CAN][S32G274 BETA] CAN Add support for Enhanced RxFIFO ,,"Add support for Enhanced RxFIFO Configuration, setup of Enhanced Rx Filters, support for read of messages(pooling, interrupt and DMA)"
ARTD-982	Bug	[OCU] Update EBT config files to remove warnings like "'macro' is not defined, evaluates to 0" ,,"Update EBT config files to remove warnings like ""_'macro' is not defined, evaluates to 0_""
ARTD-1052	New	New Feature [S32G274 BETA][S32K3 BETA] GPT: Update test specification to fix comments from STRX team ,,"When creating the TestCases and the Test Specification, please check attachment and fix comments from STRX team for below module: ADC, CAN, CRYPTO, DIO, ETH, FEE, FLS, GPT, I2C_CDD, ICU, MCL, MCU, OCU, PORT, PWM, SPI, WDG"
ARTD-1161	New	New Feature [SENT][S32K3XX BETA] Implementation for Serial Enhanced Messages ,,"Serial Enhanced support needs to be implemented: Implement algorithm to decode Serial message from FLEXIO timer to: Enhanced Short data. Create 2 functions Sent_GetSerialMsgData, Sent_GetSerialChannelMsgData to receive serial message."
ARTD-1176	Bug	[MCL] TRGMUX: S32CT Configuration of Logic Trigger Group is not limited<*> The TRGMUX S32CT Logic Group number of triggers is not limited to the number of possible triggers per group.
ARTD-1464	New	New Feature [cdd_qd] [S32G274 BETA]Fix copyright violations ,,"Please refer to the attached ""copyright_violations.txt"" ([https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/General/Attachments/S32G%20RTD%204.4%200.9.0/ARTD-972/copyright_violations.txt]) to identify the files that need to be updated. The plugins of the following drivers contain at least a source file or header file without copyright notice: [adc|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+adc], [base|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+base], [can|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+can], [canif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+canif], cryif, crypto, csm[, dem|https://

ID	Subtype	Headline and Description
		jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+dem], [det|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+det], [dio|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+dio], [ecum|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+ecum], eep, [eth|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+eth], [fee|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+fee], [fls|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+fls], [gpt|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+gpt], [i2c_cdd|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+i2c_cdd], [icu|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+icu], [linif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+linif], [mcl|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+mcl], [mcu|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+mcu], [memif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+memif], ocu, os, [port|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+port], pwm, qdec, rm, sent, [spi|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+spi], uart, [wdg|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+wdg], [wdgif|https://jira.sw.nxp.com/issues/?jql=project+%3D+ARTD+AND+component+%3D+wdgif] Please refer to the following link to obtain the correct header comment (which contains the copyright notice): [https://confluence.sw.nxp.com/display/AUTORD/Module+C+source+files+templates]"
ARTD-1474	New	 New Feature [ETH]Support time-aware shaper and Preemption ,,Support time-aware shapper along the credit base feature
ARTD-1499	Bug	 [MCL] Hard Fault is triggered when using Mcl_Init() to configure channels from 13 to 31<*> Detailed description (how to reproduce it): I have tried running a test but it not work because the program jump to hard fault when using Mcl_Init function to configure for channel 12 > 31. With configuration on EB as: Config all paramater for the logic channels 0 > 31. I investigated and saw that the address offset of channels 12 31, which the drive defined, is incorrect. it will result the program jump to hard fault in Dma_Ip_Features.h file in MCL drive #define DMA_IP_TCD_PTR_ARRAY ((Dma_Ip_HwChTcdRegType) ((uint32)DMA_IP_TCD_BASE (uint32)(0U 16384U))),\ ..... ((Dma_Ip_HwChTcdRegType)((uint32)DMA_IP_TCD_BASE (uint32)(11U 16384U))),\ ((Dma_Ip_HwChTcdRegType)((uint32)DMA_IP_TCD_BASE (uint32)(1916928U (0U 16384U)))),\ ((Dma_Ip_HwChTcdRegType)((uint32)DMA_IP_TCD_BASE (uint32)(1916928U (1U 16384U)))),\ .....} I have calculated and replaced 1916928U to 2097152U. it works well. Preconditions: Config all paramater for the logic channels 0 > 31 on EB tresos. Test Case ID (internal TC that caught the defect) optional: Mcl_TC_FCT_0201 Observed behavior:

ID	Subtype	Headline and Description
		Got Hard Fault when using Mcl_init function to configure for channels 13 through 31 Expected behavior: Hard Fault no longer occur Note:* in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: N/A
ARTD-1525	New	 New Feature [SENT][S32K3XX BETA] Implementation for Fast Messages using polling ,,"Implement feature to receive Fast message using polling method (Synchronous reception using polling method) Sent_GetFastMsgData Sent_GetFastChannelMsgData"
ARTD-1550	Bug	 [S32CC][DIO] Driver implement missing SIUL2 Parallel GPIO Pad Data In Register (PGPDI)<*> Test case Wiring for test_dio build fail. DIO driver missing SIUL2 Parallel GPIO Pad Data In Register (PGPDI)) TC : tse_bbx_wir_dio_00100 Expected behavior:* Dio driver add PGPDI feature Solution: Add the MACRO for PGPDI. Check all the other MACRO for other register and update.
ARTD-1552	New	 New Feature [CRYPTO] Add Tresos support for running on top of different HSE Firmware Types (Standard, Premium)" ,,"Add support for running on top of different HSE Firmware Types (Standard, Premium) add a new attribute in Tresos plugin called HseFwType allowing the user to choose the flavour of the HSE that runs under Crypto update resource.txt files to include distinct values for the supported Hse Fw types update the EBT Crypto,xdm file such that all ecu:get and ecu:list calls are made to the resource variables constructed based on the user chosen Hse Fw Type update the EBT Crypto_Cfg.c/h file such that all ecu:get and ecu:list calls are made to the resource variables constructed based on the user chosen Hse Fw Type
ARTD-1564	Bug	 [MCL] Mcl_CacheDisable() triggers HardFault_Handler()<*> when use function Mcl_CacheDisable(Mcl_CacheAll); to disable cache for S32K3xx Function disable cache is not available and jump to HardFault_Handler() (Note: If call to funtion clean cache before disable cache, function Mcl_CacheDisable() is available) Detail on attached file
ARTD-1567	New	 New Feature [SENT][S32K3XX BETA] Implementation for Fast Messages using interrupt ,,Implement feature to receive Fast message using interrupt method (Asynchronous reception using interrupt method)
ARTD-1619	New	

ID	Subtype	Headline and Description
		New Feature [ocu] Update target_path in manifest files ,,"The target folder name in DS has been changed to ""RTD"" from ""SDK"": !image-2020-09-16-17-01-39-986.png! As a result, all the target_path attributes in the driver's manifest files must be updated: Example: {code:xml|title=old_sdk_manifest_ethernet.xml|borderStyle=solid} <component id=""platform.driver.gmac"" full_name=""Gmac"" brief=""""" dependency="""" name=""Gmac"" type=""driver"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2"">"> <source path=""Eth_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""SDK/ src"">"> <files mask=""Gmac*.c""/> </source> <source path=""Eth_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""SDK/include"">"> <files mask=""Gmac*.h""/> <files mask=""Emac_Ip_Wrapper.h""/> </source> </component> {code:xml|title=new_sdk_manifest_ethernet.xml|borderStyle=solid} <component id=""platform.driver.gmac"" full_name=""Gmac"" brief=""""" dependency="""" name=""Gmac"" type=""driver"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2"">"> <source path=""Eth_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/ src"">"> <files mask=""Gmac*.c""/> </source> <source path=""Eth_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include"">"> <files mask=""Gmac*.h""/> <files mask=""Emac_Ip_Wrapper.h""/> </source> </component> "
ARTD-1708	New	New Feature [I2C] Driver should support for precompile variant ,,Driver should support for precompile variant
ARTD-1752	New	New Feature [ocu] Handle SchM files in a Design Studio project ,,"Each driver that has SchM files in the Rte driver needs to update its sdk manifest xml file to copy the .c and .h files from Rte when the component is added in the project. Reference implementation: [https://bitbucket.sw.nxp.com/projects/ARTD/repos/dem/pull-requests/10/diff#specific/S32CC/sdk_manifest_dem.xml] A new component will be added in the driver manifest: The name of the new component should be Rte_<module_name>. Ex: Rte_Spi, Rte_Can_43_LLCE (for vendor API infix extended module names) <component id=""platform.driver.rte_dem"" full_name=""Rte_Dem"" brief=""""" dependency="""" name=""Rte_Dem"" type=""utilities"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2"">"

ID	Subtype	Headline and Description
		<source path=""Rte_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""Rte_Dem_Type.h""/> </source> </component> or <component id=""platform.driver.rte_eth"" full_name=""Rte_Eth"" brief="""" dependency="""" name=""Rte_Eth"" type=""utilities"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Rte_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""SchM_Eth.c""/> </source> <source path=""Rte_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""SchM_Eth.h""/> </source> </component> The new component will be added as dependency for the other components that need it: Example: <component id=""platform.driver.dem"" full_name=""Dem"" brief="""" dependency=""platform.driver.rte_dem"" name=""Dem"" type=""driver"" devices=""S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Dem_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""*.c""/> </source> <source path=""Dem_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""*.h""/> </source> </component> "
ARTD-1862	Bug	 [SENT] Fix bugs on Sent_Init and Flexio_Sent_Ip_Init<*> Flexio_apChnlConfig should be pointer to pointer in Flexio_CtrlConfigType structure Flexio_aChnlUserConfig's elements which are generated from EB are not matched with Flexio_Sent_Ip_UserConfigType. Re-struct Flexio_Sent_Ip_StateType, flexioCommon (rename to chnlCfg) should be array of channel configuration (instead of array of pointer). Flexio_Sent_Ip.c: global variables have no address when were initialized.
ARTD-2022	Bug	 [SENT] Fix algorithm to receive fast message<*> List of issues: Flexio_Sent_Ip_Configure: TRGSEL bit need to be written with 2*N (Pin N input). Flexio_Sent_Ip_GetFastMsgFromRaw: wrong algorithm to extract nibble value from the RAW value. Flexio_Sent_Ip_StartTransfer: update code to prevent reduce error of calculation. Flexio_Sent_Ip_GetFastChannelMsgData: TIMSTAT need to be cleared only when this flag was raised
ARTD-2052	New	 New Feature

ID	Subtype	Headline and Description
		[CAN][CPR_RTD_00513.can] Can_ListenOnlyMode API ,,"Feature for CAN Listen-Only Mode need to be implemented disabling/enabling Can_ListenOnlyMode API on EB Std_ReturnType Can_ListenOnlyMode(uint8 Controller, Can_ListenOnlyType State) API in driver code TC_ID: CAN_TC_FCT_*11550"
ARTD-2056	Bug	[SENT] Fix algorithm to receive serial message<*> List of bugs: # Missing Sent_GetSerialChannelMsgData and +Sent_GetSerialMsgData on HLD and IPW layer. # Flexio_Sent_Ip_ProcessSerialMsg+: Missing extract startbit from status&communication nibble:_ startbit = ((data->aNibbleVal[0] & 0x08) >> 3); # Flexio_Sent_Ip_GetSerialChannelMsgData+: Wrong condition to check serial message processing done Fast message state is not reset after fast message processing done. TIMSTAT bit need to be cleared only when this flag was raised.
ARTD-2092	New	New Feature [crypto] Fix XDM violations ,,"Please refer to the attached ""xdm_violations.txt"" ([https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/General/Attachments/S32G%20RTD%204.4%200.9.0/ARTD-2088/xdm_violations.txt]) to identify the xdm lines that need to be updated. There are 3 types of violations: # Violation 1: Nodes that have constant false editable conditions (exception being the nodes under <Mdl>_ModuleDescription) Solution 1: <a:a name=""EDITABLE"" value=""false""/> will change to <a:a name=""READONLY"" value=""true""/> # Violation 2: Nodes which have READONLY attributes with XPath Solution 2: <a:da name=""READONLY"" type=""XPath"" expr=""..."" /> will change to <a:da name=""EDITABLE"" type=""XPath"" expr=""..."" /> # Violation 3: Reference nodes which use READONLY instead of EDITABLE Solution 3: Reference nodes (type=""REFERENCE"") with <a:a name=""READONLY"" ... />will change to <a:a name=""EDITABLE"" ... />"
ARTD-2100	New	New Feature [ocu] Fix XDM violations ,,"Please refer to the attached ""xdm_violations.txt"" ([https://nxp1.sharepoint.com/sites/Zebra/Shared%20Documents/General/Attachments/S32G%20RTD%204.4%200.9.0/ARTD-2088/xdm_violations.txt]) to identify the xdm lines that need to be updated. There are 3 types of violations: # Violation 1: Nodes that have constant false editable conditions (exception being the nodes under <Mdl>_ModuleDescription) Solution 1: <a:a name=""EDITABLE"" value=""false""/> will change to <a:a name=""READONLY"" value=""true""/> # Violation 2: Nodes which have READONLY attributes with XPath Solution 2: <a:da name=""READONLY"" type=""XPath"" expr=""..."" /> will change to <a:da name=""EDITABLE"" type=""XPath"" expr=""..."" /> # Violation 3: Reference nodes which use READONLY instead of EDITABLE Solution 3: Reference nodes (type=""REFERENCE"") with <a:a name=""READONLY"" ... />will change to <a:a name=""EDITABLE"" ... />"

ID	Subtype	Headline and Description
ARTD-2145	Bug	[SENT] IRQ Handler functions need to be combined due to FLEXIO has only 1 interrupt vector<*> With the current implementation, a SENT channel (Flexio timer) has a processing type (interrupt/polling/dma) individually. This is incompatible with FLEXIO hardware. A FLEXIO controller has only 1 interrupt vector for all inside timer channel*. It causes that Fast/Serial message need to handle in a IRQ handler function. So driver needs change: Configuration file: merge Fast/Serial processing type to Sent processing (_SentProcessing_) type and move from the channel to the controller. Configuration file: SentProcessing is enabled only when InterruptCombination is enabled. Used FLEXIO_Ctrl0_SentMessageIRQHandler for IRQ handler in combinedIRQ and SENT has only Combined IRQ type when IPV = FLEXIO.
ARTD-2177	Bug	[MCU] Fix compiling errors on PMC activation<*> When the POWER component is added, some errors appear by default. !pwr_errors.png! Fixed by removing "_U32" from some lines of the PMC.c file. There is also a missing parenthesis in line #214, causing issues. Working PMC_PrepareLowPowerEntry looks like this. !pwr_solved.png!
ARTD-2178	Bug	[MCU] Fix inconsistent naming problems in MC_ME<*> There are some inconsistent naming between MC_ME.c and MC_ME.h files. Fixed by changing MC_ME_GetPreviousMode MC_ME_SocStandbyEntry MC_ME_CoreStandbyEntry To Power_Ip_MC_ME_GetPreviousMode Power_Ip_MC_ME_SocStandbyEntry Power_Ip_MC_ME_CoreStandbyEntry in the MC_ME.c driver file.
ARTD-2180	Bug	[MCU] Fix incorrect MC_ME register access<*> Incorrect access to the following MCME registers. pMC_ME->MODE_CONF pMC_ME->MODE_UPD Fixed as follows in MC_ME.c file !conf.png! !upd.png!
ARTD-2181	Bug	[MCU] Fix Main Core Select generation issue in CT<*> The selection of the Main Core in the ConfigTool is not reflected in the generated code. !ct.png! !maincore.png!
ARTD-2200	Bug	

ID	Subtype	Headline and Description
		[SENT] Sent_Config is generated incorrectly in some cases of ECUC and VariantPostBuild<*> Sent_Config is generated with unexpectation in case: Driver is in Precompile with both of existing SENT EcucPartition References and no ECUC partition referenced in SENT. The issue comes from Sent_PBcfg.c: Name of some nodes variables (SentControllerConfig, SentEcucPartitionName,) is wrong.
ARTD-2211	New	New Feature [PORT] Implement the CPR_RTD_00026: Adding HIGH_Z direction for Port driver ,,"Internal Requirement: CPR_RTD_00026: ""The type Port_PinDirectionType shall be of enumeration type having range as PORT_PIN_IN, PORT_PIN_OUT, PORT_PIN_INOUT, PORT_PIN_HIGH_Z. (extension of SWS_Port_00220 AUTOSAR requirement)"" The HIGH_Z direction need to be added in Port driver"
ARTD-2228	New	New Feature [PORT] Implement SIUL2_PORT_007_001, SIUL2_PORT_007_002: Add Siul2_Port_Ip_SetPinDirection API" ,,"SIUL2_PORT_007_001, SIUL2_PORT_007_002+_: "A function, named Siul2_Port_Ip_SetPinDirection shall configure the IBE and OBE according to the direction parameter."
ARTD-2242	New	New Feature [SENT] Implement CRC checking for Fast and Serial message ,,"Current driver supports CRC Recommended Implementation with 256 Element Array for Fast message only. Therefore, driver need to update following by SAEJ2716 For Fast Short message: add more LEGACY Implementation: The CRC checksum can be implemented as a series of shift left by 4 (multiply by 16) followed by a 256 array lookup. RECOMMENDED implementation with 6 Element Array: The CRC checksum can be implemented as a bit-wise exclusive OR with a 16 element array lookup. For Enhanced message: Add new function to check CRC. The CRC checksum can be implemented via a bit-wise exclusive OR with a 64 array lookup"
ARTD-2498	Bug	[gpt] Fix attached findings for generation with S32DS<*> For details see one note page [GPT|#section-id=\{353E5BC1-7280-46C5-B130-090DAA3A19F8}&end] ([Web view|https://nxp1-my.sharepoint.com/personal/viet_nguyen_nxp_com/_layouts/OneNote.aspx?id=%2Fpersonal%2Fviet_nguyen_nxp_com%2FDocuments%2FNotebooks%2FLIST_BUG_G6_TEST&wd=target%28GPT.one%7C353E5BC1-7280-46C5-B130-090DAA3A19F8%2F%29]) attached pictures Also align templates from UCT with templates from EBT
ARTD-2503	Bug	PORT: PortPinMode Error of PTC6&PTC7<*> when I input 70/71(means PTC6&PTC7) in "PortPin Mscr"(dynamic range), these two pins' "PortPin Mode" do not have I2C related item. The chip is S32K344.

ID	Subtype	Headline and Description
ARTD-2567	New	New Feature [eth] How to handle Det files in DS+CT projects ,,"Det files need to be added in a DS+CT project when HLD components are used so the drivers can be compiled when the development errors detection is enabled. The Det stub already has a manifest associated to it, so each driver that needs Det for a successful build should add Det as a dependency in its manifest. Example from the Adc driver: <component id=""platform.driver.adc"" full_name=""Adc"" brief=""Adc Component"" dependency=""platform.driver.det"" name=""Adc"" type=""driver"" devices=""S32K314 S32K324 S32K344 S32G233A S32G234M S32G254A S32G274A S32G274A_Rev2""> <source path=""Adc_TS_$(AR_RELEASE_ID)/src"" type=""src"" target_path=""RTD/src""> <files mask=""*.c""/> <files mask=""Adc_Sar_Ip_HwAccess.h""/> </source> <source path=""Adc_TS_$(AR_RELEASE_ID)/include"" type=""c_include"" target_path=""RTD/include""> <files mask=""*.h""/> </source> </component> "
ARTD-2594	Bug	[S32K344] OCU: CT Config files - remove magic numbers or hard-coded values<*> Do not use magic numbers or hard-coded values; use resource values or defines from platform header files as much as possible

ARTD-2623	Bug	[IP_Flexcan][FLEXCAN_IP_001_003] FlexCAN_Ip_SetBitrate should remain in original mode after timeout<*>
		
		eResult = FlexCAN_Ip_SetStopMode(u8Inst);
		EU_ASSERT(FLEXCAN_STATUS_SUCCESS == eResult);
		
		eResult = FlexCAN_Ip_SetBitrate(u8Inst, &bitrate, false);
		EU_ASSERT(FLEXCAN_STATUS_TIMEOUT == eResult);
		
		Verification point: EU_ASSERT(TRUE == FlexCAN_Ip_GetStopMode(u8Inst));
		> fail due to after timeout, FlexCAN_Ip_SetBitrate did not return to original mode (stop/disabled mode).
		TC_ID: *Ip_FlexCAN_TC_FCT_1054
		A:
		!image-2020-10-19-16-55-24-980.png!
		=> this snippet code should be considered to be updated
		
		B: FlexCAN_EnterFreezeMode does not enter freeze mode if module is being in stop/disabled mode (this is another issue)
		=> below code should be considered !image-2020-10-19-16-52-45-500.png!

ARTD-2662	Bug	[CRYPTO] Crypto_Example_002 S32DS project not working properly<*> The S32DS example project called Crypto_Example_002 provided within RTD EAR 0.8.0 patch 02 is not working as expected. Please see attached picture and next observations: The output cipher text is not the same as the expected cipher text. Variable u32NumFailedApiCalls is 2, while it should be 0. Issue can be seen using Lauterbach or P&E interface. If using P&E, just build the project with D_CACHE_ENABLE macro removed, due to current bug of P&E while reading static/global variables when data cache enabled.

ID	Subtype	Headline and Description
ARTD-2771	Bug	[CAN] IMASK must not be cleared by FlexCAN_Ip_AbortTransfer()<*> Requirement SWS_Can_00426 says that: !image-2020-10-22-19-53-35-664.png! Although interrupts have been disabled by Can_DisableControllerInterrupts() previously, the driver code always disables MB interrupt (IMAKS) by function FlexCAN_Ip_AbortTransfer() in Can_SetControllerMode(CAN_CS_STOPPED) In
ARTD-2781	Bug	[S32CC][RM] Abnormal switch from secure to nonsecure module when PID value is greater than 0x20<*> Sequence of test case: Initialize RM module Call Rm_XrdcSetProcessID function with PID value is 0x3F PID bit #5 should not be touched, as it will decide the module will use secure or non-secure mode, user should be prohibited from affecting this bit. XRDC_PID_FIELD_MASK has the value of 0x3F if the user use u8Pid with a value of 3F then the whole PID will be affected and set to 1, which is non-secure mode.
ARTD-2806	Bug	[OsIf] Change OsIf_Init(void) to OsIf_Init(void* Config) to be called with NULL_PTR<*> Add param to OsIf_Init, always validate as being NULL_PTR
ARTD-2829	Bug	[FLS] S32CC_4.4 BETA 0.9.0 Lack of DET report FLS_E_TIMEOUT in case Timeout Occur<*> #1. For Sync Mode of FLS: During verify Timeout report for Fls Job(s), , in case configured to make time out occur on Write/Erase/ Read/DLL Lock. it's lake of DET report FLS_E_TIMEOUT. #2. For Async Mode : Timeout report not implemented yet, for 2 nodes: FlsQspiAsyncWriteTimeout and FlsQspiAsyncEraseTimeout. #3. Read Job , in Qspi_Ip_Read: it's missing "break" in case STATUS_QSPI_TIME_OUT == status (see snap shot for detail)
ARTD-2906	New	New Feature [ocu] Verify and fix all the MemMap violations ,,"Problem*: Driver variables (and functions) placed in default linker sections (.data, .bss, .text, .rodata) instead of RTD specific ones (.mcal_data, .mcal_bss, .mcal_const). Impact*: Memory partitioning impact; for safety reasons the customer does not want the RTD specific data to bleed into default or other linker sections. Higher impact in Autosar applications. Why could this problem appear*: # No or inconsistent MemMap sections placed around all definitions and declarations* +. # Incorrect MemMap sections, which do not match the variable type, like:

ID	Subtype	Headline and Description
		## Initialized variable placed in NO_INIT section ## Modifyable variable placed in CONST section ## Const variable, config data, placed in VAR sections ## Zero Initilized variable, or unintialized variables placed in incorrect sections, see the attached picture. Solution: Build a test, check in the output .map file that all driver specific variables and functions are allocated in .mcal sections, not the default ones (.data, .bss, .rodata, .text) Fix all the inconsistencies. !image-2020-10-23-14-57-28-805.png!"
ARTD-2943	Bug	[CAN] Can Automatic Time Segments can not work<*> A>* Enable Can Automatic Time Segments Calculation as below: !image-2020-10-27-11-41-17-880.png! generated code reflects that the computed bitrate segments are correct but is not located on Flexcan_aCtrlConfigPB_VS_0 => Can_Init() will use unexpected bitrate configuration. [detail in attached file] TC_ID: CAN_TC_FCT_*2880 B>* Bitrate warning is not correct. It only notify when bitrate segments > computed segments. Expectation: warning should be notified incase: bitrate segments != computed segments. C> Bitrate warning *does not notify error when CanControllerPrescallerAlternate is used (due clock is enabled) && Can Automatic Time Segments Calculation is enabled-> invalid computed birate still be generated
ARTD-2967	Bug	[S32CC][RM] XrdcMasterMode is missing 1xb - Use the bus master's secure/ nonsecure attribute directly mode<*> RM(S32G2_RM_Rev2_DraftF) has stated that !image-2020-10-23-10-28-18-886.png|thumbnail! However, when i assign a core for both domains, an error occur !EB_RM.png|thumbnail! When use select XRDC_NONCORE_MASTER mode then XrdcMasterInstance, XrdcMasterPID, XrdcMasterPIDMask options should be hidden, because MDA_Wr_m_DFMT1 does not have PID bit and XrdcMasterMode is missing 1xb Use the bus master's secure/nonsecure attribute directly XrdcMasterMode is missing 1xb Use the bus master's secure/nonsecure attribute directly mode
ARTD-3018	New	New Feature [S32K344] OCU: Align '.component' to '.xdm' nodes with epd attributes stored ,,"Update .component file used for Design Studio CT AUTOSAR/nonAUTOSAR version with: align the nodes and tree structure with xdm file used in EB Tresos use same names; run the epd2ct executable to add option attributes to .component file procedure desribed in Chapter 9 in [link|https://teams.microsoft.com/l/file/C3F9B9A6-C039-4BA5-AFC3-FE18D8BB7208?tenantId=686ea1d3-bc2b-4c6f-a92c-d99c5c301635&fileType=pptx&objectUrl=https%3A%2F%2Fnxp1.sharepoint.com%2Fsites%2FZebra%2FShared%20Documents%2FConfiguration%20(code%2C%20DS%2C%20EB%2C%20etc)%2FNXP_RTD_AUTOSAR_UCT.pptx&baseUrl=https%3A%2F%2Fnxp1.sharepoint.com%2Fsites

ID	Subtype	Headline and Description
		%2FZebra&serviceName=teams&threadId=19:e451c595d3ba410c8f9c1f5efc19a8a3@thread.tacv2& a4d2-ad54e86f727f] The updated .component will be used afterwards for epd / epc generation for import / export actions."
ARTD-3026	Bug	[S32DS 3.3 Update1] Error when enable the flexcan_43 component<*> Steps: # Enable flexcan_43 component # Add a new item to the FlexCAN configurations array # Check the log file. There is an error related to some expressions that couldn't be resolved: !ENTRY com.nxp.swtools.common.utils.expression 4 0 2020-10-27 14:59:15.245 !MESSAGE [DATA] Error resolving: (($configSet.flexcanCfg.pe_clock_frequency.getValue() / ((($parent.flexcan_cfg_preDivider.getValue() 1) (((4 $parent.flexcan_cfg_propSeg.getValue()) $parent.flexcan_cfg_phaseSeg1.getValue()) $parent.flexcan_cfg_phaseSeg2.getValue())) (0r1000))) < 1001), Value of: $configSet.flexcanCfg.pe_clock_frequency not found !ENTRY com.nxp.swtools.common.utils.expression 4 0 2020-10-27 14:59:15.551 !MESSAGE [DATA] Error resolving: $parent.pattern.getValue().toString().formatMessage(($configSet.flexcanCfg.pe_clock_frequency.getV ((($parent.flexcan_cfg_preDivider.getValue() 1) (((4 $parent.flexcan_cfg_propSeg.getValue()) $parent.flexcan_cfg_phaseSeg1.getValue()) $parent.flexcan_cfg_phaseSeg2.getValue())) (0r1000)))), Value of: $configSet.flexcanCfg.pe_clock_frequency not found!ENTRY com.nxp.swtools.common.utils.expression 4 0 2020-10-27 14:59:15.558 !MESSAGE [DATA] Error resolving: $parent.pattern.getValue().toString().formatMessage(($configSet.flexcanCfg.pe_clock_frequency.getV ((($parent.flexcan_cfg_preDivider.getValue() 1) (((3 $parent.flexcan_cfg_propSeg.getValue()) $parent.flexcan_cfg_phaseSeg1.getValue()) $parent.flexcan_cfg_phaseSeg2.getValue())) (0r1000)))), Value of: $configSet.flexcanCfg.pe_clock_frequency not found
ARTD-3049	Bug	[SENT] Flexio_Sent_Ip_GetSerialMsgData missed serial message on multiple of channel<*> When the number of channel which received serial message continuously is upper than 2 channels, Flexio_Sent_Ip_GetSerialMsgData always missed serial message on later channels. The issue comes from serial message handling on channels in sequentially.* In-while processing of the first channel, the sencond channel is in idle state, compare register of the timer can not update the timer value from SENT signal. This one causes missing serial message on the second channel. To solve this issue, I propose another way to handle serial message: Using interrupt of timer to trigger saving timer value to a virtual buffer on every channel (global variable: g_flexioTimerBuffer). Flexio_Sent_Ip_GetSerialMsgDaata calls enable/disable timer interrupt to use interrupt. the algorithm of serial message will apply on g_flexioTimerBuffer, instead of timer register as present driver.
ARTD-3073	New	New Feature [Crypto] Handling timeout implementation using OsIf

ID	Subtype	Headline and Description

		,,"Add a referenceable enum in Tresos for OsIf that can be used by other drivers to allow selection only of available osif counter types
		
		In each module configuration that needs to implement a timeout add the following field
		<v:var name=""<Module>TimeoutMethod"" type=""ENUMERATION"">
		<a:a name=""LABEL"" value=""<Module> Timeout Method""/>
		<a:a name=""DESC"">
		<a:v>
		<![CDATA[EN:
		<html>
		 <Module>TimeoutMethod
		 Configures the timeout method.
		 Based on this selection a certain timeout method from OsIf will be used in the driver.
		 Note: If SystemTimer or CustomTimer are selected make sure the corresponding timer is enabled in OsIf General configuration.
		Note: Implementation Specific Parameter.
		</html>
		]]>
		</a:v>
		</a:a>
		<a:a name=""IMPLEMENTATIONCONFIGCLASS""
		type=""IMPLEMENTATIONCONFIGCLASS"">
		<icc:v vclass=""PreCompile"">VariantPreCompile</icc:v>
		<icc:v vclass=""PostBuild"">VariantPreCompile</icc:v>
		</a:a>
		<a:a name=""ORIGIN"" value=""M4_XDM_AR_MODULE_ORIGIN""/>
		<a:a name=""SCOPE"" value=""LOCAL""/>
		<a:a name=""SYMBOLICNAMEVALUE"" value=""false""/>
		<a:a name=""UUID"" value=""ECUC:7228a335-4003-4639-8e1a-bb3d9f762a7b""/>
		<a:a name=""DEFAULT"" value=""DummyTimer""/>
		<a:da name=""INVALID"" type=""XPath"">
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseCustomTimer') = 'false' and node:fallback(.,'DummyTimer') = 'CustomTimer'"" true=""Custom Timer is not enabled in OsIf (OsIfGeneral/OsIfUseCustomTimer checkbox)""/>
		<a:tst expr=""node:refs('ASPathDataOfSchema:/M4_XDM_AR_PKG_NAME/Base/OsIfGeneral/OsIfUseSystemTimer') = 'false' and node:fallback(.,'DummyTimer') = 'SystemTimer'"" true=""System Timer is not enabled in OsIf (OsIfGeneral/OsIfUseSystemTimer checkbox)""/>
		</a:da>
		<a:da name=""RANGE"">
		<a:v>DummyTimer</a:v>
		<a:v>SystemTimer</a:v>
		<a:v>CustomTimer</a:v>
		</a:da>
		</v:var>
		Based on its configuration generate an enum field of the type OsIf_CounterType (which is defined in OsIf.h and described below)
		// This is defined in OsIf.h
		typedef enum
		{
		OSIF_COUNTER_DUMMY, /**< dummy counter /
		#if (OSIF_USE_SYSTEM_TIMER == STD_ON)
		OSIF_COUNTER_SYSTEM, /**< system counter /
		#endif / (OSIF_USE_SYSTEM_TIMER == STD_ON) /
		#if (OSIF_USE_CUSTOM_TIMER == STD_ON)
		OSIF_COUNTER_CUSTOM /**< custom counter /

ID	Subtype	Headline and Description

		#endif / (OSIF_USE_CUSTOM_TIMER == STD_ON) /
		} OsIf_CounterType;
		Use the generated value of the type described above to use the OsIf APIs for implementing timeouts:
		// Defined in OsIf.h
		/*!
		brief Get the current value counter
		This function returns the current value of the counter.
		param[in] SelectedCounter the type of counter to use
		return the current value of the counter
		/
		uint32 OsIf_GetCounter(OsIf_CounterType SelectedCounter);/*!
		brief Get the elapsed value from a reference point
		This function returns the delta time in ticks compared to a reference, and updates the reference.
		param[inout] CurrentRef reference counter value, updated to current counter value
		param[in] SelectedCounter the type of counter to use
		return the elapsed time
		/
		uint32 OsIf_GetElapsed(uint32 const CurrentRef, OsIf_CounterType SelectedCounter);/*!
		brief Set a new frequency used for time conversion (microseconds to ticks)
		This function stores a new timer frequency used for time conversion computations
		param[in] Freq the new frequency
		param[in] SelectedCounter the type of counter to use
		/
		void OsIf_SetTimerFrequency(uint32 Freq, OsIf_CounterType SelectedCounter);/*!
		brief Convert microseconds to ticks
		This function converts a value from microsecond units to ticks units.
		param[in] Micros microseconds value
		param[in] SelectedCounter the type of counter to use
		return the equivalent value in ticks
		/
		uint32 OsIf_MicrosToTicks(uint32 Micros, OsIf_CounterType SelectedCounter);
		Implementation example from GMAC (only an example, not a guideline)
		/*FUNCTION
		Function Name : GMAC_StartTimeout
		Description : Checks for timeout condition
		END**********/
		void GMAC_StartTimeout(uint32 startTimeOut,
		uint32 elapsedTimeOut,
		uint32 timeoutTicksOut,
		uint32 timeoutUs)
		{
		startTimeOut = OsIf_GetCounter(GMAC_TIMEOUT_TYPE);
		elapsedTimeOut = 0U;
		timeoutTicksOut = OsIf_MicrosToTicks(timeoutUs, GMAC_TIMEOUT_TYPE);
		}/*FUNCTION
		Function Name : GMAC_TimeoutExpired
		Description : Checks for timeout expiration condition
		END**********/
		boolean GMAC_TimeoutExpired(uint32 startTimeInOut,
		uint32 elapsedTimeInOut,
		uint32 timeoutTicks)
		{
		elapsedTimeInOut = OsIf_GetElapsed(startTimeInOut, GMAC_TIMEOUT_TYPE);
		return ((*elapsedTimeInOut >= timeoutTicks)? TRUE : FALSE);
		}

ID	Subtype	Headline and Description

		/ Usage /
		uint32 startTime, elapsedTime, timeoutTicks;
		uint32 timeoutUs = 100U;
		/ Wait for completion /
		GMAC_StartTimeout(&startTime, &elapsedTime, &timeoutTicks, timeoutUs);
		do
		{
		if ((base->MAC_MDIO_ADDRESS & GMAC_MAC_MDIO_ADDRESS_GB_MASK) == 0U)
		{
		status = GMAC_STATUS_SUCCESS;
		break;
		}
		} while (!GMAC_TimeoutExpired(&startTime, &elapsedTime, timeoutTicks));
		
		"

ARTD-3091	Bug	 [IP_FLEXCAN][FLEXCAN_IP_002_002] FlexCAN_Ip_SetBitrateCbt should return error in case disabled fd<*> TC_ID: *Ip_FlexCAN*_TC_FCT_*2063 init flexcan with disabled FD call FlexCAN_Ip_SetBitrateCbt > verification point: FlexCAN_Ip_SetBitrateCbt should return FLEXCAN_STATUS_ERROR => fail due to wrong condition expression: !image-2020-10-29-11-25-46-191.png! Additional: the call of FlexCAN_Ip_SetBitrateCbt on HLD should be updated also after above issue is fixed
ARTD-3092	Bug	 [S32G274] OCU: remove all tabulators in source files<*> remove all tab characters in all file, follow the table below: *File*||*Hits Ftm_Ocu_Ip.c|774 Ftm_Ocu_Ip_Irq.c|69 Ocu.c|49 Ftm_Ocu_Ip_PBcfg.c|48 Ocu_PBcfg.c|40 Ftm_Ocu_Ip_Types.h|28 Ftm_Ocu_Ip_PBcfg.h|12 Ocu_Ipw_PBcfg.h|12 Ocu_Cfg.h|12 !image-2020-10-29-11-28-33-300.png!
ARTD-3101	Bug	 [LIN] LIN cannot transmit and receive frame correctly<*> Description: 1.The current LinDriver cannot send frame with PID higher than 0x3F. The correct behavior should be LinDriver cannot send frame with ID higher than 0x3F.

ID	Subtype	Headline and Description

		LIN driver need check invalid ID instead of PID and call
		Lpuart_Lin_Ip_MasterSendHeader() with parameter is ID (Lin_Ipw_SendResponse()
		and Lin_Ipw_SendHeader() in Lin_Ipw.c).
		2.The current LinDriver cannot return the correct recived data from frame via
		Lin_GetStatus() function if driver doesn't use LPUART0
		In Lin_Ipw_HardwareGetStatus() the code should be:
		
		for (u8Indx = 0U; u8Indx < Lin_Ipw_eCurrentDataLength[u8Channel]; u8Indx++)
		Instead of:
		for (u8Indx = 0U; u8Indx < Lin_Ipw_eCurrentDataLength[u8HwUnit]; u8Indx++)
		3. the function Lin_GetStatus() does not return LIN_RX_ERROR or LIN_TX_ERROR if
		framing error happens in bus
		In Lin_Ipw_HardwareGetStatus() the code should be:
		/ Frame error in transmission occured /
		else if ((LIN_FRAMING_ERROR == u8FrameError) &&
		(LIN_TX_MASTER_RES_COMMAND == u8TransmitHeaderCommand))
		{
		u8ReturnStatus = LIN_TX_ERROR;
		}
		/ Frame error in reception occured /
		else if ((LIN_FRAMING_ERROR == u8FrameError) &&
		(LIN_TX_SLAVE_RES_COMMAND == u8TransmitHeaderCommand))
		instead of:
		/ Frame error in transmission occured /
		else if ((LIN_FRAME_ERROR == u8FrameError) &&
		(LIN_TX_MASTER_RES_COMMAND == u8TransmitHeaderCommand))
		{
		u8ReturnStatus = LIN_TX_ERROR;
		}
		/ Frame error in reception occured /
		else if ((LIN_FRAME_ERROR == u8FrameError) &&
		(LIN_TX_SLAVE_RES_COMMAND == u8TransmitHeaderCommand))
		4. Driver cannot send frame which has ID 0x3F in bus.
		In Lin_Ipw_SendHeader() and Lin_Ipw_SendResponse() the checking code should be:
		0x3FU >= id
		Instead of:
		0x3FU > id
		
		Proposal solution:
		Please see attached file for more information.

ARTD-3480	New	 New Feature [ETH]Fix trace ability warning ,,In trace ability report contains some warning uncovered.
ARTD-3484	Bug	 [SENT] Missing serial message in interrupt mode<*> 1. Interrupt mode, serial message missed. The problem comes from Flexio_Sent_Ip_IRQ_Dispatch implementation: interrupt enable and interrupt flags in for loop; timer value and clear interrupt are in Flexio_Sent_Ip_IRQHandler function > decrease speed of interrupt handler Solution: Read all interrupt flag at the same time (read TIMSTAT register). Read timer value and clear interrupt flag in Flexio_Sent_Ip_IRQ_Dispatch.

ID	Subtype	Headline and Description
		2. Remove hardcode for tick time value, and get this value from user configuration. 3. Improve *Flexio_Sent_Ip_IRQHandler:* Remove some serial message checking, the current code make serial message missed in some special case. 4. Fix spurious interrupt. 5. Implement returning fast message data when call Flexio_Sent_Ip_GetSerialMsgData, Flexio_Sent_Ip_GetSerialChannelMsgData 6. Fix CRC calculating for SENT_RECOMMENDED_IMPLEMENTATION_256_ELEMENT
ARTD-3486	New	New Feature [S32K3XX] update multicore int monitor in EB ,,"Update multicore, porting from S32CC"
ARTD-3490	New	New Feature [ETH]Fix cyclomatic complexity > 20 ,,The function Eth_MainFunction has cyclomatic complexity > 20.
ARTD-3500	Bug	[Ip_Flexcan][S32_DS] Can not choose flexcan channel in case of more than one Instances<*> Create new project Add first flexcan configuration, refer to FLEXCAN_*0*, input maxmb value is 95 Add second flexcan configuration, refer it to FLEXCAN_*1 > at this step error happen at *first flexcan configuration because it refer to FLEXCAN_*1* also Expected behavior: the implementation should be done as the HLD's one, so we can map each configuration to expected Flexcan channel. I set high priority for this task since DS update will impact much to testing activities this release.
ARTD-3520	Bug	[CAN][EB] CanMainFunctionRWPeriodRef should be enabled in case of CanHardwareObjectUsesPolling/Mix<*> Two issues should be analysed A> Add Can Choose Tx/Rx Processing Type: MIXED Add one Tx or Rx hardware object Enable CanHardwareObjectUses*Polling* => CanMainFunctionRWPeriodRef need to be notified to be selected. (should have same behavior as case of Tx/Rx Processing Type is POLL*) B>* **Look at desciption of CanHwFilterMask: !image-2020-11-02-15-06-46-919.png! The highlight description (and related srs ids) is no longer applied with current implementation: CanFilterMaskRef is not be implemented now => users always need to configure mask with BASIC CanHandleType => FULL value of CanHandleType is not supported (have no meaning) anymore => the description should be updated.
ARTD-3522	Bug	[IP_Flexcan] FDCTRL_FDRATE should not be enabled by FlexCAN_Ip_Send<*> Init Flexcan with Config.bitRateSwitch = FALSE

ID	Subtype	Headline and Description
		FlexCAN_Ip_Send with tx_info.enable_brs = TRUE => brs request should be ignored in this case, normal frames should be sent, because FDCTRL_FDRATE config is on Flexcan_Init now, and FlexCAN_Ip_Send should not change module configuration by itself (additionally, this cause an extra/redundant access exclusive area each time call FlexCAN_Ip_Send !) !image-2020-11-02-15-26-15-570.png! => Flexcan_send should control BRS bit in Tx Mb, instead of controlling FDRATE bit in FDCTRL Expectation: remove below code: !image-2020-11-02-15-28-47-513.png! Additionally*: Please add below typical development error detect for FlexCAN_Ip_Init_Privileged DEV_ASSERT(instance < CAN_INSTANCE_COUNT); DEV_ASSERT(state != NULL); DEV_ASSERT(*g_flexcanStatePtr[instance] == NULL); (re-init without de-init) TC_ID: *Ip_*FlexCAN_TC_FCT*_2060
ARTD-3564	Bug	[S32G][ETH] Fix conmpiler warning<*> Fix conmpiler warning
ARTD-3579	Bug	[IP_Flexcan][FLEXCAN_IP_005_001] FlexCAN_Ip_SetRxFifoGlobalMask now set literal user's mask<*> A> FLEXCAN_IP_005_001: A function called FlexCAN_Ip_SetRxFifoGlobalMask shall Set Rx FIFO global mask as the 11-bit standard mask or the 29-bit extended mask*. > This description is no longer applied in Zebra due to the implementation was changed (see attached file) Expectation: update description in header file and requirement (should be similar as the description FlexCAN_Ip_SetRxIndividualMask) B>* For now: FlexCAN_Ip_Set*RxMb*GlobalMask: Set Rx Message Buffer global mask as the 11-bit standard mask or the 29-bit extended mask (calculated mask) FlexCAN_Ip_Set*RxFifo*GlobalMask: Sets FlexCAN Rx FIFO literal mask FlexCAN_Ip_Set*RxIndividual*Mask: Sets FlexCAN Rx individual literal mask FlexCAN_Ip_Set*RxIndividual*MaskCalc: Sets FlexCAN Rx individual calculated mask* => please see how the names of APIs can lead to confuses. and currently, Set*RxMb*GlobalMask is supported as calculated mask Set*RxFifo*GlobalMask is not supported as calculated mask! Expectation*: need to analysis and finalize the clear API showcase that will come to users
ARTD-3585	Bug	[S32K3]SIUL2 Config Tool PORT defines mismatch RTD Siul2_Dio_Ip_Cfg.h<*> Config Tool defines for the user pin and port configurations macros to be used further in the application development. However, the macro value for each PORT differs from the ones defined in RTD. For example, RTD defines port as PTB_H_HALF and PTB_L_HALB while the Config tools generates output port as simply PTB. Siul2_Port_Ip_Cfg.h

ID	Subtype	Headline and Description
		#define RGBLED0_RED_PIN 13u #define RGBLED0_RED_PORT PTB Siul2_Dio_Ip_Cfg.h #define PTA_L_HALF ((GPIO_Type)(&(SIUL2->PGPDO0))) #define PTA_H_HALF ((GPIO_Type)(&(SIUL2->PGPDO1))) #define PTB_L_HALF ((GPIO_Type)(&(SIUL2->PGPDO2))) #define PTB_H_HALF ((GPIO_Type)(&(SIUL2->PGPDO3))) !image-2020-11-03-13-23-39-737.png!!image-2020-11-03-13-24-05-011.png!
ARTD-3674	Bug	 [SENT] Build fail relate to name of sent controller object's pointer structure in case variant_no > 1<*> In case varian_no > 1, SENT gets this error in build step: In file included from ../../../output/S32K3XX_S32K344/sent/Sent_TS_001_cfgPB/generate/src/Sent_VS_1_PBcfg.c:90: ../../../output/S32K3XX_S32K344/sent/Sent_TS_001_cfgPB/generate/include/Sent_Ipw_Cfg.h:98:5: error: unknown type name 'SENT_IPW_CONFIG_VS_1_PB'; did you mean 'SENT_IPW_CONFIG_VS_0_PB'? 98 SENT_IPW_CONFIG_VS_1_PB \ Solution: Need to change name of controller pointer structure following by postBuildVariant. Flexio_aCtrlConfig > Flexio_aCtrlConfigPB[!IF "var:defined('postBuildVariant')"!]_[!"$postBuildVariant"!][!ENDIF!] Sent_Ipw_aCtrlConfig > Sent_Ipw_aCtrlConfigPB[!IF "var:defined('postBuildVariant')"!]_[!"$postBuildVariant"!][!ENDIF!]
ARTD-3678	New	 New Feature [SPI] Support FlexIO ,,Support FlexIO
ARTD-3691	New	 New Feature [SENT] Update resource for SENT driver ,,"Update resource names. Sent_s32k314_mapbga257 Sent_s32k314_mqfp100 Sent_s32k314_mqfp172 Sent_s32k324_mapbga257 Sent_s32k324_mqfp172 Sent_s32k344_mapbga257 Sent_s32k344_mqfp172 Update resource content: Sent.SentConfigSet.SentControllerConfig:1 Sent.SentConfigSet.SupvAvailable:STD_ON Sent.SentConfigSet.SentHwUnderRegProtList:SENT_FLEXIO_0 Sent.SentConfigSet.SentControllerConfig.SentChannelConfig:8 Sent.SentConfigSet.SentControllerConfig.SentHwController:FLEXIO_0 Sent.SentConfigSet.SentControllerConfig.SentHwChannel:CHANNEL_0,CHANNEL_1,CHANNEL_2, Sent.SentConfigSet.SentControllerConfig.SentPinID:PIN_0,PIN_1,PIN_2,PIN_3,PIN_4,PIN_5,PIN_6,
ARTD-3704	New	 New Feature

ID	Subtype	Headline and Description
		[I2C][S32K3XX] Add SlaveListening function for K3 ,,SlaveListening functions should be available for S32K3XX platform.
ARTD-3782	Bug	[build_env] The interrupt vector table can be overwriten when there is a variable define in no-cacheable section<*> !image-2020-11-09-13-30-28-402.png! As in the highlight picture, the size of .intc_vector_ram will be zero so it's address will be same as starting address of .mcal_data_no_cacheable. Currently the issue occur on gcc, please also check with iar.
ARTD-3790	Bug	[FEE]: Some variables are placed in different sections<*> Fee_ClrGrps and Fee_BlockConfig are placed in different section in generated files: are placed in FEE_START_SEC_CONFIG_DATA_UNSPECIFIED in Fee_Cfg.c in FEE_START_SEC_CONST_UNSPECIFIED in Fee_Cfg.h
ARTD-3819	New	New Feature [FLS][S32K3XX-4.4] Update Test List ,,Fls Update Test list
ARTD-3822	Bug	[MCU] There are no warnings/errors when system clock doesn't have the correct ratios<*> There are no warnings/errors when system clock is not respect follow ratio (the same issue for CORE and HSE clocks) !image-2020-11-10-14-30-24-471.png|width=689,height=456!
ARTD-3843	New	New Feature [PORT] Add support for USER MODE for S32K3 BETA 0.9.0 ,,Add support for USER MODE for S32K3 BETA 0.9.0. Refer the implementation from S32XX platform
ARTD-3897	Bug	[SENT][S32K344 BETA] The first FAST message which received from MAF always missed<*> The issue is that: The first SENT message which received from MAF always missed when the ticktime 10us and the FLEXIO's freq = 80Mhz. The root cause: The time counter start as soon as SENT initialized, this one causes the Time Compare gets a random value when detect a falling edge from MAF (calibration pulse). If this Time Compare value = SYNC_CAL_TICK 25% (this occurs when ticktime 10us and the FLEXIO's freq = 80Mhz in my test), the second Time Compare value (time for calibration pulse) will be rejected and it will be ignore the first Fast message and it mean the first Serial message will be missed also. Solution:

ID	Subtype	Headline and Description
		To prevent this issue, the time counter must start only when detect a falling edge. It means TIMENA = 0x7 (Timer enabled on Trigger rising or falling edge) when configure TIMCFG register
ARTD-3898	Bug	[ETH] Build failed related to names of interrupts<*> The name of interrupt should be changed to EMAC in stead of ENET
ARTD-3906	New	New Feature [FLS] Update eec feature for internal flash ,,Update ecc feature for internal flash
ARTD-3923	Bug	[S32K344][ADC] Wrong index range of list and can not select ADC channel for LIST conversion mode<*> Detailed description (how to reproduce it): Wrong index range of list and can not select ADC channel for LIST conversion mode. List Index range: 0-31 but config in EB 0-23. Details are in the attached file. Preconditions: Config ADC in BCTU mode. Select trigger conversion mode is LIST Can not select ADC channel. Observed behavior: Wrong index range of list and can not select ADC channel for LIST conversion mode. Expected behavior: Incorrect index range of list (0-31) and can select ADC channel for LIST conversion mode. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-3927	Bug	[SENT][S32K344 BETA] Fix build fail on GHS compiler<*> Fix all build fails on GHS compiler
ARTD-3929	Bug	[S32K3XX] ADC: Adc_SetChannel calling before Adc_Init cause hard fault error<*> Detailed description (how to reproduce it): Adc_SetChannel calling before Adc_Init cause hard fault error (Adc_GroupType GroupIndex = Adc_pCfgPtr[u32CoreId]- >pGroupIdToIndexMap[Group]; out of checking StatusChecks == E_OK) Preconditions: Adc_SetChannel is enable Compiler IAR Test Case ID (internal TC that caught the defect) optional: Adc_TC_FCT_1103 Observed behavior: / Call the Adc_SetChannel before initial driver / Adc_SetChannel(t_u16AdcGroupType, t_g_pAdcChannel[t_u16AdcGroupType], T_ADC_MAX_CHANNEL_COUNT);

ID	Subtype	Headline and Description
		/ [CPR_RTD_00329.adc] Verification point: Det error ADC_E_UNINIT / EU_ASSERT_FATAL(Det_TestLastReportError(ADC_MODULE_ID, 0U, ADC_SETCHANNEL_ID, ADC_E_UNINIT)); > cause hard fault errors Expected behavior: Hard fault does not occur Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: NA
ARTD-3944	Bug	[SENT] Sent_Init gets build fail in case precompile+nopartition+variantno>1<*> Condition: Precompile No partition Variant no >=1 Issue: "e:/gitwork/Zerba/S32K3XX_4.4_noSASW/output/S32K3XX_S32K344_ghs/sent/../../eclipse/plugins/Sent_TS_T40D34M8I1R0/src/CDD_Sent.c", line 293: error #142: expression must have pointer-to-object type if (NULL_PTR == Sent_Config[u32CoreId]) Root cause: In the mention case, the configuration variable is +const Sent_ConfigType Sent_Config +, so need to update Sent_Init function: +Sent_pConfig[u32CoreId] = pConfig;
ARTD-3945	Bug	[ETH] Multicast packages reception doesn't works<*> Controller doesn't work at multicast filtering modes
ARTD-3953	Bug	[S32K344][ADC-BCTU] Faulty reading from FIFO result when using function Adc_CtuReadFifoResult() to read<*> Detailed description (how to reproduce it): Faulty reading from FIFO result when using function Adc_CtuReadFifoResult() to read. Step check: Step1: Config ADC in BCTU mode. With data conversions are saved in FIFO. Step2: Call Adc_CtuReadFifoResult(), read FIFO result. Step3: the reading result is false. Incorrect channel index. Preconditions: Follow the steps above. Observed behavior: Faulty reading from FIFO result when using function Adc_CtuReadFifoResult() to read. Expected behavior: Correct reading from FIFO result when using function Adc_CtuReadFifoResult() to read. Note: in the "Expected behavior" field, please mention also the requirement source too (cPRD, Errata version, RM, CR number etc.) Proposed solution optional: [...]
ARTD-3982	Bug	[RTD_S32K344][PORT] no prototype of Siul2_Port_Ip_SetUserAccessAllowed<*> build fail at IAR compiler, error log: no prototype of Siul2_Port_Ip_SetUserAccessAllowed
ARTD-3998	Bug	[eth] Update the used schema for all the .component files to 8.0 version<*>

ID	Subtype	Headline and Description
		The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"
ARTD-4002	Bug	[spi] Update the used schema for all the .component files to 8.0 version<*> The used version for the component file from the header should be updated to 8.0 to be compatible with the S32CT framework version. If it is not updated, when the .component validation is done, will fail and the component file will not be loaded with success. xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component.xsd" should be updated to: xsi:schemaLocation="http://swtools.freescale.net/XSD/component/1.0 http://swtools.freescale.net/XSD/component/1.0/component-8.0.xsd"
ARTD-4032	New	New Feature [S32K3XX] update list test ,,Update list test
ARTD-4049	New	New Feature [SPI] Remove instance parameter of spi_Ip_Init, spi_Ip_SyncTransmit and spi_Ip_AsyncTransmit" ,,"Currently, some functions are declared as below: Lpspi_Ip_StatusType Lpspi_Ip_Init(uint32 instance, const Lpspi_Ip_ConfigType Configuration); Lpspi_Ip_StatusType Lpspi_Ip_SyncTransmit(uint32 instance, const Lpspi_Ip_ExternalDeviceType externalDevice, void txBuffer, void rxBuffer, uint16 numberOfFrames, uint32 timeout); Lpspi_Ip_StatusType Lpspi_Ip_AsyncTransmit(uint32 instance, const Lpspi_Ip_ExternalDeviceType externalDevice, void txBuffer, void rxBuffer, uint16 numberOfFrames, Lpspi_Ip_CallbackType callback); Each instance is allocated by SpiPhyUnitMapping node on configuration tools (EB or CT) for each SpiPhyUnit. And each external device configuration is also allocated to each SpiPhyUnit. So, to avoid confusing for choise wrong instance corresponds with SpiPhyUnit and External Device configuration: instance can be stored in structures Lpspi_Ip_ConfigType and Lpspi_Ip_ExternalDeviceType. So, instance parameter can be removed.

ID	Subtype	Headline and Description
		To easy for remember structure name for each configuration. Structure name is generated by configuration tools should be added infix <Configuration Name of each configuration on EB or CT> like: const Lpspi_Ip_ConfigType Lpspi_Ip_PhyUnitConfig_<Name of Config>_<Variant name> const Lpspi_Ip_ExternalDeviceType Lpspi_Ip_DeviceAttributes_<Name of Config>_<Variant name>
ARTD-4053	New	 New Feature [ETH] Workaround relative to LDRA's issue ,,"for checking define have multiple sub expressions, these sub expression always checked parawell. This lead to build failed if the first or second sub expression not defined. ex: #if ((STD_ON == GMAC_ENABLE_USER_MODE_SUPPORT) && defined(MCAL_GMAC_REG_PROT_AVAILABLE) && (STD_ON == MCAL_GMAC_REG_PROT_AVAILABLE)) will build failed if MCAL_GMAC_REG_PROT_AVAILABLE has not defined yet."
ARTD-4367	New	 New Feature [ETH]Fix build failed on CT

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