NXP Semiconductors

Hardware Design Guidelines for S32K3xx Microcontrollers

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1 Introduction

The S32K3XX Microcontroller further extends the highly scalable portfolio of Arm® Cortex® MCUs in the automotive industry. It builds on the legacy of the S32K series, while introducing higher memory options alongside a richer peripheral set extending capability into a variety of automotive applications.

With a +2.97V – +5.5V supply and focus on automotive environment robustness, the S32K3 series devices are well suited to a wide range of applications in electrical harsh environments. These devices are optimized for cost-sensitive applications offering low pin-count options.
The purpose of this application note is to describe possible hardware considerations using the S32K3XX Microcontroller in an automotive system. It covers the most important topics such as the power considerations, Bulk/Bypass and decupling capacitors required, reset, crystal, Ethernet and QSPI configurations. Some PCB Layout recommendations are also provided.

2 Power System

Subsequent sections describe the different options for power supply configurations, as well as considerations to have for a proper connection of supply and ground pins.

2.1 S32K3XX Power Domains and Configurations

The S32K3x8 – 289MBGA and 172MaxQFP+EP, S32K344/24/14 - 257MBGA, S32K344/42/24/22/14 - 172MAXQFP and S32K342/22 - 100MAXQFP versions have two important and flexible power domains, *VDD_HV_A,VREFH* and *VDD_HV_B* that must be supplied externally at the same or different voltage level if in the application is required, and a V15 domain to +1.5V that can be supplied using an external NPN ballast transistor or externally supplied by an SBC. The S32K312-172MaxQFP and the S32K314 /12 /11-100MaxQFP versions have just a single power domain, *VDD_HV_A*. This VDD_HV_A reference will be the voltage domain for their IOs pins.

In the *Table 1* is shown all positive power pins and domains that must be supplied externally and the internal MCU references.

Table 1. S32K3XX - Power supply pins and domains

S32K3 MCU version	MCU Package	Power supply pins and domains					
		VDD_HV_A	VREFH	VDD_HV_B	V15	V25	V11
		+3.3V or +5.0V [1]	≤ VDD_HV_A	+3.3V or +5.0V[1]	+1.5V [1]	+2.5V	+1.1V
S32K328 **S32K338** **S32K348** **S32K358**	289 MBGA	Domain and Ref. voltage for I/O pins	ADC High Reference Voltage	Domain and Ref. voltage for I/O pins	Power Supply Input	Internal MCU Reference	Internal MCU Reference
	172 MaxQFP +Exposed Pad						
S32K344 **S32K324** **S32K314**	257 MBGA	Domain and Ref. voltage for I/O pins	ADC High Reference Voltage	Domain and Ref. voltage for I/O pins	Power Supply Input	Internal MCU Reference	Internal MCU Reference
S32K344 [V1.1] **S32K344 [V1.0]** **S32K342** **S32K324** **S32K322** **S32K314**	172 MaxQFP						
S32K342 **S32K322**	100 MaxQFP						
S32K312	172 MaxQFP	Domain and Ref. voltage for I/O pins	ADC High Reference Voltage	NA	NA	Internal MCU Reference	Internal MCU Reference
S32K312 **S32K311**	100 MaxQFP						
S32K311	48 LQFP	Domain and Ref. voltage for I/O pins	ADC High Reference Voltage	NA	NA	Internal MCU Reference	Internal MCU Reference
[1] Normal Operation Voltage							

- VDD_HV_A = VREFH = VDD_HV_B = +5.0V or +3.3V and V15 = +1.5V with SPMS

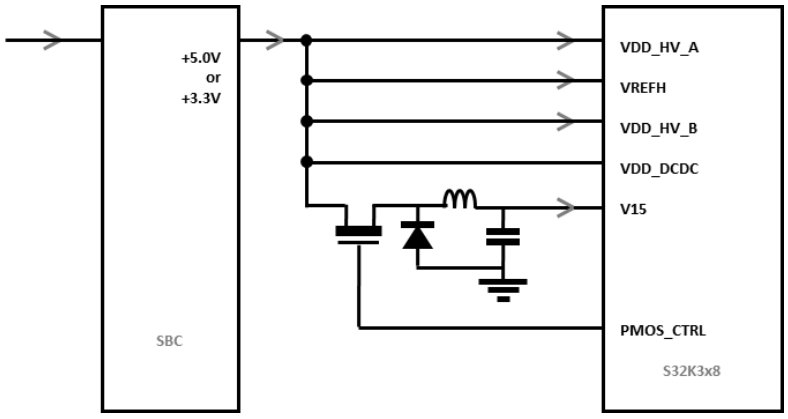


Figure 1. Block Diagram - VDD_HV_A = VREFH = VDD_HV_B = +5.0V or +3.3V, and V15 = + 1.5V with SMPS. MCU Power Configuration for S32K3x8 - 289MBGA and 172MAXQFP

- VDD_HV_A = VREFH = +5.0V, VDD_HV_B = +3.3V and V15 = + 1.5V with SMPS

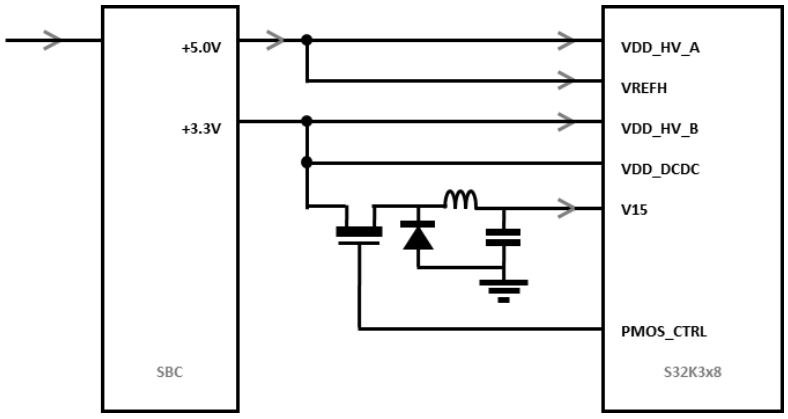


Figure 2. Block Diagram - VDD_HV_A = VREFH = +5.0V, VDD_HV_B = +3.3V and V15 = + 1.5V with SMPS. MCU Power Configuration for S32K3x8 - 289MBGA and 172MAXQFP

- VDD_HV_A = VREFH = +5.0V, VDD_HV_B = +3.3V and V15 = + 1.5V with SMPS supplied by SBC

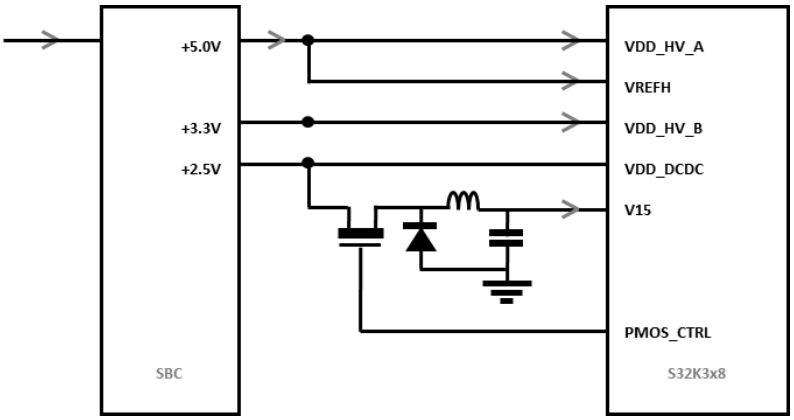


Figure 3. Block Diagram - VDD_HV_A = VREFH = +5.0V, VDD_HV_B = +3.3V and V15 = + 1.5V with SMPS supplied by SBC. MCU Power Configuration for S32K3x8 - 289MBGA and 172MAXQFP

- VDD_HV_A = VREFH = VDD_HV_B = +5.0V or +3.3V and V15 = +1.5V with external NPN Ballast Transistor

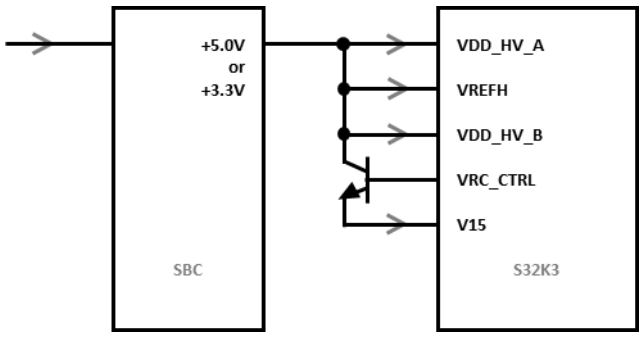


Figure 4. Block Diagram - VDD_HV_A = VREFH = VDD_HV_B = +5.0V or +3.3V, and V15 = + 1.5V with external NPN Ballast Transistor. MCU Power Configuration for S32K344/24/14 - 257MBGA, S32K344/42/24/22/14 - 172MAXQFP and S32K342/22 - 100MAXQFP

- VDD_HV_A = VREFH = VDD_HV_B = +5.0V and V15 =+1.5V

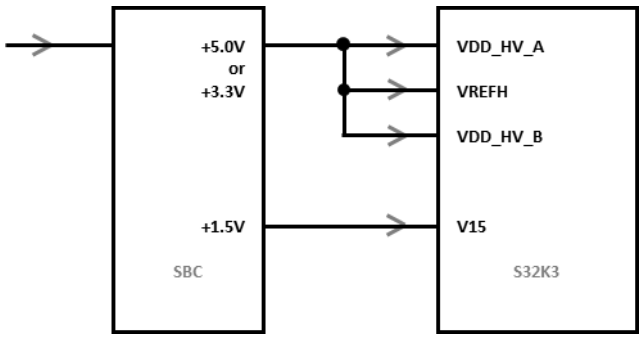


Figure 5. Block Diagram - VDD_HV_A = VREFH = VDD_HV_B = 5.0V and V15 = +1.5V - MCU Power Configuration for S32K344/24/14 - 257MBGA, S32K344/42/24/22/14 - 172MAXQFP, S32K342/22 - 100MAXQFP and S32K3x8 - 289MBGA/172MAXQFP

- VDD_HV_A = VREFH = +5.0V and VDD_HV_B = +3.3V and V15 = +1.5V with external NPN Ballast Transistor

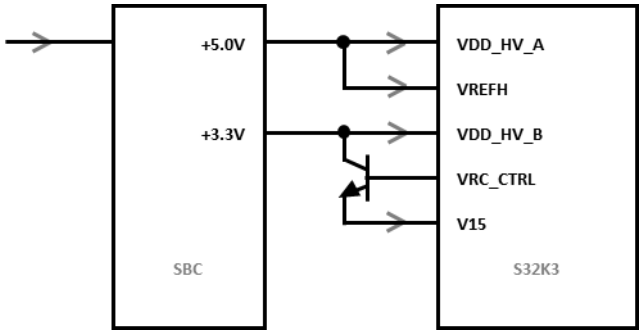


Figure 6. Block Diagram - VDD_HV_A = VREFH = +5.0V and VDD_HV_B = +3.3V and V15 = +1.5V with external NPN Ballast Transistor - MCU Power Configuration for S32K344/24/14 - 257MBGA, S32K344/42/24/22/14 - 172MAXQFP, S32K342/22 - 100MAXQFP and S32K3x8 - 289MBGA/172MAXQFP

- VDD_HV_A = VREFH = +5.0V and VDD_HV_B = +3.3V and V15 = +1.5V

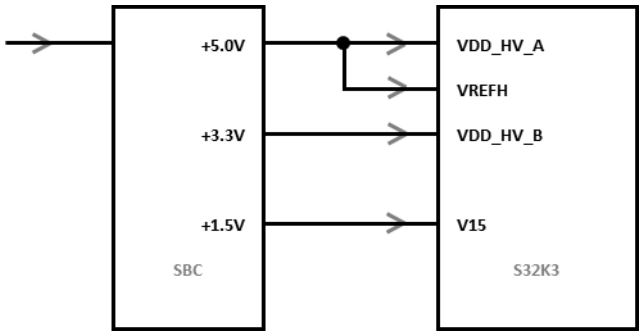


Figure 7. Block Diagram - VDD_HV_A = VREFH = +5.0V and VDD_HV_B = +3.3V and V15 = +1.5V - MCU Power Configuration for S32K344/24/14 - 257MBGA, S32K344/42/24/22/14 - 172MAXQFP, S32K342/22 - 100MAXQFP and S32K3x8 - 289MBGA/172MAXQFP

For the S32K312 - 172MAXQFP and the S32K312/11 - 100MAXQFP, just the VDD_HV_A domain and VREFH are presented.

- VDD_HV_A = VREFH = +5.0V or +3.3V

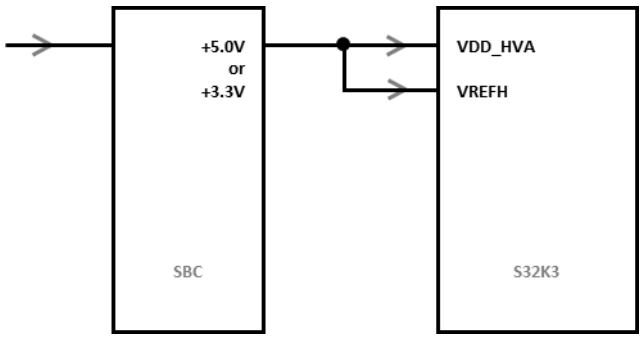


Figure 8. Block Diagram - VDD_HV_A = VREFH = +5.0V. MCU Power Configuration for S32K312 - 172MAXQFP, S32K314/12/11 - 100MAXQFP and S32K311 – 48LQFP

2.1.1 General view of the pinout and power domains for the S32K3 MCU family

In this section is shown an overview of the voltage domains for the different interfaces and I/Os in the MCU. Please refer to the latest version of the *Datasheet* and *S32K3XX_IO_Signal_Description File* for more details.

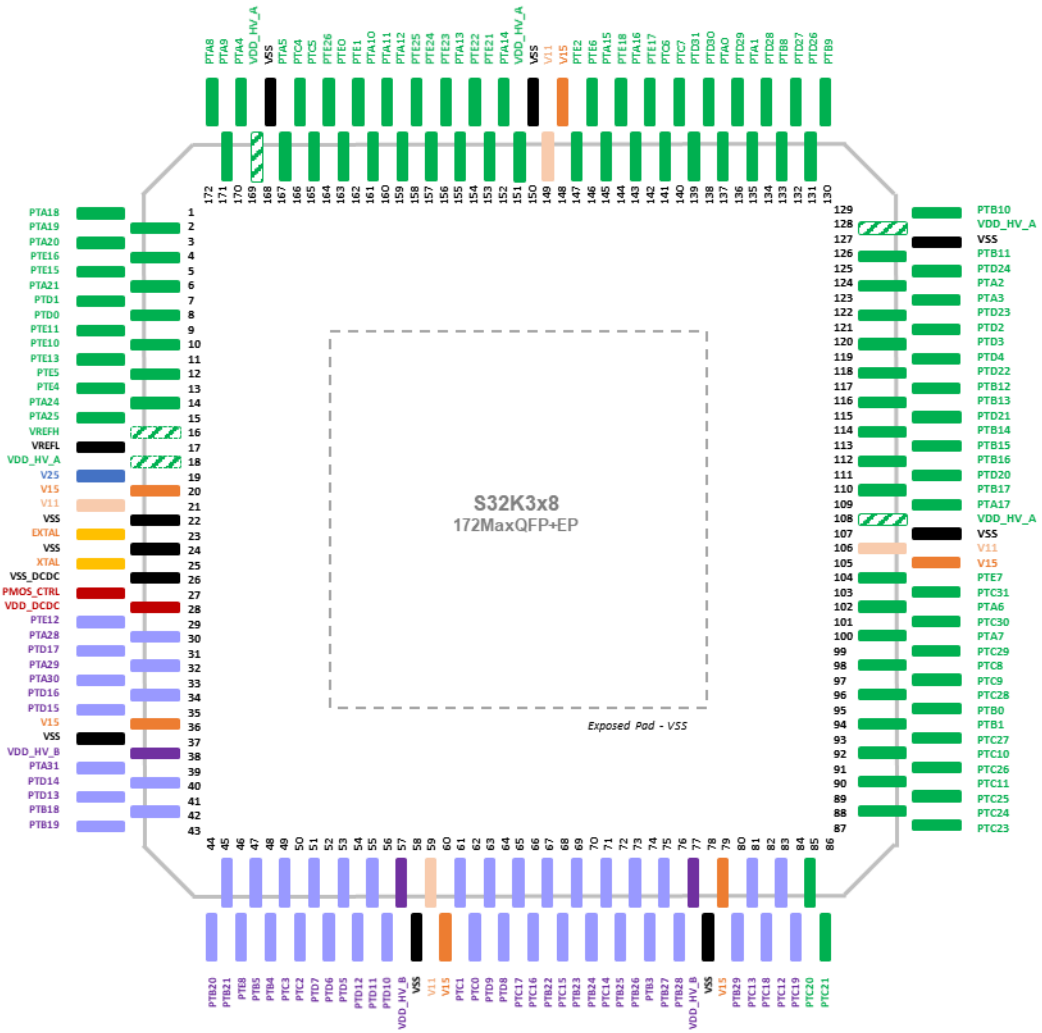
2.1.1.1 General view of the pinout and power domains for the S32K3x8 - 289MapBGA Package

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	PTG10	PTA8	PTA5	PTE30	PTE1	PTF0	PTA12	PTE24	PTA13	PTA14	PTA15	PTA16	PTA0	PTB8	PTD27	PTD26	PTG11	A
B	PTA18	VSS	PTA9	PTE31	PTE0	PTF1	PTA11	PTE25	PTE22	PTE2	PTE6	PTC7	PTD28	PTA1	PTF9	VSS	PTF10	B
C	PTA19	PTE16	PTA22	PTE28	PTE29	PTF2	PTF4	PTF5	PTF7	PTE20	PTE19	PTC6	PTD31	PTD29	PTB9	PTD25	PTB11	C
D	PTA21	PTE15	PTA23	VSS	PTE26	PTF3	PTF6	PTE23	VSS	PTF8	PTE18	PTE17	PTD30	VDD_HV_A	PTB10	PTD24	PTA2	D
E	PTE11	PTE10	PTD1	PTA20	VDD_HV_A	PTG31	PTH0	PTH1	V15	PTH2	PTH3	PTH4	VSS	PTF13	PTF12	PTA3	PTD23	E
F	PTE13	PTE5	PTD0	PTG8	PTG30	PTA4	PTC4	PTC5	PTE21	PTG27	PTG26	PTG25	PTH5	PTF15	PTF14	PTD2	PTD3	F
G	PTA24	PTG9	PTG13	PTG4	PTG29	PTE4	VSS	PTA10	PTE27	VDD_HV_A	VSS	PTG24	PTH6	PTF17	PTF16	PTD4	PTD22	G
H	PTA25	PTG1	PTG14	PTG5	PTG28	VREFH	VDD_HV_A	V15	V11	V15	PTF11	PTG23	VDD_HV_A	PTF18	PTD21	PTB13	PTB12	H
J	VSS	PTG0	PTG2	VSS	VSS_DCDC	VREFL	V25	V11	VSS	V11	PTF19	PTG22	V15	VSS	PTF20	PTB15	PTB14	J
K	EXTAL	PTG3	PTF30	PTF29	PMOS_CTRL	PTG7	PTG6	V15	V11	V15	VDD_HV_A	PTG21	PTH7	PTF21	PTD20	PTB17	PTB16	K
L	XTAL	PTA26	PTE14	PTD15	VDD_DCDC	PTG15	VSS	VDD_HV_A	PTF31	PTF28	VSS	PTG20	PTH8	PTC31	PTD19	PTD18	PTA17	L
M	PTE12	PTA27	PTA29	PTD14	VSS	PTB22	PTB23	PTG16	PTG17	PTG18	PTG19	PTF24	PTH9	PTF23	PTA6	PTA7	PTE7	M
N	PTE3	PTA28	PTD17	VDD_HV_B	VDD_HV_A	V15	VSS	V15	VDD_HV_A	VSS	PTH12	PTH11	PTH10	PTC9	PTC8	PTC29	PTC30	N
P	PTA31	PTD16	PTA30	VSS	PTD13	PTC16	PTB24	PTB25	PTB27	PTB28	PTC12	PTF25	PTF27	VSS	PTC26	PTB0	PTC28	P
R	PTB18	PTB19	PTE9	PTE8	PTD12	PTC17	VDD_HV_B	PTD8	PTB26	VDD_HV_B	PTC13	PTF26	PTC21	PTC25	PTC24	PTC27	PTB1	R
T	PTB20	VSS	PTC3	PTC2	PTD6	PTD10	VSS	PTC1	PTC14	VSS	PTB2	PTC19	PTC20	PTB31	PTC11	VSS	PTC10	T
U	PTB21	PTB5	PTB4	PTD7	PTD5	PTD11	PTC0	PTD9	PTC15	PTB3	PTC18	PTB29	PTB30	PTC23	PTC22	PTF22	PTG12	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

MCU Pin Function	#Pins
VDD_HV_A and VREFH Power Pin	10
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	183
VDD_HV_B Power Pin	3
I/Os pins on the VDD_HV_B Power Domain	52
XTAL/EXTAL	2
V25 Power Pin	1
V15 Power Pin	8
SMPS Interface for V15	2
V11 Power Pin	4
VSSx and VREFL – Ground pin	24
TOTAL of pins	289

Figure 9. General view of the pinout and power domains for the S32K3x8 - 289MapBGA Package

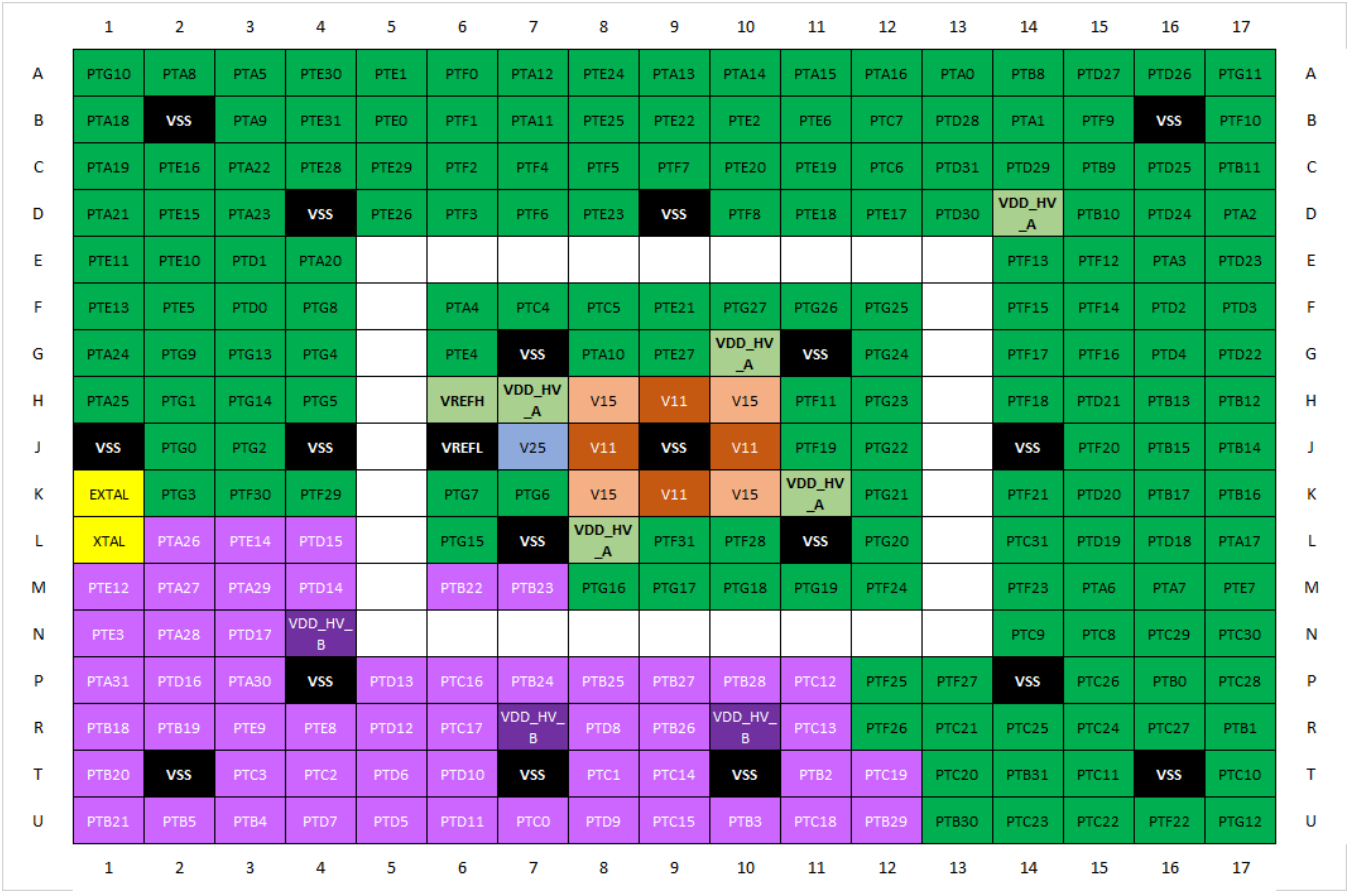
2.1.1.2 General view of the pinout and power domains for the S32K3x8 - 172MaxQFP Package



MCU Pin Function	#Pins
VDD_HV_A and VREFH Power Pin	6
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	91
VDD_HV_B Power Pin	3
I/Os pins on the VDD_HV_B Power Domain	46
XTAL/EXTAL	2
V25 Power Pin	1
V15 Power Pin	6
SMPS Interface for V15	2
V11 Power Pin	4
VSSx and VREFL – Ground pin	11
TOTAL of pins	172

Figure 10. General view of the pinout and power domains for the S32K3x8 - 172MaxQFP Package

2.1.1.3 General view of the pinout and power domains for the S32K344/24/14 – 257MapBGA Package

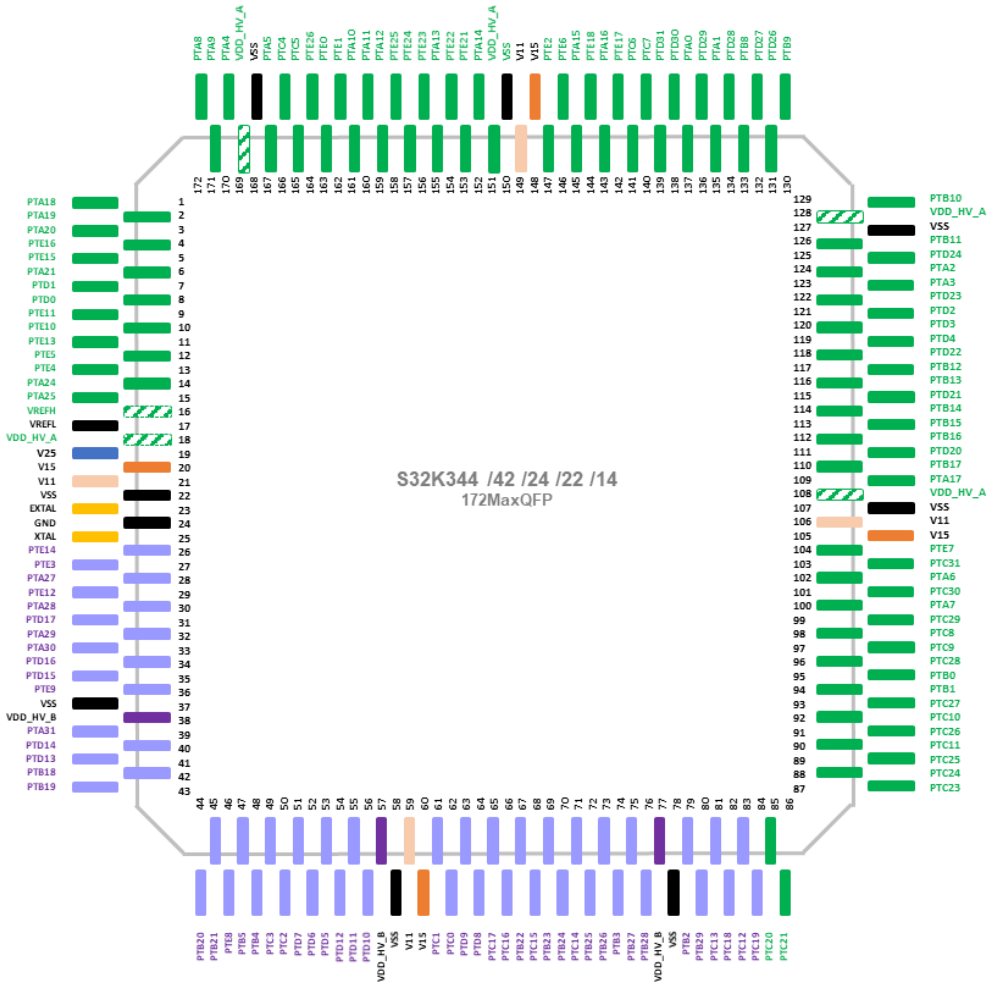


	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	PTG10	PTA8	PTA5	PTE30	PTE1	PTF0	PTA12	PTE24	PTA13	PTA14	PTA15	PTA16	PTA0	PTB8	PTD27	PTD26	PTG11	A
B	PTA18	VSS	PTA9	PTE31	PTE0	PTF1	PTA11	PTE25	PTE22	PTE2	PTE6	PTC7	PTD28	PTA1	PTF9	VSS	PTF10	B
C	PTA19	PTE16	PTA22	PTE28	PTE29	PTF2	PTF4	PTF5	PTF7	PTE20	PTE19	PTC6	PTD31	PTD29	PTB9	PTD25	PTB11	C
D	PTA21	PTE15	PTA23	VSS	PTE26	PTF3	PTF6	PTE23	VSS	PTF8	PTE18	PTE17	PTD30	VDD_HV_A	PTB10	PTD24	PTA2	D
E	PTE11	PTE10	PTD1	PTA20										PTF13	PTF12	PTA3	PTD23	E
F	PTE13	PTE5	PTD0	PTG8		PTA4	PTC4	PTC5	PTE21	PTG27	PTG26	PTG25		PTF15	PTF14	PTD2	PTD3	F
G	PTA24	PTG9	PTG13	PTG4		PTE4	VSS	PTA10	PTE27	VDD_HV_A	VSS	PTG24		PTF17	PTF16	PTD4	PTD22	G
H	PTA25	PTG1	PTG14	PTG5		VREFH	VDD_HV_A	V15	V11	V15	PTF11	PTG23		PTF18	PTD21	PTB13	PTB12	H
J	VSS	PTG0	PTG2	VSS		VREFL	V25	V11	VSS	V11	PTF19	PTG22		VSS	PTF20	PTB15	PTB14	J
K	EXTAL	PTG3	PTF30	PTF29		PTG7	PTG6	V15	V11	V15	VDD_HV_A	PTG21		PTF21	PTD20	PTB17	PTB16	K
L	XTAL	PTA26	PTE14	PTD15		PTG15	VSS	VDD_HV_A	PTF31	PTF28	VSS	PTG20		PTC31	PTD19	PTD18	PTA17	L
M	PTE12	PTA27	PTA29	PTD14		PTB22	PTB23	PTG16	PTG17	PTG18	PTG19	PTF24		PTF23	PTA6	PTA7	PTE7	M
N	PTE3	PTA28	PTD17	VDD_HV_B										PTC9	PTC8	PTC29	PTC30	N
P	PTA31	PTD16	PTA30	VSS	PTD13	PTC16	PTB24	PTB25	PTB27	PTB28	PTC12	PTF25	PTF27	VSS	PTC26	PTB0	PTC28	P
R	PTB18	PTB19	PTE9	PTE8	PTD12	PTC17	VDD_HV_B	PTD8	PTB26	VDD_HV_B	PTC13	PTF26	PTC21	PTC25	PTC24	PTC27	PTB1	R
T	PTB20	VSS	PTC3	PTC2	PTD6	PTD10	VSS	PTC1	PTC14	VSS	PTB2	PTC19	PTC20	PTB31	PTC11	VSS	PTC10	T
U	PTB21	PTB5	PTB4	PTD7	PTD5	PTD11	PTC0	PTD9	PTC15	PTB3	PTC18	PTB29	PTB30	PTC23	PTC22	PTF22	PTG12	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

MCU Pin Function	#Pins
VDD_HV_A and VREFH Power Pin	6
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	166
VDD_HV_B Power Pin	3
I/Os pins on the VDD_HV_B Power Domain	52
XTAL/EXTAL	2
V25 Power Pin	1
V15 Power Pin	4
V11 Power Pin	4
VSS and VREFL – Ground pin	19
TOTAL of pins	257

Figure 11. General view of the pinout and power domains for the S32K344/24/14 – 257MapBGA Package

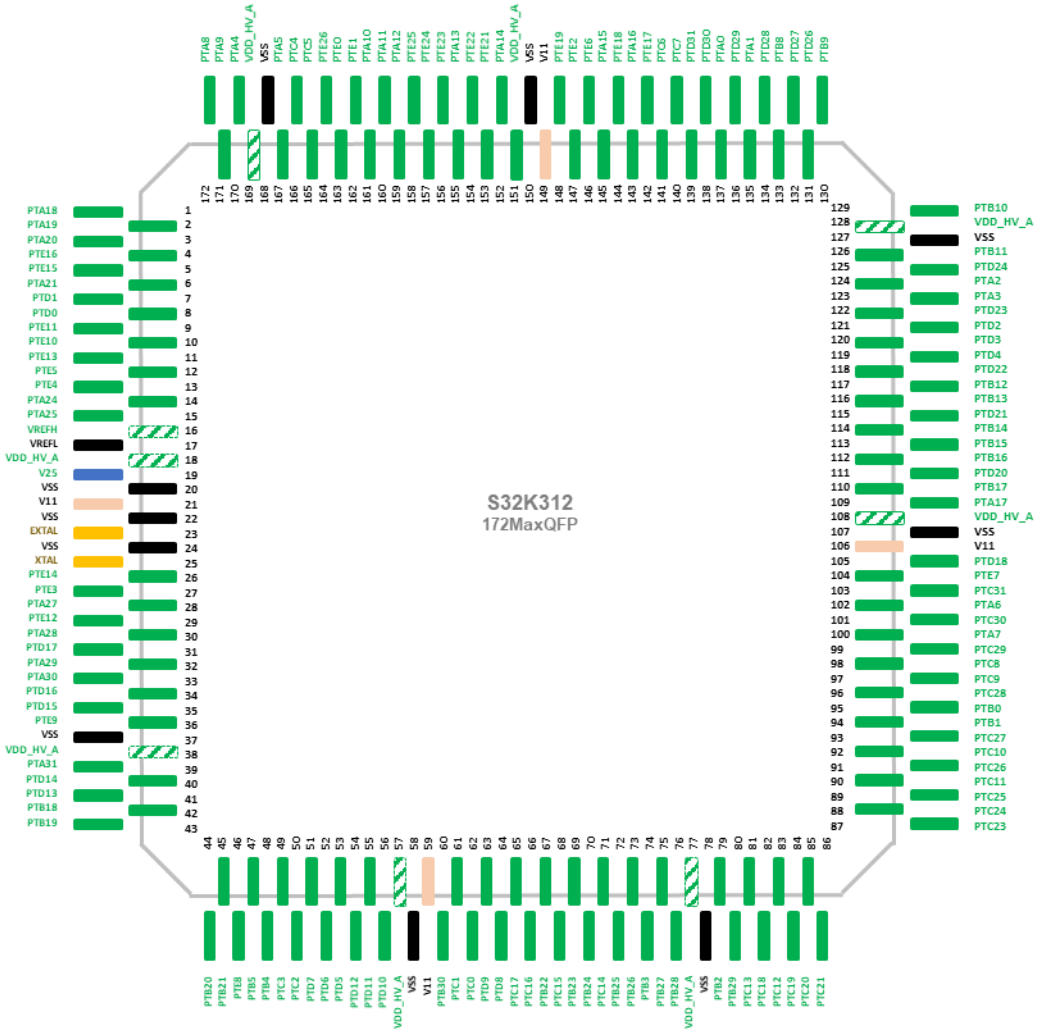
2.1.1.4 General view of the pinout and power domains for the S32K344 /42 /24 /22 /14 - 172MaxQFP Package



MCU Pin Function	#Pins
VDD_HV_A and VREFH Power Pin	6
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	90
VDD_HV_B Power Pin	3
I/Os pins on the VDD_HV_B Power Domain	52
XTAL/EXTAL	2
V25 Power Pin	1
V15 Power Pin	4
V11 Power Pin	4
VSS and VREFL – Ground pin	10
TOTAL of pins	172

Figure 12. General view of the pinout and power domains for the S32K344 /42 /24 /22 /14 - 172MaxQFP Package

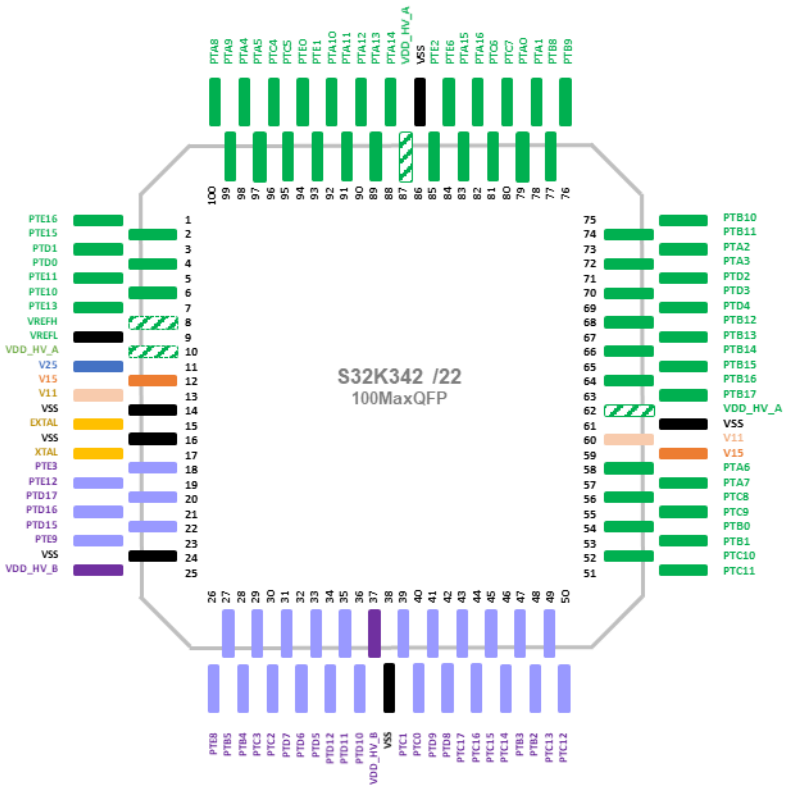
2.1.1.5 General view of the pinout and power domains for the S32K312 - 172MaxQFP Package



MCU Pin Function		#Pins
	VDD_HV_A and VREFH Power Pin	9
	I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	145
	XTAL/EXTAL	2
	V25 Power Pin	1
	V11 Power Pin	4
	VSS and VREFL – Ground pin	11
	TOTAL of pins	172

Figure 13. General view of the pinout and power domains for the S32K312 - 172MaxQFP Package

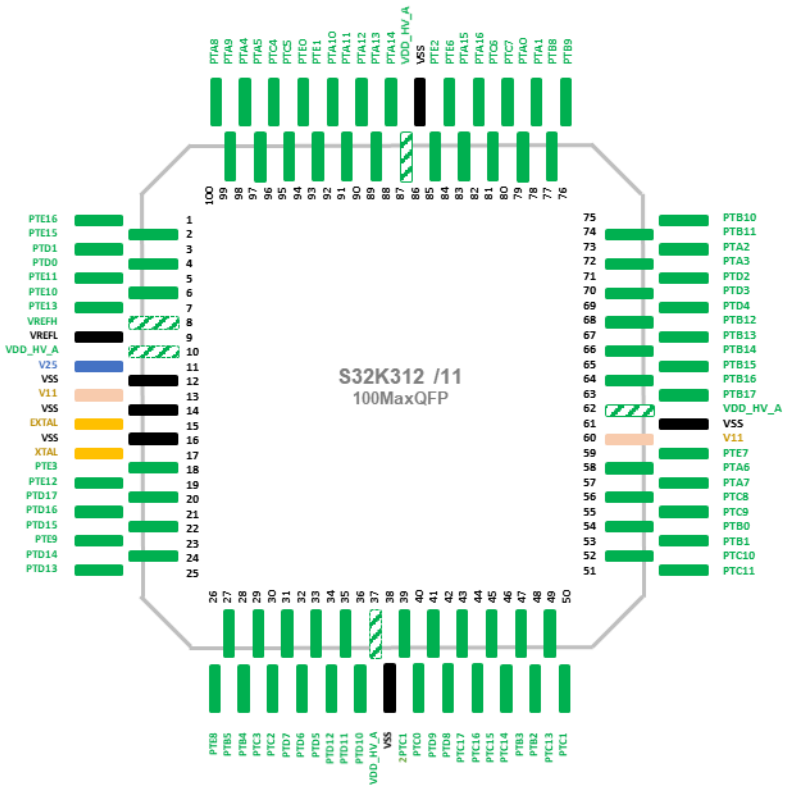
2.1.1.6 General view of the pinout and power domains for the S32K342 /22 - 100MaxQFP Package



MCU Pin Function		#Pins
	VDD_HV_A and VREFH Power Pin	4
	I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	50
	VDD_HV_B Power Pin	2
	I/Os pins on the VDD_HV_B Power Domain	30
	XTAL/EXTAL	2
	V15 Power Pin	2
	V25 Power Pin	1
	V11 Power Pin	2
	VSS and VREFL – Ground pin	7
	TOTAL of pins	100

Figure 14. General view of the pinout and power domains for the S32K342 /22 - 100MaxQFP Package

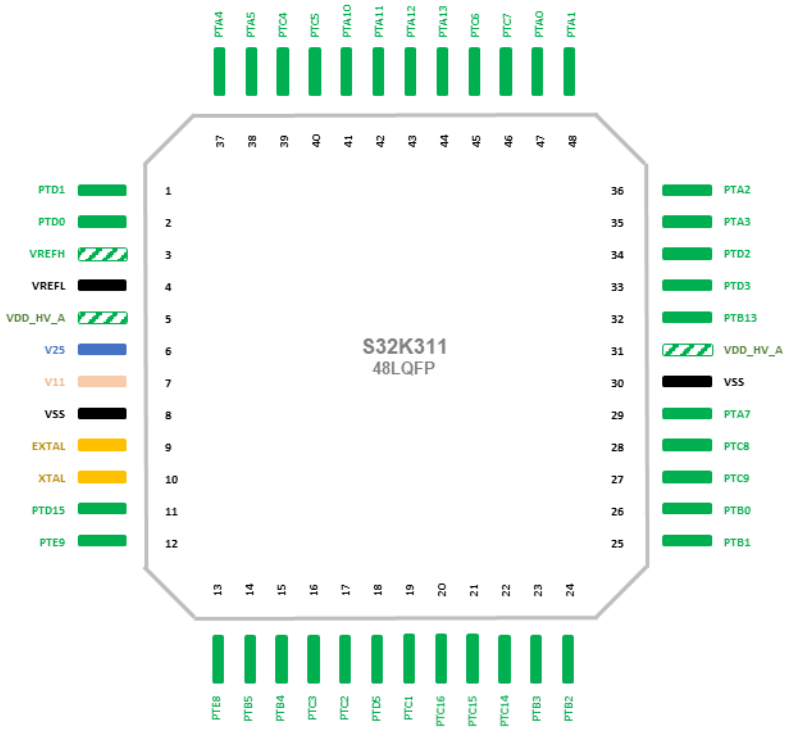
2.1.1.7 General view of the pinout and power domains for the S32K314 /12 /11 - 100MaxQFP Package



MCU Pin Function	#Pins
VDD_HV_A and VREFH Power Pin	5
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	83
XTAL/EXTAL	2
V25 Power Pin	1
V11 Power Pin	2
VSS and VREFL – Ground pin	7
TOTAL of pins	100

Figure 15. General view of the pinout and power domains for the S32K314 /12 /11 - 100MaxQFP Package

2.1.1.8 General view of the pinout and power domains for the S32K311 - 48LQFP Package



MCU Pin Function	#Pins
VDD_HV_A and VREF Power Pin	3
I/Os pins on the VDD_HV_A Power Domain [including JTAG(4) and RESET(1)]	38
XTAL/EXTAL	2
V25 Power Pin	1
V11 Power Pin	1
VSS and VREFL – Ground pin	3
TOTAL of pins	48

Figure 16. General view of the pinout and power domains for the S32K311 - 48LQFP Package

2.1.2 Bulk/Bypass and decoupling capacitors scheme for the S32K3 family

2.1.2.1 Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /289MBGA

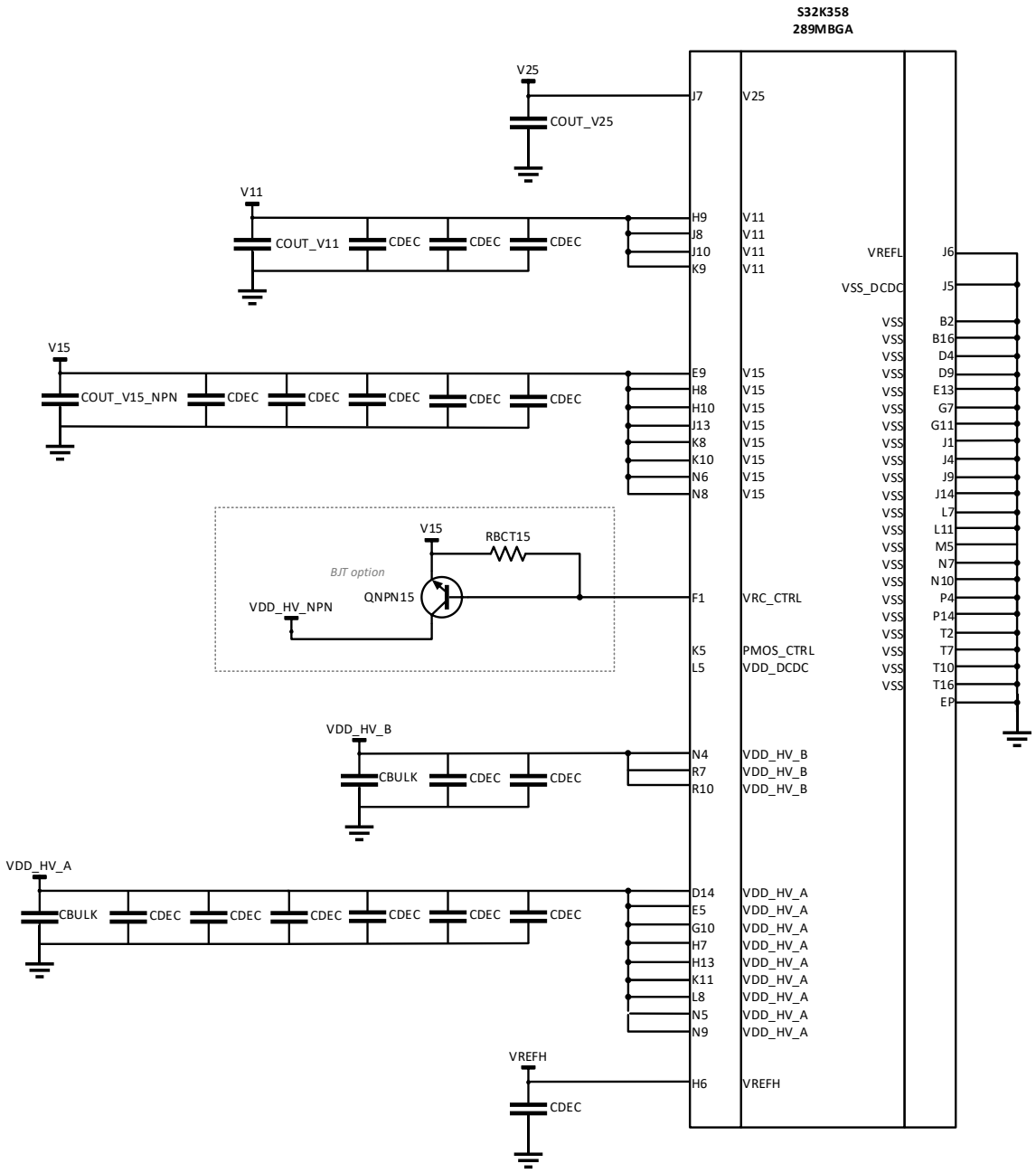


Figure 17. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /289MBGA

2.1.2.2 Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /289MBGA

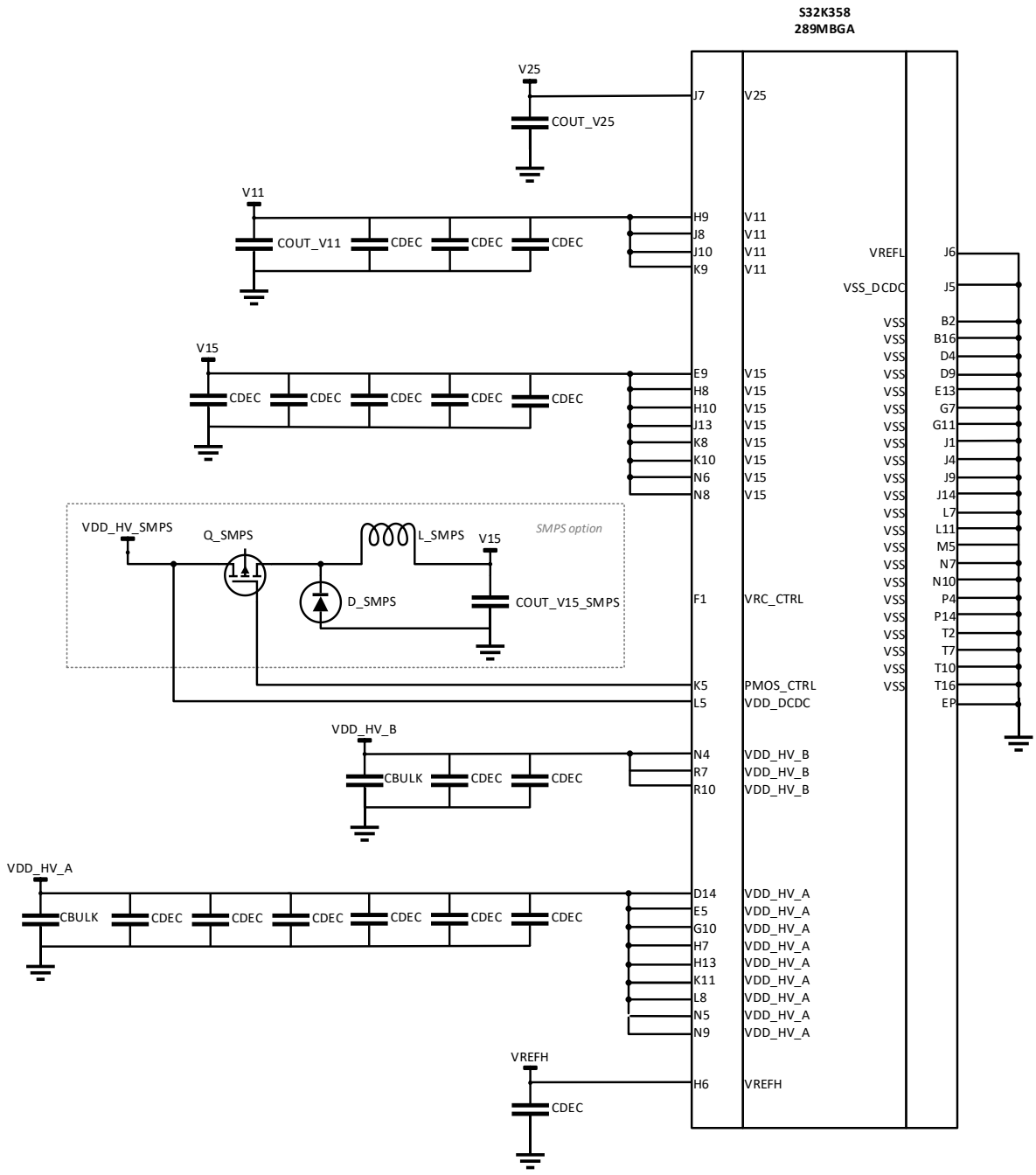


Figure 18. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /289MBGA

2.1.2.3 Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /172MaxQFP+EP

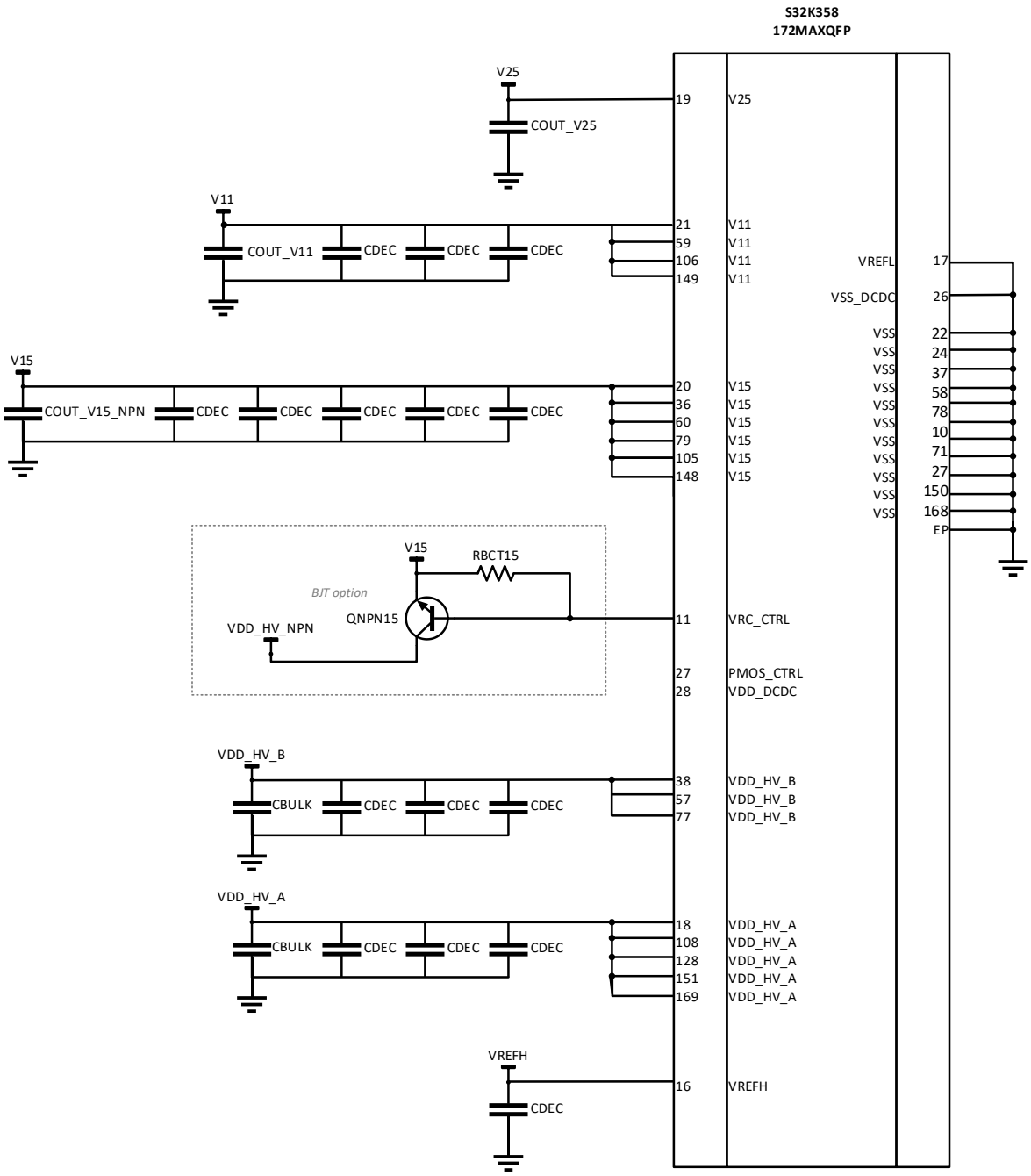


Figure 19. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /172MaxQFP+EP

2.1.2.4 Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /172MaxQFP+EP

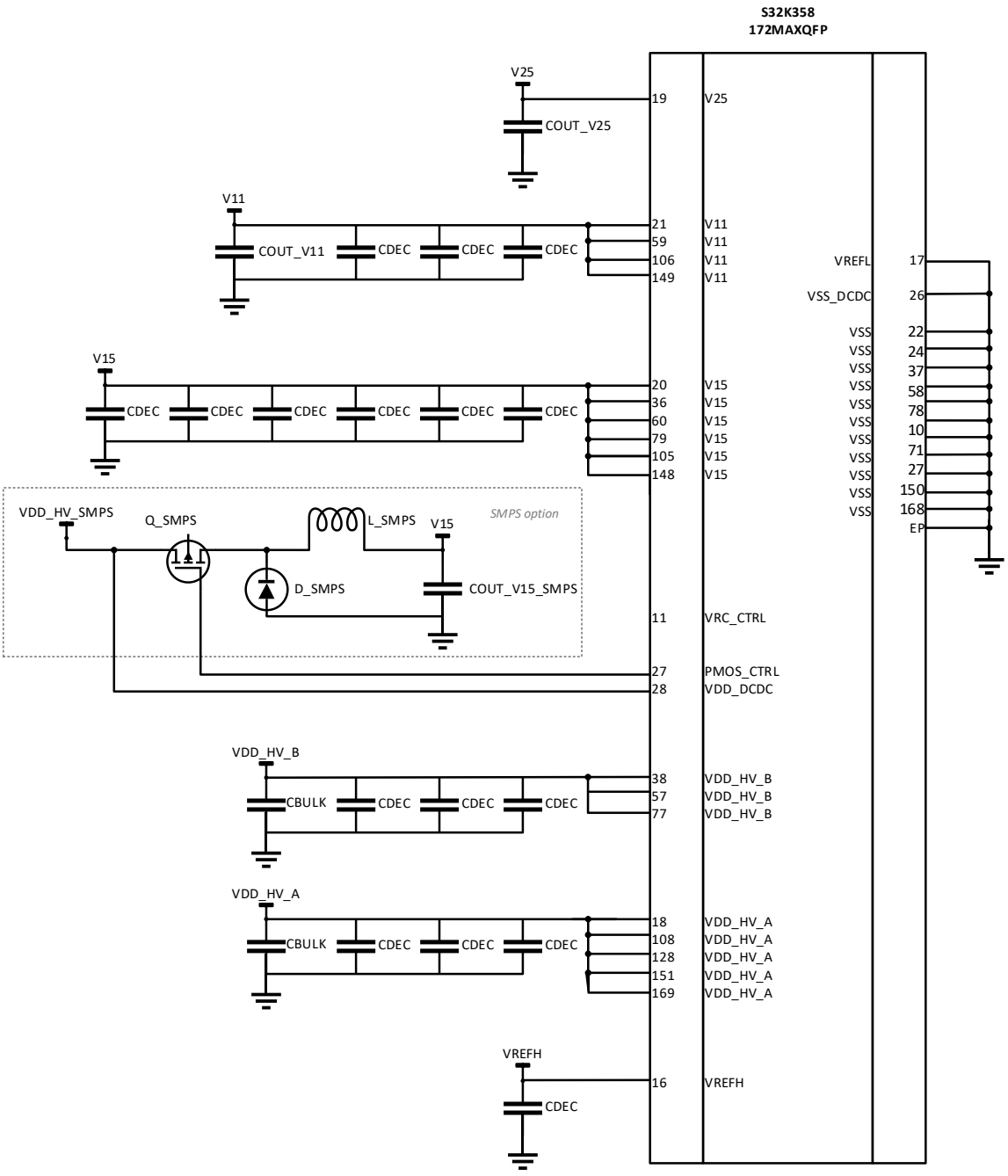


Figure 20. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /172MaxQFP+EP

2.1.2.5 Bulk/Bypass and decoupling capacitors scheme for the S32K344 /257MBGA

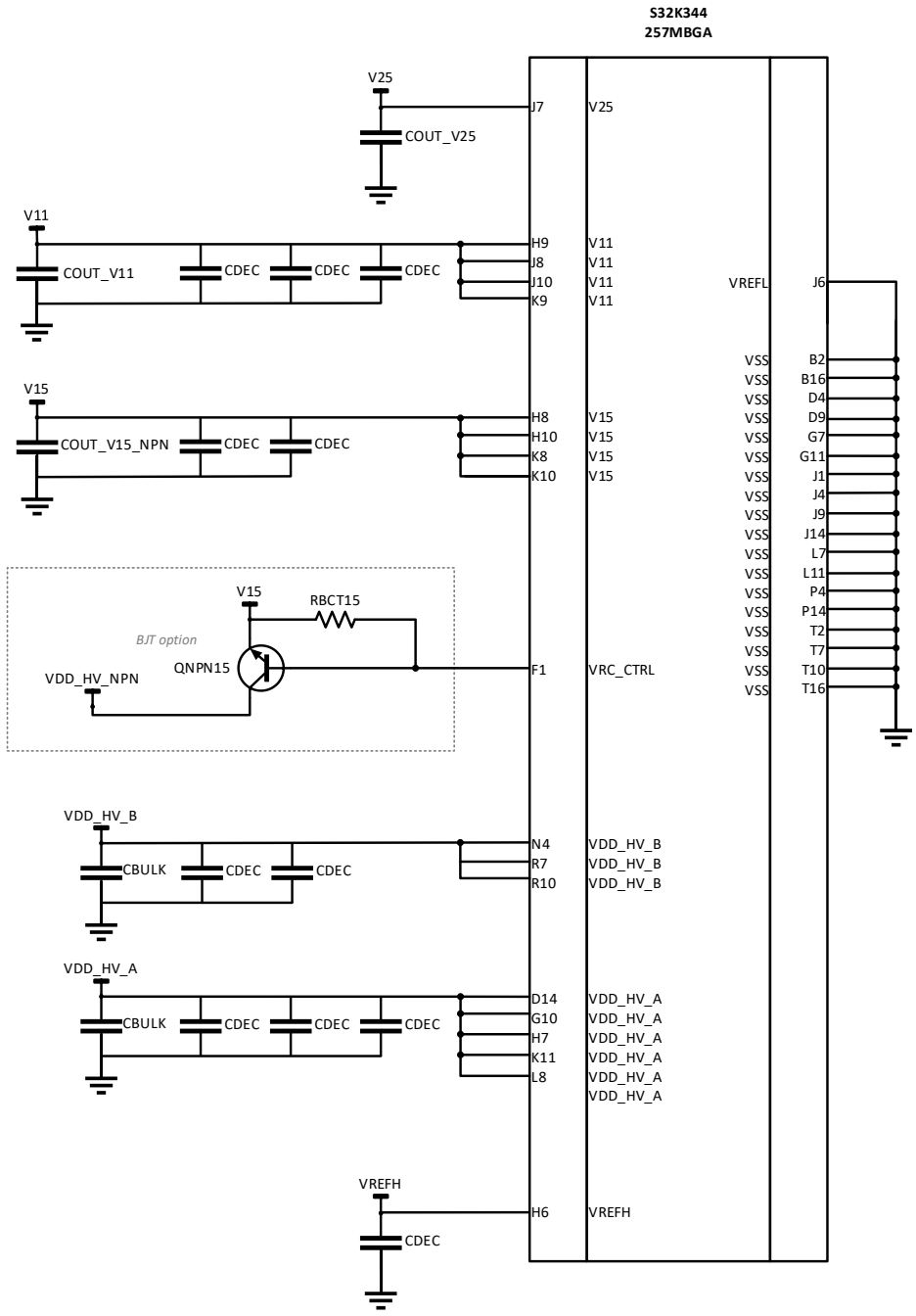


Figure 21. Bulk/Bypass and decoupling capacitors scheme for the S32K344 /257MBGA

2.1.2.6 Bulk/Bypass and decoupling capacitors scheme for the S32K344 /42 /24 /22 /14 – 172MaxQFP

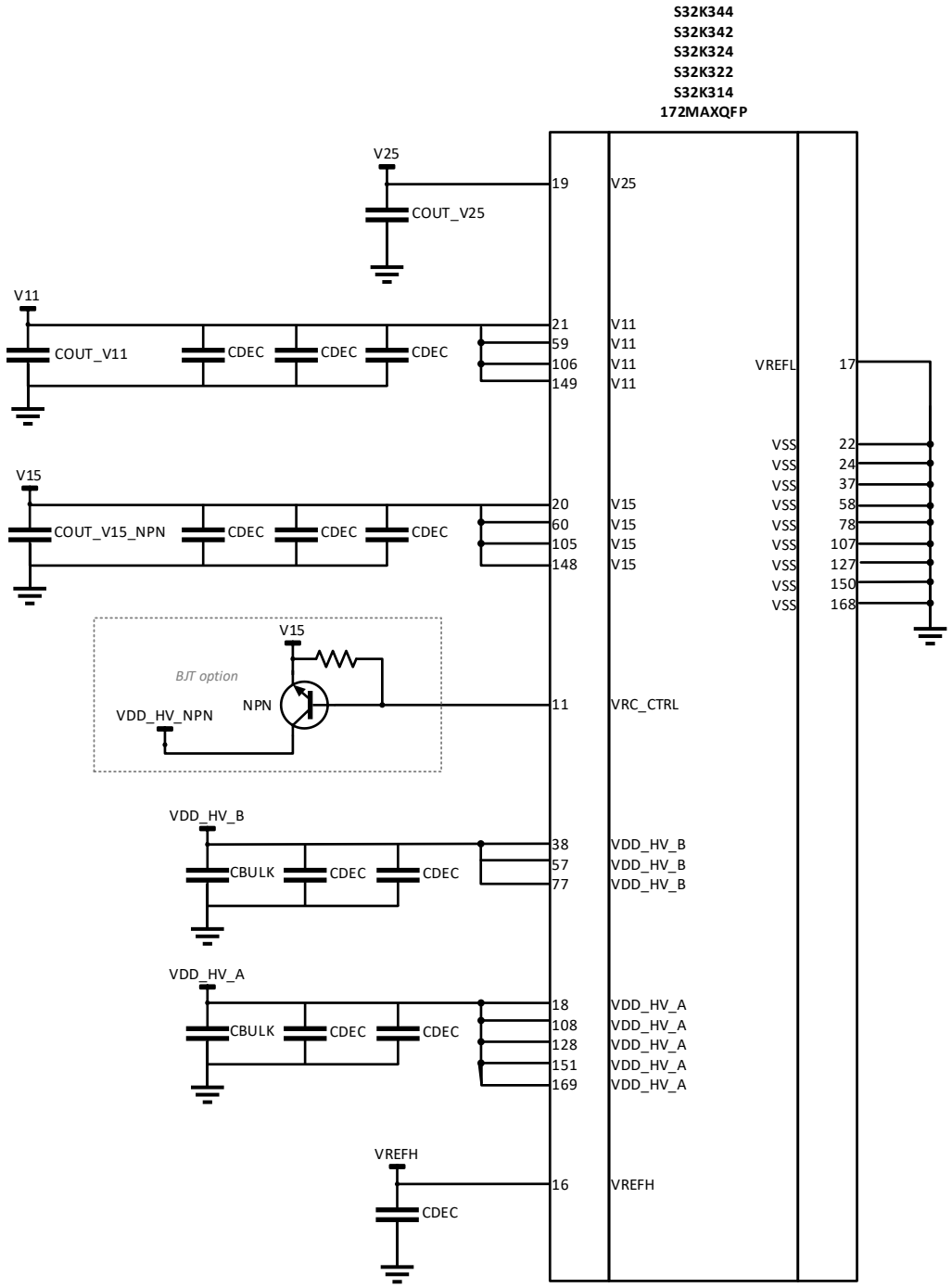


Figure 22. Bulk/Bypass and decoupling capacitors scheme for the S32K344 /42 /24 /22 /14 – 172MaxQFP

2.1.2.7 Bulk/Bypass and decoupling capacitors scheme for the S32K342 - 100MaxQFP

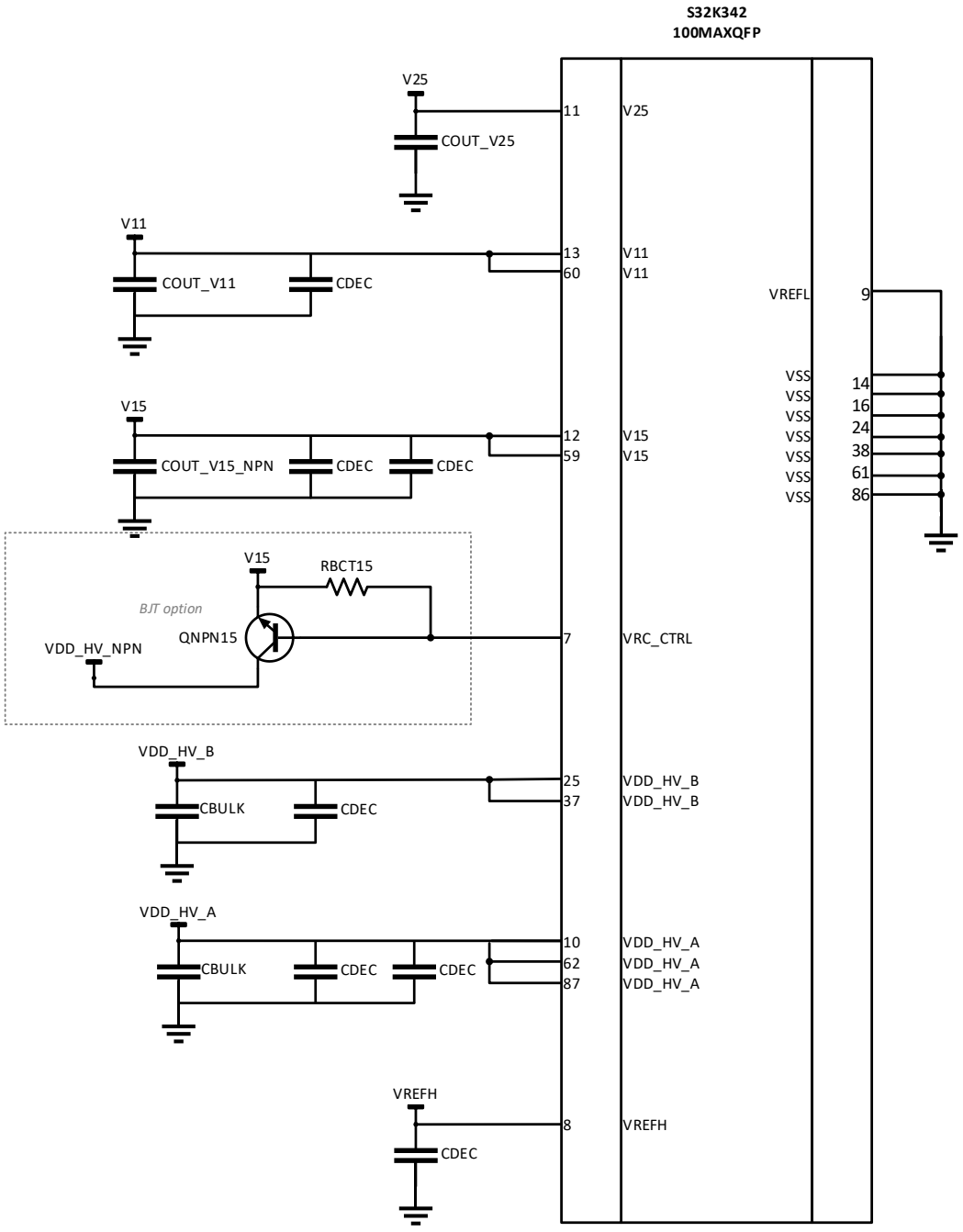


Figure 23. Bulk/Bypass and decoupling capacitors scheme for the S32K342 - 100MaxQFP

2.1.2.8 Bulk/Bypass and decoupling capacitors scheme for the S32K312 – 172MaxQFP

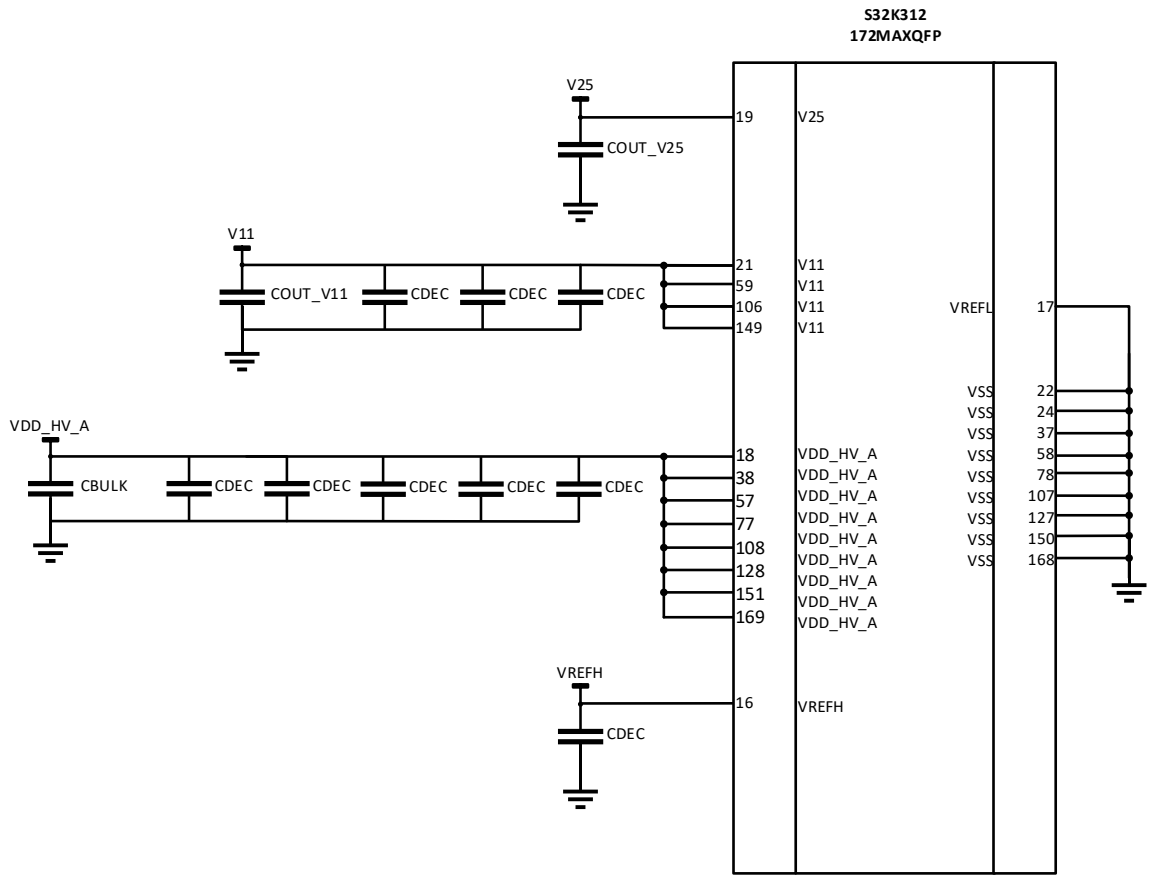


Figure 24. Bulk/Bypass and decoupling capacitors scheme for the S32K312 – 172MaxQFP

2.1.2.9 Bulk/Bypass and decoupling capacitors scheme for the S32K312 /11 - 100MaxQFP

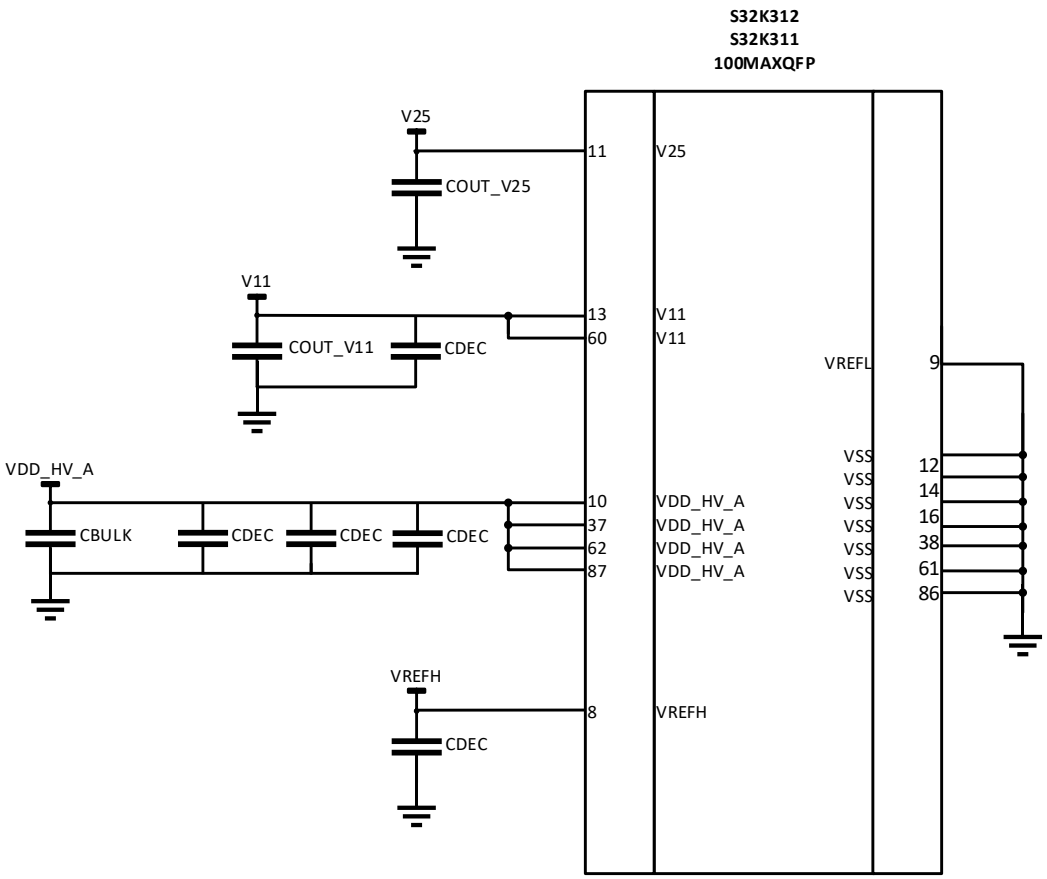


Figure 25. Bulk/Bypass and decoupling capacitors scheme for the S32K312 /11 - 100MaxQFP

2.1.2.10 Bulk/Bypass and decoupling capacitors scheme for the S32K311 /48LQFP

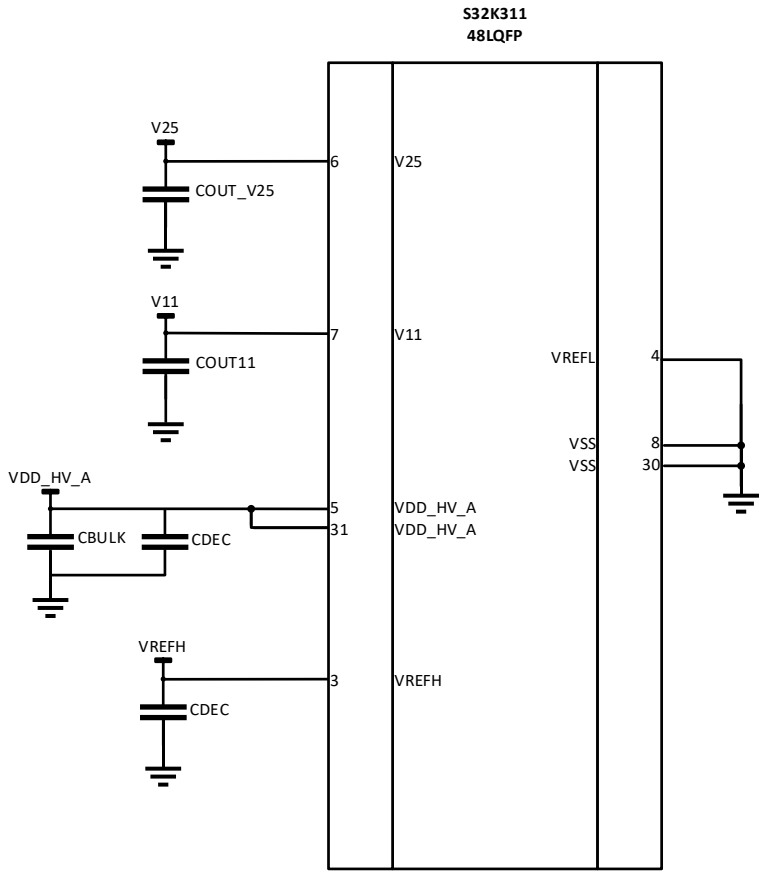


Figure 26. Bulk/Bypass and decoupling capacitors scheme for the S32K311 /48LQFP

Table 2. Components description and values

Symbol	Characteristic	Value	Description
C_{BULK}	X7R Ceramic or Tantalum	4.7uF – 10uF	Local Bulk/Bypass Capacitor for domain
C_{DEC}	X7R Ceramic	100nF - 220nF	Decoupling Capacitor
C_{OUT_V25}	X7R Ceramic	220nF	Decoupling Capacitor for V25
C_{OUT_V11}	X7R Ceramic or Tantalum	2.2uF	Local Bulk/Bypass Capacitor for domain

1. All VDD_HV_A pins must be shorted and connected externally together to a common and same reference on PCB.
2. All VDD_HV_B pins must be shorted and connected externally together to a common and same reference on PCB.
3. All V11 pins must be shorted and connected externally together to a common and same reference on PCB. This internal reference voltage must not be used or connected to other interfaces in the application.
4. All V15 pins must be shorted and connected externally together to a common and same reference on PCB. This internal reference voltage must not be used or connected to other interfaces in the application.
5. The V25 is an MCU internal reference voltage that must not be used or connected to other interfaces in the application.

2.2 VDD_HV_A - Main I/O and Analog Supply Voltage

VDD_HV_A is the main I/O and analog supply voltage in the S32K3xx MCU. The VDD_HV_A domain must be connected to an external power supply of +3.3 V or +5.0V. An off-chip local Bulk/bypass and decoupling capacitors between the VDD_HV_A pins and the VSS reference are required. From the ***Figure 17*** to ***Figure 26*** are shown the recommended power supply decoupling schemes on the VDD_HV_A domain for designs using the S32K3xx MCUs.

Table 3. VDD_HV_A – Main I/O and Analog Supply pins

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number								Comments
		S32K311 48LQFP	**S32K342/22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP - V1.0/V1.1	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
VDD_HV_A	+3.3V or +5.0V	5	10	10	18	18	D14	18	D14	All VDD_HV_A pins must be shorted and connected externally together to a common reference on the PCB. A decoupling capacitor can be used per each supply pin and a local Bulk/bypass capacitor just for the VDD_HV_A domain, in order to increase the robustness and decoupling effect on this voltage reference of the MCU.
		31	62	62	108	108	G10	108	G10	
		-	87	87	128	128	H7	128	H7	
		-	-	37	151	151	K11	151	K11	
		-	-	-	169	169	L8	169	L8	
		-	-	-	-	38	-	-	H13	
		-	-	-	-	57	-	-	E5	
		-	-	-	-	77	-	-	N5	
		-	-	-	-	-	-	-	N9	

2.3 VREFH – ADC High Reference Voltage

VREFH is the ADC High Reference Voltage. An off-chip decoupling capacitor between the VREFH pin and the VSS/VREFL reference are required.

The VREFH is the ADC High Reference Voltage in the S32K3xx MCU. The VREFH pin must be connected to an external power supply or a reference voltage ≤ VDD_HV_A. An off-chip local decoupling capacitor between the VREFH pin and the VSS/VREFL reference is required. From the ***Figure 17*** to ***Figure 26*** are shown the recommended power supply decoupling scheme on the VREFH pin for designs using the S32K3xx MCUs.

Table 4. VREFH – ADC High Reference Voltage

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number								Comments
		S32K311 48LQFP	**S32K342/22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP - V1.0/V1.1	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
VREFH	≤VDD_HV_A	3	8	8	16	16	H6	16	H6	A decoupling capacitor must be used on the supply pin.
VREFL	GND	4	9	9	17	17	J6	17	J6	Refers the section *VSS, VSS_DCDC and VREFL – Ground and* ADC Reference Low.

2.4 VDD_HV_B - Secondary I/O Supply Voltage

The VDD_HV_B is the secondary I/O Supply voltage in some versions of the S32K3xx MCU family. The VDD_HV_B domain must be connected to an external power supply of +3.3 V or +5.0V. An off-chip local Bulk/bypass and decoupling capacitors between the VDD_HV_B pins and the VSS reference are required. From the ***Figure 17*** to ***Figure 23*** are shown the recommended power supply decoupling schemes on the VDD_HV_B domain for designs using the S32K3xx MCUs.

Table 5. VDD_HV_B - Secondary I/O Supply Voltage

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number								Comments
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K312 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP V1.0 and V1.1]	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
VDD_HV_B	+3.3V or +5.0V	-	25	-	38	-	N4	38	N4	All VDD_HV_B pins must be shorted and connected externally together to a common reference on the PCB. A decoupling capacitor can be used per each supply pin and a local Bulk/bypass capacitor just for the VDD_HV_B domain, in order to increase the robustness and decoupling effect on this voltage reference of the MCU.
		-	37	-	57	-	R7	57	R7	
		-	-	-	77	-	R10	77	R10	

2.5 V11 - Core logic voltage supply (+1.1 V)

V11 is the internally generated core logic voltage supply. And an off-chip Bulk/bypass, decoupling and filter capacitors between the V11 pins and the VSS reference are required. From the ***Figure 17*** to ***Figure 26*** are shown the recommended power supply decoupling scheme on the V11 pin for designs using the S32K3xx MCUs. This reference voltage must not be used or connected to other interfaces in the application.

Table 6. V11 - Core logic voltage supply (+1.1 V)

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number								Comments
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP V1.0 and V1.1]	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
V11[1]	+1.1V Internal voltage reference	7	13	13	21	21	H9	21	H9	All V11 pins must be shorted and connected externally together to a common reference on the PCB. A decoupling capacitor can be used per each supply pin and a local Bulk/bypass capacitor just for the V11 domain, in order to increase the robustness and decoupling effect on this voltage reference of the MCU. [1]
		-	60	60	59	59	J8	59	J8	
		-	-	-	106	106	J10	106	J10	
		-	-	-	149	149	K9	149	K9	

1. This internal reference voltage must not be used or connected to other interfaces in the application.

2.6 V25 - Flash memory supply (+2.5 V)

V25 is the internally generated Flash memory supply. And an off-chip filtering and decoupling capacitor between the V25 pin and the VSS reference are required. This reference voltage must not be used or connected to other interfaces in the application.

Table 7. V25 - Flash memory supply (+2.5 V)

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number								Comments
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP V1.0 and V1.1]	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
V25[1]	+2.5V Internal voltage reference	19	11	11	19	19	J7	19	J7	This internal reference voltage must not be used or connected to other interfaces in the application. [1]

1. This internal reference voltage must not be used or connected to other interfaces in the application.

2.7 V15 - High-current logic supply voltage (+1.5V)

V15 is the high-current logic supply voltage for some MCU versions of the K3 family. The S32K3 MCU has the option to supply voltage reference using an external NPN ballast transistor and a stability ceramic capacitor or supplied externally by an SBC to +1.5V. An off-chip bulk/bypass capacitor and a decoupling capacitor between each V15 pin and the VSS reference are required for both configurations. This MCU reference voltage must not be used or connected to other interfaces in the application. From the ***Figure 17*** to ***Figure 23*** are shown the recommended power supply decoupling schemes on the V15 domain for designs using the S32K3xx MCUs.

Table 8. V15 – High Current Logic Supply Voltage

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number								Comments
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP V1.0 and V1.1]	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
V15[1]	+1.5V High-current logic supply voltage	-	12	-	20	-	H8	20	E9	All V15 pins must be shorted and connected externally together to a common reference on the PCB. A decoupling capacitor can be used per each supply pin and a local Bulk/bypass capacitor just for the V15 domain, in order to increase the robustness and decoupling effect on this voltage reference of the MCU. [1]
		-	59	-	60	-	H10	36	H8	
		-	-	-	105	-	K8	60	H10	
		-	-	-	148	-	K10	79	J13	
		-	-	-	-	-	-	105	K8	
		-	-	-	-	-	-	148	K10	
		-	-	-	-	-	-	-	N6	
		-	-	-	-	-	-	-	N8	

1. This internal reference voltage must not be used or connected to other interfaces in the application.

2.7.1 V15 - Supplying with the NPN Ballast Transistor option

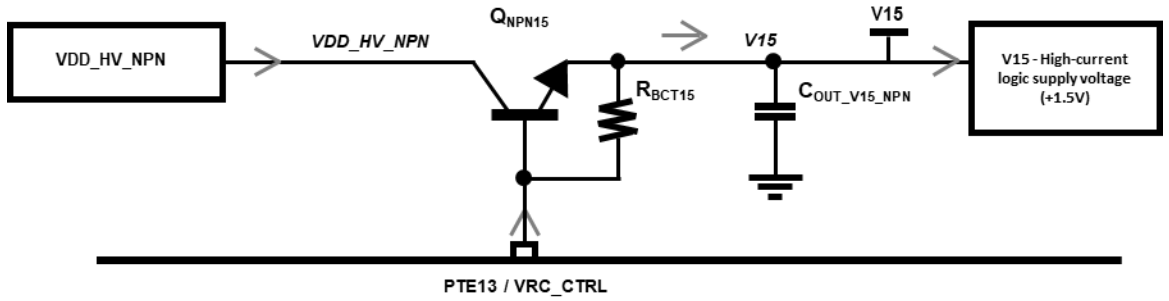


Figure 27. V15 - Supplying with the NPN Ballast Transistor option

Table 9. V15 - Supplying with the NPN Ballast Transistor option

Module	MCU Pin Name	Function	S32K3 MCU Package - Pin Number								Comments
			S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
|NPN Ballast Transistor Interface - Supply Option [1]	PTE13	VRC_CTRL [1]	-	7	-	11	-	F1	11	F1	Control base pin for the external NPN Ballast transistor for V15. [1]

1. This internal function for the External NPN ballast transistor option must not be used or connected to other interfaces in the application.

Table 10. V15 - Component description and values for the external NPN Ballast transistor option

Symbol	Characteristic	Value
Q_{NPN15}	NPN Ballast Transistor	
R_{BCT15}	Metal Film Resistor	2.2kΩ
$C_{OUT\_V15\_NPN}$	Stability Capacitor. X7R Ceramic or Tantalum	2.2uF
C_{DEC} [1]	Decoupling Capacitor	100nF – 220nF

1. A decoupling capacitor can be used per each supply pin and a local Bulk/bypass capacitor just for the V15 domain, in order to increase the robustness and decoupling effect on this voltage reference of the MCU.

2.7.1.1 Selecting the NPN external ballast transistor

The maximum V15 current capability using an NPN External Ballast transistor [Q_{NPN15}], is determined by the allowed maximum power of the device. The designer should consider that the maximum power dissipation of the transistor will depend mainly on the following factors:

- Package type
- Dissipation mounting pad area on the PCB
- Ambient temperature

Like the maximum power supply potentials, maximum junction temperature is a worst-case limitation which shouldn't be exceeded. This is a critical point, since the lifetime of all semiconductors is inversely related to their operating junction temperature. For almost all transistors packages, the maximum power dissipation is specified to +25°C; and above this temperature, the power derates to the maximum Junction Temperature (+150°C). The Rth_{JA} depends considerably on the package transistor and the PCB mounting pad area. The final product thermal limits should be tested and qualified in order to ensure acceptable performance and reliability.

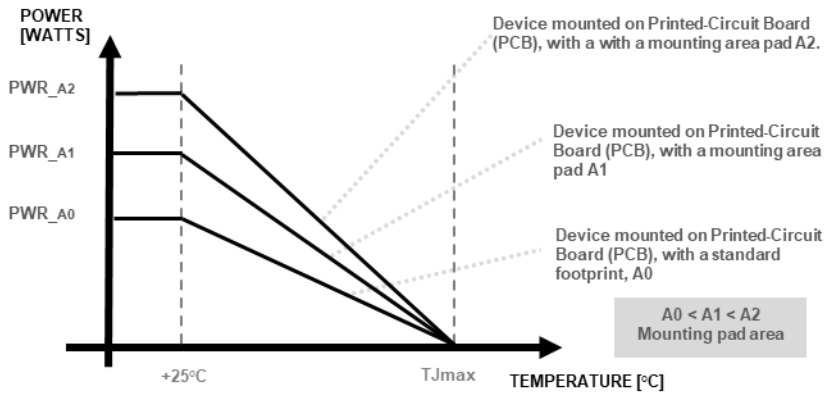


Figure 28. Typical Maximum power dissipation versus temperature for BJT transistors

The maximum power dissipation PWR_{MAX} by the device is given by:

$$PWR_{MAX} = \frac{Tj_{MAX} - Tamb_{MAX}}{Rth_{JA}}$$

where $Tamb_{MAX}$ is maximum ambient temperature, Tj_{MAX} is maximum junction temperature and Rth_{JA} is the Junction to Ambient Thermal Resistance of the Ballast transistor mounted on the specific PCB.

2.7.1.2 Recommended NPN Ballast transistors

Transistor specifications give the minimum and maximum gain. The worst case is usually significantly lower than the nominal figure on the transistor datasheet cover page. Furthermore, the datasheet values are usually given at room temperature (+25 °C). The required gain should be calculated at cold temperature, because a NPN transistor has minimum gain at low temperature. The worst-case gain at cold temperature can be obtained from the transistor supplier or can be estimated using the graphs given in the transistor datasheet. The *hfe* of the external BJT transistor should be ≥ 75. Darlington devices are not permitted.

Table 11. Recommended NPN Ballast transistor

Part Number	Package Type	Manufacturer
BCP56-16TX	SOT223	NEXPERIA
PZT2222A	SOT223	NEXPERIA
MJD31CAJ	DPak-3	NEXPERIA
NJD2873T4G	DPak-3	ONSEMI

The designer must follow and verify all Layout/soldering footprint recommendations of the transistor supplier in order to reach a good performance transistor.

2.7.2 V15 - Supplying with the SMPS Interface for the S32K3x8

Table 12. V15 – Supplying with the SMPS Interface

Module	MCU Pin Name	Function	S32K3 MCU Package - Pin Number								Comments
			S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
SMPS Interface - Supply Option	PMOS _CTRL	PMOS Gate Control for the SMPS option	-	-	-	-	-	-	27	K5	
	VDD_DCDC		-	-	-	-	-	-	28	L5	
	VSS_DCDC	VSS/GND	-	-	-	-	-	-	26	J5	Refers the section *VSS, VSS_DCDC and VREFL – Ground and* ADC Reference Low.

1. These internal functions/pins must not be used or connected to other interfaces in the application.

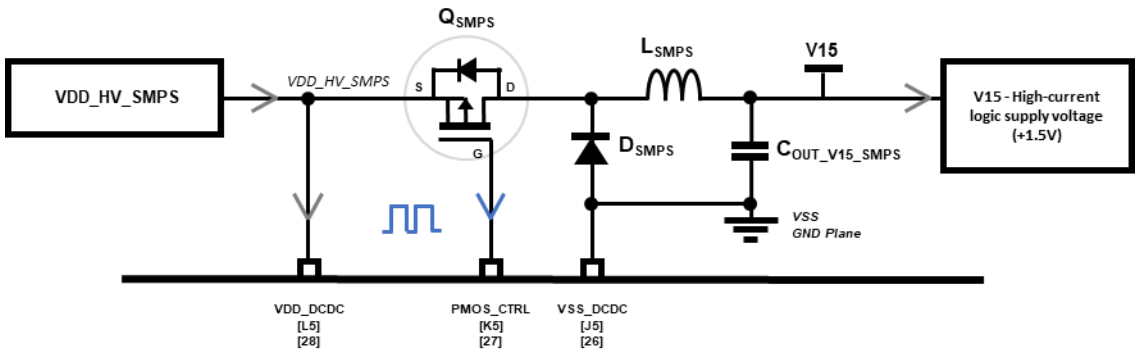


Figure 29. V15 - Supplying with the SMPS Interface option

Table 13. V15 - Component description and values for the SMPS option

Symbol	Characteristic	Value
Q_{SMPS}	P-Channel Mosfet	-
D_{SMPS}	Schottky Diode	-
L_{SMPS}	Inductor	4.7uF - 5.6uF
C_{SMPS}	Stability Capacitor. X7R Ceramic or Tantalum	20uF - 22uF

1. A decoupling capacitor can be used per each supply pin of the V15 domain, in order to increase the robustness and decoupling effect on this voltage reference of the MCU.

2.7.2.1 Selecting the power MOSFET

When determining the gate drive requirements for the switching device in the motor control application, the dynamic characteristics determine the performance of the device. The total gate charge [QG], is one of most important parameters which define the selection of the right MOSFET. The charge on the gate terminal of the MOSFET as determined by its gate-to-source capacitance. The lower the gate charge, the easier it is to drive the MOSFET. Total gate charge, [QG], affects the highest reliable switching frequency of the MOSFET. The lower the gate charge, the higher the frequency. Operation at higher frequencies allows use of lower value, smaller size capacitors and inductors, which can be significant factors in system cost. A low gate charge also makes it easier to drive the MOSFET, however, designers sometimes need to trade-off switching frequency with EMI considerations.

The amount of charge necessary to switch the MOSFET can be determined from its data sheet by knowing the intended gate-to-source voltage, drain current and drain-to-source voltage. The number can be taken from the characteristic curve for gate charge or taken directly from the electrical characteristics section of the MOSFET data sheet. The gate charge number will give the total gate charge necessary to switch the device.

The amount of current required to switch a MOSFET is directly related to the gate charge and can be determined using the next equation:

Equation 3. $QG = I \times t$

Where:
QG = total gate charge number I = gate current t = device switching time

2.7.2.2 Switching process of the power MOSFET

The turn-on transition is broken down into three phases, refer to figure 17. These phases will be briefly explained. The figure 18 shows the transition through these regions in terms of output characteristics. Gate charge can be derived from the non-linear capacitance curves.

In the stage-1 [S1], from t0 to t1, the MOSFET is OFF, gate-to-source voltage [VGS] rises from 0 V to its plateau voltage [VGP]. Once VGS reaches the threshold voltage [VTH], the MOSFET starts conducting and ID rises. In this phase, the gate current charges the input capacitance (CISS) with its VDS being clamped. MOSFET starts to conduct, and the turn-on process enters the second stage.

In the stage-2 [S2], from t1 to t2, the drain current finally reaches the level of the total load current. VGS is clamped at VGP and remains relatively flat, during this region, the gate current is used to charge the reverse transfer capacitance (CRSS) and the MOSFET operates in the linear region. After the MOSFET takes over all the load current, the drain to source voltage VDS starts to drop, and the circuit enters the third stage.

Switching losses occur between the phase where the VG reaches the VTH, in the stage1 to t2. The minimum turn-on time is usually governed by the dv/dt capability of the system. Reducing the turn-on time increases the amount of diode reverse recovery current and hence increases the peak power dissipation, however the total power dissipated tends to reduce.
In the stage-3 [S2], from t2 to t3, the MOSFET enters into Ohmic mode operation. VGS rises from VGP to driver supply voltage (VGDR). Both ID and VDS remain relatively constant.

Several of the dynamic parameters are highly dependent on the measurement conditions. Consequently, understand the dynamic characteristics before comparing data sheets from suppliers with different standard conditions.

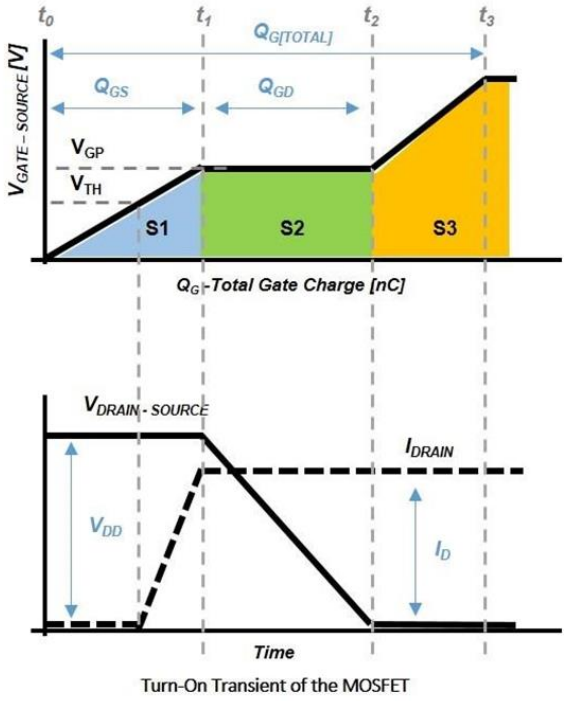


Figure 30. Gate-to-Source voltage and switching versus total charge

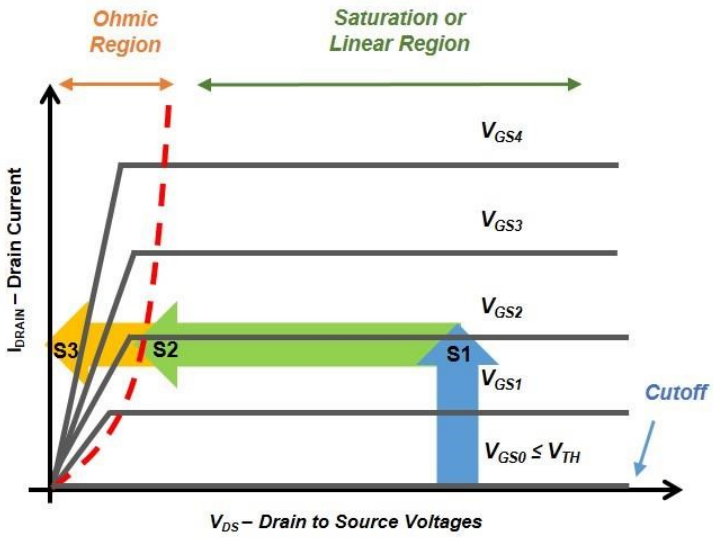


Figure 31. On-Region characteristics for different Gate-to-Source voltages

2.7.2.3 Internal diode reverse characteristic

In motor applications that make positive use of a power MOSFET internal diode, there is a requirement for this reverse recovery time [trr] to be fast. The diode characteristics are important if the MOSFET is being used in the so-called "third quadrant". The third quadrant is a typical arrangement where the MOSFET replaces a diode to reduce the voltage drop from the inherent diode forward voltage drop. In such a situation, there is always a small time period when the MOSFET parasitic diode is conducting before the MOSFET turns on. For such applications, the diode switching parameters are important. In addition, diode reverse recovery contributes to the power losses as well as oscillation, which can cause EMC concern.

2.7.2.4 Circuit layout considerations

The optimum performance of the SMPS interface cannot be achieved without taking due considerations on the circuit board design and layout. The precautions which must be taken to minimize the amount of stray inductance in the circuit include:

- Positioning the power MOSFETs as close as possible to the pre-driver interface of the S32M2xx microcontroller.
- Reducing circuit board track lengths to a minimum and using twisted pairs for all interconnections.
- For paralleled devices, keeping all connections short and symmetrical.

2.7.2.5 Recommended PMOS for SMPS Interface

Table 14. Recommended P-channel Mosfet

Part Number	Package Type	Manufacturer
PXP400-100QSJ	MLPAK33	Nexperia
BUK4D110-20PX	MLPAK33	Nexperia
PMV48XPA	SOT23	Nexperia

The designer must follow and verify all Layout/soldering footprint recommendations of the transistor supplier in order to reach a good performance transistor.

2.8 VSS, VSS_DCDC and VREFL – Ground and ADC Reference Low

All VSS pins and VREFL pin of the MCU must be externally connected together in a continuous and single solid GND plane.

Table 15. VSS pins – MCU Ground reference

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number									Comments
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP [V1.1] V1.0 and V1.1]	**S32K344** 172MAXQFP [V1.0]	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
VSS	0V-GND	8	14	12	22	22	20	B2	22	B2	All VSSx/VSS_DCDC pins and the VREFL pin of the MCU must be externally connected in a continuous and single solid GND plane as mandatory.
		30	16	14	24	37	22	B16	24	B16	
		-	24	16	37	58	24	D4	37	D4	
		-	38	38	58	78	37	D9	58	D9	
		-	61	61	78	107	58	G7	78	E13	
		-	86	86	107	127	78	G11	107	G7	
		-	-	-	127	150	107	J1	127	G11	
		-	-	-	150	168	127	J4	150	J1	
		-	-	-	168	-	150	J9	168	J4	
		-	-	-	-	-	168	J14	-	J9	
		-	-	-	-	-	-	L7	-	J14	

MCU Pin Name	Normal Operating Voltage	S32K3 MCU Package - Pin Number									Comments
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP [V1.1] V1.0 and V1.1]	**S32K344** 172MAXQFP [V1.0]	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
		-	-	-	-	-	-	L11	-	L7	
		-	-	-	-	-	-	P4	-	L11	
		-	-	-	-	-	-	P14	-	M5	
		-	-	-	-	-	-	T2	-	N7	
		-	-	-	-	-	-	T7	-	N10	
		-	-	-	-	-	-	T10	-	P4	
		-	-	-	-	-	-	T16	-	P14	
		-	-	-	-	-	-	-	-	T2	
		-	-	-	-	-	-	-	-	T7	
		-	-	-	-	-	-	-	-	T10	
		-	-	-	-	-	-	-	-	T16	
VREFL	VSS	4	9	9	17	17	17	J6	17	J6	
VSS_DCDC	VSS	-	-	-	-	-	-	-	26	J5	
Exposed Pad	VSS	-	-	-	-	-	-	-	EP	-	The Exposed pad must be externally connected to VSS/GND reference of the MCU.

2.8.1 Suggestions for the PCB layout and connection of the exposed-pad in the S32K358-172MaxQFP

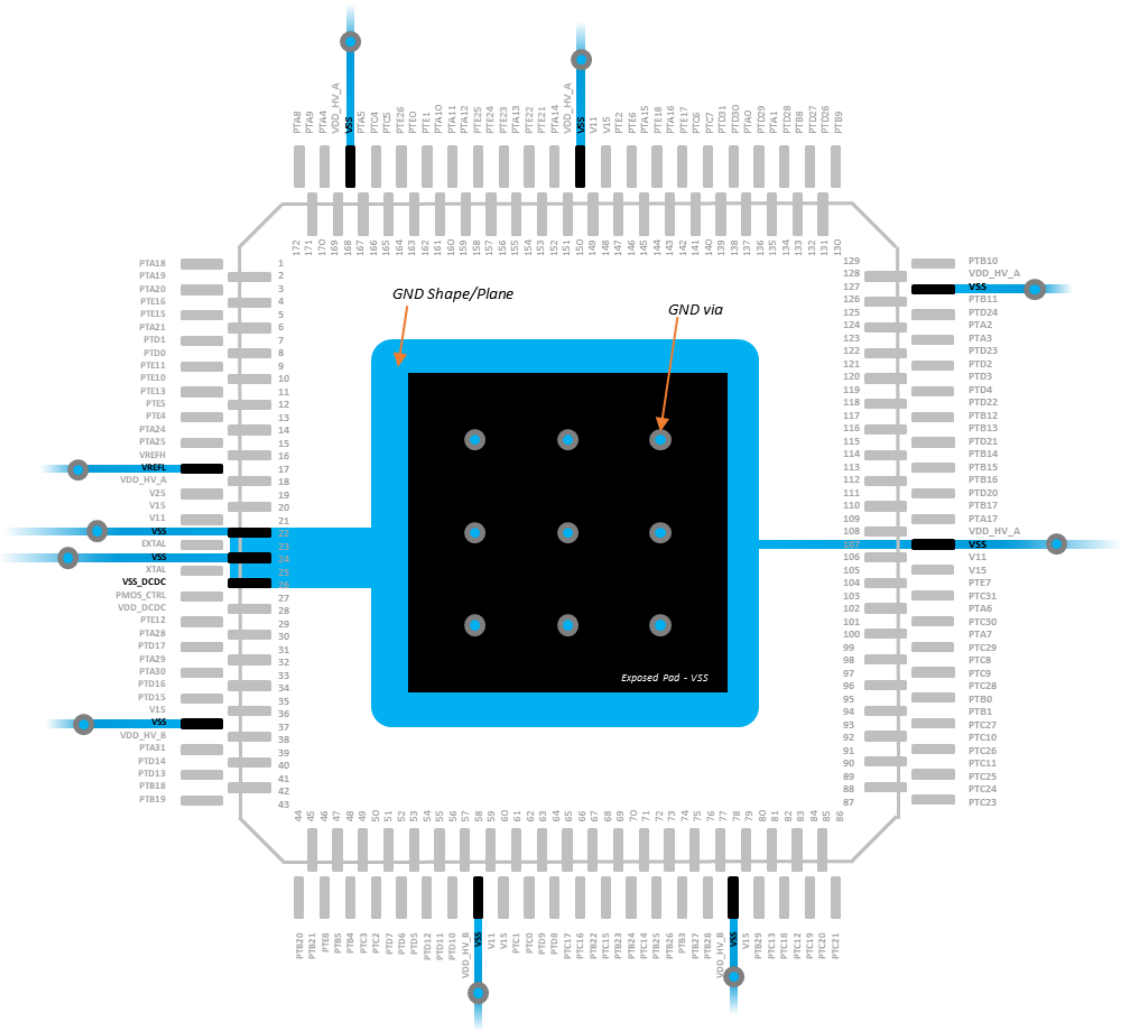


Figure 32. Suggestions for the PCB layout and connection of the exposed-pad in the S32K358-172MaxQFP

2.9 Bulk and decoupling capacitors

The effectiveness of the bulk/bypass and the decoupling capacitors depends on the optimum placement and connection type. The bulk capacitor acts as a local power supply to the power pin, near the decoupling capacitors and close as possible to the assigned reference voltage pin. Decoupling capacitors make the current loop between supply, MCU, and ground reference as short as possible for high frequency transients and noise. Therefore, all decoupling capacitors should be placed as close as possible to each of their respective power supply pin; the ground side of the decoupling capacitor should have a via to the pad which goes directly down to the ground plane.

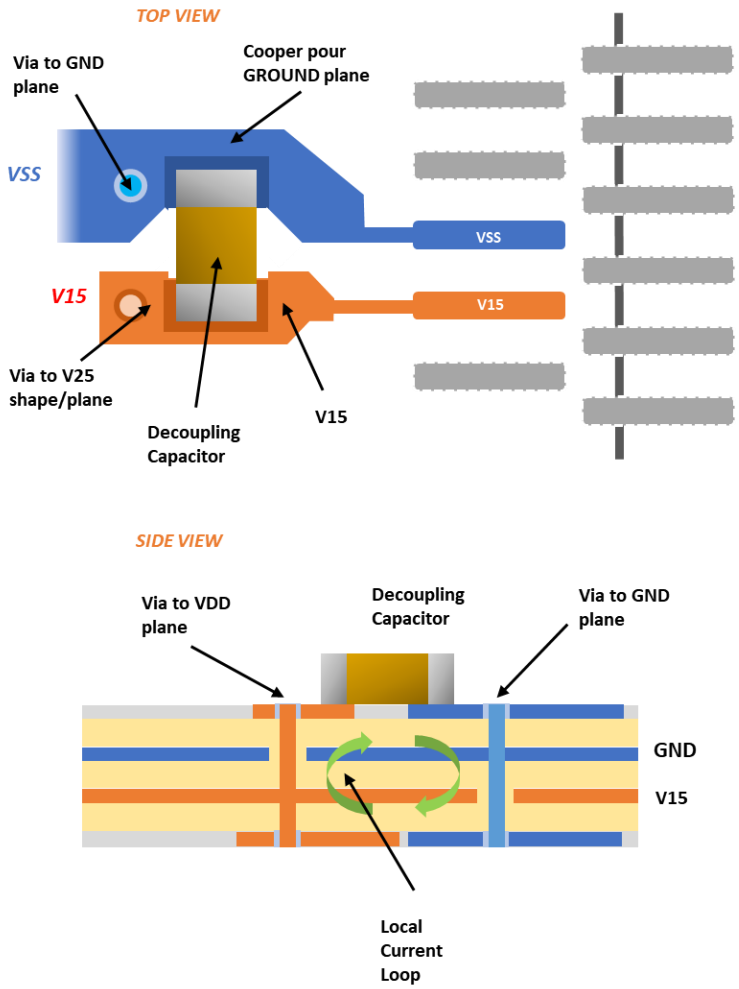


Figure 33. Bulk and decoupling capacitor Connections

2.10 MCU Power Supply Ramp rate

In the S32K3XX datasheet, there is a parameter called "*MCU supply ramp rate*" with a maximum and a minimum limit. During the power-on of MCU, the power supply must assure a ramp-rate within this range from VDD_OFF=0.1V to the voltage operating level of VDD_HV_A, VDD_HV_B and V15. The outcome of violating the specification causes unexpected behavior, stuck operation or damage in the MCU.

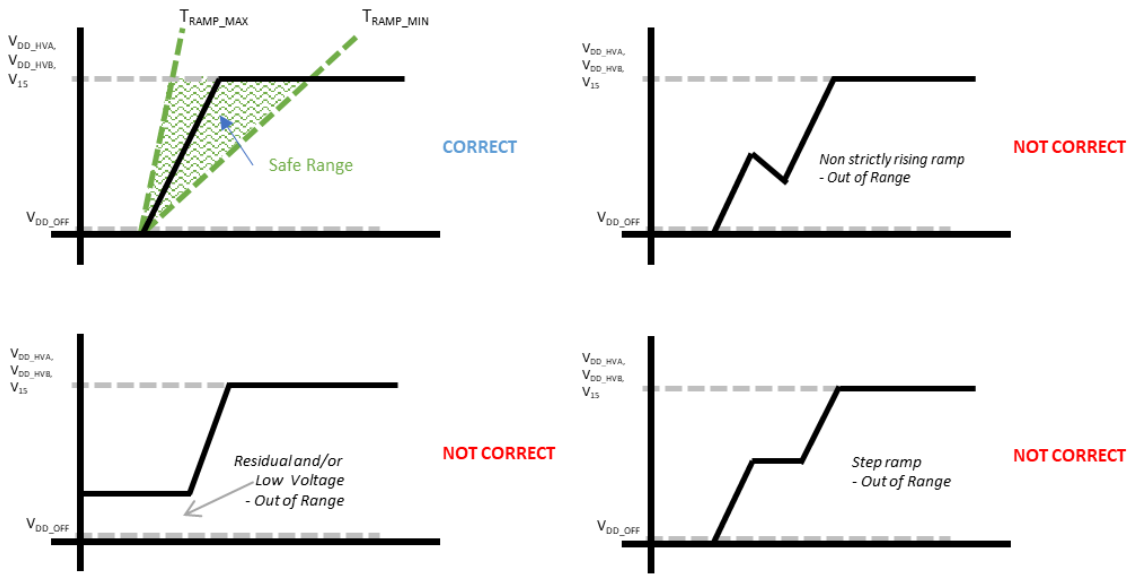
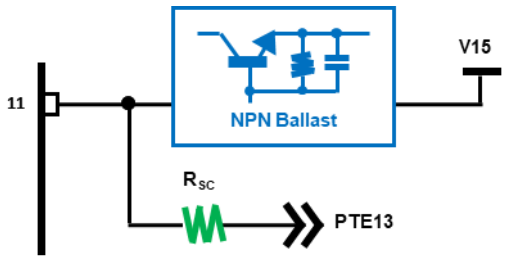
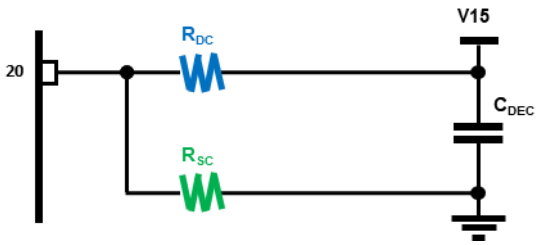
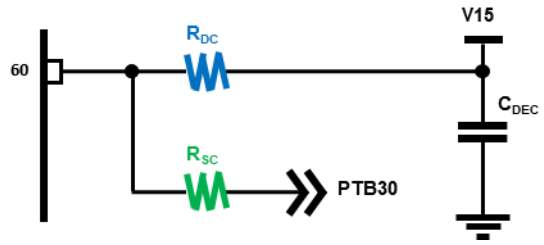
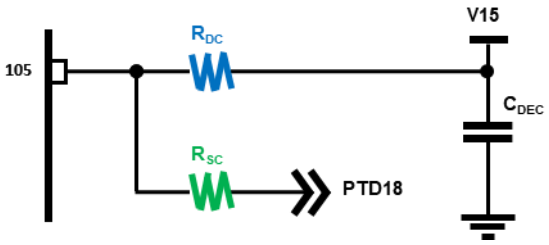
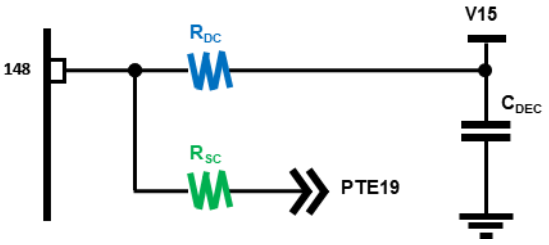
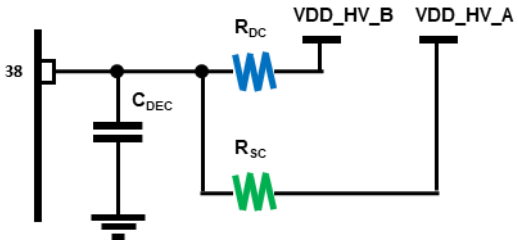


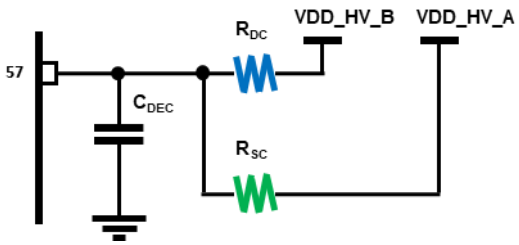
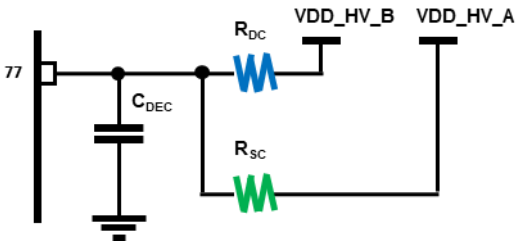
Figure 34. MCU Power Supply Ramp rate

2.11 Pinout differences between *S32K344/42/24/22/14 -172MaxQFP* and *S32K312-172MaxQFP*

Table 16. Pinout differences between S32K344/42/24/22/14 -172MaxQFP and S32K312-172MaxQFP

172 MaxQFP MCU Pin Number	S32K312 [8]			S32K344/42/24/22/14 [8]		Topology Recommended for a drop-in replacement between a S32K312 and a S32K344/42/24/22 on a 172MaxQFP package
	Pin Name	Pin Function	I/O Power Domain	Pin Name	Pin Function	
11	PTE13	IO [8]	VDD_HV_A [5]	PTE13 [4]	VRC_CTRL - PMC Voltage Regulator Control Output [4]	 See note [1], [2], [3] and [4].
20	VSS	Supply GND	-	V15 [4]	+1.5V - High-current logic supply voltage [4]	 See note [1], [2], [3] and [4].

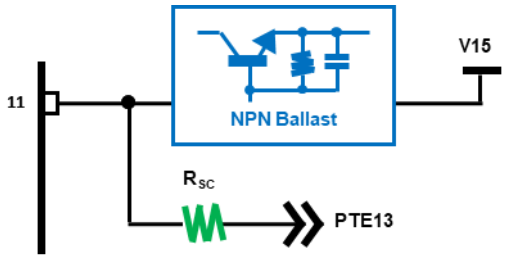
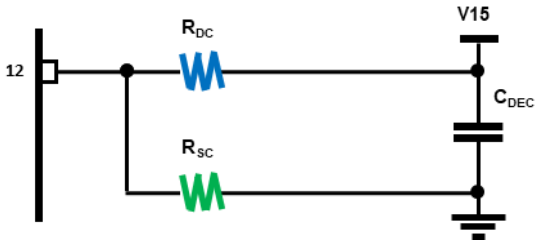
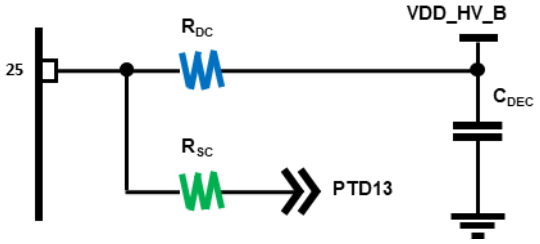
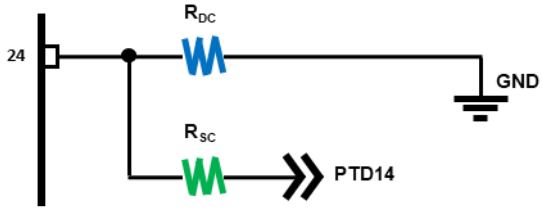
172 MaxQFP MCU Pin Number	S32K312 [8]			S32K344/42/24/22/14 [8]		Topology Recommended for a drop-in replacement between a S32K312 and a S32K344/42/24/22 on a 172MaxQFP package
	Pin Name	Pin Function	I/O Power Domain	Pin Name	Pin Function	
60	PTB30	IO [8]	VDD_HV_A [5]	V15 [4]	+1.5V - High-current logic supply voltage [4]	 See note [1], [2], [3] and [4].
105	PTD18	IO [8]	VDD_HV_A [5]	V15 [4]	+1.5V - High-current logic supply voltage	 See note [1], [2], [3] and [4].
148	PTE19	IO [8]	VDD_HV_A [5]	V15 [4]	+1.5V - High-current logic supply voltage [4]	 See note [1], [2], [3] and [4].
38	VDD_HV_A	VDD_HV_A - Main I/O and Analog Supply Voltage [5]	-	VDD_HV_B [6]	VDD_HV_B - Secondary I/O Supply Voltage [6]	 See note [1], [2], [3], [5] and [6].

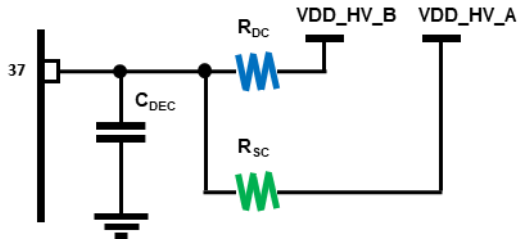
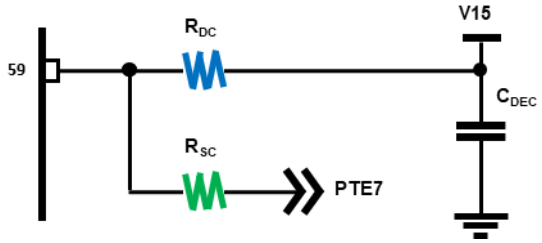
172 MaxQFP MCU Pin Number	S32K312 [8]			S32K344/42/24/22/14 [8]		Topology Recommended for a drop-in replacement between a S32K312 and a S32K344/42/24/22 on a 172MaxQFP package
	Pin Name	Pin Function	I/O Power Domain	Pin Name	Pin Function	
57	VDD_HV_A	VDD_HV_A - Main I/O and Analog Supply Voltage [5]	-	VDD_HV_B [6]	VDD_HV_B - Secondary I/O Supply Voltage [6]	 See note [1], [2], [3], [5] and [6].
77	VDD_HV_A	VDD_HV_A - Main I/O and Analog Supply Voltage [5]	-	VDD_HV_B [6]	VDD_HV_B - Secondary I/O Supply Voltage [6]	 See note [1], [2], [3], [5] and [6].

1. $R_{DC} = R_{SC} = 0$ Ohms
2. R_{DC} must be used just for S32K344/42/24/22 [8], and R_{SC} should be removed
3. R_{SC} must be used just for S32K312[8], and R_{DC} should be removed
4. The V15 reference for the S32K344/42/24/22 [8] should have all considerations mentioned on the section *V15 - High-current logic supply voltage.*
5. The VDD_HV_A reference for the S32K312[8] should have all considerations mentioned on the *VDD_HV_A - Main I/O and Analog Supply Voltage*
6. The VDD_HV_B reference for the S32K344/42/24/22 [8] should have all considerations mentioned on the section *VDD_HV_B - Secondary I/O Supply Voltage.*
7. Customer must evaluate the differences between a S32K344/42/24/22 [8] and a S32K312[8] for a replacement in the application.
8. Refers the Reference Manual and the latest version of S32K3-MCU Pinout file for more details

2.12 Pinout differences between *S32K342/22-100MaxQFP* and *S32K312/11-100MaxQFP*

Table 17. Pinout differences between S32K342/22-100MaxQFP and S32K312/11-100MaxQFP

100 MaxQFP MCU Pin Number	S32K312/11 [8] 100MaxQFP			S32K342/22 [8] 100MaxQFP		Topology Recommended for a drop-in replacement between a S32K312/11 and a S32K342/22on a 100MaxQFP package
	Pin Name	Pin Function	I/O Power Domain	Pin Name	Pin Function	
7	PTE13	IO [8]	VDD_HV_A [5]	PTE13 [4]	VRC_CTRL - PMC Voltage Regulator Control Output [4]	 See note [1], [2], [3] and [4].
12	VSS	Supply GND	-	V15 [4]	+1.5V - High-current logic supply voltage [4]	 See note [1], [2], [3] and [4].
25	PTD13	IO [8]	VDD_HV_A [5]	VDD_HV_B [6]	VDD_HV_B - Secondary I/O Supply Voltage [6]	 See note [1], [2], [3] and [4].
24	PTD14	IO [8]	VDD_HV_A [5]	VSS	Supply GND	 See note [1], [2], [3] and [4].

100 MaxQFP MCU Pin Number	S32K312/11 [8] 100MaxQFP			S32K342/22 [8] 100MaxQFP		Topology Recommended for a drop-in replacement between a S32K312/11 and a S32K342/22on a 100MaxQFP package
	Pin Name	Pin Function	I/O Power Domain	Pin Name	Pin Function	
37	VDD_HV_A [5]	VDD_HV_A - Main I/O and Analog Supply Voltage [5]	-	VDD_HV_B [6]	VDD_HV_B - Secondary I/O Supply Voltage [6]	 See note [1], [2], [3] and [4].
59	PTE7	IO [8]	VDD_HV_A [5]	V15 [4]	+1.5V - High-current logic supply voltage [4]	 See note [1], [2], [3] and [4].

1. $R_{DC} = R_{SC} = 0$ Ohms
2. R_{DC} must be used just for S32K42/22[8], and R_{SC} should be removed
3. R_{SC} must be used just for S32K312/11[8], and R_{DC} should be removed
4. The V15 reference for the S32K42/22[8], should have all considerations mentioned on the section *V15 - High-current logic supply voltage.*
5. The VDD_HV_A reference for the S32K312/11[8], should have all considerations mentioned on the *VDD_HV_A - Main I/O and Analog Supply Voltage*
6. The VDD_HV_B reference for the S32K42/22[8],] should have all considerations mentioned on the section *VDD_HV_B - Secondary I/O Supply Voltage.*
7. Customer must evaluate the differences between a S32K42/22[8], and a S32K312/11[8], for a replacement in the application.
8. Refers the Reference Manual and the latest version of S32K3-MCU Pinout file for more details

3 Clock circuitry

The S32K3xx MCU has the following clock sources:

- 8 - 40 MHz Fast External Oscillator (FXOSC)
- 48 MHz Fast Internal RC oscillator (FIRC)
- 32 kHz Low Power Oscillator (SIRC)
- 32 kHz Slow External Oscillator (SXOSC)
- Up to 320 MHz System Phased Lock Loop (SPLL)

FIRC, SIRC are internal and does not have to be considered from the hardware design perspective. The external oscillator works with a range from 8–40 MHz It provides an output clock that can be provided to the PLL or used as clock source for some peripherals. When using the external oscillator as input source for the PLL, the frequency range of the external oscillator should be 8–40 MHz.

3.1 EXTAL and XTAL pins

These pins provide the interface for a crystal to control the internal clock generator circuitry. EXTAL is the input to the crystal oscillator amplifier. XTAL is the output of the crystal oscillator amplifier. The pierce oscillator provides a robust, low-noise and low power external clock source. It is designed for optimal start-up margin with typical crystal oscillators. S32K3XX MCU supports crystals or resonators from 8 MHz to 40 MHz The Input Capacitance of the EXTAL, XTAL pins is 7pF.

Table 18. S32K3xx - EXTAL and XTAL pins

MCU Pin Name	Signal Description	S32K3 MCU Package - Pin Number									Comments
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP [V1.1]	**S32K344** [1 2 3] 172MAXQFP [V1.0]	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA	
XTAL	External Crystal Output	10	17	17	25	24	25	L1	25	L1	
EXTAL	External Crystal Input	9	15	15	23	23	23	K1	23	K1	

1. The S32K344-172MAXQFP [*V1.0*] is a predecessor version of the S32K344 /42 /24 /22 /14-172MAXQFP [*V1.1*] versions.
2. The S32K344-172MAXQFP [*V1.0]* version is used just for prototypes and initial hardware and software enablement purposes, not for high production or new designs.
3. The hardware differences between S32K344-172MAXQFP [*V1.0*] and S32K344 /42 /24 /22 /14-172MAXQFP [*V1.1*] are clearly mentioned in the Pinout differences between *S32K344-172MaxQFP V1.0* and *S32K344-172MaxQFP V1.1* section

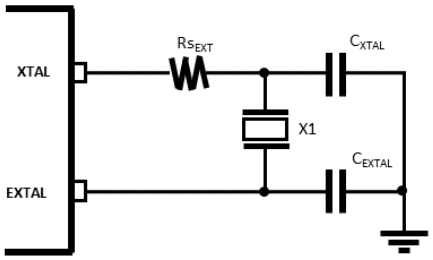


Figure 35. Reference oscillator circuit

Table 19. Components of the oscillator circuit

Symbol	Description
Rs_{EXT}	Series resistor for current limitation
X1	Quartz Crystal / Ceramic Resonator
C_{XTAL}	External load capacitor on XTAL pin.
C_{EXTAL}	External load capacitor on EXTAL pin.

1. The Rs and load capacitors values are dependent on the specifications of the crystal and on the board capacitance. It is recommended the customer develops evaluation and characterization of the crystal on their PCB with the part manufacturer.

3.2 Suggestions for the PCB layout of oscillator circuit

The crystal oscillator is an analog circuit and must be designed carefully and according to the analog-board layout rules:

- It is recommended to send the PCB to the crystal manufacturer to determine the negative oscillation margin as well as the optimum regarding R_S, C_{XTAL} and C_{EXTAL} capacitors. The data sheet includes recommendations for the tank capacitors C_{XTAL} and C_{EXTAL}. These values together with the expected PCB, pin, etc. stray capacity values should be used as a starting point.
- Signal traces between the XTAL/EXTAL pins, the crystal and the external capacitors must be as short as possible, without using any via, these traces pins should only be connected to required oscillator components and must not be connected to any other devices or components. This minimizes parasitic capacitance and sensitivity to crosstalk and EMI.
- Keep other digital signal lines, especially clock lines, analog and frequently switching signal lines, as far away from the crystal connections as possible. Crosstalk from the digital activities may affect the small amplitude of the oscillator signal.
- A ground area should be placed under the crystal oscillator area. This ground plane must be clean ground connected to the VSSx/GND reference of the S32K3XX.
- The main oscillation loop current is flowing between the crystal and the load capacitors. This signal path (crystal to C_{EXTAL} to C_{XTAL} to crystal) should be kept as short as possible and should have a symmetric layout. Hence, both capacitor's ground connections should always be as close together as possible.

The following *Figure 36* and *Figure 37* show the recommended placement and routing for the oscillator layout.

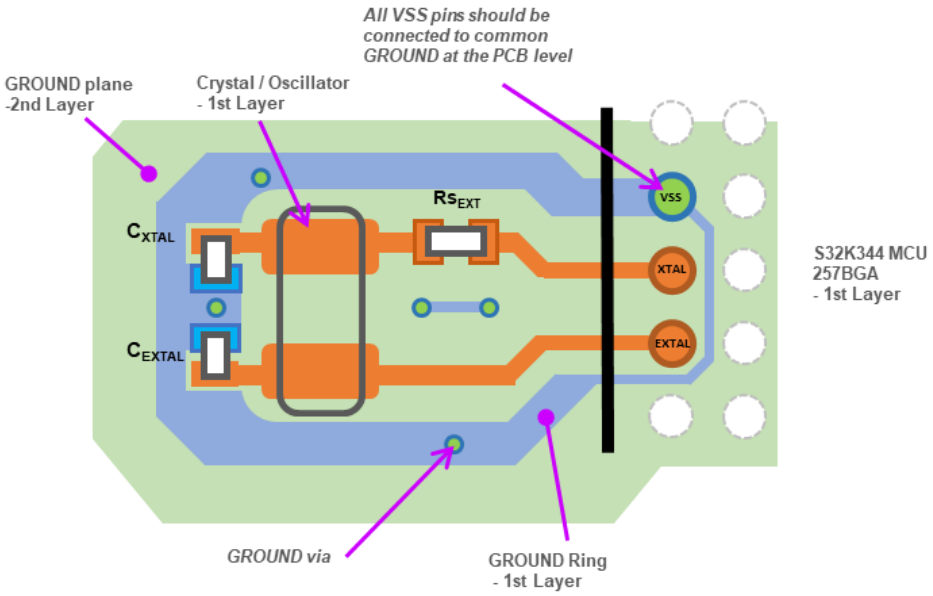


Figure 36. Suggested crystal layout for 257MBGA package

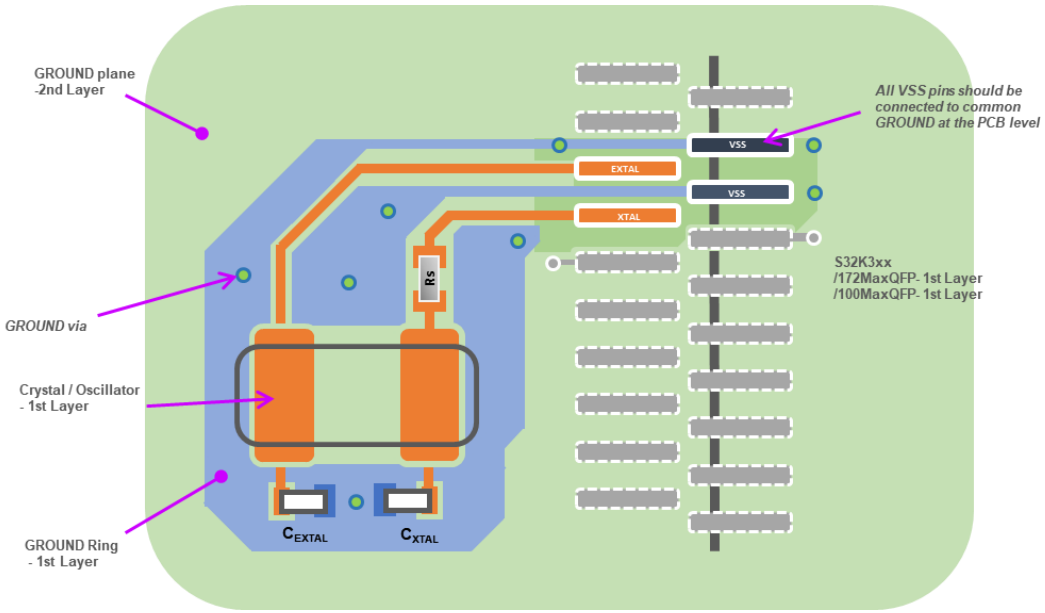


Figure 37. Suggested crystal layout for the 172MaxQFP and 100MaxQFP package

To improve the FXOSC jitter performance, the functionality of the pin next to the Oscillator (PTA26 in the172MaxQFP package) must be limited to static GPIO operation.

Crystal oscillator circuit provides a very-safe stable oscillation when the $GM > 5 \times g_{mcrit}$. The g_{mcrit} is defined as:

$$g_{mcrit} = 4 \times (ESR_{OSC} + Rs_{EXT}) \times (2\pi \times F_{OSC})^2 \times \left(C_{0\_OSC} + C_{LOAD}\right)^2$$

where:

Table 20. Transconductance Equation – Parameters

Parameter	Description
GM	Transconductance of the MCU internal oscillator circuit
F_{OSC}	Frequency of the external crystal oscillation.
ESR_{OSC}	Equivalent series resistance of the external crystal
C_{0_OSC}	Shunt capacitance of the external crystal
C_{LOAD}	Total load capacitance on the external crystal $$C_{LOAD} = C_S + \left(\frac{[C_{XTAL} \times C_{EXTAL}]}{[C_{XTAL} + C_{EXTAL}]}\right)$$ For the frequency to be accurate, the oscillator circuit must show the same load capacitance to the crystal as the one the crystal was adjusted for. Frequency stability mainly requires that the load capacitance be constant. The external capacitors C_{XTAL} and C_{EXTAL} are used to tune the desired value of C_{LOAD} to reach the value specified by the crystal manufacturer.
C_S	Stray or parasitic capacitance on the pin due to any PCB traces, 5pF~7pF.
C_{EXTAL}	External load capacitor on EXTAL pin.
C_{XTAL}	External load capacitor on XTAL pin.
R_{S_EXT}	External series resistance connected between XTAL pin and external crystal for current limitation, Rs_{EXT} should be selected carefully to have appropriate oscillation amplitude for both protecting crystal or resonator device and satisfying proper oscillation startup condition and prevents the oscillator from vibrating at the odd harmonics of the fundamental frequency If the power dissipation in the selected crystal or oscillator is lower than the drive level (uW) specified by the crystal supplier, the insertion of Rs_{EXT} is not recommended and its value is then 0Ω. An approximation for the initial value of Rs_{EXT} can be obtained by considering the voltage divider formed by Rs_{EXT} and C_{XTAL}. Thus, the value of $Rs_{EXT}$is equal to the reactance of C_{XTAL}. Then $$Rs_{EXT} = \frac{1}{2\pi \times F_{OSC} \times C_{XTAL}}$$

Parameter	Description
	.

For example, to design the oscillation loop in a S32K3xx microcontroller with a maximum Amplifier Transconductance value $gmOSCX = 18.5\,{}^{mA}/_{V}$ for a frequency range 8MHz-40MHz, and it is selected the crystal *AT-16.000MAGE-x - 16MHz /TXC* crystal, with the following characteristics:

Table 21. Example – Pierce Oscillator Design

Parameter	Value	Value	Units
F_{OSC}	Frequency of the external crystal oscillation.	16	MHZ
ESR_{OSC}	Equivalent series resistance of the external crystal	60	Ω
Rs_{EXT}	Series resistor for current limitation	100	Ω
$C_{0\ OSC}$	Shunt capacitance of the external crystal	12	pF
C_{LOAD}	Total load capacitance on the external crystal	8	pF
C_S	Stray or parasitic capacitance on the pin due to any PCB traces	3	pF
C_{EXTAL}	External load capacitor on EXTAL pin.	10	pF
C_{XTAL}	External load capacitor on XTAL pin.	10	pF

Calculating g_{mcrit}

$$g_{mcrit} = 4 \times (60 + 100) \times (2\pi \times [16 \times 10^{6}])^2 \times ([12 \times 10^{-12}] + [8 \times 10^{-12}])^2$$

$$g_{mcrit} = 2.587\,{}^{mA}/_{V}$$

$$\therefore\ 5 \times g_{mcrit} = 12.935\,{}^{mA}/_{V}$$

Due to the Crystal oscillator transconductance ($18.5\,{}^{mA}/_{V}$) is higher than $5 \times g_{mcrit}$, The estimation of the gain margin is sufficient to start the oscillation and the oscillator is expected to reach a stable oscillation after a typical delay specified in the datasheet.

Based on the analysis and characterization of the oscillator manufacturer, the Rs_{EXT} and the values for C_{EXTAL} and C_{XTAL} can be adjusted or redefined in order to assure a safe oscillation margin. In order to check and measure the crystal oscillation or any other signal characteristics, a frequency counter equipment is useful. Oscilloscopes and spectrum analyzers are generally not recommended because these types of equipment are usually not able to distinguish main oscillation from spurious), and the other hand, if the probes of the oscilloscope (despite that some probes are of low impedance) are connected directly to the oscillation circuit, it will stop and may affect or attenuate the crystal's oscillations.

3.3 Pinout differences between *S32K344-172MaxQFP V1.0* and *S32K344-172MaxQFP V1.1*

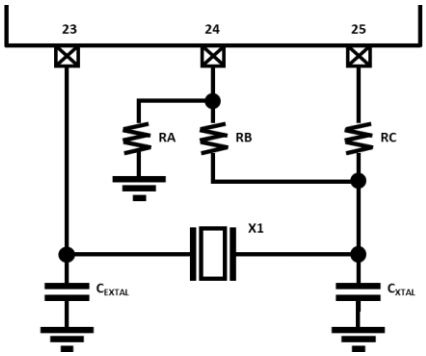
Table 22. 2.13 Pinout differences between S32K344-172MaxQFP V1.0 and S32K344-172MaxQFP V1.1

MCU Pin Number	S32K344 - 172MaxQFP V1.0		S32K344 - 172MaxQFP V1.1	
	Pin Name	Pin Function	Pin Name	Pin Function
23	EXTAL	External Crystal Input	EXTAL	External Crystal Input
24	XTAL	External Crystal Output	GND	External Crystal Output
25	PTA26	GPIO	XTAL	External Crystal Output

1. The S32K344-172MAXQFP [*V1.0*] is a predecessor version of the S32K344 /42 /24 /22 /14-172MAXQFP [*V1.1*] versions.
2. The S32K344-172MAXQFP [*V1.0*] version is used just for prototypes and initial hardware and software enablement purposes, not for high production or new designs.

3.3.1 Topology Recommended for a drop-in replacement between a S32K344-172MaxQFP/V1.0 and S32K344 -172MaxQFP/V1.1

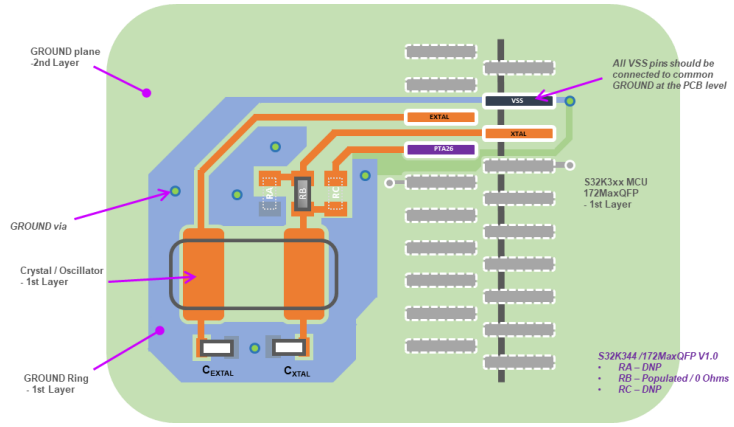
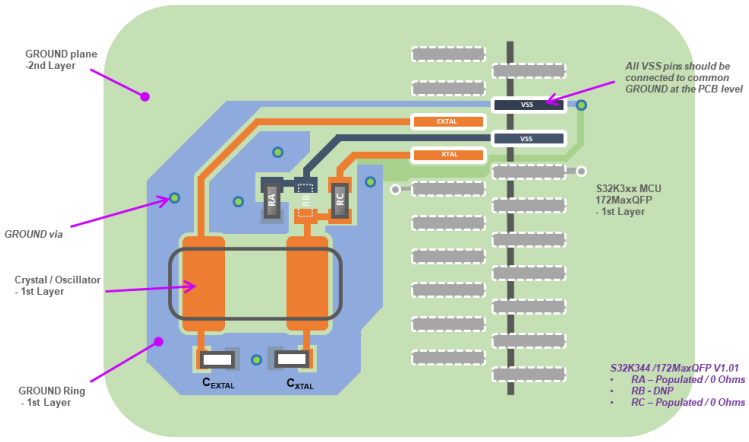
Table 23. Topology Recommended for a drop-in replacement between a S32K344-172MaxQFP/V1.0 and S32K344 -172MaxQFP/V1.1



S32K344 /172MaxQFP V1.0
RA – DNP
RB – Populated / 0 Ohms
RC – DNP

S32K344 /172MaxQFP V1.1
RA – Populated / 0 Ohms
RB – DNP
RC – Populated / 0 Ohms

Figure 38. Topology Recommended for a drop-in replacement between a S32K344-172MaxQFP/V1.0 and S32K344 -172MaxQFP/V1.1

MCU Pin Number	Topology Recommended for a drop-in replacement between a S32K344-172MaxQFP/V1.0 and S32K344 -172MaxQFP/V1.1
S32K344 172MaxQFP V1.0	
S32K344 172MaxQFP V1.1	

MCU Pin Number	Topology Recommended for a drop-in replacement between a S32K344-172MaxQFP/V1.0 and S32K344 -172MaxQFP/V1.1

1. The S32K344-172MAXQFP [*V1.0*] is a predecessor version of the S32K344 /42 /24 /22 /14-172MAXQFP [*V1.1*] versions.
2. The S32K344-172MAXQFP [*V1.0]* version is used just for prototypes and initial hardware and software enablement purposes, not for high production or new designs.

4 Debug and programing interface

4.1 RESET system

Resetting the MCU provides a way to start processing from a known set of initial conditions. System reset begins with the on-chip regulator in full regulation and system clocking generation from an internal reference.

4.1.1 External pin RESET

For all reset sources, the RESET_B pin is driven low by the MCU for at least 128 bus clock cycles and until flash memory initialization has completed. After flash memory initialization has completed, the RESET_B pin is released and the internal chip reset desserts. Keeping the RESET_B pin asserted externally delays the negation of the internal chip reset. The RESET pin is the same as the standard SIUL2_GPIO/eMIOS_GPIO. It can operate as a pseudo-open-drain output because there is also a PMOS device in the output stage.

The reset pin, similar to some other GPIO has a weak internal pull-up. If the environment and the customer application is noisy, an external pull up resistor to VDD_HV_A must be added directly to the reset pin in order to avoid a sporadic or unintended reset occurs. Refer to the device datasheet for the levels of voltage and current allowed in the pin. Despite a capacitor in the reset line is not directly required for the MCU. In some cases, in order to add a further ESD protection, an external capacitor is added between the RESET pin to ground and this capacitor must be place as close as possible and directly to the debug interface or connector. The values of the pull up resistor and the capacitor must be selected according to the design requirements of the application. Refer to the device datasheet for the minimum RESET pulse value that can be detected for the MCU.

4.2 JTAG and TRACE interface

A number of commonly used debug connectors are shown here. Most of the Arm® development tools uses one of these pins. When developing your Arm® circuit board, it is recommended to use a standard debug signal arrangement to make connection to debugger easier:

Table 24. JTAG signal description

Signal Name	Signal Description	MCU Pin Name	S32K3 MCU Package - Pin Number								Recommendation	I/O Power Domain
			S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP V1.0 and V1.1	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA		
JTAG_TDO	JTAG Test Data Output	PTA10	44	92	92	161	161	G8	161	G8	Pull-Up	VDD_HV_A
JTAG_TDI	JTAG Test Data Input	PTC5	45	95	95	165	165	F8	165	F8	Pull-Up	
JTAG_TCK / SWD_CLK	Clock into the core	PTC4	46	96	96	166	166	F7	166	F7	Pull-Down	
JTAG_TMS / SWD_DIO	JTAG Test Mode Select	PTA4	48	98	98	170	170	F6	170	F6	Pull-Up	
RESET	Reset MCU	PTA5	47	97	97	167	167	A3	167	A3	Pull-Up	
External pull up/down resistors for the JTAG signals can be added to increase debugger connection robustness.												

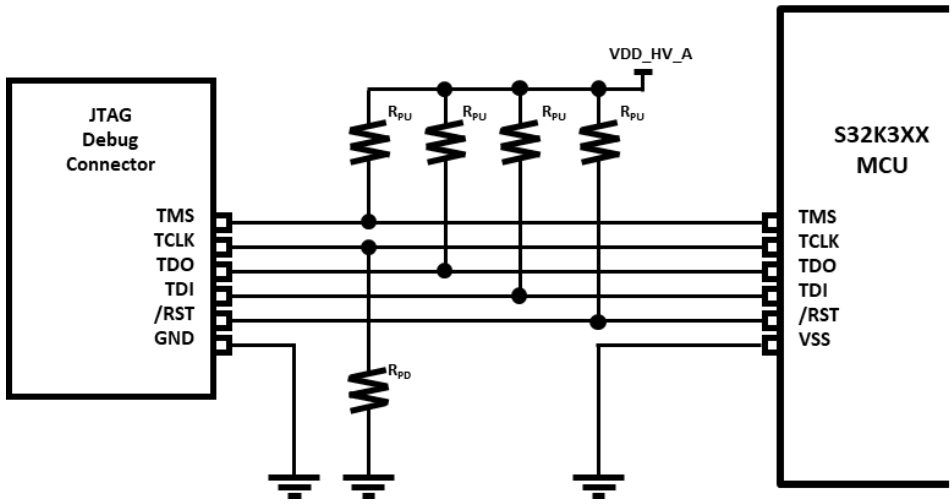


Figure 39. JTAG Pin Connections

Table 25. JTAG connector – Component description

Symbol	Parameter	Typ Value Range	Units
R_{PU}	Pull up Resistor	4.7k-10k	Ω
R_{PD}	Pull down Resistor	4.7k-10k	Ω

4.3 Debug connector pinouts

4.3.1 20-pin Cortex® Debug-D ETM connector

Some newer ARM® microcontroller board use a 0.05” 20-pin header (*Samtec FTSH-110*) for both debug and trace. (The 20-pin Cortex® Debug D ETM connector support both JTAG and Serial Wire debug protocols. When the Serial debug protocol is used, the TDO signal can be used for Serial Wire Viewer output for trace capture. The connector also provides a 4-bit wide trace port for capturing of trace that require a higher trace bandwidth (example, when ETM trace is enabled).

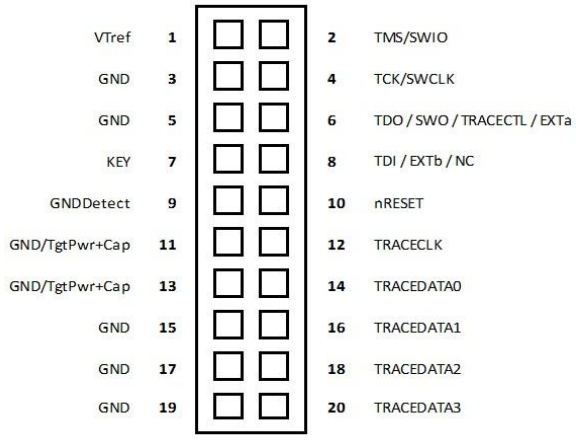


Figure 40. 20-pin Cortex® Debug D ETM connector pin layout

4.3.2 10-pin Cortex® Debug connector

For device without ETM, you can use an even smaller 0.05” 10-pin connector (*Samtec FTSH-105)* for debug. Similar to the 20pin Cortex® Debug D ETM connector, both JTAG and Serial-Wire debug protocols are supported in the 10-pin version.

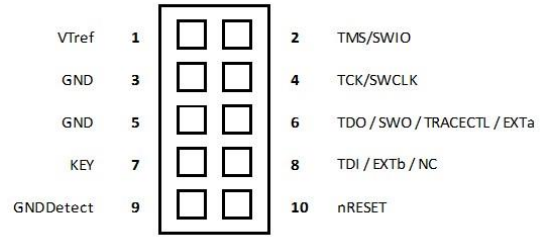


Figure 41. 10-pin Cortex® Debug connector pin layout

4.3.3 Legacy 20-pin IDC connector

A common debug connector used in Arm® development boards is the 20-pin IDC connector. The 20-pin IDC connector arrange support JTAG debug, Serial Wire debug (SWIO and SWCLK), Serial Wire Output (SWO). The nICEDETECT pin allows the target system to detect if a debugger is connected. When no debugger is attached, this pin is pulled high. A debugger connection connects this pin to ground. This is used in some development boards that support multiple JTAG configurations. The nSRST connection is optional; debugger can reset a Cortex®-M system via the System Control Block (SCB), so this connection is often omitted from the top level of microcontroller designs.

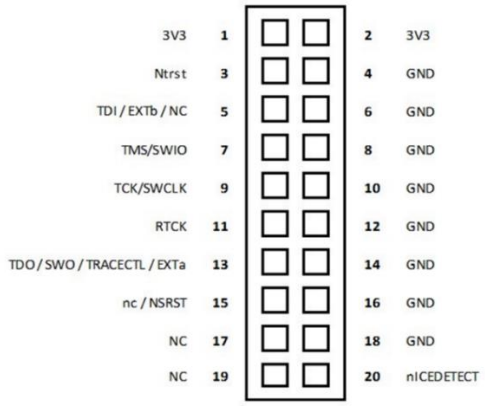


Figure 42. 20-pin IDC connector

4.3.4 38-pin Mictor connector

In some ARM® system designs, Mictor connector is used when trace port is required (example, for instruction trace with ETM). It can also be used for JTAG/SWD connection. The 20-pin IDC connector can be connected in parallel with the Mictor connector (only one is use at a time).

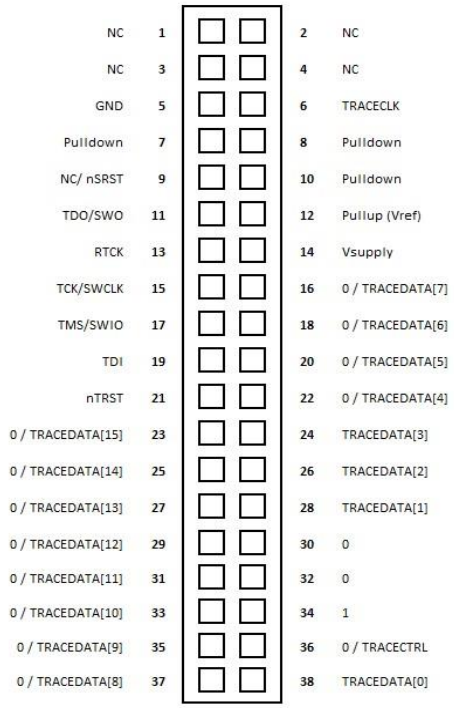


Figure 43. 20-pin IDC connector

Typically, a Cortex®-M3 or Cortex®-M4 microcontroller only has 4-bit of trace data signals, so most of the trace data pins on the Mictor connectors are not used. The Mictor connector is used mostly in other ARM® Cortex® processors (Cortex®A8/A9, Cortex®-R4) or in some multiprocessor systems the trace system might require a wider trace port. In such cases, some of the other unused pins on the connector will also be used. For a typical Cortex®-M3 or Cortex®-M4 system, the Cortex® Debug D ETM connector is recommended.

Table 26. TRACE signal description

Signal Name	MCU Pin Name	S32K3 MCU Package - Pin Number								I/O Power Domain	Comment
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA	**S32K3x8** 172MAXQFP + EP	**S32K3x8** 289MBGA		
TRACE_ETM_CLKOUT	PTC2	-	-	-	50	50	T4	50	T4	VDD_HV_B	See note [1]
	PTC1	-	-	-	-	-	-	61	T8	VDD_HV_A	
	PTG6	-	-	-	-	-	K7	-	K7	VDD_HV_A	See note [2]
	PTH4	-	-	-	-	-	-	-	E12	VDD_HV_A	
TRACE_ETM_D0	PTD7	-	-	-	51	51	U4	51	U4	VDD_HV_B	See note [1]
	PTC0	-	-	-	-	-	K6	62	U7	VDD_HV_B	
	PTG7	-	-	-	-	-	K6	-	K6	VDD_HV_A	See note [2]
	PTG28	-	-	-	-	-	-	-	H5	VDD_HV_A	
TRACE_ETM_D1	PTD12	-	-	-	54	54	R5	54	R5	VDD_HV_B	See note [1]
	PTD9	-	-	-	-	-	-	63	U8	VDD_HV_B	
	PTG15	-	-	-	-	-	L6	-	L6	VDD_HV_A	See note [2]
	PTG29	-	-	-	-	-	-	-	G5	VDD_HV_A	
TRACE_ETM_D2	PTD11	-	-	-	55	55	U6	55	U6	VDD_HV_B	See note [1]
	PTD18	-	-	-	-	-	-	64	R8	VDD_HV_A	
	PTG16	-	-	-	-	-	M8	-	M8	VDD_HV_A	See note [2]
	PTG30	-	-	-	-	-	-	-	F5	VDD_HV_A	
TRACE_ETM_D3	PTD10	-	-	-	56	56	T6	56	T6	VDD_HV_B	See note [1]
	PTC17	-	-	-	-	-	-	65	R6	VDD_HV_B	
	PTF31	-	-	-	-	-	L9	-	L9	VDD_HV_A	See note [2]
	PTG31	-	-	-	-	-	-	-	E6	VDD_HV_A	
TRACE_ETM_D4	PTG17	-	-	-	-	-	M9	-	M9	VDD_HV_A	
	PTH0	-	-	-	-	-	-	-	E7	VDD_HV_A	
TRACE_ETM_D5	PTF28	-	-	-	-	-	L10	-	L10	VDD_HV_A	
	PTH1	-	-	-	-	-	-	-	E8	VDD_HV_A	
TRACE_ETM_D6	PTG18	-	-	-	-	-	M10	-	M10	VDD_HV_A	
	PTH2	-	-	-	-	-	-	-	E10	VDD_HV_A	
TRACE_ETM_D7	PTG19	-	-	-	-	-	M11	-	M11	VDD_HV_A	
	PTH3	-	-	-	-	-	-	-	E11	VDD_HV_A	
TRACE_ETM_D8	PTG20	-	-	-	-	-	L12	-	L12	VDD_HV_A	
	PTH5	-	-	-	-	-	-	-	F13	VDD_HV_A	
TRACE_ETM_D9	PTG21	-	-	-	-	-	K12	-	K12	VDD_HV_A	
	PTH6	-	-	-	-	-	-	-	G13	VDD_HV_A	
TRACE_ETM_D10	PTG22	-	-	-	-	-	J12	-	J12	VDD_HV_A	
	PTH7	-	-	-	-	-	-	-	K13	VDD_HV_A	
TRACE_ETM_D11	PTG23	-	-	-	-	-	H12	-	H12	VDD_HV_A	
	PTH8	-	-	-	-	-	-	-	L13	VDD_HV_A	
TRACE_ETM_D12	PTG24	-	-	-	-	-	G12	-	G12	VDD_HV_A	
	PTH9	-	-	-	-	-	-	-	M13	VDD_HV_A	
TRACE_ETM_D13	PTG25	-	-	-	-	-	F12	-	F12	VDD_HV_A	
	PTH10	-	-	-	-	-	-	-	N13	VDD_HV_A	
TRACE_ETM_D14	PTG26	-	-	-	-	-	F11	-	F11	VDD_HV_A	
	PTH11	-	-	-	-	-	-	-	N12	VDD_HV_A	
TRACE_ETM_D15	PTG27	-	-	-	-	-	F1 0	-	F10	VDD_HV_A	
	PTH12	-	-	-	-	-	-	-	N11	VDD_HV_A	

1. For a 257bga version. If QSPIA and/or Ethernet functions are required in the customer application, then the TRACE function must be selected just on the VDD_HV_A domain.
2. For the S32K344 /42 /24 /22 /14 - 172MaxQFP versions. The user should select one function between TRACE or QSPIA on the VDD_HV_B domain for the application.

5 Communication modules

5.1 LIN interface

The Local Interconnect Network (LIN) is a serial communication protocol, designed to support automotive networks. As the lowest level of a hierarchical network, LIN enables cost-effective communication with sensors and actuators when all the features of CAN are not required. The LIN bus topology utilizes a single master and multiple nodes, as shown below. Connecting application modules to the vehicle network makes them accessible for diagnostics and service.

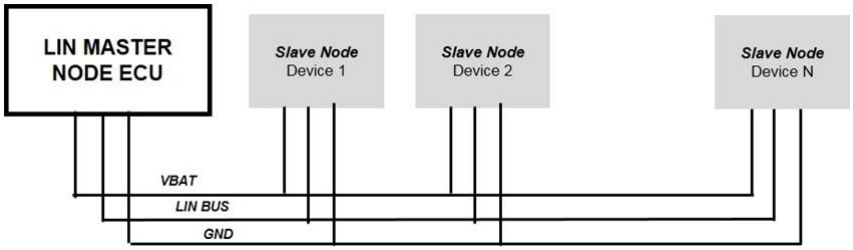


Figure 44. LIN bus topology

The LIN physical layer has is a low-side MOSFET with a current limitation and overcurrent transmitter shutdown. A selectable internal pullup resistor with a serial diode structure is integrated, so no external pull-up components are required for the application in a slave node. To be used as a master node, an external resistor of 1 kΩ in series with a diode must be placed in parallel between VBAT [Battery Voltage] and the LIN Bus line. The fall time from recessive to dominant and the rise time from dominant to recessive is selectable and controlled to guarantee communication quality and reduce EMC emissions.

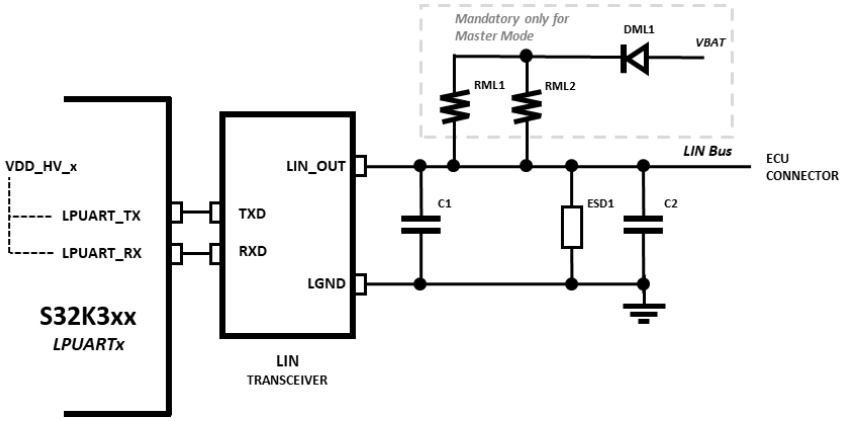


Figure 45. Block diagram for LIN interface

NOTE

In the applications where the user/customer is using different voltage levels in the MCU domains (*for example VDD_HV_A = +5.0 and VDD_HV_B = +3.3V*). The user must select that the LPUARTx_TX/RX data lines have the same voltage domain, VDD_HV_A or VDD_HV_B; and are within the range allowed for communication with the LIN Physical layer.

5.1.1 LIN components data

Table 27. LIN components

Reference	Part	Mounting	Remark
DMLIN	Diode	Mandatory only for master ECU	Reverse Polarity protection from LIN to Battery Voltage.
RML1 and RML2	Resistor: 2 kΩ Power Loss: 250 mW Tolerance: 1% Package Size: 1206 Requirement: Min Power rating of the complete master termination must be ≥500nW	Mandatory only for Master ECU	For Master ECU If more than 2 resistors are used in parallel, the values must be chosen in a way that the overall resistance RM of 1 kΩ and the minimum power loss of the complete master termination must be fulfilled. For Slave ECU RMLIN1 and RMLIN2 are not needed on the PCB layout
C1	Capacitor: Slave ECU: typically, 220 pF Master ECU: from 560 pF up to approximately ten times that value in the slave node [CSLAVE], so that the total line capacitance is less dependent on the number of slave nodes. Tolerance: 10% Package Size: 0805 Voltage: ≥50 V	Mandatory	The value of the master node must be chosen in a way that the LIN specification is fulfilled.
C2	Capacitor: Package Size: 0805	Optional	Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.
ESD1	ESD Protection Package Size: 0603-0805	Optional	Layout pad for an additional ESD protection part. Mounting of the optional part only allowed if there is an explicit written permission of the respective OEM available. Place close to the connector.

5.2 CAN interface

The physical layer characteristics for CAN are specified in ISO-11898-2. This standard specifies the use of cable comprising parallel wires with an impedance of nominally 120 Ω (95 Ω as minimum and 140 Ω as maximum). The use of shielded twisted pair cables is generally necessary for electromagnetic compatibility (EMC) reasons, although ISO-11898-2 also allows for unshielded cable. A maximum line length of 40 meters is specified for CAN at a data rate of 1 Mb. However, at lower data rates, potentially much longer lines are possible. ISO-11898-2 specifies a line topology, with individual nodes connected using short stubs.

Though not exclusively intended for automotive applications, CAN protocol is designed to meet the specific requirements of a vehicle serial data bus: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth. Each CAN station is connected physically to the CAN bus lines through a transceiver device. The transceiver is capable of driving the large current needed for the CAN bus and has current protection against defective CAN or defective stations. A typical CAN system with an S32K3XX microcontroller is shown in Figure 46.

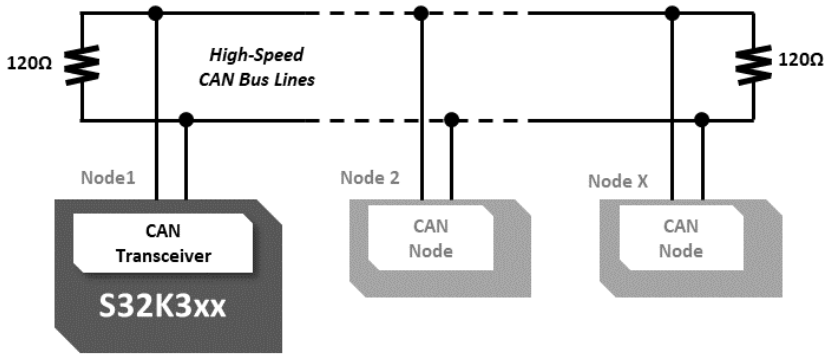


Figure 46. CAN system

The CAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads up to 64 bytes transferred at faster rates up to 8 Mbps. The message buffers are stored in an embedded RAM dedicated to the CAN module. See the chip configuration details in the Reference Manual for the number of message buffers configured in the chip.
Like most others CAN physical transceivers, the CANH, CANL and SPLIT pins are available for the designer to terminate bus depending on the application. The Figure 47 and Figure 48 show examples of the CAN node terminations.

NOTE

In the applications where the user/customer is using different voltage levels in the MCU domains (*for example VDD_HV_A = +5.0 and VDD_HV_B = +3.3V*). The user must select that the CANx_TX/RX data lines have the same voltage domain, VDD_HV_A or VDD_HV_B; and are within the range allowed for communication with the CAN Physical layer.

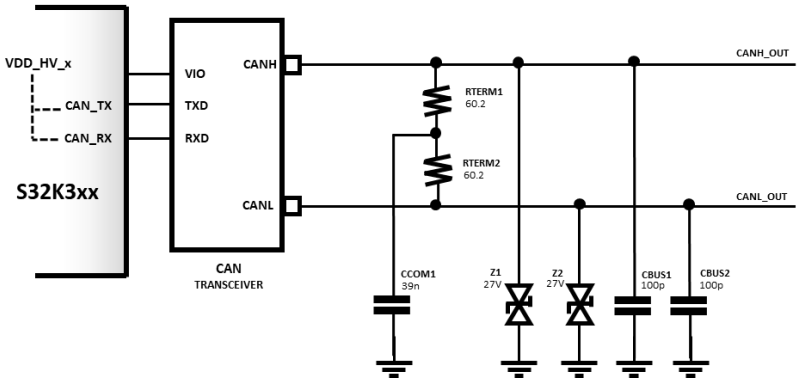


Figure 47. CAN physical transceiver circuit

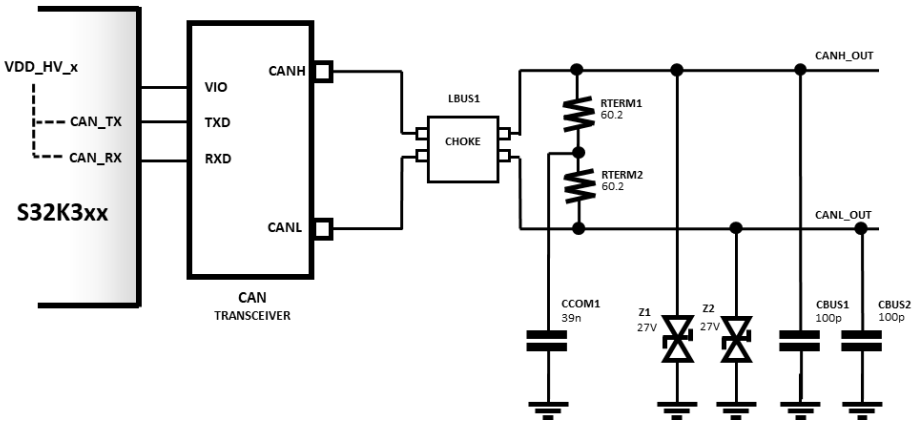


Figure 48. CAN Physical transceiver circuit with common mode choke

5.2.1 CAN components data

Table 28. CAN components

Reference	Description
CBUS1 and CBUS2	The Capacitors CBUS1 and CBUS2 are not specifically required. They may be added for EMC reasons, in which case the maximum capacitance from either bus wire to ground must not exceed 300 pF total. If Zener stacks are also needed, the parasitic capacitance of the Zener stacks must also be included in the total capacitance budget.
Z1 and Z2	The Zener stacks Z1 and Z2 could be required to satisfy Automotive EMC requirements (ESD in particular). These devices should be placed close to the connector.
RTERM1, RTERM2 and CCOM1	Depending on the position of the node within the CAN network it might need a specific termination. RTERM1, RTERM2 and CCOM1 must be that they assist in having an overall cable impedance. On a bus implementation of a CAN network only the two nodes on the two ends of the bus have terminator resistors. The nodes not placed on the end of the CAN bus do not have termination. A thorough analysis is required to maintain this requirement of the CAN networks. The SPLIT pin on the transceiver is optional and the designer might choose not to use it. This pin helps stabilize the recessive state of the CAN bus and can be enabled or disabled by software when required.
LBUS1–Common mode choke	A common mode choke on the CANH and CANL lines can help reduce coupled electromagnetic interference and needed to satisfy Automotive EMC requirements. This choke, together with transient suppressors on the transceiver pins can greatly reduce coupled electromagnetic noise, and high frequency transients. LBUS1 is not specifically required.

5.2.2 CAN termination

In a transmission line, there are two current paths, one to carry the currents from the driver to the receiver and another to provide the return path back to the driver. In the CAN transmission lines is more complex because there are two signals that are sharing a common termination as well as a ground return path. For reliable CAN communications, it is essential that the reflections in the transmission line be kept as small as possible. This can only be done by proper cable termination. Figure 49 and Figure 50. demonstrate two CAN termination schemes.

Reflections happen very quickly during and just after signal transitions. On a long line, the reflections are more likely to continue long enough to cause the receiver to misread logic levels. On short lines, the reflections occur much sooner and have no effect on the received logic levels.

5.2.2.1 Parallel termination

In CAN applications, both ends of the bus must be terminated because any node on the bus may transmit/receive data. Each end of the link has a termination resistor equal to the characteristic impedance of the cable, although the recommended value for the termination resistors is nominally 120 Ω (100 Ω as minimum and 130 Ω as maximum).

There should be no more than two terminating resistors in the network, regardless of how many nodes are connected, because additional terminations place extra load on the drivers. ISO-11898-2 recommends not integrating a terminating resistor into a node, but rather attaching standalone termination resistors at the furthest ends of the bus. This is to avoid a loss of a termination resistor if a node containing that resistor is disconnected. The concept also applies to avoiding the connection of more than two termination resistors to the bus or locating termination resistors at other points in the bus rather than at the two ends.

Figure 49. CAN Bus - parallel termination

5.2.2.2 Parallel termination with common-mode filtering

To further enhance signal quality, split the terminating resistors at each end in two and place a filter capacitor, CSPLIT, between the two resistors. This filters unwanted high frequency noise from the bus lines and reduces common-mode emissions.

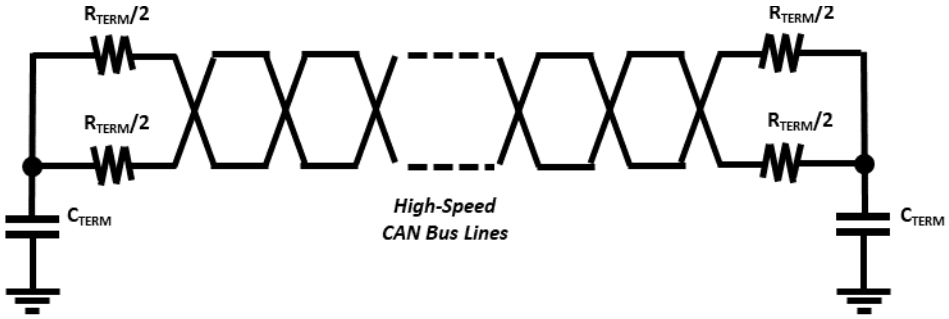


Figure 50. CAN Bus – parallel transmission with common-mode filtering

5.3 Ethernet MAC Interface

MII/RMII Interface signal can be directly routed to the MAC-NET interface, however series termination resistors may be considerate on RXCLK, TXCLK and all RX/TX signals for EMI suppression. MII/RMII series termination should be placed within 100 of the Ethernet Physical Interface and routed to an uninterrupted reference plane. 33-50 Ohms series termination resistors have been to be good recommended value for improving EMI.

Although RMII and MII are synchronous bus architectures, there are a number of factors limiting signal trace lengths. With a longer trace, the signal becomes more attenuated at the destination and thus more susceptible to noise interference. Longer traces also act as antennas, and if run on the surface layer, can increase EMI radiation. If a long trace is running near and adjacent to a noisy signal, the unwanted signals could be coupled in as cross talk. It is recommended to keep the signal trace lengths as short as possible. Ideally, keep the traces under 6 inches. Trace length matching, to within 2.0 inches on the MII or RMII bus is also recommended. Significant differences in the trace lengths can cause data timing issues. Minimize the use of vias throughout the design. Vias add capacitance to signal traces. As with any high-speed data signal, good design practices dictate that impedance should be maintained and stubs should be avoided throughout the entire data path.

Because the TX and RX data signals are triggered by the rising edge of the clock, communication in MII and RMII is synchronous. Therefore, the length of the EMAC data lines and the clock line between the K3 Microcontroller and the PHY must be matched. The allowed deviation in length matching depends on the rise/fall time for digital signals between these two elements, although it is generally recommended that any deviation be less than 10 mm as MII and RMII

MII signaling: Figure 51 shows the PHY-MAC and MAC-MAC connections in an MII interface. Data is exchanged via 4-bit wide data nibbles TXD[3:0] and RXD[3:0]. Data transmission is synchronous with the transmit (TX_CLK) and receive (RX_CLK) clocks. For the

PHY-MAC interface, both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal 25 MHz or from the CLK_OUT signal on the switch. When the Ethernet Switch is configured for MAC-MAC communication, the switch provides the clocks and acts like a PHY.

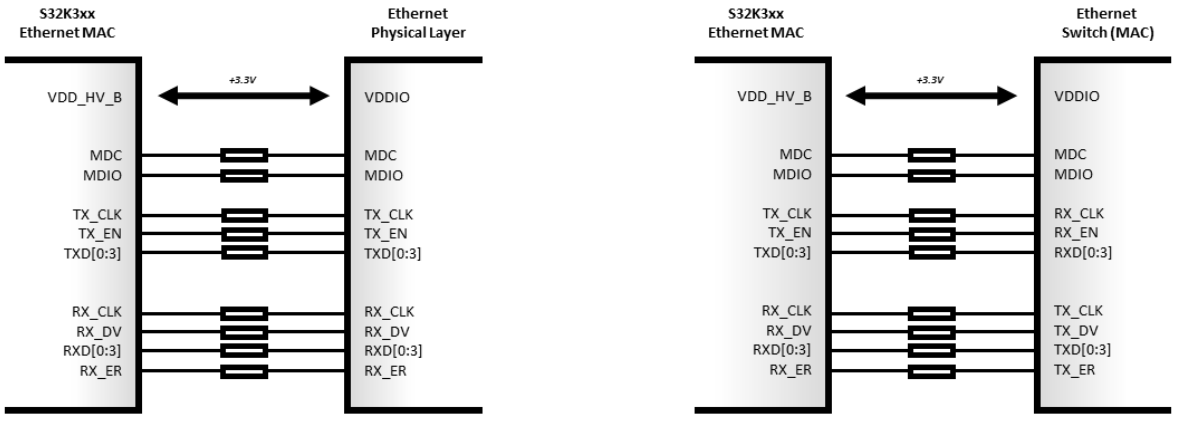


Figure 51. MII interface connections – Block Diagram

RMII signaling: RMII data is exchanged via 2-bit data signals TXD[1:0] and RXD[1:0] as shown in Figure 52. Transmit and receive signals are synchronous with the shared reference clock, REF_CLK.

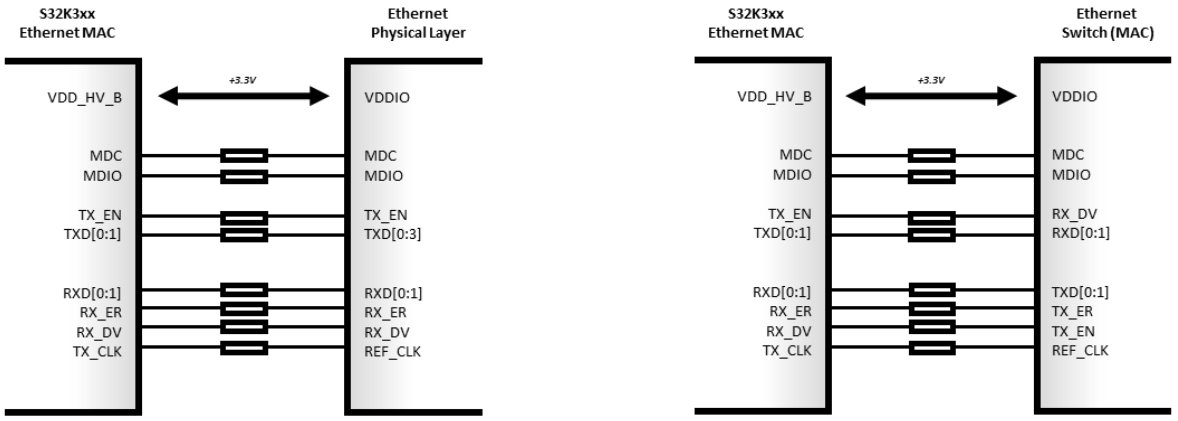


Figure 52. RMII interface connections – Block Diagram

NOTE

All signals of the Ethernet MAC module of the S32K3XX Microcontroller are in the VDD_HV_B domain. A method for voltage level translation is not required in the Ethernet Physical layer or MAC interface since the VDD_HV_B domain should be connected to +3.3V.

6 Quad Serial Peripheral Interface

The S32K3XX MCU has one instance of QuadSPI. The Quad Serial Peripheral Interface (QuadSPI) block acts as an interface to an external serial flash device. It supports SDR mode up to 4 bidirectional data lines respectively. The QuadSPI supports an A-side. As such the following external memory options can be supported:

• Single Quad Flash on the A-side

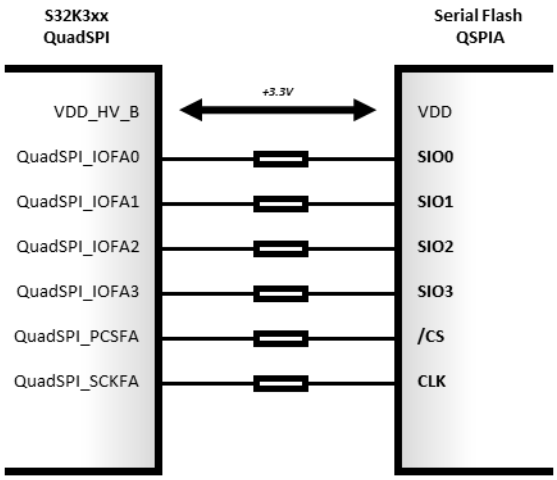


Figure 53. Block Diagram - Single Quad serial Flash

NOTE

All signals of the QSPI module of the S32K3XX Microcontroller are in the VDD_HV_B domain. A method for voltage level translation is not required in the QSPI Memory interface since the VDD_HV_B domain should be connected to +3.3V.

Table 29. QSPI signal description

Signal Name	MCU Pin Name	S32K3 MCU Package - Pin Number						I/O Power Domain	Comment
		S32K311 48LQFP	**S32K342 /22** 100MAXQFP	**S32K314 /12 /11** 100MAXQFP	**S32K344 /42 /24 /22 /14** 172MAXQFP V1.0 and V1.11	**S32K312** 172MAXQFP	**S32K344 /24 /14** 257MBGA		
QuadSPI_PCSFA	PTC3	-	-	-	49		T3	VDD_HV_B	
QuadSPI_IOFA3	PTC2	-	-	-	50		T4	VDD_HV_B	
QuadSPI_IOFA2	PTD12	-	-	-	54		R5	VDD_HV_B	
QuadSPI_IOFA1	PTD7	-	-	-	51		U4	VDD_HV_B	
QuadSPI_IOFA0	PTD11	-	-	-	55		U6	VDD_HV_B	
QuadSPI_SCKFA	PTD10	-	-	-	56		T6	VDD_HV_B	
For the S32K344 /42 /24 /22 /14 - 172MaxQFP versions. The user should select just one function between TRACE or QSPIA for their application.									

Data and Clock Signal Termination: Clock generation and distribution becomes more difficult as the speed and performance of microprocessors increase to higher limits. Controlled and precise clocking distribution techniques are needed to maintain a synchronous system. Clock signal quality and skew are the two major problems with distributing clock signals. With higher frequencies, and the associated fast edge rates, long traces behave like transmission lines. Ring back, overshoot, and undershoot occur as a result of poor termination of transmission lines. They contribute to bad signal quality, false switching, and they can cause damage in extreme cases.

Given the effective output driver strength of 22-33 Ohms and the transmission line characteristic impedance of 50 Ohms, one should add the termination resistor close to the output driver, to minimize the reflection as shown below.

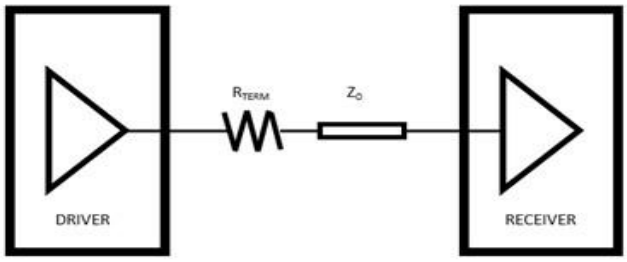


Figure 54. Point-To-Point transmission line

Data Signal Routing: In order to keep the correct timing for the data transfer from the Microcontroller to the IC Memory, the PCB data traces should be the same length and time delay as the clock trace from Microcontroller to the IC Memory. Data signals should be routed with controlled impedance traces to reduce signal reflections. Avoid routing traces with 90 ° angle corners. The recommendation is to cut the corner and smooth the trace when a trace route needs to change direction. To further improve the signal integrity, avoid using multiple signal layers for data signal routing. All signal traces should have a continuous and solid GND reference plane.

Clock Signal Routing: In high-speed synchronous data transfer, good signal integrity in a PCB design is of critical importance, especially for the clock signals, SCLK and DQS. When routing the clock signal, special cares should be taken. The following practices are recommended.

- Run the clock signal at least 3W of the trace width away from all other signal traces. This helps keep the clock signal clean from crosstalk noise.
- Use as few via(s) as possible for the whole signal path, each signal via should have a ground transition via next to them; without this, the signal routing could have an impedance change and to cause a signal reflection.
- All signal traces should go with a solid GND reference plane.
- Run the clock trace as straight as possible and avoid using serpentine routing.
- Keep a continuous ground in the next layer as reference plane.
- Keep as much space between high-speed routing (differential pairs, clock routing, etc.) and other routing. The general principle here is by spacing out traces at three times their line width, measured center to center, 70% of their electrical field can be stopped from mutual interference.

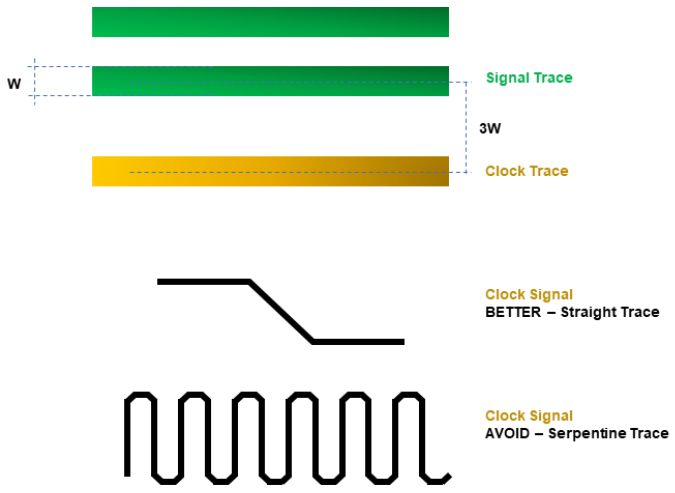


Figure 55. Recommended clock signal routing

7 Unused pins

The following table describes the options and configurations for the unused pins and the considerations for other modules and sections of the MCU.

Table 30. Used pins configuration

Module	Pin Name	Function	Recommendation
GPIO	PTx [2]	ENETx	The unused GPIO should be left unconnected or can be externally connected to VSS/GND reference. [1] [3]
		FTMx	
		FlexIOx	
		CANx	
		LPUARTx	
		LPI2Cx	
		ADCx	
		CMPx	
		Others	
External Clock	XTAL	XTAL	The pins with the XTAL and EXTAL functions must be left unconnected if are not used.
	EXTAL	EXTAL	
JTAG	PTA4	JTAG_TMS	Since these pins have either internal weak pull-ups (TDI, TDO and TMS) or pull-down (TCK) it is ok to add external pull resistors in parallel to the internal ones in order to increase debugger connection robustness. Refer to the chapter of the *Debug and programing interface*
	PTA10	JTAG_TDO	
	PTC5	JTAG_TDI	
	PTC4	JTAG_TCK	

Module	Pin Name	Function	Recommendation
RESET	PTA5	PTA5/TCLK1/RESET_b	Reset pin cannot be left unconnected. This must be pulled up to VDD_HV_A with an external resistor directly to the RESET pin. Refer to the chapter of RESET system.
Power	VDD_HV_A	Main I/O and Analog Supply Voltage	No VDD_HV_A, VREFH and VDD_HV_B power pin should be left unconnected or unpowered. All power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used to filter noise on the supplies respectively. Refer to their chapters in this document.
	VDD_HV_B	Secondary I/O Supply Voltage	
	VREFH	ADC High Reference Voltage	
	V15	High-current logic supply voltage (+1.5V)	No V15 power pin should be left unconnected or unpowered. All V15 power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used to filter noise on the supply. Refer to the chapter in this document. The V15 domain must not be used or connected to other interfaces in the application.
	V11	Core logic voltage supply (+1.1 V)	No V11 power pin should be left unconnected. All V11 power pins must be shorted together externally on their voltage domain. Appropriate bulk/bypass and decoupling capacitors should be used to filter noise on the supply. Refer to the chapter in this document. The V11 domain must not be used or connected to other interfaces in the application.
	V25	Flash memory supply (+2.5 V)	The V25 power pin should not be left unconnected; the decoupling capacitor should be used to filter noise on the supply. Refer to the chapter in this document. The V25 domain must not be used or connected to other interfaces in the application.
	PMOS_CTRL[4]	PMOS Gate Control for the SMPS option	The pin with the PMOS_CTRL function must be left unconnected if the SMPS options is not used only.[4]
	VDD_DCDC [4]		The pin with the VD_DCDC function must be left unconnected if the SMPS option is not used only.[4]
Ground	VSSx	VSSx	No VSSx/VREFL pin should be left unconnected. All VSSx/VSS_DCDC and VREFL must be shorted together externally to GND.
	VREFL	ADC Low Reference Voltage	
	VSS_DCDC	VSS/Ground Reference of the SMPS Interface.[4]	

1. The DISABLED function is default state for all pins not initialized. For digital and analog pins, this means that the corresponding SSS, IBE and OBE bits, in the SIUL_MSCR register should not modified for that particular pin.
2. Pins bonded and not bonded out.
3. If the unused pin is connected to VSS, and the pin is unintentionally configured to output with a different state (high), then there could be a path that can increase current drastically and causes major damage in the MCU.
4. For S3K3x8 versions only.

8 General board layout guidelines

8.1 Traces recommendations

A right angle in a trace can causes more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in the Figure 56.

Figure 56. Poor and correct way of bending traces in right angles

In a PCB stack-up, If two signal layers (L_N and L_{N+1}) are adjacent, the routing must be configured in order to the board layers so that these adjacent signal layers will have routing directions that cross each other instead of running parallel to each other. If layer L_N has a routing direction “north-to-south,” then make sure that L_{N+1} has a routing direction “east-to-west.” In this way, you can minimize the possibility of broadside coupling.

8.2 Grounding

Grounding techniques apply to both multi-layer and single-layer PCBs. The objective of grounding techniques is to minimize the ground impedance and thus to reduce the potential of the ground loop from circuit back to the supply.

To minimize crosstalk, Ground planes between two adjacent signal layers must be used to reduce the chance of broadside coupling even more. Not only will this increase the distance between the layers but also this configuration will give you a much better return path through the ground plane.

- Route high-speed signals above a solid and unbroken ground plane.
- If the high-speed signal requires a change of layer by a via, therefore every time a via is utilized, a ground via should also be utilized next to the signal via. This allows the return current to flow near the signal current flow and minimize that the trace changes their impedance.
- Do not split the ground plane into separate planes for analog, digital, and power pins. A single and continuous ground plane is recommended.
- There should be no floating metal/shape of any kind near any area close to the microcontroller pins. Fill copper in the unused area of signal planes and connect these coppers to the ground plane through vias.

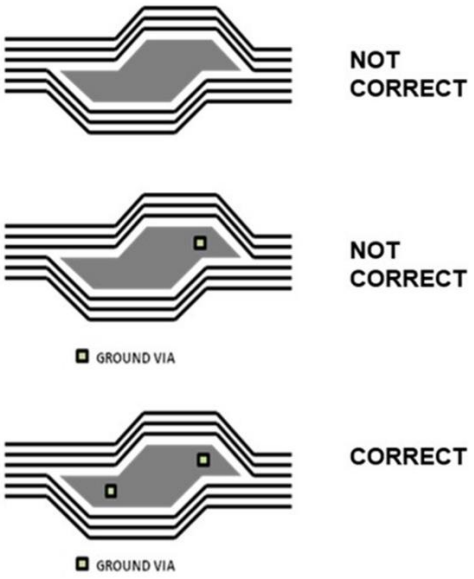
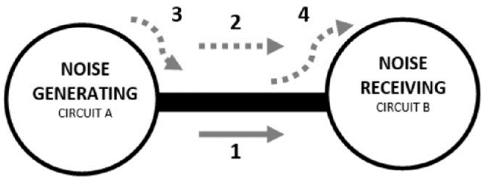


Figure 57. **Eliminating floating metal/shape**

8.3 EMI/EMC and ESD considerations for layout

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

This application note does not go into the electromagnetic theory or explain the whys of different techniques used to combat the effects, but it considers the effects and solutions most recommended as applied to CMOS circuits. EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby. Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it. The electromagnetic noise or disturbances travels via two media: Conduction and Radiation.



	Propagation path
1	Conductor
2	Air
3	Air to Conductor
4	Conductor to Air

Figure 58. **Electromagnetic noise propagation**

The design considerations narrow down to:

- The radiated & conducted EMI from the board should be lower than the allowed levels by the standards you are following.
- The ability of the board to operate successfully counteracting the radiated & conducted electromagnetic energy (EMC)from other systems around it.

The EMI sources for a system consists of several components such as PCB, connectors, cables and so on. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy, e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses and PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test. This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

Every board or system is different as far as EMI/EMC and ESD issues are concerned, requiring its own solution.
However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Ensure that the power supply is rated for the application and optimized with decoupling capacitors.
- Provide adequate filter capacitors on the power supply source. The bulk/bypass and decoupling capacitors should have low equivalent series inductance (ESL).
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.

9 CAD/CAE Schematic Symbols and PCB Footprints.

Microcontroller symbols and PCB footprints for the 289MBGA, 172MaxQFP, 172MaxQFP+EP, 100MaxQFP and 48LQFP packages are available in CADENCE format. Please find the source files attached to this S32K3XX - HW Package.

10 Package drawings

Package dimensions are provided in the package drawings. To find a package drawing, go to nxp.com and perform a keyword search for the drawing's document number:

Table 31. Package drawings

Package option	Document Number
289-ball MAPBGA	98ASA01216D
257-ball MAPBGA	98ASA01483D
172-pin MaxQFP	98ASA01107D
172-pin MaxQFP + Exposed pad	98ASA01667D
100-pin MaxQFP	98ASA01570D
48-pin LQFP	98ASH00962A

11 PCB stackup design

. The following layer stack-ups are recommended from six to sixteen-layer boards, although other options are feasible.

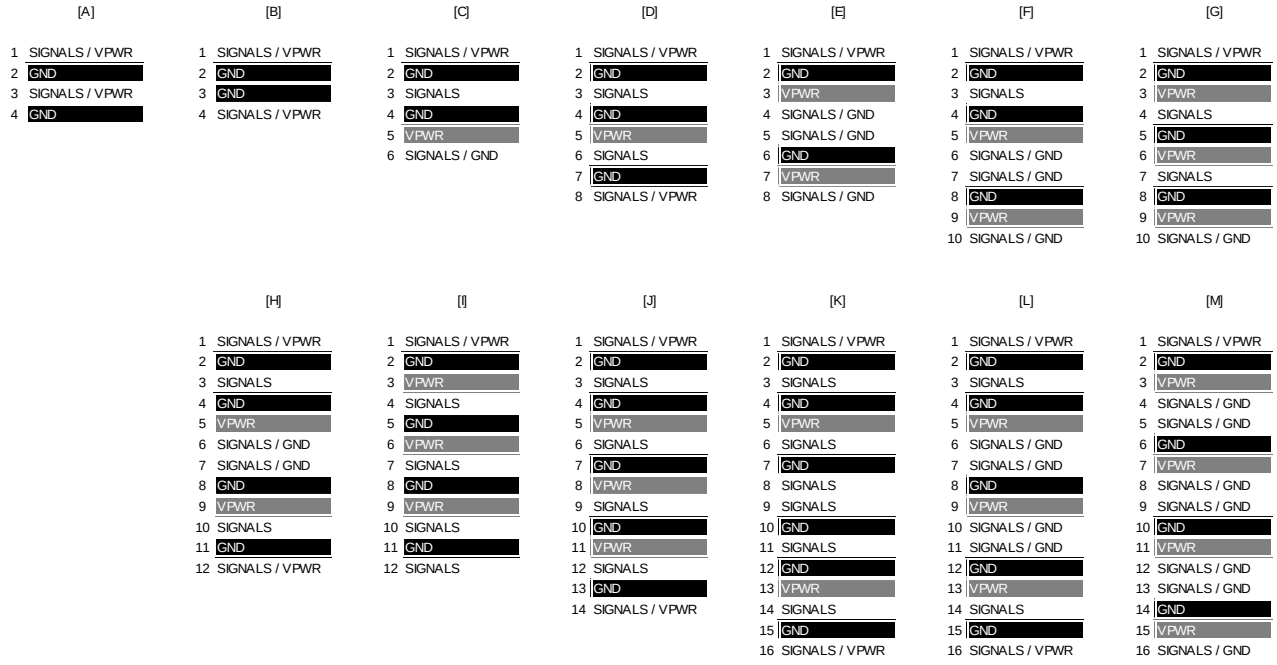


Figure 59. Recommended PCB layer stack-up

12 Injection current

All pins implement protection diodes that protect against electrostatic discharge (ESD). These internal ESD diodes of the microcontroller are designed just for short discharge pulses only, and these do not sustain a constant current over time. Therefore, the maximum continuous voltage that drops over them is specified in the DC electrical parameters and the maximum high input voltage should not be higher than VDD_HVx + 0.3 V, and the current injection also should be limited as defined in the device datasheet. In other words, the voltage and current of an input signal must be within the electrical parameter allowed. The outcome of violating these specifications causes unexpected behavior, stuck operation or damage in the MCU.

When the MCU is in an unpowered state, current injected through the chip pins may bias internal chip structures (for example, ESD diodes) and incorrectly power up these internal structures through inadvertent paths. The presence of such residual voltage may influence different chip-internal blocks in an unpredictable manner and may ultimately result in unpredictable chip behavior (for example, POR flag not set). Once in the illegal state, powering up the chip further and then applying reset will clear the illegal state. Injection current specified for the chip under the aspect of absolute maximum ratings represent the capability of the internal circuitry to withstand such condition without causing physical damage.

13 References

- Crystal Oscillator Troubleshooting Guide - NXP Semiconductors
- AN2049 Some Characteristics and Design Notes for Crystal Feedback ...
- AN10853 ESD and EMC sensitivity of IC - NXP Semiconductors
- AN2321: Designing for Board Level Electromagnetic Compatibility - NXP Semiconductors
- AN10897 A guide to designing for ESD and EMC
- AN4731 - Understanding Injection Current on NXP Automotive Microcontrollers
- AN2747 - Power Supply Design for PowerPC™ Processors

14 Revision history

Revision	Date	Substantive changes	Author
A	06/2021	• Draft version and internal review	Jesús Sanchez
B	01/2022	• Added the K358 versions • Added the K311 on 48LQFP package • Added Figure 17. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /289MBGA • Added Figure 18. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /289MBGA • Added Figure 19. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /172MaxQFP+EP • Added Figure 20. Bulk/Bypass and decoupling capacitors scheme for the S32K3x8 /172MaxQFP+EP • Added Figure 21. Bulk/Bypass and decoupling capacitors scheme for the S32K344 /257MBGA • Added Figure 22. Bulk/Bypass and decoupling capacitors scheme for the S32K344 /42 /24 /22 /14 – 172MaxQFP • Added Figure 23. Bulk/Bypass and decoupling capacitors scheme for the S32K342 - 100MaxQFP • Added Figure 24. Bulk/Bypass and decoupling capacitors scheme for the S32K312 – 172MaxQFP • Added Figure 25. Bulk/Bypass and decoupling capacitors scheme for the S32K312 /11 - 100MaxQFP • Added Figure 26. Bulk/Bypass and decoupling capacitors scheme for the S32K311 /48LQFP	
B1		• Updated Figure 22. Bulk/Bypass and decoupling capacitors scheme for the S32K344 /42 /24 /22 /14 – 172MaxQFP	
B2		• Updated Figure 37. Suggested crystal layout for the 172MaxQFP and 100MaxQFP package • Added Table 13. V15 - Component description and values for the SMPS option	
C	06/2022	• Added Figure 32. Suggestions for the PCB layout and connection of the exposed-pad in the S32K358-172MaxQFP. • Updated Figure 33. Bulk and decoupling capacitor Connection • Updated Figure 59. Recommended PCB layer stack-up • Updated Table 13. V15 - Component description and values for the SMPS option • Updated Table 15. VSS pins – MCU Ground reference	

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