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DATIS: DRAM Architecture and Technology Integrated Simulation

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Background: Why DRAM and DTCO Matter

- DRAM is a cornerstone of modern memory architecture
- DTCO improves DRAM reliability, performance, and efficiency in AI and data-driven systems

2x Intel Sapphire Rapids Server	
Component	AI Server
CPU	$ 1,850
8 GPU + 4 NVSwitch Baseboard	$ -
Memory	$ 3,930
Storage	$ 1,536
SmartNIC	$ 654
Chassis (Case, backplanes, cabling)	$ 395
Motherboard	$ 350
Cooling (Heatsinks+fans)	$ 275
Power Supply	$ 300
Assembly and Test	$ 495
Markup	$ [illegible]
Total Cost	$ [illegible]
DRAM BOM %	[illegible]
NAND BOM %	14.7%
Memory BOM %	52.2%

37.5%

DRAM accounts for over 37% of AI server costs

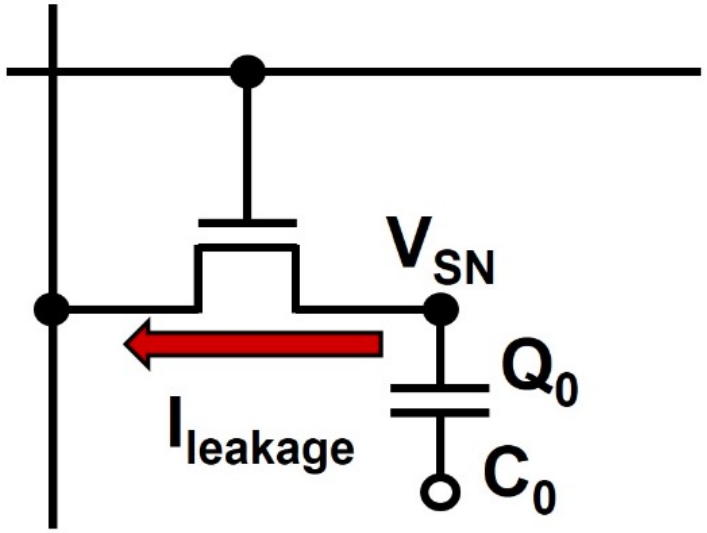
DTCO optimizes:

- optimizing system reliability
- accelerating application kernels
- enhancing architectural performance and energy efficiency

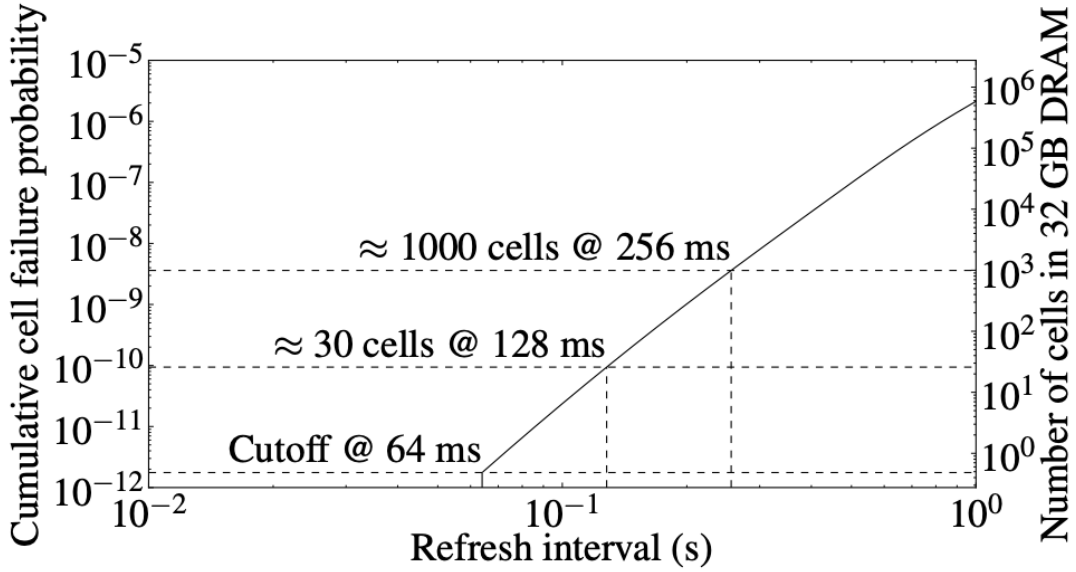
DTCO has become essential

Motivation- DTCO Case I (refresh strategies)

- Retention-aware refresh improves throughput (↑50%) and power (↓40%) [1]



DRAM cells leak charge over time



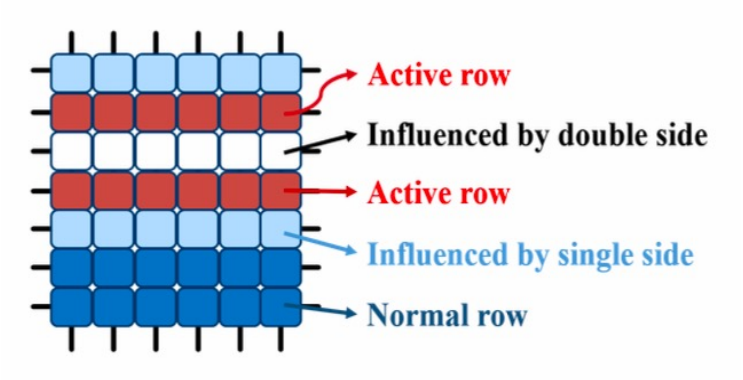
different cells lose charge at different speeds

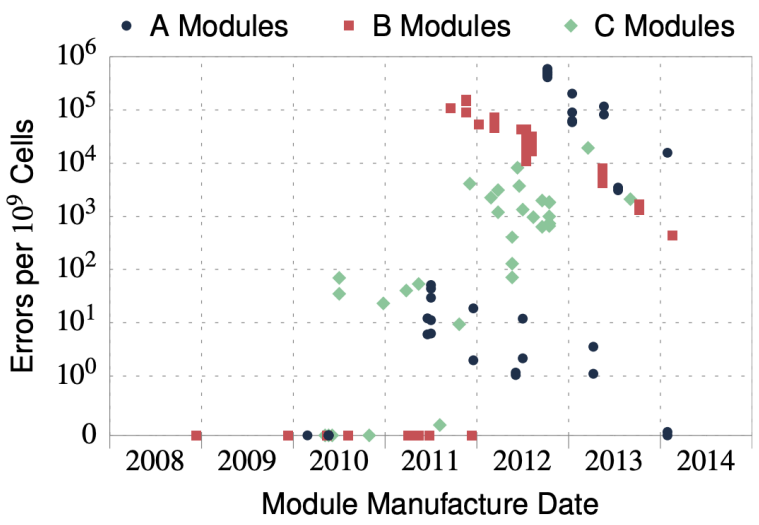
These architecture-level optimizations are highly related to process variation

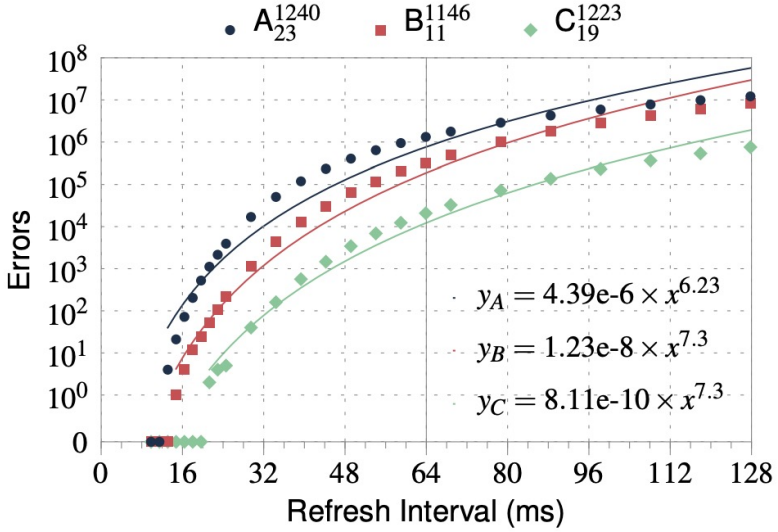
[1] J. Liu, B. Jaiyen, R. Veras, and O. Mutlu, "Raidr: Retention-aware intelligent dram refresh," ACM SIGARCH Computer Architecture News, 2012.

Motivation- DTCO Case II (RowHammer)

- Mitigate RowHammer effect by new refresh algorithms [1]







RowHammer effect

RowHammer related to process

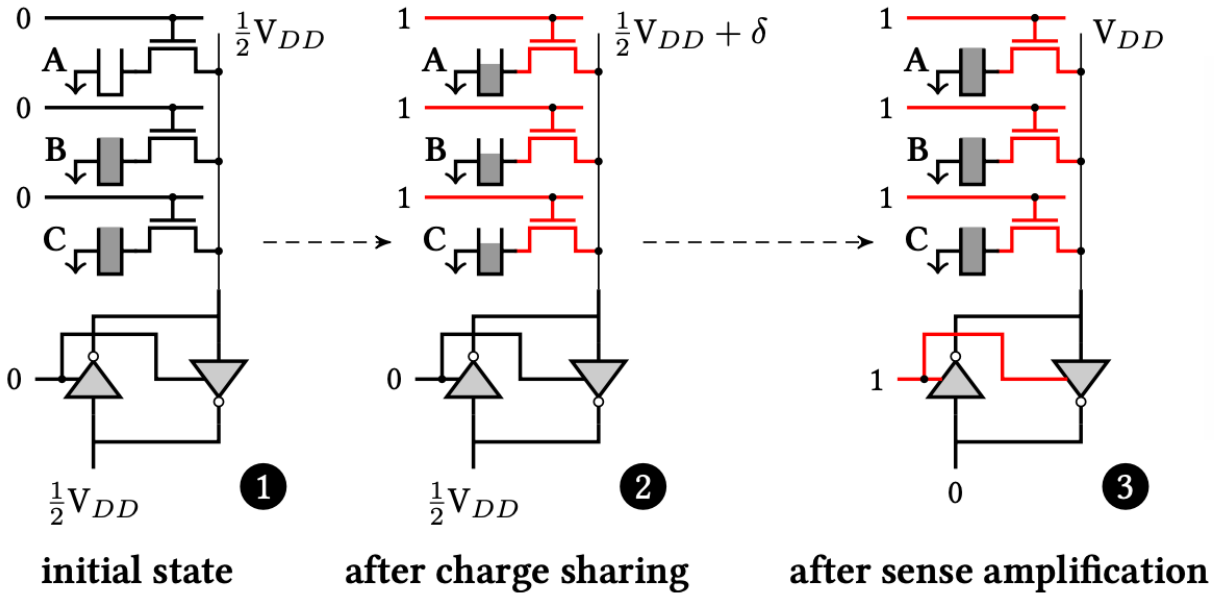
Address RowHammer effect by new refresh algorithm

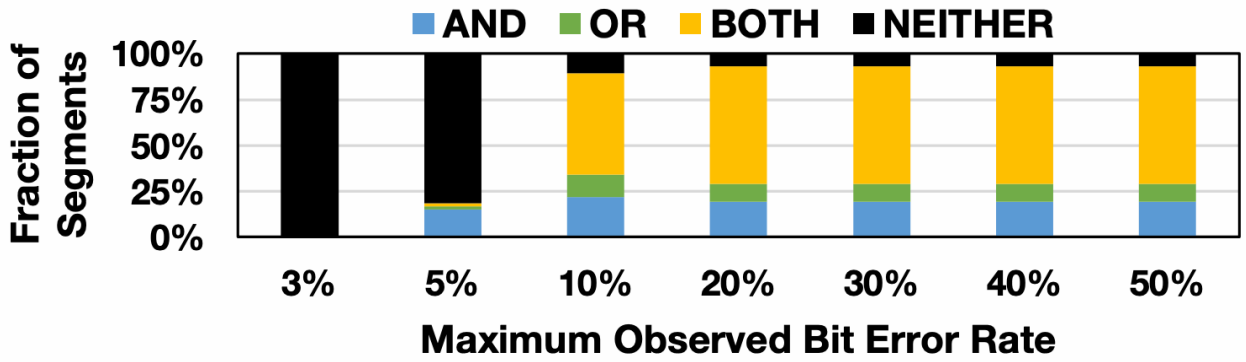
These optimizations are highly related to process variation

[1] O. Mutlu, "The rowhammer problem and other issues we may faceas memory becomes denser," in DATE, 2017. IEEE, 2017, pp. 1116–1121.

Motivation- DTCO Case III (CIM)

- Error of compute in memory (e.g. bulk bitwise AND and OR operations) related to device-level behavior (e.g. leakage and crosstalk) [1]





[2] Olgun A, Mutlu, O, et al. IEEE TCAD, 2023

CIM (AND/OR) by charge sharing

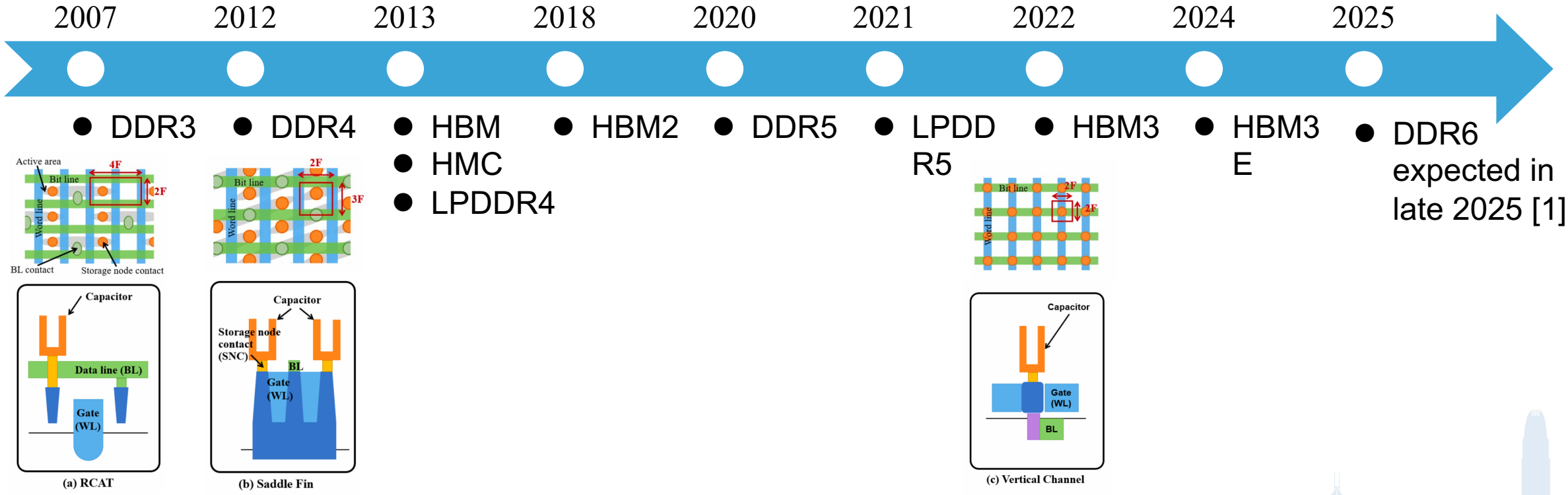
Compute error in DRAM due to device-level non-ideal factors (e.g. leakage and crosstalk)

The bit error rate in CIM is highly related to process

[1] Seshadri V, Lee D, Mullins T, et al. Ambit: In-memory accelerator for bulk bitwise operations using commodity DRAM technology[C]//Proceedings of the 50th Annual IEEE/ACM Microarchitecture. 2017.

Motivation

- DRAM and memory architecture evolve quickly (DDR4, LPDDR5, HBM, HBM3E, DDR6)



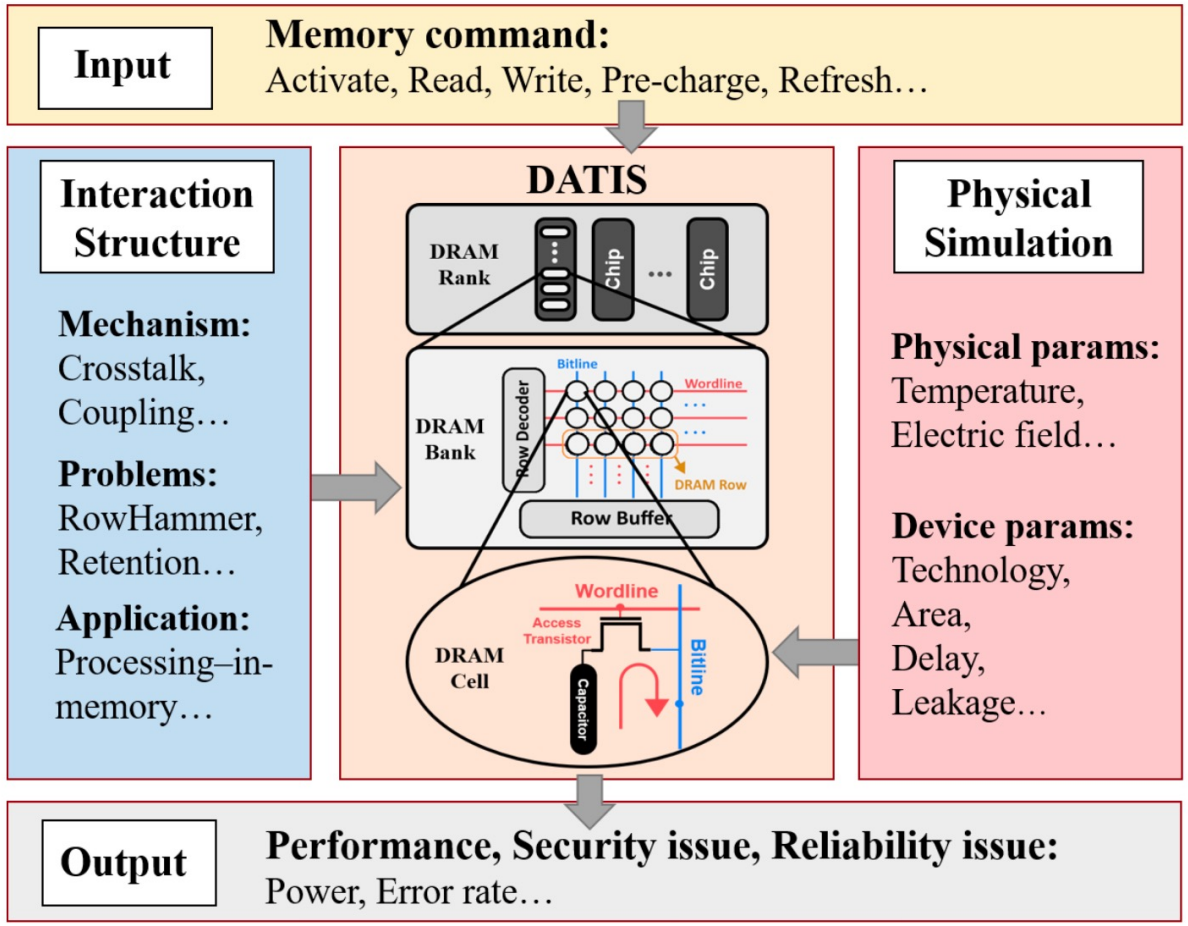
[1] PCWorld Editors. (2025). DDR6 RAM: What you should already know about the upcoming RAM standard. PCWorld. https://www.pcworld.com/article/2237799/ddr6-ram-what-you-should-already-know-about-the-upcoming-ram-standard.html

Previous work

- Existing architectural simulators ignore device-level behaviors, which are vital for DTCO studies
- A fast and extensible simulator with device-level models is very much needed

		With device-level model
USIMM	2012	❌
DRAMSim2	2011	❌
DRAMSim3	2020	❌
Ramulator	2015	❌
Ramulator2	2023	❌
This work	2025	✅

What is DATIS

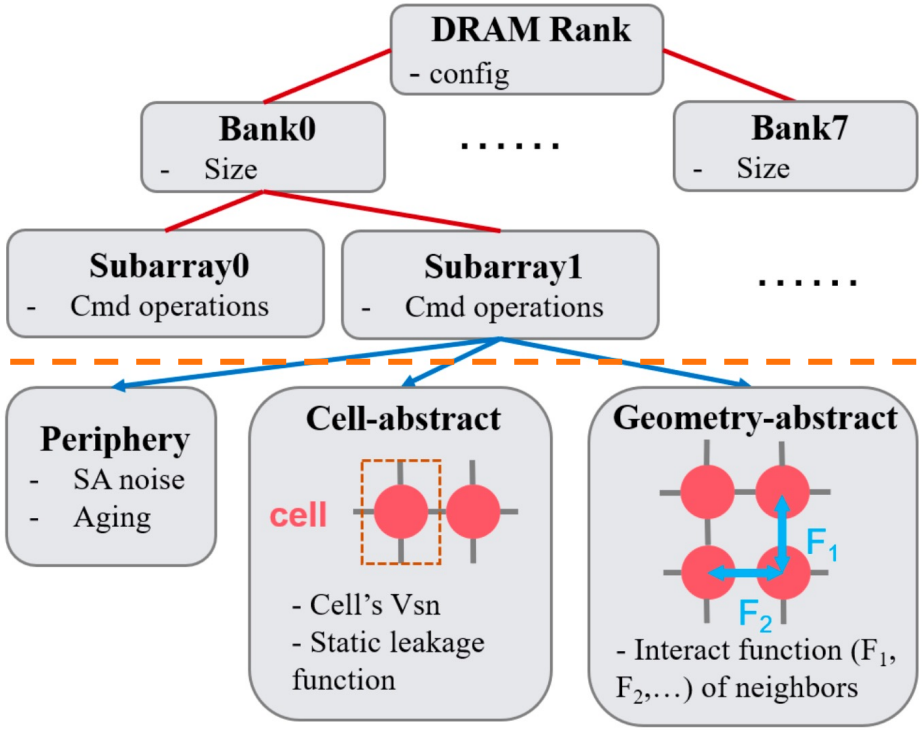


Overview of the DATIS Framework

- DATIS bridges DRAM device and architecture
- Based on Ramulator, with analog device modeling
- Supports multiple DRAM standards

DATIS - Hierarchical structure

- Standard hierarchy (Rank/Bank/Subarray) -- similar to prior work
- Cell/geometry abstraction -- DATIS Highlights



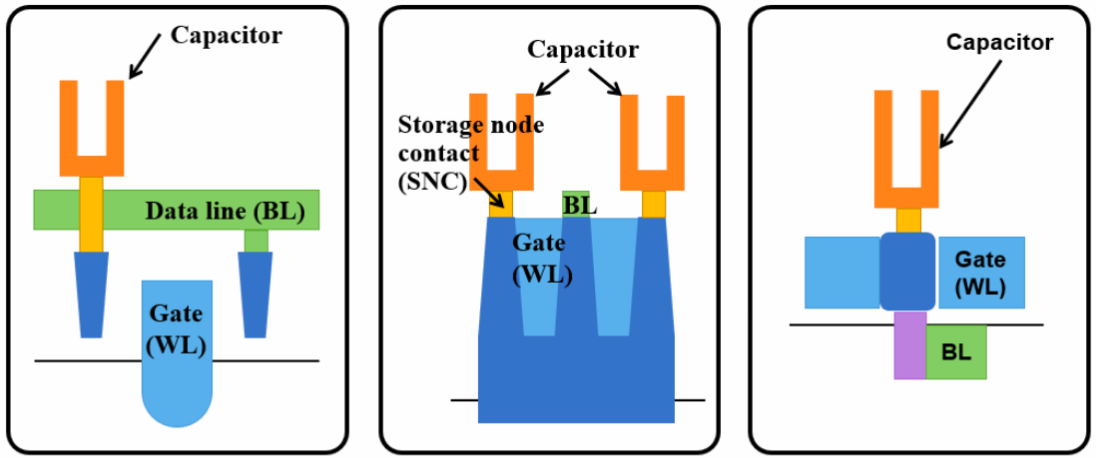
Similar to prior work

DATIS highlight

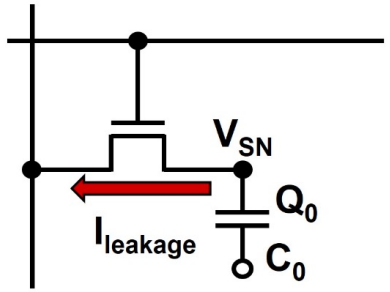
Hierarchical structure of DATIS

DATIS Internals: cell-abstract

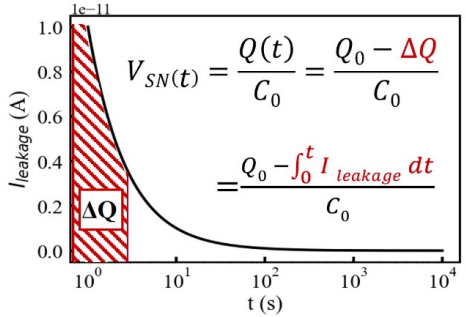
- Supports diverse DRAM cell structures across technologies
- Abstracts them into a unified leakage-aware circuit model



(a) RCAT (b) Saddle Fin (c) Vertical Channel



(a) Leakage Current Diagram



(b) The Leakage Curve Over Time

Mechanism	Types	Formulas
Generation-Recombination	GIDL	$I_{GIDL} = A_{GIDL} \exp\left(-\frac{E_a}{kT}\right)$
	GIJL	$I_{GIJL} = A_{GIJL} \exp\left(-\frac{E_a}{kT}\right)$
Drift-Diffusion	Sub-threshold	$I_{D-D} = A_{D-D} \exp\left(-\frac{E_a}{kT}\right)$
	P-N junction drift/diffusion	
Tunneling through oxide	Gate leakage	$I_{GATE\_LEAKAGE} = \sum_{i=1}^{n} \Delta I_{IT}(i)$
$I_{leakage} = I_{GIDL} + I_{GIJL} + I_{DD} + I_{GATE\_LEAKAGE}$		

(c) Table of Leakage Mechanisms and Corresponding Formulas

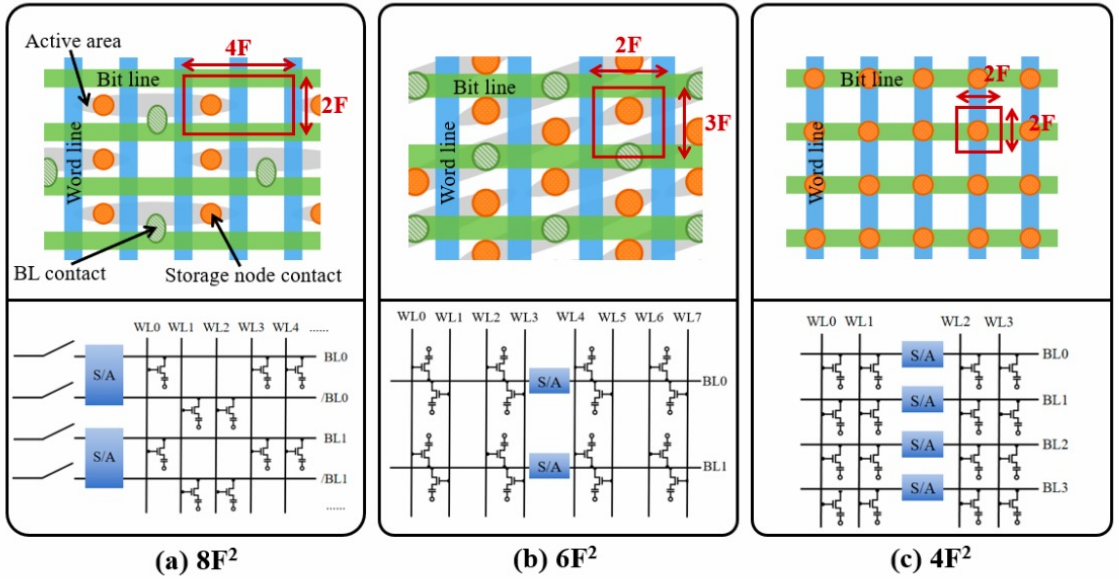
Different DRAM cell structure

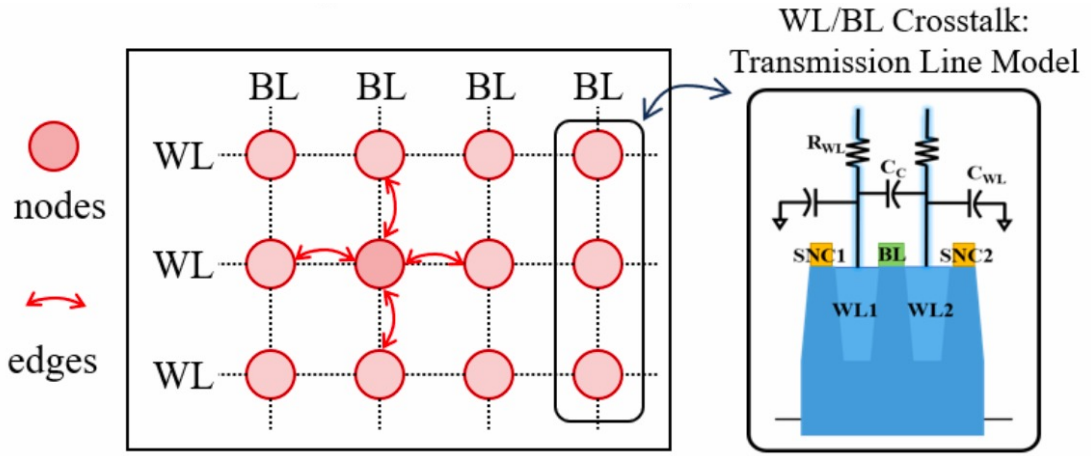
Device Leakage Model in DATIS

Different DRAM cell designs can be unified under DATIS's cell-abstraction

DATIS Internals: geometry-abstract

- Supports different DRAM process and layout structures
- Abstracts each cell as a node and interactions as edges
- Graph-based modeling enables efficient crosstalk simulation





graph-based intermediate representation (GIR)

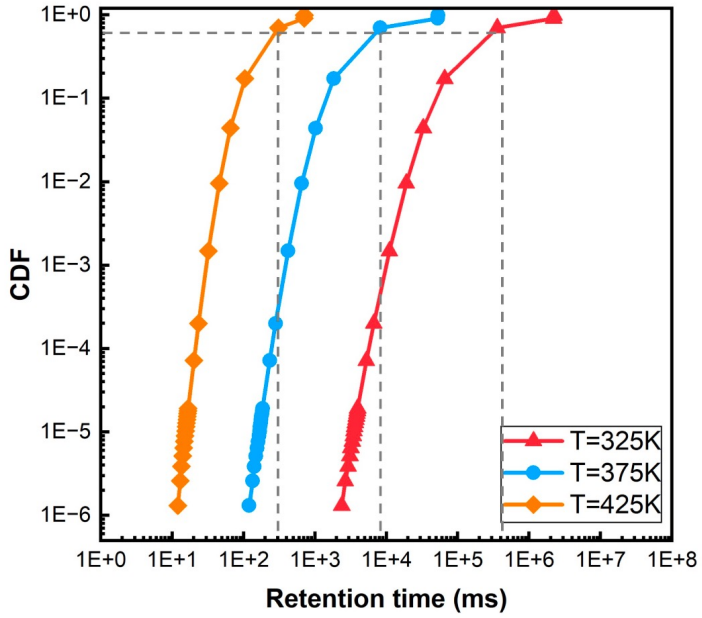
Different DRAM process and geometry structures

Graph IR to model interaction crosstalks.

Crosstalk effects are efficiently modeled under DATIS's geometry-abstract

Case Study I – Retention & Leakage

- DATIS reproduces temperature-dependent retention behavior as observed in prior work

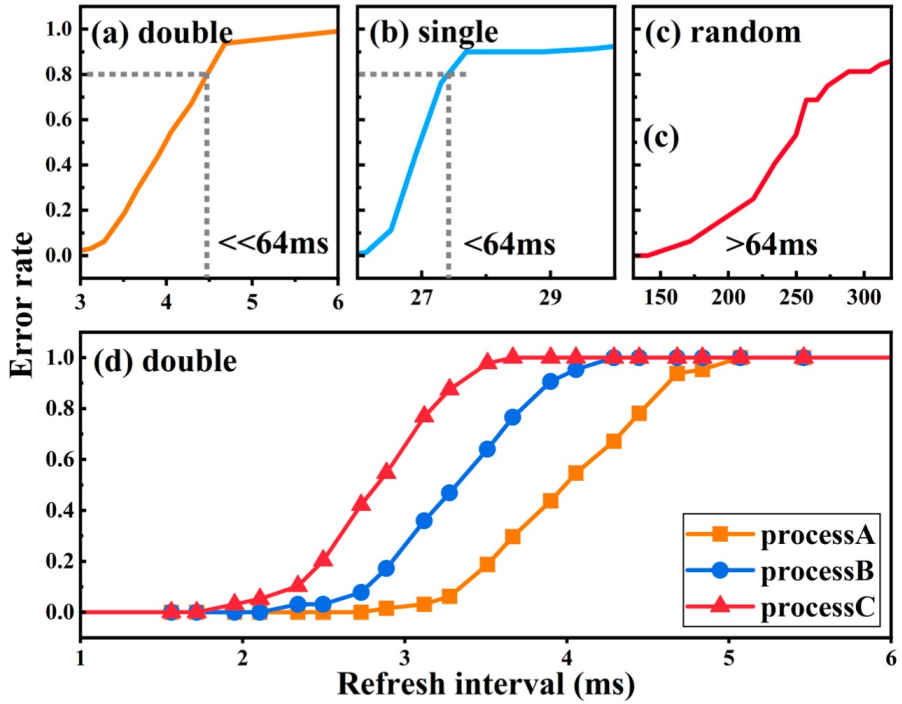


Cumulative distribution function (CDF) of retention time at 325K / 375K / 425K

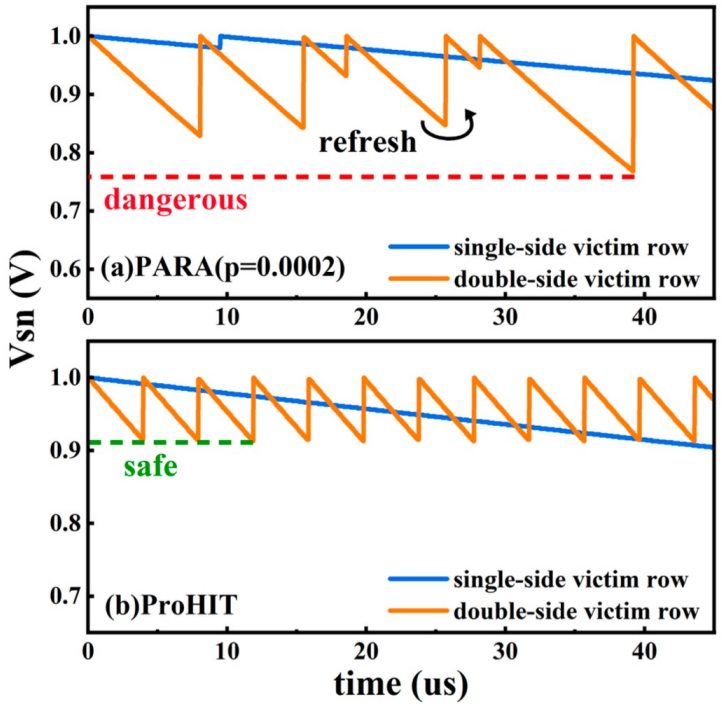
DATIS accurately captures retention times as reported in prior studies

Case Study II – RowHammer

- DATIS reproduces RowHammer error rates and evaluates mitigation algorithms (e.g., PARA, ProHIT)



Error rate with respect to varied access pattern (a-c) and processes(d)



Simulation of two refreshing algorithms for RowHammer

DATIS accurately captures RowHammer effect as reported in prior studies

Case Study III – CIM in DRAM

- DATIS simulates analog CIM behavior and error rates across operation cases

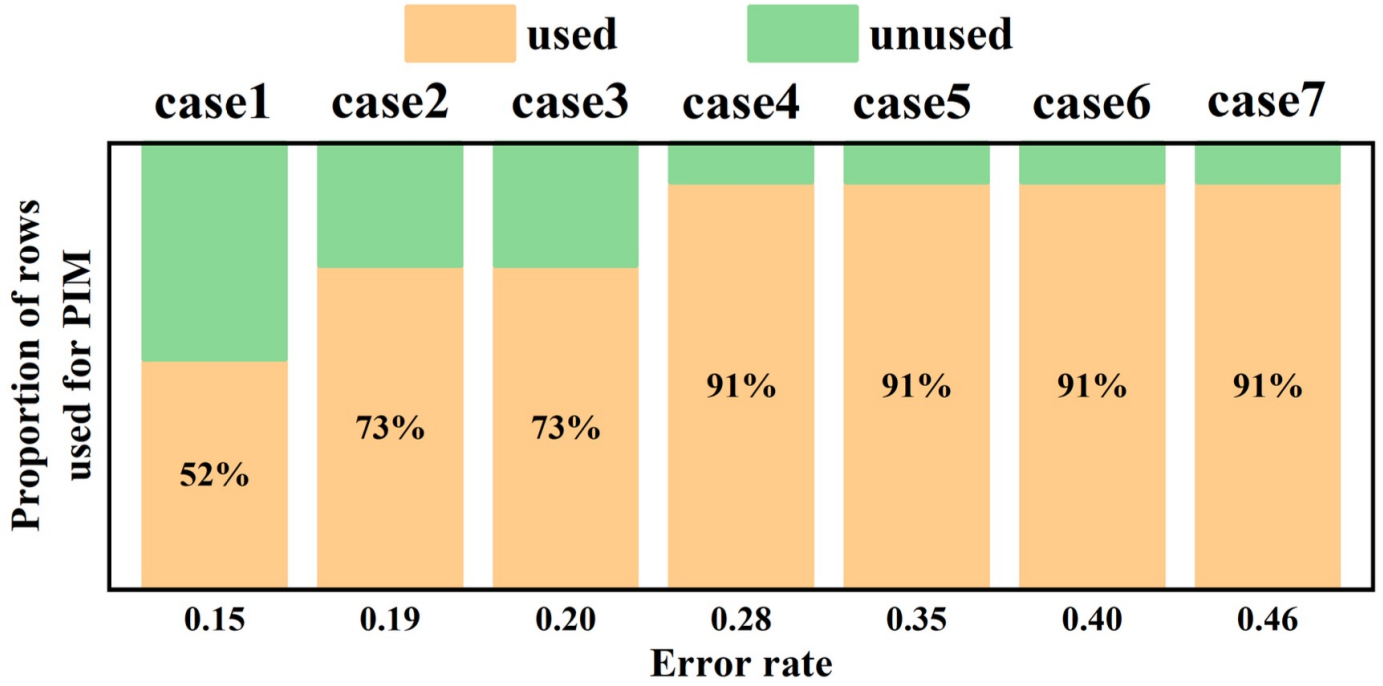


Figure 11. Error rate under different cases

Case	Computation Complexity
Case 1	Convolution x1
Case 2	Convolution x1 & Multiplication x1
Case 3	Convolution x2
Case 4	Convolution x1 & Multiplication x2
Case 5	Convolution x2 & Multiplication x1
Case 6	Convolution x2 & Multiplication x2
Case 7	Convolution x2 & Multiplication x3

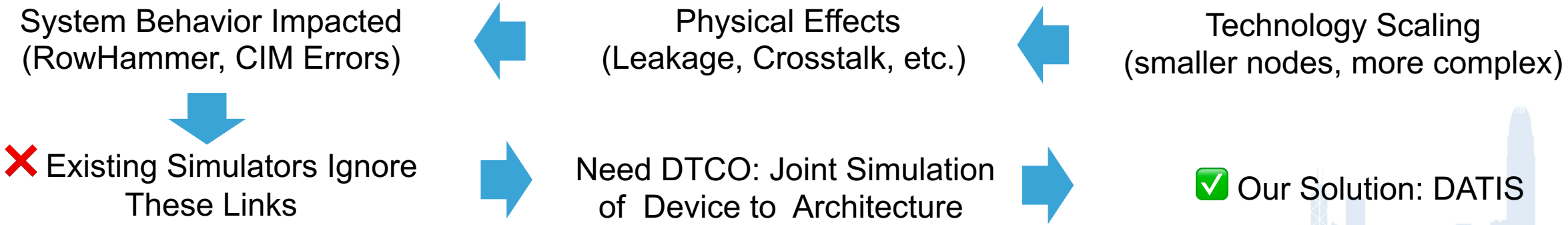
DATIS accurately captures CIM error trends as reported in prior studies

Conclusion

- Extend DATIS to support stochastic computing in DRAM
- Evaluate precision, energy, and variation effects in SC logic
- Enable fast DTCO evaluation of SC-friendly DRAM designs

Future Work

- Extend DATIS to support stochastic computing in DRAM
- Evaluate precision, energy, and variation effects in SC logic
- Enable fast DTCO evaluation of SC-friendly DRAM designs



Q & A

Thank you for your time and attention.
Questions are welcome.