1. Description

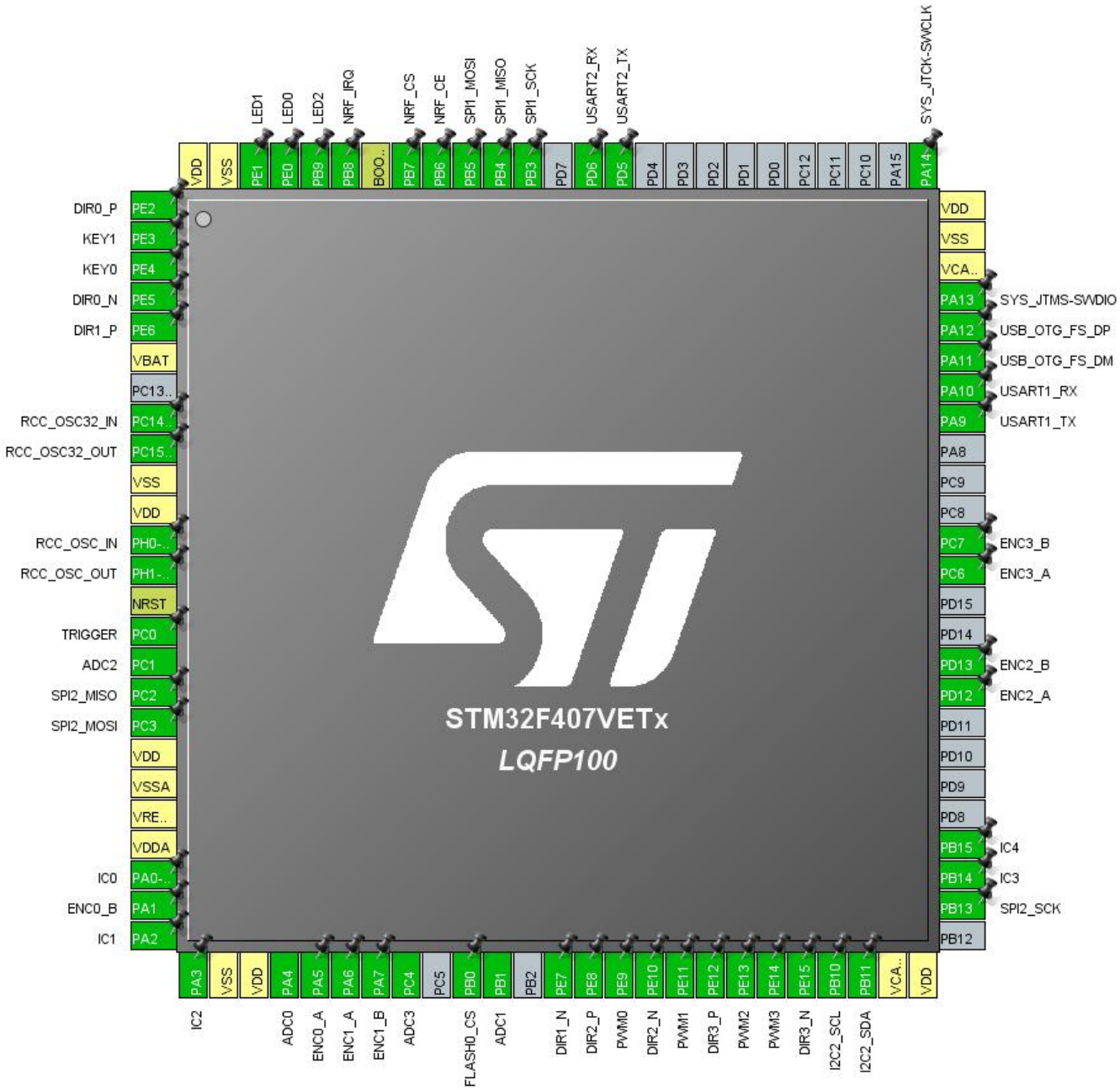
1.1. Project

Project Name	zerobot
Board Name	zerobot
Generated with:	STM32CubeMX 5.0.1
Date	03/10/2019

1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F407/417
MCU name	STM32F407VETx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



3. Pins Configuration

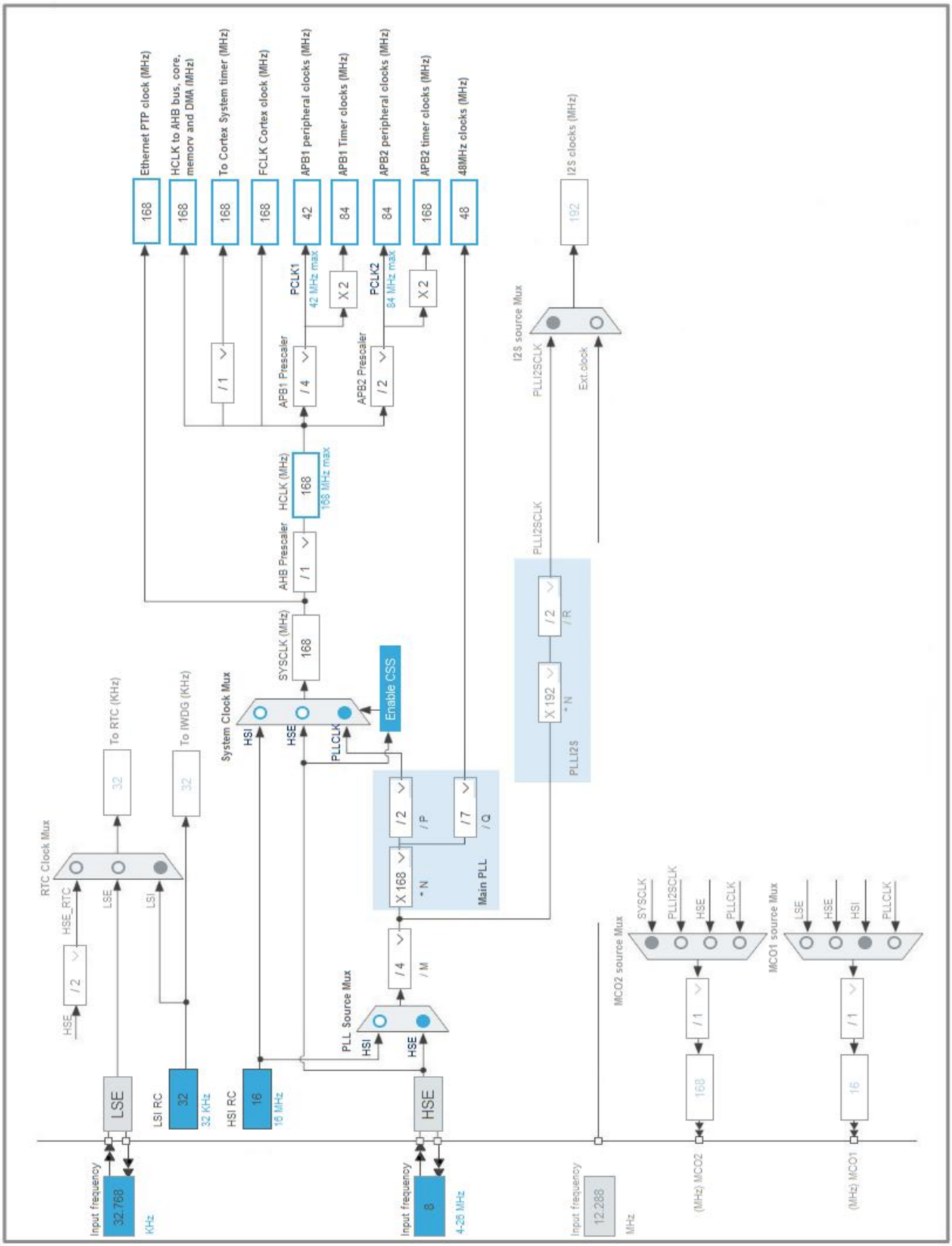
Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	DIR0_P
2	PE3	I/O	GPIO_EXTI3	KEY1
3	PE4	I/O	GPIO_EXTI4	KEY0
4	PE5 *	I/O	GPIO_Output	DIR0_N
5	PE6 *	I/O	GPIO_Output	DIR1_P
6	VBAT	Power		
8	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
9	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
10	VSS	Power		
11	VDD	Power		
12	PH0-OSC_IN	I/O	RCC_OSC_IN	
13	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0 *	I/O	GPIO_Output	TRIGGER
16	PC1	I/O	ADC1_IN11	ADC2
17	PC2	I/O	SPI2_MISO	
18	PC3	I/O	SPI2_MOSI	
19	VDD	Power		
20	VSSA	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	IC0
24	PA1	I/O	TIM2_CH2	ENC0_B
25	PA2	I/O	TIM5_CH3	IC1
26	PA3	I/O	TIM5_CH4	IC2
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	ADC0
30	PA5	I/O	TIM2_CH1	ENC0_A
31	PA6	I/O	TIM3_CH1	ENC1_A
32	PA7	I/O	TIM3_CH2	ENC1_B
33	PC4	I/O	ADC1_IN14	ADC3
35	PB0 *	I/O	GPIO_Output	FLASH0_CS
36	PB1	I/O	ADC1_IN9	ADC1
38	PE7 *	I/O	GPIO_Output	DIR1_N
39	PE8 *	I/O	GPIO_Output	DIR2_P

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
40	PE9	I/O	TIM1_CH1	PWM0
41	PE10 *	I/O	GPIO_Output	DIR2_N
42	PE11	I/O	TIM1_CH2	PWM1
43	PE12 *	I/O	GPIO_Output	DIR3_P
44	PE13	I/O	TIM1_CH3	PWM2
45	PE14	I/O	TIM1_CH4	PWM3
46	PE15 *	I/O	GPIO_Output	DIR3_N
47	PB10	I/O	I2C2_SCL	
48	PB11	I/O	I2C2_SDA	
49	VCAP_1	Power		
50	VDD	Power		
52	PB13	I/O	SPI2_SCK	
53	PB14	I/O	TIM12_CH1	IC3
54	PB15	I/O	TIM12_CH2	IC4
59	PD12	I/O	TIM4_CH1	ENC2_A
60	PD13	I/O	TIM4_CH2	ENC2_B
63	PC6	I/O	TIM8_CH1	ENC3_A
64	PC7	I/O	TIM8_CH2	ENC3_B
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
70	PA11	I/O	USB_OTG_FS_DM	
71	PA12	I/O	USB_OTG_FS_DP	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	VCAP_2	Power		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
89	PB3	I/O	SPI1_SCK	
90	PB4	I/O	SPI1_MISO	
91	PB5	I/O	SPI1_MOSI	
92	PB6 *	I/O	GPIO_Output	NRF_CE
93	PB7 *	I/O	GPIO_Output	NRF_CS
94	BOOT0	Boot		
95	PB8	I/O	GPIO_EXTI8	NRF_IRQ
96	PB9 *	I/O	GPIO_Output	LED2
97	PE0 *	I/O	GPIO_Output	LED0
98	PE1 *	I/O	GPIO_Output	LED1

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	zerobot
Project Folder	C:\Users\chenz\OneDrive\zerobot
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F4 V1.23.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F407/417
MCU	STM32F407VETx
Datasheet	022152_Rev8

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN4

mode: IN9

mode: IN11

mode: IN14

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	**PCLK2 divided by 8 ***
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Enabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	**Enabled ***
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	**4 ***
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel 4
Sampling Time	**480 Cycles ***
Rank	**2 ***
Channel	**Channel 9 ***
Sampling Time	**480 Cycles ***
Rank	**3 ***
Channel	**Channel 11 ***
Sampling Time	**480 Cycles ***
Rank	**4 ***
Channel	**Channel 14 ***
Sampling Time	**480 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. I2C2

I2C: I2C

7.2.1. Parameter Settings:

Master Features:

I2C Speed Mode	Standard Mode
I2C Clock Speed (Hz)	100000

Slave Features:

Clock No Stretch Mode	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0
General Call address detection	Disabled

7.3. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.3.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulatror Voltage Scale	Power Regulator Voltage Scale 1

7.4. SPI1

Mode: Full-Duplex Master

7.4.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**10.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.5. SPI2

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**4 ***
Baud Rate	**10.5 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SYS

Debug: Serial Wire

Timebase Source: TIM7

7.7. TIM1

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**16800 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Break And Dead Time management - BRK Configuration:

BRK State	Disable
BRK Polarity	High

Break And Dead Time management - Output Configuration:

Automatic Output State	Disable
Off State Selection for Run Mode (OSSR)	Disable
Off State Selection for Idle Mode (OSSI)	Disable
Lock Configuration	Off

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

CH Idle State	Reset

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High
CH Idle State	Reset

7.8. TIM2

Combined Channels: Encoder Mode

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.9. TIM3

Combined Channels: Encoder Mode

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.10. TIM4

Combined Channels: Encoder Mode

7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.11. TIM5

Channel1: Input Capture direct mode

Channel3: Input Capture direct mode

Channel4: Input Capture direct mode

7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**83 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**4294967295 ***
Internal Clock Division (CKD)	No Division

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 3:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 4:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.12. TIM8

Combined Channels: Encoder Mode

7.12.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

Encoder:

Encoder Mode	**Encoder Mode TI1 and TI2 ***
____ Parameters for Channel 1 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0
____ Parameters for Channel 2 ____	
Polarity	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter	0

7.13. TIM12

Channel1: Input Capture direct mode

Channel2: Input Capture direct mode

7.13.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**83 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**65535 ***
Internal Clock Division (CKD)	No Division

Input Capture Channel 1:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

Input Capture Channel 2:

Polarity Selection	Rising Edge
IC Selection	Direct
Prescaler Division Ratio	No division
Input Filter (4 bits value)	0

7.14. USART1

Mode: Asynchronous

7.14.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.15. USART2

Mode: Asynchronous

7.15.1. Parameter Settings:

Basic Parameters:

Baud Rate	**921600 ***

Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.16. USB_OTG_FS

Mode: Device_Only

7.16.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Endpoint 0 Max Packet size	64 Bytes
Enable internal IP DMA	Disabled
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.17. FREERTOS

mode: Enabled

7.17.1. Config parameters:

Versions:

FreeRTOS version	9.0.0
CMSIS-RTOS version	1.02

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	128
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	**Disabled ***
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled

USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	**Disabled ***
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	**Disabled ***

Memory management settings:

Memory Allocation	Dynamic
TOTAL_HEAP_SIZE	15360
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled
USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

7.17.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	**Enabled ***
vTaskSuspend	Enabled
vTaskDelayUntil	**Enabled ***
vTaskDelay	Enabled

xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	**Enabled ***
eTaskGetState	**Enabled ***
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	**Enabled ***

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC1	ADC1_IN11	Analog mode	No pull-up and no pull-down	n/a	ADC2
	PA4	ADC1_IN4	Analog mode	No pull-up and no pull-down	n/a	ADC0
	PC4	ADC1_IN14	Analog mode	No pull-up and no pull-down	n/a	ADC3
	PB1	ADC1_IN9	Analog mode	No pull-up and no pull-down	n/a	ADC1
I2C2	PB10	I2C2_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB11	I2C2_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI1	PB3	SPI1_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB4	SPI1_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB5	SPI1_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI2	PC2	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PC3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM1	PE9	TIM1_CH1	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	PWM0

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PE11	TIM1_CH2	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	PWM1
	PE13	TIM1_CH3	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	PWM2
	PE14	TIM1_CH4	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	PWM3
TIM2	PA1	TIM2_CH2	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC0_B
	PA5	TIM2_CH1	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC0_A
TIM3	PA6	TIM3_CH1	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC1_A
	PA7	TIM3_CH2	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC1_B
TIM4	PD12	TIM4_CH1	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC2_A
	PD13	TIM4_CH2	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC2_B
TIM5	PA0-WKUP	TIM5_CH1	**Alternate Function Open Drain ***	**Pull-down ***	Low	IC0
	PA2	TIM5_CH3	**Alternate Function Open Drain ***	**Pull-down ***	Low	IC1
	PA3	TIM5_CH4	**Alternate Function Open Drain ***	**Pull-down ***	Low	IC2
TIM8	PC6	TIM8_CH1	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC3_A
	PC7	TIM8_CH2	**Alternate Function Open Drain ***	No pull-up and no pull-down	Low	ENC3_B
TIM12	PB14	TIM12_CH1	**Alternate Function Open Drain ***	**Pull-down ***	Low	IC3
	PB15	TIM12_CH2	**Alternate Function Open Drain ***	**Pull-down ***	Low	IC4
USART1	PA9	USART1_TX	Alternate Function Push Pull	Pull-up	**Very High ***	
	PA10	USART1_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USART2	PD5	USART2_TX	Alternate Function Push Pull	Pull-up	**Very High**	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					*	
	PD6	USART2_RX	Alternate Function Push Pull	Pull-up	**Very High ***	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE2	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR0_P
	PE3	GPIO_EXTI3	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	KEY1
	PE4	GPIO_EXTI4	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	KEY0
	PE5	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR0_N
	PE6	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR1_P
	PC0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TRIGGER
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	FLASH0_CS
	PE7	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR1_N
	PE8	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR2_P
	PE10	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR2_N
	PE12	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR3_P
	PE15	GPIO_Output	**Output Open Drain ***	No pull-up and no pull-down	Low	DIR3_N
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	NRF_CE
	PB7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**Very High ***	NRF_CS
	PB8	GPIO_EXTI8	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	**n/a**	NRF_IRQ
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED2
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED0
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LED1

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI1_RX	DMA2_Stream0	Peripheral To Memory	Low
SPI1_TX	DMA2_Stream3	Memory To Peripheral	Low
USART2_RX	DMA1_Stream5	Peripheral To Memory	Low
USART2_TX	DMA1_Stream6	Memory To Peripheral	Low
SPI2_RX	DMA1_Stream3	Peripheral To Memory	Low
SPI2_TX	DMA1_Stream4	Memory To Peripheral	Low
USART1_RX	DMA2_Stream2	Peripheral To Memory	Low
USART1_TX	DMA2_Stream7	Memory To Peripheral	Low
ADC1	DMA2_Stream4	Peripheral To Memory	Low

SPI1_RX: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI1_TX: DMA2_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_RX: DMA1_Stream5 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART2_TX: DMA1_Stream6 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_RX: DMA1_Stream3 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

SPI2_TX: DMA1_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_RX: DMA2_Stream2 DMA request Settings:

Mode:	**Circular ***
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

USART1_TX: DMA2_Stream7 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Byte
Memory Data Width:	Byte

ADC1: DMA2_Stream4 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
EXTI line3 interrupt	true	5	0
EXTI line4 interrupt	true	5	0
DMA1 stream3 global interrupt	true	5	0
DMA1 stream4 global interrupt	true	5	0
DMA1 stream5 global interrupt	true	5	0
DMA1 stream6 global interrupt	true	5	0
EXTI line[9:5] interrupts	true	5	0
I2C2 event interrupt	true	5	0
I2C2 error interrupt	true	5	0
SPI1 global interrupt	true	5	0
SPI2 global interrupt	true	5	0
USART1 global interrupt	true	5	0
USART2 global interrupt	true	5	0
TIM8 break interrupt and TIM12 global interrupt	true	5	0
TIM5 global interrupt	true	5	0
TIM7 global interrupt	true	0	0
DMA2 stream0 global interrupt	true	5	0
DMA2 stream2 global interrupt	true	5	0
DMA2 stream3 global interrupt	true	5	0
DMA2 stream4 global interrupt	true	5	0
DMA2 stream7 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 global interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
TIM1 capture compare interrupt	unused		
TIM2 global interrupt	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
TIM8 update interrupt and TIM13 global interrupt	unused		
TIM8 trigger and commutation interrupts and TIM14 global interrupt	unused		
TIM8 capture compare interrupt	unused		
USB On The Go FS global interrupt	unused		
FPU global interrupt	unused		

*** User modified value**

9. Software Pack Report