Hyunwoo Oh

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Education

M.S. in Electronic Engineering (GPA: 4.33/4.5) **2023**
Seoul National University of Science and Technology (SEOULTECH) Seoul, Korea
• Thesis Title: Research on Optimized Processor and Floating-point Unit Architecture for Embedded Systems
Advisor: Seung Eun Lee

B.S. in Electronic Engineering (GPA: 3.38/4.5) (Last 60 GPA: 3.94/4.5) **2021**
Seoul National University of Science and Technology (SEOULTECH) Seoul, Korea

Research Interests

Hardware/Software Co-Design: Developing co-optimization techniques to enhance energy efficiency and performance in the context of digital VLSI.

- Parameterized Hardware: Designing configurable, scalable architectures and generators that can be tailored for target specifications.
- Software Stack: Optimizing software architectures to practically adapt to various hardware configurations.

Computer Architecture: Finding the efficient processor architectures and compiler architectures to fulfill the domain-specific computing requirements.

- Heterogeneous SoC: Designing the optimized processor architecture to integratek the emerging parallel architectures (PIM, NPU, etc.) and conventional general-purpose processors.
- Compilers: Developing domain-specific compilers optimized for targeted hardware designs.

Selected Publications [See all ⇓]

Conference Papers (2 of 8)

C8. **An SoC FPGA-based Integrated Real-time Image Processor for Uncooled Infrared Focal Plane Array**.
Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Joon Hwan Han, Jung-Ho Shin.
*Euromicro Conference on Digital System Design (**DSD**)*, Durres, Albania, Sep. **2023**. [Accepted] [Long Presentation]

C6. **RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit**.
Hyun Woo Oh, Seongmo An, Won Sik Jeong, Seung Eun Lee.
*ACM/IEEE International Symposium on Low Power Electronics and Design (**ISLPED**)*, Vienna, Austria, Aug. **2023**. [Accepted] [Oral Presentation]

Journal Articles (3 of 6)

J6. **The Design of Optimized RISC Processor for Edge Artificial Intelligence Based on Custom Instruction Set Extension**.
Hyun Woo Oh, Seung Eun Lee.
IEEE Access, Vol. 11, pp. 49409-49421, May **2023**.

J3. **ASimOV: A Framework for Simulation and Optimization of an Embedded AI Accelerator**.
Dong Hyun Hwang, Chang Yeop Han, **Hyun Woo Oh**, Seung Eun Lee.
Micromachines, Vol. 12, No. 7, Jul. **2021**.

J2. **The Design of a 2D Graphics Accelerator for Embedded Systems**.
Hyun Woo Oh, Ji Kwang Kim, Gwan Beom Hwang, Seung Eun Lee.
Electronics, Vol. 10, No. 4, Feb. **2021**.

Awards and Honors

Academic Scholarship, SEOULTECH **2021**

Future Talent Scholarship to pursue a M.S., SEOULTECH **2021 - 2022**

President of the Institute of Semiconductor Engineers Award, 21st Korea Semiconductor Design Contest **2020**

Work Experience

FPGA & Firmware Engineer, Core H/W Team, Hanwha Systems, Korea **Jan. 2023 - present**

- Designed SoC FPGA-based integrated thermal image processor for infrared focal plane arrays. [DSD 2023 (C8)]
  - Designed several AXI4-compliant accelerators for thermal image processing on Zynq Ultrascale+ MPSoC.
  - Developed RTOS firmware based on FreeRTOS with AMP to control the image processor.
  - Designed the PCB schematic for the digital signal processing module, including Zynq Ultrascale+ MPSoC.
- Developed RTOS for Heterogeneous MPSoC (TI TDA3x SoC for ADAS) using the Vision SDK platform.
  - Activated the Control Area Network (CAN) driver to establish communication with automotive processors.
  - Developed the driver for external heater manipulation using the GPIO and timer peripheral.

Research Experience

Research Assistant, SoC Platform Lab., SEOULTECH, Korea **Dec. 2019 - Dec. 2022**

Processing Software on AI Semiconductor Devices **Jul. 2022 - Dec. 2022**

Ministry of Science and ICT, Korea

- Designed the RISC processor with a custom instruction set extension for flexible AI acceleration for edge devices. This work includes scalable k-NN coprocessor architecture with parameterized HDL generator software and hardware driver library using assembly and C. [IEEE Access 2023 (J6)]
- Conducted research on optimized hardware and software architecture for applying posit number format to previous applications based on IEEE-754. This work includes scalable arithmetic unit architecture to provide versatility in terms of specifications, compiler (GCC) optimization to minimize the additional workloads for migration, and a practical evaluation platform for swift analysis of numeric performance. [ISLPED 2023 (C6)] [ISOCC 2022 (C5)]

Next-Generation System Semiconductor Design Engineer Development Program **Mar. 2021 - Dec. 2022**

Ministry of Trade, Industry and Energy, Korea

- Designed local interconnect network (LIN) peripheral IP for ARM Cortex-M0. My work was building a synthesis and verification environment, including automation scripts for Synopsys EDA tools, a randomized testbench pattern generator, and the LIN peripheral software driver. [ICCE 2022 (C4)]

Multi-core Hardware Accelerator for High-Performance Computing (HPC) **Dec. 2019 - Mar. 2022**

Ministry of Science and ICT, Korea

- Conducted research on processor architecture to provide a platform for building an accelerator-rich environment. This work includes designing a 32-bit pipelined MIPS core, cache controller, and system bus from scratch and building a GCC-based development environment for the designed processor. [ISOCC 2020 (C1)]

Embedded Artificial Intelligence Module and System Based on Neuromorphic **Dec. 2019 - Dec. 2021**

Ministry of Trade, Industry and Energy, Korea

- Developed the parameterized HDL generator software for reconfigurable embedded AI module based on the k-NN algorithm. [Micromachines 2021 (J3)]
- Conducted research on applications using the embedded AI module. [JICCE 2022 (J5)] [Micromachines 2021 (J4)] [ICFICE 2022 (C3)] [ICCE 2021 (C2)]

Light-weight SW-SoC Solution for Respiratory Medical Device **Dec. 2019 - Dec. 2020**

Ministry of Trade, Industry and Energy, Korea

- Designed a 2D graphics accelerator architecture based on Bresenham's line algorithm. This accelerator was mounted to the processor with ARM Cortex-M0 core and AHB bus, and specially optimized for graph visualization tasks in medical devices. [Electronics 2021 (J2)]
- Developed a software stack for hardware implementation of Lempel-Ziv 77 lossless decompression accelerator, which is used for PNG images. This work includes baseline C code for prototyping hardware, pre-processing software to extract ZLIB blocks and metadata, and visualization/analysis code written in MATLAB. [Micromachines 2021 (J1)]

Participated in designing several digital VLSI chips using Synopsys EDA tools. [See list ⇓]

Teaching Experience

Teaching Assistant for "Digital System Design", SEOULTECH **Spring 2021**

- Grading, preparation of lab lecture materials

Teaching Assistant for "Computer Architecture", SEOULTECH **Fall 2021**

- Grading

Training

ISO 26262:2018 Functional Safety Engineering Course: Automotive Foundation Level (FSE-AFL), DNV	**2023.01.02-01.04**
Design of High-speed Memory Interface, IDEC	**2022.12.09**
[Synopsys] Block-level Auto P&R utilizing IC Compiler II, IDEC	**2021.11.01-11.05**
Cell-based Chip Design Flow for Samsung 28nm Process, IDEC	**2021.10.19-10.21**
Cell-based Chip Design Flow, IDEC	**2021.07.05-07.09**
[Infineon] Automotive Semiconductor Expert Training - Basic Course, KSIA	**2021.06.30-07.02**
Cell-based Chip Design Flow, IDEC	**2020.08.10-08.14**

Technical Skills

Computer Programming	General Programming	C, C++, Python, Perl, Bash
	Mathematical	MATLAB (+ GNU Octave)
	Version Control	Git, SVN
	Operating System Development	FreeRTOS, TI Vision SDK, PetaLinux
	Machine Learning Toolkit	Tensorflow*, PyTorch*
	Document Tools	LaTex, Obsidian (Markdown)
Digital Hardware Design	Hardware Description	Verilog, SystemVerilog, Chisel
	Simulation	Verilator, ModelSim
FPGA-based Design	Xilinx FPGA Tools	Vivado, Vitis
	Intel FPGA Tools	Quartus II/Prime, Nios II EDS
Digital VLSI Design	Synopsys EDA Tools	VCS (Simulation), Verdi (Analysis), Formality (Validation)
		Design Compiler (Synthesis), IC Compiler I/II (Layout)
		StarRCXT (Parasitic Extraction), PrimeTime (STA)
	Cadence EDA Tools	Virtuoso Layout Suite* (Layout)
		Calibre DRC*/LVS* (Physical/Layout Verification)
PCB Design	Cadence CAD Tools	OrCAD Capture* (Schematic), Allegro PCB Designer* (Artwork)
Miscellaneous	GUI Programming Framework	Winform/WPF* (C#), JavaFX* (Java), Qt* (C++), Kivy* (Python)
	Mobile Programming	Android* (Java)
	Analytical Language	R* (Mostly used for data visualization)
	Familiar OS for development	Ubuntu, Windows 10 (with WSL), CentOS

* stands for beginner level.

All Publications [Go up ⇑]

Conference Papers

C8. **An SoC FPGA-based Integrated Real-time Image Processor for Uncooled Infrared Focal Plane Array**.
Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Joon Hwan Han, Jung-Ho Shin.
*Euromicro Conference on Digital System Design (**DSD**)*, Durres, Albania, Sep. **2023**. [Accepted] [Long Presentation]

C7. **Disparity Refinement Processor Architecture utilizing Horizontal and Vertical Characteristics for Stereo Vision Systems**.
Cheol-Ho Choi, **Hyun Woo Oh**.
*Euromicro Conference on Digital System Design (**DSD**)*, Durres, Albania, Sep. **2023**. [Accepted] [Long Presentation]

C6. **RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit**.
Hyun Woo Oh, Seongmo An, Won Sik Jeong, Seung Eun Lee.
*ACM/IEEE International Symposium on Low Power Electronics and Design (**ISLPED**)*, Vienna, Austria, Aug. **2023**. [Accepted] [Oral Presentation]

C5. **Evaluation of Posit Arithmetic on Machine Learning based on Approximate Exponential Functions**.
Hyun Woo Oh, Won Sik Jeong, Seung Eun Lee.
*International SoC Design Conference (**ISOCC**)*, Gangneung, Korea, Oct. **2022**.

C4. **A Local Interconnect Network Controller for Resource-Constrained Automotive Devices**.
Kwonneung Cho, **Hyun Woo Oh**, Jeongeun Kim, Young Woo Jeong, Seung Eun Lee.
*IEEE International Conference on Consumer Electronics (**ICCE**)*, Las Vegas, NV, USA, Jan. **2022**.

C3. **Intelligent Transportation System based on an Edge AI**.
Young Woo Jeong, **Hyun Woo Oh**, Su Yeon Jang, Seung Eun Lee.
*International Conference on Future Information & Communication Engineering (**ICFICE**)*, Jeju, Korea, Jan. **2022**.

C2. **Vision-based Parking Occupation Detecting with Embedded AI Processor**.
Kwonneung Cho, **Hyun Woo Oh**, Seung Eun Lee.
*IEEE International Conference on Consumer Electronics (**ICCE**)*, Las Vegas, NV, USA, Jan. **2021**.

C1. **Design of 32-bit Processor for Embedded Systems**.
Hyun Woo Oh, Kwon Neung Cho, Seung Eun Lee.
*International SoC Design Conference (**ISOCC**)*, Yeosu, Korea, Oct. **2021**.

Journal Articles

J6. **The Design of Optimized RISC Processor for Edge Artificial Intelligence Based on Custom Instruction Set Extension**.
Hyun Woo Oh, Seung Eun Lee.
IEEE Access, Vol. 11, pp. 49409-49421, May **2023**.

J5. **An Edge AI Device based Intelligent Transportation System**.
Youngwoo Jeong, **Hyun Woo Oh**, Soohee Kim, Seung Eun Lee.
Journal of Information and Communication Convergence Engineering, Vol. 20, No. 3, pp. 166-173, Sep. **2022**.

J4. **A Multi-Core Controller for an Embedded AI System Supporting Parallel Recognition**.
Suyeon Jang, **Hyun Woo Oh**, Young Hyun Yoon, Dong Hyun Hwang, Won Sik Jeong, Seung Eun Lee.
Micromachines, Vol. 12, No. 8, Jul. **2021**.

J3. **ASimOV: A Framework for Simulation and Optimization of an Embedded AI Accelerator**.
Dong Hyun Hwang, Chang Yeop Han, **Hyun Woo Oh**, Seung Eun Lee.
Micromachines, Vol. 12, No. 7, Jul. **2021**.

J2. **The Design of a 2D Graphics Accelerator for Embedded Systems**.
Hyun Woo Oh, Ji Kwang Kim, Gwan Beom Hwang, Seung Eun Lee.
Electronics, Vol. 10, No. 4, Feb. **2021**.

J1. **Lossless Decompression Accelerator for Embedded Processor with GUI**.
Gwan Beom Hwang, Kwon Neung Cho, Chang Yeop Han, **Hyun Woo Oh**, Young Hyun Yoon, Seung Eun Lee.
Micromachines, Vol. 12, No. 2, Jan. **2021**.

Chip Designs [Go up ⇑]

A RISC-V Processor Supporting AMBA AXI Protocol for Embedded Systems **Jul. 2022**

- Designer: Won Sik Jeong, Sun Beom Kwon, **Hyun Woo Oh**, Jeongeun Kim
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Verification

Robot-Specific Processor for Autonomous Driving **Jul. 2022**

- Designer: Youngwoo Jeong, Yue Ri Jeong, **Hyun Woo Oh**, Kwang Hyun Go
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: System Verification Assistant

In-Vehicle Network Processor based on Cortex-M0 **Mar. 2022**

- Designer: Kwon Neung Cho, Jeong Eun Kim, **Hyun Woo Oh**
- Technology: TSMC 180nm RFCMOS (1-poly 6-metal)
- Role: System Verification SW Dev., RTL Verification, Pre/Post-Layout Simulation

A Programmable Embedded AI Processor with Cortex-M0 **Jul. 2021**

- Designer: Kwon Neung Cho, Young Woo Jeong, **Hyun Woo Oh**, Chang Yeop Han
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Subblock Design

32-bit Processor with Posit Arithmetic Coprocessor for Embedded Systems **Jul. 2021**

- Designer: **Hyun Woo Oh**, Jeong Eun Kim, Do Young Choi, Kwang Hyun Go
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Design & Verification, ASIC Design Front-end/Back-end, Firmware Development, PCB Design & Chip Test

Implementation of Lossless Decompression Accelerator Based on Inflate Algorithm **Sep. 2020**

- Designer: Gwan Beom Hwang, Do Young Choi, **Hyun Woo Oh**, Chang Yeop Han
- Technology: Samsung 65nm RFCMOS (1-poly 8-metal)
- Role: System Verification SW Dev., PCB Design & Chip Test

Communication System with Simple and Fast Communication Error Check Code Based on CRC **Jun. 2020**

- Designer: Chang Yeo Hanp, Kwon Neung Cho, **Hyun Woo Oh**
- Technology: Magnachip Hynix 0.18um CMOS
- Role: RTL Subblock Design

Professional Services

Reviewer, IEEE Access **2023**

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