

# Hyunwoo Oh

+82.10.7590.2846 [ohhyunwoo@seoultech.ac.kr](mailto:ohhyunwoo@seoultech.ac.kr) [hyun-woo-oh.github.io](https://github.com/hyun-woo-oh) [Hyunwoo Oh](#)

## EDUCATION

### M.S. in Electronic Engineering

2023

Seoul National University of Science and Technology (SEOULTECH)

Seoul, Korea

- Thesis: Research on Optimized Processor and Floating-point Unit Architecture for Embedded Systems

Advisor: Seung Eun Lee

### B.S. in Electronic Engineering

2021

Seoul National University of Science and Technology (SEOULTECH)

Seoul, Korea

## RESEARCH INTERESTS

**Computer Architecture:** Exploring novel HW architecture and methodologies to meet the growing computing performance and efficiency demands.

- Heterogeneous Computing: Designing the optimized processor architectures that integrate both emerging parallel machines (PIM, NPU, etc.) and conventional general-purpose processors.
- Compilers: Developing SW compilers optimized for targeted HW designs.

**HW/SW Co-Design:** Developing techniques for co-optimization to improve energy efficiency and performance.

- Parameterized HW Design Framework: Designing configurable, scalable architectures with RTL generators, compilers, and SW stacks to tailor the HW to system constraints such as power, energy, and area.
- Partitioning Methodology: Investigating a method to derive the parameters to mitigate the impact of Amdahl's law and maximize system performance.

## SELECTED PUBLICATIONS [\[SEE ALL ↓↓\]](#)

### Peer-Reviewed Conference Papers (2 of 8)

C8. **An SoC FPGA-based Integrated Real-time Image Processor for Uncooled Infrared Focal Plane Array.**

Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Joon Hwan Han, Jung-Ho Shin.

*Euromicro Conference on Digital System Design (DSD)*, Durres, Albania, Sep. 2023. [Accepted] [Long Presentation]

C6. **RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit.**

Hyun Woo Oh, Seongmo An, Won Sik Jeong, Seung Eun Lee.

*ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Vienna, Austria, Aug. 2023. [Accepted] [Oral Presentation]

### Peer-Reviewed Journal Articles (2 of 6)

J6. **The Design of Optimized RISC Processor for Edge Artificial Intelligence Based on Custom Instruction Set Extension.**

Hyun Woo Oh, Seung Eun Lee.

*IEEE Access*, Vol. 11, pp. 49409-49421, May 2023.

J2. **The Design of a 2D Graphics Accelerator for Embedded Systems.**

Hyun Woo Oh, Ji Kwang Kim, Gwan Beom Hwang, Seung Eun Lee.

*Electronics*, Vol. 10, No. 4, Feb. 2021.

## AWARDS AND HONORS

Academic Scholarship, SEOULTECH

2021

Future Talent Scholarship to pursue a M.S., SEOULTECH

2021 - 2022

President of the Institute of Semiconductor Engineers Award, 21st Korea Semiconductor Design Contest

2020

## WORK EXPERIENCE

### FPGA & Firmware Engineer, Core H/W Team, Hanwha Systems, Korea

Jan. 2023 - present

- Designed SoC FPGA-based integrated thermal image processor for infrared focal plane arrays. [DSD 2023 (C8)]
  - Designed several AXI4-compliant accelerators for thermal image processing on Zynq Ultrascale+ MPSoC.
  - Developed RTOS firmware based on FreeRTOS with AMP to control the image processor.
  - Designed the PCB schematic for the digital signal processing module, including Zynq Ultrascale+ MPSoC.
- Developed RTOS for Heterogeneous MPSoC (TI TDA3x SoC for ADAS) using the Vision SDK platform.
  - Activated the Control Area Network (CAN) driver to establish communication with automotive processors.
  - Developed the driver for external heater manipulation using the GPIO and timer peripheral.

## RESEARCH EXPERIENCE

### Research Assistant, SoC Platform Lab., SEOULTECH, Korea

Dec. 2019 - Feb. 2023

#### Development for Processing Software on AI Semiconductor Devices

Jul. 2022 - Dec. 2022

Ministry of Science and ICT, Korea

- Designed the RISC processor with a custom instruction set extension for flexible AI acceleration running on edge devices. This work includes a scalable AI coprocessor with a parameterized hardware generator. [IEEE Access 2023 (J6)]
- Researched optimized processor and compiler architecture for posit-based FPU support. This work includes scalable arithmetic unit architecture, compiler optimization, and a practical evaluation platform. [ISLPED 2023 (C6)] [ISOC 2022 (C5)]

#### Development of DRAM PIM Semiconductor Technology For Enhanced Computing Function for Edge

Apr. 2022 - Dec. 2022

Ministry of Science and ICT, Korea

- Designed hierarchical hardware architecture for DRAM-based PIM and software simulator architecture.

#### Next-Generation System Semiconductor Design Engineer Development Program

Mar. 2021 - Dec. 2022

Ministry of Trade, Industry and Energy, Korea

- Designed local interconnect network (LIN) peripheral IP for ARM Cortex-Mo. My work was synthesis and verification using Synopsys EDA tools, and developing a randomized test pattern generator and peripheral driver. [ICCE 2022 (C4)]

#### Multi-core Hardware Accelerator for High-Performance Computing (HPC)

Dec. 2019 - Mar. 2022

Ministry of Science and ICT, Korea

- Researched processor architecture to provide a platform for building an accelerator-rich environment. This work includes designing a 32-bit pipelined MIPS core, cache controller, and system bus from scratch and building a GCC-based development environment for the designed processor. [ISOC 2020 (C1)]

#### Development of Embedded Artificial Intelligence Module and System Based on Neuromorphic

Dec. 2019 - Dec. 2021

Ministry of Trade, Industry and Energy, Korea

- Developed the parameterized hardware generator for an embedded AI module. [Micromachines 2021 (J3)]
- Researched applications of the AI module. [JICCE 2022 (J5)] [Micromachines 2021 (J4)] [ICFICE 2022 (C3)] [ICCE 2021 (C2)]

#### Development of Light-weight SW-SoC Solution for Respiratory Medical Device

Dec. 2019 - Dec. 2020

Ministry of Trade, Industry and Energy, Korea

- Designed a 2D graphics accelerator architecture optimized for graph visualization tasks in lightweight medical devices. This accelerator was mounted to the processor with ARM Cortex-Mo core and AHB bus. [Electronics 2021 (J2)]
- Developed a software stack for hardware implementation of Lempel-Ziv 77 lossless decompression accelerator. My work was C code-based prototyping, PNG pre-processing software, and evaluation. [Micromachines 2021 (J1)]

Participated in designing several digital VLSI chips using Synopsys EDA tools. [See list ↓↓]

## TEACHING EXPERIENCE

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**Teaching Assistant** for “Computer Architecture”, SEOULTECH

**Fall 2021**

- Grading

**Teaching Assistant** for “Digital System Design”, SEOULTECH

**Spring 2021**

- Grading, preparation of lab lecture materials

## TECHNICAL SKILLS

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<b>Computer Programming</b>	Programming Languages	C, C++, Python, Perl, Bash, MATLAB, R*
	Version Control	Git, SVN
	Operating System Development	FreeRTOS, TI Vision SDK, PetaLinux
	Machine Learning Toolkit	Tensorflow*, PyTorch*
	Document Tools	LaTeX, Obsidian (Markdown)
<b>Digital Hardware Design</b>	Hardware Description Language	Verilog, SystemVerilog, Chisel
	Simulation	Verilator, ModelSim
<b>FPGA-based Design</b>	Xilinx FPGA Tools	Vivado, Vitis
	Intel FPGA Tools	Quartus II/Prime, Nios II EDS
<b>Digital VLSI Design</b>	Synopsys EDA Tools	VCS (Simulation), Verdi (Analysis), Formality (Validation)
		Design Compiler (Synthesis), IC Compiler I/II (Layout)
		StarRCXT (Parasitic Extraction), PrimeTime (STA)
	Cadence EDA Tools	Virtuoso Layout Suite* (Layout)
		Calibre DRC*/LVS* (Physical/Layout Verification)
<b>PCB Design</b>	Cadence CAD Tools	OrCAD Capture* (Schematic), Allegro PCB Designer* (Artwork)
<b>Miscellaneous</b>	GUI Programming Framework	Winform/WPF* (C#), JavaFX* (Java), Qt* (C++), Kivy* (Python)
	Mobile Programming	Android* (Java)
	Familiar OS for development	Ubuntu, Windows 10 (with WSL), CentOS

\* stands for beginner level.

## TRAINING

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ISO 26262:2018 Functional Safety Engineering Course: Automotive Foundation Level (FSE-AFL), DNV	<b>2023.01.02-01.04</b>
Design of High-speed Memory Interface, IDEC	<b>2022.12.09</b>
Cell-based Chip Design Flow for Samsung 28nm Process, IDEC	<b>2021.11.01-11.05</b>
[Synopsys] Block-level Auto P&R utilizing IC Compiler II, IDEC	<b>2021.10.19-10.21</b>
Cell-based Chip Design Flow, IDEC	<b>2021.07.05-07.09</b>
[Infineon] Automotive Semiconductor Expert Training - Basic Course, KSIA	<b>2021.06.30-07.02</b>
Cell-based Chip Design Flow, IDEC	<b>2020.08.10-08.14</b>

## PROFESSIONAL SERVICES

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Reviewer, IEEE Access

**2023**

## MILITARY SERVICE

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**Full-time Reserve Service**

**Oct. 2015 - Jul. 2017**

Republic of Korea Army

Seoul, Korea

### Peer-Reviewed Conference Papers

**C8. An SoC FPGA-based Integrated Real-time Image Processor for Uncooled Infrared Focal Plane Array.**

**Hyun Woo Oh**, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Joon Hwan Han, Jung-Ho Shin.

*Euromicro Conference on Digital System Design (DSD)*, Durres, Albania, Sep. **2023**. [Accepted] [Long Presentation]

**C7. Disparity Refinement Processor Architecture utilizing Horizontal and Vertical Characteristics for Stereo Vision Systems.**

Cheol-Ho Choi, **Hyun Woo Oh**.

*Euromicro Conference on Digital System Design (DSD)*, Durres, Albania, Sep. **2023**. [Accepted] [Long Presentation]

**C6. RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit.**

**Hyun Woo Oh**, Seongmo An, Won Sik Jeong, Seung Eun Lee.

*ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, Vienna, Austria, Aug. **2023**. [Accepted] [Oral Presentation]

**C5. Evaluation of Posit Arithmetic on Machine Learning based on Approximate Exponential Functions.**

**Hyun Woo Oh**, Won Sik Jeong, Seung Eun Lee.

*International SoC Design Conference (ISODC)*, Gangneung, Korea, Oct. **2022**.

**C4. A Local Interconnect Network Controller for Resource-Constrained Automotive Devices.**

Kwonneung Cho, **Hyun Woo Oh**, Jeongeun Kim, Young Woo Jeong, Seung Eun Lee.

*IEEE International Conference on Consumer Electronics (ICCE)*, Las Vegas, NV, USA, Jan. **2022**.

**C3. Intelligent Transportation System based on an Edge AI.**

Young Woo Jeong, **Hyun Woo Oh**, Su Yeon Jang, Seung Eun Lee.

*International Conference on Future Information & Communication Engineering (ICFICE)*, Jeju, Korea, Jan. **2022**.

**C2. Vision-based Parking Occupation Detecting with Embedded AI Processor.**

Kwonneung Cho, **Hyun Woo Oh**, Seung Eun Lee.

*IEEE International Conference on Consumer Electronics (ICCE)*, Las Vegas, NV, USA, Jan. **2021**.

**C1. Design of 32-bit Processor for Embedded Systems.**

**Hyun Woo Oh**, Kwon Neung Cho, Seung Eun Lee.

*International SoC Design Conference (ISODC)*, Yeosu, Korea, Oct. **2021**.

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### Peer-Reviewed Journal Articles

**J6. The Design of Optimized RISC Processor for Edge Artificial Intelligence Based on Custom Instruction Set Extension.**

**Hyun Woo Oh**, Seung Eun Lee.

*IEEE Access*, Vol. 11, pp. 49409-49421, May **2023**.

**J5. An Edge AI Device based Intelligent Transportation System.**

Youngwoo Jeong, **Hyun Woo Oh**, Soohee Kim, Seung Eun Lee.

*Journal of Information and Communication Convergence Engineering*, Vol. 20, No. 3, pp. 166-173, Sep. **2022**.

**J4. A Multi-Core Controller for an Embedded AI System Supporting Parallel Recognition.**

Suyeon Jang, **Hyun Woo Oh**, Young Hyun Yoon, Dong Hyun Hwang, Won Sik Jeong, Seung Eun Lee.

*Micromachines*, Vol. 12, No. 8, Jul. **2021**.

**J3. ASimOV: A Framework for Simulation and Optimization of an Embedded AI Accelerator.**

Dong Hyun Hwang, Chang Yeop Han, **Hyun Woo Oh**, Seung Eun Lee.

*Micromachines*, Vol. 12, No. 7, Jul. **2021**.

**J2. The Design of a 2D Graphics Accelerator for Embedded Systems.**

**Hyun Woo Oh**, Ji Kwang Kim, Gwan Beom Hwang, Seung Eun Lee.

*Electronics*, Vol. 10, No. 4, Feb. **2021**.

**J1. Lossless Decompression Accelerator for Embedded Processor with GUI.**

Gwan Beom Hwang, Kwon Neung Cho, Chang Yeop Han, **Hyun Woo Oh**, Young Hyun Yoon, Seung Eun Lee.

*Micromachines*, Vol. 12, No. 2, Jan. **2021**.

<b>A RISC-V Processor Supporting AMBA AXI Protocol for Embedded Systems</b>	<b>Jul. 2022</b>
<ul style="list-style-type: none"><li>• Designer: Won Sik Jeong, Sun Beom Kwon, <b>Hyun Woo Oh</b>, Jeongeun Kim</li><li>• Technology: Samsung 28nm RFCMOS (1-poly 8-metal)</li><li>• Role: RTL Verification</li></ul>	
<b>Robot-Specific Processor for Autonomous Driving</b>	<b>Jul. 2022</b>
<ul style="list-style-type: none"><li>• Designer: Youngwoo Jeong, Yue Ri Jeong, <b>Hyun Woo Oh</b>, Kwang Hyun Go</li><li>• Technology: Samsung 28nm RFCMOS (1-poly 8-metal)</li><li>• Role: System Verification Assistant</li></ul>	
<b>In-Vehicle Network Processor based on Cortex-Mo</b>	<b>Mar. 2022</b>
<ul style="list-style-type: none"><li>• Designer: Kwon Neung Cho, Jeong Eun Kim, <b>Hyun Woo Oh</b></li><li>• Technology: TSMC 180nm RFCMOS (1-poly 6-metal)</li><li>• Role: System Verification SW Dev., RTL Verification, Pre/Post-Layout Simulation</li></ul>	
<b>A Programmable Embedded AI Processor with Cortex-Mo</b>	<b>Jul. 2021</b>
<ul style="list-style-type: none"><li>• Designer: Kwon Neung Cho, Young Woo Jeong, <b>Hyun Woo Oh</b>, Chang Yeop Han</li><li>• Technology: Samsung 28nm RFCMOS (1-poly 8-metal)</li><li>• Role: RTL Subblock Design</li></ul>	
<b>32-bit Processor with Posit Arithmetic Coprocessor for Embedded Systems</b>	<b>Jul. 2021</b>
<ul style="list-style-type: none"><li>• Designer: <b>Hyun Woo Oh</b>, Jeong Eun Kim, Do Young Choi, Kwang Hyun Go</li><li>• Technology: Samsung 28nm RFCMOS (1-poly 8-metal)</li><li>• Role: RTL Design &amp; Verification, ASIC Design Front-end/Back-end, Firmware Development, PCB Design &amp; Chip Test</li></ul>	
<b>Implementation of Lossless Decompression Accelerator Based on Inflate Algorithm</b>	<b>Sep. 2020</b>
<ul style="list-style-type: none"><li>• Designer: Gwan Beom Hwang, Do Young Choi, <b>Hyun Woo Oh</b>, Chang Yeop Han</li><li>• Technology: Samsung 65nm RFCMOS (1-poly 8-metal)</li><li>• Role: System Verification SW Dev., PCB Design &amp; Chip Test</li></ul>	
<b>Communication System with Simple and Fast Communication Error Check Code Based on CRC</b>	<b>Jun. 2020</b>
<ul style="list-style-type: none"><li>• Designer: Chang Yeo Hanp, Kwon Neung Cho, <b>Hyun Woo Oh</b></li><li>• Technology: Magnachip Hynix 0.18um CMOS</li><li>• Role: RTL Subblock Design</li></ul>	