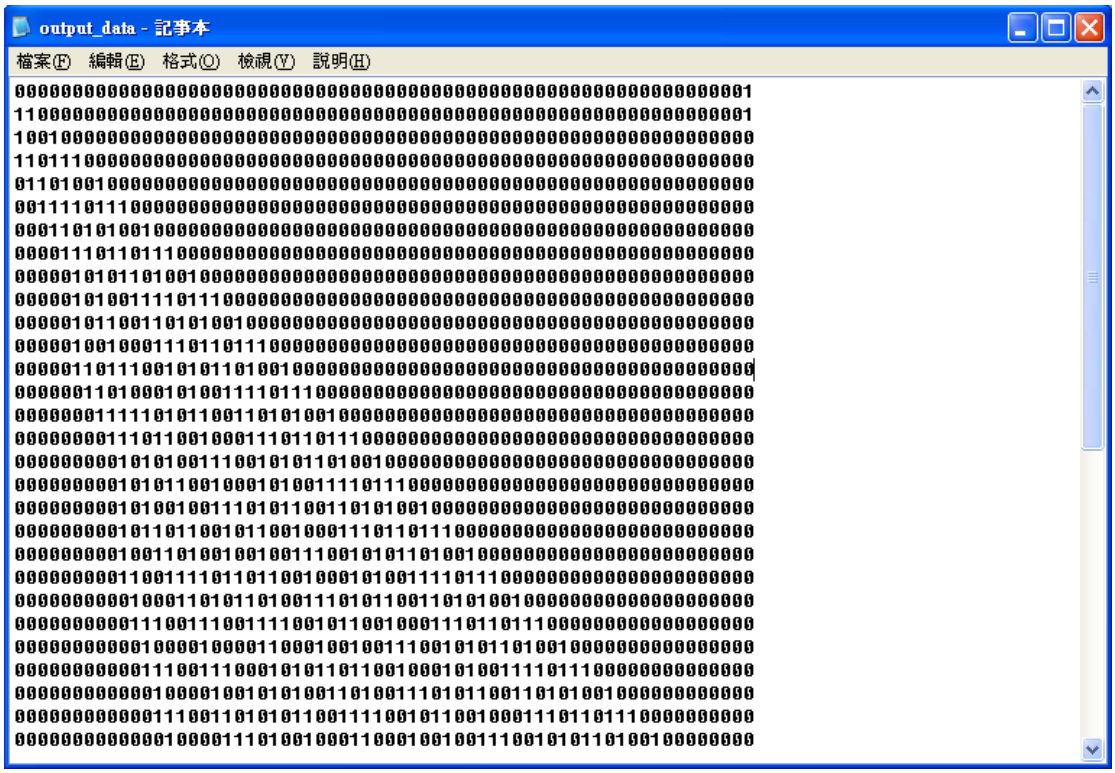
Homework 4
Due Day 6/9

Implement and simulate the 64-bit random number generator (RNG) circuit at **RTL level** introduced in Chapter 8 using Modelsim. In the simulation, **please DO NOT use the same initial seed value shown in Chapter 8 for the observation of output**. The implementation of 1D cell array with 64 cells is required.

Your project report should include the following items.

1. the Modelsim project file containing the VHDL code of the system,
2. the ppt or word files containing the simulation results and the corresponding discussions.

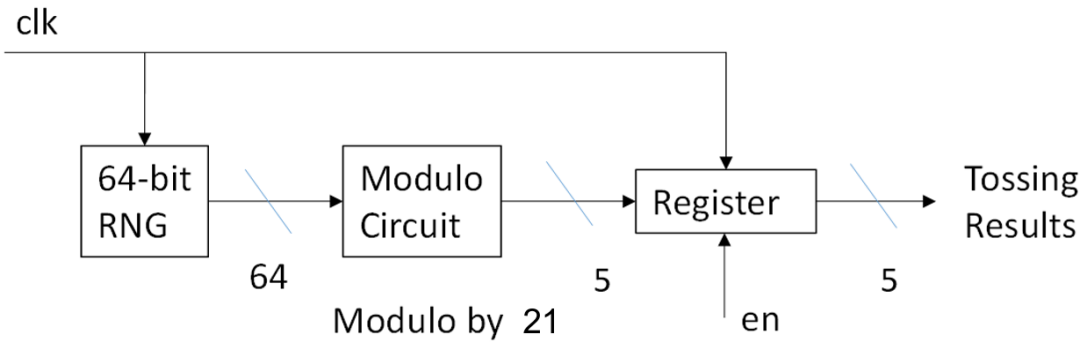
Please show your output as a textfile shown below.




## Optional:

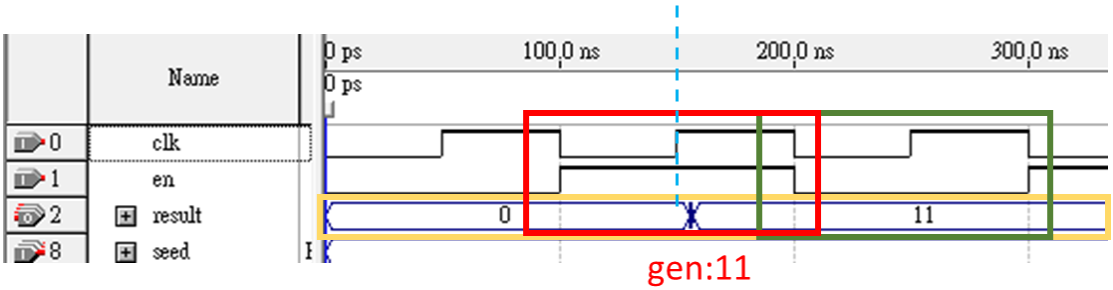
Extra credits (**40 points**) will be granted if you have successfully applied the circuit for the applications such as lottery number generation.

In our system, the lottery number is between 0 to 20. We need to generate 3 lottery numbers. As shown in the following figure, the electronic lottery generation circuit is based on 64-bit RNG and a modulo-by-21 circuit.




You can implement the modulo circuit by modulo operator (i.e., mod) in VHDL.

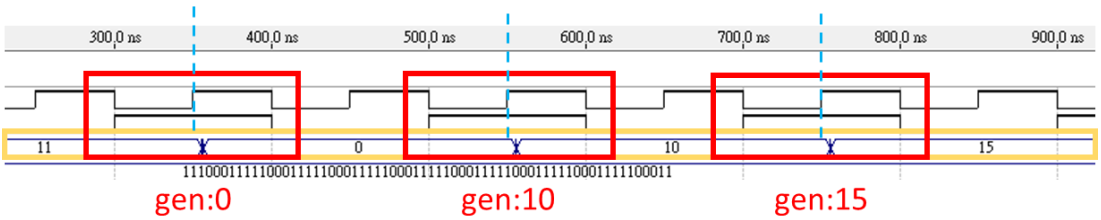
Vector Waveform(僅供參考)




說明:

可以看到每當 en=‘1’時，亂數產生器即可產生出亂數，再經過 module circuit mod 21 之後的結果。

當 en=‘0’(綠框)時，輸出不變。




請依題目敘述產生出三組 lottery number，如紅框所示。