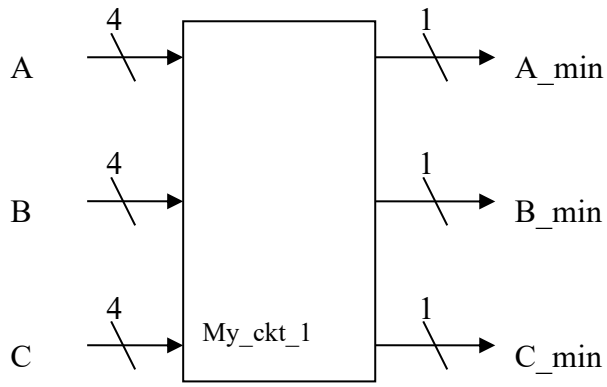
Homework 1
Due Day: 4/14

Consider a system consisting of 3 input ports and 3 output ports as shown below.



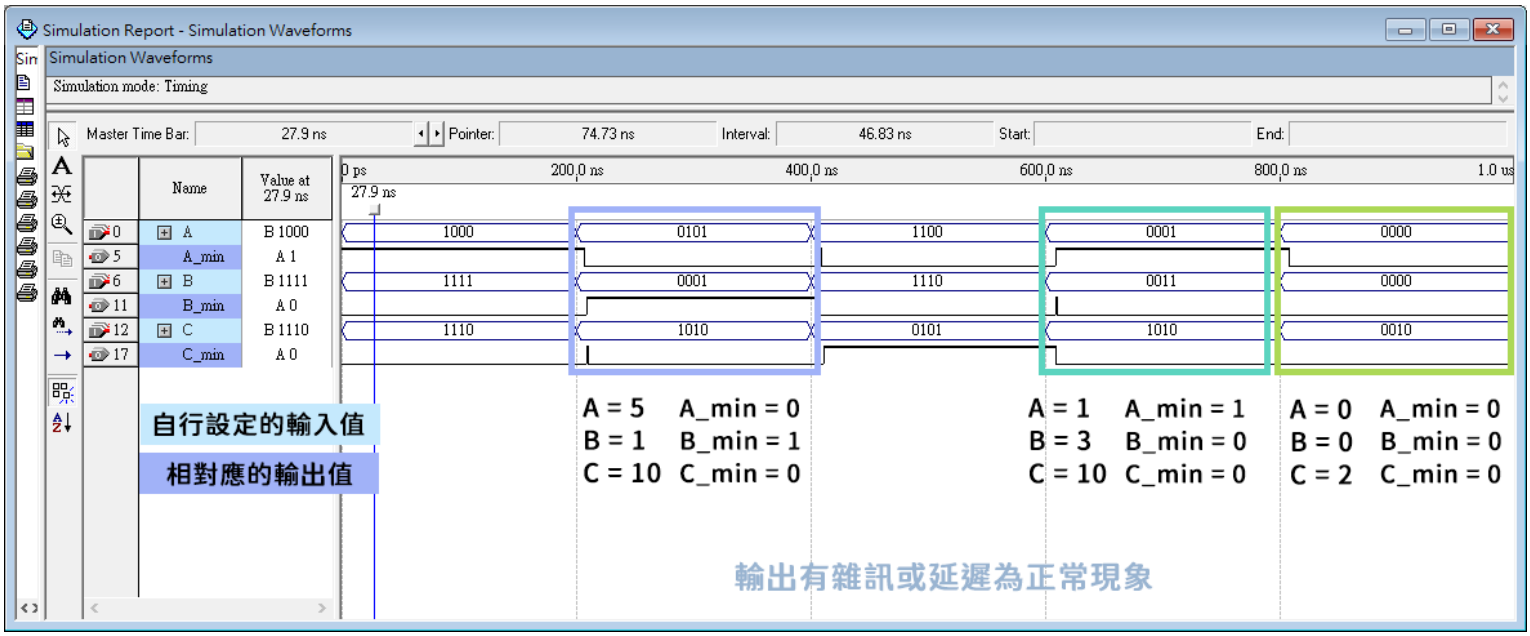
Each input port represents a 4-bit positive binary number. Each output port contains only 1 bit. Output ports will indicate which input port has minimum value. The functions of the system are shown below.

Input Ports	Output Ports
There is only one minimum value. A=min{A, B, C}	A_min=1; B_min=C_min=0;
There is only one minimum value. B=min{A, B, C}	B_min=1; A_min=C_min=0;
There is only one minimum value. C=min{A, B, C}	C_min=1; A_min=B_min=0;
Other cases	A_min= B_min= C_min=0;

Write a VHDL code to implement the system using Quartus II. Your project report should include the following items.

1. the Quartus II **project file** containing the **VHDL code** of the system,
2. **the ppt or word files** containing the **simulation results** and the **corresponding discussions**.

The next page shows the reference test data and the resulting waveform diagram after simulation. You can change the test input values yourself.


Simulation Report - Simulation Waveforms
Simulation Waveforms
Simulation mode: Timing
Master Time Bar: 27.9 ns
Pointer: 74.73 ns
Interval: 46.83 ns
Start:
End:
Name
Value at 27.9 ns
0 A B 1000
5 A_min A 1
6 B B 1111
11 B_min A 0
12 C B 1110
17 C_min A 0
0 ps
200.0 ns
400.0 ns
600.0 ns
800.0 ns
1.0 us
27.9 ns
1000
0101
1100
0001
0000
1111
0001
1110
0011
0000
1110
1010
0101
1010
0010
自行設定的輸入值
相對應的輸出值
A = 5 A_min = 0
B = 1 B_min = 1
C = 10 C_min = 0
A = 1 A_min = 1
B = 3 B_min = 0
C = 10 C_min = 0
A = 0 A_min = 0
B = 0 B_min = 0
C = 2 C_min = 0
輸出有雜訊或延遲為正常現象