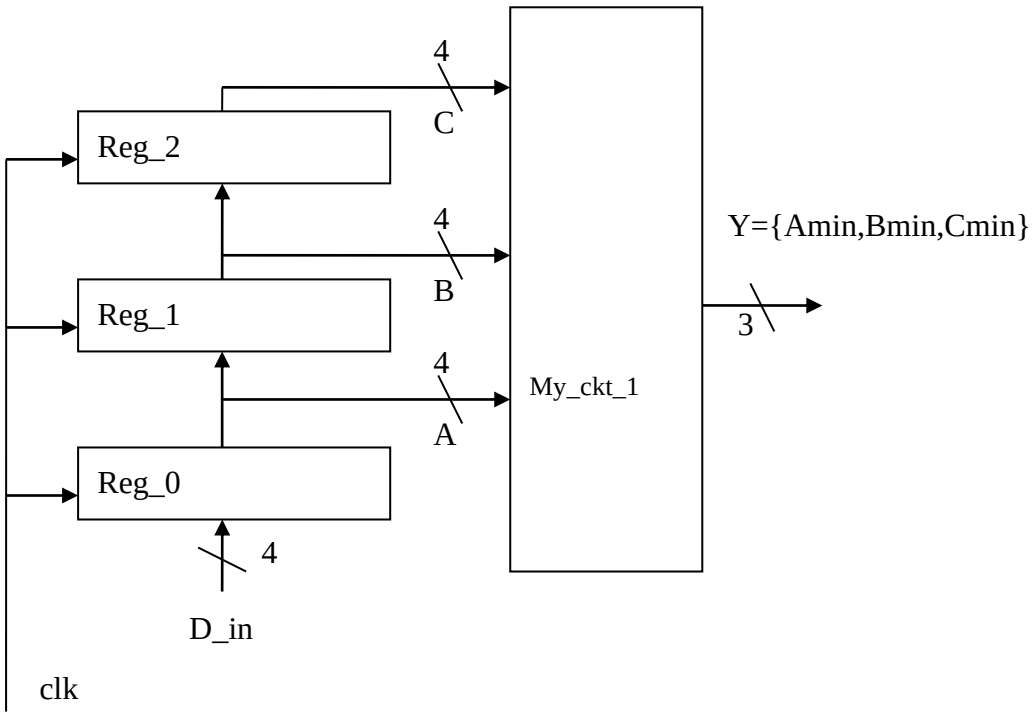
Homework 2
Due Day: 05/05

Consider a shift register based system shown below. It contains two input ports (clk and D_in) and one output port (B). The shift register in the circuit consists of three stages. The circuit with entity name My_ckt_1 is the circuit developed in the first homework.



Write a VHDL code to implement the system using Quartus II. Your project report should include the following items.

1. the Quartus II project file containing the VHDL code of the system,
2. the word files containing the simulation results and the corresponding discussions.

Reference output:

(此結果僅為參考範例，同學的輸入輸出可能與下圖不同。)

My_ckt_1 (from HW1)

Input Ports	Output Ports
There is only one minimum value. A=min{A, B, C}	A_min=1; B_min=C_min=0; Case 1
There is only one minimum value. B=min{A, B, C}	B_min=1; A_min=C_min=0; Case 2
There is only one minimum value. C=min{A, B, C}	C_min=1; A_min=B_min=0; Case 3
Other cases	A_min= B_min= C_min=0; Case 4

When rising_edge, D_in moves into the shift register