VLSI Homework #3
Due Day: 5/19

The goal of this homework is to design a traffic light control circuit. As shown in Figure 1, the circuit consists of a controller and a counter.

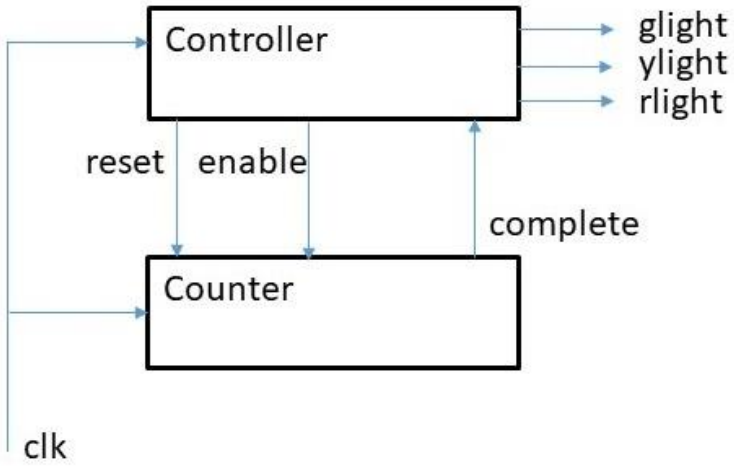

Figure 1. The architecture of the traffic light control circuit.

The ASM chart of the controller is shown in Figure 2. The controller has six states: **green1**, **green**2, **red1**, **red2, yellow1** and **yellow2**. When the controller in **green1** state, it turns on g_light (g_light=1) for the green light, and resets the counter (reset=1). It then enters **green2** state. Note that, in **green2** state, the counter is activated (enable=1).

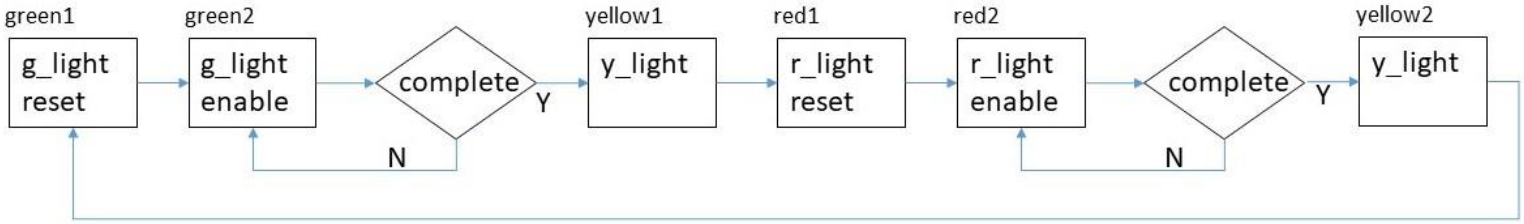

Figure 2. The ASM chart of the controller.

The counter performs up counting operations. It will be reset as 0 when reset=1. When reset=0 and enable=1, the counter will increase its counting value by 1 on the rising edge of the clock. When counting value reaches the maximum value, the complete=1.

After the counting operation is completed (complete=1), the controller then enters **yellow1** state. In the **yellow1** state, the controller turns on y_light (y_light=1) for yellow light, and then enters to **red1** state.

The states **red1** and **red2** correspond to the operations for red light. These operations are the same as those for the green light. After the completion of operations for red light, the controller turns on

yellow light again in the state **yellow2**. After that, the controller goes back to green1 state.

Implement the traffic light controller by VHDL. Your project report should include the following items.

1. the Quartus II **project file** containing the **VHDL code** of the system,
2. **The word files** containing the **simulation results** and the **corresponding discussions**.

The figure shows the reference test data and the resulting waveform diagram after simulation. You can **set the maximum value of the counter yourself**.