PAPER

SEGR- and SEB-hardened structure with DSPSOI in power MOSFETs

SEGR- and SEB-hardened structure with DSPSOI in power MOSFETs*

Zhaohuan Tang[1, 2], Xinghua Fu[1, †], Fashun Yang[1], Kaizhou Tan[2], Kui Ma[1], Xue Wu[2], and Jiexing Lin[1]

[1]College of Big Data and Information Engineering, Guizhou University, Guiyang 550025, China
[2]Science and Technology on Analog Integrated Circuit Laboratory, Chongqing 400060, China

Abstract: Single event irradiation-hardened power MOSFET is the most important device for DC/DC converter in space environment application. Single event gate rupture (SEGR) and single event burnout (SEB), which will degrade the running safety and reliability of spacecraft, are the two typical failure modes in power MOSFETs. In this paper, based on recombination mechanism of interface between oxide and silicon, a novel hardened power MOSFETs structure for SEGR and SEB is proposed. The structure comprises double stagger partial silicon-on-insulator (DSPSOI) layers. Results show that the safety operation area (SOA) of a 130 V N-channel power MOSFET in single event irradiation environment is enhanced by up to 50% when the linear-energy-transfer value of heavy ion is a constant of 98 MeV·cm^2/mg in the whole incident track, and the other parameters are almost maintained at the same value. Thus this novel structure can be widely used in designing single event irradiation-hardened power MOSFETs.

Key words: power MOSFETs; partial silicon-on-insulator; single event gate rupture; single event burnout
DOI: 10.1088/1674-4926/38/12/124006 **EEACC:** 2550R; 2560P

1. Introduction

Power MOSFETs, with the advantages of lower power dissipation, fast switching speed, high driving capability and negative temperature coefficient[1], are widely used in the power module of the electronic system in satellites, as they are incorporated in a wide variety of power control and conversion applications. When in flight, these devices are exposed to energetic heavy ions, and it has been widely accepted that the single event gate rupture (SEGR) and single event burnout (SEB) are the two catastrophic failure modes for power MOSFETs when a heavy ion passes through sensitive regions in the device[2, 3]. In 1986 and 1987, the SEB and SEGR were first reported by Waskiewicz and Fischer, respectively, which opened the door to the research of single event irradiation of power MOSFETs. During the past 30 years, the single event effect (SEE), the failure mechanisms, threshold voltage effect factors, worst testing condition of SEGR and SEB have been experimentally investigated by the technologists, such as Liu, Titus, Wheatley, *et al.*[2–5]. In particular, irradiation-hardened power MOSFETs are mainly applied in space or military systems, thus the hardening technologies for power MOSFETs are quite important. The published technologies include reducing feature size, reducing junction depth of source, increasing body doping, growing double epitaxial layer[6], growing thick oxide above neck region[7], graded doping profile in the epitaxial layer[8, 9], etc. However, with the tech-scheme of planer structure and micro-level manufacture process for power MOSFETs, the hardening technologies remain an issue in restricting its application in space.

As is known to all, a gate oxide layer and a parasitic bipolar junction transistor (comprising source, body and epitaxial layer) are inherent to the VDMOS device structure [1, 4, 7, 10]. The SEGR would occur as an ion vertically penetrates through the neck of a power MOSFET, and the SEB would happen when an ion vertically penetrates through the channel or source of the power MOSFET. If a single ion vertically penetrates through the channel area, the ion would trigger SEB, SEGR or both. No matter of the failure mode, the number of electron–hole pairs is an important factor to trigger SEE of a power MOSFET. Hence it is a useful technology to decrease the number of electron–hole pairs with recombination center in the Si–SiO_2 interface. In this paper, based on recombination mechanism of interface between oxide and silicon, a hardened structure with double stagger partial silicon-on-insulator layers in VDMOS (DSPSOI_MOS) is proposed. Simulated results show that safety operation area (SOA) of the DSPSOI_MOS is V_{gs} = 0 V and V_{ds} = 60 V at LET = 98 MeV·cm^2/mg, whereas the SOA of a conventional unhardened VDMOS is V_{gs} = 0 V and V_{gs} = 40 V at the same LET value.

2. The novel DSPSOI_MOS structure

From Ref. [11], the single event effect tolerance of a partial SOI VDMOS is much better than that of a conventional VDMOS, and the LET value of the partial SOI VDMOS is twice that of the conventional VDMOS with the same excel-

* Project supported by the National Natural Science Foundation of China (No. 61464002), the Grand Science and Technology Special Project in Guizhou Province of China (No. [2015]6006), and the Ministry of Education Open Foundation for Semiconductor Power Device Reliability (No. 010201).
† Corresponding author. Email: sisc_tang@163.com
Received 19 April 2017, revised manuscript received 15 June 2017

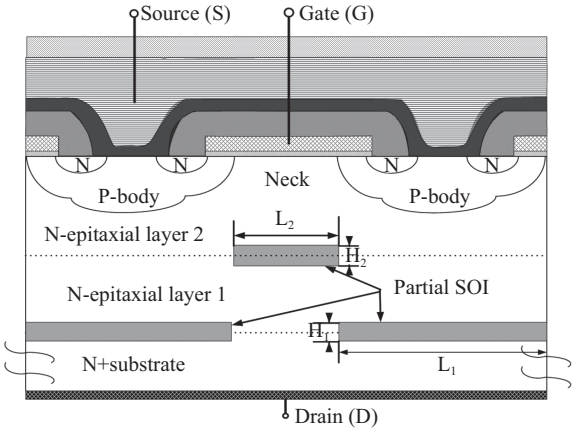

Fig. 1. Cross section of the proposed VDMOS structure.

Table 1. The structure and process parameters for a 130 V DSPSOI_MOS.

Parameters	Conventional MOS	DSPSOI_MOS	Unit
Resistivity of epitaxial	2.4	–	Ω·cm
Resistivity of layer 1	–	2.4	Ω·cm
Resistivity of layer 1	–	2.4	Ω·cm
L_1 length	–	5	μm
H_1 thickness	–	1	μm
L_2 length	–	6	μm
H2 thickness	–	1	μm
Epitaxial layer thickness	14	–	μm
Epitaxial layer 1 thickness	–	6	μm
Epitaxial layer 2 thickness*	–	8	μm
P-body junction depth	3.4	3.4	μm
P-body implanting dose	7×10^{13}	7×10^{13}	cm^{-2}
P-body width size	8	8	μm
Poly-silicon width size	8	8	μm

*2 μm is sacrificial layer, and used up in oxidation.

lent power characteristics. But there is no partial SOI below the neck region of the structure reported in the Ref. [11]. The SEGR will be triggered for the structure, if a heavy ion vertically strikes the power VDMOS from neck area.

A new DSPSOI_MOS is proposed to improve the irradiation hardness as shown in Fig. 1. The first partial SOI layer is between the N-epitaxial layer 1 and substrate, below P-body. The length of the first partial SOI layer (L1) equals the length of P-body shadow on substrate, and the thickness (H1) is 1–2 μm. The second partial SOI layer is between the N-epitaxial layer 1 and N-epitaxial layer 2, below neck region, the second partial SOI layer (L2) and neck shadow on the N-epitaxial layer1 are the same length, and the thickness (H2) is 1–2 μm, too. In particular, the thickness of N-epitaxial layer 1 equals that of N-epitaxial layer 2.

As a simulated example using a 130 V N-channel VDMOS, the cell size is 16 × 16 μm^2, the SOI is oxide, the structure and process parameters are shown in Table 1. Based on etch silicon, deposit oxide, chemical mechanical polishing, silicon-oxide bonding and double sided mask aligner, the main processing stages in fabricating the DSPSOI wafer are given in Fig. 2.

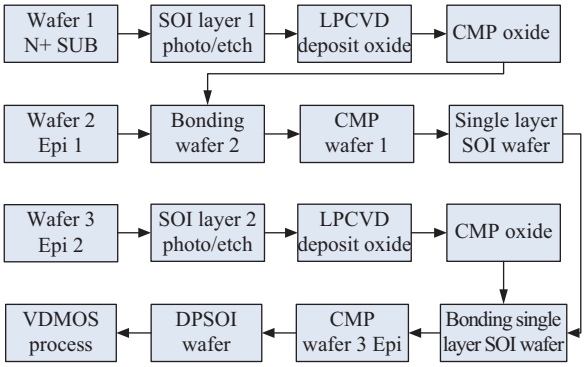

Fig. 2. (Color online) The main processing stages fabricated the DSPSOI wafer.

3. Validation and discussion

It indicates that the power VDMOS with double partial SOI holds great benefit for SEGR and SEB based on TCAD simulation. By employing the simulator, Athena in Silvaco, the conventional and proposed power VDMOS structures are created. By using Atlas simulator to call the build structure, and then using the statement, like "set LET = 98", "set density = $let*0.011", to set up LET value and the electron-hole pairs number. Further, using the command "single event upset" to define ion track information, following single event upset, the "entrypoint" and "exitpoint" are used to specify the *x*, *y*, and *z* coordinates, the "radius" specifies the radius of heavy ion track, the radius is 0.05 μm[12].

Using the Athena in Silvaco, the cross section of the proposed structure and the conventional structure are created; the simulated size is 16 × 1 μm^2, as shown in Fig. 3. The remarkable differences are that two partial SOI layers are fabricated and there are two epitaxial layers in the proposed device. From Fig. 3, no matter whether a heavy ion impacts any point on the surface of the DSPSOI_MOS, the ion would pass through a partial SOI layer.

When a single ion passes through the device as track "A" shown in Fig. 3, the SEGR characteristic curves of an N-channel VDMOS with the conventional and the proposed structure are simulated and shown in Figs. 4 and 5. From Fig. 4, when the gate-source bias (V_{gs}) is 0 V, and the drain-source bias (V_{ds}) is 40 V, the gate current keeps in a lower level, and the global device temperature is lower than 1400 K. No SEGR occurred, however, we know that when the bias is V_{gs} = 0 V and V_{ds} = 50 V, the gate current of a 16 × 1 μm^2 cell rapidly increases from ~1 μA to over 2 A in 1.5 ns, and the global device temperature is 1400 K, the SEGR is triggered at 1.5 ns. Fig. 5 is the SEE curves of the DSPSOI_MOS, if the bias is V_{gs} = 0 V and V_{ds} = 60 V, there is no SEGR in DSPSOI_MOS, and if the bias is V_{gs} = 0 V and V_{ds} = 70 V, the gate current of a 16 × 1 μm^2 cell rapidly increases from ~1 μA to 0.4 mA in 4.3 ns, and the SEGR is also triggered at 4.3 ns.

Fig. 6 illustrates the simulated SEE characteristic curves of the conventional structure and the proposed structure. When the heavy ion strikes as track "B" in Fig. 6(a), the SEB occurs after ion impacting in the conventional structure in 3.7 ns on the condition of V_{ds} = 70 V, and the SEGR is also

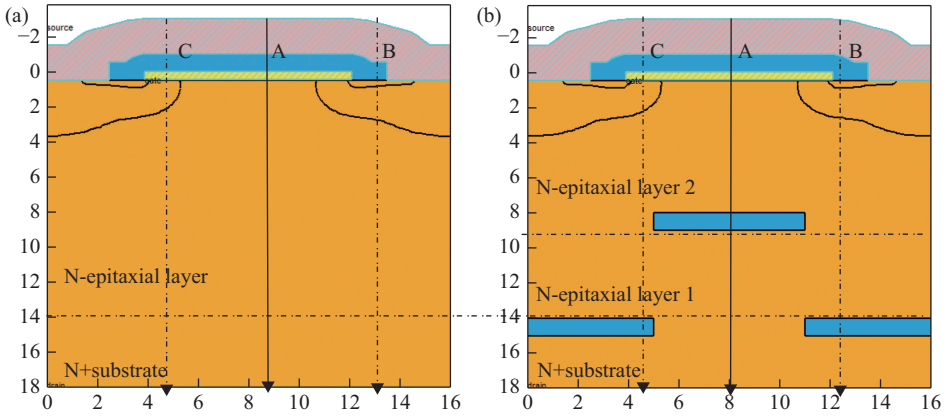

Fig. 3. (Color online) Simulated cross section of (a) the conventional structure and (b) the proposed structure.

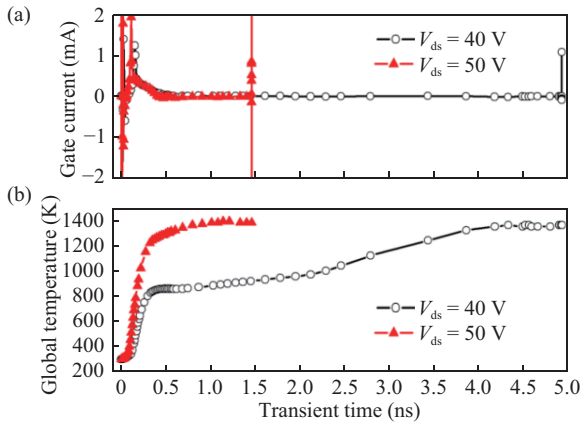

Fig. 4. (Color online) SEGR characteristic curves of an ion impacting along track "A" in the conventional VDMOS at different drain–source bias, (a) is of the transient time and gate current, (b) is of the transient time and global device temperature.

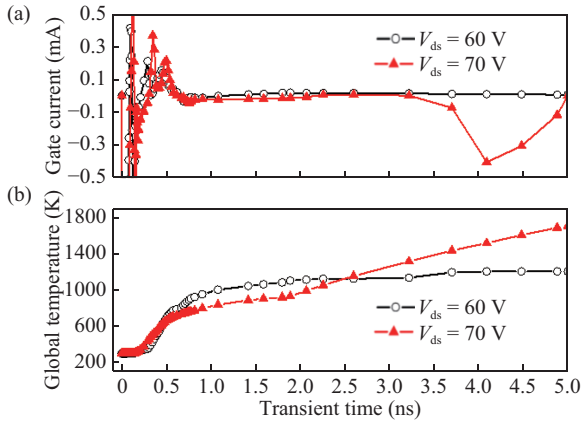

Fig. 5. (Color online) SEGR characteristic curves of an ion impacting along track "A" in the DSPSOI_MOS at different drain–source bias, (a) is of the transient time and gate current, (b) is of the transient time and global device temperature.

triggered at the same time. From Fig. 6(b), the SEB is triggered after heavy ion penetrating through the structure in 2.8 ns, and the SEGR starts to be triggered at 2.8 ns, too. Obviously, the peak drain current of conventional structure is 0.27 A whereas the peak drain current of the DSPSOI_MOS

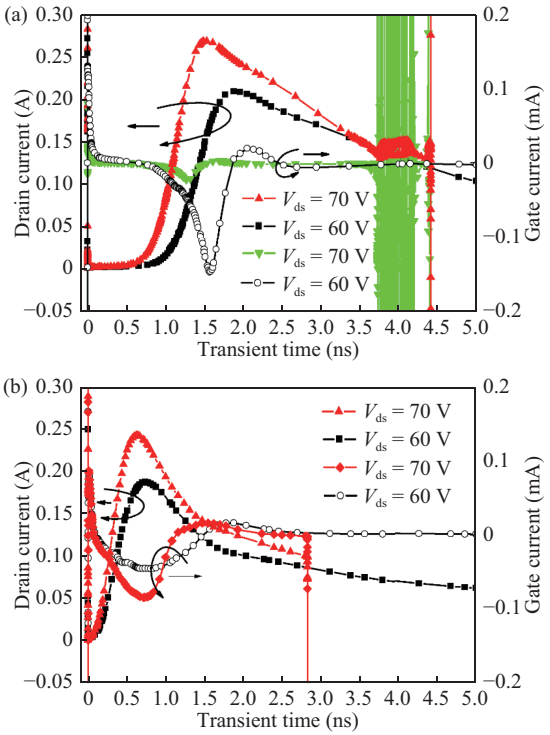

Fig. 6. (Color online) SEE characteristic curves of an ion impacting along track "B" in different drain–source bias, (a) is of the conventional structure, (b) is of the DSPSOI_MOS.

is 0.25 A.

The simulated SEB and/or SEGR characteristic curves of the conventional structure and the proposed structure are shown in Fig. 7, when the heavy ion strikes along the track "C". The SEE characteristic curves of an ion impacting along track "C" in different drain-source bias of the conventional structure are simulated, the peak drain current is 0.23 A on the condition of V_{ds} = 80 V, the SEB and SEGR are triggered at 4.5 ns. In contrast to the conventional structure, the SEGR is triggered after a heavy ion penetrates through the DSPSOI_MOS in 4.9 s, the peak drain current is 0.18 A, the peak drain current is lower than the current of the conventional structure.

In conclusion, no matter whether an ion impacts DSPSOI_MOS as track "A", "B" or "C" in Fig. 3, the single event ef-

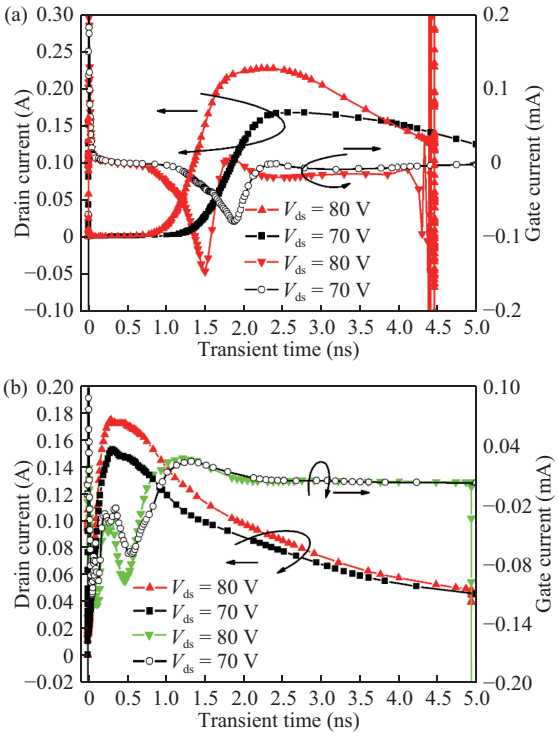

Fig. 7. (Color online) SEE characteristic curves of an ion impacting along track "C" in different drain–source bias, (a) is of the conventional structure, (b) is of the DSPSOI_MOS.

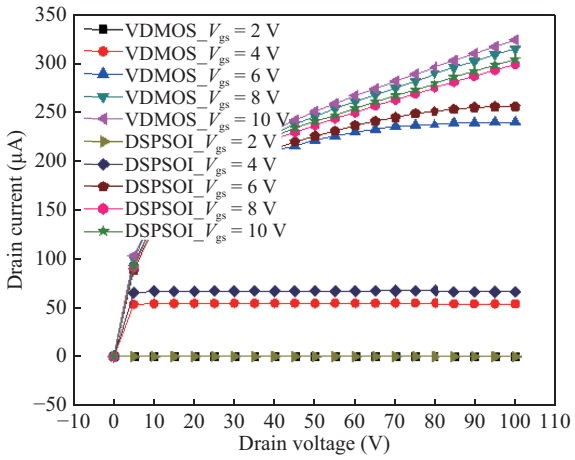

Fig. 8. (Color online) The output characteristic curves of conventional VDMOS and DSPSOI_MOS.

Table 2. The simulated DC parameters of the conventional and proposed structures.

DC parameter	Conventional VDMOS	DSPSOI_MOS
Threshold voltage (V)	2.87	2.62
Breakdown voltage (V)	150.8	161.2
Specific on-resistance (mΩ·cm^2)	10.96	11.36

fect would occur. From Figs. 4–6, we can summarize that the SOA of the conventional structure is V_{gs} = 0 V, V_{ds} = 40 V when a single heavy ion irradiates the device as a constant of 98 MeV·cm^2/mg, and the SOA of the DSPSOI_MOS is V_{gs} = 0 V, V_{ds} = 60 V. The reason that the SOA is enhanced by up to 50% is the recombination mechanism of interface between oxide and silicon, because there are large numbers of mobile ionic charges, oxide fixed charges, interface trapped charges and oxide trapped charges in SOI and the interface between oxide and silicon, added electron–holes would be reduced around the partial SOI[13–15]. From Figs. 6 and 7, the SEGR happens within 2–4 ns after the drain current increases up to the peak point. The possible reason may be that the drain current begins to drop after reaching the peak point, but the lattice temperature continues to rise, and then the intrinsic breakdown voltage of the gate oxide is reduced. The most sensitive region of the DSPSOI_MOS is the channel area. Fig. 8 is the output characteristic curves of conventional VDMOS and DSPSOI_MOS. Table 2 lists the DC parameters. Obviously, the key DC parameters of DSPSOI_MOS are almost maintained at the same value as the single event irradiation-hardened abilities are improved.

From Table 2, the specific on-resistance of the DSPSOI_MOS is 11.36 mΩ·cm^2 whereas the value for the conventional structure is 10.96 mΩ·cm^2. There is a simple model to analyze the relationship. As shown in Fig. 9, the resistance of N-epitaxial layer for a conventional VDMOS is R_{epi}, and on-resistance is given by

$$R_{on1} = R_{cts} + R_s + R_{ch} + R_{neck} + R_{epi} + R_{sub} + R_{ctd}, \quad (1)$$

where R_{cts}, R_s, R_{ch}, R_{neck}, R_{epi}, R_{sub} and R_{ctd} is the resistance of source contact, source, channel, neck area, epitaxial layer, substrate and drain contact, respectively.

The resistance of N-epitaxial layer for the DSPSOI_MOS is R_{epi1} added R_{epi2}, and on-resistance is given by

$$R_{on2} = R_{cts} + R_s + R_{ch} + R_{neck} + R_{epi1} + R_{epi2} + R_{sub} + R_{ctd}. \quad (2)$$

From Fig. 9, an isosceles right triangle is used to describe the drain current path in the epitaxial layer, the relationship between R_{epi} and R_{epi1}, R_{epi2} would be given by

$$R_{epi1} + R_{epi2} = \sqrt{2}R_{epi}, R_{epi1} = R_{epi2}. \quad (3)$$

From Ref. [1], the relationship curve between the percentage of R_{epi} in R_{on1} and different breakdown voltage for a VDMOS was given, and the value is 42% for a 130 V VDMOS. The relationship between R_{on1} and R_{on2} can be given by

$$R_{on2} = R_{on1}(0.42\sqrt{2} + 0.58) = 1.174R_{on1}. \quad (4)$$

From Eq. (4), the R_{on2} is 12.86 mΩ·cm^2 whereas the R_{on1} is 10.96 mΩ·cm^2. So the isosceles right triangle model would be used to estimate the on-resistance of DSPSOI_MOS.

4. Conclusion

A novel hardened structure for SEB and SEGR in power MOSFETs is developed. The typical differences of the structure in contrast to a conventional structure are that two partial SOI layers are fabricated in DSPSOI_MOS. The results show that SOA of a 130 V N-channel power MOSFET in

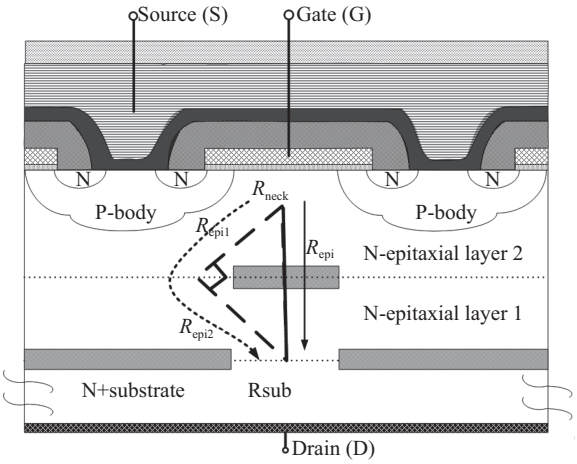

Fig. 9. The sketch map of drain current paths of a conventional VDMOS and DSPSOI_MOS.

single event irradiation is improved from V_{gs} = 0 V, V_{ds} = 0 V to V_{gs} = 0 V, V_{gs} = 60 V when the LET value of heavy ion is a constant of 98 MeV·cm^2/mg in the whole incident track. Meanwhile, the power characteristics are the same excellent values as the conventional structure. The proposed DSPSOI_MOS is simulated and demonstrated to be appropriate for application in space irradiation environment.

References

[1] Sze S M. Physics of semiconductor devices. 2nd ed. Wiley, 1981: 222

[2] Johnson G H, Galloway K F, Schrimpf R D, et al. A physical interpretation for the single event gate rupture cross-section of N-channel power MOSFETs. IEEE Trans Nucl Sci, 1996, 43(6): 2932

[3] Johnson G H, Palau J M, Dachs C, et al. A review of the techniques used for modeling single-event effects in power MOSFETs. IEEE Trans Nucl Sci, 1996, 43(6): 546

[4] Sandra L, Jeffery L T, Christopher D, et al. Recommended test conditions for SEB evaluation of planar power DMOSFETs. IEEE Trans Nucl Sci, 2008, 55(6): 3122

[5] Sandra L, Jeffery L T, Max Z, et al. Worst-case test conditions of SEGR for power DMOSFETs. IEEE Trans Nucl Sci, 2010, 57(1): 279

[6] Saburo T, Takashi K, Fumiaki K, et al. Semiconductor device having an SEB voltage suitable for use in space. USA Patent, US6885063 B3, 2005

[7] Tang Z H, Hu G Y, Chen G B, et al. A novel structure for improving the SEGR of a VDMOS. J Semicond, 2012, 33(4): 044002

[8] Dumitru S, Marc H V, Eric K. Pseudo self aligend radhard MOSFET and process of manufacture. USA Patent, US0181280 A1, 2013

[9] Jia Y P, Su H Y, Jin R, et al. Simulation study on single event burnout in liner doping buffer layer engineered power VDMOSFET. J Semicond, 2016, 37(2): 024008

[10] Jeffery L T. An updated perspective of single event gate rupture and single event burnout in power MOSFETs. IEEE Trans Nucl Sci, 2013, 60(3): 1912

[11] Li Z H, Zhang Z C, Zhang B, et al. The radiation characteristic of partial SOI VDMOS. International Conference on Communications, Circuits and Systems, 2008: 1361

[12] Silvaco Company, Atlas User's Manual.Version W-2013.10, 2013

[13] Vladimir V E, Alexander S, Vatuev, et al. New insight into heavy ion induced SEGR impact of charge yield. 15th European Conference on Radiation and Its Effects on Components and Systems, 2015: 1

[14] Cheng H Y, Ying W, Fei C, et al. Research of single-event burnout in power planar VDMOSFETs by localized carrier lifetime control. IEEE Trans Nucl Sci, 2014, 62(1): 143

[15] Arto J, Veronique F, Alexander B, et al. SEGR in SiO_2–SI_3N_4 stack. IEEE Trans Nucl Sci, 2014, 61(4): 1902