This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

Single-Event Damage observed in GaN-on-Si HEMTs for Power Control Applications

E. Mizuta, S. Kuboyama, Y. Nakada, A. Takeyama, T. Ohshima, Y. Iwata, and K. Suzuki

***Abstract*—The single-event damage observed in AlGaN/GaN High Electron Mobility Transistors (HEMTs) was investigated. For power control applications, normally–off operation is achieved by p-type GaN gate material and its rated drain–source voltage of 600 V. Because of no gate insulator, Single-Event Gate Rupture (SEGR) is essentially excluded. Therefore, the HEMTs are expected to exhibit better immunity to heavy ions in comparison with SiC power MOSFETs. In the test results, two types of catastrophic failure modes were observed with different leakage current paths; one failure mode was caused by the introduction of a leakage current path between the drain and Si substrate via the buffer layer. The other was caused by the damage between the drain and source electrodes.**

两种类型 一种是漏和硅衬底的泄漏电流 一种是漏和源电极的损伤

***Index Terms*—GaN, Gallium Nitride, GIT, FET, power device, normally-off**

I. Introduction

GALLIUM Nitride (GaN) is one of the candidate materials for next-generation semiconductor devices. Wide bandgap semiconductor devices such as GaN and SiC exhibit fast electron mobility and high breakdown field strength [1] - [5], and are expected to significantly reduce energy losses. These devices are also attractive for next-generation satellites to reduce the energy losses in high-power, high-voltage and high-frequency systems. Although Si remains the dominant material used in semiconductor devices for space systems, there is a strong demand to develop new devices utilizing GaN or SiC materials. For GaN devices, the Single-Event Effects (SEEs) on HEMTs for telecommunication or radar components have already been evaluated [6] – [10]. However, there are few reports about SEEs on GaN devices with normally-off operation [11] for power control applications, and no reports have discussed the failure mechanisms thereof.

In this study, AlGaN/GaN HEMTs were evaluated for Single-Event Effects (SEEs) with heavy ions and under several test conditions. As the result of this study, it was confirmed that the SEGR-related failure mode was excluded, and that two types of failure mode were observed. The failure modes were discussed in terms of their failure mechanisms.

II. Experimental

The GaN HEMTs used in this study are prototypes of PGA26E19 manufactured by Panasonic with AlGaN/GaN layers on Si wafer. Fig. 1 shows the cross-sectional structure of the HEMTs. The normally-off operation is achieved by a selectively thinned i-AlGaN layer underneath the p-GaN controlling gate, in which holes are injected from the p-type gate to the Two-Dimensional Electron Gas (2DEG) region for conductivity modulation [12]. The structure is referred to as Gate Injection Transistors (GITs) to distinguish from conventional Field Effect Transistors (FETs). As the gate is not isolated with any insulator film, gate current can flow reproducibly depending on the gate bias voltage. Therefore, the device is not expected to pose any risk for SEGR, in which the gate insulator material is damaged by heavy ions.

The HEMTs also utilize the Hybrid Drain-embedded (HD) structure to accomplish the current-collapse-free operation observed under a high drain voltage condition [13]. The current-collapse is a temporal phenomenon which is increase of the dynamic on-state resistances after applying high drain voltage. The phenomenon is generally observed in GaN-based power devices. There are no other reports of completely eliminating this phenomena in normally-off GaN power transistors with operating voltage of 600 V and higher. For the HD structure, the p-GaN region is formed in the vicinity of the drain electrode. This p-GaN region is electrically connected to the drain electrode via the metallization layer. Holes are injected from the p-GaN in the off-state by applying high drain

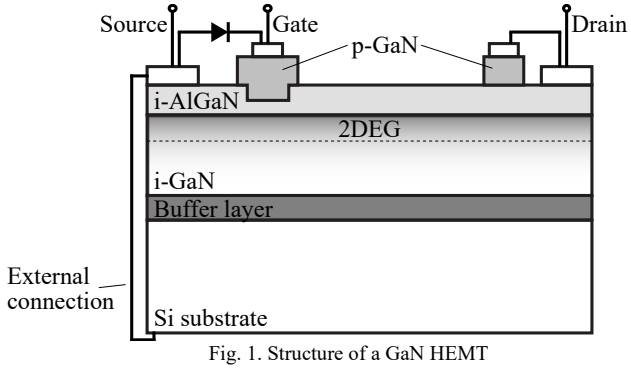

Fig. 1. Structure of a GaN HEMT

Manuscript received September 29, 2017; revised February 2, 2018 and March 9, 2018; accepted March 12, 2018.

E. Mizuta, S. Kuboyama, Y. Nakada, and K. Suzuki are with Japan Aerospace Exploration Agency, Tsukuba, Ibaraki 305-8505, Japan (corresponding author to provide phone: +81-50-3362-4328; e-mail: mizuta.eiichi@jaxa.jp).

A. Takeyama, and T. Ohshima are with Takasaki Advanced Radiation Research Institute, National Institutes for Quantum and Radiological Science and Technology, Takasaki, Gunma 370-1292, Japan (e-mail: takeyama.akinori@qst.go.jp).

Y. Iwata is with National Institute of Radiological Sciences, National Institutes for Quantum and Radiological Science and Technology, Inage, Chiba 263-8555, Japan (e-mail: iwata.yoshiyuki@qst.go.jp).

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

Table 1. Specifications of GaN HEMTs used in this study.

Item (@T_j =25 °C)	Specified value
$V_{DSS\ min.}$	600 V
$I_{D\ max.}$	10 A
Ron $_{typ.}$	140 mΩ
$I_{DSS\ max.}$	39 μA
V_{TH}	0.9 - 1.6 V

voltage, which effectively releases the electrons trapped during the transition period of switching operations. In order to avoid the depletion of 2DEG under the p-GaN region, a thicker i-AlGaN layer is employed.

Table 1 shows the specifications of the HEMTs used in this study. The source electrode and Si substrate are electrically connected inside the package in the GaN HEMTs.

This study used Ar, Kr and Xe heavy ions, the characteristics of which are listed in Table 2. The thickness of the i-GaN layer including i-AlGaN and the electrode is less than 10 μm (GaN equivalent). The ranges of heavy ions are sufficient to traverse the active layer of the HEMTs. The irradiation experiments were conducted at Takasaki Ion Accelerators for Advanced Radiation Application (TIARA) and Heavy Ion Medical Accelerator in Chiba (HIMAC) at the National Institutes for Quantum and Radiological Science and Technology (QST) and RI Beam Factory (RIBF) at RIKEN Nishina Center. All the experiments were performed at room temperature. The fluence of the ions was set to 1×10^5 - 1×10^7 cm^{-2} for each irradiation run. The gate source voltage V_{GS} was set to 0.95, 0.0 or −2.5 V. The post-irradiation gate stress test (PIGS) was not performed, because of no gate oxide in the HEMTs. To protect the current measurement instruments, resistors were inserted in series for both the gate (540 Ω) and drain (100 kΩ) terminals of each sample device, and a ceramic capacitor of 68 nF was connected to the drain and source terminals in parallel to supply sufficient current during the SEE events. Current limiter of the power supply was set to 10 mA during the irradiations.

Table 2. Characteristics of the ion species used in this study.

Ion species	Energy [MeV]	LET@surface [MeV/(mg/cm^2)] GaN	(Si)	Range [μm] GaN	(Si)	Facility
$^{40}Ar^{8+}$	104	13.0	(17.0)	14.4	(27.3)	QST TIARA
$^{84}Kr^{17+}$	315	30.6	(40.0)	21.0	(40.1)	QST TIARA
$^{129}Xe^{23+}$	443	52.9	(69.2)	19.9	(37.8)	QST TIARA
^{132}Xe	22849	9.8	(11.4)	2370	(5290)	QST HIMAC
	16435	12.0	(14.1)	1400	(3100)	QST HIMAC
	15306	12.6	(14.7)	1250	(2760)	QST HIMAC
	5147	25.4	(30.0)	241	(512)	QST HIMAC
$^{86}Kr^{31+}$	1607	18.0	(22.5)	112	(229)	RIKEN

III. Results

A. Ion species dependence

Fig. 2 shows the typical experimental results for the cases, in which the incident ions hit normal to the chip surface. In Fig. 2 (a), the change of I_{DS} during irradiation is shown as a function of fluence at V_{GS} = −2.5 V. The fluence of the ions was set to

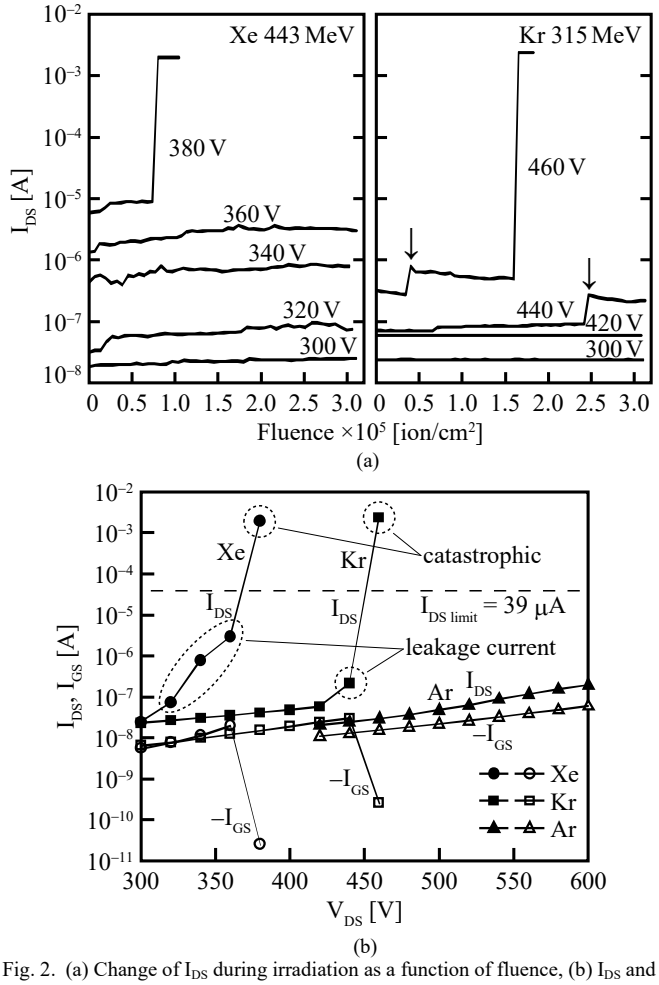

Fig. 2. (a) Change of I_{DS} during irradiation as a function of fluence, (b) I_{DS} and I_{GS} at the end of each irradiation run as a function of V_{DS}.

3×10^5 cm^{-2} for each voltage step. A sample device was irradiated sequentially from V_{DS} = 300 V with 20 V steps. Therefore, each curve indicates the increase in leakage current introduced by the heavy ions during irradiation. For 443 MeV Xe ions, the permanent leakage current increased continuously along with increasing fluence in the range of 300 - 360 V, and finally the device was destroyed at 380 V due to excessive current. The continuous behavior suggests that the damage consists of localized small damage sites introduced by each ion strike. For 315 MeV Kr ions, leakage current did not increase up to V_{DS} = 420 V. At V_{DS} = 440 V, a stepwise increase in leakage current was observed in addition to a slightly continuous increase. After the stepwise increase, the leakage current gradually decreased. The same type of stepwise increase was observed at 460 V, and then the device was destroyed during the irradiation run due to excessive current. Both devices showed an abrupt decrease of I_{GS} after the catastrophic failure. In Fig. 2 (b), I_{DS} and I_{GS} at the end of each irradiation run are shown as a function of V_{DS} for the devices used for the experiments shown in Fig. 2 (a). The difference in behavior of the Xe and Kr ions might be attributable to the difference of LET used to create the damage sites. When the small leakage current of I_{DS} was observed, I_{GS} was not

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

increased as I_{DS}. Conversely, the current of I_{GS} decreased when the catastrophic damage occurred. Ar ions were also tested; however, no leakage or catastrophic failure was observed up to 600 of V_{DS} as shown in Fig. 2 (b).

Fig. 3 shows the I_{DSS}–V_{DS} curves at pre- and post-irradiation for the device (shown in Fig. 2) irradiated by Xe ions at V_{GS} = –2.5 V. After the irradiation, an ohmic behavior with resistance of around 600 Ω was observed. For this type of failure mode, there were no apparent burnout signatures on the chip surface. To locate the leakage current path in this device, pre- and post-irradiation I–V curves for the gate to drain/source were compared as shown in Fig. 4 (a) and (b), respectively. The

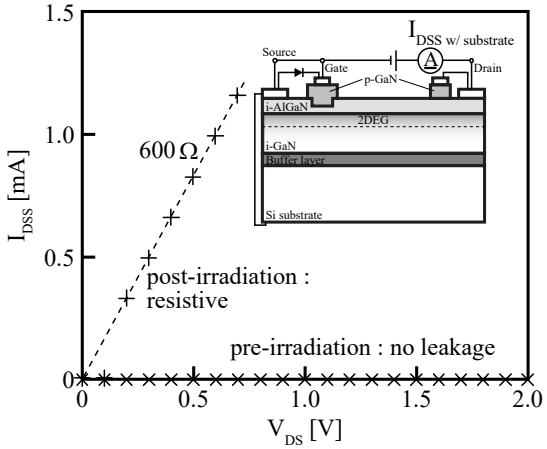

Fig. 3. I_{DSS}-V_{DS} curves at the pre- and post-irradiation for the device irradiated by Xe ions at V_{GS} = –2.5 V (shown in Fig. 2).

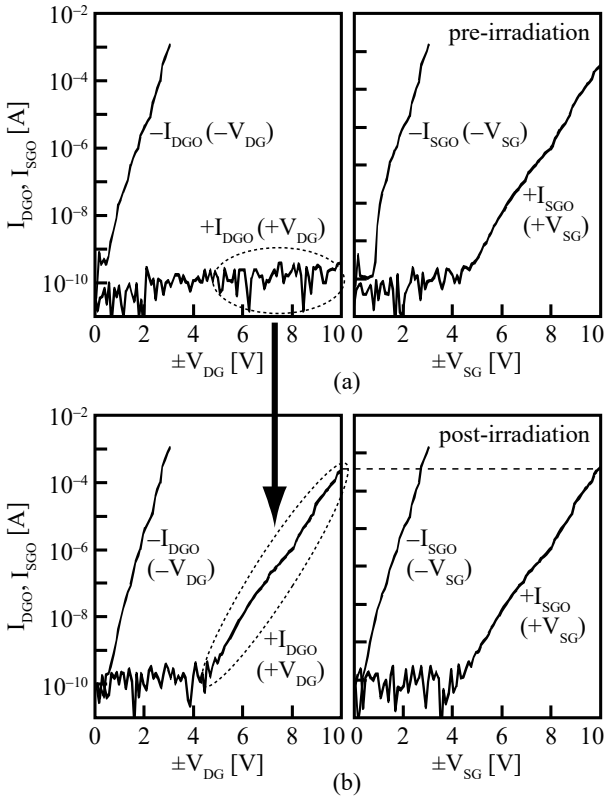

Fig. 4. I–V curves for the device irradiated by Xe ions at V_{GS} = –2.5 V (shown in Fig. 2); (a) pre- irradiation, (b) post- irradiation.

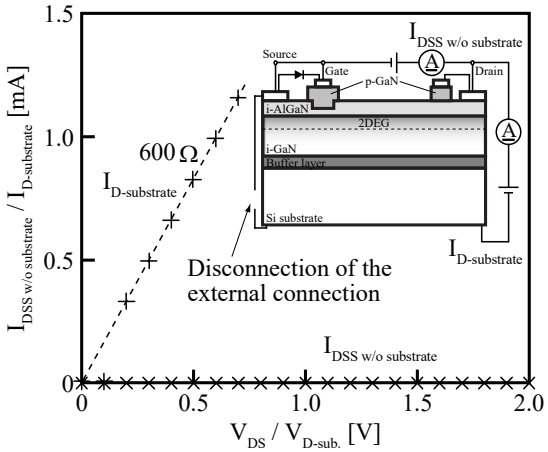

Fig. 5. Leakage current path analysis for the device irradiated by Xe ions at V_{GS} = –2.5 V (shown in Fig. 2).

forward I–V curves for the gate–channel heterojunction are indicated by $-I_{DGO}$ and $-I_{SGO}$; $+I_{DGO}$ is the reverse curve. For the pre-irradiation condition, the current from the source to the gate ($+I_{SGO}$) mostly flows through the on-chip protection diode inserted between the gate and the source. For the post-irradiation condition, the behavior of $-I_{DGO}$, $+I_{SGO}$ and $-I_{SGO}$ did not change; however, $+I_{DGO}$ became identical to $+I_{SGO}$. This result suggests that the source and drain were shorted by an ohmic path introduced by irradiation. However, there were no apparent burnout signatures on the chip surface.

To locate the leakage current path more precisely, the electrical connection between the source and substrate was disconnected. After the disconnection, the leakage current path was identified between the drain and substrate as shown in Fig. 5. The result suggests that the drain region was damaged and a leakage current path running from the drain to the substrate was introduced. The damage model is consistent with the fact that there were no burnout signatures on the chip surface. Because the active layer of the devices is deposited on the Si substrate, a conductive filament is formed traversing the drain electrode, the GaN layer, the buffer layer, and the substrate along the ion trajectory. This conductive path might be responsible for the catastrophic failure.

To enforce the failure mechanism mentioned above, we performed the charge collection measurements. Fig. 6 shows the collected charge spectra obtained by using 1607 MeV Kr ions. The fluence of the ions was set to 1×10^5 cm^{-2} for each voltage step. The bias voltage was applied to the drain while the substrate was grounded. In the case of the gate and source being grounded (Fig. 6 (a)), a relatively narrow single peak was observed in all the spectra. The cross-sectional area for the peak is given by simple calculations (i.e. total count in a spectrum divided by fluence applied to obtain the spectrum). The averaged cross-sectional area is around 0.015 cm^2, and corresponds to the geometric drain area as expected. In the case of the gate and source being connected to the drain (Fig. 6 (b)), widely spread spectra were obtained. However, the calculated cross-sectional area is almost constant at around 0.027 cm^2 on average. It was identified that this value corresponded to the geometric entire active area on the Si substrate. The maximum

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

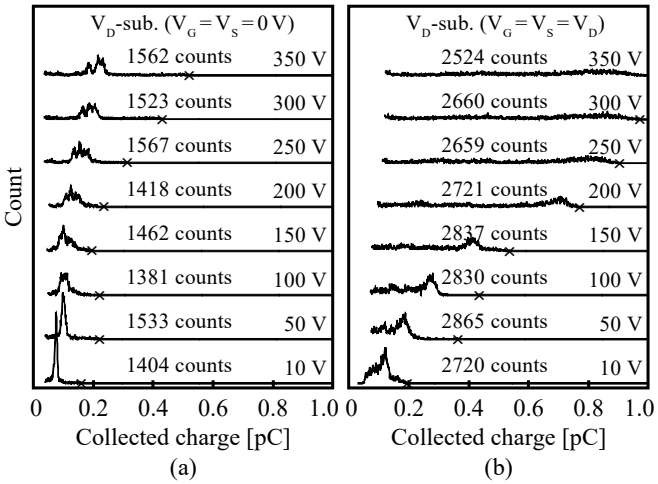

Fig. 6. Collected charge spectra obtained by Kr ion irradiation with charge collection system.

collected charge observed is around 1.1 pC, which is much less than deposited charge around 70 pC in the Si substrate. The fact suggests that the electrons generated in the Si substrate cannot penetrate the GaN layer due to the potential barrier at the Si-buffer layer boundary. These results apparently support the mechanism proposed for this type of failure (i.e. active layer and substrate connected electrically by an ion track).

Fig. 7 (a) shows the change of I_{DS} during 443 MeV Xe ion irradiation as a function of fluence at V_{GS} = 0 V. Fig. 7 (b) shows I_{DS} and I_{GS} at the end of each irradiation run as a function of V_{DS} for the devices used for the experiments shown in Fig. 7 (a). There is no difference between Fig. 2 and Fig. 7 regarding the change of I_{DS}; however, I_{GS} level after the catastrophic failure is clearly different (not abruptly decreased). In this sample device, there is an apparent burnout signature and a drain runner is also broken. Fig. 8 shows the post-irradiation I–V curves for the gate to drain/source in the same device as shown in Fig. 7. Both curves show ohmic behavior and are entirely different from the curves shown in Fig. 4. This fact suggests that the gate to channel junction was catastrophically damaged and electrically shorting paths to the source and drain

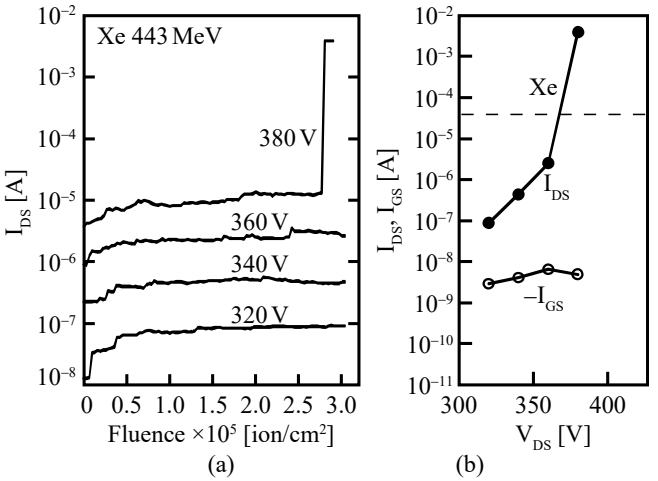

Fig. 7. (a) Change of I_{DS} during irradiation as a function of fluence, (b) I_{DS} and I_{GS} at the end of each irradiation run as a function of V_{DS}.

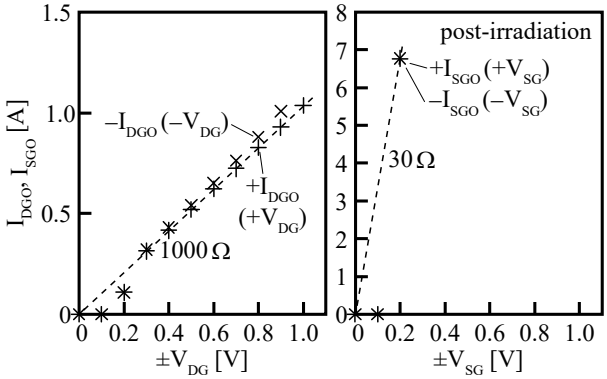

Fig. 8. Post- irradiation I–V curves of the device damaged by Xe ions.

were introduced. The failure mode in this result suggests that the GaN surface area is also sensitive to heavy ions.

B. LET dependence

To clarify LET dependence of the failures, Xe ions with several energies were irradiated. The energies were 443, 5147 and 22849 MeV, and their LETs were 52.9, 25.4 and 9.8 MeV/(mg/cm^2), respectively. For a direct comparison with Fig. 2 (b), the bias conditions and fluence for each test run were the same.

Fig. 9 shows LET dependence of the leakage current increase after each irradiation run. The data with LET of 52.9 MeV/(mg/cm^2) is the same data shown in Fig. 2 (b). For the data with LET of 9.8 MeV/(mg/cm^2) and V_{GS} of −2.5 V, no burnout or increase in leakage current was observed. The result is mostly identical to the data obtained with Ar ions with LET of 13.0 MeV/(mg/cm^2). For the data with LET of 25.4 MeV/(mg/cm^2), the increase in leakage current and catastrophic failure at 460 V of V_{DS} with V_{GS} of −2.5V were almost similar for the Kr ions with LET of 30.6 MeV/(mg/cm^2). In addition, the same type of catastrophic failure was observed at 420 V of V_{DS} with V_{GS} of 0 V. These data suggest that the failures observed in the GaN HEMTs are solely dependent on LET of ions, regardless of ion species, their energies, and ranges as demonstrated in the experiments. Note that the catastrophic failure mode observed with LET of 25.4 MeV/(mg/cm^2) was not the same for Kr ions with LET of 30.6 MeV/(mg/cm^2). The failure mode will be discussed in Section IV.

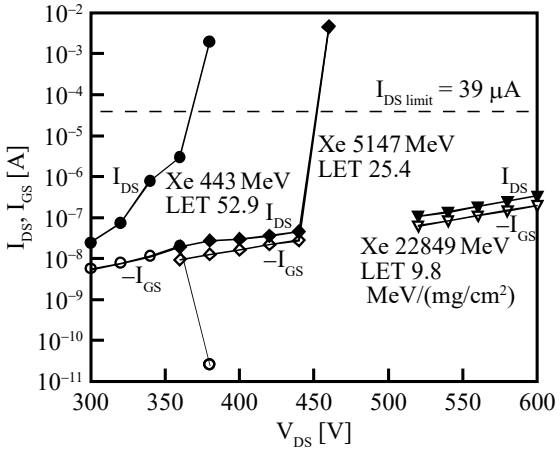

Fig. 9. I_{DS} and I_{GS} at the end of each irradiation run with various LET of Xe ions.

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

C. *Gate bias voltage dependence*

In this study, V_{GS} = –2.5 V was applied as a default during irradiation runs, because the strong reverse biased condition of the gate was usually applied for SEGR testing for power MOSFETs as the worst case. However, the GaN HEMTs have no gate oxide. Therefore, it should be important to define the worst bias voltage for V_{GS} for this type of device. Kr ions with LET of 18 MeV/(mg/cm^2) were used for the experiments. The fluence of the ions was set to 3×10^5 cm^{-2} for each voltage step of V_{DS}. The experiments were repeated with V_{GS} = –2.5, 0 and +0.95 V.

Fig. 10 shows I_{DS} and I_{GS} after each irradiation run. For V_{GS} = –2.5 V, catastrophic failure with a burnout signature was observed at V_{DS} = 520 V, and no increase in permanent leakage current was observed up to 500 V. The voltage at the catastrophic failures observed is consistent with the data shown in Fig. 9 with LET of 25.4 MeV/(mg/cm^2). $-I_{GS}$ and I_{DS} were abruptly increased to an identical value at the catastrophic failure. It indicates that a completely shorting path between the drain and gate was introduced. For V_{GS} = 0 V, although the curves were not shown in Fig. 10 for clarity, mostly the same curves were observed with the case of V_{GS} = –2.5 V, no increase in permanent leakage current was observed up to 500 V, but catastrophic failure without a burnout signature at V_{DS} = 520 V. In the case of V_{GS} = 0.95 V (i.e. near gate threshold voltage), no damage was observed up to 600 V of V_{DS}. It was demonstrated that V_{GS} = +0.95 V prevented the damage introduced by ions, and the bias condition is not the worst case. In conclusion, it was demonstrated that the worst-case gate bias voltage for this type of device is completely off state (i.e. 0 V and less).

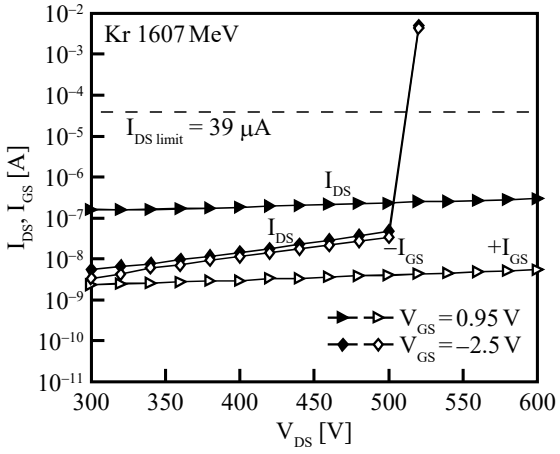

Fig. 10. V_{GS} dependence of I_{DS} and I_{GS} at the end of each irradiation run with Kr ions.

D. *V_{DS} dependence*

In the experiments described in the previous subsections, the fluence level for each irradiation run was fixed to 3×10^5 cm^{-2}. Therefore, failure modes with a cross section less than $1/(3\times10^5)$ cm^2 are essentially not observable. To observe these types of failure modes, the fluence level was extended up to 1×10^7 cm^{-2} with several fixed V_{DS} levels ranging from 280 to 400 V. In the experiments, 443 MeV Xe ions with LET of 52.9 MeV/(mg/cm^2) were irradiated. V_{GS} for all sample devices was set to 0 V. The sample size was just one device for each V_{DS}.

Fig. 11 shows the change of I_{DS} and I_{GS} during irradiation for each V_{DS}. The leakage current increase in I_{DS} was observed in the initial phase for cases of V_{DS} = 320 V and higher voltages (and in the case of V_{DS} = 400 V, the current increase was not recorded because catastrophic failure occurred before the first current measurement during irradiation). Catastrophic failures were observed all cases except V_{DS} = 280 V. The V_{DS} dependence of the fluence to the catastrophic failures was clearly observed. In the cases of V_{DS} = 360 V and higher voltage, the fluence at the catastrophic failure observed is apparently V_{DS} dependent. After the catastrophic failure occurred, I_{GS} was decreased less than 0.1 nA, similar to the data shown in Fig. 2 (b). In the cases of V_{DS} = 340, 320 and 300 V, the dependence on V_{DS} was much smaller than the higher V_{DS} cases, and I_{GS} after catastrophic failure occurred also decreased but remained larger than 1 nA. There is a possibility that the failure mode for V_{DS} = 340 V and lower voltage is different from that observed in the higher V_{DS} group.

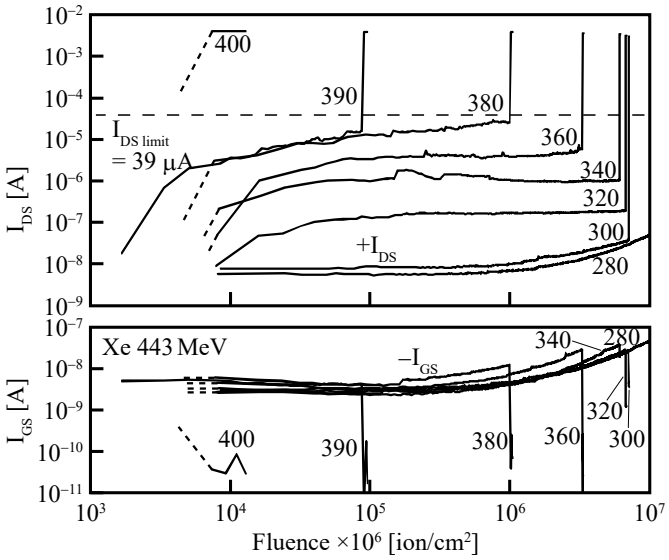

Fig. 11. Change of I_{DS} and I_{GS} during irradiation as a function of fluence by Xe ions.

E. *Irradiation angle dependence*

Given the lateral structure of the GaN HEMTs used in this study, a strong electric field is also generated parallel to the chip surface. Therefore, the worst-case susceptibility to heavy ions may be observed in that direction. To explore such possibility, experiments were conducted to irradiate ions in the direction parallel to the chip surface. This type of experiment requires long range ions. In the experiments, Xe ions with energy of 16435 and 22849 MeV with a range in GaN of 1400 and 2370 μm, respectively, were applied. V_{GS} was set to 0 V. The fluence of the ions was set to 1×10^6 cm^{-2} for each voltage step.

Fig. 12 shows I_{DS} and I_{GS} at the end of each irradiation run as a function of V_{DS}. Catastrophic failures were observed at 280

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

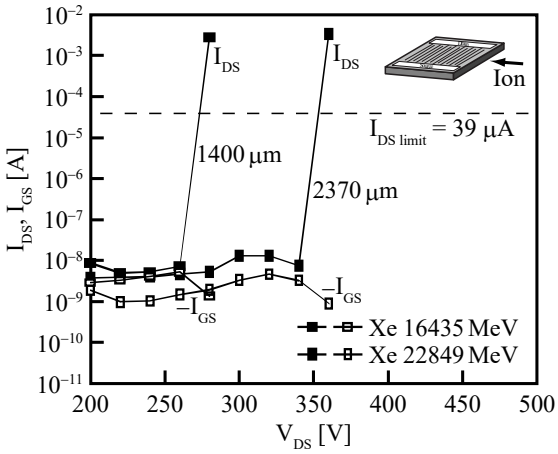

Fig. 12. Change of I_{DS} and I_{GS} at the end of each irradiation run with Xe ions (their direction parallel to the chip surface).

and 360 V of V_{DS} with 16435 and 22849 MeV Xe ions, respectively. A burnout signature was identified on the chip surface for all the sample devices tested. There was no abrupt change in leakage current in I_{GS} up to the catastrophic failure, and even after the catastrophic failure, the current level stayed at the same order of magnitude. The results suggest that the buffer layer is not damaged, because the ions never pass through the GaN active layer, buffer layer and Si substrate with the orientation. The 16435 MeV Xe ions with a range of 1400 μm are stopped inside the chip, and the maximum LET reaches 53 MeV/(mg/cm^2) at Bragg peak (estimated by SRIM). In comparison with the normal incidence case having almost identical LET of 52.9 MeV/(mg/cm^2) shown in Fig. 2 (a), the V_{DS} observed at catastrophic failure was considerably reduced from 360 to 280 V. The 22849 MeV Xe ions with a range of 2370 μm pass through the entire chip structure. The values of LET at which the burnout signature was identified were estimated by SRIM as 14 to 17 MeV/(mg/cm^2). In comparison with the normal incidence case having LET of 18.0 MeV/(mg/cm^2) shown in Fig. 12, the V_{DS} observed at catastrophic failure was also considerably reduced from 520 to 360 V. The possibility of the orientation being more susceptible to heavy ions has thus been identified.

Additional experiments were performed with the irradiation orientation parallel to the chip surface, but not traversing the drain and source stripes (i.e., incident from another side of the chip edge). In the experiments, Xe ions with energy of 15306 MeV were used. Although their range in GaN is 1250 μm and they reach their maximum LET of 53.0 MeV/(mg/cm^2) inside the chip, no damage was observed up to 600 V_{DS}. It was demonstrated that the ion tracks traversing the high electric field region are responsible for the catastrophic damage in this type of device.

IV. Physical Failure Mode Analysis and Discussion

Given the lateral structure of the GaN HEMTs on Si substrate used in this study, it is expected that there are unique failure modes never observed in Si and SiC vertical power MOSFETs. Actually, we observed three unique failure modes in the GaN HEMTs. Physical failure analyses were conducted on those failure modes and are discussed in this section.

A. Permanent Leakage current damage

During an irradiation run, an increase in permanent leakage current was observed for ions with LET of 30.6 MeV/(mg/cm^2) and higher at normal incidence as shown in Fig. 2 (a), Fig. 7 (a), and Fig. 11. Fig. 13 shows a Photo Emission Microscopy (PEM) view of the chip surface on the device showing an increase in permanent leakage current. The device was damaged during Xe ion irradiation at V_{DS} = 380 V with V_{GS} = 0 V. The fluence of the ions was set to 1.6×10^5 cm^{-2}. It was clearly confirmed that the damage sites were randomly distributed on the chip surface as expected. For SiC power MOSFETs with a vertical structure, a similar increase in permanent leakage current was also observed, but the source metal on top of the chip surface made this type of direct observation impossible. Figure 14 shows one cross-sectional view of a damaged site taken by a High-Voltage Electron Microscope (HVEM). There is a small line-shaped crystal defect in the Si substrate extending from the buffer layer. To form a leakage current path connecting between active layers and the Si substrate, the buffer layer should also be damaged. Although the damage site in the buffer layer is not clearly observed, the line-shaped defect in Si suggests that it was introduced by current flowing along the ion track. This assumption is supported by the fact that damage sites were never introduced by ions from the direction parallel to the chip surface (i.e. never traversing the buffer layer and penetrating the Si substrate) as shown in Fig. 12.

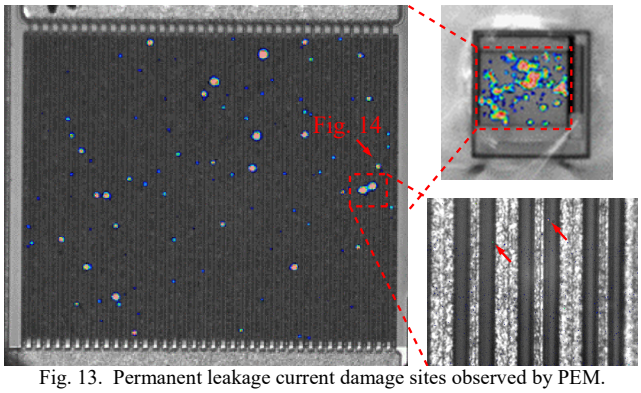

Fig. 13. Permanent leakage current damage sites observed by PEM.

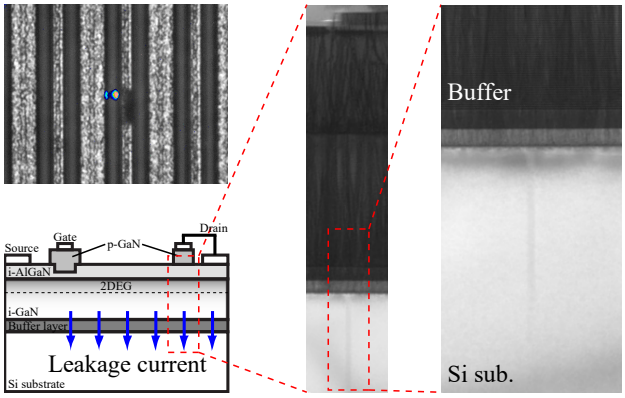

Fig. 14. Cross-sectional view of a leakage current damage site.

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

B. *Catastrophic damage, drain-substrate short mode*

During an irradiation run, this type of catastrophic damage was observed for ions with LET of 30.6 MeV/(mg/cm^2) and higher at normal incidence. There are apparent features for this category of catastrophic damage: (1) No burnout signature on the chip surface and (2) An abrupt decrease in I_{GS} when catastrophic damage occurs, because the drain current begins to flow into the Si substrate and the effective V_{DS} is reduced by the protection resistor, as shown in Fig. 2 (b) and Fig. 11 with 400, 390, 380, and 360 V of V_{DS} cases. Fig. 15 shows a top view taken by an optical microscope and a cross-sectional view of the damaged site taken by a Scanning Electron Microscope (SEM). The device was damaged during Xe ion irradiation at V_{DS} = 380 V as shown in Fig. 2 (a). Apparently the GaN layer, buffer layer, and Si substrate under the drain electrode are severely damaged. To introduce this category of catastrophic damage, apparently ions must traverse these layers. Therefore, ions from the direction parallel to the chip surface are excluded from being a cause of the damage.

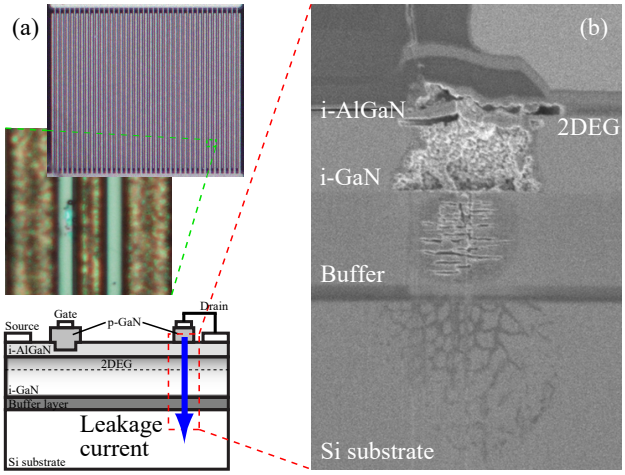

Fig. 15. Damage site for a drain-substrate short mode; (a) top view by optical microscope, (b) SEM image of the cross-sectional damage site.

C. *Catastrophic damage, drain-source short mode*

During an irradiation run, this type of catastrophic damage was observed for ions with LET of 25.4 MeV/(mg/cm^2) and higher at normal incidence. In addition to the normal incidence, the same type of damage was observed with an orientation incidence (i.e. parallel to the chip surface and traversing the source and drain stripe perpendicularly). There are apparent features for this category of catastrophic damage: (1) A burnout signature on the chip surface and (2) I_{GS} staying at the same order of magnitude in most cases when catastrophic damage occurs, because the gate electrode in the burnout region is blown and the remaining portion of the gate continues to work as shown in Fig. 7, Fig. 11 with 340, 320 and 300 V of V_{DS} cases, and Fig. 12. In some cases, I_{GS} abruptly increases as shown in Figs. 9 and 10, because the gate electrode is connected to the drain electrode directly as shown in Fig. 16. Fig. 16 shows a SEM image of a damaged site. The device was damaged during Xe ion irradiation at V_{DS} = 380 V as shown in Fig. 7 (b). A portion of the area bridging the drain and source is blown in addition to thermal damage along the drain electrode. It should be noted that this category of catastrophic damage is also observed during irradiation with a direction normal to the chip surface incidence, in which ion tracks never traverse the drain and source electrodes.

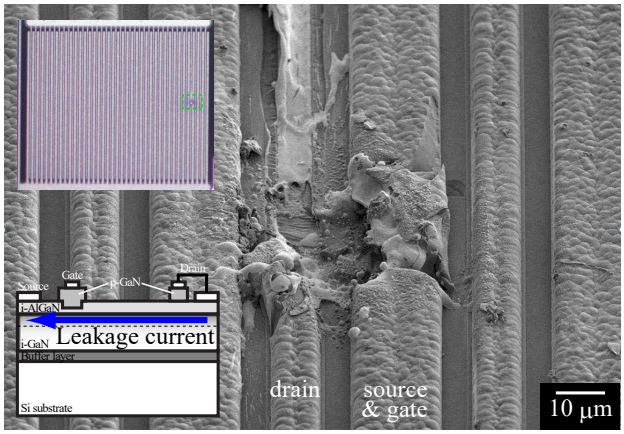

Fig. 16. SEM image of a damage site for a drain-source short mode

V. Conclusions

The single-event damages observed in AlGaN/GaN HEMTs on the Si substrate for power control applications were investigated. In addition to the commonly observed increase in permanent leakage current in the devices made with compound semiconductor materials, two catastrophic failure modes were identified as being attributable to the unique device structure.

Given the increase in permanent leakage current, the distribution of damaged sites on the chip surface was directly observed by a PEM technique for the first time. Its cross-sectional structure with line-shaped crystal damage was also identified. The damage site was introduced by ions with LET of 30.6 MeV/ (mg/cm^2) and higher with normal incidence.

There were two categories of catastrophic damage identified. The first one shows the drain-substrate short mode and no burnout signature on the chip surface. This category of damage was only observed with normal incidence of ions to the chip surface. The other one shows an apparent burnout signature on the chip surface, with a portion of the area bridging the drain and source being blown.

第一种是漏和衬底短路模式这个只在正常的芯片表面入射时观测到，另一种是明显的表面烧毁还有桥连。

It was demonstrated that the damages observed in the GaN HEMTs were introduced by a function of LET, rather than ion species, energy, and range. The worst-case gate bias condition was also demonstrated to be 0 V and less. It was suggested that irradiation with a direction of ions directly traversing between the drain and source regions was possibly the worst case.

损伤主要是let的函数 而不是粒子种类，能量和范围，最差的栅偏压可是0v或者更低。横向入射击直接贯穿源漏的是最差的情况

Acknowledgment

The authors would like to thank Dr. M. Yanagihara of Panasonic Corporation for his helpful discussions. The authors also give thanks to Dr. A. Yoshida and Dr. T. Kambara of RIKEN for their dedicated support with the heavy ion testing. The authors gratefully acknowledge the technical support

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TNS.2018.2819990, IEEE Transactions on Nuclear Science

provided by the members of Ryoei Technica Corporation for the experiments and analysis, and also thank the members of the accelerator operation group at the National Institutes for Quantum and Radiological Science and Technology (QST).

REFERENCES

[1] T. P. Chow and R. Tyagi, "Wide bandgap compound semiconductors for superior high-voltage unipolar power devices," *IEEE Trans. Electron Devices*, vol. 41, no. 8, pp. 1481–1483, Aug. 1994.

[2] W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, and H. Ohashi, "High breakdown voltage AlGaN/GaN power-HEMT design and high current density switching behavior," *IEEE Trans. Electron Devices*, vol. 50, no. 12, pp. 2528–2531, Dec. 2003.

[3] H. J. van Daal, C. A. A. J. Greebe, W. F. Knippenberg, and H. J. Vink, "Investigations on Silicon Carbide," *J. Appl. Phys*., vol. 32, no. 10, pp. 2225-2233, Oct. 1961.

[4] W. E. Nelson, F. A. Halden, and A. Rosengreen, "Growth and Properties of β-SiC Single Crystals," *J. Appl. Phys*., vol. 37, no. 1, pp. 333-336, Jan. 1966.

[5] J. A. Cooper, Jr., M. R. Melloch, R. Single, A. Agarawal, and J. W. Palmour, "Status and Prospects for SiC Power MOSFETs," *IEEE Trans. Electron Devices*, vol. 49, no. 4, pp. 658-664, Apr. 2002.

[6] G. Sonia, F. Brunner,A. Denker, R. Lossy,M.Mai, J. Opitz-Coutureau, G. Pensl, E. Richter, J. Schmidt, U. Zeimer, L. Wang, M. Weyers, J. Würfl, and G. Tränkle, "Proton and heavy ion irradiation effects on AlGaN/GaN HEFT devices," *IEEE Trans. Nucl. Sci*., vol. 53, no. 6, pp. 3661–3666, Dec. 2006.

[7] S. Bazzoli, S. Girard, V. Ferlet-Cavrois, J. Baggio, P. Paillet, and O. Duhamel, "SEE sensitivity of a COTS GaN transistor and silicon MOSFETs," in *Proc. 9th European Conference on Radiation and Its Effects on Components and Systems* (RADECS 2007), 10.1109/RADECS. 2007.5205553.

[8] S. Kuboyama, A. Maru, H. Shindou, N. Ikeda, T. Hirao, H. Abe, and T. Tamura, "Single-Event Damages Caused by Heavy Ions Observed in AlGaN/GaN HEMTs," *IEEE Trans. Nucl. Sci*., vol. 58, no. 6, pp. 2734–2738, Dec. 2011.

[9] S. Onoda, A. Hasuike, Y. Nabeshima, H. Sasaki, K. Yajima, S.-i. Sato, and T. Ohshima, "Enhanced Charge Collection by Single Ion Strike in AlGaN/GaN HEMTs," *IEEE Trans. Nucl. Sci*., vol. 60, no. 6, pp. 4446–4450, Dec. 2013.

[10] B. D. Olson, J. D. Ingalls, C. H. Rice, C. C. Hedge, P. L. Cole, A. R. Duncan, and S. E. Armstrong, "Leakage Current Degradation of Gallium Nitride Transistors Due to Heavy Ion Tests," in *Proc. Radiation Effects Data Workshop*, Boston, MA, pp. 120-129, July 13-17, 2015.

[11] L. Scheick, "Determination of Single-Event Effect Application Requirements for Enhancement Mode Gallium Nitride HEMTs for Use in Power Distribution Circuits," *IEEE Trans. Nucl. Sci*., vol. 61, no. 6, pp. 2881–2888, Dec. 2014.

[12] Y. Uemoto, M. Hikita, H. Ueno, H. Matsuo, H. Ishida, M. Yanagihara, and T. Ueda, "Gate Injection Transistor (GIT)—A Normally-Off AlGaN/GaN Power Transistor Using Conductivity Modulation," *IEEE Trans. Electron Devices*, vol. 54, no. 12, pp. 3393–3399, Dec. 2007.

[13] S. Kaneko, M. Kuroda, M. Yanagihara, A. Ikoshi, H. Okita, T. Morita, K.Tanaka, M. Hikita, Y. Uemoto, S. Takahashi, and T. Ueda, "Current-collapse-free Operations up to 850V by GaN-GIT utilizing Hole Injection from Drain," in *Proc. 27th Int. Symp. on Power Semicond. Devices & IC's*, pp. 41-44, 2015.

0018-9499 (c) 2018 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission. See http://www.ieee.org/publications_standards/publications/rights/index.html for more information.