50.002 COMPUTATIONAL STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

The CMOS Technology

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1 The Ideal Combinational Device

We would want our device to be:

1. Can tolerate some amount of errors, using Noise Margins : VTC gain > 1 and nonlinear gain
2. If we have **lots of gain**, that means we have **more noise margin**
3. Cheap, small
4. We want **zero power dissipation** when voltages aren't changing
5. Otherwise when voltage is changing from, '0' to '1' or '1' to '0' then power has to dissipate
6. Our device has to be functional, meaning that it conforms to the **truth table** at all times

2 The MOSFET

Metal-oxide semiconductor field effect transistors (MOSFET, or shortened as FETs): to implement the functionality of our combinational device (see figure below).
Things to note about FETs:

1. Used to 'switch' 1s to 0s and vice versa, so that we can implement functionalities (truth table or logics)
2. The current flow between source and drain I_{DS} is proportional to W/L (the width and the length) of the FET.
3. Source and drain is physically symmetrical, we name them depending on the type of the MOSFET (see section 4).

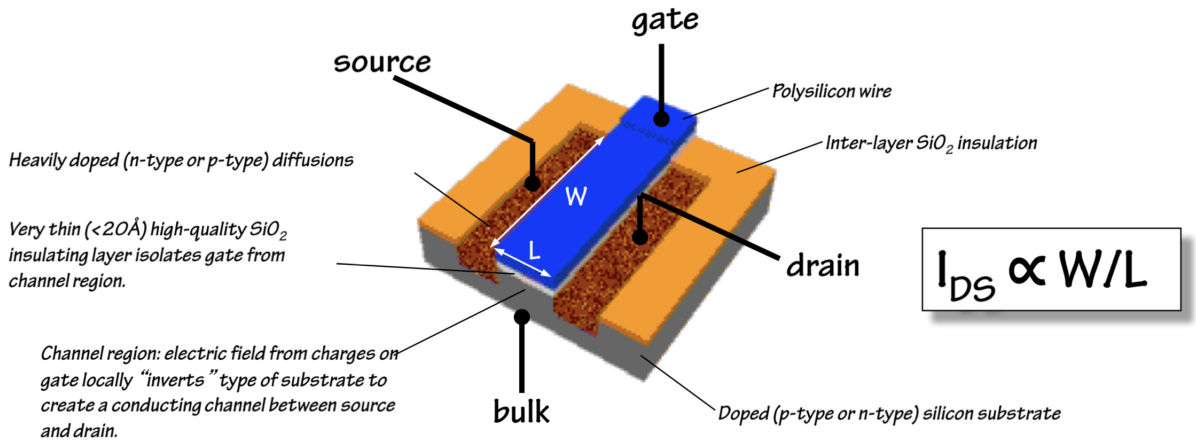

Figure 1

4. Current flows from higher potential (+) to lower potential (-)
5. Electron flows from lower potential (-) to higher potential (+)

3 Types of MOSFETs

There are two types of FETs: the **NFET** and the **PFET**.

1. The NFET : the majority of the charge carrier for the bulk are holes (p-type semiconductor). The majority of the charge carrier for the source and drain are electrons (n-type semiconductor). Typically, the bulk is connected to GND to keep the pn junction *reverse biased*
2. The PFET :the majority of the charge carrier for the bulk are electrons (n-type semiconductor). The majority of the charge carrier for the source and drain are holes (p-type semiconductor). Typically, the bulk is connected to VDD to keep the pn junction *reverse biased*

Some terms you need to know:

1. VDD : voltage source, V_{TH}: threshold voltage.
2. GND : ground

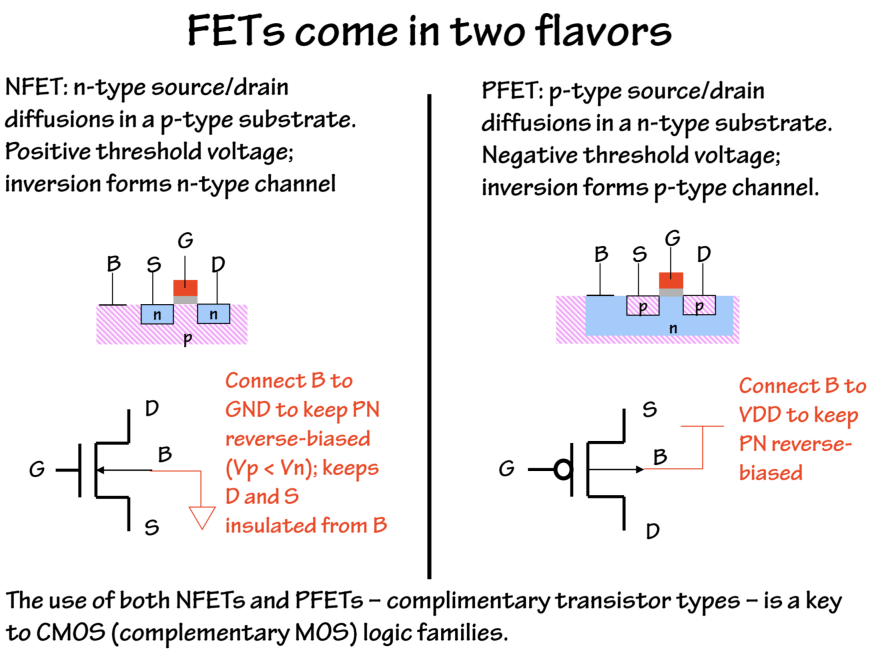

Figure 2

3. Reverse-biased: a state whereby D is insulated from S, where current cannot flow from D to S **in the presence of applied voltage**.

4. A FET that is ”ON” means that there’s connection between D and S, current can flow through them.

5. A FET that is ”OFF” means that there’s no connection between D and S, current cannot flow through them.

The circuit symbol for NFET and PFET are shown as below,

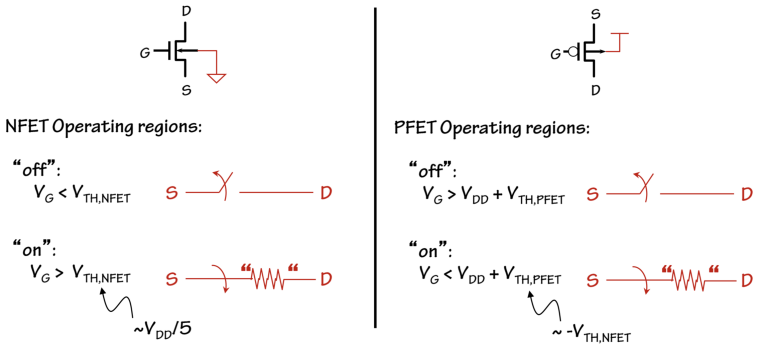

Figure 3

How NFET operates:

1. Indicated by the FET with **no** bubble: ∘
2. It is ”ON” when V_{gs} is **high**
3. Bulk is connected to GND to keep the pn junction reverse biased, meaning that no current flows or leaks between source and bulk and between drain and bulk.
4. When it is ”ON” then current can pass from D to S through Bulk
5. S (and also bulk) is connected to GND for NFET. Current from D is therefore drained to GND at S.
6. The output of an NFET is at the D terminal.
7. Hence, the output of an ”ON” n-type is ’0’
8. It is ”OFF” when V_{gs} is **low**, as it encourages depletion region to form further.

How PFET operates:

1. Indicated by the FET with the bubble ∘
2. It is ”ON” when V_{gs} is **low**
3. Bulk is connected to VDD, meaning that no current flows or leaks between source and bulk and between drain and bulk.
4. When it is ”ON” then current can pass from S to D through Bulk
5. S (and also bulk) is connected to VDD for PFET. Current can flow from S to D.
6. The output of an PFET is also at the D terminal.
7. Hence, the output of an ”ON” n-type is ’1’
8. It is ”OFF” when V_{gs} is **high**, as it encourages depletion region to form further.

See the figure below to understand better how NFET and PFET operates

4 P-type and N-type Semiconductors

Not to be confused with PFET and NFET.

In the **p-type** semiconductor there are plenty of **acceptor atoms** and in the **n-type** semiconductor there are plenty of **extra electrons (donor atoms)**. We can say that a p-type region is where the majority of the carriers are holes and an n-type region is where the majority of the carriers are electrons. To be precise, an electron is one

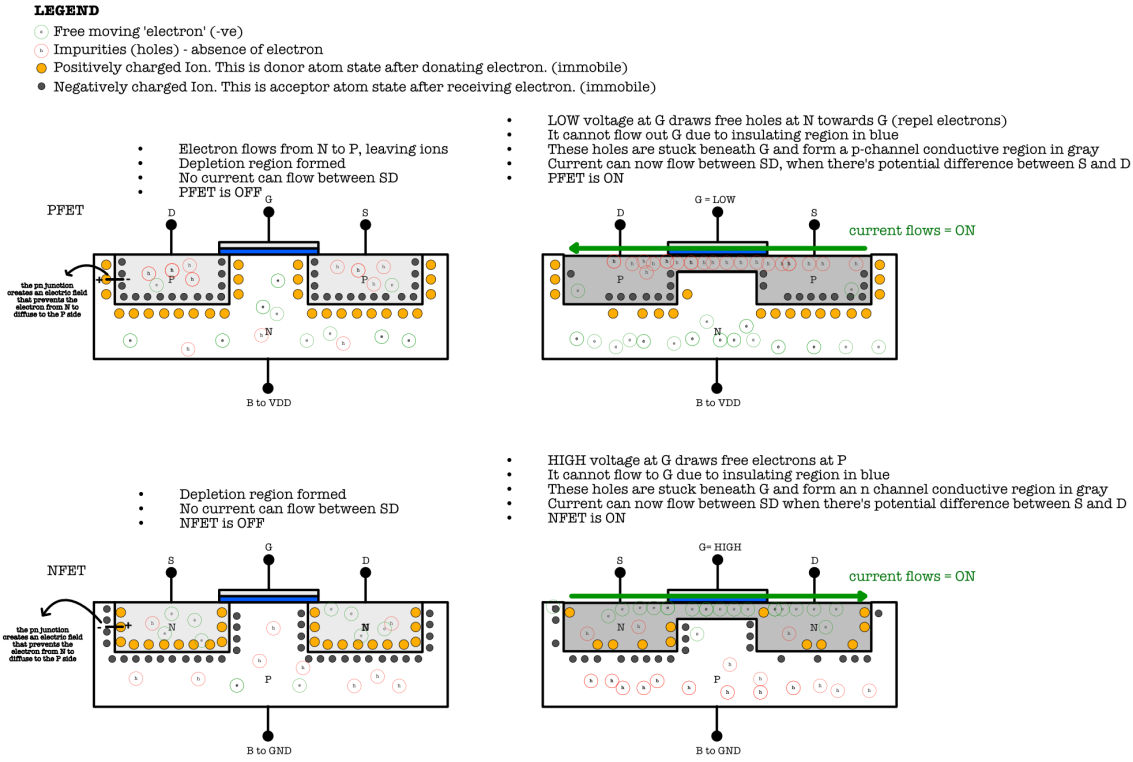

Figure 4

of the constituents of an atom, having a negative charge. An acceptor atom has for example 3 electrons in valence shell and can accept one electron to complete the covalent bonding. Thus it gains one extra electron and acquires negative charge. On the other hand, a donor atom has 5 electrons (one extra) in valence shell and can donate one extra electron. It thus acquires unit positive charge in the process.

5 Depletion Region

When p-type and n-type semiconductors are placed together, the free electrons from n-type will flow over (diffuse) to the p-type and fill its holes (impurities). Filling up a hole results in a negatively charged ion at the p-type semiconductor, as illustrated as the gray circles in Figure 4. Equally, these free electrons leaving the n-type leaves behind a positively charged ion at the n-type semiconductor. This is illustrated as yellow circles in Figure 4.

Eventually, a space-charge builds up forming an electric field as denoted in the left drawings in Figure 4 (the yellow circles and the grey circles form electric field), preventing more free electrons from the n-type side to the p-type side, thereby forming an insulating layer called *depletion region*.

6 P-channel or N-channel Formation

For NFETs, when there's presence of high (positive) voltage at the gate, it repels the extra holes at the p-type bulk. Basically, a positive voltage applied to the gate attracts electrons (which are minority in the p-type substrate) to the interface between the gate dielectric and the two n-types semiconductors (drain and source). These electrons form a conducting channel between the source and the drain, called the *inversion layer*. When there's potential difference between the drain and the source, the current will flow from source to drain through this inversion layer.

For PFETs the opposite happens. When there's presence of low (negative) voltage at the gate, it repels the extra electrons at the n-type bulk. Basically, holes (which are minority in the n-type substrate) are left behind at the interface between the gate dielectric and the two p-types semiconductors. When there's potential difference between drain and source, then the current will flow from source to drain through this inversion layer. Note that the position of the source and drain in PFET is switched as what is depicted for NFET. Read the next section for details.

7 Naming of Source and Drain

The naming of the Source terminal depends on the majority of the charge carrier. In PFETs, current flows from Source to Drain, because the majority of the charge carrier is holes (positively charged). In nFETS, current flows from Drain to Source, because the majority of the charge carrier is electrons (negatively charged).

Note: Current (I) cannot flow out back to the Gate because there's a capacitor there (infinite resistance). The function of the gate capacitor is to create electric field enough to pull either electrons up to the gate in NFETS or holes up to gate in PFETs to create a conductive n-type (electrons) or p-type(holes) channel.

8 The Pull-up and Pull-down Circuit in CMOS

These PFETS and NFETS can be connected together to form a CMOS : Complementary Metal-Oxide Semiconductor. There are two parts of CMOS: **the pull-up circuit** and **the pull-down circuit**, see figure below:
Contents of the pull-up circuit:

1. All FETs in the pull-up circuit are PFETS
2. So all of their bulks are connected to the VDD
3. It is called 'pull-up' because when there is open connection to the VDD (from any path through VDD to output) then the output of the overall CMOS circuit is 1

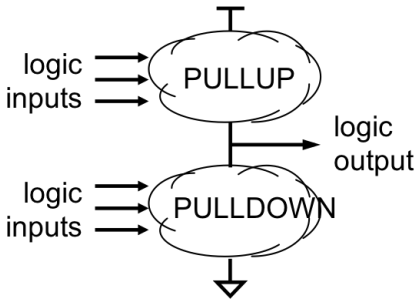

Figure 5

Contents of the pull-down circuit:

1. All FETs in the pull-down circuit are NFETS
2. So all of their bulks are connected to GND
3. It is called 'pull-down' because when there is open connection to the GND (from any path through the PD circuit) then the output of the overall CMOS circuit is 0

9 The CMOS Complements

Imagine if pull-up and pull-down is bot "ON". This means that VDD has a straight open connection to GND : resulting in short-circuit. Hence, **it is very important for a CMOS circuit to contain complementary pull-ups and pull-downs**.
The CMOS complements is summarized as below:
An example below explains the CMOS complement more clearly. Explanation: (make sure you know how these works)

1. From the diagram, A is connected to the PFET on the **left** and the NFET on the **top**
2. B is connected to the PFET on the **right** and the NFET on the **bottom**

Case 1:

1. Lets see what happens when A = 1 and B = 1.
2. When A = 1, the PFET on the **left** is "OFF", the NFET on the **top** is "ON"
3. When B = 1, the PFET on the **right** is "OFF" and the NFET on the **bottom** is "ON"
4. Current from VDD **cannot** flow to the output through any of the left and the right PFET
5. Current at the output **is drained down to the GND** through either NFET on the top or NFET on the bottom.

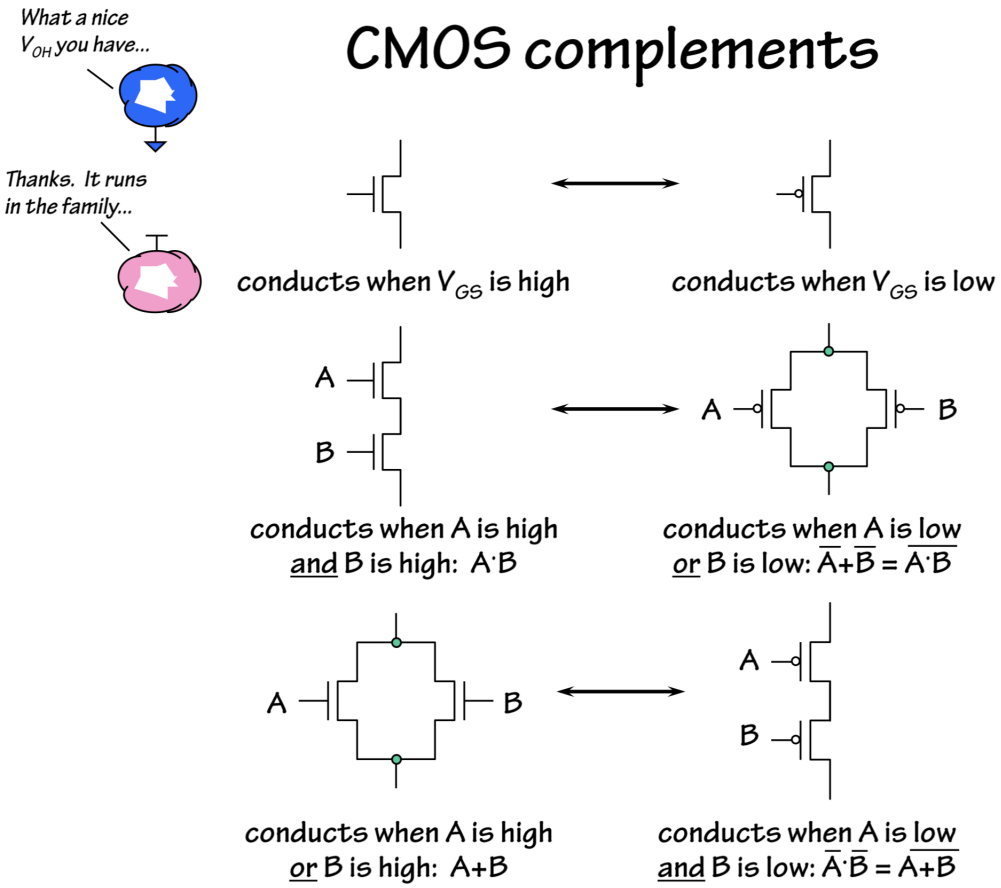

Figure 6

6. Hence the output is 0 when A = 1 and B = 1

Case 2:

1. Another case, when A = 0, and B = 1,
2. When A = 0, the PFET on the **left** is ”ON”, the NFET on the **top** is ”OFF”
3. When B = 1, the PFET on the **right** is ”OFF” and the NFET on the bottom is ”ON”. This draws current from B = 1 and pull it down to 0.
4. Current from VDD can still flow from the PFET on the **left** to the output
5. Hence the output is 1 when A = 0 and B = 1

Notice how there’s parallel PFET in the pull-up, and series NFET in the pull-down: **they are the CMOS complement**.

10 The Combinational Logic Propagation Delay t_{pd}

t_{pd} is the time delay from **valid** input to **valid** output. The effective t_{pd} of an entire circuit is the **maximum** cumulative propagation delay over all paths from inputs to

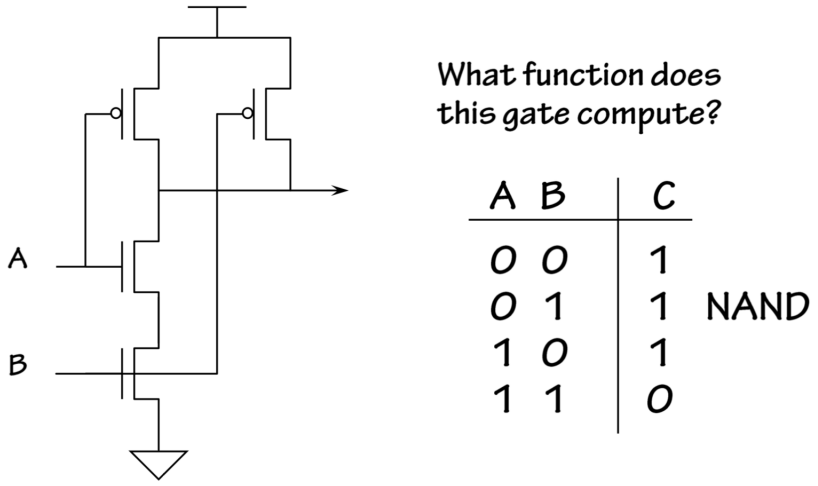

Figure 7

outputs **in the combinational logic circuit**. This works only in **acyclic circuits**.

Why is t_{pd} the maximum cumulative propagation delay over all paths:

1. Each component (gates, made up of FETS in CMOS arrangements) in the combinational logic circuit must wait for one another
2. All components have to produce valid results before the OUTPUT can produce a valid result

11 The Combinational Logic Contamination delay t_{cd}

t_{cd} is the time delay from **invalid** input to **invalid** output. The effective t_{cd} of an entire circuit is the **minimum** cumulative contamination delay over all paths from inputs to outputs **in the combinational logic circuit**. This works only in **acyclic circuits**.

Why is t_{cd} the minimum cumulative propagation delay over all paths:

1. To propagate *invalid* signal and finally produce it at the output, it only takes one component to relay that invalid signal (basically illegal voltage value, neither digital 0 nor 1) from input to output

12 Timing Example

Complementary pull-up (made up of PFETs) and pull-down circuits (made up of n-FETs) form a CMOS gate. t_{pd} and t_{cd} are specified per gates. Consider the example below on how to calculate these timings,

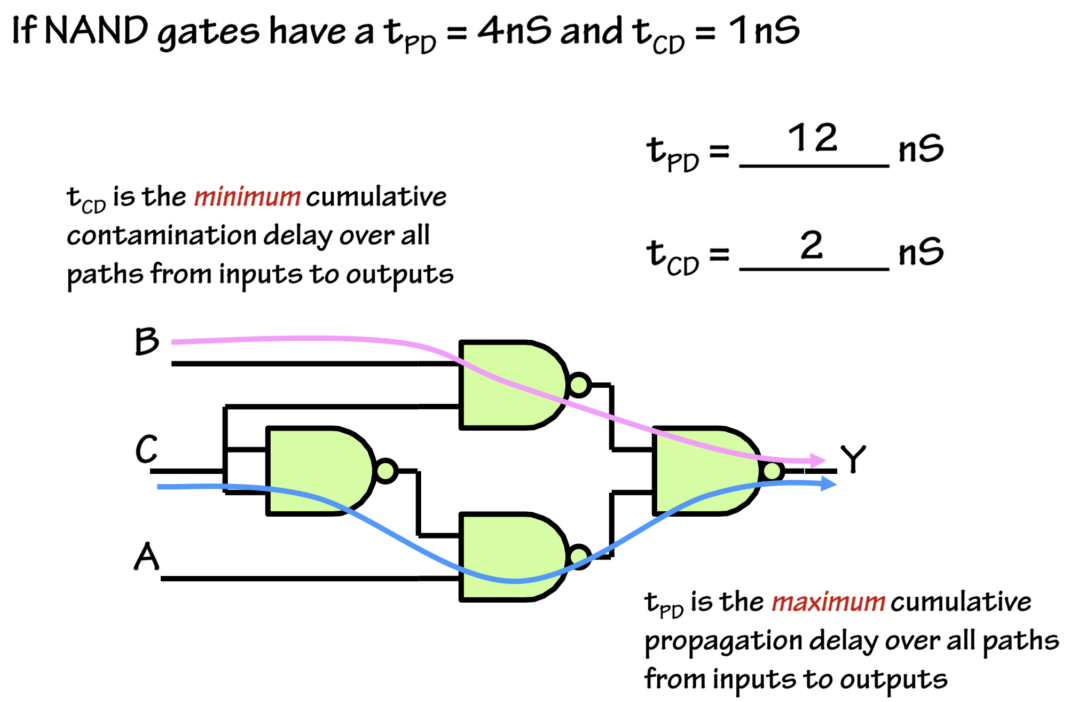

Figure 8