

50.002 COMPUTATIONAL STRUCTURES

INFORMATION SYSTEMS TECHNOLOGY AND DESIGN

Sequential Logic & Synchronisation

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1 Sequential Logic

Look at the diagram below.

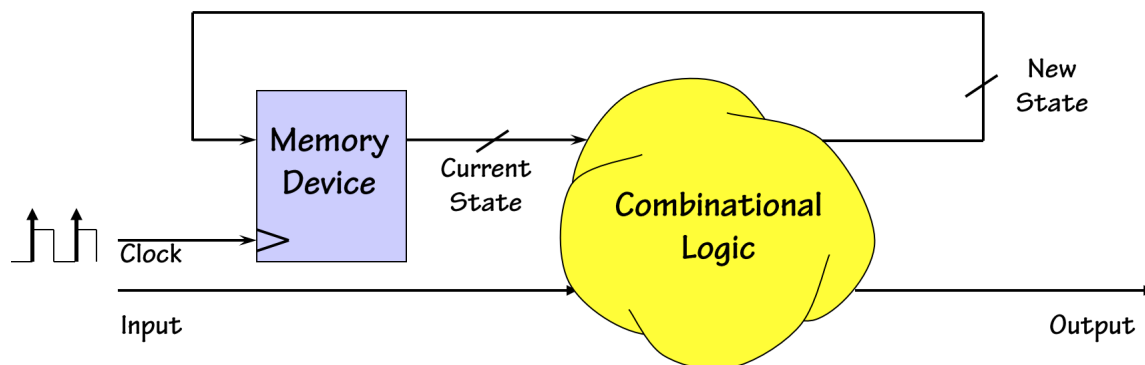


Figure 1

So far we have learned **combinational device** (also called combinational logic), that implements your truth table functional specs. But it isn't enough to make a complete computer that we know today. We are missing the **storage (memory) device**.

2 Storage Device: D-Latch

A D-latch is a mux with a feedback loop,

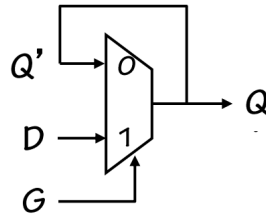


Figure 2

How it works:

1. G is clock signal. It will periodically switch between '1's and '0's
2. If G is 1, then the input signal on wire D will be passed to output wire Q, independent of the signal on wire Q'. Lets call this the **write mode**.
3. If G is 0, then output signal on wire Q follows the signal on wire Q', independent of input wire D. Lets call this the **read memory mode**.

Possible problems:

1. **Storing invalid information:** If G changes from 1 to 0 at the exact moment when D is changing (invalid), then we will end up storing that new invalid information on wire D.
2. **Unstable Output because of unstable input:** In practice, input from users can be highly unstable. We do not want it to affect our devices. If G is 1, then it will pass **all** input from D to the output wire Q, regardless on whether it is a valid or stable input or not.

We address these problems in the next two sections.

3 The Dynamic Discipline

The dynamic discipline addresses problem 1 above: **storing invalid information**. It is **very important to never violate the dynamic discipline to ensure any sequential logic circuits to work properly**.

Take a look at the clock signal below for G, it basically changes between 0 to 1 periodically:



Figure 3

The dynamic discipline states that:

1. $T_{setup} = 2t_{pd}$
2. $T_{hold} = t_{pd}$

where,

1. T_{setup} = the minimum amount of time that the voltage on wire D needs to be stable **before** the **clock edge changes from 1 to 0**.
2. T_{hold} = the minimum amount of time that the voltage on wire D needs to be stable **after** the **clock edge changes from 1 to 0**.
3. t_{pd} is the propagation delay of the D-latch ¹.

4 Edge-Triggered Flip-Flop

To address the second problem of **Unstable Output because of unstable input**, we put two D-Latches in series to make another device called the **Flip Flop**,

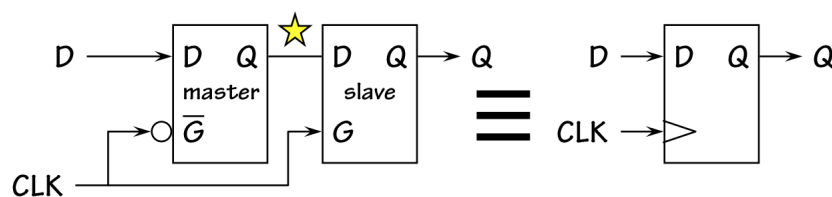


Figure 4

Things to note:

1. There is an inverter on the G input on the master flip flop
2. The diagram on the right is how flip-flop is drawn in books or on paper to save space

How it works:

1. The user gets output only from the output wire of the **slave** Q wire, and the user supplies input only to the **master** D wire.
2. Remember CLK periodically changes from 0 to 1 and vice versa
3. When CLK signal is 0, the G wire of **master** latch will receive a 1 (due to the inverter) and the G wire of **slave** flip flop will receive a 0.

¹Recall that D-latch is made of mux consisted of NAND gates, so the this t_{pd} is the propagation delay of that mux - a combinational circuit

4. This means that the **master** latch is in "write mode", i.e: it lets signal from its D wire through to its Q wire, while the **slave** latch is in "read memory mode", i.e: slave's output depends on *its own* memory wire Q' and not affected by input on wire ★.
5. When CLK signal is 1, the G wire of **master** latch will receive a 0 due to the inverter and the G wire of **slave** latch will receive a 1.
6. This means that the **master** latch is in "read memory mode", i.e: master's output depends on *its own* memory wire Q' and not affected by input on wire D. Meanwhile, the **slave** latch is on "write mode", i.e: it lets signal from the ★ wire to be passed through its slave output.
7. Hence, **Only one of the two D-Latches is on "write mode" at a time** or equivalently, only one D-latch is on "memory-mode" at a time.

The explanation above is illustrated in terms of waveforms below:

Flip Flop Waveforms

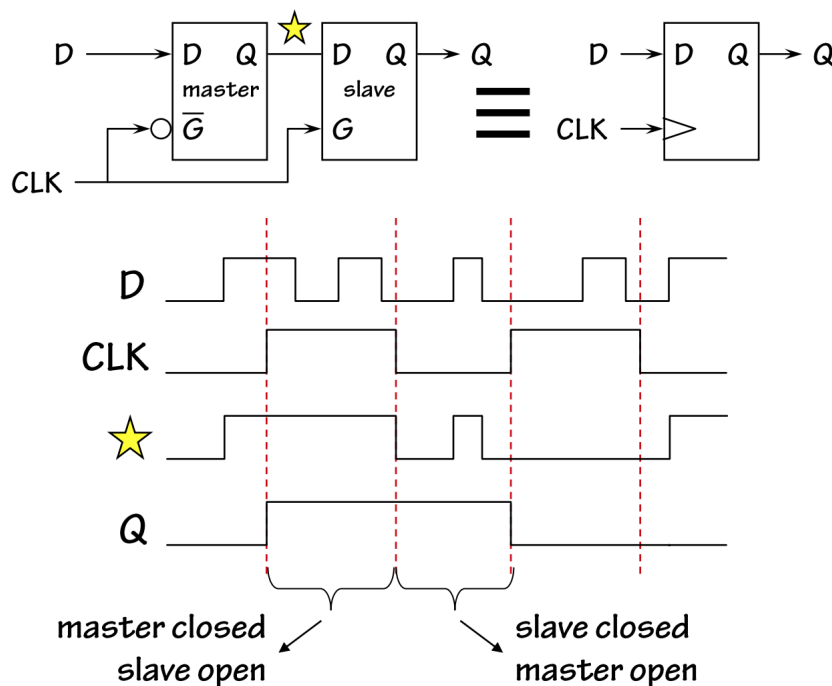


Figure 5

The name "edge-triggered" comes from the fact that the output wire Q from the slave *changes* only when the CLK rises from 0 to 1.

5 t_{pd} and t_{cd} of Sequential Logic vs Combinational Logic

In the previous lessons, we learn about t_{CD} and t_{PD} for **combinational device**. For **sequential device**, i.e: circuits with CLK in it, these timings means:

1. t_{CD} of a Register (or sequential logic unit with registers and CLs in it) is the time taken for **invalid** CLK input (**not input to the sequential logic circuit**) to produce an **invalid** output on wire D (or the final output of the sequential logic unit)
2. t_{PD} of a Register (or sequential logic unit with registers and CLs in it) is the time taken for **valid** CLK input (**again, not input to the sequential logic circuit**) to produce a **valid** output on wire D (or the final output of the sequential logic unit)

Note the **subtle difference** between the t_{PD} and t_{CD} of a combinational vs a sequential device. In combinational device, there is no CLK involved, so t_{PD} of a combinational device is the time taken for a valid input to the circuit to produce a valid output of the circuit, and its t_{CD} is the time taken for an invalid input to the circuit to produce an invalid output of the circuit.

6 Flip-Flop Timing Constraint

For a single D-latch, we have the dynamic discipline to ensure that we do not end up storing invalid input signals. **Now that we cascade two D-latches to make a Flip-Flop, the dynamic discipline is translated into this timing constraint for Flip-Flop:**

$$t_{CD_{master}} > t_{hold_{slave}}$$

Explanation:

1. When signal at G in master changes from 1 to 0, and signal at G in slave changes from 0 to 1, master goes into read memory mode and slave goes into write mode.
2. Again, these CLK signals do not magically transform from 0 to 1 or 1 to 0. It has to **gradually** change to high voltage '1' or to low voltage '0', and it will cross the invalid region (the region which voltage value doesn't translate to either digital 1 or 0).
3. Then ★ cannot change too quickly while G is transitioning, otherwise it will not meet the **hold time**² of the slave latch.
4. This means the contamination delay of the master latch³ has to meet the hold time of the slave latch.

²Recall: time for ★, input to the slave latch, to be stable after the clock rise edge - i.e: clock changes from 0 to 1

³Time taken on signal on ★ to be invalid after G becomes invalid

7 Sequential Logic Timing Constraint

We can now use Flip-Flop in our system as a 'memory' device that's cascaded before and after any combinational logic circuit. Due to dynamic discipline, we have two timing constraints called t_1 and t_2 :

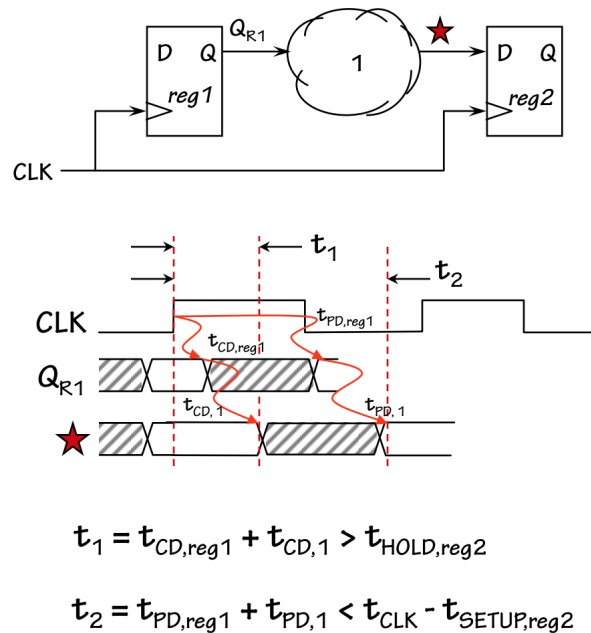


Figure 6

Note: The '1' in the picture above means any combinational logic unit, **and it is unrelated with the '1' in t_1** . The two boxes reg_1 and reg_2 are **both flip flops**, each made up of 2 D-latch. t_{CLK} means the clock period.

Explanation:

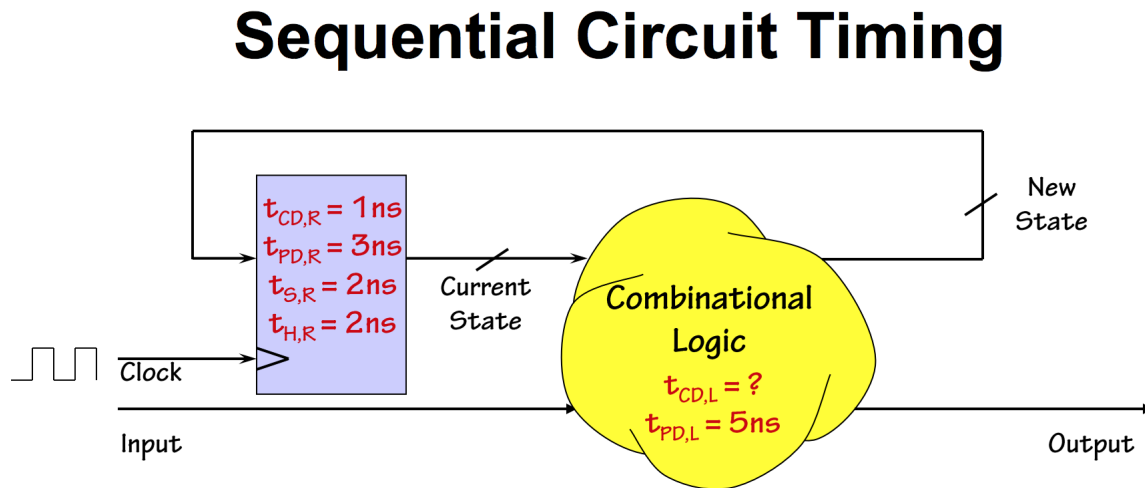
1. For t_1 , it is basically saying that an "invalid" CLK signal that propagates from the input to R1 through combinational logic 1 should not arrive 'too soon' at R2 because R2 requires the signal \star for as long as t_{hold} in order to latch into the valid values during write mode.
2. For t_2 , it ensures that the things that has to be done between two clock edges are the propagation delay of R1, the propagation delay of the combinational logic CL1, and the setup time for R2 in order to go to write mode and store the value value properly.

Look at t_2 constraint. The time taken to do *actual work* at the combinational logic unit '1' is therefore,

$$t_{work_1} = t_{PD_1} = t_{CLK} - t_{setup_{R2}} - t_{pd_{R1}}$$

8 Timing Example

Below is one sequential timing example:



Questions:

- Constraints on T_{CD} for the logic? $> 1\text{ ns}$
- Minimum clock period? $> 10\text{ ns } (T_{PD,R} + T_{PD,L} + T_{S,R})$
- Setup, Hold times for Inputs? $T_S = T_{PD,L} + T_{S,R}$
 $T_H = T_{H,R} - T_{CD,L}$

Figure 7

Explanation:

1. According to t_1 in the previous section, the contamination delay of the combinational logic CL and the contamination delay of register R1 has to be larger than the hold time of the register R2.
2. Here, $R1 = R2$ because of the feedback path, hence the contamination delay of CL is at least $t_{H,R} - t_{CD,R} = 2 - 1 = 1$.
3. **Note that symbols T_S and T_H in flip-flop timings like this simply means the setup and hold time required for the input at the input wire to be stable**
4. Refer to the extra notes on sequential logic timing for more examples on sequential circuit timing

9 Synchronization

In sequential logic, we use a **single synchronous clock**, meaning that we use one same clock to any flip-flop in the computer. Recall that dynamic discipline is crucial for any sequential logic to work properly. We are now going to address two problems of synchronisation that can violate dynamic discipline:

1. There's dynamic discipline that make sure that the input D has to meet the setup and hold time of the latches. But in real world, user does not always supply input that is synchronous with the clock edge. This carries the risk of violating dynamic discipline and may end up storing the invalid values in read memory mode. This event of storing invalid value is called the **metastable state**, as shown in the figure below,

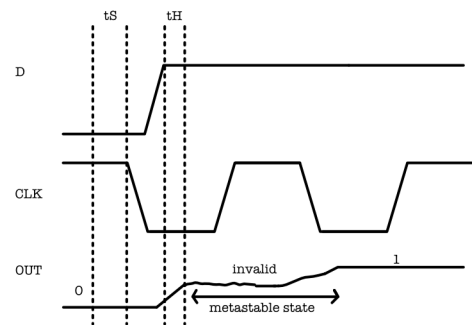


Figure 8

2. Clock skew: The clock does not arrive at all registers at the same time and skew is the difference between two clock edges. This may also potentially violate dynamic discipline.

The next two sections address these problems.

10 The Metastable State

The D-latch device has a unique property where there exist a point whereby $V_{in} = V_{out}$. Take a look at the diagram in the figure below.

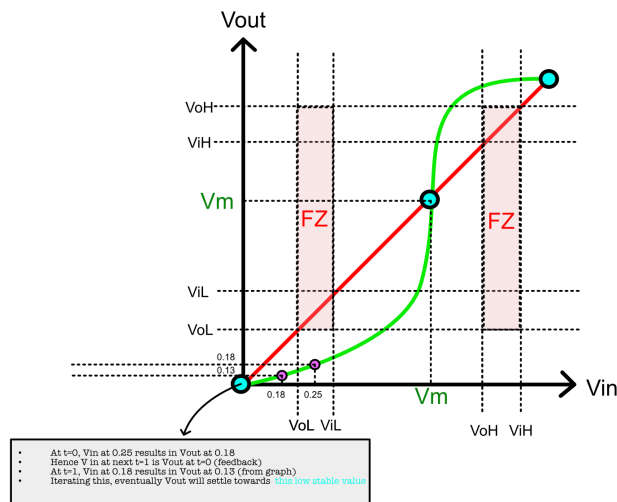


Figure 9

The red line signifies the feedback constraint, where **should** we have Q at V_{out} equivalent to Q' as V_{in} . **This is the effect of connecting the output of the mux to itself.** The green line signifies the VTC of a "closed latch" state. Notice that in the close latch state, the D-latch passes the value at Q' as the output at Q , thus we have a shape that resembles that of a buffer. There are three solutions between the feedback constraint and the VTC of the closed latch, as indicated by the three circles in the figure: two end points that are stable, and one middle point that's metastable (denoted as V_m).

Why are we looking for this **solution**? Well, we are indeed creating a device which output is connected back as its input, so we need to know where the system will *tend towards* if let's say we have a small change in V_{in} due to noise. In the figure above, if we have an input value below V_m , then it will tend towards the stable low indicated by the teal circle on the left. The note at the figure above illustrates just that. Otherwise, if it is above V_m , then it will tend towards the stable high indicated by the teal circle on the right. However, if we have $V_{in} = V_m$, then the output will be again at V_m . This output will be an input back at V_m , and without the presence of noise, if V_{in} is exactly at V_m then there's a chance that we could wait forever for it to come to a stable value (basically the result never settles). A small presence of noise will drive V_{in} down or up and eventually it will settle to a stable value, however this is **not guaranteed in bounded time**.

The properties of metastable state are illustrated below: And in summary, the rea-

Metastable State: Properties

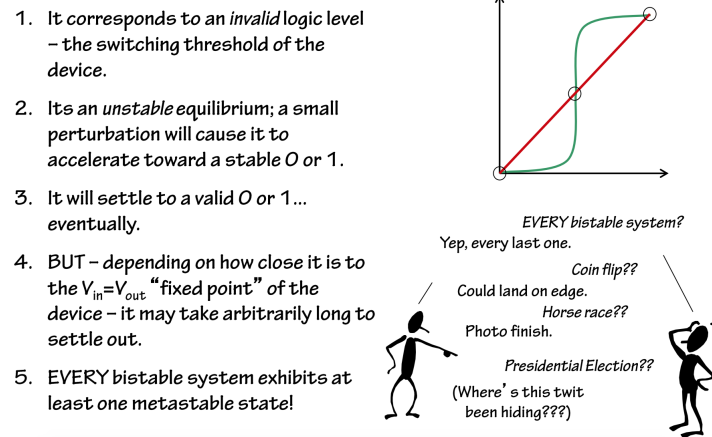


Figure 10

son behind metastable state is:

The Metastable State:

Why is it an inevitable risk of synchronization?

- Our active devices always have a fixed-point voltage, V_M , such that $V_{in}=V_M$ implies $V_{out}=V_M$
- Violation of dynamic discipline puts our feedback loop at some voltage V_O near V_M
- The rate at which V progresses toward a stable “0” or “1” value is proportional to $(V - V_M)$
- The time to settle to a stable value depends on $(V_O - V_M)$; its theoretically infinite for $V_O = V_M$
- Since there's no lower bound on $(V_O - V_M)$, there's no upper bound on the settling time.
- Noise, uncertainty complicate analysis (but don't help).

Figure 11

In other words, we cannot completely avoid the metastable state. The metastable state *might* eventually settle to a valid zero, or a valid one, but in unbounded time. The only thing we can do is to *minimize its probability*. We can do that by introducing more **delays** between input and output in the hopes that the signal will somehow resolve itself before reaching the output, like illustrated here,

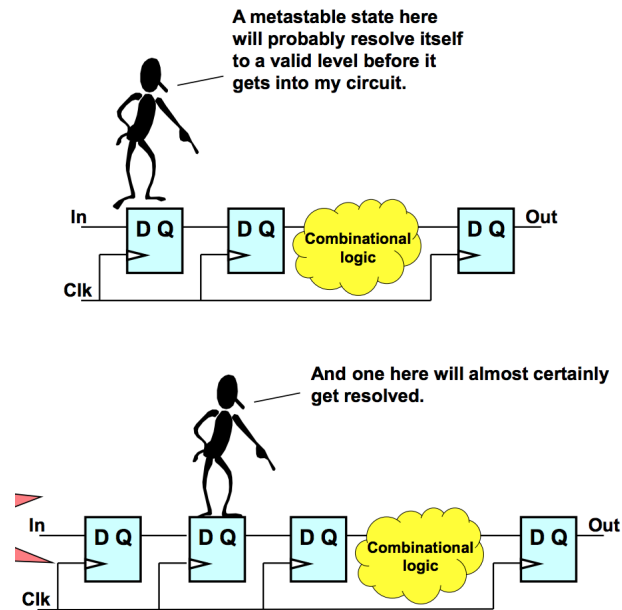


Figure 12

11 Clock Skew

To fix clock skew, we need to know t_{skew} , which is the maximum difference in clock signal arrival times across all flip-flops in the computer. We just need to adjust the two rules t_1 and t_2 for flip flops into,

$$t_1 = t_{CD,Reg1} + t_{CD,CL1} > t_{hold,Reg2} + t_{skew} \quad (1)$$

$$t_2 = t_{PD,Reg1} + t_{PD,CL1} + t_{SETUP,Reg2} < t_{CLK} + t_{skew} \quad (2)$$