

**Batch: A-4 Roll No.: 16010422211 Experiment No.: 6**

**Aim:** Implementation of a 3-bit synchronous up counter using JK flip flops

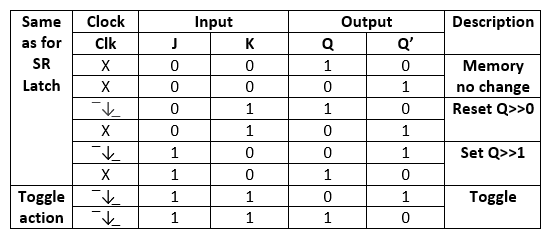
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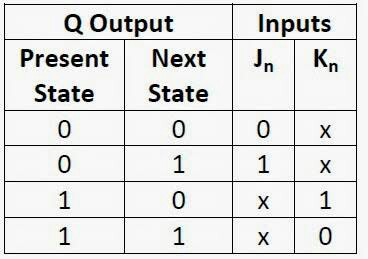
**Resources needed:** Simulation Software, (Circuitverse)

**Theory:**

We prefer to use edge-triggered JK flip-flops to design counters as they are more versatile than the other flip-flops; they have all the advantages of the other FFs and none of their disadvantages.

To design a 3 bit up counter we first need to refer to the characteristic table and the excitation table of the JK flip flop, which are given below:

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| Synchronous counters are designed in such a way that the clock pulses are applied to the CP inputs of all the flip-flops. The common pulse triggers all the flip-flops simultaneously, rather than one at a time in succesion.  In the 3-bit synchronous counter, we have used three j-k flip-flops. As in the diagram, The J and K inputs of FF0 are connected to HIGH. The inputs J and K of FF1 are connected to the output of FF0, and the J and K inputs of FF2 are connected to the output of an AND gate, which is fed by the outputs of FF0 and FF1. https://www.iitg.ac.in/cseweb/vlab/Digital-System-Lab/images/ckt_el/3bit.png |
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Binary state sequence

| **FF2** | **FF1** | **FF0** |
| --- | --- | --- |
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |
| 1 | 1 | 1 |

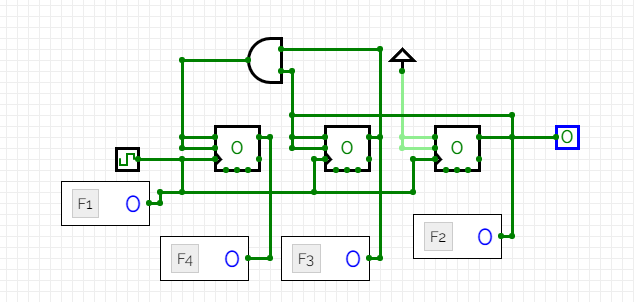
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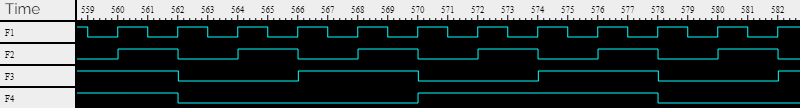
**Procedure**:

1. Create the above circuit diagram in the CircuitVerse simulator.
2. Connect flags to monitor the waveforms of all FF outputs.
3. Choose a suitable clock speed to get a steady waveform.
4. Write a testbench and attach it to the circuit.
5. Download the circuit image, the output waveform and export the testbench file. Copy-paste these into the writeup document.
6. Complete the writeup and upload.

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**Observations:** Generate the timing diagrams (waveforms) and download a snapshot to verify the output.

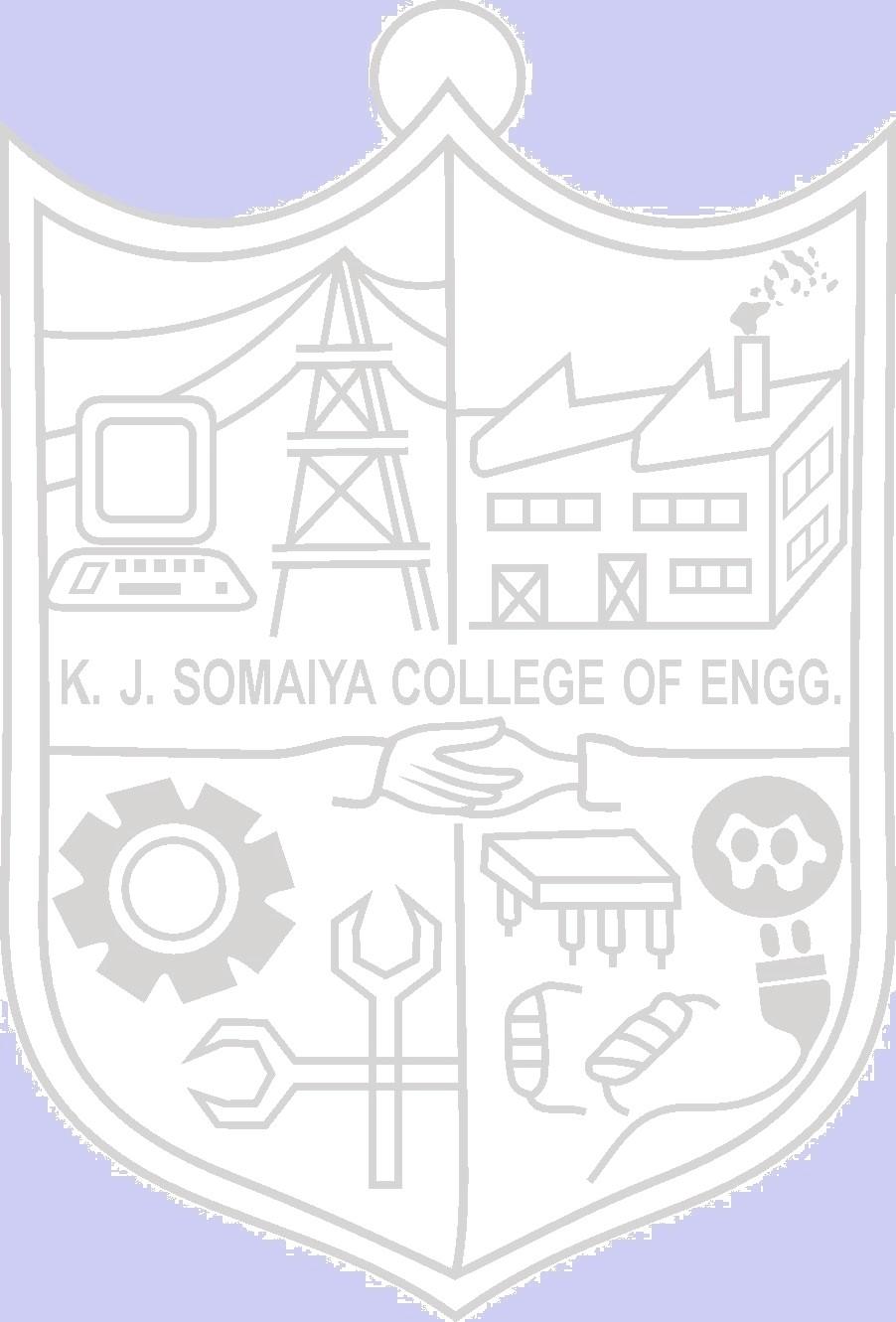


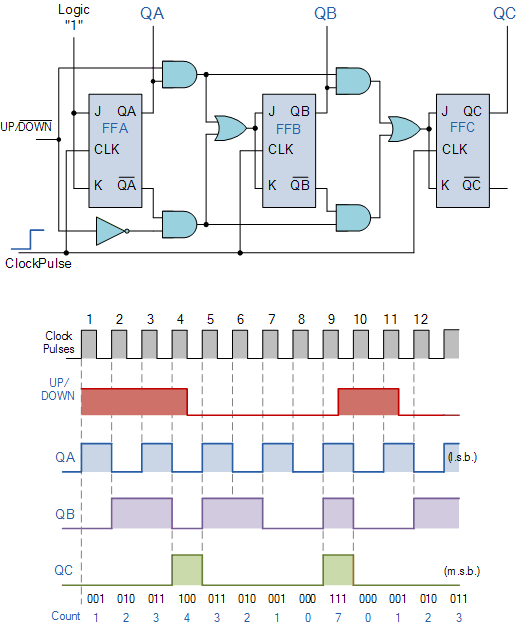


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# Post Lab:

Q1. Analyse the following 3 bit synchronous Up/Down Counter

Schematic diagram and timing diagram with Assumption M=1 for Up count and M=0 for Down count write the working of the same.



1. Initialization: The counter begins in a specific state

2. Up Count (M=1):

- When M=1, the counter counts up.

- On each rising edge of the clock signal, the flip-flops are triggered.

- The logic gates associated with each flip-flop determine whether it should increment the

count based on the current state and M=1.

3. Down Count (M=0):

- When M=0, the counter counts down.

- Similar to Up count, on each rising edge of the clock signal, the flip-flops are triggered.

- The logic gates associated with each flip-flop determine whether it should decrement the

count based on the current state and M=0.

4. State Transitions: The flip-flops change state based on their current state and the control

input M, as well as the rising edge of the clock signal. The logic gates ensure that the counter

counts in the specified direction (Up or Down) accurately.

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**Outcomes:**

*Design the combination and sequential circuits using basic building blocks.*

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**Conclusion:**

*We learnt the Implementation of a 3-bit synchronous up counter using JK flip flops on the software called circuit verse.*

**Grade: AA / AB / BB / BC / CC / CD /DD**

**Signature of faculty in-charge with date**

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**References:**

**Books/ Journals/ Websites:**

1. R. P. Jain, “Modern Digital Electronics”, Tata McGraw Hill.
2. <http://www.electronics-tutorials.ws/counter/count_4.html>